N32A003 Series Errata Sheet V1.0.0

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1 Errata List

Errata overview

Errata link		Chip version
		Version B
Section 2: ADC	Section 2.1 : When the ENDC flag is set, immediately read the ADC data register value for abnormal issues	●
Section 3: TIM	Section 3.1: The issue of switching from another mode to 100% or 0% duty cycle PWM mode	●

●: there is this problem -: there is no this problem

Note: The current mass production version is version B

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2 ADC

2.1 When the ENDC flag is set, immediately read the ADC data register value for abnormal issues

Description

After ENDC is set, immediately read the ADC data register, which may read the result of the previous conversion.

Resolution

1.After the ENDC flag is set, delay by 8 ADC_CK clocks before reading the ADC data register;

2.In some scenarios, the ENDCA flag is used instead of the ENDC flag.

3 Timer(TIM)

3.1 The issue of switching from another mode to 100% or 0% duty cycle PWM mode

Description

When switching from any mode (except frozen mode) to PWM1/2 mode, if the PWM duty cycle is set to 100% or 0%, the mode switch to PWM1/2 mode fail, if reconfig the PWM duty (not 0% or 100%), the mode switch to PWM1/2 mode success.

Workaround

When switching from forced active/forced inactive/set channel x to the active level on match/ set channel x to the inactive level on match mode to PWM1/2 mode with a 100% or 0% duty cycle, modify CCxP to achive the PWM with 100% or 0% duty.

When switching from toggle mode to PWM1/2 mode with a 100% or 0% duty cycle, have no solution.

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4 Version history

Date	Version	Remark
2026.3.16	V1.0.0	Initial release

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5 Notice

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