N32A003x5 Product Brief

N32A003 series based on 32-bit ARM Cortex-M0, runup to 48MHz, up to 29.5KB embedded flash, 3KB SRAM, 1x12bit 1Msps ADC, 1xCOMP, 2xUART, 1xI2C, 1xSPI.

Key features

- **Core**
  - A 32-bit ARM Cortex-M0 core, Single-cycle hardware multiply instruction
  - Run up to 48MHz
- **Encrypted memory**
  - Up to 29.5KByte embedded Flash memory, data 100,000 cycling and 10 years retention
  - Up to 3KB SRAM
- **Power consumption mode**
  - Run mode: all peripherals are configurable
  - Stop mode: TIM6, IWDG can be configured to work, SRAM data is maintained, and all IO states are maintained
  - Power Down mode: All power supply off, support NRST, PA1_WKUP0, PA2_WKUP1 wake-up
- **Clock**
  - HSI: Internal high-speed RC OSC 48MHz
  - LSI: Internal low-speed RC OSC 32KHz
  - MCO: Support 1-way clock output, configurable HSI or LSI clock output that can be divided.
- **Reset**
  - Support power-on/power-off/external pin reset
  - Support programmable low voltage detection and reset
  - Support watchdog reset, software reset
- **Communication interface**
  - 2xUART, which supports asynchronous mode, multiprocessor communication mode, single-wire half-duplex mode
  - 1xSPI, rate up to 12MHz
  - 1xI2C, rate up to 1MHz, which can be configured in master/slave mode
- **Analog interface**
  - 1x12bit 1Msps high-speed ADC , up to 9 external single-ended input channels and 1 internal channel connected to the 1.2V reference
  - 1xhigh-speed analog comparator
- **Support up to 18 GPIOs that support multiplexing.**
- **1xBeeper, support complementary output**
- **Timer counter**

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- 1x16-bit advanced timer counters, support input capture, output compare, each timer has 4 independent channels, 3 of which support 6 complementary PWM output
- 1x16-bit general purpose timer counters, each timer has 2 independent channels, supports input capture/output compare/PWM output
- 1x16-bit basic timer counter, supports STOP wake-up low-power mode
- 1x24-bit SysTick
- 1x12-bit Independent watchdog (IWDG)

- **Programming mode**
  - Support SWD online debugging interface
- **Security features**
  - CRC16 calculation
  - Support multiple read protection(RDP) levels (L0/L1/L2)
- **96-bit UID and 128-bit UCID**
- **Working conditions**
  - Operating Voltage Range: 2V~5.5V
  - Operating Temperature Range:
    - ✧ Temperature coefficient 8, -40 ℃~125 ℃, certified by AEC-Q100-G1
    - ✧ Temperature coefficient 7, -40 ℃~105 ℃, certified by AEC-Q100-G2
- **Package**
  - QFN20(3mm x 3mm, 0.5mm pitch)

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1 Part number information

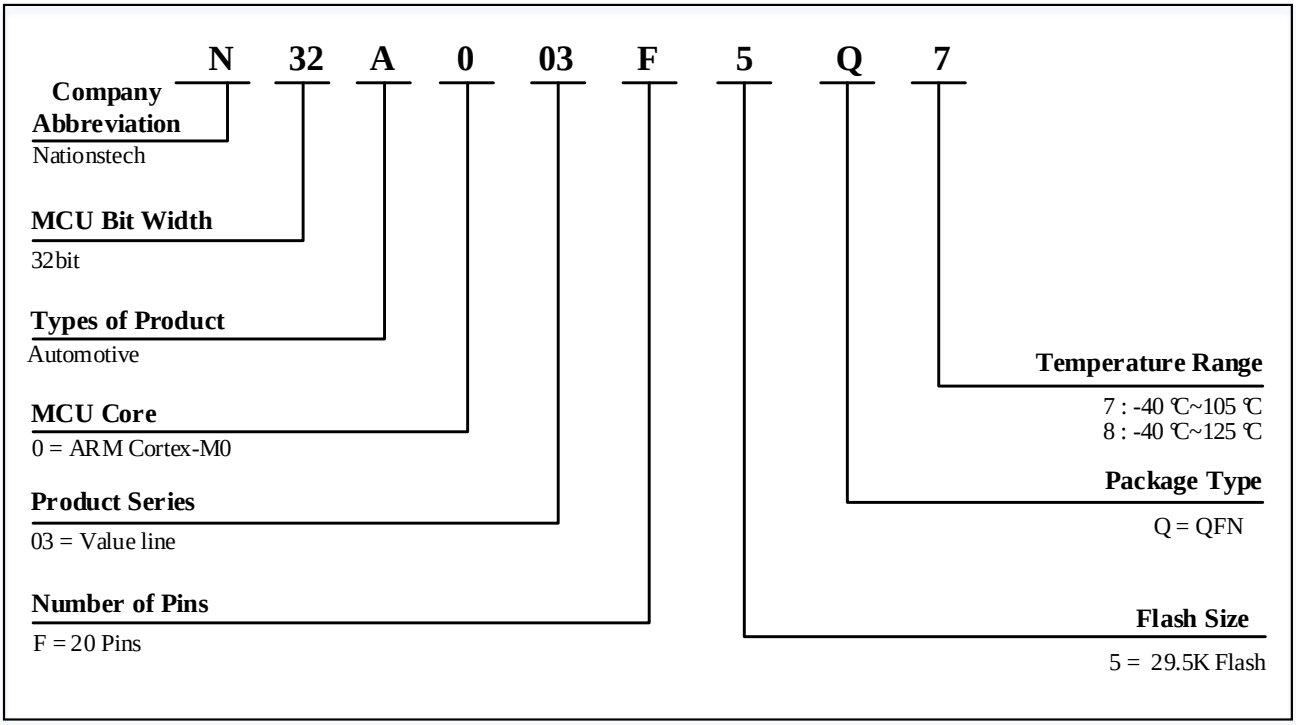

Table 1-1 N32A003 Series Ordering Code information

Ordering Code[1]	Package	Size	Packaging[2]	SPQ[3]	Temperature range
N32A003F5Q7	QFN20	3mm x 3mm	Tray	490	-40℃ ~ 105℃
			Reel	5000	
N32A003F5Q8	QFN20	3mm x 3mm	Tray	490	-40℃ ~ 125℃
			Reel	5000	

1. For the latest detailed ordering information, please refer to the selection manual.
2. This packaging is the basic packaging. If you have any other requirements, please contact Nsing Technology
3. Minimum packaging quantity

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2 Product Model Resource Configuration

Table 2-1 N32A003 Series Resource Configuration

Part Number		**N32A003F5Q7**	**N32A003F5Q8**
Flash capacity (KB)		29.5	29.5
SRAM capacity (KB)		3	3
CPU frequency		ARM Cortex-M0 @ 48MHz	ARM Cortex-M0 @ 48MHz
Working environment		2~5.5V/-40~105℃	2~5.5V/-40~125℃
Timer	General	1	1
	Advanced	1	1
	Basic	1	1
Communication interface	SPI	1	1
	I2C	1	1
	UART	2	2
GPIO		18	18
12bit ADC		1x12bit 9Channel	1x12bit 9Channel
COMP		1	1
Beeper		1	1
Algorithm support		CRC16	CRC16
Security protection		Read protection（RDP）	Read protection（RDP）
Package		QFN20(3x3mm, 0.4mm pitch)	QFN20(3x3mm, 0.4mm pitch)

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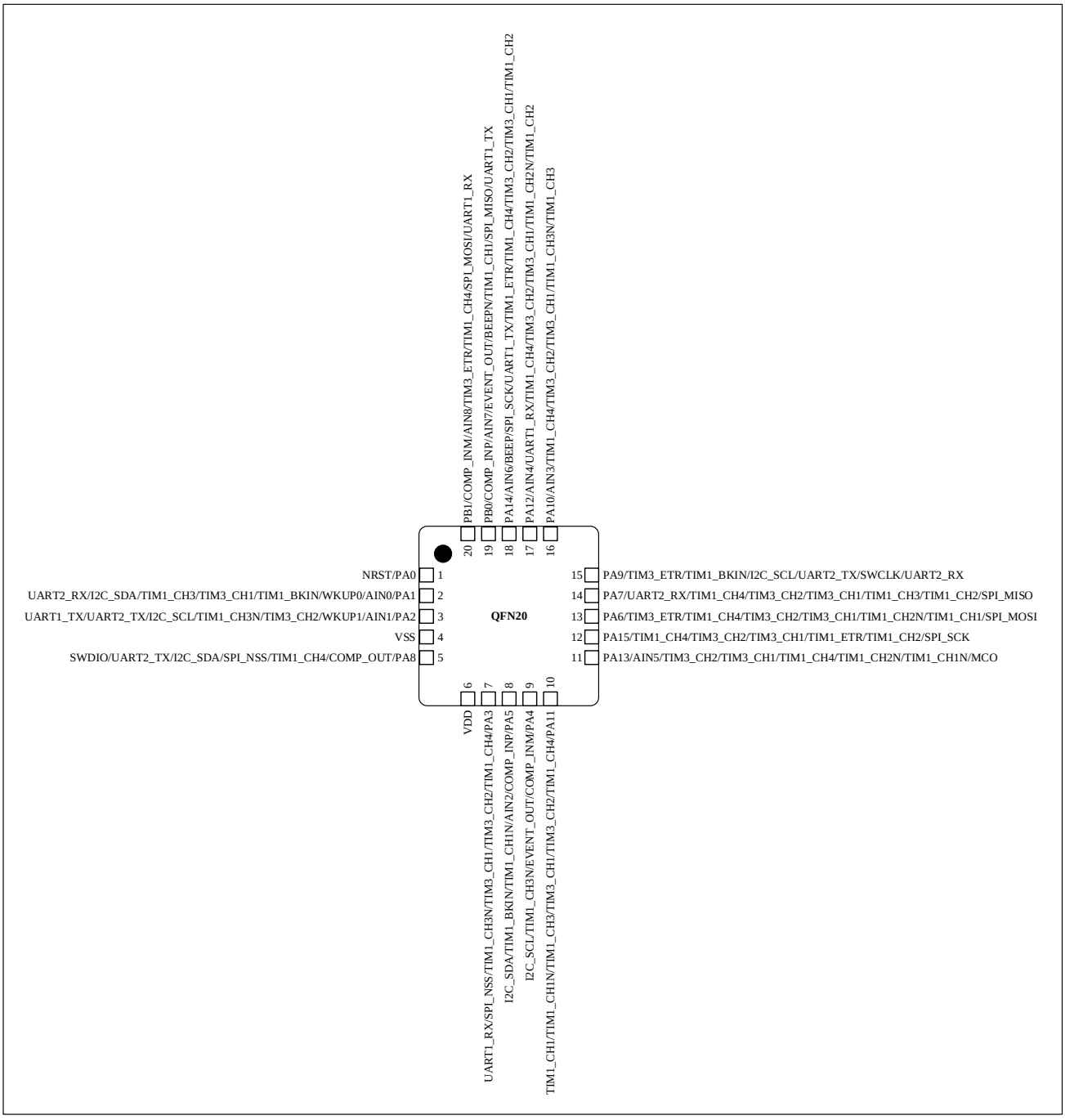
3 Package Information

3.1 QFN20

3.1.1 QFN20 Pinout



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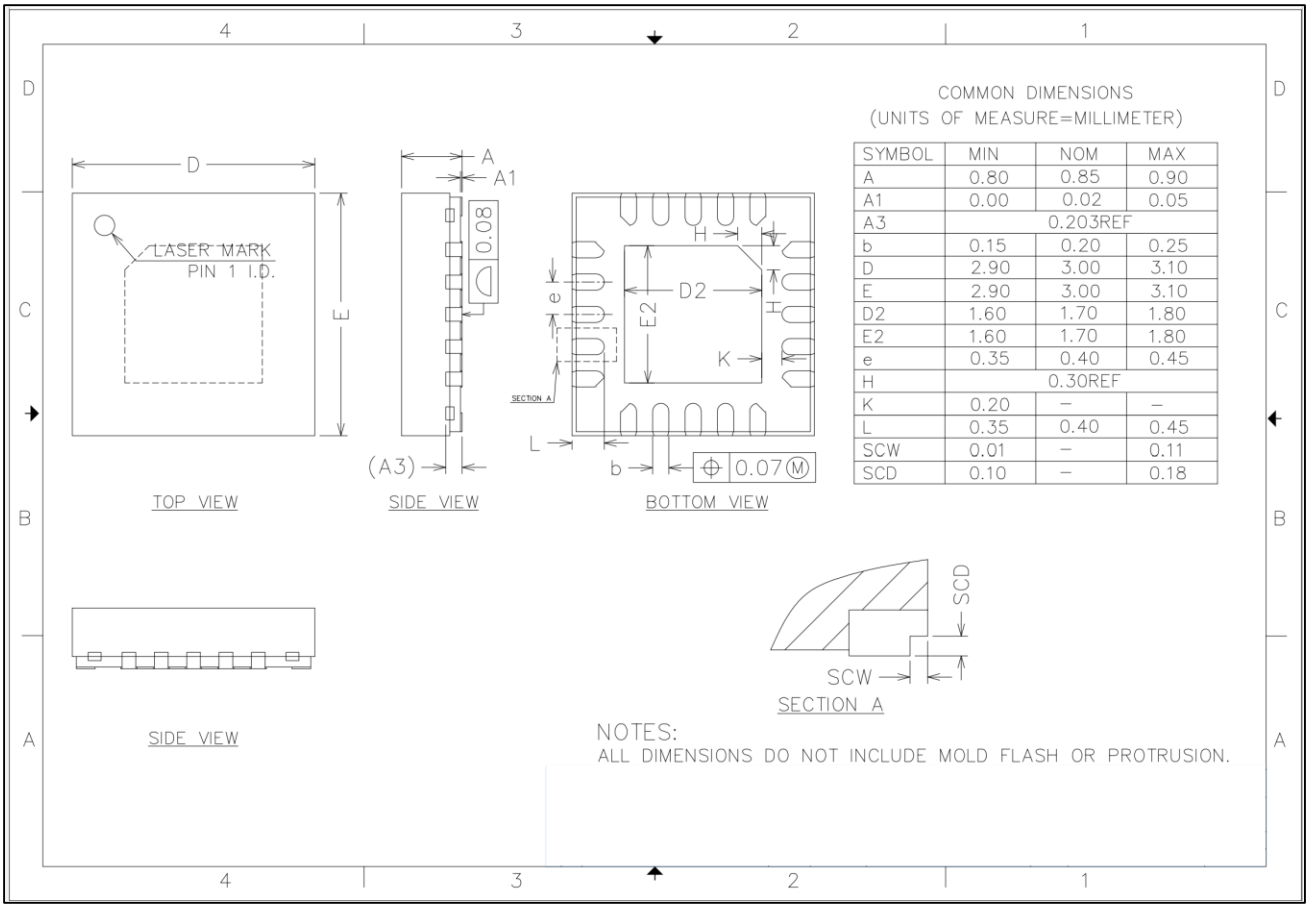
3.1.2 QFN20 Package



4 Version history

Date	Version	Remark
V1.0.0	2026.3.24	Initial release

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5 Notice

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