

User Guide

N32H785XIB7_STB Development Board Hardware User Guide

Introduction

The purpose of this document is to enable users to quickly familiarize themselves with the N32H785XIB7_STB development board, understand its functions, usage instructions, and precautions, so as to conduct MCU debugging and development based on the development board.

Table of contents

1.	HARDWARE DEVELOPMENT NOTES.....	1
1.1	<i>Brief.....</i>	<i>1</i>
1.2	<i>Development board functions</i>	<i>1</i>
1.3	<i>Development board layout.....</i>	<i>2</i>
1.4	<i>Development Board Jumper Usage Instructions</i>	<i>5</i>
1.5	<i>Development board schematic.....</i>	<i>6</i>
2.	HISTORICAL VERSIONS	12
3.	NOTICE.....	13

1. Hardware Development Notes

1.1 Brief

The N32H785XIB7_STB development board is used for sample development of NSING TECHNOLOGIES INC. 32-bit N32H785XIB7 chip. This document details the functions, usage instructions, and precautions of the N32H785XIB7_STB development board.

1.2 Development board functions

The main MCU chip on the development board is N32H785XIB7, in a BGA240 package. The development board provides all functional interfaces for customer development.

1.3 Development board layout

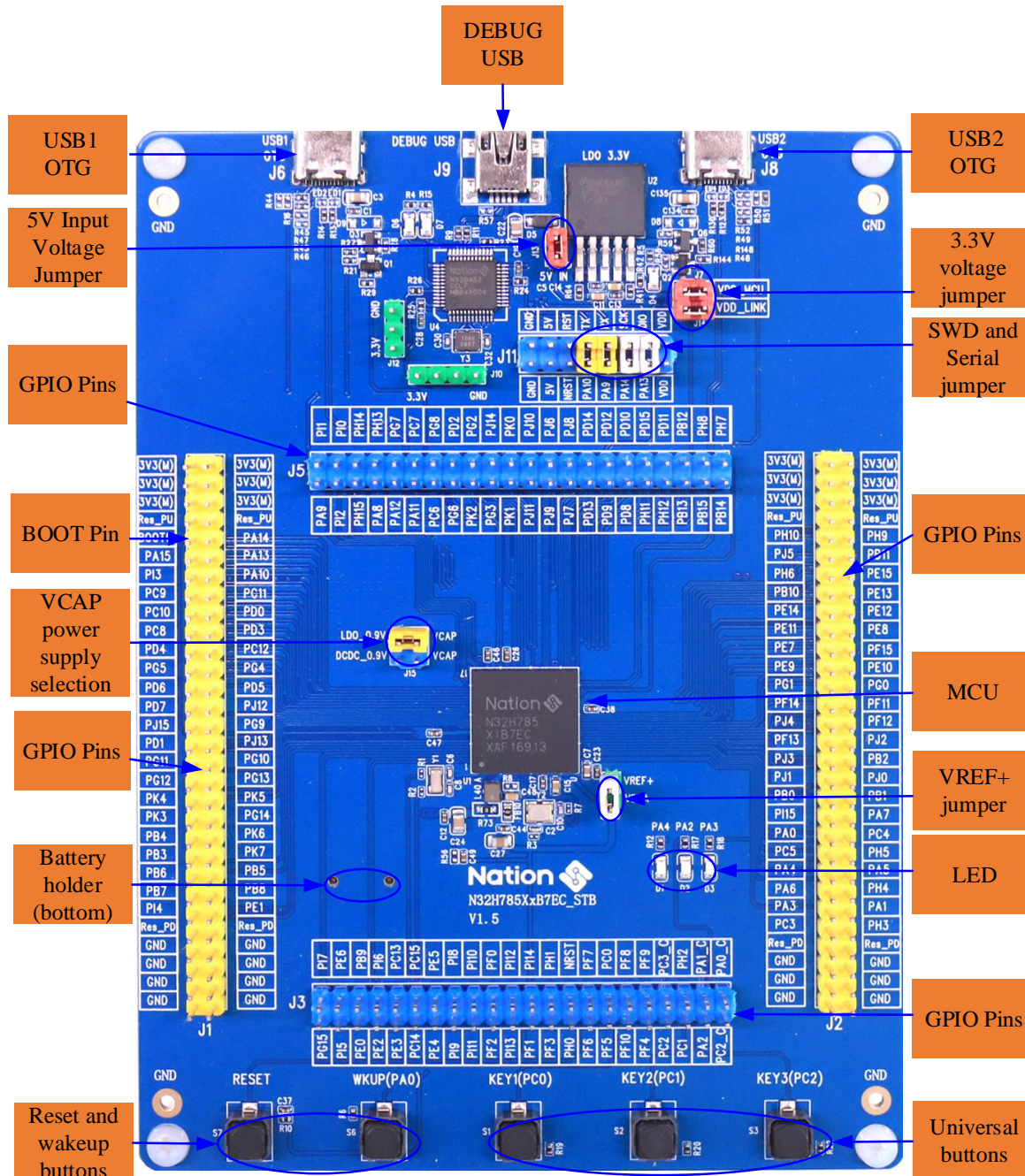


Figure 1-1 Development board layout

1) Power supply for development board

The development board can be powered via a USB1 OTG interface (J6), a USB2 OTG interface (J8), and a DEBUG USB (J9), and is connected to the 3.3V LDO input port via jumper J13.

2) Debug USB (J9)

The NS-LINK chip (U4) provides a DEBUG USB interface for downloading and debugging the main MCU program, and can also be connected to the MCU's serial port to provide a USB-to-serial function.

3) USB OTG (J6 , J8)

The development board has two onboard USB OTG interfaces (J6 and J8), which enable upgrades and debugging between master and slave devices.

4) SWD interface and serial port (J11)

SWD Interface: PA13 (SWDIO) and PA14 (SWDCK) are used for downloading and debugging the main MCU program. ULINK2 or JLINK can be used to download and debug the MCU, or jumpers can be used to short the SWDIO and SWDCK signal pins to download and debug the MCU via DEBUG USB.

Serial ports: MCU_TX and MCU_RX are used as external serial signals. PA9 (TX) and PA10 (RX) of the MCU are used as serial ports. They can be used to connect serial devices independently, or jumpers can be used to short the MCU_TX and MCU_RX signal pins to convert the USB port to a serial port via the NS-LINK on the development board for customer convenience.

5) Reset and wake-up buttons (S7, S6)

S7 and S6 are the reset and wake-up buttons, respectively, connected to the chip's NRST and PA0 pins, and used for chip reset and wake-up functions.

6) General-purpose buttons (S1, S2, S3)

S1, S2, and S3 are general-purpose buttons, which are connected to the PC0, PC1, and PC2 pins of the chip, respectively.

7) LED

D1, D2, and D3 are LEDs, which are connected to pins PA4, PA2, and PA3 of the chip, respectively.

8) BOOT (J1 PIN9)

J1 PIN9 is the BOOT0 connector, which can be shorted to power or ground via a jumper as needed.

9) GPIO ports (J1, J2 , J3 , J5)

All GPIO interfaces of the chip are brought out, with 3.3V and GND pins provided, as well as pull-up and pull-down pins with series resistors for easy testing. For detailed definitions of the GPIO interfaces, please refer to the "UM_N32H78X Series User Manual".

1.4 Development Board Jumper Usage Instructions

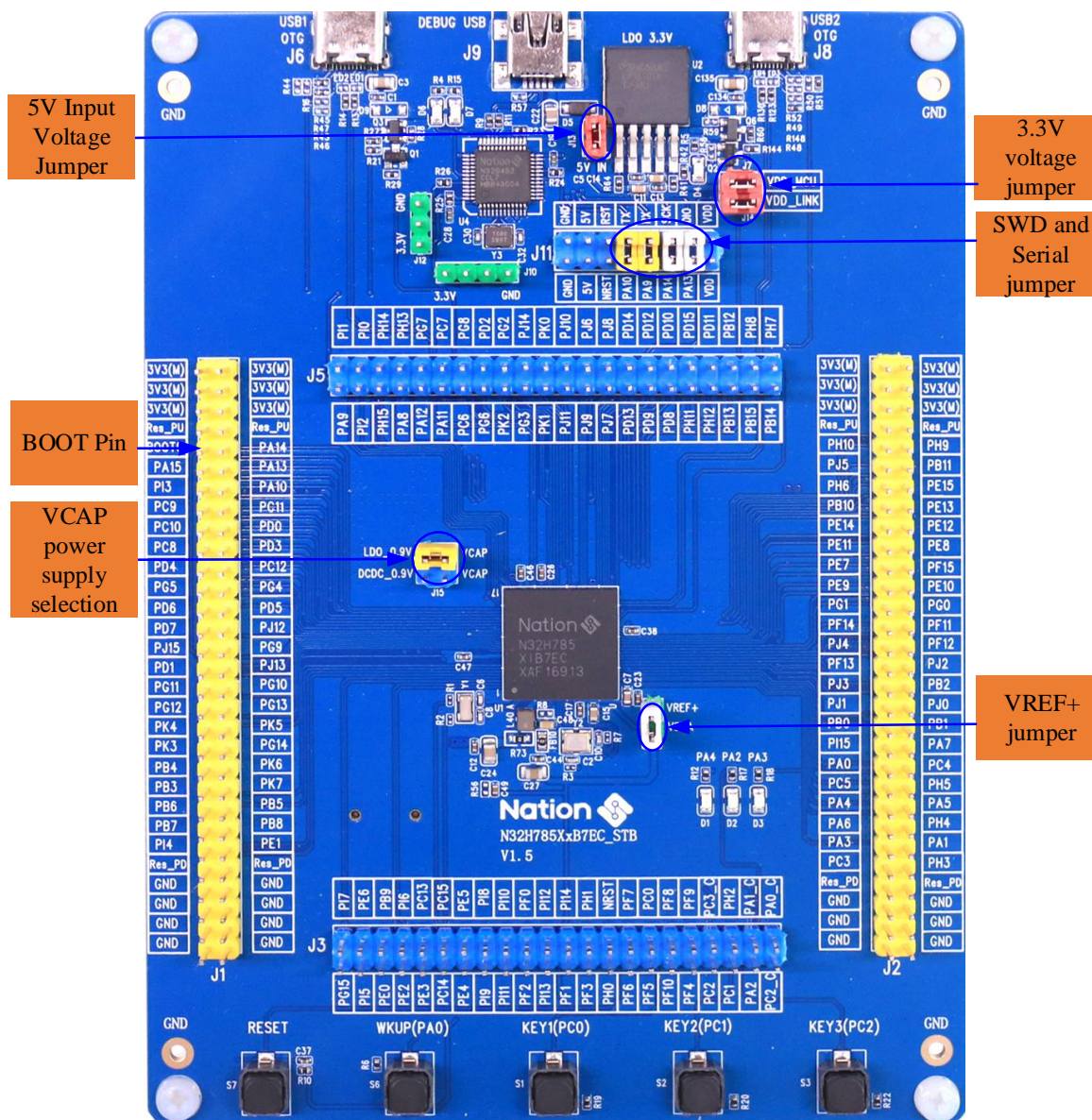


Figure 1-2 Development board jumper instructions

surface 1-1 Development Board Jumper Specifications

No.	jumper number	Jumper function	Instructions for use
1	J13	5V input voltage jumper	The J13 jumper is used to connect the three USB OTG (J6, J8) and DEBUG USB (J9) interfaces to the 3.3V LDO input port.
2	J7, J14	3.3V power supply jumper	J7: 3.3V power supply to the main MCU chip. J14 : 3.3V power supply to the NS-LINK MCU chip.
3	J11	SWD jumper	To download the program to the MCU using NS-LINK via the USB DEBUG port, you need to short the SWDIO and SWDCK signal pins.
	J11	Serial jumper	When using NS-LINK as a serial port via the USB DEBUG port, it is necessary to short the MCU_TX signal pin and the MCU_RX signal pin.
4	J1 PIN9	BOOT jumper	J1 PIN9: BOOT0.
5	J4	VREF+ jumper	J4: Shorting this jumper allows VREF to use the external VDD_MCU voltage as a reference source.
6	J15	VCAP power supply selection	Based on the silkscreen markings on pin J15, you can select either LDO_0.9V or DCDC_0.9V to power the VCAP.

1.5 Development board schematic

The schematic diagram of the N32H785XIB7_STB development board is described below (see "N32H785XIB7_STB_V1.5" for details):

1) MCU connection

Referring to Figure 1-3, which shows the MCU connection schematic, each VDD pin of the MCU is connected to a capacitor, and all GPIO pins are led out and connected to the J1, J2, J3, and J5 pins for easy debugging.

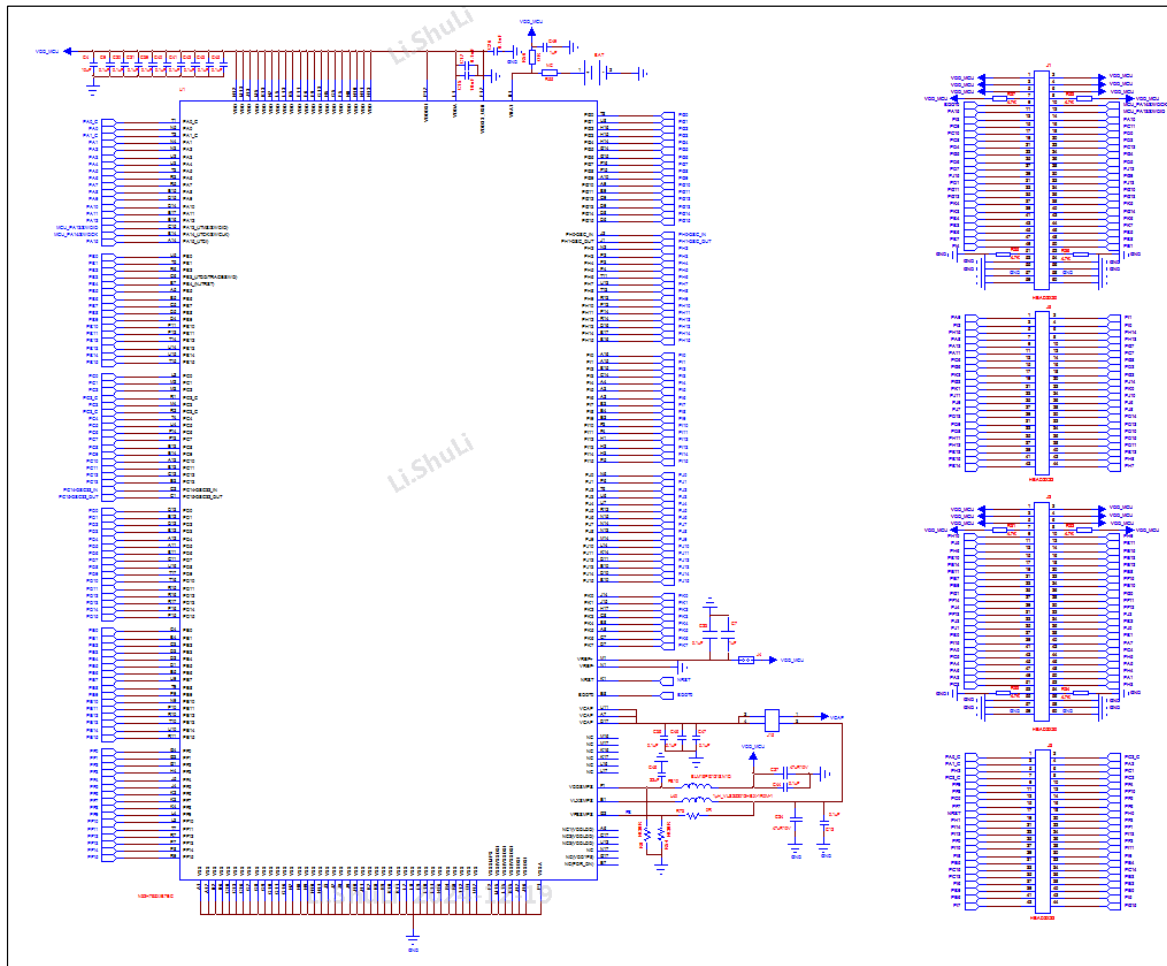
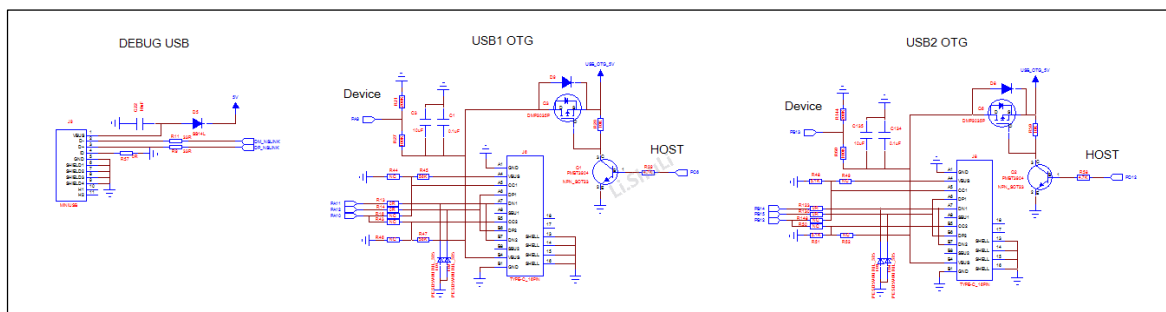


Figure 1-3 MCU connection diagram

2) Power supply design

Referring to Figure 1-4, which shows the power supply design schematic, the development board can be powered at 5V via USB OTG (J6, J8) or DEBUG USB (J9), and then the LDO outputs 3.3V to power the entire PCB board.



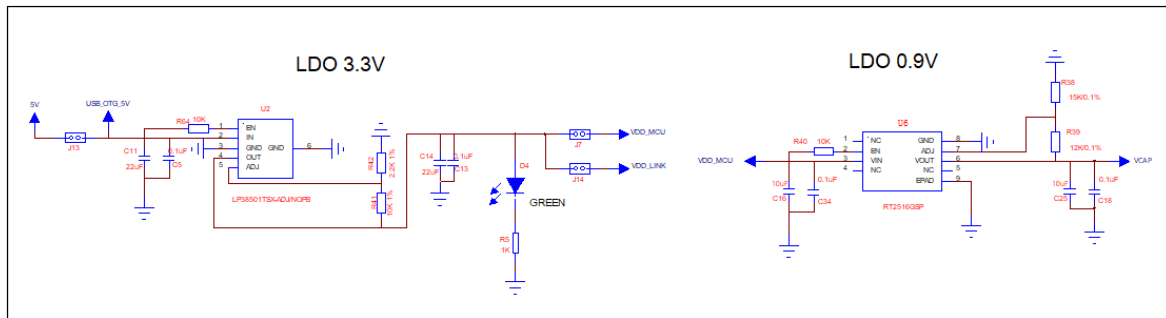


Figure 1-4 Power supply design

3) Button Design

Referring to Figure 1-5, which shows the button design schematic, there are a total of 5 buttons: 3 general-purpose buttons, an MCU wake-up button, and a reset button.

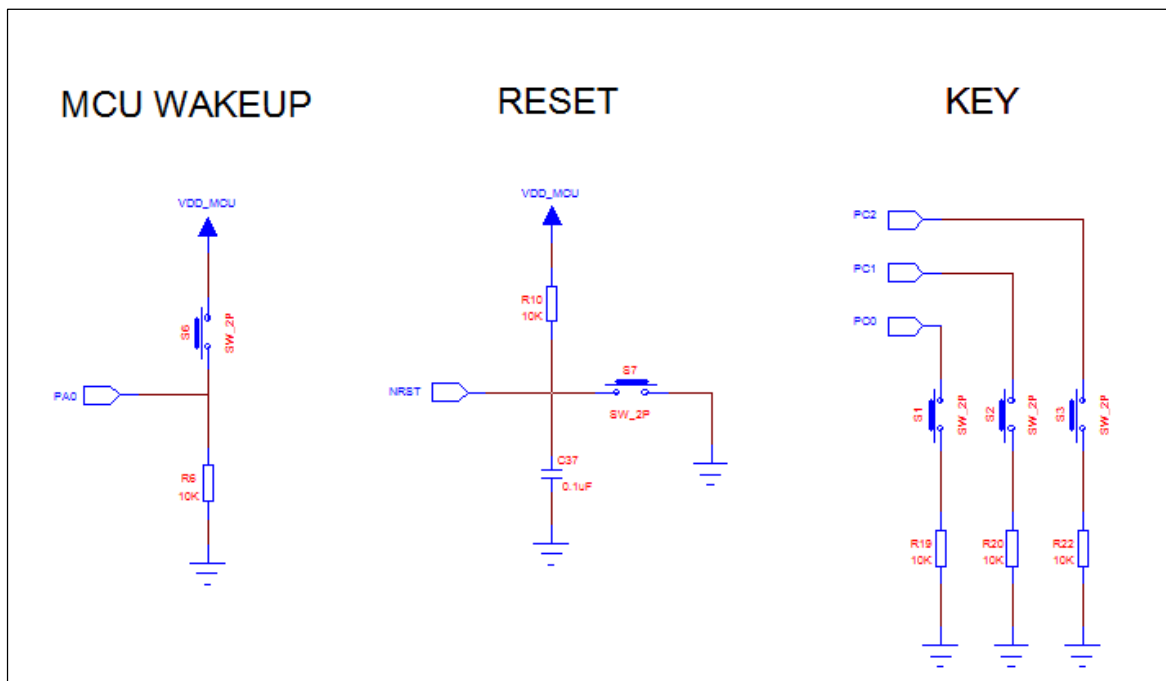


Figure 1-5 Button Design

4) LED design

Referring to Figure 1-6, which shows the schematic diagram of the LED design, there are a total of 5 LEDs. D1, D2, and D3 are connected to PA4, PA2, and PA3 of the main MCU, respectively, and can be used for debugging. D6 and D7 are used for NS-LINK MCU control to monitor the NS-LINK's operating status.

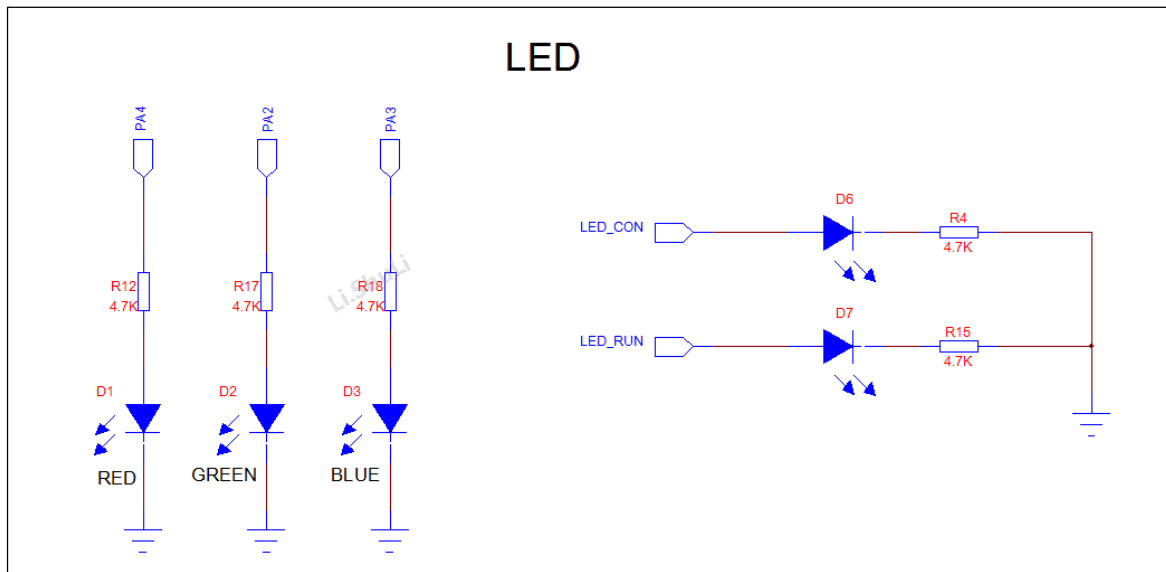


Figure 1-6 LED design

5) crystal

Referring to Figure 1-7, which shows the crystal connection diagram, the chip has two external crystals, one at 32.768 kHz and the other at 25 MHz.

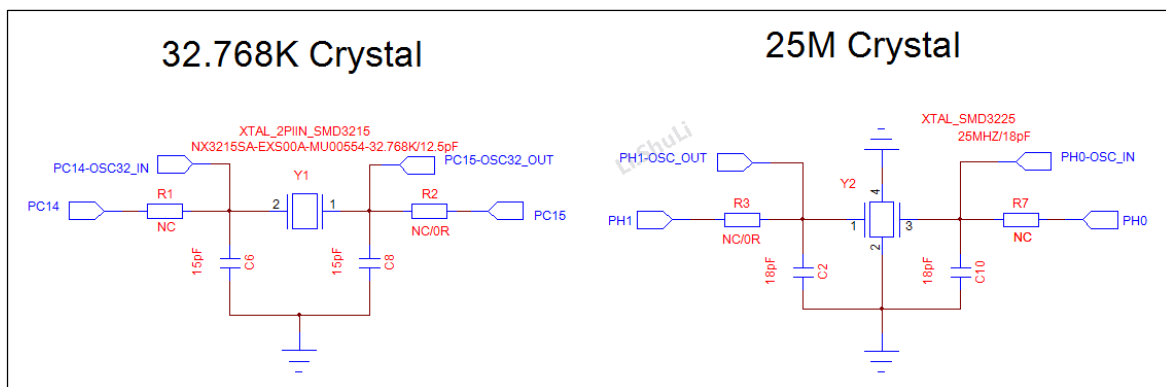


Figure 1-7 Crystal Design

6) BAT

Referring to Figure 1-8, which shows the schematic diagram of an external BAT battery, the VBAT pin can be powered by an external CR1220 battery connected to the PCB board via an external battery holder, or directly via VDD.

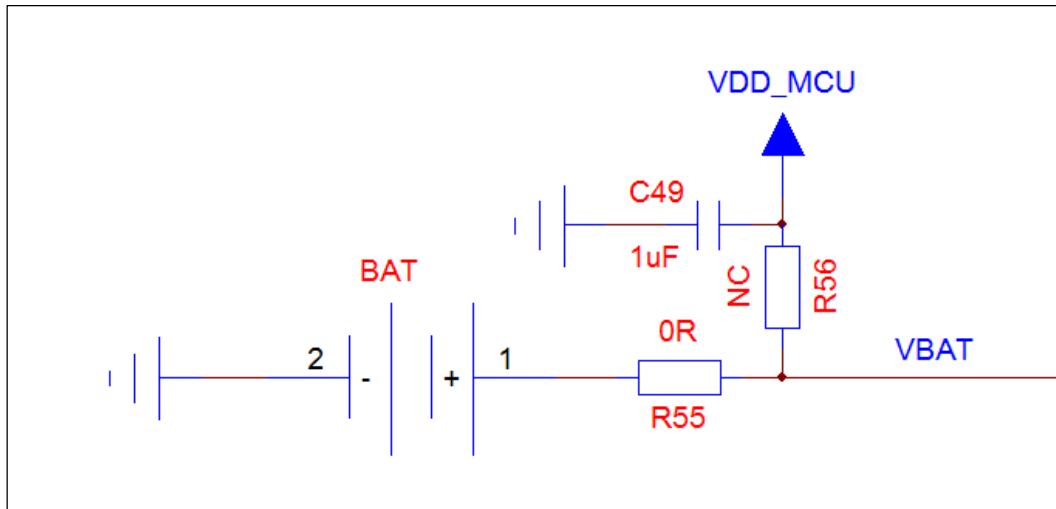


Figure 1-8 BAT

7) NS-LINK

Referring to Figure 1-9, which shows the NS-LINK schematic, users can directly connect a USB cable via the DEBUG USB port to download programs, eliminating the need for a ULINK or JLINK programmer. Debugging can also be performed via the DEBUG USB port, which simulates a serial port.

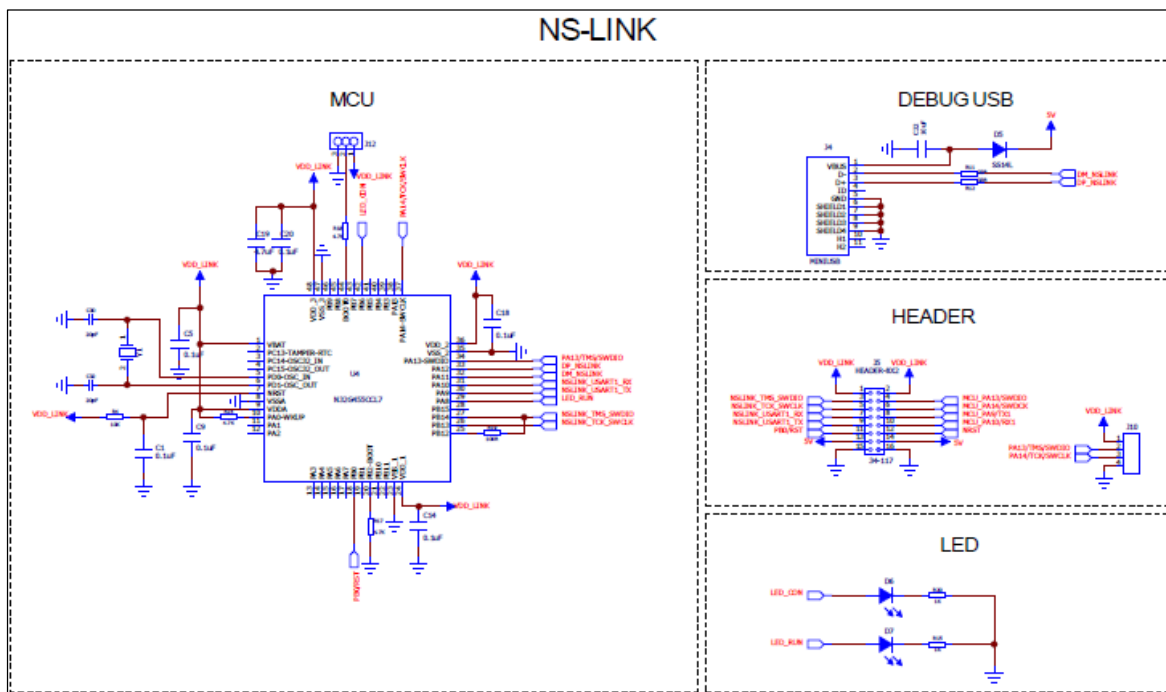


Figure 1-9 NS-LINK

- **MCU Peripheral Components Description:**

- 1) When designing the PCB layout, for VDD power supply, place two decoupling capacitors (10uF + 0.1uF) near the chip, and then place a 0.1uF decoupling capacitor near each VDD pin.
- 2) It is recommended to place a 0.1uF and a 10uF capacitor on the VDDA input pin.
- 3) When VREF+ uses the built-in reference source VREFBUF, it is recommended to place a 0.1uF and a 1uF capacitor near the VREF+ pin. When VREF+ is externally powered, it is recommended to place a 0.1uF and a 10uF capacitor near the VREF+ pin.
- 4) PC14-OSC32_IN, PC15-OSC32_OUT: If an external high-precision RTC clock is required, a 32.768kHz crystal needs to be connected close to the pins. Otherwise, this step is not necessary.

2. Historical Versions

Version	Date	Remark
V1.3	2024-10-10	Create document
V 1.5	2025-8-10	1. Update the 0.9V LDO model to: RT2516GSP

3. Notice

This document is the exclusive property of NSING TECHNOLOGIES PTE. LTD. (Hereinafter referred to as NSING). This document, and the product of NSING described herein (Hereinafter referred to as the Product) are owned by NSING under the laws and treaties of Republic of Singapore and other applicable jurisdictions worldwide. The intellectual properties of the product belong to NSING Technologies Inc. and NSING Technologies Inc. does not grant any third party any license under its patents, copyrights, trademarks, or other intellectual property rights. Names and brands of third party may be mentioned or referred thereto (if any) for identification purposes only. NSING reserves the right to make changes, corrections, enhancements, modifications, and improvements to this document at any time without notice. Please contact NSING and obtain the latest version of this document before placing orders. Although NSING has attempted to provide accurate and reliable information, NSING assumes no responsibility for the accuracy and reliability of this document. It is the responsibility of the user of this document to properly design, program, and test the functionality and safety of any application made of this information and any resulting product. In no event shall NSING be liable for any direct, indirect, incidental, special, exemplary, or consequential damages arising in any way out of the use of this document or the Product. NSING Products are neither intended nor warranted for usage in systems or equipment, any malfunction or failure of which may cause loss of human life, bodily injury or severe property damage. Such applications are deemed, Insecure Usage'. Insecure usage includes, but is not limited to: equipment for surgical implementation, atomic energy control instruments, airplane or spaceship instruments, all types of safety devices, and other applications intended to supporter sustain life. All Insecure Usage shall be made at user's risk. User shall indemnify NSING and hold NSING harmless from and against all claims, costs, damages, and other liabilities, arising from or related to any customer's Insecure Usage Any express or implied warranty with regard to this document or the Product, including, but not limited to. The warranties of merchantability, fitness for a particular purpose and non-infringement are disclaimed to the fullest extent permitted by law. Unless otherwise explicitly permitted by NSING, anyone may not use, duplicate, modify, transcribe or otherwise distribute this document for any purposes, in whole or in part.