

NP11 Series

Datasheet

The NP11 is a highly integrated, cost-effective fast-charging protocol chip supporting USB Type-C Power Delivery (PD) or Type-A single-port charging. It integrates a high-performance processor and programmable Flash memory. The chip includes CC/CV control loop, bidirectional discharge circuits, multiple system protection features. With its high level of integration and minimal external components, it provides a low-cost, complete solution for power adapters, car chargers, and other fast-charging devices.

1 Key Features

- Core MCU
 - 32-bit ARM Cortex-M0 core
 - Up to 48MHz
- Memory
 - 29.5K bytes Flash
 - 3K bytes SRAM
- Fast Charging Protocol
 - Support PD2.0 / PD3.1 (SPR/PPS), up to **100W (20V@5A)**
 - Support QC2.0 / QC3.0 (Class A / Class B)
 - Support UFCS unified fast charging protocol
 - Support Apple 2.4A charging
- Interfaces
 - Integrated Type-C interface logic
 - Supports DRP (Dual Role Port)
 - Supports E-marker
 - Supports USB BC1.2 and HVDCP modes
- Power Management
 - Wide input voltage: **3V~28V**
 - Support
 - OPTO Optocoupler regulation
 - FB feedback regulation
 - I2C regulation
 - Integrated CC/CV loop
 - Integrated VPWR/VBUS bidirectional discharge

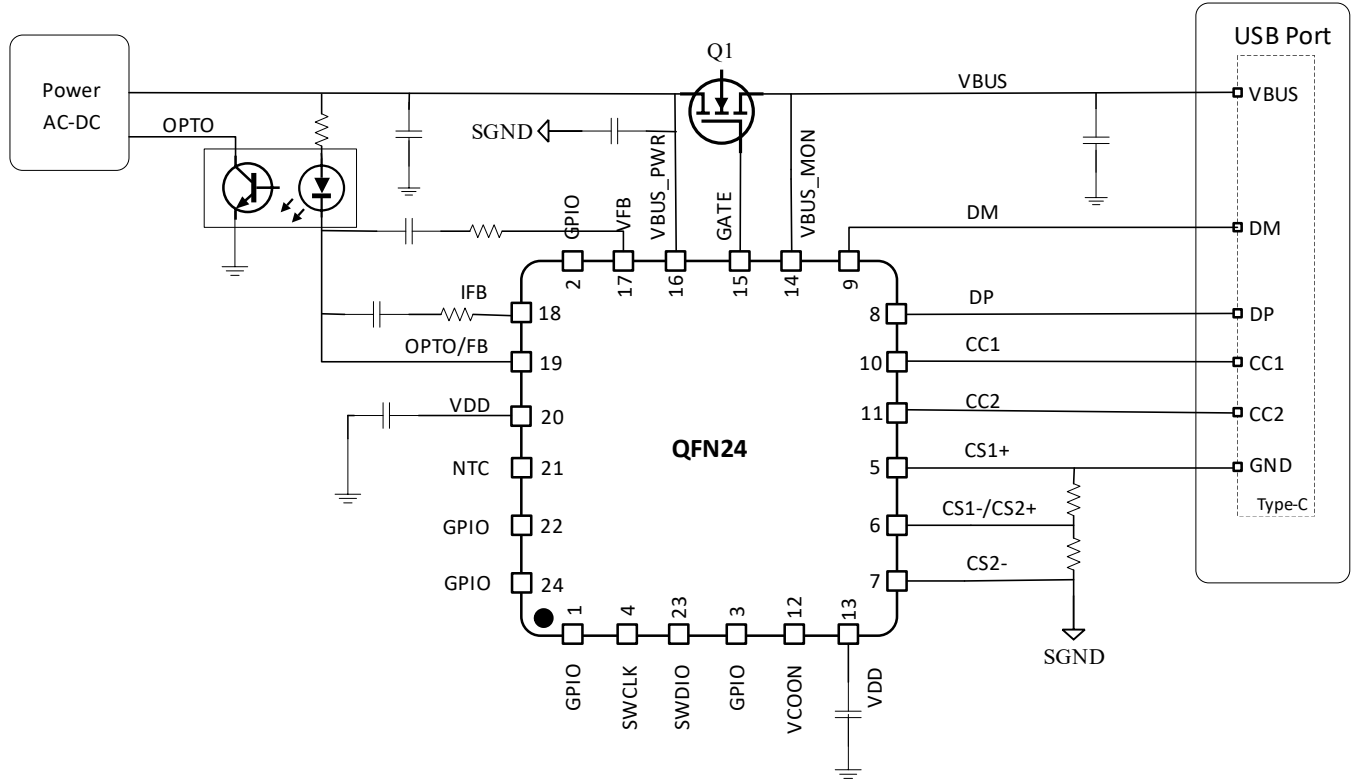
- Supports minimum 5mΩ current sensing resistor
- Compliant with LPS safety certification
- **Protection Features**
 - Output over-voltage protection (OVP)
 - Output under-voltage protection (UVP)
 - Output over-current protection (OCP)
 - NTC over-temperature protection
 - Chip over-temperature protection
 - CC / DM / DP over-voltage protection
 - Output current limiting
- **System Control**
 - Support NMOS high-side driver
 - Integrated VPWR/VBUS discharge
 - Supports switch between OPTO / FB / I2C regulation modes
 - Programmable, supports vendor customization and authentication
- **Operating Modes**
 - Normal Mode: <6mA
 - Sleep Mode: <200uA
- **Debug & Upgrade**
 - Supports SWD / online debugging
 - Supports firmware upgrade via USB (optional)
- **Operating Conditions**
 - Voltage: 3V ~ 25V
 - Temperature: -40°C ~ 105°C
- **Package**
 - QFN24 (4mm x 4mm)

2 Applications

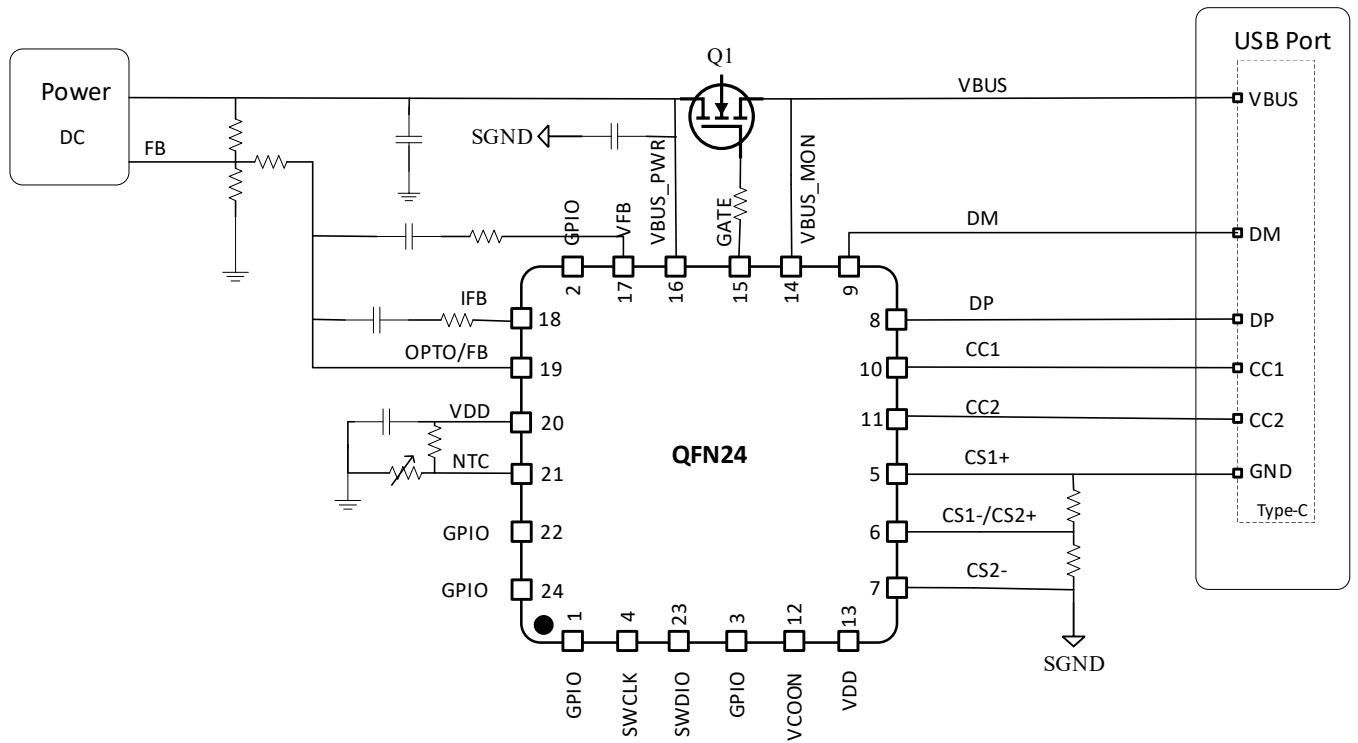
- AC Adapters
- Car Chargers
- Power Strips
- Power tool battery packs
- Other PD fast-charging devices

3 Application Diagram

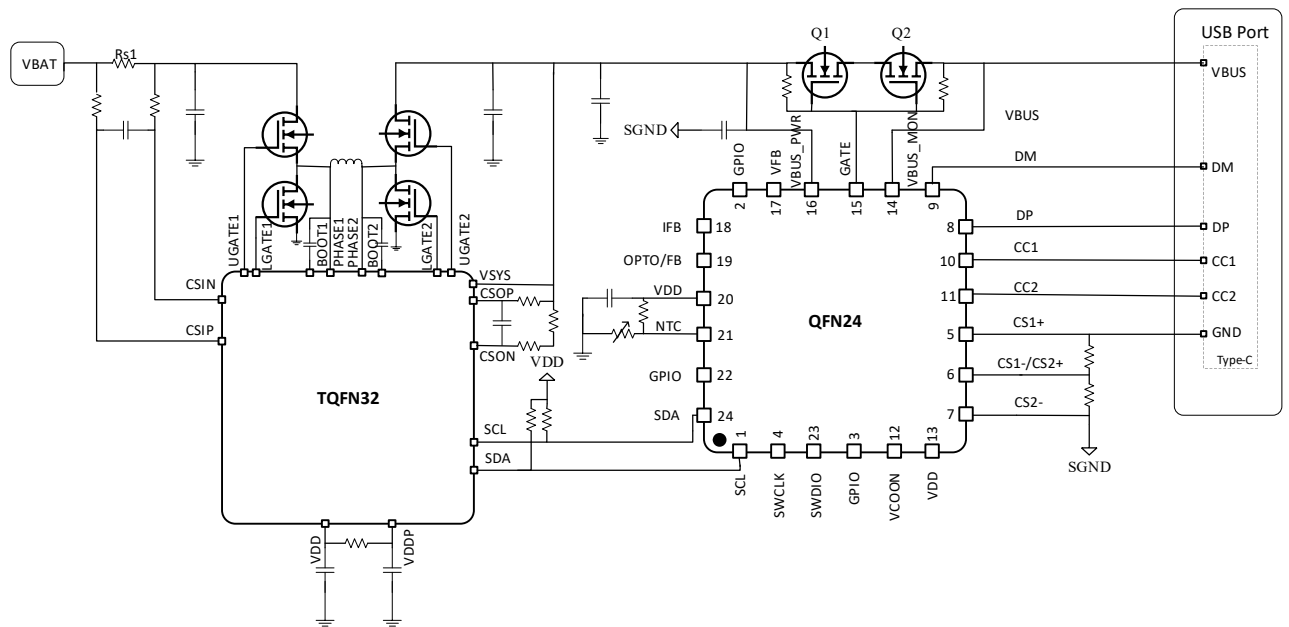
3.1 AC-DC block diagram



3.2 DC-DC block diagram 1

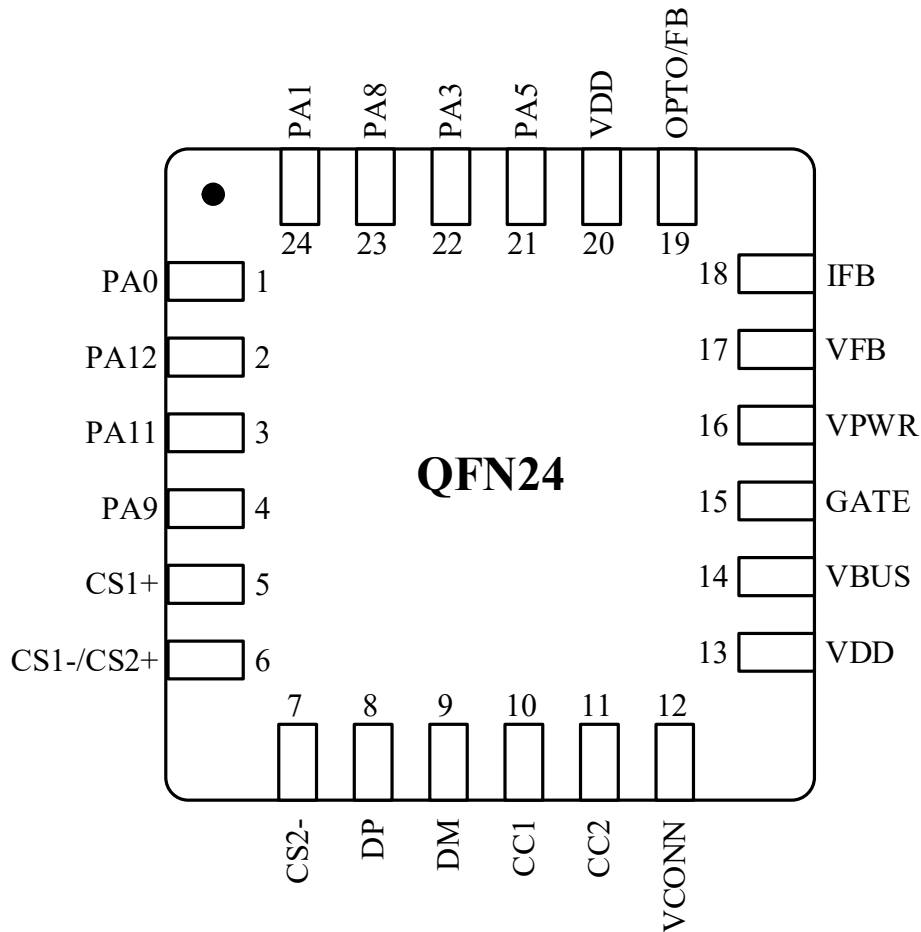


3.3 DC-DC block diagram 2



4 Pinout

4.1 Pinout



4.2 Pin list

No.	Name	Description
1	PA0	GPIO
2	PA12	GPIO/ADC
3	PA11	GPIO

4	PA9	GPIO/SWCLK
5	CSP1	Current sense (positive)
6	CSN1/CSP2	Current sense (negative)
7	CSN2	Current sense (positive)
8	DP	USB D+
9	DM	USB D-
10	CC1	USB CC1
11	CC2	USB CC2
12	VCONN	E-marker power
13	VDD	VDD
14	VBUS	VBUS Output
15	GATE	External NMOS driver
16	VPWR	Power Input
17	VFB	CV loop compensation
18	IFB	CC loop compensation
19	OPTO	Optocoupler drive
20	VDD	VDD
21	PA5	GPIO / ADC
22	PA3	GPIO
23	PA8	GPIO / SWDIO
24	PA1	GPIO / ADC

5 Electrical Specifications

5.1 Absolute maximum ratings

Parameter		Min	Max	Unit
Voltage	VPWR, VBUS, VREG, GATE, CC1, CC2, OPTO	-0.3	28.0	V
	CS1-, CS1+, CS2-, CS2+, VFB, IFB, DP, DM	-0.3	7	V
T _J		-40	125	°C
Storage Temperature		-40	150	°C

Exceeding limits may cause permanent damage.

5.2 Electrical Characteristics

VPWR = 5V to 21V, T_{AMB} = 25°C

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
VPWR Section						

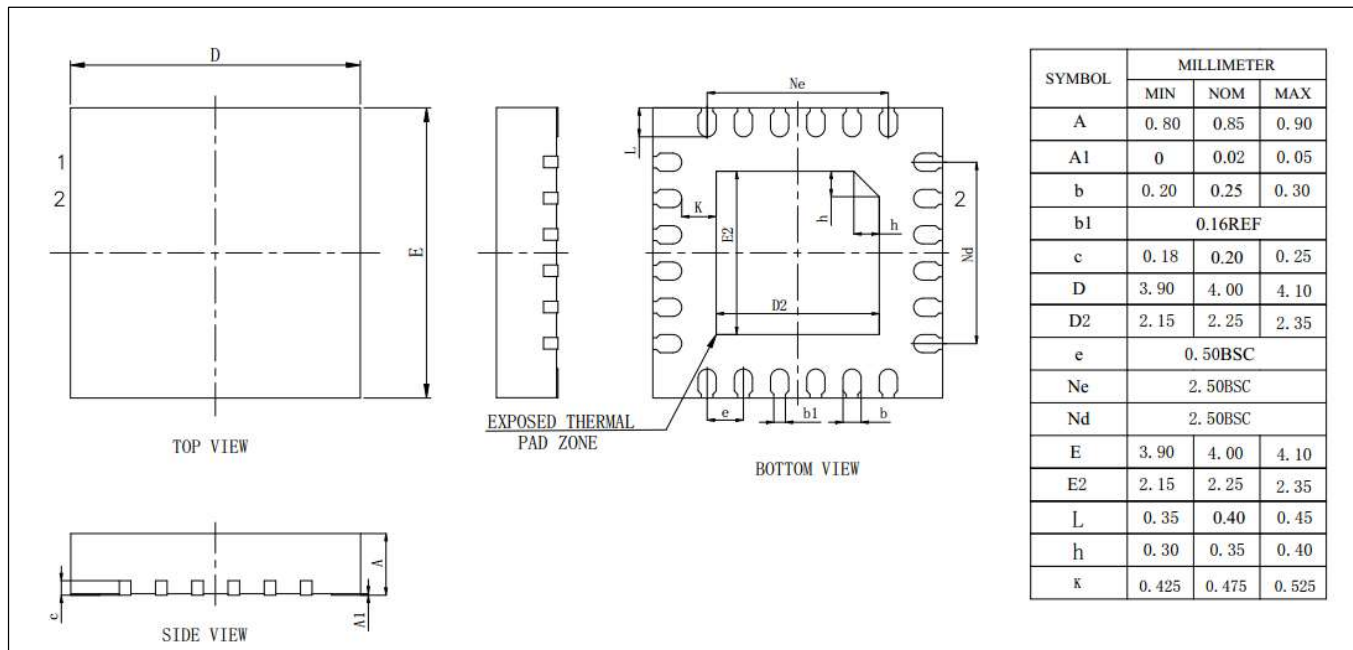
V _{PWR_MAX}	Max input supply voltage			20	28	V
V _{PWR_ON}	VPWR UVLO Threshold			3		V
I _{PWR_OP}	Normal Operating Current	VPWR=5V, VBUS=5V, in normal mode, SR driver is disabled.		3	4	mA
I _{PWR_LP}	Low Power Current	VPWR=5V, VBUS=5V, in sleep mode, CC1/CC2 pin floating.		200	350	μA
		VPWR=5V, VBUS=5V, LP mode, CC1/CC2 pin 5.1kΩ pull down.		400	500	μA
T _{DB_LP}	Low power switching time		100			ms
V _{REG}			3.234	3.3	3.366	V
VPWR Protection						
V _{PWR_OVP}	OVP threshold			00	+110%	V
				01	+115%	
				10	+120%	
				11	+125%	
V _{PWR_UVP}	UVP threshold			000	55%	V
				001	60%	
				010	65%	
				011	70%	
				100	75%	
				101	80%	
				110	85%	
				111	90%	
OCP (Current Through VPWR to VBUS)						
I _{OCP}	OCP threshold			000	105%	A
				001	110%	
				010	112.5%	
				011	115%	
				100	117.5%	
				101	120%	

			110	125%			
			111	130%			
BC1.2 Interface Section							
R _{DM_DWN}	D- pull-down resistor		14.25		24.5	kΩ	
R _{DCP_DAT}	D+ D- short resistor	D+ to D- Short VD+=VD-=0.6V		20	40	Ω	
R _{DP_DWN}	D+ pull-down resistor (reference ON, SLG)		0	300		1100	kΩ
			1	14.25	20	24.5	kΩ
VD+, VD- OVP							
V _{D+_OVP}	D + OVP threshold		4.5	4.75	5	V	
V _{D-_OVP}	D - OVP threshold		4.5	4.75	5	V	
Type-C CC1 and CC2							
I _{RP_SRC}	CC1/CC2 Advertised Current	3A DFP mode: $0 \ll V_{CCX} \ll 2.5V$	11	304	330	356	μA
		1.5A DFP mode: $0 \ll V_{CCX} \ll 1.5V$	10	166	180	194	
		Default USB Power	01	72	80	88	
		Disable	00	High Impedance			
V _{CC_CD_RD}	CC1/CC2 Plug / Unplug detection threshold.		1	2.55	2.60	2.75	V
			0	1.55	1.60	1.75	V
CC1 and CC2 OVP							
V _{CC_OVP}	CC1/CC2 OVP threshold		5.225	5.5	5.775	V	

CC1 and CC2 VCONN						
VCONN			4	4.5	4.8	V
Apple 2.4A Charging Mode						
V _{DAT_2P7V}	D+/D- Output voltage		2.57	2.7	2.84	V
R _{DAT_2P7V}	D+/D- Output Impedance			30		kΩ
Internal Discharge Section						
I _{DSCHG_VPWR}	V _{PWR} Internal discharge current		20	80	120	mA
I _{DSCHG_VBUS}	V _{BUS} Internal discharge current		15	20	25	mA
OPTO Section						
I _{OPTO_MAX}	Opto drive current		2		10	mA
CS- Section						
R _{SNS}	Current sense resistance		4.95	5	5.05	mΩ
K_{CBL} : Cable Drop Compensation Section						
K _{CBL}	VBUS Line Compensation	000	Disable			mV/A
		001	67.5	75	82.5	
		010	90	100	110	
		011	135	150	165	
		100	180	200	220	
		101	225	250	275	
		110	270	300	330	
		111	315	350	385	
Voltage Loop DAC Reference						
N _{DAC_CV}	CV DAC resolution			11		bit
V _{CVDAC_STEP}	CV DAC step size			10		mV

Current Loop DAC Reference						
N_{DAC_CC}	CC DAC resolution			10		bit
V_{CCDAC_STEP}	CC DAC step size			10		mA

6 Package information



7 Version history

Version	Date	Modify
V0.1.0	2023.8.25	Initial release
V0.2.0	2025.5.13	Corrections

8 Notice

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