N32H785 Datasheet

The N32H785 series utilizes a high-performance dual-core architecture. The ARM Cortex-M7 core is the main core, running at frequencies up to 600MHz, supporting double-precision floating-point operations and DSP instructions. The Cortex-M4 core is the auxiliary core, running at frequencies up to 300MHz. It integrates (2/4MB) on-chip FLASH, up to 1504KB of SRAM (including 1024KB TCM SRAM and 480KB SRAM) + 4KB Backup SRAM, 3 12-bit 5Msps ADCs, 4 high-speed comparators, 6 12-bit DACs, multiple high-speed U(S)ART, I2C, xSPI, SPI, USBFS Dual Role, USBHS Dual Role, CAN-FD, SDRAM, FEMC, SDMMC, and 10/100/1000M Ethernet communication interfaces. It supports Digital Camera Interface (DVP), TFT-LCD graphical interface, JPEG hardware codec and GPU. It features a built-in high-performance encryption algorithm hardware acceleration engine supporting AES/TDES, SHA, and SM4 algorithms, TRNG true random number generator, and CRC8/16/32 support. It supports up to 166 GPIOs, with package types including LQFP176, UFBGA176+25, LQFP208, and TFBGA240+25 packages.

Key Features

- **Dual-Core CPU Architecture (Cortex-M7 and Cortex-M4F)**
  - ARM Cortex-M7
    - 32-bit ARM Cortex-M7 core, double-precision floating-point unit, supports DSP instructions and MPU
    - Built-in 32KB instruction cache and 32KB data cache with ECC
    - Maximum frequency 600MHz, 1284 DMIPS
- **ARM Cortex-M4F**
  - 32-bit ARM Cortex-M4F core + FPU, single-cycle hardware multiply/divide instructions, supports DSP instructions and MPU
  - Built-in 16KB instruction cache and 16KB data cache with parity check, supports Flash acceleration unit for 0-wait program execution
  - Maximum frequency 300MHz, 375 DMIPS
- **Encrypted Memory**
  - 2M/4M Byte on-chip Flash, supports encrypted storage and automatic program decryption during execution
  - 1504KB built-in SRAM, supports ECC verification
    - 1024KB TCM SRAM, configurable as D-TCM, I-TCM or SRAM
    - 480KB on-chip SRAM
- **Operating Modes**
  - Run mode
  - SLEEP mode: AXI enabled, AHB enabled
  - Stop0 mode: SRAM, TCM, RTC, LSE, IWDG enabled
  - Stop2 mode: Flash standby mode, SRAM, TCM, RTC, LSE, IWDG, Backup SRAM, backup registers enabled, I/O maintained

NSING Technologies Pte. Ltd.
Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

- Standby mode: Backup SRAM, RTC, IWDG, LSE, backup registers enabled, SRAM, TCM disabled
- VBAT mode: Backup SRAM, RTC, LSE, backup registers enabled

- **Clock**
  - 4MHz~48MHz external high-speed crystal
  - 4MHz~50MHz external clock input
  - 32.768KHz external low-speed crystal
  - Built-in 3 high-speed PLLs
  - Built-in MSI clock, supporting configurable 31.25K/62.5K/125K/250K/500K/1M/2M/4M/8M/16MHz clocks
  - Internal high-speed RC 64MHz
  - Internal low-speed RC 32KHz
- **Reset**
  - Supports power-on/power-down/external pin reset
  - Supports watchdog reset and software system reset
  - Supports programmable voltage detection
- **High-Speed Communication Interfaces**
  - 8 USART interfaces/7 UART interfaces, supporting ISO7816, IrDA, LIN
  - 2 LPUART interfaces
  - 7 SPI interfaces, supporting master/slave modes, rates up to 50 MHz
  - 10 I2C interfaces, rates up to 3.4 MHz, configurable master/slave modes, supports dual address response in slave mode
  - 1 USBHS Dual Role interface, supporting built-in high-speed PHY
  - 1 USBFS Dual Role interface
  - 8 CAN-FD bus interfaces
  - 2 Ethernet MAC interfaces, ETH1 supporting 10M/100M/1000M communication rates, ETH2 supporting 10M/100M communication rates, both supporting IEEE 1588 time synchronization protocol
- **High-Performance Analog Interfaces**
  - 3 12-bit 5Msps ADCs, supporting 12-bit, 10-bit resolution, hardware oversampling up to 16-bit, supporting up to 55 external single-ended input channels, 5 internal single-ended input channels, supporting single-ended mode and differential mode
  - 4 high-speed analog comparators
  - 6 12-bit DACs, of which 2 1Msps DACs support external output with or without Buffer individually, internal output only supports without Buffer mode; simultaneous internal and external output must enable Buffer; the other 4 DACs only support one output channel internally to the chip, sampling rate 15Msps, supporting internal output without Buffer
  - 2 MCO outputs, configurable to output SYSCLK, HSE, MSI, LSE, LSI, HSI64 or PLL clock division
  - Supports 1 reference voltage VREFBUF (1.5V/1.8V/2.048V/2.5V configurable)

NSING Technologies Pte. Ltd.
Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

- 1 temperature sensor

- **Audio Interfaces**
  - 4 I2S, supporting half/full duplex modes, audio sampling frequencies from 8KHz to 192KHz
  - 8 PDM digital microphone interfaces built into the DSMU
- **Memory Expansion Interfaces**
  - 1 FEMC (Flexible External Memory Controller) interface, bus rate 100 MHz, SRAM/PSRAM/Nor Flash supporting configurable 16/32-bit data width, NAND Flash supporting configurable 8/16-bit data width
  - 1 xSPI interface, supporting 1/2/4/8-bit data width, configurable master/slave modes, rates up to 133 MHz, can be used for external SRAM, PSRAM and Flash expansion, supporting XIP
  - 1 SDRAM interface, rates up to 133 MHz
  - 2 SDMMC interfaces, supporting SD/SDIO 3.0, eMMC 4.51 formats, rates up to 104MHz
- **Image Processing Interfaces**
  - 2 digital camera interfaces (DVP), supporting 8/10/12/16bit, rates up to 110MHz
  - 1 MIPI display controller (DSI), with built-in D-PHY
  - 1 TFT-LCD display interface, supporting up to 24-bit parallel digital RGB LCD, providing all signal interfaces to directly connect various LCD and TFT panels, resolution up to 1920x1080
  - Built-in 2.5D graphics processor, supporting image scaling, rotation, mixing, anti-aliasing, texture mapping, etc.
  - Hardware JPEG codec
- **Maximum support for 166 GPIOs, low-speed GPIOs support 5V tolerance (under VDD = 3.3V ± 10% conditions)**
- **Motor Control Cordic Accelerator, supporting trigonometric and hyperbolic function acceleration, supporting floating point input and output**
- **Delta Sigma Module Unit (DSMU)**
- **Built-in filtering algorithm accelerator FMAC, supporting FIR, IIR filtering**
- **3 high-speed DMA controllers, each controller supporting 8 channels, 1 MDMA supporting 16 channels, channel source and destination addresses freely configurable**
- **RTC real-time clock, supporting leap year perpetual calendar, alarm events, periodic wake-up, supporting internal and external clock calibration**
- **Timers and Counters**
  - 2 16-bit ultra-high precision timer counters (SHRTIM1/SHRTIM2), highest control precision 100ps, each ultra-high precision timer counter has 1 master timer and 6 16-bit slave timer units. Each timer unit has 2 independent channels, supporting 12 independent PWM outputs or 6 pairs of complementary PWM outputs
  - 4 16-bit advanced timer counters, supporting input capture, complementary output, quadrature encoder input and other functions, highest control precision 3.3ns; each timer has 6 independent channels, 4 of which support 4 pairs of complementary PWM outputs
  - 10 16-bit general-purpose timers (GTIMA13), each timer with 4 independent channels, supporting input capture, output compare, PWM generation
  - 4 32-bit basic timer counters (BTIM1~4)

NSING Technologies Pte. Ltd.
Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

- 5 16-bit low-power timers (LPTIM1~5), can work in Stop2 mode
- 2x 24-bit SysTick, 2x 14-bit window watchdogs (WWDG), 2x 12-bit independent watchdogs (IWDG)

- **Programming Methods**
  - Supports SWD/JTAG online debugging interfaces
  - Supports USB, UART Bootloader
- **Security Features**
  - FLASH has up to 4 encryption partitions, supporting encrypted storage
  - Supports write protection (WRP), multiple read protection (RDP) levels (L0/L1/L2)
  - Built-in cryptographic algorithm hardware acceleration engine, supporting AES/TDES, SHA, SM4 algorithms
  - TRNG true random number generator, CRC8/16/32 operations
  - Supports secure boot, encrypted program download, secure updates, supports external high-speed and low-speed clock failure detection
  - Supports tamper detection
- **OTP Supports 128-bit UCID**
- **Operating Conditions**
  - Operating voltage range:
    - 2.3V~3.6V
  - Chip junction temperature range: -40°C~125°C
- **Certifications**
  - USB IF
  - IEC61508 SIL2
- **Packages**
  - LQFP176(24mm x 24mm)
  - UFBGA176+25(10mm x 10mm)
  - LQFP208(28mm x 28mm)
  - TFBGA240+25(14mm x 14mm)
- **Ordering Models**

Series	Mode
N32H785xxx7	N32H785IKL7, N32H785IIL7, N32H785IKB7, N32H785IIB7, N32H785BKL7, N32H785BIL7, N32H785XKB7, N32H785XIB7

NSING Technologies Pte. Ltd.
Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

1 Product Introduction

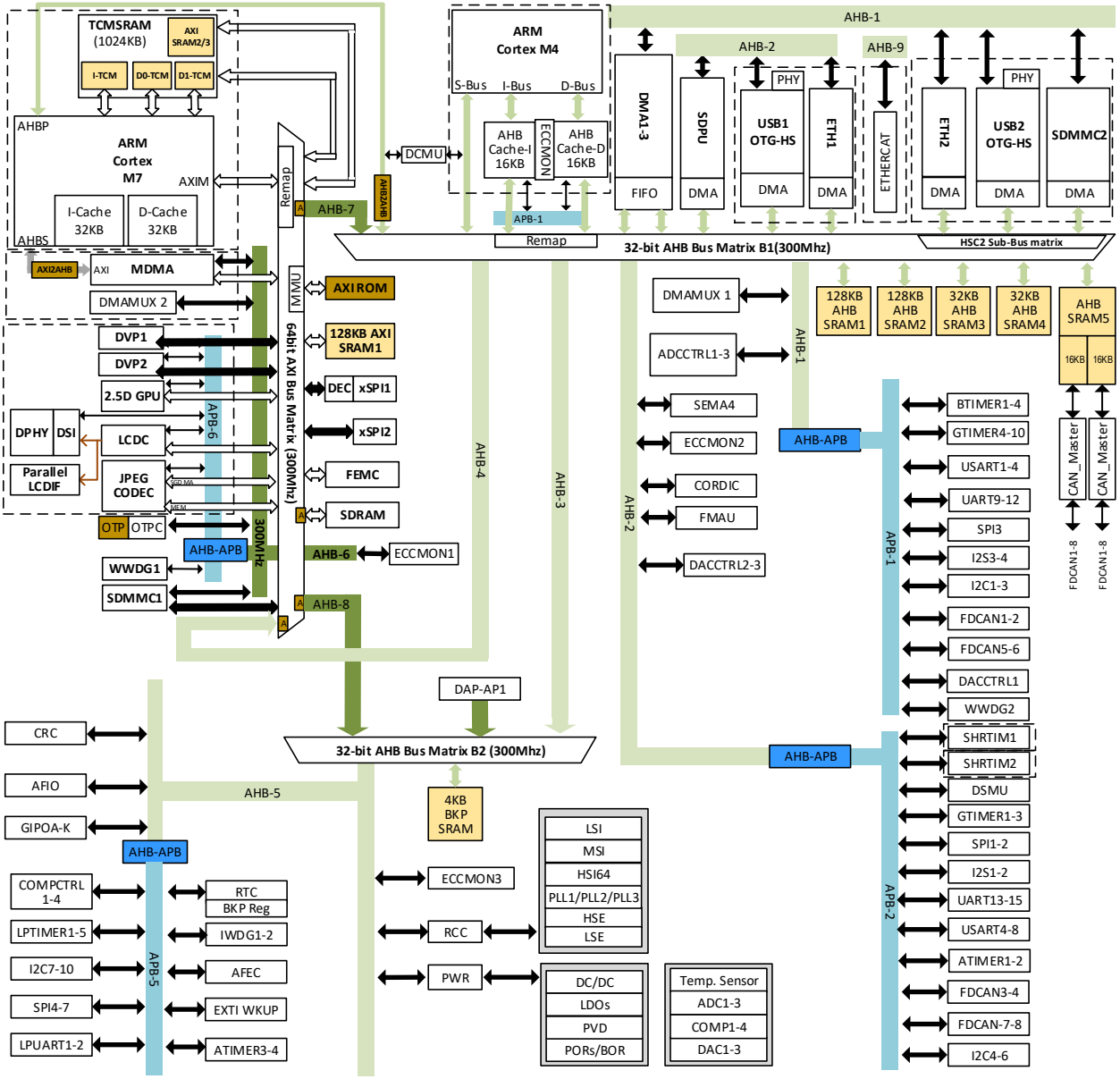
The N32H785 series utilizes a high-performance dual-core architecture. The ARM Cortex-M7 core is the main core, running at frequencies up to 600MHz, supporting double-precision floating-point operations and DSP instructions. The Cortex-M4 core is the auxiliary core, running at frequencies up to 300MHz. It integrates (2/4MB) on-chip FLASH, up to 1504KB of SRAM (including 1024KB TCM SRAM and 480KB SRAM) + 4KB Backup SRAM, 3 12-bit 5Msps ADCs, 4 high-speed comparators, 6 12-bit DACs, multiple high-speed U(S)ART, I2C, xSPI, SPI, USBFS Dual Role, USBHS Dual Role, CAN-FD, SDRAM, FEMC, SDMMC, and 10/100/1000M Ethernet communication interfaces. It supports Digital Camera Interface (DVP), TFT-LCD graphical interface, JPEG hardware codec and GPU. It features a built-in high-performance encryption algorithm hardware acceleration engine supporting AES/TDES, SHA, and SM4 algorithms, TRNG true random number generator, and CRC8/16/32 support. It supports up to 166 GPIOs, with package types including LQFP176, UFBGA176+25, LQFP208, and TFBGA240+25 packages.

The N32H787 series products can operate stably in a temperature range from -40°C to +105°C, with supply voltage from 2.3V to 3.6V, offering multiple power consumption modes.

Figure 1-1 shows the bus block diagram of this product series.

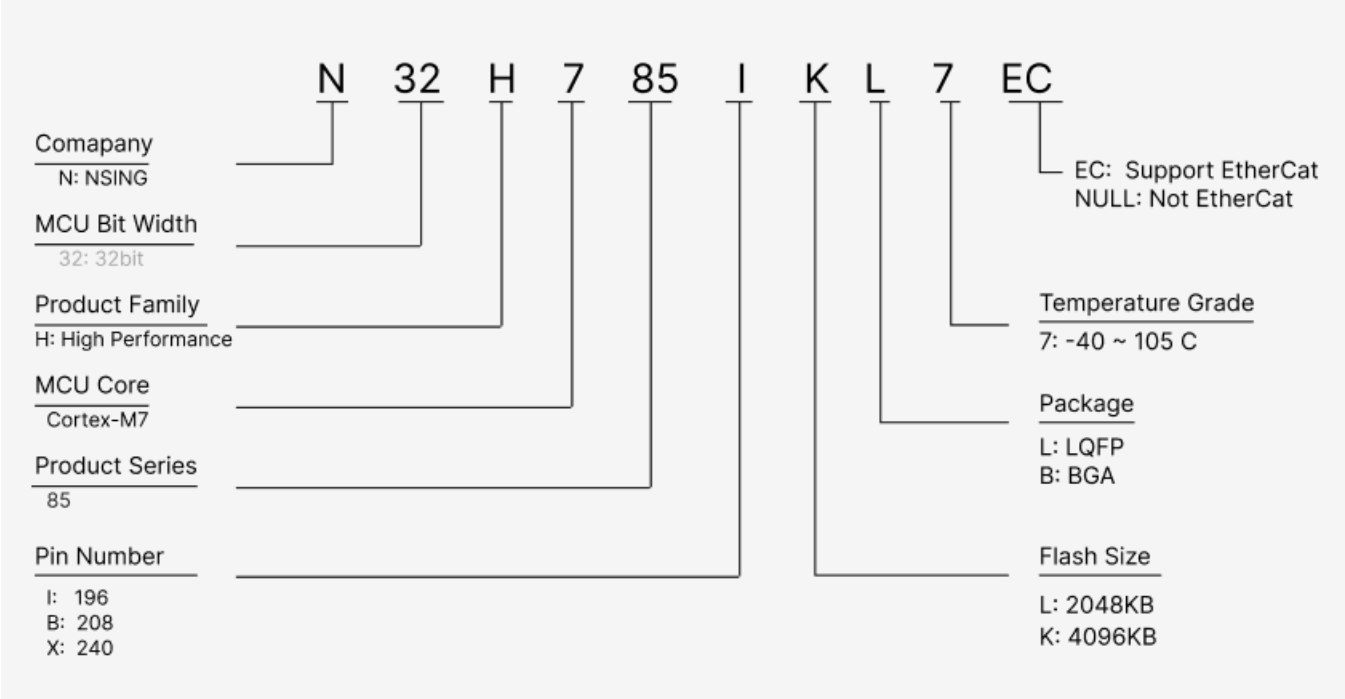
NSING Technologies Pte. Ltd.
Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

Figure 0-1 N32H785 Series Block Diagram



NSING Technologies Pte. Ltd.
Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

1.1 Naming Convention



NSING Technologies Pte. Ltd.
Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

1.2 Product model resource configuration

Table 1-1 N32H785 series resource configuration

Device Mode		N32H785 IKL7	N32H785 IIL7	N32H785 IKB7	N32H785 IIB7	N32H785BKL7	N32H785BIL7	N32H785XKB7	N32H785XIB7
Flash（KB）		4096	2048	4096	2048	4096	2048	4096	2048
SRAM（KB）	TCM	1024							
	System RAM	480							
	Backup RAM	4							
Core	M7	600MHz							
	M4	300MHz							
Operating Voltage		2.3V~3.6V							
Operating Temperature		-40℃~105℃							
DCDC（step-down）		Yes							
Coprocessor	Cordic	Yes							
	DSMU	Yes							
	FMAC	Yes							
Timers	SHRTIM	2							
	ADTIM	4							
	GPTIM	10							
	BSTIM	4							
	LPTIM	5							
	SysTick timer	2							
	WWDG	2*14bit							
	IWDG	2*12bit							
	RTC	Yes							
Communication Interfaces	SPI/I2S	6/4				7/4			
	I2C	8				10			
	USART	7				8			
	UART	6				7			
	LPUART	2							
	USBHS Dual Role	1							
	USBFS Dual Role	1							
	CAN FD	8							
	10/100M ETH	1							
	10/100/1000M ETH	1							
Expanded Memory	SDRAM	Yes							
	xSPI	1							
	FEMC	Yes							
	SDMMC	2							
Analog	12bit ADC	3							
	12bit DAC Number of channels	2+4(1) 2 External channels							
	Comparator	4							

NSING Technologies Pte. Ltd.
Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

	VREFBUF	Yes			
Imaging	LCDC	Yes			
	GPU	Yes			
	JPEG	Yes			
	DVP	2			
GPIO		117	126	148	166
DMA Number of channels		3 24Channel			
MDMA Number of channels		1 16Channel			
Algorithm Support		DES/3DES, AES, SHA1/SHA224/SHA256, CRC8/16/CRC32			
Security Protection		R/W Protection (RDP/WRP), storage encryption, secured boot			
Package		LQFP176	UFBGA176+25	LQFP208	TFBGA240+25

Note：The 4 DACs only support internal connection and cannot be output to GPIO

NSING Technologies Pte. Ltd.
Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

2 Functional Overview

2.1 Processor Cores

The N32H787 series devices are based on high-performance Arm® Cortex®-M7 and Cortex®-M4 32-bit RISC cores. The Cortex®-M7 core operates at frequencies up to 600 MHz, while the Cortex®-M4 core operates at frequencies up to 300 MHz. Both cores have floating-point units (FPU), supporting Arm® single-precision and double-precision (Cortex®-M7 core only) operations and conversions (IEEE 754 compatible), including a complete set of DSP instructions and memory protection unit (MPU) to enhance application security.

2.1.1 Arm® Cortex®-M7

Arm® Cortex®-M7 is a high-performance processor with nearly twice the performance of the Arm® Cortex®-M4. It features a 6-stage superscalar pipeline with an FPU capable of single-precision and double-precision operations. Instruction and data buses are extended to 64-bit width.

Processor supported interfaces include:

- 64-bit AXI4 interface
- 32-bit AHB master interface
- 32-bit AHB slave interface
- 64-bit instruction TCM interface
- 2x32-bit data TCM interfaces

Other processor features include:

- 32kB instruction cache, 32kB data cache, all cache memories protected by ECC
- Memory Protection Unit (MPU), configurable with up to 16 memory protection regions
- Double-precision and single-precision floating-point FPU
- ETM support
- Efficient DSP instructions

2.1.2 Arm® Cortex®-M4

Arm® Cortex®-M4 is a high-performance 32-bit RISC reduced instruction set core. It operates at frequencies up to 300 MHz. This core enhances computational capabilities, supporting single-precision floating-point calculations, DSP instructions, parallel computing, etc., capable of meeting the needs of effective control and mixed signal processing applications.

Processor features include:

- Three-stage pipeline
- Harvard bus architecture
- 16KB instruction cache, 16KB data cache, all cache memories protected by ECC
- Single-precision floating-point unit (FPU)

2.1.3 MPU

The MPU has configurable memory protection attributes. It allows the definition of up to 16 protected regions, which can be divided into up to 8 independent sub-regions, where region address, size, and attributes can be configured. The protection range covers 32B to 4GB of addressable memory. When illegal access occurs, a memory management exception is generated.

2.2 Memory

The N32H787 series devices feature Flash, configurable embedded SRAM, and external storage interfaces such as FEMC, SDRAM, and xSPI2. The configurable architecture provides flexibility in partitioning memory resources according to application requirements, allowing for appropriate performance trade-offs in terms of application code size, data size, and power saving. Additionally, embedded ROM is used as the initial bootloader and for secure boot.。

2.2.1 Embedded SRAM

TCM RAMs (for Cortex-M7 only)

TCM RAM consists of 1MB SRAM, which can be configured as ITCM-RAM, DTCM-RAM, and AXI-SRAM2/3. Software can flexibly configure D-TCM and I-TCM sizes, with remaining SRAM automatically configured as AXI-SRAM2/3, with a granularity of 128KB. ITCM RAM is mapped to address 0x0000 0000 and can only be accessed by the Cortex®-M7 CPU and MDMA (even when the CPU is in sleep mode). DTCM RAM is mapped at **address 0x2000** 0000 and can also only be accessed through the Cortex®-M7 CPU core and MDMA.

AXI SRAM

Up to 1152KB of AXI RAM, which can be accessed by byte (8-bit), half-word (16-bit), full word (32-bit), or double word (64-bit). AXI SRAM is divided into the following types:

- 128KB of AXI SRAM 1 mapped to address 0x2400 0000
- Up to 512KB of AXI RAM 2 (shared with ITCM and DTCM), mapped to address 0x2402 0000
- Up to 512KB of AXI RAM 3 (shared with ITCM and DTCM), mapped to address 0x240A 0000

AHB SRAM

Up to 352KB of AHB SRAM1-5, which can be accessed by byte, half-word (16-bit), or word (32-bit). AHB SRAM is divided into the following types:

- 128 KB of AHB SRAM1 mapped to address 0x3000 0000
- 128 KB of AHB SRAM2 mapped to address 0x3002 0000
- 32 KB of AHB SRAM3 mapped to address 0x3004 0000
- 32 KB of AHB SRAM4 mapped to address 0x3004 8000
- 32 KB of AHB SRAM5 mapped to address 0x3005 0000
- AHB SRAM 5 is divided into two blocks, shared with CANFD1-8, used as CANFD data frame buffer.

Backup SRAM

Backup SRAM is located in AHB bus domain 2 and is mapped to address 0x3800 0000. It can be accessed by byte, half-word (16-bit), or word (32-bit).

Error Correction Code (ECC)

All internal system RAM includes error correction code (ECC). It can be programmatically configured through their respective ECC monitor (ECCMON) modules. The ECC mechanism is based on the SECDED algorithm, supporting single-bit and double-bit error detection as well as single-bit error correction.

SRAM data ECC protection methods:

- Each 32-bit word adds 7 ECC bits
- For ITCM-RAM and AXI_SRAM1, each 64-bit word adds 8 ECC bits

2.2.2 Embedded ROM

The N32H787 series devices have 32KB of embedded ROM, mapped to address 0x1FFF0000. It contains a small bootloader divided into two parts: secure code and API. The secure code can only be accessed by the Cortex-M7, while the API can be called by the core CPU.

2.2.3 On-chip Flash

The maximum capacity of on-chip Flash is 4MB, with the first 128KB used for BOOTPATCH and option bytes, and the remaining space used for user application code. The on-chip Flash supports real-time AES128 decryption via the RTAD module, and this decryption applies to any data stored in Flash.

2.3 System Boot Modes

After reset, the Cortex®-M7 is started by default, with the Cortex®-M4 being started by the Cortex®-M7 application as needed. The BOOTROM program has two modes: Boot Application and Serial Download. These two modes can be selected via the Boot pin and option bytes:

Boot Application: After normal execution of the BOOTROM program, the application image will boot from Flash/TCM/SRAM according to BOOTADDR_M7 in the option bytes.

Serial Download: The BOOTROM program receives the application image via USART1 or USB1 and stores it in Flash/TCM/SRAM.

Table 0-1 Boot Mode

BOOT pin	Option Bytes (OTP_SYS_CFG_BTM)	Mode	Decription
0	!0x5AA5 and !0x4884	Boot Application	boot from Flash/TCM/SRAM
1	!0x5AA5 and !0x4884	Serial Download	Built communication with Host by UART or USB
*	0x5AA5	Boot Application	boot from Flash/TCM/SRAM
*	0x4884	Serial Download	Built communication with Host by UART or USB

2.4 Power Supply Scheme

External Power Supplies:

VDD, VDDA, VREF, VBAT, VDDSMPS, VDDLDO, VDD33USB, VDDDSI. Among these, VDD is the chip power supply, mainly powering the supply system and clock system; VDDA is the analog peripheral power supply, mainly powering analog peripherals; VREF provides reference power for analog peripherals to provide higher accuracy. VBAT connects to a battery to power the backup domain. VDDSMPS powers the DCDC SMPS;

VDDLDO powers the main LDO (only for supported models, otherwise NC); VDD33USB powers the USB PHY; VDDDSI powers the MIPI-DSI PHY.

Five Power Domains, supplying different power regions through external power sources:

- **VDD Domain**: Voltage range 1.8V~3.63V, mainly powers SMPS, Main LDO, most GPIO, HSE, HSI, PLL, POR/PDR, BOR, PVD, USB PHY, DSI PHY, etc.
- **VDDA Domain**: Voltage range 1.8V~3.63V, mainly powers ADC, DAC, COMP, VREFBUF, TS, etc.
- **VDDBK Domain**: Voltage range 1.8V~3.63V, mainly powers WKUP pins, NRST, PC13/14/15, LSE, LSI, etc.
- **VDDD Domain**: Voltage of 0.9V or 0.8V. Mainly powers CPU, SRAM, RCC, TRNG, USB PHY digital part, DSI PHY digital part, and most peripherals. The VDDD domain is divided into VDDDRET and VDDDMAIN sub-power domains:
  - **VDDDRET Domain**: For LPUART, LPTIMER, EXTI and other modules, powered by VDDD, with separate switch control.
  - **VDDDMAIN Domain**: Directly powers AXI, AHB, APB buses and bus adapters; low-speed communication interfaces SPI, I2C, UART; timers ATIMER, GTIMER, BTIMER, etc. And includes the following sub-power domains:
    - CM7 Sub-power Domain: Contains CM7 core, TCM memory and controllers;
    - MDMA Sub-power Domain: Contains MDMA;
    - HRTIM1 Sub-power Domain: Contains the digital circuits of HRTIMER 1;
    - HRTIM2 Sub-power Domain: Contains the digital circuits of HRTIMER 2;
    - HRTIMAFE Sub-power Domain: Contains the HRTIMER analog front-end shared by HRTIMER1 and HRTEIMER2;
    - HSC1 Sub-power Domain: Contains high-speed communication interfaces USB1 and Ethernet 1;
    - HSC2 Sub-power Domain: Contains high-speed communication structures USB2, Ethernet 2, and SDMMC 2;
    - GRAPHICS Sub-power Domain: Contains GPU, DVP1, DVP2, LCDC, JPEG CODEC, MIPI-DSI and other modules.

  The power switches for the above sub-power domains are controlled by hardware for the CM7 core subsystem, while others are controlled by software.
- **VDDDBK Domain**: Voltage of 0.9V or 0.8V, mainly powers PWR, Backup SRAM, RTC, WKUP pins, NRST, PC13/14/15, backup IOM, IWDG, RCC_BKP, and Backup registers.

2.5 Reset

The device has integrated power-on reset (POR) and power-down reset (PDR) circuits that are always operational, ensuring the system works when the power supply exceeds 1.8V. When VDD falls below the set threshold (VPOR/PDR), the device enters reset state without requiring an external reset circuit.

2.6 Programmable Voltage Detector

A built-in programmable voltage detector (PVD) monitors VDD supply and compares it with the threshold VPVD. When VDD falls below or rises above the VPVD threshold, an interrupt is generated, and the interrupt handler can issue warning messages. The PVD function needs to be enabled via software. For values of VPOR/PDR and VPVD, refer to table 4-9.

2.7 Low Power Modes

N32H787 supports five low-power modes:

- **SLEEP Mode**

  In SLEEP mode, only the CPU stops while all peripherals remain operational and can wake up the CPU when an interrupt/event occurs.

- **STOP0 Mode**

  STOP0 mode is based on the Cortex-M7F deep sleep mode and can achieve low power consumption without losing SRAM and register contents. In STOP0 mode, all high-speed clocks are shut down, such as PLL, HSI, and HSE.

  Wake-up: The chip can be awakened from STOP0 mode by any signal configured as EXTI. EXTI signals can be from 16 external EXTI signals (I/O related), PVD output, LPTIMER, LPUART, RTC wake-up, RTC alarm, etc.

- **STOP2 Mode**

  STOP2 mode is based on the Cortex-M7F deep sleep mode. CPU internal registers are preserved, and the contents of TCM or SRAM running the program remain intact while the main power domain VDDDMAIN is powered down. STOP2 mode achieves lower power consumption than STOP0 mode. In STOP2 mode, high-speed clocks in the main power domain are shut down, such as PLL, HSI, HSE; the retention domain (VDDDRET) power remains on, allowing modules like LPUART and LPTIMER to work with low-speed clocks LSE or LSI; the backup domain (VDDDBKP) power is on, allowing RTC, IWDG, etc. to function normally.

  Wake-up: The chip can be awakened from STOP2 mode by any signal configured as EXTI. EXTI signals can be from 16 external EXTI signals (I/O related), PVD output, RTC wake-up, RTC alarm, etc. After wake-up, the CPU can continue running from where it was before entering STOP2.

- **STANDBY Mode**

  STANDBY mode achieves the lowest current consumption state. The internal voltage regulator is turned off, and the PLL, HSI RC oscillator, and HSE crystal oscillator are also turned off. After entering STANDBY mode, the retention domain (VDDDRET) loses power, most register contents

are lost, but backup register contents are preserved, backup SRAM can optionally be maintained, and the backup domain (VDDDBKP) circuits remain operational.

Wake-up: External reset signal on NRST, IWDG reset, edge on WKUP pin, RTC wake-up, or RTC alarm wake-up events.

- VBAT Mode

At any time, whenever VDD loses power while VBAT has power, the device will automatically enter VBAT mode. In VBAT mode, most I/O pins are in high-impedance state except for NRST, WKUP, PC13_TAMPER, PC14, and PC15.

Wake-up: VDD power-on

2.8 RCC

RCC manages the generation of all clocks, clock gating, and control of system and peripheral resets. It offers high flexibility in clock source selection and allows application of clock ratios to improve power consumption.

2.8.1 Clock Management

The device has 3 built-in internal oscillators, 2 oscillators with external crystal or resonator, and 4 PLLs.

RCC has the following clock source inputs:

- **HSI64**: 64 MHz internal high-speed oscillator
  The control logic for this oscillator is located in the standby power domain. After initial power-up and wake-up from system low-power modes (stop0, stop2, and standby), this clock is used as the default system clock.
- **MSI**: 16 MHz medium-speed oscillator
  The control logic for this oscillator is located in the retention power domain. In stop2 system power mode, this clock is used as the high-speed clock by peripherals in the retention power domain. This clock can also optionally serve as the system clock and core clock for certain peripherals.
- **HSE**: 4 ~ 48 MHz external high-speed oscillator
  The control logic for this oscillator is located in the core power domain. This clock can optionally serve as the system clock, core clock for certain peripherals, and reference clock for some PHYs (USB, DSI...).
- **LSI**: 32KHz low-speed internal oscillator
  The control logic for this oscillator is located in the standby power domain. It is the first clock switched during system power-up and is used by PWR in the standby power domain to start system power-up and wake-up from low-power system modes such as standby and stop2. Peripherals in the standby and retention power domains also use this clock.
- **LSE**: 32.768 KHz low-speed external oscillator
  The control logic for this oscillator is located in the standby power domain. This oscillator provides low-power and precise clock for peripherals in the standby and retention power domains.

- **PLL**: 430MHz ~ 1.25GHz phase-locked loop

  The control logic for this oscillator is located in the core power domain. HSI64, MSI, and HSE clocks can be configured as source clocks for the PLL. It has 4 PLLs.

  - **PLL1** maximum frequency 600 MHz, this PLL is used by certain peripherals as a system clock source and core clock source.
  - **PLL2** maximum frequency 800 MHz, this PLL is used by certain peripherals as a system clock source and core clock source.
  - **PLL3** maximum frequency 800 MHz, certain peripherals use this PLL as a core clock source.
  - **SHRPLL** maximum frequency 1.25 GHz, this PLL is used by the SHRTIMER peripheral as a core clock source.

The clock outputs of PLL1, PLL2, and PLL3 are further divided by configurable digital dividers and then used as system clock or peripheral core clock. The SHRPLL clock output is divided by 4 in the AFE to generate a 312.5 MHz clock for the SHRTIMER peripheral.

2.8.2 System Reset Sources

System reset will reset all registers to their reset values, except for the reset flags in the reset status register and certain registers in the standby domain (these registers can only be reset by programming the BDRST register and through standby domain POR reset).

System reset comes from the following sources:

- Main power domain POR from PWR and AFE.
- NRST pin.
- POR reset (main domain) from PWR and AFE.
- Reset requests from IWDG and WWDG.
- Reset request from the CPU.
- EMC reset request.
- Low-power reset request from PWR.
- BOR reset.
- MMU reset request.

2.9 SEMA4

The hardware semaphore module provides 32 (32-bit) register-based semaphores. Semaphores can be used to ensure synchronization between different processes running on cores. SEMA4 provides a non-blocking mechanism to atomically lock semaphores. It offers the following functions:

- Semaphores can be locked in 2 ways:
  - 2-step locking: Write COREID and PROCID to the semaphore, then read to check
  - 1-step locking: Read COREID from the semaphore
- Generate an interrupt when a semaphore is released
  - Each semaphore can generate one interrupt
- Semaphore clear protection
  - A semaphore will only be cleared when COREID matches PROCID

- Global semaphore clearing based on COREID

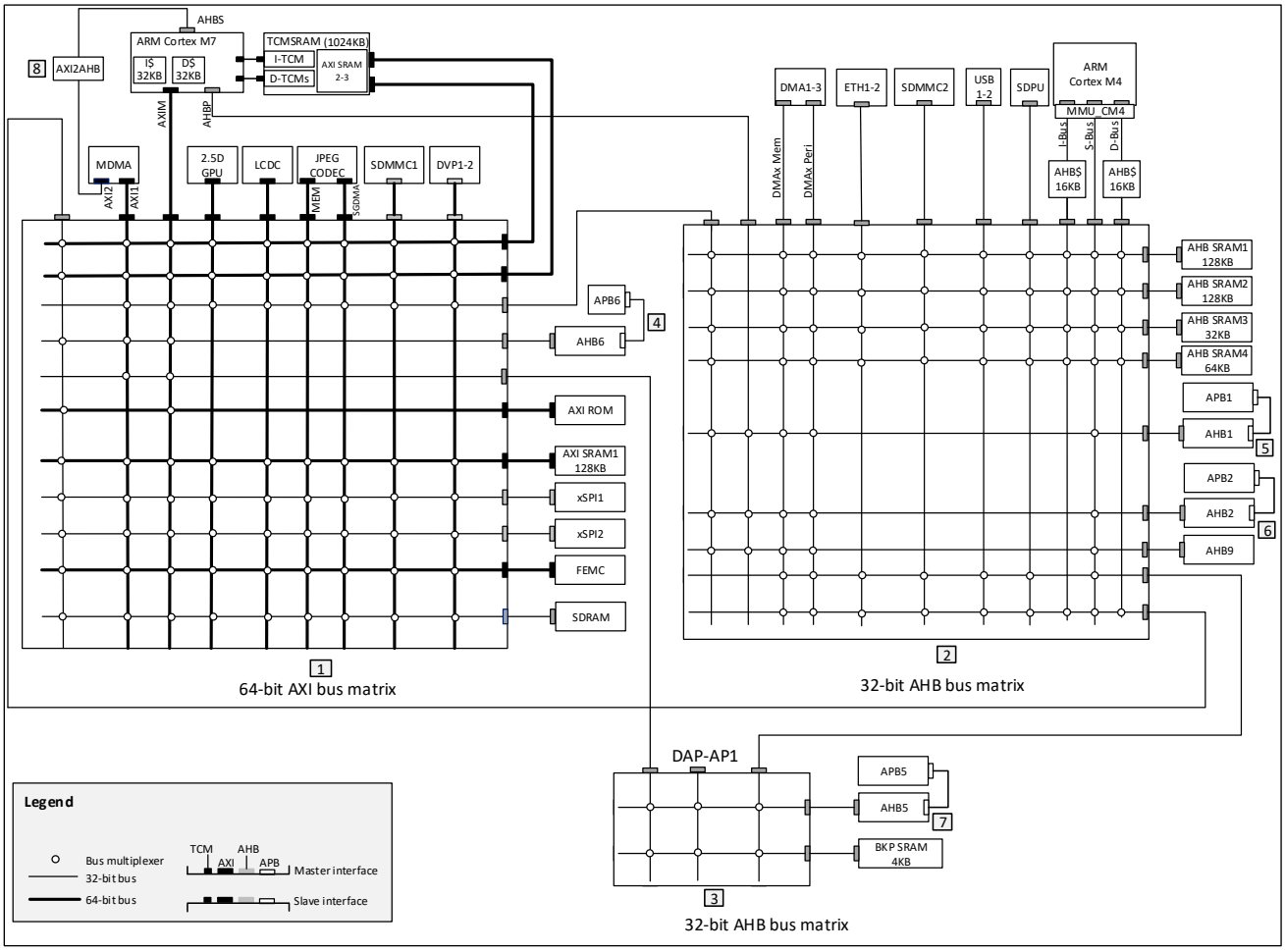
SEMA4 includes the following features:

- 32 (32-bit) semaphores
- 8-bit ProcessID
- Bit MasterID
- 1 interrupt line
- Lock indication

2.10 Bus Interconnect Matrix

These devices feature an AXI bus matrix, two AHB bus matrices, and bus bridges to implement interconnection between bus masters and bus slaves.

Figure 2-1 Bus Matrix Architecture



2.11 General Purpose Input/Output Interface (GPIO) and Alternate Function Input/Output Interface (AFIO)

GPIO refers to General Purpose Input/Output interface, while AFIO refers to Alternate Function Interface. The chip supports up to 168 GPIOs, which are divided into 11 groups (GPIOA/GPIOB/GPIOC/GPIOD/GPIOE/GPIOF/GPIOG/GPIOH/GPIOI/GPIOJ/GPIOK). Each group has 16 ports. GPIO ports share pins with other alternate peripheral functions. Users can configure them flexibly according to their needs. Each GPIO pin can be independently configured as output (push-pull or open-drain), input (floating, pull-up, or pull-down), or alternate peripheral function port. Except for analog function pins, other GPIO pins have high current capability.

GPIO ports have the following characteristics:

- Each GPIO port can be separately configured by software into the following modes:
  - Floating input
  - Pull-up input
  - Pull-down input
  - Analog function
  - Open-drain output, pull-up/pull-down configurable
  - Push-pull output, pull-up/pull-down configurable
  - Push-pull alternate function, pull-up/pull-down configurable
  - Open-drain alternate function, pull-up/pull-down configurable
- Independent set or clear functions
- All IOs support external interrupts
- All IOs support low-power mode wake-up, with configurable rising or falling edge
  - 16 EXTIs available for STOP0 mode wake-up, all IOs can be multiplexed as EXTI
  - PA0/PA2/PC1/PC13/PI8/PI11 can be used for STANDBY mode wake-up
- Support for software remapping of IO alternate functions
- Support for GPIO locking mechanism; once locked, can only be cleared by reset

Each I/O port bit can be programmed arbitrarily through the AHB interface, but I/O port registers must be accessed as 32-bit words, 16-bit half-words, or 8-bit bytes (AFIO registers only support 32-bit word access).

2.12 Nested Vectored Interrupt Controller (NVIC)

The device has an embedded Nested Vectored Interrupt Controller (NVIC).
NVIC includes the following features:

- 234 maskable interrupt channels
- 16 programmable priority levels

2.13 External Interrupt/Event Controller (EXTI)

The External Interrupt/Event Controller (EXTI) controls wake-up through configurable and direct event inputs generated by on-chip peripherals or external outputs. It sends wake-up events to PWR and transmits interrupt and event signals to both CPUs.

EXTI wake-up requests allow the system to wake up from STOP0 and STOP2 modes, and can also wake up CPUs from CSLEEP, CSTOP0, and CSTOP2 modes. Interrupt requests and event requests can also be used in Run mode.

EXTI includes the following features:

- Wakes up the system from STOP0 and CSTOP2 modes
- Generates interrupts and events transmitted to CPUs

These requests can be generated from the following input

- Direct events (generated by on-chip peripherals, event flags are saved or cleared in the source peripheral, not in EXTI) with the following characteristics:
  - Fixed rising edge triggering
  - Have interrupt and event mask bits
- Configurable events (generated from external devices or on-chip peripherals, only producing pulse events) with the following characteristics:
  - Software triggering
  - Both rising edge and falling edge triggering are allowed and configurable
  - Have interrupt and event mask bits

2.14 DMA Request Multiplexer (DMAMUX)

Peripherals indicate the existence of a DMA transfer request by setting their DMA request signal. The DMA controller processes these requests and generates a DMA acknowledgment signal, at which point the corresponding DMA request signal becomes invalid. Until then, the DMA request remains pending.

The DMAMUX request multiplexer can reconfigure (route) DMA request lines between the product's peripherals and the DMA controller. This routing functionality is implemented through a programmable multi-channel DMA request line multiplexer. Each channel can select a DMA request line without restriction, or select one synchronized with events from its DMAMUX synchronization inputs. Additionally, the DMAMUX can be used as a DMA request generator for programmable events from its input trigger signals.

Key features are as follows:

Table 2-2 DMAMUX Input/Output

Feature	DMAMUX1	DMAMUX2
Number of DMAMUX synchronization inputs	9	1 (internal use or unused)
Number of DMAMUX peripheral requests	210	4
Number of DMAMUX request trigger inputs	26	38
Number of DMAMUX request generator channels	8	16
Number of DMAMUX output request channels	24	16

- Each DMA request generator channel has:
  - DMA request trigger input selector
  - DMA request counter
  - Event overflow flag for the selected DMA request trigger input
- Each DMA request multiplexed channel output has:
  - Up to 210 input DMA request lines from peripherals
  - Up to 3 DMA request line outputs
  - Synchronization input selector
  - DMA request counter
  - Event overflow flag for the selected synchronization input
  - An event output for DMA request linking
- AHB slave interface, does not support burst, 32-bit access only
- DMAMUX overflow interrupts

2.15 DMAController (DMA)

The DMA controller is controlled by the CPU and can perform fast data transfers from source to destination. Once configured, data transfers occur without CPU intervention. This frees the CPU to execute other computational/control tasks or reduce overall system power consumption.

The chip has three DMA controllers (DMA1, DMA2, DMA3), with each controller having 8 logical channels. Each logical channel handles memory access requests from one or more peripherals. An internal arbiter controls the priority of different DMA channels.

Main features are as follows:

General Features

- Compliant with AMBA 2.0 standard
- AHB slave interface for DMA programming
- Channels
  - Up to eight channels, one channel per source and destination pair
  - Unidirectional channels - data transfers in one direction only
  - Programmable channel priority
- AHB master interface
  - Up to four independent AHB master interfaces, allowing:
    - Up to four simultaneous DMA transfers
    - Masters can be located on different AHB layers (multi-layer support)
    - Source and destination can be on different AHB layers (pseudo fly-by performance)
    - Configurable data bus width for each AHB master interface (up to 256 bits)
    - Configurable byte order for master interfaces
- Transfers
  - Support for memory-to-memory, memory-to-peripheral, peripheral-to-memory, and peripheral-to-peripheral DMA transfers
  - DMA transfers between APB peripherals through APB bridge
- Configurable identification registers
- Component ID parameters for configurable software driver support
- DesignWare AHB Lite system configuration
- Last beat DMA burst indication
- Support for little-endian, address-invariant (AI) big-endian scheme, and BE-32 (word-invariant) scheme for data access on AHB slave interface and each AHB master interface
- Arbitration scheme to determine which request line is granted access to a specific master bus interface

Address Generation

- Programmable source and destination addresses (on AHB bus)

- Incrementing, decrementing, or fixed addresses
- Multi-block transfers achieved through:
  - Linked lists (block chaining)
  - Automatic reload of channel registers
  - Contiguous addressing between blocks
- Independent source and destination selection for multi-block transfer types
- Scatter/gather support

Channel Buffering

- Single FIFO per channel for source and destination
- Configurable FIFO depth
- D flip-flop based FIFO
- Automatic data packing or unpacking to accommodate FIFO width

Channel Control

- Programmable source and destination for each channel
- Programmable transfer type per channel (memory-to-memory, memory-to-peripheral, peripheral-to-memory, peripheral-to-peripheral)
- Programmable burst transaction size per channel
- Programmable enable and disable of DMA channels
- Support for disabling channels without data loss
- Support for pausing DMA operations
- Support for RETRY, SPLIT, and ERROR responses
- Programmable maximum burst transfer size per channel
- Configurable maximum transaction size for gate optimization
- Configurable maximum block size for gate optimization
- Bus locking - programmable at transaction, block, or DMA transfer level
- Channel locking - programmable at transaction, data block, or DMA transfer level
- Hardcoded multi-block transfer type options
- Option to disable writeback of channel control registers at the end of each block transfer

Transfer Initiation

- Handshaking interfaces for source and destination peripherals (up to 8)
  - Hardware handshaking interface
  - Software handshaking interface
  - Peripheral interrupt handshaking interface
- Handshaking interface supports single or burst DMA transactions

- Polarity control for hardware handshaking interface
- Enable and disable individual DMA handshaking interfaces

Flow Control

- Programmable flow control at block transfer level (source, destination, or DMA controller)
- Software control of source data prefetching when destination is the flow controller

Interrupts

- Consolidated and separate interrupt requests
- Interrupt generation on:
  - DMA transfer (multiple data blocks) completion
  - Block transfer completion
  - Single and burst transaction completion
  - Error conditions
- Support for interrupt enabling and masking

Low Power Modes

- Global clock gating
- Channel-specific clock gating

2.16 MDMA Controller (MDMA)

MDMA is a highly configurable, highly programmable, high-performance, multi-master, multi-channel DMA controller that uses AXI as its data transfer bus interface.

Main features are as follows:

General Features

- Independent core, slave interface, and master interface clocks
- Up to 24 channels, one channel per source and destination pair
- Unidirectional data transfers only (each channel is unidirectional)
- Up to two AXI master interfaces:
  - Support for two master interfaces on multiple layers
  - Multiple AXI master interfaces can connect directly to peripherals on different AXI interconnects, improving bus performance
  - Support for different ACLK on different AMBA layers
- Memory-to-memory, memory-to-peripheral, peripheral-to-memory, and peripheral-to-peripheral DMA transfers
- Separate external memory interface (per channel) for connecting SRAM or register file-based memory to channel FIFO
- AMBA 3 AXI/AMBA 4 AXI compatible master interfaces
- AHB/APB4 slave interface for DMA controller programming
  - AHB slave interface supports single transfers only (hburst = 3'b000)

- AXI master data bus width up to 512 bits (applicable to both AXI master interfaces)
- Static or dynamic selection of Endian mode for AXI master interfaces
- Input pin for dynamic endianness selection
- Configurable independent control of endianness mode for linked list access on master interfaces
- Optional identification registers
- Support for channel locking
  - Support for internal channel arbitration locking a master bus interface at different transfer levels
- DMAC status indication outputs
  - Idle/busy indication
- DMA retention functionality
- Output pin indicating the last write transfer at DMA transaction level
- Multi-level DMA transfer hierarchy
  - DMA transfers divided into transaction level, block level, and complete DMA transfer level
- Support for AXI non-aligned transfers
- Support for context-sensitive low power options
- Support for unique ID functionality, generating AXI read/write transfers with unique IDs on AXI read/write channels

Channel Buffering

- One FIFO per channel
- Configurable FIFO depth
- Automatic packing/unpacking of data to accommodate FIFO width

Channel Control

- Programmable transfer type per channel (memory-to-memory, memory-to-peripheral, peripheral-to-memory, and peripheral-to-peripheral)
- Single or multiple DMA transactions
- Programmable multi-transaction size per channel
- Programmable maximum AMBA burst transfer size per channel
- Disabling channels without data loss
- Channel pause and resume
- Programmable channel priority
- Internal channel arbitration locking a master bus interface at different transfer levels
- Programmable multi-block transfers using linked lists, contiguous addressing, auto-reload, and shadow register methods
- Dynamic extension of linked lists
- Independent configuration of SRC/DST multi-block transfer types
- Multiple state machines, one each for SRC and DST per channel
- Separate state machines for data and LLI access

- Control signals such as cache and protection, programmable for each DMA block
- Programmable transfer length (block length)
- Error status registers for debugging when errors occur

Flow Control

- Programmable flow control at DMA transfer level
  - DMA controller is the flow controller at DMA block transfer level if the size of block transfers is known prior to DMA initialization
  - Source peripheral or destination peripheral is the flow controller for undefined length (demand mode) DMA block transfers if the size of DMA block transfers is not known prior to DMA initialization

Handshaking Interface

- Programmable software and hardware handshaking interfaces for non-memory peripherals
- Up to 64 hardware handshaking interfaces/peripherals
- Programmable mapping between enabling/disabling individual handshaking interface peripherals and channels; many-to-one mapping with only one peripheral active at a time
- Memory-mapped registers controlling DMA transfers in software handshaking mode

Interrupt Outputs

- Consolidated and separate interrupted outputs
- Interrupt generation on:
  - DMA transfer completion
  - Block transfer completion
  - Single or multiple transaction completion
  - Error conditions
  - Channel pause or disable
- Interrupt enabling and masking

Bus Interface

- Master interfaces using AMBA 3 AXI and AMBA 4 AXI protocols, slave interfaces using AHB, AXI4-Lite, and APB 3 protocols
- Data bus width for master interfaces up to 512 bits
- Outstanding transactions on master interfaces
- Setting outstanding transaction limits per channel on master interfaces
- Configurable AXI transfer width
- Out-of-order transaction support for different channels connected to the same master interface; transactions for a specific channel always initiated in order
- Incrementing and fixed address transfers on master interfaces
- Source address and destination address data transfers must be aligned with respective transfer widths
- Data bus width for slave interfaces of 32/64 bits
- Transfer size (width) used by slave interfaces; must be the same as data bus width

Security Features

- Parity protection for all common registers and channel-specific registers at interface level, data integrity checks through parity
- Error Correction Code (ECC) protection features to correct single-bit errors and detect double-bit errors, enabled to prevent data corruption
  - ECC protection for FIFO memory interfaces
  - ECC protection for UID memory interfaces
  - ECC protection for AXI master interfaces
- Lock-step functionality for safety-critical applications, enhancing security and reliability against adverse operating conditions such as Single Event Upsets (SEU) and extreme EMI/EMC

2.17 AES Real-Time Decryption (RTAD)

Main features are as follows:

- Real-time 128-bit decryption (single or multiple) during XSPI memory-mapped read operations.
  - Uses AES in Counter (CTR) mode with a key stream FIFO queue (depth = 4).
  - Supports any read size.
  - Physical address of the read is used for encryption/decryption.
  - Up to four independent encryption zones.
  - Zone definition granularity: 4096 bytes.
  - Zone configuration write-lock mechanism.
  - Two optional decryption modes: Execute-Only and Never-Execute.
  - Each zone has its own 128-bit key, two-byte firmware version, and eight-byte application-defined nonce. At least one of these must change each time application encryption is performed.

- Confidentiality and integrity protection for encryption keys.
  - Write-only registers with software lock mechanism.
  - Provides 8-bit CRC as public key information.

- Support for xSPI prefetch mechanism.
- In Execute-Only mode, an enhanced encryption mode can be selected, adding a proprietary protection layer on top of the AES stream cipher.
- AMBA AHB slave peripheral, accessible only via 32-bit word single accesses (otherwise generates an AHB bus error, and write accesses are ignored).

2.18 SDRAM (Synchronous Dynamic Random Access Memory)

Support for one SDRAM controller connected to the AHB bus, capable of accessing up to two external SDRAM/LPSDRAM memory devices.

Main features are as follows:

- Two SDRAM memory devices that can be independently configured
- Data bus with 8-bit, 16-bit, or 32-bit width
- 13-bit row address, 11-bit column address, 4 internal memory banks: 4x16Mx32bit (256 MB), 4x16Mx16bit (128 MB), 4x16Mx8bit (64 MB)

- Configurable row address: 11-bit, 12-bit, or 13-bit; configurable column address: 8-bit, 9-bit, 10-bit, or 11-bit
- Support for word, half-word, and byte access
- Automatic management of row and bank boundaries
- Support for burst mode
- Write access protection
- Programmable timing parameters
- Support for software reset
- SDRAM power-up initialization via software
- CAS latency 1, 2, 3
- Support for auto-refresh operations with programmable refresh rate
- Support for software-controlled suspend and wake-up

2.19 Filter Mathematics Accelerator (FMAC)

The Filter Mathematics Accelerator Unit is used for arithmetic operations on vectors, including a multiplier, accumulator, and address generation logic capable of indexing vector elements in local memory. The unit supports input and output circular buffers for implementing digital filters such as Finite Impulse Response (FIR) and Infinite Impulse Response (IIR).

This unit relieves the processor from frequent or lengthy filtering operations, freeing it to perform other tasks. In many cases, it can accelerate such computations compared to software implementations, speeding up time-critical tasks.

Main features are as follows:

- 16 x 16-bit multiplier
- 24 + 2-bit accumulator with addition and subtraction capabilities
- 16-bit fixed-point input and output data
- 256 x 16-bit data buffer
- Up to three data buffers definable in memory (two inputs, one output), defined by programmable base address pointers and associated size registers
- Input and output buffers can be used cyclically
- Filter functions: FIR, IIR (direct form 1)
- Vector functions: dot product, convolution, correlation
- Support for DMA reading and writing data

2.20 CORDIC Coprocessor (CORDIC)

The CORDIC hardware computation unit provides hardware acceleration for mathematical functions, primarily trigonometric functions. It is typically used to accelerate mathematical function calculations in applications such as motor control, metering, and signal processing.
Main features are as follows:

- Support for rotation and vector calculation modes
- Support for circular and hyperbolic coordinate systems
- Once calculation begins, any operation to read result registers will put the bus in a wait state until calculation completes, allowing calculation results to be read out after completion without polling or interrupting

- Support for acceleration of 10 functions: sine, cosine, sinh, cosh, atan, atan2, atanh, modulus, square root, natural logarithm
- Support for fixed-point and floating-point data input/output modes
- Support for interruption, polling, and DMA read/write modes
- Configurable iteration precision

2.21 Sigma-Delta Modulator Digital Filter Unit (DSMU)

The DSMU is a high-performance module for connecting external Σ-Δ modulators, featuring 8 external digital serial channels and 4 flexibly configurable Sigma-Delta digital filters that provide up to 24-bit final ADC resolution. The external serial channels can be configured as SPI interfaces or Manchester-encoded single-wire interfaces (with configurable parameters) to accommodate various modulators. It also supports internal parallel data input channels for receiving 16-bit parallel data streams from ADC peripherals or device memory.

The DSMU can operate in single conversion mode or continuous mode, and provides analog watchdogs with independently configurable digital filters, as well as short-circuit detection, extremum detection, and other functions. It also supports two power modes: normal mode and stop mode.

DSMU main features are as follows:

- 8 configurable external digital serial input channels:
  - Support for SPI interface to connect various Σ-Δ modulators
  - Support for the Manchester-encoded single-wire interface
  - Support for output clock to external Σ-Δ modulators
- 8 internal digital parallel input channels:
  - Up to 16-bit resolution
  - Data sources: ADC data or memory (CPU/DMA) data streams
- 4 configurable data signal processing units:
  - 1 Sincx filter: filter order/type (1..5), oversampling ratio (up to 1..1024)
  - 1 integrator: oversampling ratio (1..256)
- Up to 24-bit signed data output
  - Final output data right aligned (0..31 bits)
- Signed data output
- Automatic data offset correction (offset written by user to specified register)
- Support for continuous or single conversion
- Conversion start supports the following synchronization methods:
  - Software trigger
  - Internal timer
  - External event
  - Synchronized conversion with the first DSMU filter (DSMU_FLT0)
- Support for analog watchdog:
  - Low threshold and high threshold can be configured separately
  - Support for independently configurable Sincx digital filter (filter order = 1..3, oversampling ratio = 1..32)
  - Configurable data source: output data register, one or more serial digital input channels
  - Continuous data monitoring independent of normal conversion

- Support for short-circuit detector to detect saturated analog input data (below negative threshold or above positive threshold)
    - 8-bit counter for detecting 1..256 consecutive 0s or 1s in the data stream
    - Continuous monitoring of each channel (8 serial channel transceiver outputs)
- Brake signal can be generated after analog watchdog event or short-circuit detection event
- Support for extremum detection:
    - Automatic storage of maximum and minimum values of output data
    - Software refresh
- Support for pulse jumping function for beam-forming applications (similar to delay line)
- Support for DMA reading of conversion data
- Support for interruptions: conversion end, out of bounds, analog watchdog, short circuit, channel clock missing
- Support for regular and injected conversions:
    - Regular conversions can be performed at any time, even in continuous mode without affecting injected conversions
    - Injected conversions provide precise timing and have high priority

2.22 Real TimeClock (RTC)

The RTC is a group of continuously running counters with a built-in calendar clock module that provides perpetual calendar functionality, as well as alarm interruptions and periodic interrupt capabilities.

Main features include:

- Real-Time Clock (RTC) is an independent BCD timer/counter
- Software support for Daylight Saving Time compensation
- Programmable periodic auto-wakeup timer
- Two 32-bit registers containing hours, minutes, seconds, year, month, date, and day of week
- Independent 32-bit register containing sub-seconds
- Two programmable alarms
- Two 32-bit registers containing programmed alarm hours, minutes, seconds, year, month, date, and day of week
- Two independent 32-bit registers containing programmed alarm sub-seconds
- Digital precision calibration function
- Reference clock detection: a more accurate external clock source (50 or 60Hz) can be used to improve calendar accuracy
- Three configurable tamper detection events with filtering and internal pull-up, five internal tamper detection events
- Timestamp functionality
- 32 backup registers that maintain data in low-power mode
- Multiple interrupt/event wakeup sources including Alarm A, Alarm B, wakeup timer, timestamp, and tamper detection
- RCC register enables the RTC module and keeps voltage within operating range; RTC never stops in any mode (including RUN mode, SLEEP mode, STOP0 mode, STOP2 mode, STANDBY mode, and VBAT mode)
- RTC provides various wakeup sources that can wake the MCU from all low-power modes (SLEEP mode, STOP0 mode, STOP2 mode, and STANDBY mode)

2.23 Analog-to-Digital Converter (ADC)

The 12-bit ADC is a high-speed analog-to-digital converter using successive approximation. There are 3 ADCs in total, where ADC1/ADC2 can form a dual ADC configuration, and ADC1/ADC2/ADC3 can form a triple ADC configuration. Each ADC has up to 20 multiplexed channels, and A/D conversion on various channels can be performed in single, continuous, scan, or discontinuous modes. ADC conversion values are stored (left-aligned or right-aligned) in 16-bit data registers. Input voltage can be monitored through analog watchdogs 1/2/3 to detect if it's within user-defined high/low thresholds, and the maximum input clock frequency for the ADC is 20MHz.

Main ADC features are described as follows:

- Supports 3 ADCs with single-ended and differential inputs
- Supports 12-bit and 10-bit resolution
- Supports triggered sampling, including EXTI/TIMER
- Each ADC has 3 analog watchdogs
- Interrupts can be triggered when ADC is ready, sampling complete, conversion complete, or analog watchdog 1/2/3 events
- Supports 4 conversion modes:
    - Single conversion
    - Continuous conversion
    - Discontinuous mode
    - Scan mode
- Supports self-calibration
- Data alignment with embedded data consistency
- Independently programmable sampling time intervals for all channels
- Can manage single-ended inputs or differential inputs (programmable by channel)
- ADC clock source from PLL clock or AHB clock
- Data can be managed by DSMU, DMA
- Regular channel conversion implemented based on FIFO
- Conversion start methods:
    - Software-triggered regular and injected conversions
    - Polarity-configurable external triggers (GPIO input events or internal timer events) for regular and injected conversions
- Oversampling:
    - Adjustable oversampling ratios: x1, x2, x4, x8, x16, x32, x64, x128, x256, x512, x1024
    - Configurable right data shift of 0-10 bits
    - 16-bit data result register
- Data preprocessing:
    - Supports gain compensation
    - Supports offset compensation
- Multi-ADC modes:
    - Dual ADC mode: combination of ADC1 and ADC2
    - Triple ADC mode: combination of ADC1, ADC2, and ADC3
- ADC operating voltage between 1.7V and 3.6V
- ADC supported conversion voltage range between VREF- and VREF+

2.24 Digital-to-Analog Converter (DAC)

The DAC is a digital-to-analog converter, primarily accepting digital inputs and providing voltage outputs. DAC data has two modes: 8-bit or 12-bit and supports DMA functionality. When the DAC is configured in 12-bit mode, DAC data can be left-aligned or right-aligned; when configured in 8-bit mode, DAC data is right-aligned. Each DAC has an independent converter that can perform conversions independently. In dual DAC mode, each DAC can either operate independently or two DACs (DAC1&DAC2, DAC3&DAC4 forming a group) can perform conversions and updates simultaneously. VREF+ is input through a pin as the DAC reference voltage, enabling higher precision in DAC conversion data.

When DAC output is internally connected to on-chip peripherals, the DACx_OUT pin can be used as a general-purpose input/output (GPIO). The DAC output buffer can be selectively enabled to achieve high drive output current.

Main features include:

- Supports 4 DACs, each corresponding to an independent DAC converter
- Supports 8-bit or 12-bit output, with data in 12-bit mode available in both right-aligned and left-aligned formats
- Dual DAC supports synchronized or independent conversion
- Each DAC supports DMA functionality and DMA underflow error detection
- DMA dual data mode to conserve bus bandwidth
- Noise wave, triangular waveform, and sawtooth wave generation
- DAC output supports connections to on-chip peripherals
- Buffer offset calibration
- Input reference voltage supports VREF+
- External events triggered conversion

2.25 Analog Comparator (COMP)

The COMP module is used to compare the magnitude of two input analog voltages and output a high/low level based on the comparison result. When the voltage at the "INP" input is higher than the voltage at the "INM" input, the comparator outputs a high level; when the voltage at the "INP" input is lower than the voltage at the "INM" input, the comparator outputs a low level.
Main comparator functions include:

- 4 independent comparators
- Two built-in 64-level programmable comparison voltage reference sources: VREF1 and VREF2
- Supports filter clock and filter reset
- Configurable output polarity (high or low)
- Supports 4 programmable hysteresis levels
- Comparison results can be output to I/O ports or trigger timers for capture events, OCREF_CLR events, brake events, or to generate interrupts
- Input channels can multiplex I/O ports, VREF1, VREF2, and outputs from general 12-bit DAC channels
- Configurable as read-only or read-write; when locked, requires reset to unlock
- Supports blanking with configurable blanking sources
- COMP1/COMP2 and COMP3/COMP4 can form window comparators

- Can wake the system from Sleep mode by generating interruptions
- Configurable filter window size
- Configurable filter threshold size
- Configurable sampling frequency for filtering

2.26 Voltage Reference Buffer (VREFBUF)

The chip has a built-in voltage reference buffer that can be used as a voltage reference for ADC, 12bit-DAC, and COMP internal 6bit-DAC. It can also serve as a voltage reference for external components through the VREF+ pin.

2.27 Timers and Watchdogs

Supports up to 2 advanced timers, 7 general-purpose timers A, 3 general-purpose timers B, 4 basic timers, 5 low-power timers, as well as 1 independent watchdog timer, 1 window watchdog timer, and 1 system tick timer.

The following table compares the functionality of advanced timers, general-purpose timers, basic timers, and low-power timers:

Table 2-3 Timer Function Comparison

Timer	Counter Resolution	Counter Type	Prescaler Factor	Capture/Compare Channels	Complementary Outputs
ATIM1~2	16-bit	Up, Down, Up/Down	Any integer between 1~65536	4	4
GTIMA1~7	16-bit	Up, Down, Up/Down	Any integer between 1~65536	4	None
GTIMB1~3	16-bit	Up, Down, Up/Down	Any integer between 1~65536	4	1
BTIM1~4	32-bit	Up	Any integer between 1~65536	0	None
LPTIM1~5	16-bit	Up	1, 2, 4, 8, 16, 32, 64, 128	0	None

2.27.1 Ultra-High Precision Timer (SHRTIM)

Supports two ultra-high precision timers.
The high-resolution timer can generate up to 12 highly precise digital timing signals, primarily used to drive switched-mode power supplies or lighting systems in power conversion systems, but also applicable to applications requiring extremely high time resolution.

This timer adopts a modular architecture capable of generating independent or coupled waveforms. The waveforms are determined by independent timing signals (using counters and comparison units) and various external events (such as analog or digital feedback and synchronization signals), enabling the generation of a wide variety of control signals (PWM, phase shift, constant Ton...) to meet the needs of most conversion topologies.

For control and monitoring purposes, this timer also features timing measurement functions and connects to built-in ADC and DAC converters. Additionally, the timer has light-load management modes and can handle various fault mechanisms for safe shutdown.

Main features include:

- Multiple timing units
  - 100ps resolution, with full resolution support for all outputs, adjustable duty cycle, frequency, and pulse width in trigger single-pulse mode
  - 6 16-bit timing units (each timing unit includes 1 independent counter and 5 comparison units (comparison unit 5 dedicated to ADC triggering))
  - 12 outputs controllable by any timing unit, with up to 32 set/reset sources per channel
  - Modular structure to meet the needs of various independent converters with 1 or 2 switches, as well as some large multi-switch topologies
- Up to 10 external events, usable for any timing unit
  - Programmable polarity and edge validity
  - 10 events for fast asynchronous mode
  - 10 events for programmable digital filters
  - Pseudo-event filtering using blanking and window modes
  - All 10 external events fully mapped to any GPIO or any analog comparator
- Multiple channels connected to built-in analog peripherals
  - 10 trigger signals for ADC converters, fully mappable to any comparison unit
  - 3 trigger signals for DAC converters
  - 7 comparators for analog signal conditioning
- Rich protection mechanisms
  - 6 fault inputs that can be used in combination and associated with any timing unit
  - All 6 fault inputs fully mappable to any analog comparator
  - Programmable polarity and edge validity, digital filters
  - Specialized delay protection for resonant converters
- Multiple SHRTIM instances can be synchronized with external synchronization inputs/outputs
- Multifunctional output stage
  - Full resolution time insertion
  - Programmable output polarity
  - Chopper mode
- Burst mode controller for handling light-load operations on multiple converters simultaneously, supporting 32-bit burst mode counting
- 8 interrupt vectors, each with up to 14 sources
- 7 DMA requests, with up to 14 sources, allowing multi-register updates through burst mode

2.27.2 Advanced Timers (ATIM1~4)

Advanced control timers (ATIMx) are mainly used for the following scenarios: counting input signals, measuring input signal pulse width, and generating output waveforms. Advanced timers feature complementary outputs, dead-time insertion, and brake functions, making them suitable for motor control.

Main features include:

- 16-bit auto-reload counter (supports up counting, down counting, up/down counting)

- 16-bit programmable prescaler (division factor configurable to any value between 1 and 65536)
- Programmable repetition counter
- ATIMx with up to 9 channels
- 4 capture/compare channels, operating modes: PWM output, output compare, single-pulse mode output, input capture
- 2 brake input signals supporting digital filtering
- Interrupts/DMA generated when the following events occur:
    - Update event
    - Trigger event
    - Input capture
    - Output compare
    - Brake signal input
- Complementary outputs with programmable dead time
    - For ATIMx, channels 1, 2, 3, 4 support this feature
- Timer control via external signals
- Multiple timers internally connected to achieve timer synchronization or linking
- Incremental (quadrature) encoder interface: for tracking running trajectories and decoding rotational orientation
- Hall sensor interface: for three-phase motor control
- Trigger input as external clock or for per-cycle current management

2.27.3 General-Purpose Timers (GTIMA1~7)

General-purpose control timers (GTIMAx) are mainly used for the following scenarios: counting input signals, measuring input signal pulse width, and generating output waveforms.
Main features include:

- 16-bit auto-reload counter (supports up counting, down counting, up/down counting)
- 16-bit programmable prescaler (division factor configurable to any value between 1 and 65536)
- GTIMAx with up to 4 channels
- Channel operating modes: PWM output, output compare, single-pulse mode output, input capture
- Interrupts/DMA generated when the following events occur:
    - Update event
    - Trigger event
    - Input capture
    - Output compare
- Timer control via external signals
- Multiple timers internally connected to achieve timer synchronization or linking
- Incremental (quadrature) encoder interface: for tracking running trajectories and decoding rotational orientation
- Hall sensor interface: for three-phase motor control

2.27.4 General-Purpose Timers (GTIMB1~3)

General-purpose control timers (GTIMBx) are mainly used for the following scenarios: counting input signals, measuring input signal pulse width, and generating output waveforms. General-purpose timers (GTIMBx) feature complementary outputs, dead-time insertion, and brake functions.

Main features include:

- 16-bit auto-reload counter (supports up counting, down counting, up/down counting)
- 16-bit programmable prescaler (division factor configurable to any value between 1 and 65536)
- Programmable repetition counter
- GTIMBx with up to 5 channels
- 4 capture/compare channels, operating modes: PWM output, output compare, single-pulse mode output, input capture
- 1 brake input signal supporting digital filtering
- Interrupts/DMA generated when the following events occur:
    - Update event
    - Trigger event
    - Input capture
    - Output compare
    - Brake signal input
- Complementary outputs with programmable dead time
    - For GTIMBx, channel 1 supports this feature
- Timer control via external signals
- Multiple timers internally connected to achieve timer synchronization or linking
- Incremental (quadrature) encoder interface: for tracking running trajectories and decoding rotational orientation
- Hall sensor interface: for three-phase motor control
- Trigger input as external clock or for per-cycle current management

2.27.5 Basic Timers (BTIM1~4)

Basic timers include a 32-bit auto-reload counter.
Main features include:

- 32-bit auto-reload up-counting counter
- 16-bit programmable prescaler (division factor configurable to any value between 1 and 65536)
- Interrupts/DMA generated for the following events:
    - Update event

2.27.6 Low-Power Timers (LPTIM1~5)

LPTIM is a 16-bit timer with multiple clock sources that can continue running in all power modes. LPTIM can operate without an internal clock source and can be used as a "pulse counter." Additionally, LPTIM can wake the system from low-power modes, implementing a "timeout function" with extremely low power consumption.

Main features include:

- 16-bit up counter
- 3-bit prescaler, 8 division factors (1, 2, 4, 8, 16, 32, 64, 128)
- Multiple clock sources
    - Internal clock sources: LSE, LSI, HSI, MSI, or APB clock

  - External clock source: external clock input through LPTIM Input1 (operates without LP oscillator running, used for pulse counter applications)

- 16-bit auto-reload register (LPTIM_ARR)
- 16-bit compare register (LPTIM_CMP)
- Continuous or single-trigger counting modes
- Programmable software or hardware input triggers
- Programmable digital filter for filtering glitches
- Configurable output (PWM)
- Configurable IO polarity
- Encoder mode
- Pulse counting mode, supporting single-pulse counting, dual-pulse counting (quadrature and non-quadrature)

2.27.7 Watchdog Timers (WDG)

Built-in Independent Watchdog (IWDG) and Window Watchdog (WWDG) timers solve problems caused by software errors. Watchdog timers are very flexible in use, improving system security and timing control accuracy.

Independent Watchdog (IWDG)

The Independent Watchdog (IWDG) is driven by the 32KHz Low-Speed Internal clock (LSI clock), allowing it to continue running even when infinite loops or MCU lockups occur. This provides a higher level of security, timing accuracy, and watchdog flexibility. It can resolve system failures caused by software faults through reset. IWDG is best suited for applications that require the watchdog to run as a completely independent process outside the main application but with lower timing precision requirements.

Main features include:

- Independent 12-bit down counter
- RC oscillator provides an independent clock source, can operate in SLEEP, STOP0, and STANDBY modes
- Can match reset and low-power wakeup
- System reset when the down counter reaches 0x000 (if the watchdog is activated)

Window Watchdog (WWDG)

The Window Watchdog (WWDG) clock is derived from the APB1 clock frequency divided by 4096, and it detects abnormal program execution through time window configuration. Therefore, WWDG is suitable for precise timing and is commonly used to monitor software failures caused by external interference or unforeseen logical conditions that cause applications to deviate from their normal operation sequence.

Main features include:

- Programmable 14-bit independent down counter
- When WWDG is enabled, reset occurs under the following conditions:
  - The down counter value is less than 0x40
  - The counter is reloaded when the decremented counter value is greater than the window register value
- Early wakeup interrupt

2.28 I²C Bus Interface

The I2C (Inter-Integrated Circuit) bus is a widely used bus structure that has only two bidirectional lines: the data bus SDA and the clock bus SCL. Through these two lines, all I2C bus-compatible devices can communicate directly with each other via the I2C bus.

The I2C bus interface handles communication between the microcontroller and the serial I2C bus. It provides multi-master functionality and can control all I2C bus-specific sequences, protocols, arbitration, and timing. It supports Standard Mode (Sm), Fast Mode (Fm), and Fast Mode Plus (Fm+). It is also compatible with SMBus (System Management Bus) and PMBus (Power Management Bus). The I2C interface module also supports DMA mode, which can effectively reduce CPU burden.

The main features of the I2C interface are described as follows:

- I2C Bus Specification Version 3 Compatibility:
  - Slave mode and master mode
  - Multi-master functionality
  - Standard Mode (up to 100 kHz) / Fast Mode (up to 400 kHz)
  - Fast Mode Plus (up to 1 MHz) / High-Speed Mode (up to 3.4 MHz)
  - 7-bit and 10-bit addressing modes
  - Multiple 7-bit slave addresses (2 slave address registers, 1 with configurable mask bit section)
  - All 7-bit address acknowledge mode
  - Broadcast call
  - Software-configurable data setup and hold times on the bus
  - Interrupts and clock stretching
- SMBus Specification Version 3.0 Compatibility:
  - Hardware CRC (packet error checking) generation and verification with ACK control
  - Command and data acknowledgment control
  - Support for Address Resolution Protocol (ARP)
  - Host and device support
  - SMBus alert
  - Timeout and idle state detection
- PMBus Rev 1.3 Standard

Other Features:

- Programmable buffer of up to 8 bytes / burst buffer with DMA
- Programmable analog and digital noise filters
- Independent clock source, making I2C communication speed unaffected by i2c_pclk reprogramming

2.29 Flexible External Memory Controller (FEMC)

The Flexible External Memory Controller (FEMC) is used to access various off-chip memory devices. It allows for convenient expansion of different types of large-capacity static memory according to application needs, enabling the simultaneous expansion of multiple different types of static memory without adding external interfaces. All external memory devices share the address, data, and control signals output by the FEMC controller, which distinguishes different external devices through a unique chip select signal.

Main features include:

- Supports expansion of the following devices:
  - SRAM
  - PSRAM
  - ROM
  - NOR Flash
  - NAND Flash (SLC)
  - LCD (8080/6800)
- Supports two NAND flash blocks, with hardware 1bit-ECC that can detect up to 2K bytes of data
- Supports burst access mode for synchronous devices, such as NOR flash and PSRAM
- Supports 8/16/32-bit data bus
- Each memory block has an independent chip select control
- Supports various devices through timing programming
- Automatically converts 64-bit AXI access requests into consecutive 32-bit, 16-bit, or 8-bit access requests based on the data width of the external memory, to communicate with external 32-bit, 16-bit, or 8-bit memory devices
- Supports write enable and byte select output for PSRAM and SRAM devices
- External asynchronous wait control
- Supports low-power management

2.30 Universal Synchronous Asynchronous Receiver Transmitter (USART)

The Universal Synchronous Asynchronous Receiver Transmitter (USART) is a full-duplex serial data exchange interface that supports both synchronous and asynchronous communication. It can be flexibly configured to facilitate full-duplex data exchange with various external devices.

The USART interface offers configurable transmission and receiving baud rates and supports continuous communication via DMA. USART also supports multi-processor communication, LIN mode, synchronous mode, single-wire half-duplex communication, smart card asynchronous protocol, IrDA SIR ENDEC functionality, and hardware flow control.

Main Features:

- Supports full-duplex, asynchronous communication
- Supports single-wire half-duplex communication
- Configurable baud rate, with maximum baud rate up to 37.5Mbit/s
- Supports 8x or 16x oversampling
- Supports 8-bit or 9-bit data frames
- Supports two internal FIFOs for receiving and transmitting data
- Supports 1-bit or 2-bit stop bits
- Supports hardware-generated parity bits and parity checking
- Supports hardware flow control: RTS, CTS
- Supports RS-485

- Supports DMA transmission and reception
- Supports multi-processor communication enters silent mode if address doesn't match, can be awakened via idle bus detection or address identification
- Supports synchronous mode, allowing users to control bidirectional synchronous serial communication in master mode
- Supports smart card asynchronous protocol, compliant with ISO7816-3 standard
- Supports serial infrared protocol (IrDA SIR) encoding and decoding, providing normal and low-power operation modes
- Supports LIN mode
- Supports multiple clock error detection: data overflow error, frame error, noise error, verification error
- Supports multiple interrupt requests: transmit data register empty, CTS flag, transmission complete, data received, data overflow, bus idle, parity error, LIN mode break frame detection, and noise flag/overflow error/frame error in multi-buffer communication

Mode Configuration:

Communication Mode	USART1~USART8	UART9~UART15
Asynchronous Mode	Y	Y
Multi-processor	Y	Y
LIN	Y	Y
Synchronous Mode	Y	N
Single-wire Mode (Half-duplex)	Y	Y
Smart Card Mode	Y	N
IrDA Infrared Mode	Y	Y
DMA Communication Mode	Y	Y
Hardware Flow Control Mode	Y	Y

Y = Supports this mode, N = Does not support this mode

2.31 Low Power Universal Asynchronous Receiver Transmitter (LPUART)

The Low Power Universal Asynchronous Receiver Transmitter (LPUART) is a low-power, full-duplex, asynchronous serial communication interface. LPUART can be clocked by LSE, HSE, HSI, MSI, SYSCLK, and PCLK. When the 32.768kHz LSE is selected as the clock source, LPUART can operate in STOP0/2 low-power modes with a maximum communication rate of 9600bps. LPUART supports data reception wake-up. By configuring wake-up events, the CPU can be awakened from STOP0/2 mode.

At the same time, when the MCU is operating in RUN mode, LPUART can also be used as a regular asynchronous serial port. Users can switch the clock source to HSI, SYSCLK, or PCLK to achieve higher communication speeds.

Main Features of LPUART:

- Full-duplex asynchronous communication
- Selectable clock sources: HSI, HSE, LSE, MSI, SYSCLK, or PCLK
- Fractional baud rate generator system: programmable baud rates up to 5Mbits/s shared for transmission and reception; baud rates from 300bps to 9600bps when using a 32.768 kHz clock source (LSE)

- Fixed 8-bit data word length, 1 stop bit, and optional 1 parity bit
- Supports DMA data transfer
- Supports hardware flow control
- Transmission detection flags: receive buffer full, receive buffer half-full, receive buffer not empty, receive buffer overflow, transmission complete, transmit buffer full, transmit buffer half-full, transmit buffer not empty
- Parity control: parity selection, parity can be disabled
- Error detection flags: parity error, overflow error, noise error
- 32-byte receive buffer, 8-byte transmit buffer
- Low-frequency baud rate error correction
- Configurable sampling method with 1 or 3 samples
- Noise detection
- Configurable RTS threshold for flow control
- Supports configurable source modes in STOP0/2 mode: start bit detection, receive buffer not empty detection, a configurable received byte (1-32 bytes), and programmable 8-byte frame

2.32 Controller Area Network with Flexible Data Rate (CAN FD)

The FDCAN module complies with the ISO 11898-1:2015 standard, supporting CAN 2.0A/B and CAN FD protocols, and is compatible with the non-ISO standard Bosch protocol.

In addition, CAN modules FDCAN1&2&3&4 also support time-triggered CAN (TTCAN) as specified in ISO 11898-4, including event-synchronized time-triggered communication, global system time, and clock drift compensation. FDCAN1&2&3&4 include dedicated additional registers for time-triggered functionality. CANFD can be used optionally with both event-triggered and time-triggered CAN communication.

The FDCAN modules share two message RAM areas. Each FDCAN can freely select either SRAM5 BANK1 or SRAM5 BANK2 for receiving message filters, receiving FIFOs, receive buffers, transmit buffers, transmit event FIFOs (and TTCAN triggers). The message RAM is in the MCU's internal SRAM, with configurable start addresses, and a single FDCAN can be allocated a maximum of 4480 words (32-bit).

Main Features:

- Completes with ISO 11898-1:2015 and ISO 11898-4 standards
- Supports CAN FD with up to 64 bytes of data
- Supports fully hardware-implemented TTCAN Level 1 and Level 2 (only supported by FDCAN1/2/3/4)
- Supports CAN error logging
- Supports AUTOSAR standard
- Supports SAE J1939 standard
- Enhanced receive filtering functionality
- Two configurable receive FIFOs
- Separate signal indication when receiving high-priority messages
- Up to 64 dedicated receive buffers

- Up to 32 dedicated transmit buffers
- Configurable transmit FIFO or queue
- Configurable transmit event FIFO
- Supports configurable message RAM, shared by 8 FDCAN controllers
- Programmable loopback test mode
- Maskable module interrupts
- Two clock domains: CAN core clock and APB bus clock
- Supports power-down mode

2.33 Serial Peripheral Interface/Inter-IC Sound Bus (SPI/I2S)

SPI allows chips to communicate with external devices in half/full-duplex, synchronous, serial mode. SPI can be configured in master mode and multi-master mode, and provides communication clock (SCK) for external slave devices. It can be used for various purposes, including two-wire simplex synchronous transmission using one bidirectional data line, and also supports hardware CRC verification.

I2S is also a synchronous serial interface communication protocol. It supports four audio standards, including Philips I2S standard, MSB and LSB aligned standards, and PCM standard. In half-duplex communication, it can work in both master and slave modes. When working as a master device, it can provide clock signals to external slave devices through the interface.

Main Features of SPI Interface:

- Full-duplex and simplex synchronous modes
- Supports master mode, slave mode, and multi-master mode
- Supports 8-bit or 16-bit data frame formats
- Programmable data bit order
- Hardware or software chip select management
- Configurable clock polarity and clock phase
- Hardware CRC calculation and verification support for transmission and reception
- Supports DMA transfer functionality
- 8-byte receive/transmit FIFO

Main Features of I2S Interface:

- Half-duplex and full-duplex synchronous modes
- Supports master mode and slave mode operation
- Supports 4 audio standards: Philips I2S standard, MSB-aligned standard, LSB-aligned standard, and PCM standard
- Configurable audio sampling frequency ranging from 8KHz to 192KHz
- Configurable steady-state clock polarity
- MSB data direction
- Supports DMA transfer functionality

- Supports multiple selectable clock sources

2.34 Multiple-line Serial Peripheral Interface (xSPI)

xSPI is an interface for single/dual/quad/octal line SPI peripheral communication. It can operate in two modes: indirect mode and memory-mapped mode.

Supported modes include:

- Indirect mode: All operations are performed using xSPI registers
- Memory-mapped mode: External flash is mapped to the microcontroller address space, and the system treats it as internal storage space

Main Features:

- Data communication supports single/dual/quad/octal line modes
- Supports Single SPI/Normal SPI, DUAL SPI, QUAD SPI, Dual-QUAD, and OCTAL SPI modes
- Maximum transmission rate up to 133MHz
- Supports Motorola SPI:
    - Standard/Dual/Quad/Octal SPI
- Supports Single Data Rate (SDR) and Double Data Rate (DDR) modes
- Read data strobe and data masking support for DDR transfers
- Supports clock extension
- Frame format and operation codes are software configurable in both indirect and memory-mapped modes
- Integrated FIFO for transmission and reception
- Allows 8/16/32-bit data access
- Dedicated 32×32bit TX FIFO and 32×32bit RX FIFO
- Supports DMA
- XIP mode supports SPI read operations but does not support XIP write operations
    - Supports continuous transfer mode
    - Supports data prefetching
- Supports automatic code decryption execution for XSPI peripherals, meaning code is stored encrypted in XSPI peripherals and automatically decrypted to plaintext for CPU execution when reading, without affecting access speed to peripheral storage; decryption can be enabled/disabled via software, with the root key stored in the NVR area, inaccessible to users
- Supports serial NAND FLASH, NOR FLASH, and PSRAM
- In master mode, supports 4 external chip select output controls; in slave mode, supports 1 chip select input; in master mode, all IOs multiplexed as chip select outputs can be multiplexed as chip select inputs in slave mode
- Supports multi-master arbitration functionality

2.35 Universal Serial Bus High-Speed Dual Role Interface (USB_HS_DualRole)

The USB High-Speed Dual Role Interface (USB HS Dual Role), hereinafter referred to as USBHS, is designed to provide a standard interface for high-speed data transfer and connection to external devices. USBHS supports both Host mode and Device mode. USBHS includes an internal USB high-speed PHY that can be configured for high-speed and full-speed operation, eliminating the need for an external PHY chip. USBHS supports all four transfer types defined by the USB 2.0 protocol (control transfer, bulk transfer, interrupt transfer, and isochronous transfer). Additionally, USBHS contains an internal DMA that can function as an AHB bus master to accelerate data transfer between USBHS and the system.

Main Features:

- Supports USB 2.0 High-speed (480Mb/s)/Full-speed (12Mb/s)/Low-speed (1.5Mb/s) Host mode
- Supports USB 2.0 High-speed (480Mb/s)/Full-speed (12Mb/s) Device mode
- Supports all 4 transfer types: control transfer, bulk transfer, interrupt transfer, and isochronous transfer
- Built-in high-speed PHY in USBHS supports high-speed, full-speed, and low-speed operation without requiring an external PHY
- Supports HS SOF, FS SOF, and LS Keep-alive tokens
- SOF pulse can be output through PAD
- SOF pulse is internally connected to timer (TIMx)
- Supports A-B device identification (ID line)
- USBHS has embedded DMA with software-configurable AHB bulk transfer types
- Features power-saving functions, such as stopping the system during USB suspension, turning off digital module clocks, and managing PHY and DFIFO power
- Features 4 KB dedicated RAM
- In Host mode, includes 16 host channels, each supporting any type of USB transfer
- Built-in hardware scheduler in Host mode:
    - Stores up to 16 interrupt plus isochronous transfer requests in periodic hardware queue
    - Stores up to 16 control plus bulk transfer requests in non-periodic hardware queue
- In Host mode, includes one RX FIFO, one periodic transfer TX FIFO, and one non-periodic transfer TX FIFO
- In Device mode, includes 1 bidirectional control endpoint 0, as well as 8 IN endpoints and 8 OUT endpoints; both IN endpoints and OUT endpoints can be configured for bulk transfer, interrupt transfer, or isochronous transfer
- Device mode includes one shared RX FIFO and one TX-OUT FIFO, as well as 9 dedicated TX-IN FIFOs
- Supports soft disconnect functionality

2.36 Secure Digital MultiMedia Card (SDMMC)

The SDMMC provides a host interface for SD storage cards, SDIO cards, and MMC devices, supporting only one protocol stack version of SD/SDIO/MMC cards at a time.

The basic transmission for bus communication is command/response, where these types of bus transfers directly transmit information in the command or response structure. Data transfers include block mode, SDIO multi-byte mode, and MMC continuous data stream mode.

Main Features:

- Compatible with SD Host Controller Standard Specification V3.00
- Compatible with SD Physical Layer Interface Specification V3.00
- Compatible with SDIO Standard Specification V3.00
- Compatible with eMMC Standard Specification V4.51
- Supports 1-bit/4-bit SD card and SDIO modes
- Supports UHS-I interface, requiring level conversion when external devices use 1.8V power supply
- Supports DS, HS, SDR12, SDR25, SDR50, DDR50, and SDR104 transfer modes
- Supports 1-bit, 4-bit, and 8-bit MMC modes and BOOT mode
- Supports single block/multiple block read and write
- Supports maximum block size of 512 bytes in SD & SDIO modes, and maximum block size of 2048 bytes in eMMC mode
- EMMC maximum clock frequency of 200MHz (limited by maximum I/O frequency), with maximum transfer rate up to 1.6Gbps (HS200 mode, 8-bit)
- Fully configurable 2048*2 byte read/write FIFO
- Supports internal dedicated DMA functionality

2.37 Digital Video Port (DVP) Interface

The DVP is a flexible and powerful CMOS optical sensor interface that can easily meet customers' image acquisition requirements, with the entire acquisition process requiring no CPU intervention.

This module can receive high-speed data from traditional or ITU-R BT.656 format CMOS image sensors. It also supports data formats including YCbCr422 and RGB565 progressive, and compressed data (JPEG).

Main Features:

- Pure hardware acquisition method
- Pure input interface
- Supports 8-bit, 10-bit, 12-bit, and 16-bit traditional synchronous parallel interfaces
- Supports 8-bit and 10-bit ITU-R BT.656 video formats
- Supports 8-bit and 16-bit YCbCr, YUV, and RGB data formats
- Supports 8-bit, 10-bit, and 16-bit Bayer data formats
- Supports clock output (via MCO output, typical value 48MHz) to provide clock for external CMOS optical sensors
- Input pixel clock DVP_PCLK, frame synchronization signal DVP_VSYNC, and line synchronization signal DVP_HSYNC polarities can all be independently configured
- Features 16x4 byte FIFO for receiving pixel data

- Supports FIFO overflow protection
- Supports DMA, requiring no CPU intervention throughout the image acquisition process
- Image acquisition size must be a multiple of 4 bytes
- Supports hardware inversion of acquired image data
- Maximum support for 1280*720@30 Hz
- Supports continuous mode and snapshot mode
- Supports hardware cropping
- Supports multiple data formats:
    - YCbCr422 progressive video
    - RGB565 progressive video
    - Compressed data (JPEG)

2.38 Graphics Processing Unit (GPU)

Supports a 2.5D GPU for high-resolution displays in embedded systems. This module is optimized even when processing millions of pixels per frame.

The main features supported by the 2.5D GPU are as follows:

High Rendering Quality

- Subpixel precise rendering
- Direct edge anti-aliasing
- Primitive edge blurring
- Static dithering during framebuffer writeback enhances RGB565 output

High Performance

- 300M pixels/second fill rate (300MHz clock, single pipeline)
- Prefetch cache

Hardware Accelerated Primitives

- Fast clear/rectangle fill
- Lines
- Triangles
- Quadrilaterals
- Bezier curves
- Advanced Blit operations supporting scaling, stretching, rotation, shading, and Alpha blending
- Convolution filtering

Blending

- Normal Alpha blending
- Independent Alpha/color blending
- Source/destination factors: 0, 1, source Alpha, 1-source Alpha

Textures

- Supports 4096 x 4096 texture size

- Flexible texture color format handling
    - ARGB8888, RGBA888, RGB888, BGR888, ARGB8565, RGBA5658, ARGB4444, RGBA4444, ARGB1555, RGBA5551, RGB565, AL88, AL44, AL17, AL8, AL4, AL2, AL1, ARGB2222, RGBA2222
- CLUT (Color Look-Up Table) index formats
    - Applicable to all ALx formats
- RLE texture decompression
- Texture addressing modes
    - Standard linear
    - Scrambling
    - Reverse scrambling
    - Virtual tiling

Framebuffer

- Supports 4096 x 4096
- ARGB8888, RGBA888, RGB888, BGR888, ARGB8565, RGBA5658, ARGB4444, RGBA4444, ARGB1555, RGBA5551, RGB565, A8, L8, AL17, ARGB2222, RGBA2222
- Blending modes: blend, multiply, multiply-add, darken, lighten

Performance Validation

- Performance counters
- Visual enumeration efficiency
- Visual cache burst access length

2.39 Image Codec (JPEG)

Supports a JPEG codec to encode or decode uncompressed image data streams in JPEG compression mode, compliant with ISO/IEC 10918-1 standard.

ENCODER Main Features:

- Supports single frame images and Motion JPEG payloads
- Supports 8-bit color component sampling
- Supports up to 3 color components
- Supports maximum image size of 64K x 64K
- Supports YCbCr and BW (grayscale) image color spaces
- YCbCr/YUV 4:4:4, 4:2:2, 4:2:0
- Configurable JPEG header generator
- 3 programmable 8-bit quantization tables
- 4 programmable Huffman tables (two AC tables and two DC tables)

- Minimum Coding Unit (MCU) fixed at 8 x 8

DECODER Main Features:

- Supports single frame images and Motion JPEG payloads
- Supports 8-bit color component sampling
- Supports up to 3 color components
- Supports maximum image size of 64K x 64K
- Supports YCbCr and BW (grayscale) image color spaces
- YCbCr/YUV 4:4:4, 4:2:2, 4:2:0
- Configurable JPEG header generator
- 3 programmable 8-bit quantization tables
- 4 programmable Huffman tables (two AC tables and two DC tables)

2.40 Ethernet (ETH)

N32H787 supports two Ethernet peripheral modules: ETH1 with 10/100/1000Mbps Ethernet MAC, and ETH2 with 10/100Mbps Ethernet MAC. The Ethernet modules use dedicated DMA to optimize packet transmission and reception performance. The ETH modules support standard interfaces for communication with the physical layer (PHY): MII, RMII, GMII (Note: ETH2 does not support GMII interface) for sending and receiving Ethernet packets.

Main Features:

MAC Tx and Rx Common Features

- Provides independent transmission, reception, and control interfaces for applications
- Supports the following PHY interfaces for 10/100/1000Mbps data transfer rates:
  - MII, for communication with external Fast Ethernet PHY
  - RMII, for communication with external Fast Ethernet PHY
  - GMII, for communication with external Gigabit Ethernet PHY
- Half-duplex operation:
  - Supports CSMA/CD protocol
  - Supports backpressure flow control
- 32-bit data transfer interface on application side
- Full-duplex flow control operation (IEEE 802.3x pause packets and priority flow control)
- Supports enforced network statistics via RMON or MIB counters (RFC2819/RFC2665)
- Ethernet packet timestamping as described in IEEE 1588-2002 and IEEE 1588-2008 (64-bit timestamp in Tx or Rx status of PTP packets), supports one-step and two-step timestamping in TX direction
- Supports flexible control of second pulse output (PPS)
- Supports MDIO (Clause 22 and Clause 45) master interface for configuration and management of PHY devices

MAC Tx Features

- Preamble and SFD insertion in transmit path
- Individual 32-bit status for each packet transmitted by the application
- Automatic CRC generation and padding bytes (PAD) based on each packet
- Programmable packet length to support standard Ethernet packets or jumbo Ethernet packets up to 16KB
- Programmable inter-packet gap (40~96 bits, with 8-bit step length)
- IEEE 802.3x flow control automatically transmits zero-wait pause packets when flow control input transitions from valid to invalid (in full-duplex mode)
- Source address field insertion or replacement, and VLAN insertion, replacement and deletion in transmitted packets (controlled per packet or using static-global control)
- Up to two VLAN tags can be inserted, replaced, or deleted
- Transmits packets with smaller preamble size in full-duplex mode
- Supports queue/channel-based VLAN tag insertion, replacement, or deletion

MAC Rx Features

- Automatic stripping of PAD and CRC in receive path
- Removal of preamble and SFD in receive path
- Programmable watchdog timeout limits
- Flexible address filtering:
    - 4 perfect 48-bit destination address (DA) filters with byte-wise masks
    - 4 source address (SA) comparison check filters with byte-wise masks
    - 64-bit hash filter for multicast and unicast (DA) addresses
    - Supports passing all multicast address packets
    - Supports promiscuous mode without filtering, passing all packets directly for network monitoring
    - Status report attached to all incoming packets (with each filtering)
- Additional packet filtering:
    - Based on VLAN tags: perfect match and hash filtering (filtering based on external or internal VLAN tags)
    - Based on Layer 3 and Layer 4: IPv4/IPv6-based TCP/UDP
- Supports IEEE 802.1Q VLAN tag detection and removal of VLAN tags in received packets
- Detection of remote wake-up packets and AMD magic packets
- Forwards received pause packets to application (in full-duplex mode)
- Layer 3/Layer 4 checksum offload for received packets

MTL Tx and Rx Common Features

- 32-bit transaction layer module (connecting application and MAC)
- Performs data transfers using simple FIFO protocol
- Packet-oriented transfers optimized with packet separators
- Dual-port RAM based on asynchronous FIFO controllers

- Programmable burst length up to half the size of MTL Rx or Tx queue to support burst data transfers in MTL configuration
- Programmable threshold capability for each queue (default threshold 64 bytes)

MTL Tx Features

- 2KB transmit FIFO with programmable threshold capability
- Supports one queue on transmit path
- Store-and-forward mode or threshold mode (cut-through mode)
- Automatic retransmission of collision packets in half-duplex mode
- Discards packets on late collision, excessive collision, excessive delay, and underrun
- Calculates and inserts IPv4 header checksum, and TCP, UDP, or ICMP checksum
- Statistics by generating pulses for packets dropped in transmit FIFO (due to underflow)
- Packet-level control:
    - VLAN tag insertion or replacement
    - Ethernet source address segment insertion
    - Layer 3/Layer 4 checksum insertion control
    - One-step timestamp
    - Timestamp control
    - CRC and PAD control

MTL Rx Features

- 2KB receive FIFO with configurable threshold
- Supports one queue on receive path
- Inserts Rx status vector into Rx queue after EOP/EOF (threshold mode) and before SOP/SOF
- Programmable Rx queue threshold in threshold mode (cut-through mode) (default fixed at 64 bytes)
- Can filter all error packets when receiving in store-and-forward mode and not forward them to the application
- Supports forwarding runt (undersized) error-free packets
- Statistics by generating pulses for packets lost in receive FIFO (due to overflow)
- Automatically generates pause packet control signal or backpressure signal to MAC based on Rx queue fill level

DMA Features

- 32-bit data transfers
- Separate DMA in transmit path and receive path
- Packet-oriented DMA transfers optimized with packet separators
- Supports byte-aligned addressing of data buffers
- Supports dual buffer (ring) descriptors
- Descriptor architecture allows transfer of large data blocks with minimal CPU intervention (up to 32K bytes of data per descriptor)

- Comprehensive status reporting for normal operation and transmission errors
- Burst length of Tx DMA and Rx DMA engines can be programmed separately to optimize host bus utilization
- Programmable interrupts for various operating conditions
- Packet-based transmission or reception completion interrupt control
- Supports round-robin or fixed priority arbitration between receive and transmit engines
- Start and stop modes
- Independent ports for host CSR (Control Status Register) access and host data interface
- Supports TCP Segmentation Offload (TSO)

AHB Master Interface Features

- 32-bit data for application data access
- Little-endian mode
- Software selection of AHB burst type (fixed burst, indefinite burst, or mixed burst)

AHB Slave Interface Features

- 32-bit data for CSR access
- Little-endian mode
- Supports all burst types

Monitoring, Testing, and Debugging Features

- Loopback mode under MII/GMII interface for debugging
- DMA status (Tx and Rx) as status bits
- Debug status register providing FSM states and FIFO fill levels in transmit and receive paths
- Application abort status bit
- MMC (RMON) module
- Current Tx or Rx buffer pointer as status register
- Current Tx or Rx descriptor pointer as status register
- Access to Tx or Rx queue memory via slave port for debugging

2.41 Cyclic Redundancy Check Calculation Unit (CRC)

The CRC calculation unit can generate CRC calculation results in 8-bit, 16-bit, or 32-bit input data according to specified generating polynomials. In other applications, CRC-based techniques are used to verify data transmission or storage integrity. Within the scope of functional safety standards, they provide a method to verify flash memory integrity. The CRC calculation unit helps calculate software signatures at runtime for comparison with reference signatures generated at link time and stored in given memory locations.

Main Features:

- Default use of CRC-32 (Ethernet) generating polynomial: 0x4C11DB7

  - X^32 + X^26 + X^23 + X^22 + X^16 + X^12 + X^11 + X^10 + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1
- Supports user-defined generating polynomials with configurable polynomial size: 7-bit, 8-bit, 16-bit, or 32-bit
- Can process 8-bit, 16-bit, or 32-bit input data
- Configurable CRC initial value
- Single input or output data register
- Built-in input buffer to avoid bus stalls during calculation
- 32-bit data CRC calculation completed in 4 AHB clock cycles (HCLK)
- Supports general-purpose 32-bit register (available for temporary data storage)
- Configurable input and output data bit order
- Supports XOR operations of input and output data with specified (configurable) data

2.42 Secure Data Processing Unit (SDPU)

The SDPU combines the SAC and SDMA modules together. SAC includes AES, DES, SM4, SHA, and RNGC (entropy post-processing) algorithms. SDMA transfers computation data from SRAM to SAC, and transfers calculation results from SAC to SRAM.

SDPU Main Features:

DES Symmetric Algorithm Support

- Supports DES and 3DES encryption/decryption operations
- TDES supports 2KEY and 3KEY modes
- Supports CBC and ECB modes

AES Symmetric Algorithm Support

- Supports 128bit/192bit/256bit key lengths
- Supports CBC, ECB, CTR modes

SM4 Symmetric Algorithm Support

- Supports CBC, ECB modes

SHA Hash Algorithm Support

- Supports SHA1/SHA224/SHA256/SHA384/SHA512

Random Number Generator (RNG) Support

- Supports True Random Number Generator (TRNG) and Pseudo-Random Number Generator (PRNG) modes
- Supports LSFR129 post-processing
- Supports XOR combining of all sources
- Supports FIPS-140 CAVP

Additional Features

- Supports simultaneous operation of RNG and other algorithms
- Supports FIFO configuration
    - Supports algorithm data configuration via FIFO
- Supports SDMA data transfer
    - Supports automatic data transfer from SRAM to SRAM as master data via AHB interface
    - Supports SRAM base address transfer via parameters
    - Supports maximum data transfer size of 4KB (1024 words)
    - Supports data transfer size checking
    - Supports CRC16 verification
    - SRAM maximum support of 2MB (512K words)
    - Supports data reconnection in cases of source/destination address offset = 1/2/3

2.43 Debug Interface (DBG)

Embedded with ARM's SWJ-DP interface, enabling software developers to use industry-standard debugging tools to debug and trace embedded firmware through JTAG or Serial Wire Debug access ports. Trace data can be captured via the trace port for recording and analysis.

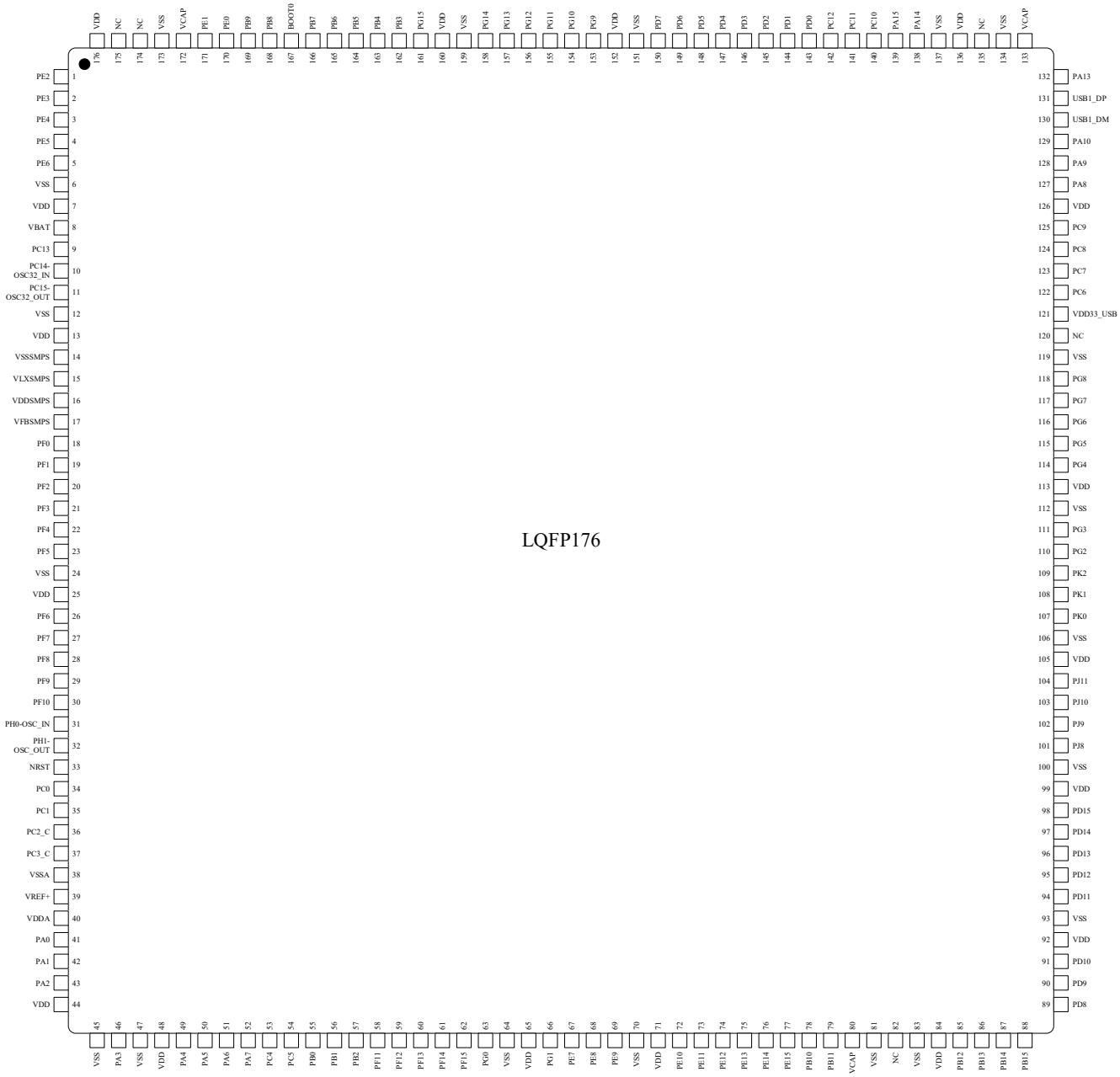
DBG Main Features:

- Breakpoint debugging
- Code execution tracing
- Software instructions
- JTAG debug port
- Serial Wire Debug port
- Trigger inputs and outputs
- Serial Wire Trace port
- Synchronous Trace port
- Debugging and tracing in low-power modes

3 Pin Definition and Description

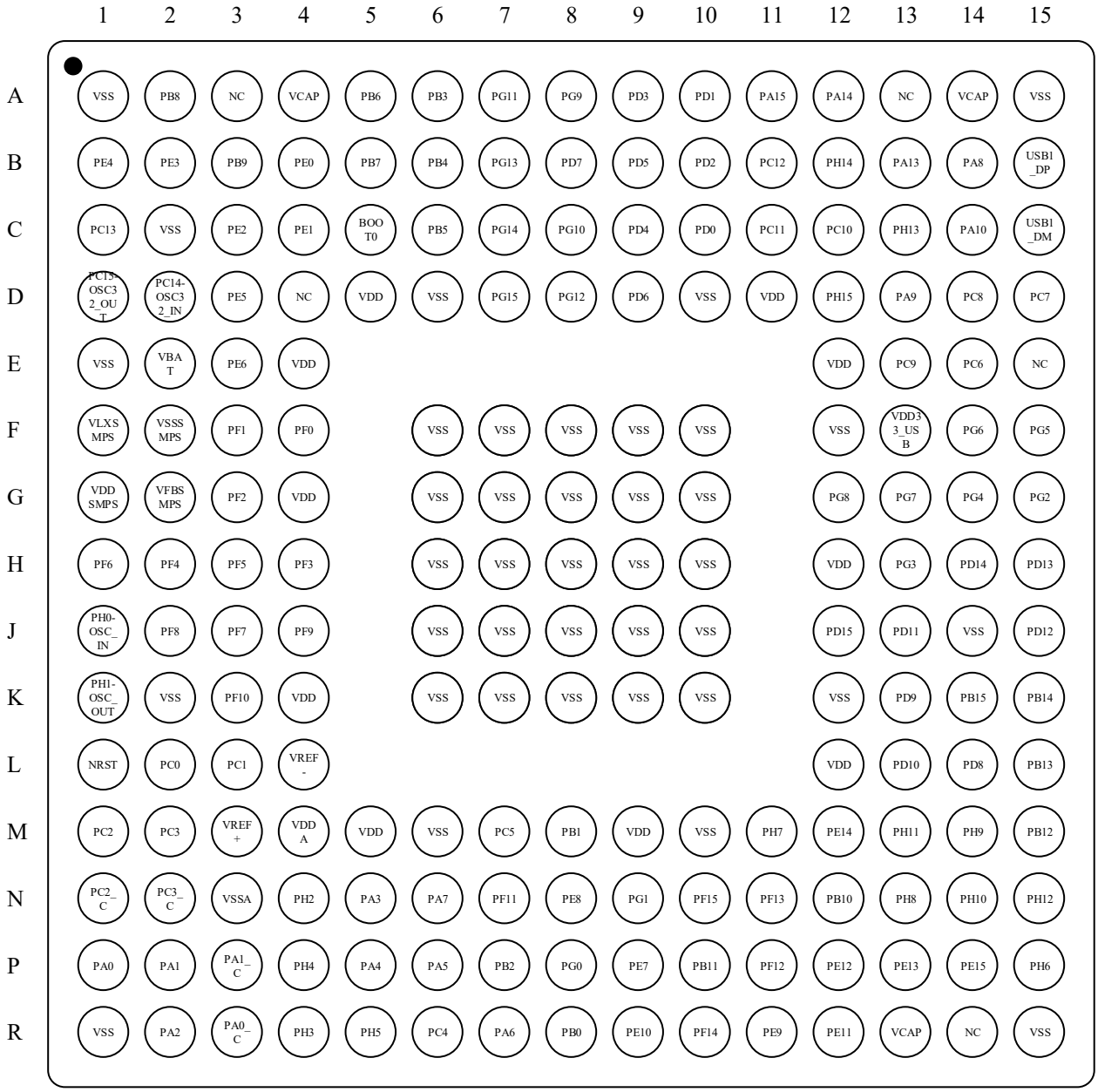
3.1 Package Diagram

3.1.1 LQFP176 Pin Distribution



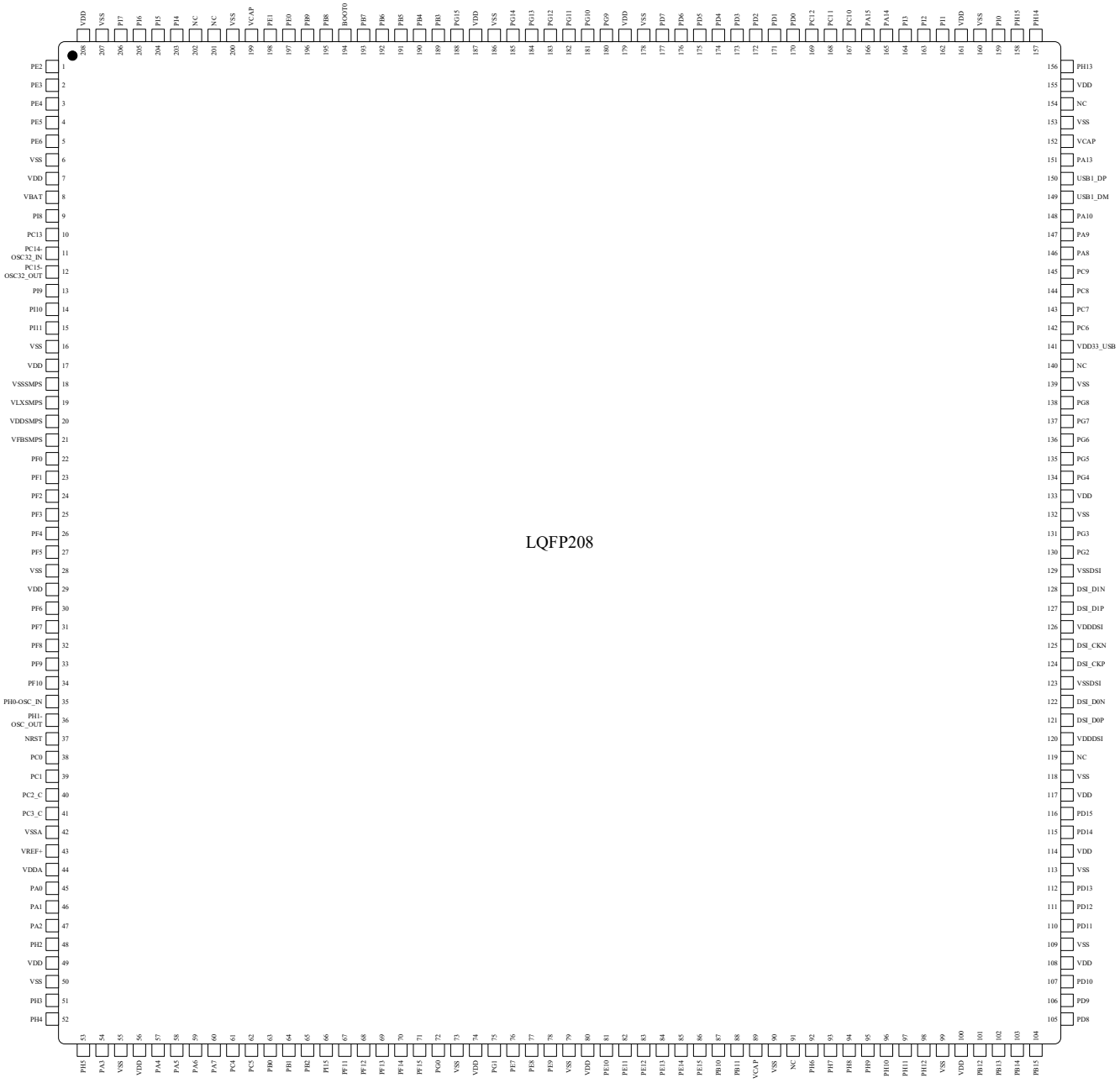
LQFP176

3.1.2 UFBGA176+25 Pin Distribution

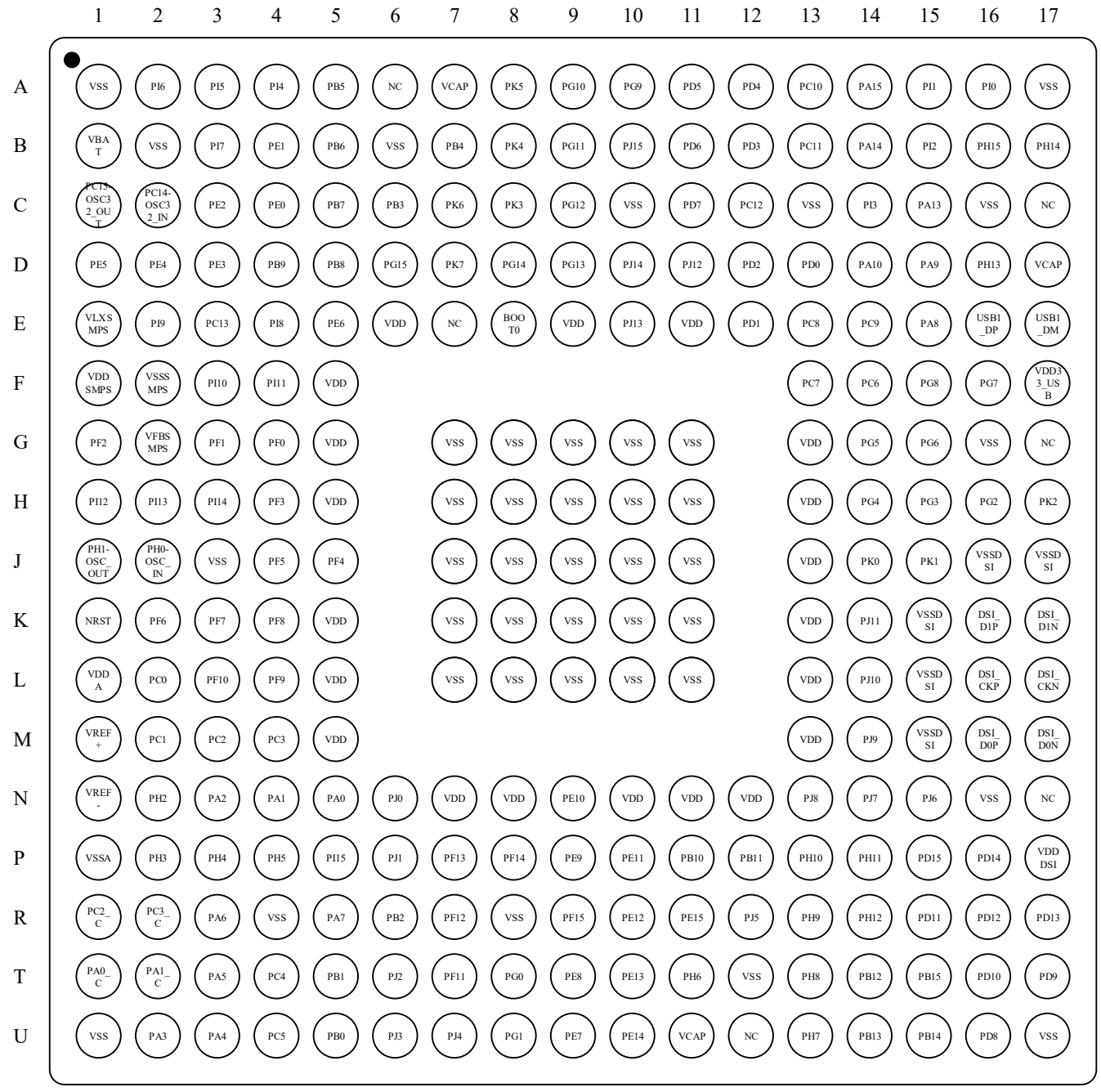


	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
A	VSS	PB8	NC	VCAP	PB6	PB3	PG11	PG9	PD3	PD1	PA15	PA14	NC	VCAP	VSS
B	PE4	PE3	PB9	PE0	PB7	PB4	PG13	PD7	PD5	PD2	PC12	PH14	PA13	PA8	USB1_DP
C	PC13	VSS	PE2	PE1	BOOT0	PB5	PG14	PG10	PD4	PD0	PC11	PC10	PH13	PA10	USB1_DM
D	PC13-OSC32_OUT	PC14-OSC32_IN	PE5	NC	VDD	VSS	PG15	PG12	PD6	VSS	VDD	PH15	PA9	PC8	PC7
E	VSS	VBAT	PE6	VDD								VDD	PC9	PC6	NC
F	VLXSMPS	VSSSMPS	PF1	PF0		VSS	VSS	VSS	VSS	VSS		VSS	VDD33_USB	PG6	PG5
G	VDDSMPS	VFBSMPS	PF2	VDD		VSS	VSS	VSS	VSS	VSS		PG8	PG7	PG4	PG2
H	PF6	PF4	PF5	PF3		VSS	VSS	VSS	VSS	VSS		VDD	PG3	PD14	PD13
J	PH0-OSC_IN	PF8	PF7	PF9		VSS	VSS	VSS	VSS	VSS		PD15	PD11	VSS	PD12
K	PH1-OSC_OUT	VSS	PF10	VDD		VSS	VSS	VSS	VSS	VSS		VSS	PD9	PB15	PB14
L	NRST	PC0	PC1	VREF-								VDD	PD10	PD8	PB13
M	PC2	PC3	VREF+	VDDA	VDD	VSS	PC5	PB1	VDD	VSS	PH7	PE14	PH11	PH9	PB12
N	PC2_C	PC3_C	VSSA	PH2	PA3	PA7	PF11	PE8	PG1	PF15	PF13	PB10	PH8	PH10	PH12
P	PA0	PA1	PA1_C	PH4	PA4	PA5	PB2	PG0	PE7	PB11	PF12	PE12	PE13	PE15	PH6
R	VSS	PA2	PA0_C	PH3	PH5	PC4	PA6	PB0	PE10	PF14	PE9	PE11	VCAP	NC	VSS

3.1.3 LQFP208 Pin Distribution



3.1.4 TFBGA240+25 Pin Distribution



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
A	VSS	PI6	PI5	PI4	PB5	NC	VCAP	PK5	PG10	PG9	PD5	PD4	PC10	PA15	PI1	PI0	VSS
B	VBAT	VSS	PI7	PE1	PB6	VSS	PB4	PK4	PG11	PJ15	PD6	PD3	PC11	PA14	PI2	PH15	PH14
C	PC13-OSC32_OUT	PC14-OSC32_IN	PE2	PE0	PB7	PB3	PK6	PK3	PG12	VSS	PD7	PC12	VSS	PI3	PA13	VSS	NC
D	PE5	PE4	PE3	PB9	PB8	PG15	PK7	PG14	PG13	PJ14	PJ12	PD2	PD0	PA10	PA9	PH13	VCAP
E	VLXSMPS	PI9	PC13	PI8	PE6	VDD	NC	BOOT0	VDD	PJ13	VDD	PD1	PC8	PC9	PA8	USB1_DP	USB1_DM
F	VDDSMPS	VSSSMPS	PI10	PI11	VDD								PC7	PC6	PG8	PG7	VDD33_USB
G	PF2	VFBSMPS	PF1	PF0	VDD		VSS	VSS	VSS	VSS	VSS		VDD	PG5	PG6	VSS	NC
H	PI12	PI13	PI14	PF3	VDD		VSS	VSS	VSS	VSS	VSS		VDD	PG4	PG3	PG2	PK2
J	PH1-OSC_OUT	PH0-OSC_IN	VSS	PF5	PF4		VSS	VSS	VSS	VSS	VSS		VDD	PK0	PK1	VSSDSI	VSSDSI
K	NRST	PF6	PF7	PF8	VDD		VSS	VSS	VSS	VSS	VSS		VDD	PJ11	VSSDSI	DSI_D1P	DSI_D1N
L	VDDA	PC0	PF10	PF9	VDD		VSS	VSS	VSS	VSS	VSS		VDD	PJ10	VSSDSI	DSI_CKP	DSI_CKN
M	VREF+	PC1	PC2	PC3	VDD								VDD	PJ9	VSSDSI	DSI_D0P	DSI_D0N
N	VREF-	PH2	PA2	PA1	PA0	PJ0	VDD	VDD	PE10	VDD	VDD	VDD	PJ8	PJ7	PJ6	VSS	NC
P	VSSA	PH3	PH4	PH5	PI15	PJ1	PF13	PF14	PE9	PE11	PB10	PB11	PH10	PH11	PD15	PD14	VDDDSI
R	PC2_C	PC3_C	PA6	VSS	PA7	PB2	PF12	VSS	PF15	PE12	PE15	PJ5	PH9	PH12	PD11	PD12	PD13
T	PA0_C	PA1_C	PA5	PC4	PB1	PJ2	PF11	PG0	PE8	PE13	PH6	VSS	PH8	PB12	PB15	PD10	PD9
U	VSS	PA3	PA4	PC5	PB0	PJ3	PJ4	PG1	PE7	PE14	VCAP	NC	PH7	PB13	PB14	PD8	VSS

3.2 Pin Multiplexing Definition

Table 0-1 Pin Definition

Package				Pin Name	Typ	I/O structure	Fail-safe(3) support	Optional Multiplexing Function	
TFBGA240+ 25	LQFP208	UFBG176+25	LQFP176					Default	Redefinition
C3	1	C3	1	PE2	IO	TT	Yes	TRACECLK SPI6_SCK ETH1_MII_TXD3/ETH1_GMII_TXD3 GTIMB1_ETR DVP2_D0 FEMC_A23 USART5_RX FDCAN4_TX	-
D3	2	B2	2	PE3	IO	TT	Yes	TRACED0 ETH1_MII_TXD2/ETH1_GMII_TXD2 SHRTIM2_EEV GTIMB1_BRK DVP2_D1 FEMC_A19 USART5_TX FDCAN4_RX	-
D2	3	B1	3	PE4	IO	FT	Yes	TRACED1 SPI6_NSS ETH2_PHY_INTNSHRTIM1_FLT GTIMB1_CH1N DVP1_D4 LCD_B0 FEMC_A20 USART6_RX DSMU_DATIN3	-
D1	4	D3	4	PE5	IO	TT	Yes	TRACED2 SPI6_MISO xSPI2_NCS1 GTIMB1_CH1P DVP1_D6 LCD_G0 FEMC_A21 USART6_TX DSMU_CKIN3	-
E5	5	E3	5	PE6	IO	FT	Yes	TRACED3 SPI6_MOSI SHRTIM1_EEV ATIM1_BKIN2 GTIMB1_CH2 DVP1_D7 LCD_G1 FEMC_A22	-
A1	6	A1	6	VSS	S	-	-	-	-
B2	-	C2	-	VSS	S	-	-	-	-
-	7	D5	7	VDD	S	-	-	-	-
B1	8	E2	8	VBAT	S	-	-	VBAT	-

E4	9	-	-	PI8	IO	FT	Yes	RTC_OUT2 RTC_TAMP2 PWR_WKUP4 SPI7_SCK ETH2_MII_TX_CLK LPTIM3_IN1 SDMMC1_SEL SDMMC2_SEL FDCAN1_TX	-
E3	10	C1	9	PC13	IO	FT	Yes	RTC_OUT1 RTC_TAMP1 RTC_TS PWR_WKUP3	-
C2	11	D2	10	PC14-OSC32_IN	IO	FT	Yes	PC14-OSC32_IN	-
C1	12	D1	11	PC15-OSC32_OUT	IO	FT	Yes	PC15-OSC32_OUT	-
E2	13	-	-	PI9	IO	TT	Yes	xSPI2_IO0 SHRTIM2_FLT GTIMA7_CH3 LPTIM3_IN2 LCD_VSYNC FEMC_D30 SDRAM_D30 UART9_RX FDCAN1_RX I2C9_SMBA SDRAM_D6	-
F3	14	-	-	PI10	IO	TT	Yes	xSPI2_IO1 ETH1_MII_RX_ER/ETH1_ GMII_RX_ER GTIMA7_CH4 LPTIM3_ETR LCD_HSYNC FEMC_D31 SDRAM_D31 FDCAN4_TX I2C9_SDA SDRAM_D7	-
F4	15	-	-	PI11	IO	TT	Yes	PWR_WKUP5 xSPI2_IO2 SHRTIM2_EEV GTIMA7_ETR LCD_G6 SDMMC1_LEDCTRL SDMMC2_LEDCTRL FDCAN4_RX I2C9_SCL FEMC_D0/FEMC_DA0	-
A17	16	A15	12	VSS	S	-	-	-	-
-	-	D10	-	VSS	S	-	-	-	-
E6	17	D11	13	VDD	S	-	-	-	-
F2	18	F2	14	VSSSMPS	S	-	-	-	-
E1	19	F1	15	VLXSMPS	S	-	-	-	-
F1	20	G1	16	VDDSMPS	S	-	-	-	-
G2	21	G2	17	VFBSMPS	S	-	-	-	-

G4	22	F4	18	PF0	IO	TT	Yes	xSPI2_IO0 ETH1_GMII_TXD4 SHRTIM2_CHA1 GTIMA1_CH1 GTIMA5_CH1 DVP2_D0 FEMC_A0 SDRAM_A0 USART1_TX FDCAN4_TX I2C2_SDA I2C5_SDA	COMP3_OUT
G3	23	F3	19	PF1	IO	TT	Yes	xSPI2_IO1 ETH1_GMII_TXD5 SHRTIM2_CHA2 GTIMA1_CH2 GTIMA5_CH2 DVP2_D1 FEMC_A1 SDRAM_A1 USART1_RX FDCAN4_RX I2C2_SCL I2C5_SCL SDRAM_D5	COMP3_INM
G1	24	G3	20	PF2	IO	TT	Yes	SPI6_NSS xSPI2_IO2 ETH1_GMII_TXD6 SHRTIM2_CHB1 GTIMA1_CH3 GTIMA5_CH3 GTIMB2_ETR DVP2_D2 FEMC_A2 SDRAM_A2 USART1_CK I2C2_SMBA I2C5_SMBA	COMP3_INP
H1	-	-	-	PI12	IO	TT	Yes	SPI7_NSS xSPI2_IO3 GTIMA7_CH3 DVP2_D2 LCD_HSYNC FDCAN6_TX I2C7_SDA FEMC_A4	-
H2	-	-	-	PI13	IO	TT	Yes	SPI7_MISO xSPI2_CLK/xSPI2_CLKIN SHRTIM2_FLT GTIMA7_CH4 DVP2_D3 LCD_VSYNC FDCAN6_RX I2C7_SCL FEMC_A7	-
H3	-	-	-	PI14	IO	TT	Yes	SPI7_MOSI xSPI2_NCLK SHRTIM1_EEV ATIM3_BKIN2 GTIMA7_ETR DVP2_D4 LCD_CLK	-

								I2C7_SMBA FEMC_A9	
H4	25	H4	21	PF3	IO	TT	Yes	SPI6_SCK xSPI2_IO3 ETH1_GMII_TXD7 SHRTIM2_CHB2 GTIMA1_CH4 GTIMA5_CH4 GTIMB2_CH4 DVP2_D3 FEMC_A3 SDRAM_A3 USART1_CTS/USART1_NSS I2C6_SDA	ADC3_INP5 COMP1_INM
J5	26	H2	22	PF4	IO	TT	Yes	SPI6_MISO xSPI2_CLK/xSPI2_CLKIN ETH2_MII_RX_CLK/ETH2_RMII_REF_CLK SHRTIM2_CHC1 GTIMA1_ETR GTIMB2_CH3 DVP2_D4 FEMC_A4 SDRAM_A4 USART1_DE/USART1_RTS FDCAN5_TX I2C6_SCL SDRAM_D4	ADC3_INN5 ADC3_INP9
J4	27	H3	23	PF5	IO	TT	Yes	SPI6_MOSI xSPI2_NCLK ETH1_GMII_GTX_CLK SHRTIM2_CHC2 ATIM3_BKIN1 GTIMB2_CH2 DVP2_D5 FEMC_A5 SDRAM_A5 FDCAN5_RX I2C6_SMBA	ADC3_INP4 COMP1_INP
C10	28	E1	24	VSS	S	-	-	-	-
E9	29	E4	25	VDD	S	-	-	-	-
K2	30	H1	26	PF6	IO	TT	Yes	SPI5_NSS xSPI2_IO3 ETH2_MDIO ATIM3_ETR ATIM4_ETR GTIMA5_CH1 GTIMB2_CH1P DVP1_PIXCLK DVP2_D5 UART11_RX FDCAN3_RX	ADC3_INN4 ADC3_INP8 COMP2_INM
K3	31	J3	27	PF7	IO	TT	Yes	SPI5_SCK xSPI2_IO2 ETH2_MDC ATIM3_CH4 ATIM4_CH3 GTIMA5_CH2 GTIMB3_CH1P DVP2_PIXCLK	ADC3_INP3 COMP2_INP

								UART11_TX FDCAN3_TX	
K4	32	J2	28	PF8	IO	TT	Yes	SPI5_MISO xSPI2_IO0 ETH2_MII_COL ATIM3_CH1 ATIM4_CH4 GTIMA5_CH3 GTIMB2_CH1N DVP2_HSYNC SDMMC2_LEDCTRL UART11_DE/UART11_RTS	ADC3_INN3 ADC3_INP7 COMP4_INM
L4	33	J4	29	PF9	IO	TT	Yes	SPI5_MOSI xSPI2_IO1 ETH2_MII_CRS SHRTIM2_FLT ATIM3_CH2 ATIM4_CH1 GTIMA5_CH4 GTIMB3_CH1N DVP2_VSYNC SDMMC1_LEDCTRL UART11_CTS	ADC3_INP2
L3	34	K3	30	PF10	IO	TT	Yes	xSPI2_CLK/xSPI2_CLKIN ETH2_PPS_OUT SHRTIM2_EEV ATIM3_CH3 ATIM4_CH2 GTIMB2_BRK DVP1_D11 LCD_DE FEMC_A3	ADC3_INN2 ADC3_INP6 COMP4_INP
J2	35	J1	31	PH0-OSC_IN	IO	FT	Yes	PH0-OSC_IN	-
J1	36	K1	32	PH1-OSC_OUT	IO	FT	Yes	PH1-OSC_OUT	-
K1	37	L1	33	NRST	I-O	NRST	-	NRST	-
L2	38	L2	34	PC0	IO	TT	Yes	ETH2_MII_RX_DV/ETH2_RMII_CRS_DV LCD_G2 LCD_R5 FEMC_A25 FEMC_D12/FEMC_DA12 SDRAM_NWE SDRAM_D12 DSMU_CKIN0 DSMU_DATIN4	ADC1_INP10 ADC2_INP10 ADC3_INP10
M2	39	L3	35	PC1	IO	TT	Yes	TRACED0 RTC_TAMP3 PWR_WKUP6 SPI2_MOSI I2S2_SDO ETH1_MDC LCD_G5 SDMMC2_CK FEMC_D0/FEMC_DA0 DSMU_CKIN4 DSMU_DATIN0	ADC1_INN10 ADC1_INP11 ADC2_INN10 ADC2_INP11 ADC3_INN10 ADC3_INP11
M3	-	M1	-	PC2	IO	TT	Yes	SPI2_MISO I2S2_SDI	ADC1_INN11 ADC1_INP12

								ETH1_MII_TXD2/ETH1_GMII_TXD2 DVP2_D6 SDRAM_NCE0 DSMU_CKIN1 DSMU_CKOUT	ADC2_INN11 ADC2_INP12 ADC3_INN11 ADC3_INP12
R1	40	N1	36	PC2_C	IO	TT	Yes	-	ADC2_INN1 ADC2_INP0 ADC3_INN1 ADC3_INP0
M4	-	M2	-	PC3	IO	TT	Yes	SPI2_MOSI I2S2_SDO ETH1_MII_TX_CLK/ETH1_GMII_TX_CLK DVP2_D7 SDRAM_CKE0 DSMU_DATIN1	ADC1_INN12 ADC1_INP13 ADC2_INN12 ADC2_INP13
R2	41	N2	37	PC3_C	IO	TT	Yes	-	ADC2_INP1 ADC3_INP1
E11	-	E12	-	VDD	S	-	-	-	-
C13	-	F6	-	VSS	S	-	-	-	-
P1	42	N3	38	VSSA	S	-	-	-	-
N1	-	L4	-	VREF-	S	-	-	-	-
M1	43	M3	39	VREF+	S	-	-	-	-
L1	44	M4	40	VDDA	S	-	-	-	-
N5	45	P1	41	PA0	IO	TT	Yes	PWR_WKUP1 SPI4_NSS I2S4_WS ETH1_MII_CRS/ETH1_GMII_CRS ATIM2_ETR GTIMA1_CH1 GTIMA1_ETR GTIMA4_CH1 GTIMB1_BRK SDMMC2_CMD FEMC_A19 USART2_CTS/USART2_NSS UART9_TX	ADC1_INP16
T1	-	R3	-	PA0_C	IO	TT	Yes	-	ADC1_INN1 ADC1_INP0 ADC2_INN1 ADC2_INP0
N4	46	P2	42	PA1	IO	TT	Yes	ETH1_MII_RX_CLK/ETH1_RMII_REF_CLK/ETH1_GMII_RX_CLK GTIMA1_CH2 GTIMA4_CH2 GTIMB1_CH1N LPTIM3_OUT LCD_R2 USART2_DE/USART2_RTS UART9_RX	ADC1_INN16 ADC1_INP17
T2	-	P3	-	PA1_C	IO	TT	Yes	-	ADC1_INP1 ADC2_INP1
N3	47	R2	43	PA2	IO	TT	Yes	PWR_WKUP2 ETH1_MDIO SHRTIM2_EEV GTIMA1_CH3	ADC1_INP14 ADC2_INP14

								GTIMA4_CH3 GTIMB1_CH1P LPTIM4_OUT LCD_R1 USART2_TX	
N2	48	N4	-	PH2	IO	TT	Yes	xSPI2_IO4 ETH1_MII_CRS/ETH1_G MII_CRS SHRTIM2_CHD1 GTIMB3_CH2 LPTIM1_IN2 LCD_R0 SDRAM_CKE0 UART15_RX	ADC3_INP13
F5	49	G4	44	VDD	S	-	-	-	-
C16	50	F7	45	VSS	S	-	-	-	-
P2	51	R4	-	PH3	IO	TT	Yes	xSPI2_IO5 ETH1_MII_COL/ETH1_G MII_COL SHRTIM2_CHD2 GTIMB3_CH3 LCD_R1 SDRAM_NCE0 USART7_CK UART15_TX	ADC3_INN13 ADC3_INP14
P3	52	P4	-	PH4	IO	FT	Yes	ETH2_MII_TXD0/ETH2_R MII_TXD0 SHRTIM2_CHE1 GTIMB3_CH4 DVP2_HSYNC LCD_G4 LCD_G5 USART7_RX UART15_DE/UART15_RT S FDCAN5_TX I2C2_SCL	ADC3_INN14 ADC3_INP15
P4	53	R5	-	PH5	IO	TT	Yes	SPI5_NSS ETH2_MII_TXD1/ETH2_R MII_TXD1 SHRTIM2_CHE2 GTIMB3_ETR DVP2_PIXCLK SDRAM_NWE USART7_TX UART15_CTS FDCAN5_RX I2C2_SDA	ADC3_INN15 ADC3_INP16
U2	54	N5	46	PA3	IO	TT	Yes	I2S4_MCK ETH1_MII_COL/ETH1_G MII_COL GTIMA1_CH4 GTIMA4_CH4 GTIMB1_CH2 LPTIM5_OUT LCD_B2 LCD_B5 USART2_RX FEMC_A10	ADC1_INP15 ADC2_INP15
-	55	F8	47	VSS	S	-	-	-	-
G5	56	H12	48	VDD	S	-	-	-	-

U3	57	P5	49	PA4	IO	TT	No	SPI1_NSS SPI3_NSS SPI4_NSS I2S1_WS I2S3_WS I2S4_WS GTIMA4_ETR DVP1_HSYNC LCD_VSYNC FEMC_D8/FEMC_DA8 SDRAM_D8 USART2_CK USB2_SOF	ADC1_INP18 ADC2_INP18 DAC1_OUT
T3	58	P6	50	PA5	IO	TT	Yes	SPI1_SCK SPI4_SCK I2S1_CK I2S4_CK ATIM2_CH1N GTIMA1_CH1 GTIMA1_ETR LCD_R4 FEMC_D9/FEMC_DA9 SDRAM_D9 SDRAM_DQM0	ADC1_INN18 ADC1_INP19 ADC2_INN18 ADC2_INP19 DAC2_OUT
R3	59	R7	51	PA6	IO	TT	Yes	SPI1_MISO SPI4_MISO I2S1_SDI I2S4_SDI xSPI2_IO3 ATIM1_BKIN1 ATIM2_BKIN1 ATIM3_CH1 GTIMA2_CH1 DVP1_PIXCLK LCD_G2	ADC1_INP3 ADC2_INP3
R5	60	N6	52	PA7	IO	TT	Yes	SPI1_MOSI SPI4_MOSI I2S1_SDO I2S4_SDO xSPI2_IO2 ETH1_MII_RX_DV/ETH1_ RMII_CRS_DV/ETH1_GM II_RX_DV ATIM1_CH1N ATIM2_CH1N ATIM4_CH1 GTIMA2_CH2 LCD_VSYNC SDRAM_NWE SDRAM_NWE	ADC1_INN3 ADC1_INP7 ADC2_INN3 ADC2_INP7
T4	61	R6	53	PC4	IO	TT	Yes	I2S1_MCK ETH1_MII_RXD0/ETH1_R MII_RXD0/ETH1_GMII_R XD0 SHRTIM2_EEV LCD_R7 SDMMC2_CKIN FEMC_A22 SDRAM_NCE0 DSMU_CKIN2	ADC1_INP4 ADC2_INP4 COMP1_INM
U4	62	M7	54	PC5	IO	TT	Yes	ETH1_MII_RXD1/ETH1_R MII_RXD1/ETH1_GMII_R	ADC1_INN4 ADC1_INP8

								XD1 SHRTIM2_FLT LCD_DE SDMMC2_SEL SDRAM_CKE0 DSMU_DATIN2 FEMC_A1 SDRAM_NCAS	ADC2_INN4 ADC2_INP8 COMP1_OUT
G13	-	K4	-	VDD	S	-	-	-	-
R4	-	F9	-	VSS	S	-	-	-	-
U5	63	R8	55	PB0	IO	TT	Yes	xSPI2_IO1 ETH1_MII_RXD2/ETH1_GMII_RXD2 ATIM1_CH2N ATIM2_CH2N GTIMA2_CH3 LCD_G1 LCD_R3 UART9_CTS DSMU_CKOUT	ADC1_INN5 ADC1_INP9 ADC2_INN5 ADC2_INP9 COMP1_INP
T5	64	M8	56	PB1	IO	TT	Yes	SPI3_MISO xSPI2_IO0 ETH1_MII_RXD3/ETH1_GMII_RXD3 ATIM1_CH3N ATIM2_CH3N GTIMA2_CH4 DVP1_MCLK LCD_G0 LCD_R6 DSMU_DATIN1	ADC1_INP5 ADC2_INP5 COMP1_INM
R6	65	P7	57	PB2	IO	TT	Yes	RTC_OUT2 SPI3_MOSI I2S3_SDO xSPI2_CLK/xSPI2_CLKIN ETH1_MII_TX_ER/ETH1_GMII_TX_ER ATIM1_CH4N ATIM2_CH4N GTIMA5_ETR DVP1_HSYNC DVP2_D12 DSMU_CKIN1	COMP1_INP
P5	66	-	-	PI15	IO	FT	Yes	ETH2_PPS_OUT SHRTIM1_FLT ATIM3_BKIN2 GTIMB3_ETR DVP2_D13 LCD_G2 LCD_R0	ADC2_INP17 ADC3_INP17
N6	-	-	-	PJ0	IO	FT	Yes	ETH2_MII_TXD2 SHRTIM2_FLT ATIM4_ETR GTIMB3_CH1N LCD_R1 LCD_R7 UART15_RX FDCAN8_TX I2C9_SDA	ADC2_INP16
P6	-	-	-	PJ1	IO	TT	Yes	SPI7_SCK xSPI2_IO4 ETH2_MII_TXD3	-

								ATIM4_CH1 GTIMB3_CH1P DVP2_VSYNC LCD_R2 UART15_TX FDCAN8_RX I2C9_SCL	
T6	-	-	-	PJ2	IO	TT	Yes	SPI7_NSS xSPI2_IO5 SHRTIM2_EEV ATIM4_CH1N GTIMB3_CH2 DVP1_D15 LCD_R3 UART15_DE/UART15_RT S I2C9_SMBA	-
U6	-	-	-	PJ3	IO	FT	Yes	SPI7_MISO ETH2_MII_RX_DV/ETH2_ RMII_CRS_DV ATIM4_CH2 GTIMB3_CH3 DVP1_D14 LCD_R4 UART13_RTS UART15_CTS FDCAN7_TX I2C9_SDA	ADC3_INP18
U7	-	-	-	PJ4	IO	FT	Yes	SPI7_MOSI ETH2_MII_RX_CLK/ETH 2_RMII_REF_CLK ATIM4_CH2N GTIMB3_CH4 DVP1_D13 LCD_R5 UART13_CTS FDCAN7_RX I2C9_SCL	ADC3_INP19
T7	67	N7	58	PF11	IO	TT	Yes	SPI5_MOSI ETH2_MII_TX_EN/ETH2_ RMII_TX_EN GTIMA6_CH1 DVP1_D12 SDRAM_NRAS I2C6_SDA SDRAM_NRAS	ADC1_INP2
R7	68	P11	59	PF12	IO	TT	Yes	xSPI2_DQS ETH2_MII_TXD0/ETH2_R MII_TXD0 GTIMA6_CH2 DVP2_D6 FEMC_A6 SDRAM_A6 FDCAN6_TX I2C6_SCL	ADC1_INN2 ADC1_INP6
J3	-	F10	-	VSS	S	-	-	-	-
H5	-	L12	-	VDD	S	-	-	-	-
P7	69	N11	60	PF13	IO	TT	Yes	ETH2_MII_TXD1/ETH2_R MII_TXD1 SHRTIM2_FLT GTIMA6_CH3 DVP2_D7	ADC2_INP2 COMP3_OUT

								FEMC_A7 SDRAM_A7 USART7_CK FDCAN6_RX I2C4_SMBA I2C6_SMBA DSMU_DATIN6 SDRAM_NCE0	
P8	70	R10	61	PF14	IO	TT	Yes	ETH2_MII_TXD2 SHRTIM2_CHF1 GTIMA6_CH4 DVP2_D8 FEMC_A8 SDRAM_A8 USART7_RX FDCAN3_RX I2C4_SCL DSMU_CKIN6	ADC2_INN2 ADC2_INP6 COMP3_INM
R9	71	N10	62	PF15	IO	TT	Yes	ETH2_MII_TXD3 SHRTIM2_CHF2 LPTIM4_ETR DVP2_D9 FEMC_A9 SDRAM_A9 USART7_TX FDCAN3_TX I2C4_SDA SDRAM_BA0	COMP3_INP
T8	72	P8	63	PG0	IO	TT	Yes	xSPI2_IO4 xSPI2_NCS2 ETH2_MII_TX_CLK SHRTIM1_EEV ATIM4_BKIN1 LPTIM4_IN1 DVP2_D10 FEMC_A10 SDRAM_A10 UART13_RX SDRAM_BA1	-
J16	73	F12	64	VSS	S	-	-	-	-
H13	74	M5	65	VDD	S	-	-	-	-
U8	75	N9	66	PG1	IO	TT	Yes	xSPI2_IO5 xSPI2_NCS3 ETH2_MII_TX_ER SHRTIM2_FLT GTIMB1_ETR LPTIM4_IN2 DVP2_D11 FEMC_A11 SDRAM_A11 UART13_TX SDRAM_A10	-
U9	76	P9	67	PE7	IO	TT	Yes	xSPI2_NCS2 ETH2_PHY_INTN ATIM1_ETR FEMC_D4/FEMC_DA4 SDRAM_D4 UART11_RX I2C7_SDA DSMU_DATIN2	COMP2_INM
T9	77	N8	68	PE8	IO	TT	Yes	ATIM1_CH1N SDMMC1_LEDCTRL	COMP2_OUT

								FEMC_D5/FEMC_DA5 SDRAM_D5 UART11_TX FDCAN5_TX I2C7_SCL DSMU_CKIN2 SDRAM_A0	
P9	78	R11	69	PE9	IO	TT	Yes	ATIM1_CH1 SDMMC2_LEDCTRL FEMC_D6/FEMC_DA6 SDRAM_D6 UART11_DE/UART11_RTS FDCAN5_RX I2C7_SMBA DSMU_CKOUT SDRAM_A1	COMP2_INP
J17	79	G6	70	VSS	S	-	-	-	-
J13	80	M9	71	VDD	S	-	-	-	-
N9	81	R9	72	PE10	IO	TT	Yes	ATIM1_CH2N FEMC_D7/FEMC_DA7 SDRAM_D7 UART11_CTS DSMU_DATIN4 SDRAM_A2	COMP2_INM
P10	82	R12	73	PE11	IO	TT	Yes	SPI6_NSS ATIM1_CH2 LCD_G3 FEMC_D8/FEMC_DA8 SDRAM_D8 DSMU_CKIN4 SDRAM_A3	COMP2_INP
R10	83	P12	74	PE12	IO	TT	Yes	SPI6_SCK ETH1_GMII_RXD4 ATIM1_CH3N LCD_B4 FEMC_D9/FEMC_DA9 SDRAM_D9 UART13_RX DSMU_DATIN5	COMP1_OUT
T10	84	P13	75	PE13	IO	TT	Yes	SPI6_MISO ETH1_GMII_RXD5 ATIM1_CH3 LCD_DE FEMC_D10/FEMC_DA10 SDRAM_D10 UART13_TX FDCAN6_TX I2C6_SDA DSMU_CKIN5	COMP2_OUT
T12	-	G7	-	VSS	S	-	-	-	-
K13	-	-	-	VDD	S	-	-	-	-
U10	85	M12	76	PE14	IO	TT	Yes	SPI6_MOSI ETH1_GMII_RXD6 SHRTIM2_EEV ATIM1_CH4 LCD_CLK FEMC_D11/FEMC_DA11 SDRAM_D11 USART6_CK UART13_CTS	-

								FDCAN6_RX I2C6_SCL	
R11	86	P14	77	PE15	IO	TT	Yes	ETH1_GMII_RXD7 ATIM1_BKIN1 LCD_R7 FEMC_D12/FEMC_DA12 SDRAM_D12 USART5_CK UART13_DE/UART13_RT S I2C6_SMBA	-
P11	87	N12	78	PB10	IO	TT	Yes	SPI2_SCK I2S2_CK ETH1_MII_RX_ER/ETH1_ GMII_RX_ER SHRTIM1_SCOUT GTIMA1_CH3 LPTIM2_IN1 LCD_G4 USART3_TX I2C2_SCL DSMU_DATIN7 FEMC_D13/FEMC_DA13	-
P12	88	P10	79	PB11	IO	TT	Yes	ETH1_MII_TX_EN/ETH1_ RMII_TX_EN/ETH1_GMII _TX_EN SHRTIM1_SCIN GTIMA1_CH4 LPTIM2_ETR LCD_G5 USART3_RX I2C2_SDA DSMU_CKIN7 FEMC_D15/FEMC_DA15	-
U11	89	R13	80	VCAP	S	-	-	-	-
-	90	M10	81	VSS	S	-	-	-	-
U12	91	R14	82	NC	S	-	-	-	-
L13	-	-	-	VDD	S	-	-	-	-
R12	-	-	-	PJ5	IO	FT	Yes	ETH2_MII_TX_ER SHRTIM1_EEV ATIM4_BKIN2 LPTIM5_ETR DVP1_D9 LCD_R6	ADC2_INP16
T11	92	P15	-	PH6	IO	TT	Yes	SPI5_SCK ETH1_MII_RXD2/ETH1_G MII_RXD2 ATIM1_CH4N GTIMA7_CH1 LPTIM5_IN1 DVP1_D8 FEMC_BAA SDRAM_NCE1 UART14_RX FDCAN7_TX I2C2_SMBA SDRAM_A4	COMP4_INM
U13	93	M11	-	PH7	IO	TT	Yes	SPI5_MISO ETH1_MII_RXD3/ETH1_G MII_RXD3 SHRTIM2_EEV ATIM3_BKIN1	COMP4_INP

								LPTIM5_IN2 DVP1_D9 FEMC_CRE SDRAM_CKE1 UART14_TX FDCAN7_RX I2C3_SCL SDRAM_A5	
T13	94	N13	-	PH8	IO	TT	Yes	ETH1_GMII_RXD4 SHRTIM2_EEV ATIM3_CH1 GTIMA4_ETR DVP1_HSYNC LCD_R2 FEMC_D16 SDRAM_D16 UART10_DE/UART10_RTS UART14_DE/UART14_RTS FDCAN2_RX I2C3_SDA SDRAM_A6	COMP4_OUT
-	-	G9	-	VSS	S	-	-	-	-
R13	95	M14	-	PH9	IO	TT	Yes	ETH1_GMII_RXD5 ATIM3_CH1N GTIMA7_CH2 DVP1_D0 LCD_R3 FEMC_D17 SDRAM_D17 UART10_CTS UART14_CTS FDCAN2_TX I2C3_SMBA SDRAM_A7	COMP4_INM
P13	96	N14	-	PH10	IO	TT	Yes	ETH1_GMII_RXD6 SHRTIM2_EEV ATIM3_CH2 GTIMA4_CH1 DVP1_D1 LCD_R4 FEMC_D18 SDRAM_D18 I2C4_SMBA SDRAM_A8	COMP4_INP
P14	97	M13	-	PH11	IO	TT	Yes	ETH1_GMII_RXD7 SHRTIM2_EEV ATIM3_CH2N GTIMA4_CH2 DVP1_D2 LCD_R5 FEMC_D19 SDRAM_D19 UART10_RX I2C4_SCL SDRAM_A9	-
R14	98	N15	-	PH12	IO	TT	Yes	SPI7_NSS ETH2_MII_RX_DV/ETH2_RMII_CRS_DV SHRTIM2_EEV ATIM3_ETR	COMP4_OUT

								GTIMA4_CH3 DVP1_D3 LCD_R6 FEMC_D20 SDRAM_D20 UART10_TX I2C4_SDA SDRAM_A11	
N16	99	G10	83	VSS	S	-	-	-	-
M13	100	-	84	VDD	S	-	-	-	-
T14	101	M15	85	PB12	IO	TT	No	SPI2_NSS I2S2_WS ETH1_MII_TXD0/ETH1_RMII_TXD0/ETH1_GMII_TXD0 ATIM1_BKIN1 LPTIM2_IN2 DVP2_D14 USART3_CK UART10_RX FDCAN2_RX USB2_ID I2C2_SMBA DSMU_DATIN1	-
U14	102	L15	86	PB13	IO	TT	No	SPI2_SCK I2S2_CK ETH1_MII_TXD1/ETH1_RMII_TXD1/ETH1_GMII_TXD1 ATIM1_CH1N LPTIM2_OUT DVP1_D2 SDMMC1_D0 USART3_CTS/USART3_NSS UART10_TX FDCAN2_TX USB2_VBUS DSMU_CKIN1	-
U15	103	K15	87	PB14	IO	TT	No	SPI2_MISO I2S2_SDI ATIM1_CH2N ATIM2_CH2N GTIMA7_CH1 LCD_CLK SDMMC2_D0 FEMC_D10/FEMC_DA10 SDRAM_D10 USART1_TX USART3_DE/USART3_RTS UART9_DE/UART9_RTS USB2_DM DSMU_DATIN2	-
T15	104	K14	88	PB15	IO	TT	No	RTC_REFIN SPI2_MOSI I2S2_SDO ATIM1_CH3N ATIM2_CH3N GTIMA7_CH2 LCD_G7 SDMMC2_D1	-

								FEMC_D11/FEMC_DA11 SDRAM_D11 USART1_RX UART9_CTS USB2_DP DSMU_CKIN2	
U16	105	L14	89	PD8	IO	TT	Yes	SHRTIM1_EEV SHRTIM2_SCIN ATIM3_CH3 DVP2_HSYNC FEMC_D13/FEMC_DA13 SDRAM_D13 USART3_TX I2C7_SDA DSMU_CKIN3	-
T17	106	K13	90	PD9	IO	TT	Yes	SHRTIM1_EEV SHRTIM2_SCOUT ATIM3_CH3N DVP2_VSYNC FEMC_D14/FEMC_DA14 SDRAM_D14 USART3_RX I2C7_SCL DSMU_DATIN3	-
T16	107	L13	91	PD10	IO	TT	Yes	ETH1_CLK125 ETH2_PPS_OUT ATIM1_CH4N LPTIM2_OUT LCD_B3 FEMC_D15/FEMC_DA15 SDRAM_D15 USART3_CK I2C7_SMBA DSMU_CKOUT	-
N12	108	-	92	VDD	S	-	-	-	-
U17	109	H6	93	VSS	S	-	-	-	-
R15	110	J13	94	PD11	IO	TT	Yes	SHRTIM2_EEV GTIMA3_ETR LPTIM2_IN2 DVP2_D15 FEMC_A16/FEMC_CLE USART3_CTS/USART3_NSS I2C4_SMBA	-
R16	111	J15	95	PD12	IO	TT	Yes	GTIMA3_CH1 LPTIM1_IN1 LPTIM2_IN1 DVP1_D12 FEMC_A17/FEMC_ALE USART3_DE/USART3_RTS UART12_TX UART13_CTS FDCAN3_RX I2C4_SCL	-
R17	112	H15	96	PD13	IO	TT	Yes	GTIMA3_CH2 LPTIM1_OUT DVP1_D13 FEMC_A18 UART12_RX UART13_DE/UART13_RTS	-

								FDCAN3_TX I2C4_SDA I2C8_SMBA	
-	113	R1	-	VSS	S	-	-	-	-
N11	114	-	-	VDD	S	-	-	-	-
P16	115	H14	97	PD14	IO	TT	Yes	ETH1_PPS_OUT ATIM3_CH4 GTIMA3_CH3 SDMMC1_D4 FEMC_D0/FEMC_DA0 SDRAM_D0 UART12_CTS UART13_RX I2C8_SDA SDRAM_CKE0	-
P15	116	J12	98	PD15	IO	TT	Yes	ETH1_PHY_INTN ETH2_PHY_INTN SHRTIM2_FLT ATIM3_CH4N GTIMA3_CH4 SDMMC1_D5 FEMC_D1/FEMC_DA1 SDRAM_D1 UART12_DE/UART12_RTS UART13_TX I2C8_SCL	-
N15	117	-	-	PJ6	IO	FT	Yes	ATIM2_CH2 DVP2_D8 LCD_R7 FDCAN7_TX FEMC_D2/FEMC_DA2	ADC3_INP18
N14	118	-	-	PJ7	IO	FT	Yes	TRGIN ATIM2_CH2N DVP2_D9 LCD_G0 FDCAN7_RX FEMC_D3/FEMC_DA3	ADC3_INP19
N10	119	-	99	VDD	S	-	-	-	-
R8	120	D6	100	VSS	S	-	-	-	-
N13	121	-	101	PJ8	IO	FT	Yes	ETH2_MII_RXD2 ATIM1_CH3N ATIM2_CH1 DVP2_D10 LCD_G1 USART8_CTS/USART8_NSS UART12_TX UART14_DE/UART14_RTS FDCAN8_TX I2C8_SDA	-
M14	122	-	102	PJ9	IO	FT	Yes	ETH2_MII_RXD3 ATIM1_CH3 ATIM2_CH1N DVP2_D11 LCD_G2 USART8_DE/USART8_RTS UART12_RX UART14_CTS	-

								FDCAN8_RX I2C8_SCL	
L14	123	-	103	PJ10	IO	FT	Yes	SPI5_MOSI ATIM1_CH2N ATIM2_CH2 DVP2_D12 LCD_G3 UART12_CTS UART14_RX I2C8_SMBA FEMC_D5/FEMC_DA5	-
K14	124	-	104	PJ11	IO	FT	Yes	SPI5_MISO ATIM1_CH2 ATIM2_CH2N DVP2_D13 LCD_G4 UART12_DE/UART12_RTS UART14_TX FEMC_D6/FEMC_DA6	-
N8/P17	-	-	-	VDD	S	-	-	-	-
U1	-	R15	-	VSS	S	-	-	-	-
K15	-	-	-	VSS	S	-	-	-	-
L15	-	-	-	VSS	S	-	-	-	-
-	125	-	105	VDD	S	-	-	-	-
M15	126	-	106	VSS	S	-	-	-	-
J14	127	-	107	PK0	IO	FT	Yes	SPI5_SCK ETH2_MII_COL SHRTIM2_EEV ATIM1_CH1N ATIM2_CH3 DVP2_D7 LCD_G5 I2C3_SCL	-
J15	128	-	108	PK1	IO	FT	Yes	SPI5_NSS ETH2_MII_CRS SHRTIM2_FLT ATIM1_CH1 ATIM2_CH3N DVP2_D6 LCD_G6 I2C3_SDA	-
H17	129	-	109	PK2	IO	FT	Yes	SHRTIM1_FLT ATIM1_BKIN1 ATIM2_BKIN1 DVP2_D5 LCD_G7 I2C3_SMBA FEMC_A11	-
H16	130	G15	110	PG2	IO	TT	Yes	ETH2_MII_RXD0/ETH2_RMII_RXD0 SHRTIM2_SCIN ATIM2_BKIN1 GTIMA6_ETR DVP2_D12 FEMC_A12 SDRAM_A12 USART7_CTS/USART7_NSS	-

								FDCAN8_TX SDRAM_DQM1	
H15	131	H13	111	PG3	IO	FT	Yes	ETH2_MII_RXD1/ETH2_RMII_RXD1 SHRTIM2_SCOUT ATIM2_BKIN2 GTIMA5_ETR DVP2_D13 FEMC_A13 USART7_DE/USART7_RTS FDCAN8_RX	-
-	132	H10	112	VSS	S	-	-	-	-
N7	133	-	113	VDD	S	-	-	-	-
H14	134	G14	114	PG4	IO	TT	Yes	ETH2_MII_RXD2 SHRTIM1_CHF1 ATIM1_BKIN2 DVP2_D14 SDMMC2_CKIN SDMMC2_D4 FEMC_A14 SDRAM_BA0 USART6_CTS/USART6_NSS I2C1_SDA I2C8_SDA	-
G14	135	F15	115	PG5	IO	TT	Yes	ETH2_MII_RXD3 SHRTIM1_CHF2 ATIM1_ETR DVP2_D15 SDMMC2_CDIR SDMMC2_D5 FEMC_A15 SDRAM_BA1 USART6_DE/USART6_RTS I2C1_SCL I2C8_SCL	-
G15	136	F14	116	PG6	IO	TT	Yes	ETH2_MII_RX_ER SHRTIM1_CHE1 GTIMB3_BRK DVP1_D12 LCD_R7 FEMC_NE3 I2C1_SMBA I2C8_SMBA	-
F16	137	G13	117	PG7	IO	TT	Yes	xSPI2_DQS ETH1_PHY_INTN SHRTIM1_CHE2 DVP1_D13 LCD_CLK FEMC_INT/FEMC_BUSY USART4_CK FDCAN7_TX	-
F15	138	G12	118	PG8	IO	TT	Yes	SPI4_NSS I2S4_WS ETH1_PPS_OUT SHRTIM2_EEV ATIM2_ETR LCD_G7 SDRAM_CLK USART4_DE/USART4_RT	-

								S FDCAN7_RX SDRAM_CLK	
G16	139	J6	119	VSS	S	-	-	-	-
G17	140	E15	120	NC	S	-	-	-	-
F17	141	F13	121	VDD33_USB	S	-	-	-	-
M5	-	-	-	VDD	S	-	-	-	-
F14	142	E14	122	PC6	IO	FT	Yes	I2S2_MCK SHRTIM1_CHA1 ATIM2_CH1 GTIMA2_CH1 DVP1_D0 LCD_HSYNC SDMMC1_D0DIR SDMMC1_D6 SDMMC2_D6 FEMC_NWAIT USART4_TX DSMU_CKIN3	-
F13	143	D15	123	PC7	IO	FT	Yes	TRGIO I2S3_MCK SHRTIM1_CHA2 ATIM2_CH2 GTIMA2_CH2 DVP1_D1 LCD_G6 SDMMC1_D123DIR SDMMC1_D7 SDMMC2_D7 FEMC_NE1/FEMC_NCE2 USART4_RX DSMU_DATIN3	-
E13	144	D14	124	PC8	IO	FT	Yes	TRACED1 SHRTIM1_CHB1 ATIM2_CH3 GTIMA2_CH3 DVP1_D2 SDMMC1_D0 FEMC_NCE1/FEMC_NE2 FEMC_INT/FEMC_BUSY USART4_CK UART10_DE/UART10_RTS	-
E14	145	E13	125	PC9	IO	TT	Yes	MCO2 I2S1_CKIN I2S2_CKIN I2S3_CKIN I2S4_CKIN ATIM2_CH4 GTIMA2_CH4 DVP1_D3 LCD_B2 LCD_G3 SDMMC1_D1 UART10_CTS I2C3_SDA I2C5_SDA	-
-	-	J7	-	VSS	S	-	-	-	-
L5	-	-	126	VDD	S	-	-	-	-

E15	146	B14	127	PA8	IO	TT	No	MCO1 ETH2_MII_RX_CLK/ETH 2_RMII_REF_CLK SHRTIM1_CHB2 ATIM1_CH1 ATIM2_BKIN2 LCD_B3 LCD_R6 USART1_CK UART11_RX USB1_SOF I2C3_SCL I2C5_SCL	-
D15	147	D13	128	PA9	IO	TT	No	SPI2_SCK I2S2_CK ETH1_MII_TX_ER/ETH1_ GMII_TX_ER SHRTIM1_CHC1 ATIM1_CH2 DVP1_D0 LCD_R5 USART1_TX LPUART1_TX USB1_VBUS I2C3_SMBA I2C5_SMBA	-
D14	148	C14	129	PA10	IO	TT	No	SHRTIM1_CHC2 ATIM1_CH3 DVP1_D1 LCD_B1 LCD_B4 USART1_RX LPUART1_RX USB1_ID	-
E17	149	C15	130	USB1_D M	USB	TT	No	-	-
E16	150	B15	131	USB1_DP	USB	TT	No	-	-
C15	151	B13	132	PA13	IO	FT	Yes	JTMS-SWDIO	-
D17	152	A14	133	VCAP	S	-	-	-	-
-	153	M6	134	VSS	S	-	-	-	-
C17	154	A13	135	NC	S	-	-	-	-
K5	155	-	136	VDD	S	-	-	-	-
D16	156	C13	-	PH13	IO	TT	Yes	SPI7_NSS ETH2_MII_TX_EN/ETH2_ RMII_TX_EN ATIM2_CH1N LCD_G2 FEMC_D21 SDRAM_D21 UART9_TX FDCAN1_TX I2C9_SMBA	-
B17	157	B12	-	PH14	IO	TT	Yes	SPI7_MISO ETH2_MII_TXD0/ETH2_R MII_TXD0 ATIM2_CH2N DVP1_D4 LCD_G3 FEMC_D22 SDRAM_D22 USART6_RX	-

								UART9_RX FDCAN1_RX I2C9_SDA	
B16	158	D12	-	PH15	IO	TT	Yes	SPI7_MOSI ETH2_MII_TXD1/ETH2_R MII_TXD1 ATIM2_CH3N DVP1_D11 LCD_G4 FEMC_D23 SDRAM_D23 USART6_TX I2C9_SCL	-
A16	159	-	-	PI0	IO	TT	Yes	SPI2_NSS I2S2_WS SHRTIM2_FLT ATIM2_CH4N GTIMA4_CH4 DVP1_D13 LCD_G5 FEMC_D24 SDRAM_D24 I2C10_SDA	-
-	160	J9	-	VSS	S	-	-	-	-
-	161	-	-	VDD	S	-	-	-	-
A15	162	-	-	PI1	IO	TT	Yes	SPI2_SCK I2S2_CK ETH2_MII_RXD0/ETH2_R MII_RXD0 ATIM2_BKIN2 DVP1_D8 LCD_G6 FEMC_D25 SDRAM_D25 USART8_CK I2C8_SMBA I2C10_SCL SDRAM_D8	-
B15	163	-	-	PI2	IO	TT	Yes	SPI2_MISO I2S2_SDI ETH2_MII_RXD1/ETH2_R MII_RXD1 ATIM2_CH4 DVP1_D9 LCD_G7 FEMC_D26 SDRAM_D26 USART8_RX LPUART2_TX I2C8_SDA SDRAM_D9	-
C14	164	-	-	PI3	IO	TT	Yes	SPI2_MOSI I2S2_SDO ETH2_MII_RX_ER ATIM2_ETR DVP1_D10 FEMC_D27 SDRAM_D27 USART8_TX LPUART2_RX I2C8_SCL	-

								I2C10_SMBA SDRAM_D10	
-	-	J10	137	VSS	S	-	-	-	-
B14	165	A12	138	PA14	IO	FT	Yes	JTCK-SWCLK	-
A14	166	A11	139	PA15	IO	FT	Yes	JTDI SPI1_NSS SPI3_NSS SPI4_NSS I2S1_WS I2S3_WS I2S4_WS SHRTIM1_FLT GTIMA1_CH1 GTIMA1_ETR LCD_B6 LCD_R3 UART9_DE/UART9_RTS UART11_TX	-
A13	167	C12	140	PC10	IO	TT	Yes	SPI3_SCK I2S3_CK SHRTIM1_EEV DVP1_D8 LCD_R2 LCD_B1 SDMMC1_D2 USART3_TX UART9_TX I2C5_SDA DSMU_CKIN5	-
B13	168	C11	141	PC11	IO	TT	Yes	SPI3_MISO I2S3_SDI SHRTIM1_FLT DVP1_D4 LCD_B4 SDMMC1_D3 USART3_RX UART9_RX I2C5_SCL DSMU_DATIN5	-
C12	169	B11	142	PC12	IO	TT	Yes	TRACED3 SPI3_MOSI SPI4_SCK I2S3_SDO I2S4_CK SHRTIM1_EEV GTIMB1_CH1P DVP1_D9 LCD_R6 SDMMC1_CK FEMC_D6/FEMC_DA6 SDRAM_D6 USART3_CK UART10_TX I2C5_SMBA	-
-	-	J14	-	VSS	S	-	-	-	-
D13	170	C10	143	PD0	IO	TT	Yes	SHRTIM2_EEV GTIMB2_CH1N LCD_B1 SDMMC1_WP FEMC_D2/FEMC_DA2 SDRAM_D2 UART9_RX	-

								UART13_CTS FDCAN1_RX DSMU_CKIN6 SDRAM_D11	
E12	171	A10	144	PD1	IO	TT	Yes	SHRTIM2_FLT GTIMB2_CH1P SDMMC1_CD FEMC_D3/FEMC_DA3 SDRAM_D3 UART9_TX FDCAN1_TX I2C1_SMBA DSMU_DATIN6 SDRAM_D12	-
D12	172	B10	145	PD2	IO	TT	Yes	TRACED2 GTIMA2_ETR GTIMB1_BRK GTIMB2_CH2 DVP1_D11 LCD_B2 LCD_B7 SDMMC1_CMD FEMC_D7/FEMC_DA7 SDRAM_D7 UART10_RX LPUART2_CTS SDRAM_D13	-
B12	173	A9	146	PD3	IO	FT	Yes	SPI2_SCK I2S2_CK GTIMB2_CH3 DVP1_D5 LCD_G7 SDMMC1_RST FEMC_CLK USART2_CTS/USART2_NSS LPUART2_DE/LPUART2_RTS DSMU_CKOUT	-
A12	174	C9	147	PD4	IO	TT	Yes	SPI3_NSS SHRTIM1_FLT GTIMB2_CH4 DVP1_D14 SDMMC2_WP FEMC_NOE USART2_DE/USART2_RTS LPUART2_TX I2C1_SCL	-
A11	175	B9	148	PD5	IO	TT	Yes	SPI3_MISO SHRTIM1_EEV GTIMB2_ETR DVP1_D15 SDMMC2_CD FEMC_NWE USART2_TX LPUART2_RX I2C1_SDA	-
-	-	K2	-	VSS	S	-	-	-	-
B11	176	D9	149	PD6	IO	TT	Yes	SPI3_MOSI I2S3_SDO DVP1_D10	-

								LCD_B2 SDMMC2_CK FEMC_NWAIT USART2_RX DSMU_CKIN4 DSMU_DATIN1	
C11	177	B8	150	PD7	IO	TT	Yes	SPI1_MOSI SPI3_SCK I2S1_SDO ATIM4_BKIN1 SDMMC2_CMD FEMC_NE1/FEMC_NCE2 USART2_CK DSMU_CKIN1 DSMU_DATIN4	-
D11	-	-	-	PJ12	IO	FT	Yes	TRGOUT ATIM4_CH3 DVP2_D15 LCD_B0 LCD_G3 SDMMC1_SEL I2C10_SMBA FEMC_BAA	-
E10	-	-	-	PJ13	IO	FT	Yes	ATIM4_CH3N DVP2_D14 LCD_B1 LCD_B4 SDMMC2_SEL I2C10_SDA FEMC_NBL0	-
D10	-	-	-	PJ14	IO	FT	Yes	SHRTIM2_EEV ATIM4_CH4 DVP2_D13 LCD_B2 FEMC_CRE I2C10_SCL	-
B10	-	-	-	PJ15	IO	FT	Yes	ATIM4_CH4N DVP2_D12 LCD_B3 FEMC_BAA	-
-	178	K6	151	VSS	S	-	-	-	-
-	179	-	152	VDD	S	-	-	-	-
A10	180	A8	153	PG9	IO	TT	Yes	SPI1_MISO I2S1_SDI ETH2_MII_RXD0/ETH2_R MII_RXD0 SHRTIM1_FLT DVP1_VSYNC SDMMC2_D0 FEMC_NCE1/FEMC_NE2 USART4_RX FDCAN3_TX	-
A9	181	C8	154	PG10	IO	TT	Yes	SPI1_NSS I2S1_WS xSPI2_IO6 xSPI2_NCS4 ETH2_MII_RXD1/ETH2_R MII_RXD1 SHRTIM1_FLT DVP1_D2 LCD_B2 LCD_G3	-

								SDMMC2_D1 FEMC_NE3 FDCAN3_RX	
B9	182	A7	155	PG11	IO	TT	Yes	SPI1_SCK I2S1_CK xSPI2_IO7 xSPI2_NCSIN ETH1_MII_TX_EN/ETH1_RMII_TX_EN/ETH1_GMII_TX_EN SHRTIM1_EEV LPTIM1_IN2 DVP1_D3 LCD_B3 SDMMC2_D2 USART5_RX	-
C9	183	D8	156	PG12	IO	TT	Yes	SPI4_MISO I2S4_SDI xSPI2_NCS1 ETH1_MII_TXD1/ETH1_RMII_TXD1/ETH1_GMII_TXD1 SHRTIM1_EEV GTIMA5_CH1 LPTIM1_IN1 DVP2_MCLK LCD_B1 LCD_B4 SDMMC2_D3 FEMC_NE4 USART4_DE/USART4_RTS USART5_TX	-
D9	184	B7	157	PG13	IO	TT	Yes	TRACED0 SPI4_SCK I2S4_CK ETH1_MII_TXD0/ETH1_RMII_TXD0/ETH1_GMII_TXD0 SHRTIM1_EEV GTIMA5_CH2 LPTIM1_OUT LCD_R0 SDMMC2_D0DIR SDMMC2_D6 FEMC_A24 USART4_CTS/USART4_NSS USART5_CTS/USART5_NSS	-
D8	185	C7	158	PG14	IO	TT	Yes	TRACED1 SPI4_MOSI I2S4_SDO ETH1_MII_TXD1/ETH1_RMII_TXD1/ETH1_GMII_TXD1 GTIMA5_CH3 LPTIM1_ETR LCD_B0 SDMMC2_D123DIR SDMMC2_D7 FEMC_A25	-

								USART4_TX USART5_DE/USART5_RTS	
-	186	K7	159	VSS	S	-	-	-	-
-	187	-	160	VDD	S	-	-	-	-
C8	-	-	-	PK3	IO	TT	Yes	xSPI2_IO6 SHRTIM1_EEV ATIM4_BKIN2 DVP2_D0 LCD_B4 I2C10_SDA FEMC_D7/FEMC_DA7	-
B8	-	-	-	PK4	IO	TT	Yes	xSPI2_IO7 SHRTIM1_EEV GTIMA6_CH1 DVP2_D1 LCD_B5 I2C10_SCL FEMC_D9/FEMC_DA9	-
A8	-	-	-	PK5	IO	TT	Yes	xSPI2_NCS1 GTIMA6_CH2 DVP2_D2 LCD_B6 I2C10_SMBA FEMC_D11/FEMC_DA11	-
C7	-	-	-	PK6	IO	TT	Yes	xSPI2_DQS SHRTIM2_FLT GTIMA6_CH3 DVP2_D3 LCD_B7 I2C10_SDA FEMC_A12	-
D7	-	-	-	PK7	IO	TT	Yes	GTIMA6_CH4 DVP2_D4 LCD_DE I2C10_SCL FEMC_A15	-
-	-	K8	-	VSS	S	-	-	0	0
D6	188	D7	161	PG15	IO	TT	Yes	xSPI2_DQS ETH1_PHY_INTN SHRTIM2_EEV DVP1_D13 SDMMC2_RST SDRAM_NCAS USART4_CTS/USART4_NSS USART5_CK SDRAM_D14	-
C6	189	A6	162	PB3	IO	FT	Yes	TRACESWO JTDO SPI1_SCK SPI3_SCK SPI4_SCK I2S1_CK I2S3_CK I2S4_CK SHRTIM1_FLT GTIMA1_CH2 GTIMA6_ETR SDMMC2_D2 UART11_RX	-

B7	190	B6	163	PB4	IO	FT	Yes	JTRST SPI1_MISO SPI2_NSS SPI3_MISO SPI4_MISO I2S1_SDI I2S2_WS I2S3_SDI I2S4_SDI ETH1_PHY_INTN SHRTIM1_EEV GTIMA2_CH1 GTIMB2_BRK SDMMC2_D3 UART11_TX	-
A5	191	C6	164	PB5	IO	TT	Yes	SPI1_MOSI/I2S1_SDO SPI3_MOSI/I2S3_SDO SPI4_MOSI/I2S4_SDO ETH1_PPS_OUT SHRTIM1_EEV GTIMA2_CH2 GTIMB3_BRK DVP1_D10 LCD_B5 SDRAM_CKE1 UART10_RX FDCAN2_RX I2C1_SMBA I2C4_SMBA	-
-	-	K9	-	VSS	S	-	-	-	-
B5	192	A5	165	PB6	IO	TT	Yes	SHRTIM1_EEV GTIMA2_CH3 GTIMA3_CH1 GTIMB2_CH1N DVP1_D5 SDMMC1_D6 SDRAM_NCE1 USART1_TX UART10_TX LPUART1_TX FDCAN2_TX I2C1_SCL I2C4_SCL DSMU_DATIN5	-
C5	193	B5	166	PB7	IO	TT	Yes	ETH1_MII_TXD2/ETH1_G MII_TXD2 SHRTIM1_EEV GTIMA2_CH4 GTIMA3_CH2 GTIMB3_CH1N DVP1_VSYNC SDMMC1_D7 FEMC_NL/FEMC_NADV USART1_RX LPUART1_RX I2C1_SDA I2C4_SDA DSMU_CKIN5	-
E8	194	C5	167	BOOT0	I	BOOT	Yes	BOOT0	-
D5	195	A2	168	PB8	IO	TT	Yes	ETH1_MII_TXD3/ETH1_G MII_TXD3 GTIMA2_ETR	-

								GTIMA3_CH3 GTIMB2_CH1P DVP1_D6 LCD_B6 SDMMC1_CKIN SDMMC1_D4 SDMMC2_D4 UART9_RX FDCAN1_RX I2C1_SCL I2C4_SCL DSMU_CKIN7	
D4	196	B3	169	PB9	IO	FT	Yes	SPI2_NSS I2S2_WS GTIMA3_CH4 GTIMB3_CH1P DVP1_D7 LCD_B7 SDMMC1_CDIR SDMMC1_D5 SDMMC2_D5 UART9_TX FDCAN1_TX I2C1_SDA I2C4_SDA I2C4_SMBA DSMU_DATIN7	-
C4	197	B4	170	PE0	IO	TT	Yes	SHRTIM1_SCIN GTIMA3_ETR GTIMB1_CH3 LPTIM1_ETR LPTIM2_ETR DVP1_D2 LCD_R0 FEMC_NBL0 SDRAM_DQM0 UART12_RX	-
B4	198	C4	171	PE1	IO	TT	Yes	SHRTIM1_SCOUT GTIMB1_CH4 LPTIM1_IN2 DVP1_D3 LCD_R6 FEMC_NBL1 SDRAM_DQM1 UART12_TX SDRAM_D15	-
A7	199	A4	172	VCAP	S	-	-	-	-
B6	200	K10	173	VSS	S	-	-	-	-
E7	201	D4	174	NC	S	-	-	-	-
A6	202	A3	175	NC	S	-	-	-	-
-	-	-	176	VDD	S	-	-	-	-
A4	203	-	-	PI4	IO	TT	Yes	xSPI2_NCS2 ETH1_GMII_TXD4 ATIM2_BKIN1 DVP1_D5 DVP2_D8 LCD_B4 FEMC_NBL2 SDRAM_DQM2 USART8_RX I2C10_SMBA SDRAM_D0	-

A3	204	-	-	PI5	IO	TT	Yes	xSPI2_NCS3 ETH1_GMII_TXD5 ATIM2_CH1 DVP1_VSYNC DVP2_D9 LCD_B5 FEMC_NBL3 SDRAM_DQM3 USART8_TX I2C10_SDA SDRAM_D1	-
A2	205	-	-	PI6	IO	TT	Yes	xSPI2_NCS4 ETH1_GMII_TXD6 SHRTIM1_FLT ATIM2_CH2 DVP1_D6 DVP2_D10 LCD_B6 FEMC_D28 SDRAM_D28 USART8_CK I2C10_SCL SDRAM_D2	-
B3	206	-	-	PI7	IO	TT	Yes	xSPI2_NCSIN ETH1_GMII_TXD7 ATIM2_CH3 DVP1_D7 DVP2_D11 LCD_B7 FEMC_D29 SDRAM_D29 SDRAM_D3	-
G7/ G8/ G9/ G10/ G11/ H7/ H8/ H9/ H10/ H11/ J7/ J8/ J9/ J10/ J11/ K7/ K8/ K9/ K10/ K11/ L7/ L8/ L9/ L10/ L11	207	K12 /G8/ H7/ H8/ H9/ J8	-	VSS	S	-	-	-	-
-	208	-	-	VDD	S	-		-	-

N17/ M16/ M17/ L16/ L17/ K16/ K17	-	-	-	NC	-	-	-	-	-

3.3 GPIO Multiplexing Functions

3.3.1 GPIOA Multiplexing Functions

Table 0-2 GPIOA Multiplexing Functions

Port	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PA0	ETH1_MII_CRS/ETH1_GMII_CRS	SDMMC2_CMD	FEMC_A19	SPI4_NSS	I2S4_WS	ATIM2_ETR	GTIMA1_CH1	GTIMA1_ETR	GTIMA4_CH1	GTIMB1_BRK	USART2_CTS/USART2_NSS	UART9_TX	-	-	EVENTOUT	-
PA1	-	-	ETH1_MII_RX_CLK/ETH1_RMII_REF_CLK/ETH1_GMII_RX_CLK	LCD_R2	GTIMA1_CH2	GTIMA4_CH2	GTIMB1_CH1N	LPTIM3_OUT	USART2_DE/USART2_RTS	UART9_RX	-	-	-	-	EVENTOUT	-
PA2	-	ETH1_MDIO	LCD_R1	GTIMA1_CH3	GTIMA4_CH3	GTIMB1_CH1P	LPTIM4_OUT	USART2_TX	-	-	-	-	-	-	EVENTOUT	-
PA3	-	-	ETH1_MII_COL/ETH1_GMII_COL	FEMC_A10	LCD_B2	LCD_B5	I2S4_MCK	GTIMA1_CH4	GTIMA4_CH4	GTIMB1_CH2	LPTIM5_OUT	USART2_RX	-	-	EVENTOUT	-
PA4	SDRAM_D8	FEMC_D8/FEMC_DA8	LCD_VSYNC	DVP1_HSYNC	SPI1_NSS	SPI3_NSS	SPI4_NSS	I2S1_WS	I2S3_WS	I2S4_WS	GTIMA4_ETR	USART2_CK	USB2_SOF	-	EVENTOUT	-
PA5	SDRAM_D9	SDRAM_DQM0	FEMC_D9/FEMC_DA9	LCD_R4	SPI1_SCK	SPI4_SCK	I2S1_CK	I2S4_CK	ATIM2_CH1N	GTIMA1_CH1	GTIMA1_ETR	-	-	-	EVENTOUT	-
PA6	-	xSPI2_IO3	LCD_G2	DVP1_PIXCLK	SPI1_MISO	SPI4_MISO	I2S1_SDI	I2S4_SDI	ATIM1_BKIN1	ATIM2_BKIN1	ATIM3_CH1	GTIMA2_CH1	-	-	EVENTOUT	-
PA7	SDRAM_NWE	-	xSPI2_IO2	ETH1_MII_RX_DV/ETH1_RMII_CRS_DV/ETH1_GMII_RX_DV	LCD_VSYNC	SPI1_MOSI	SPI4_MOSI	I2S1_SDO	I2S4_SDO	ATIM1_CH1N	ATIM2_CH1N	ATIM4_CH1	GTIMA2_CH2	-	EVENTOUT	-
PA8	ETH2_MII_RX_CLK/ETH2_RMII_REF_CLK	LCD_B3	LCD_R6	SHRTIM1_CHB2	ATIM1_CH1	ATIM2_BKIN2	USART1_CK	UART11_RX	USB1_SOF	I2C3_SCL	I2C5_SCL	-	-	-	EVENTOUT	RCC_MCO1
PA9	ETH1_MII_TX_ER/ETH1_GMII_TX_ER	LCD_R5	DVP1_D0	SPI2_SCK	I2S2_CK	SHRTIM1_CHC1	ATIM1_CH2	USART1_TX	LPUART1_TX	USB1_VBUS	I2C3_SMBA	I2C5_SMBA	-	-	EVENTOUT	-
PA10	LCD_B1	LCD_B4	DVP1_D1	SHRTIM1_CHC2	ATIM1_CH3	USART1_RX	LPUART1_RX	USB1_ID	-	-	-	-	-	-	EVENTOUT	-
PA13	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT	JTMS/SWDIO
PA14	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT	JTCK/SWCLK
PA15	LCD_B6	LCD_R3	SPI1_NSS	SPI3_NSS	SPI4_NSS	I2S1_WS	I2S3_WS	I2S4_WS	-	GTIMA1_CH1	GTIMA1_ETR	UART9_DE/UART9_RTS	UART11_TX	-	EVENTOUT	JTDI

NSING Technologies Pte. Ltd.
Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

3.3.2 GPIOB Multiplexing Functions

Table 0-3 GPIOB Multiplexing Functions

Port	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PB0	-	xSPI2_IO1	ETH1_MII_RXD2/ETH1_GMII_RXD2	LCD_G1	LCD_R3	ATIM1_CH2N	ATIM2_CH2N	GTIMA2_CH3	UART9_CTS	DSMU_CKOUT	-	-	-	-	EVENTOUT	-
PB1	-	xSPI2_IO0	ETH1_MII_RXD3/ETH1_GMII_RXD3	LCD_G0	LCD_R6	DVP1_MCLK	SPI3_MISO	ATIM1_CH3N	ATIM2_CH3N	GTIMA2_CH4	DSMU_DATIN1	-	-	-	EVENTOUT	-
PB2	-	-	xSPI2_CLK/xSPI2_CLKIN	ETH1_MII_TX_ER/ETH1_GMII_TX_ER	DVP1_HSYNC	DVP2_D12	SPI3_MOSI	I2S3_SDO	ATIM1_CH4N	ATIM2_CH4N	GTIMA5_ETR	DSMU_CKIN1	-	-	EVENTOUT	RTC_OUT2
PB3	SDMMC2_D2	SPI1_SCK	SPI3_SCK	SPI4_SCK	I2S1_CK	I2S3_CK	I2S4_CK	-	GTIMA1_CH2	GTIMA6_ETR	UART11_RX	-	-	-	EVENTOUT	JTDO/TRACESWO
PB4	ETH1_PHY_INTN	SDMMC2_D3	SPI1_MISO	SPI2_NSS	SPI3_MISO	SPI4_MISO	I2S1_SDI	I2S2_WS	I2S3_SDI	I2S4_SDI	GTIMA2_CH1	GTIMB2_BRK	UART11_TX	-	EVENTOUT	JTRST
PB5	SDRAM_CKE1	-	ETH1_PPS_OUT	LCD_B5	DVP1_D10	SPI1_MOSI/I2S1_SDO	SPI3_MOSI/I2S3_SDO	SPI4_MOSI/I2S4_SDO	GTIMA2_CH2	GTIMB3_BRK	UART10_RX	FDCAN2_RX	I2C1_SMBA	I2C4_SMBA	EVENTOUT	-
PB6	SDRAM_NCE1	-	SDMMC1_D6	DVP1_D5	GTIMA2_CH3	GTIMA3_CH1	GTIMB2_CH1N	USART1_TX	UART10_TX	LPUART1_TX	FDCAN2_TX	I2C1_SCL	I2C4_SCL	DSMU_DATIN5	EVENTOUT	-
PB7	ETH1_MII_TXD2/ETH1_GMII_TXD2	SDMMC1_D7	FEMC_NL/FEMC_NADV	DVP1_VSYNC	-	GTIMA2_CH4	GTIMA3_CH2	GTIMB3_CH1N	USART1_RX	LPUART1_RX	I2C1_SDA	I2C4_SDA	DSMU_CKIN5	-	EVENTOUT	-
PB8	ETH1_MII_TXD3	SDMMC1_CKIN	SDMMC1_D4	SDMMC2_D4	LCD_B6	DVP1_D6	GTIMA2_ETR	GTIMA3_CH3	GTIMB2_CH1P	UART9_RX	FDCAN1_RX	I2C1_SCL	I2C4_SCL	DSMU_CKIN7	EVENTOUT	-
PB9	SDMMC1_CDIR	SDMMC1_D5	SDMMC2_D5	LCD_B7	DVP1_D7	SPI2_NSS/I2S2_WS	GTIMA3_CH4	GTIMB3_CH1P	UART9_TX	FDCAN1_TX	I2C1_SDA	I2C4_SDA	I2C4_SMBA	DSMU_DATIN7	EVENTOUT	-
PB10	-	ETH1_MII_RX_ER/ETH1_GMII_RX_ER	FEMC_D13/FEMC_DA13	LCD_G4	SPI2_SCK	I2S2_CK	SHRTIM1_SCOUT	GTIMA1_CH3	LPTIM2_IN1	USART3_TX	I2C2_SCL	DSMU_DATIN7	-	-	EVENTOUT	-
PB11	ETH1_MII_TX_EN/ETH1_RMII_TX_EN/ETH1_GMII_TX_EN	FEMC_D15/FEMC_DA15	LCD_G5	SHRTIM1_SCIN	GTIMA1_CH4	LPTIM2_ETR	USART3_RX	I2C2_SDA	DSMU_CKIN7	-	-	-	-	-	EVENTOUT	-
PB12	-	-	ETH1_MII_TXD0/ETH1_RMII_TXD0/ETH1_GMII_TXD0	-	DVP2_D14	SPI2_NSS/I2S2_WS	ATIM1_BKIN1	LPTIM2_IN2	USART3_CK	UART10_RX	FDCAN2_RX	USB2_ID	I2C2_SMBA	DSMU_DATIN1	EVENTOUT	-
PB13	-	ETH1_MII_TXD1/ETH1_RMII_TXD1/ETH1_GMII_TXD1	SDMMC1_D0	DVP1_D2	SPI2_SCK	I2S2_CK	ATIM1_CH1N	LPTIM2_OUT	USART3_CTS/USART3_NSS	UART10_TX	FDCAN2_TX	USB2_VBUS	DSMU_CKIN1	-	EVENTOUT	-
PB14	SDRAM_D10	SDMMC2_D0	FEMC_D10/FEMC_DA10	LCD_CLK	SPI2_MISO	I2S2_SDI	ATIM1_CH2N	ATIM2_CH2N	GTIMA7_CH1	USART1_TX	USART3_DE/USART3_RTS	UART9_DE/UART9_RTS	USB2_DM	DSMU_DATIN2	EVENTOUT	-
PB15	SDRAM_D11	SDMMC2_D1	FEMC_D11/FEMC_DA11	LCD_G7	SPI2_MOSI	I2S2_SDO	ATIM1_CH3N	ATIM2_CH3N	GTIMA7_CH2	USART1_RX	UART9_CTS	USB2_DP	DSMU_CKIN2	-	EVENTOUT	RTC_REFIN

NSING Technologies Pte. Ltd.
Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

3.3.3 GPIOC Multiplexing Functions

Table 0-4 GPIOC Multiplexing Functions

Port	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PC0	SDRAM_NWE	SDRAM_D12	ETH2_MII_RX_DV/ETH2_RMII_CRS_DV	FEMC_A25	FEMC_D12/FEMC_DA12	LCD_G2	LCD_R5	DSMU_CKIN0	DSMU_DATIN4	-	-	-	-	-	EVENTOUT	-
PC1	-	ETH1_MDC	SDMMC2_CK	LCD_G5	SPI2_MOSI	I2S2_SDO	DSMU_CKIN4	DSMU_DATIN0	FEMC_D0/FEMC_DA0	-	-	-	-	-	EVENTOUT	TRACED0
PC2	SDRAM_NCE0	-	-	-	ETH1_MII_TXD2/ETH1_GMII_TXD2	DVP2_D6	SPI2_MISO	I2S2_SDI	DSMU_CKIN1	DSMU_CKOUT	-	-	-	-	EVENTOUT	-
PC3	SDRAM_CKE0	-	-	-	ETH1_MII_TX_CLK/ETH1_GMII_TX_CLK	DVP2_D7	SPI2_MOSI	I2S2_SDO	DSMU_DATIN1	-	-	-	-	-	EVENTOUT	-
PC4	SDRAM_NCE0	ETH1_MII_RXD0/ETH1_RMII_RXD0/ETH1_GMII_RXD0	SDMMC2_CKIN	FEMC_A22	LCD_R7	I2S1_MCK	DSMU_CKIN2	-	-	-	-	-	-	-	EVENTOUT	-
PC5	SDRAM_CKE0	-	ETH1_MII_RXD1/ETH1_RMII_RXD1/ETH1_GMII_RXD1	FEMC_A1	LCD_DE	DSMU_DATIN2	COMP1_OUT	SDRAM_NCAS	SDMMC2_SEL	-	-	-	-	-	EVENTOUT	-
PC6	SDMMC1_D0DIR	SDMMC1_D6	SDMMC2_D6	FEMC_NWAIT	LCD_HSYNC	DVP1_D0	I2S2_MCK	SHRTIM1_CHA1	ATIM2_CH1	GTIMA2_CH1	USART4_TX	DSMU_CKIN3	-	-	EVENTOUT	-
PC7	SDMMC1_D123DIR	SDMMC1_D7	SDMMC2_D7	FEMC_NE1/FEMC_NCE2	LCD_G6	DVP1_D1	I2S3_MCK	SHRTIM1_CHA2	ATIM2_CH2	GTIMA2_CH2	USART4_RX	DSMU_DATIN3	-	-	EVENTOUT	TRGIO
PC8	SDMMC1_D0	FEMC_NCE1/FEMC_NE2	FEMC_INT/FEMC_BUSY	DVP1_D2	SHRTIM1_CHB1	ATIM2_CH3	GTIMA2_CH3	USART4_CK	UART10_DE/UART10_RTS	-	-	-	-	-	EVENTOUT	TRACED1
PC9	-	SDMMC1_D1	LCD_B2	LCD_G3	DVP1_D3	I2S1_CKIN	I2S2_CKIN	I2S3_CKIN	I2S4_CKIN	ATIM2_CH4	GTIMA2_CH4	UART10_CTS	I2C3_SDA	I2C5_SDA	EVENTOUT	RCC_MCO2
PC10	-	SDMMC1_D2	LCD_R2	LCD_B1	DVP1_D8	SPI3_SCK	I2S3_CK	USART3_TX	UART9_TX	I2C5_SDA	DSMU_CKIN5	-	-	-	EVENTOUT	-
PC11	-	SDMMC1_D3	LCD_B4	DVP1_D4	SPI3_MISO	I2S3_SDI	-	USART3_RX	UART9_RX	I2C5_SCL	DSMU_DATIN5	-	-	-	EVENTOUT	-
PC12	SDRAM_D6	SDMMC1_CK	FEMC_D6/FEMC_DA6	LCD_R6	DVP1_D9	SPI3_MOSI	SPI4_SCK	I2S3_SDO	I2S4_CK	GTIMB1_CH1P	USART3_CK	UART10_TX	I2C5_SMBA	-	EVENTOUT	TRACED3
PC13	-	-	-	-	-	-	-	-	-	RTC_TAMP1 / RTC_TS	-	-	-	-	EVENTOUT	RTC_OUT1
PC14	-	-	-	-	-	-	-	-	-	TIMESTAMP	-	-	-	-	EVENTOUT	-
PC15	-	-	-	-	-	-	-	-	-	TIMESTAMP	-	-	-	-	EVENTOUT	-

NSING Technologies Pte. Ltd.
Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

3.3.4 GPIOD Multiplexing Functions

Table 0-5 GPIOD Multiplexing Functions

Port	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PD0	SDRAM_D2	SDRAM_D11	SDMMC1_WP	FEMC_D2/FEMC_DA2	LCD_B1	GTIMB2_CH1N	UART9_RX	UART13_CTS	FDCAN1_RX	DSMU_CKIN6	-	-	-	-	EVENTOUT	-
PD1	SDRAM_D3	SDRAM_D12	SDMMC1_CD	FEMC_D3/FEMC_DA3	GTIMB2_CH1P	UART9_TX	FDCAN1_TX	I2C1_SMBA	DSMU_DATIN6	-	-	-	-	-	EVENTOUT	-
PD2	SDRAM_D7	SDRAM_D13	SDMMC1_CMD	FEMC_D7/FEMC_DA7	LCD_B2	LCD_B7	DVP1_D11	GTIMA2_ETR	GTIMB1_BRK	GTIMB2_CH2	UART10_RX	LPUART2_CTS	-	-	EVENTOUT	TRACED2
PD3	SDMMC1_RST	FEMC_CLK	LCD_G7	DVP1_D5	SPI2_SCK	I2S2_CK	GTIMB2_CH3	USART2_CTS/USART2_NSS	LPUART2_DE/LPUART2_RTS	DSMU_CKOUT	-	-	-	-	EVENTOUT	-
PD4	-	SDMMC2_WP	FEMC_NOE	DVP1_D14	SPI3_NSS	-	GTIMB2_CH4	USART2_DE/USART2_RTS	LPUART2_TX	I2C1_SCL	-	-	-	-	EVENTOUT	-
PD5	-	SDMMC2_CD	FEMC_NWE	DVP1_D15	SPI3_MISO	GTIMB2_ETR	USART2_TX	LPUART2_RX	I2C1_SDA	-	-	-	-	-	EVENTOUT	-
PD6	-	SDMMC2_CK	FEMC_NWAIT	LCD_B2	DVP1_D10	SPI3_MOSI	I2S3_SDO	USART2_RX	DSMU_CKIN4	DSMU_DATIN1	-	-	-	-	EVENTOUT	-
PD7	-	SDMMC2_CMD	FEMC_NE1/FEMC_NCE2	SPI1_MOSI	SPI3_SCK	I2S1_SDO	ATIM4_BKIN1	USART2_CK	DSMU_CKIN1	DSMU_DATIN4	-	-	-	-	EVENTOUT	-
PD8	SDRAM_D13	-	FEMC_D13/FEMC_DA13	DVP2_HSYNC	SHRTIM2_SCIN	ATIM3_CH3	USART3_TX	I2C7_SDA	DSMU_CKIN3	-	-	-	-	-	EVENTOUT	-
PD9	SDRAM_D14	FEMC_D14/FEMC_DA14	DVP2_VSYNC	SHRTIM2_SCOUT	ATIM3_CH3N	USART3_RX	I2C7_SCL	DSMU_DATIN3	-	-	-	-	-	-	EVENTOUT	-
PD10	SDRAM_D15	ETH1_CLK125	ETH2_PPS_OUT	FEMC_D15/FEMC_DA15	LCD_B3	ATIM1_CH4N	LPTIM2_OUT	USART3_CK	I2C7_SMBA	DSMU_CKOUT	-	-	-	-	EVENTOUT	-
PD11	-	FEMC_A16/FEMC_CLE	DVP2_D15	GTIMA3_ETR	LPTIM2_IN2	USART3_CTS/USART3_NSS	I2C4_SMBA	-	-	-	-	-	-	-	EVENTOUT	-
PD12	-	FEMC_A17/FEMC_ALE	DVP1_D12	GTIMA3_CH1	LPTIM1_IN1	LPTIM2_IN1	USART3_DE/USART3_RTS	UART12_TX	UART13_CTS	FDCAN3_RX	I2C4_SCL	-	-	-	EVENTOUT	-
PD13	-	FEMC_A18	DVP1_D13	GTIMA3_CH2	LPTIM1_OUT	UART12_RX	UART13_DE/UART13_RTS	FDCAN3_TX	I2C4_SDA	I2C8_SMBA	-	-	-	-	EVENTOUT	-
PD14	SDRAM_D0	SDRAM_CKE0	ETH1_PPS_OUT	SDMMC1_D4	FEMC_D0/FEMC_DA0	ATIM3_CH4	GTIMA3_CH3	UART12_CTS	UART13_RX	I2C8_SDA	-	-	-	-	EVENTOUT	-
PD15	SDRAM_D1	ETH1_PHY_INTN	ETH2_PHY_INTN	SDMMC1_D5	FEMC_D1/FEMC_DA1	ATIM3_CH4N	GTIMA3_CH4	UART12_DE/UART12_RTS	UART13_TX	I2C8_SCL	-	-	-	-	EVENTOUT	-

NSING Technologies Pte. Ltd.
Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

3.3.5 GPIOE Multiplexing Functions

Table 0-6 GPIOE Multiplexing Functions

Port	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PE0	SDRAM_DQM0	-	FEMC_NBL0	LCD_R0	DVP1_D2	SHRTIM1_SCIN	GTIMA3_ETR	GTIMB1_CH3	LPTIM1_ETR	LPTIM2_ETR	UART12_RX	-	-	-	EVENTOUT	-
PE1	SDRAM_DQM1	-	FEMC_NBL1	LCD_R6	DVP1_D3	SHRTIM1_SCOUT	GTIMB1_CH4	LPTIM1_IN2	UART12_TX	SDRAM_D15	-	-	-	-	EVENTOUT	-
PE2	-	ETH1_MII_TXD3/ETH1_GMII_TXD3	FEMC_A23	DVP2_D0	SPI6_SCK	GTIMB1_ETR	USART5_RX	FDCAN4_TX	-	-	-	-	-	-	EVENTOUT	TRACECLK
PE3	ETH1_MII_TXD2/ETH1_GMII_TXD2	FEMC_A19	DVP2_D1	GTIMB1_BRK	USART5_TX	FDCAN4_RX	-	-	-	-	-	-	-	-	EVENTOUT	TRACED0
PE4	ETH2_PHY_INTN	FEMC_A20	LCD_B0	DVP1_D4	SPI6_NSS	GTIMB1_CH1N	USART6_RX	DSMU_DATIN3	-	-	-	-	-	-	EVENTOUT	TRACED1
PE5	xSPI2_NCS1	FEMC_A21	LCD_G0	DVP1_D6	SPI6_MISO	GTIMB1_CH1P	USART6_TX	DSMU_CKIN3	-	-	-	-	-	-	EVENTOUT	TRACED2
PE6	FEMC_A22	LCD_G1	DVP1_D7	SPI6_MOSI	ATIM1_BKIN2	GTIMB1_CH2	-	-	-	-	-	-	-	-	EVENTOUT	TRACED3
PE7	SDRAM_D4	-	-	xSPI2_NCS2	ETH2_PHY_INTN	FEMC_D4/FEMC_DA4	ATIM1_ETR	UART11_RX	I2C7_SDA	DSMU_DATIN2	-	-	-	-	EVENTOUT	-
PE8	SDRAM_D5	SDRAM_A0	-	-	SDMMC1_LEDCTRL	FEMC_D5/FEMC_DA5	ATIM1_CH1N	UART11_TX	FDCAN5_TX	I2C7_SCL	DSMU_CKIN2	COMP2_OUT	-	-	EVENTOUT	-
PE9	SDRAM_D6	SDRAM_A1	-	-	SDMMC2_LEDCTRL	FEMC_D6/FEMC_DA6	ATIM1_CH1	UART11_DE/UART11_RTS	FDCAN5_RX	I2C7_SMBA	DSMU_CKOUT	-	-	-	EVENTOUT	-
PE10	SDRAM_D7	SDRAM_A2	-	-	FEMC_D7/FEMC_DA7	ATIM1_CH2N	UART11_CTS	DSMU_DATIN4	-	-	-	-	-	-	EVENTOUT	-
PE11	SDRAM_D8	-	FEMC_D8/FEMC_DA8	LCD_G3	SPI6_NSS	ATIM1_CH2	DSMU_CKIN4	SDRAM_A3	-	-	-	-	-	-	EVENTOUT	-
PE12	SDRAM_D9	-	ETH1_GMII_RXD4	FEMC_D9/FEMC_DA9	LCD_B4	SPI6_SCK	ATIM1_CH3N	UART13_RX	DSMU_DATIN5	COMP1_OUT	-	-	-	-	EVENTOUT	-
PE13	SDRAM_D10	ETH1_GMII_RXD5	FEMC_D10/FEMC_DA10	LCD_DE	SPI6_MISO	ATIM1_CH3	UART13_TX	FDCAN6_TX	I2C6_SDA	DSMU_CKIN5	COMP2_OUT	-	-	-	EVENTOUT	-
PE14	SDRAM_D11	-	ETH1_GMII_RXD6	FEMC_D11	LCD_CLK	SPI6_MOSI	ATIM1_CH4	USART6_CK	UART13_CTS	FDCAN6_RX	I2C6_SCL	-	-	-	EVENTOUT	-
PE15	SDRAM_D12	ETH1_GMII_RXD7	FEMC_D12/FEMC_DA12	LCD_R7	ATIM1_BKIN1	USART5_CK	UART13_DE/UART13_RTS	I2C6_SMBA	-	-	-	-	-	-	EVENTOUT	-

NSING Technologies Pte. Ltd.
Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

3.3.6 GPIOF Multiplexing Functions

Table 0-7 GPIOF Multiplexing Functions

Port	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PF0	SDRAM_A0	xSPI2_IO0	ETH1_GMII_TXD4	FEMC_A0	DVP2_D0	SHRTIM2_CHA1	GTIMA1_CH1	GTIMA5_CH1	USART1_TX	FDCAN4_TX	I2C2_SDA	I2C5_SDA	COMP3_OUT	-	EVENTOUT	-
PF1	SDRAM_A1	SDRAM_D5	xSPI2_IO1	ETH1_GMII_TXD5	FEMC_A1	DVP2_D1	SHRTIM2_CHA2	GTIMA1_CH2	GTIMA5_CH2	USART1_RX	FDCAN4_RX	I2C2_SCL	I2C5_SCL	-	EVENTOUT	-
PF2	SDRAM_A2	xSPI2_IO2	ETH1_GMII_TXD6	FEMC_A2	DVP2_D2	SPI6_NSS	SHRTIM2_CHB1	GTIMA1_CH3	GTIMA5_CH3	GTIMB2_ETR	USART1_CK	I2C2_SMBA	I2C5_SMBA	-	EVENTOUT	-
PF3	SDRAM_A3	xSPI2_IO3	ETH1_GMII_TXD7	FEMC_A3	DVP2_D3	SPI6_SCK	SHRTIM2_CHB2	GTIMA1_CH4	GTIMA5_CH4	GTIMB2_CH4	USART1_CTS/USART1_NSS	I2C6_SDA	-	-	EVENTOUT	-
PF4	SDRAM_A4	SDRAM_D4	xSPI2_CLK/xSPI2_CLKIN	ETH2_MII_RX_CLK/ETH2_RMII_REF_CLK	FEMC_A4	DVP2_D4	SPI6_MISO	SHRTIM2_CHC1	GTIMA1_ETR	GTIMB2_CH3	USART1_DE/USART1_RTS	FDCAN5_TX	I2C6_SCL	-	EVENTOUT	-
PF5	SDRAM_A5	xSPI2_NCLK	ETH1_GMII_GTX_CLK	FEMC_A5	DVP2_D5	SPI6_MOSI	SHRTIM2_CHC2	ATIM3_BKIN1	GTIMB2_CH2	FDCAN5_RX	I2C6_SMBA	-	-	-	EVENTOUT	-
PF6	-	xSPI2_IO3	ETH2_MDIO	DVP1_PIXCLK	DVP2_D5	SPI5_NSS	ATIM3_ETR	ATIM4_ETR	GTIMA5_CH1	GTIMB2_CH1P	UART11_RX	FDCAN3_RX	-	-	EVENTOUT	-
PF7	-	xSPI2_IO2	ETH2_MDC	DVP2_PIXCLK	SPI5_SCK	ATIM3_CH4	ATIM4_CH3	GTIMA5_CH2	GTIMB3_CH1P	UART11_TX	FDCAN3_TX	-	-	-	EVENTOUT	-
PF8	-	xSPI2_IO0	ETH2_MII_COL	SDMMC2_LEDCTRL	DVP2_HSYNC	SPI5_MISO	ATIM3_CH1	ATIM4_CH4	GTIMA5_CH3	GTIMB2_CH1N	UART11_DE/UART11_RTS	-	-	-	EVENTOUT	-
PF9	-	xSPI2_IO1	ETH2_MII_CRS	SDMMC1_LEDCTRL	DVP2_VSYNC	SPI5_MOSI	-	ATIM3_CH2	ATIM4_CH1	GTIMA5_CH4	GTIMB3_CH1N	UART11_CTS	-	-	EVENTOUT	-
PF10	-	xSPI2_CLK/xSPI2_CLKIN	ETH2_PPS_OUT	LCD_DE	DVP1_D11	ATIM3_CH3	ATIM4_CH2	GTIMB2_BRK	FEMC_A3	-	-	-	-	-	EVENTOUT	-
PF11	SDRAM_NRAS	-	DVP1_D12	SPI5_MOSI	GTIMA6_CH1	I2C6_SDA	ETH2_MII_TX_EN/ETH2_RMII_TX_EN	-	-	-	-	-	-	-	EVENTOUT	-
PF12	SDRAM_A6	xSPI2_DQS	ETH2_MII_TXD0/ETH2_RMII_TXD0	FEMC_A6	DVP2_D6	GTIMA6_CH2	FDCAN6_TX	I2C6_SCL	-	-	-	-	-	-	EVENTOUT	-
PF13	SDRAM_A7	SDRAM_NCE0	ETH2_MII_TXD1/ETH2_RMII_TXD1	FEMC_A7	DVP2_D7	-	GTIMA6_CH3	USART7_CK	FDCAN6_RX	I2C4_SMBA	I2C6_SMBA	DSMU_DATIN6	COMP3_OUT	-	EVENTOUT	-
PF14	SDRAM_A8	ETH2_MII_TXD2	FEMC_A8	DVP2_D8	SHRTIM2_CHF1	GTIMA6_CH4	USART7_RX	FDCAN3_RX	I2C4_SCL	DSMU_CKIN6	-	-	-	-	EVENTOUT	-
PF15	SDRAM_A9	SDRAM_BA0	ETH2_MII_TXD3	FEMC_A9	DVP2_D9	SHRTIM2_CHF2	LPTIM4_ETR	USART7_TX	FDCAN3_TX	I2C4_SDA	-	-	-	-	EVENTOUT	-

NSING Technologies Pte. Ltd.
Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

3.3.7 GPIOG Multiplexing Functions

Table 0-8 GPIOG Multiplexing Functions

Port	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PG0	SDRAM_A10	SDRAM_BA1	xSPI2_IO4	xSPI2_NCS2	ETH2_MII_TX_CLK	FEMC_A10	DVP2_D10	ATIM4_BKIN1	LPTIM4_IN1	UART13_RX	-	-	-	-	EVENTOUT	-
PG1	SDRAM_A11	SDRAM_A10	xSPI2_IO5	xSPI2_NCS3	ETH2_MII_TX_ER	FEMC_A11	DVP2_D11	-	GTIMB1_ETR	LPTIM4_IN2	UART13_TX	-	-	-	EVENTOUT	-
PG2	SDRAM_A12	SDRAM_DQM1	ETH2_MII_RXD0/ETH2_RMII_RXD0	FEMC_A12	DVP2_D12	SHRTIM2_SCIN	ATIM2_BKIN1	GTIMA6_ETR	USART7_CTS/USART7_NSS	FDCAN8_TX	-	-	-	-	EVENTOUT	-
PG3	ETH2_MII_RXD1/ETH2_RMII_RXD1	FEMC_A13	DVP2_D13	SHRTIM2_SCOUT	ATIM2_BKIN2	GTIMA5_ETR	USART7_DE/USART7_RTS	FDCAN8_RX	-	-	-	-	-	-	EVENTOUT	-
PG4	SDRAM_BA0	ETH2_MII_RXD2	SDMMC2_CKIN	SDMMC2_D4	FEMC_A14	DVP2_D14	SHRTIM1_CHF1	ATIM1_BKIN2	USART6_CTS/USART6_NSS	I2C1_SDA	I2C8_SDA	-	-	-	EVENTOUT	-
PG5	SDRAM_BA1	-	ETH2_MII_RXD3	SDMMC2_CDIR	SDMMC2_D5	FEMC_A15	DVP2_D15	SHRTIM1_CHF2	ATIM1_ETR	USART6_DE/USART6_RTS	I2C1_SCL	I2C8_SCL	-	-	EVENTOUT	-
PG6	-	ETH2_MII_RX_ER	FEMC_NE3	LCD_R7	DVP1_D12	SHRTIM1_CHE1	GTIMB3_BRK	I2C1_SMBA	I2C8_SMBA	-	-	-	-	-	EVENTOUT	-
PG7	xSPI2_DQS	ETH1_PHY_INTN	FEMC_INT/FEMC_BUSY	LCD_CLK	DVP1_D13	SHRTIM1_CHE2	USART4_CK	FDCAN7_TX	-	-	-	-	-	-	EVENTOUT	-
PG8	SDRAM_CLK	-	ETH1_PPS_OUT	LCD_G7	SPI4_NSS	I2S4_WS	ATIM2_ETR	USART4_DE/USART4_RTS	FDCAN7_RX	-	-	-	-	-	EVENTOUT	-
PG9	-	ETH2_MII_RXD0/ETH2_RMII_RXD0	SDMMC2_D0	FEMC_NCE1/FEMC_NE2	DVP1_VSYNC	SPI1_MISO	I2S1_SDI	USART4_RX	FDCAN3_TX	-	-	-	-	-	EVENTOUT	-
PG10	xSPI2_IO6	xSPI2_NCS4	ETH2_MII_RXD1/ETH2_RMII_RXD1	SDMMC2_D1	FEMC_NE3	LCD_B2	LCD_G3	DVP1_D2	SPI1_NSS	I2S1_WS	-	FDCAN3_RX	-	-	EVENTOUT	-
PG11	xSPI2_IO7	xSPI2_NCSIN	ETH1_MII_TX_EN/ETH1_RMII_TX_EN/ETH1_GMII_TX_EN	SDMMC2_D2	LCD_B3	DVP1_D3	SPI1_SCK	I2S1_CK	LPTIM1_IN2	USART5_RX	-	-	-	-	EVENTOUT	-
PG12	xSPI2_NCS1	ETH1_MII_TXD1/ETH1_RMII_TXD1/ETH1_GMII_TXD1	SDMMC2_D3	FEMC_NE4	LCD_B1	LCD_B4	DVP2_MCLK	SPI4_MISO	I2S4_SDI	GTIMA5_CH1	LPTIM1_IN1	USART4_DE/USART4_RTS	USART5_TX	-	EVENTOUT	-
PG13	ETH1_MII_TXD0/ETH1_RMII_TXD0/ETH1_GMII_TXD0	SDMMC2_D0DIR	SDMMC2_D6	FEMC_A24	LCD_R0	SPI4_SCK	I2S4_CK	GTIMA5_CH2	LPTIM1_OUT	USART4_CTS/USART4_NSS	USART5_CTS/USART5_NSS	-	-	-	EVENTOUT	TRACED0
PG14	-	ETH1_MII_TXD1/ETH1_RMII_TXD1/ETH1_GMII_TXD1	SDMMC2_D123DIR	SDMMC2_D7	FEMC_A25	LCD_B0	SPI4_MOSI	I2S4_SDO	GTIMA5_CH3	LPTIM1_ETR	USART4_TX	USART5_DE/USART5_RTS	-	-	EVENTOUT	TRACED1
PG15	SDRAM_NCAS	xSPI2_DQS	ETH1_PHY_INTN	SDMMC2_RST	DVP1_D13	USART4_CTS/USART4_NSS	USART5_CK	SDRAM_D14	-	-	-	-	-	-	EVENTOUT	-

NSING Technologies Pte. Ltd.
Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

3.3.7 GPIOH Multiplexing Functions

Table 0-9 GPIOH Multiplexing Functions

Port	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PH0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT	-
PH1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT	-
PH2	SDRAM_CKE0	-	-	xSPI2_IO4	ETH1_MII_CRS/ETH1_GMII_CRS	LCD_R0	SHRTIM2_CHD1	GTIMB3_CH2	LPTIM1_IN2	UART15_RX	-	-	-	-	EVENTOUT	-
PH3	SDRAM_NCE0	-	xSPI2_IO5	ETH1_MII_COL/ETH1_GMII_COL	LCD_R1	SHRTIM2_CHD2	GTIMB3_CH3	USART7_CK	UART15_TX	-	-	-	-	-	EVENTOUT	-
PH4	ETH2_MII_TXD0/ETH2_RMII_TXD0	LCD_G4	LCD_G5	DVP2_HSYNC	SHRTIM2_CHE1	GTIMB3_CH4	USART7_RX	UART15_DE/UART15_RTS	FDCAN5_TX	I2C2_SCL	-	-	-	-	EVENTOUT	-
PH5	SDRAM_NWE	ETH2_MII_TXD1/ETH2_RMII_TXD1	DVP2_PIXCLK	SPI5_NSS	SHRTIM2_CHE2	GTIMB3_ETR	USART7_TX	UART15_CTS	FDCAN5_RX	I2C2_SDA	-	-	-	-	EVENTOUT	-
PH6	SDRAM_NCE1	SDRAM_A4	ETH1_MII_RXD2/ETH1_GMII_RXD2	FEMC_BAA	DVP1_D8	SPI5_SCK	ATIM1_CH4N	GTIMA7_CH1	LPTIM5_IN1	UART14_RX	FDCAN7_TX	I2C2_SMBA	-	-	EVENTOUT	-
PH7	SDRAM_CKE1	ETH1_MII_RXD3/ETH1_GMII_RXD3	FEMC_CRE	DVP1_D9	SPI5_MISO	ATIM3_BKIN1	LPTIM5_IN2	UART14_TX	FDCAN7_RX	I2C3_SCL	SDRAM_A5	-	-	-	EVENTOUT	-
PH8	SDRAM_D16	SDRAM_A6	ETH1_GMII_RXD4	FEMC_D16	LCD_R2	DVP1_HSYNC	ATIM3_CH1	GTIMA4_ETR	UART10_DE/UART10_RTS	UART14_DE/UART14_RTS	FDCAN2_RX	I2C3_SDA	COMP4_OUT	-	EVENTOUT	-
PH9	SDRAM_D17	ETH1_GMII_RXD5	FEMC_D17	LCD_R3	DVP1_D0	ATIM3_CH1N	GTIMA7_CH2	UART10_CTS	UART14_CTS	FDCAN2_TX	I2C3_SMBA	SDRAM_A7	-	-	EVENTOUT	-
PH10	SDRAM_D18	SDRAM_A8	ETH1_GMII_RXD6	FEMC_D18	LCD_R4	DVP1_D1	ATIM3_CH2	GTIMA4_CH1	I2C4_SMBA	-	-	-	-	-	EVENTOUT	-
PH11	SDRAM_D19	ETH1_GMII_RXD7	FEMC_D19	LCD_R5	DVP1_D2	ATIM3_CH2N	GTIMA4_CH2	UART10_RX	I2C4_SCL	SDRAM_A9	-	-	-	-	EVENTOUT	-
PH12	SDRAM_D20	SDRAM_A11	ETH2_MII_RX_DV/ETH2_RMII_CRS_DV	FEMC_D20	LCD_R6	DVP1_D3	SPI7_NSS	ATIM3_ETR	GTIMA4_CH3	UART10_TX	I2C4_SDA	COMP4_OUT	-	-	EVENTOUT	-
PH13	SDRAM_D21	ETH2_MII_TX_EN/ETH2_RMII_TX_EN	FEMC_D21	LCD_G2	SPI7_NSS	ATIM2_CH1N	UART9_TX	FDCAN1_TX	I2C9_SMBA	-	-	-	-	-	EVENTOUT	-
PH14	SDRAM_D22	ETH2_MII_TXD0/ETH2_RMII_TXD0	FEMC_D22	LCD_G3	DVP1_D4	SPI7_MISO	ATIM2_CH2N	USART6_RX	UART9_RX	FDCAN1_RX	I2C9_SDA	-	-	-	EVENTOUT	-
PH15	SDRAM_D23	-	ETH2_MII_TXD1/ETH2_RMII_TXD1	FEMC_D23	LCD_G4	DVP1_D11	SPI7_MOSI	ATIM2_CH3N	USART6_TX	I2C9_SCL	-	-	-	-	EVENTOUT	-

NSING Technologies Pte. Ltd.
Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

3.3.8 GPIOI Multiplexing Functions

Table 0-10 GPIOI Multiplexing Functions

Port	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PI0	SDRAM_D24	FEMC_D24	LCD_G5	DVP1_D13	SPI2_NSS	I2S2_WS	ATIM2_CH4N	GTIMA4_CH4	I2C10_SDA	-	-	-	-	-	EVENTOUT	-
PI1	SDRAM_D25	SDRAM_D8	ETH2_MII_RXD0	FEMC_D25	LCD_G6	DVP1_D8	SPI2_SCK	I2S2_CK	ATIM2_BKIN2	USART8_CK	I2C8_SMBA	I2C10_SCL	-	-	EVENTOUT	-
PI2	SDRAM_D26	ETH2_MII_RXD1	FEMC_D26	LCD_G7	DVP1_D9	SPI2_MISO	I2S2_SDI	ATIM2_CH4	USART8_RX	LPUART2_TX	I2C8_SDA	SDRAM_D9	-	-	EVENTOUT	-
PI3	SDRAM_D27	SDRAM_D10	ETH2_MII_RX_ER	FEMC_D27	DVP1_D10	SPI2_MOSI	I2S2_SDO	ATIM2_ETR	USART8_TX	LPUART2_RX	I2C8_SCL	I2C10_SMBA	-	-	EVENTOUT	-
PI4	SDRAM_DQM2	xSPI2_NCS2	ETH1_GMII_TXD4	FEMC_NBL2	LCD_B4	DVP1_D5	DVP2_D8	ATIM2_BKIN1	USART8_RX	I2C10_SMBA	SDRAM_D0	-	-	-	EVENTOUT	-
PI5	SDRAM_DQM3	SDRAM_D1	xSPI2_NCS3	ETH1_GMII_TXD5	FEMC_NBL3	LCD_B5	DVP1_VSYNC	DVP2_D9	ATIM2_CH1	USART8_TX	I2C10_SDA	-	-	-	EVENTOUT	-
PI6	SDRAM_D28	xSPI2_NCS4	ETH1_GMII_TXD6	FEMC_D28	LCD_B6	DVP1_D6	DVP2_D10	ATIM2_CH2	USART8_CK	I2C10_SCL	SDRAM_D2	-	-	-	EVENTOUT	-
PI7	SDRAM_D29	SDRAM_D3	xSPI2_NCSIN	ETH1_GMII_TXD7	FEMC_D29	LCD_B7	DVP1_D7	DVP2_D11	ATIM2_CH3	-	-	-	-	-	EVENTOUT	-
PI8	ETH2_MII_TX_CLK	SDMMC1_SEL	SDMMC2_SEL	SPI7_SCK	LPTIM3_IN1	FDCAN1_TX	-	-	-	-	-	-	-	-	EVENTOUT	RTC_OUT2
PI9	SDRAM_D30	xSPI2_IO0	FEMC_D30	LCD_VSYNC	-	GTIMA7_CH3	LPTIM3_IN2	UART9_RX	FDCAN1_RX	I2C9_SMBA	SDRAM_D6	-	-	-	EVENTOUT	-
PI10	SDRAM_D31	SDRAM_D7	xSPI2_IO1	ETH1_MII_RX_ER	FEMC_D31	LCD_HSYNC	GTIMA7_CH4	LPTIM3_ETR	FDCAN4_TX	I2C9_SDA	-	-	-	-	EVENTOUT	-
PI11	xSPI2_IO2	SDMMC1_LEDCTRL	SDMMC2_LEDCTRL	FEMC_D0	LCD_G6	GTIMA7_ETR	FDCAN4_RX	I2C9_SCL	-	-	-	-	-	-	EVENTOUT	-
PI12	xSPI2_IO3	FEMC_A4	LCD_HSYNC	DVP2_D2	SPI7_NSS	GTIMA7_CH3	FDCAN6_TX	I2C7_SDA	-	-	-	-	-	-	EVENTOUT	-
PI13	xSPI2_CLK	FEMC_A7	LCD_VSYNC	DVP2_D3	SPI7_MISO	GTIMA7_CH4	FDCAN6_RX	I2C7_SCL	-	-	-	-	-	-	EVENTOUT	-
PI14	xSPI2_NCLK	FEMC_A9	LCD_CLK	DVP2_D4	SPI7_MOSI	ATIM3_BKIN2	GTIMA7_ETR	I2C7_SMBA	-	-	-	-	-	-	EVENTOUT	-
PI15	ETH2_PPS_OUT	LCD_G2	LCD_R0	DVP2_D13	ATIM3_BKIN2	GTIMB3_ETR	-	-	-	-	-	-	-	-	EVENTOUT	-

NSING Technologies Pte. Ltd.
Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

3.3.9 GPIOJ Multiplexing Functions

Table 0-11 GPIOJ Multiplexing Functions

Port	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PJ0	ETH2_MII_TXD2	LCD_R1	LCD_R7	-	ATIM4_ETR	GTIMB3_CH1N	UART15_RX	FDCAN8_TX	I2C9_SDA	-	-	-	-	-	EVENTOUT	-
PJ1	xSPI2_IO4	ETH2_MII_TXD3	LCD_R2	DVP2_VSYNC	SPI7_SCK	ATIM4_CH1	GTIMB3_CH1P	UART15_TX	FDCAN8_RX	I2C9_SCL	-	-	-	-	EVENTOUT	-
PJ2	xSPI2_IO5	LCD_R3	DVP1_D15	SPI7_NSS	ATIM4_CH1N	GTIMB3_CH2	UART15_RTS	I2C9_SMBA	-	-	-	-	-	-	EVENTOUT	-
PJ3	ETH2_MII_RX_DV	LCD_R4	DVP1_D14	SPI7_MISO	ATIM4_CH2	GTIMB3_CH3	UART13_RTS	UART15_CTS	FDCAN7_TX	I2C9_SDA	-	-	-	-	EVENTOUT	-
PJ4	ETH2_MII_RX_CLK	LCD_R5	DVP1_D13	SPI7_MOSI	ATIM4_CH2N	GTIMB3_CH4	UART13_CTS	FDCAN7_RX	I2C9_SCL	-	-	-	-	-	EVENTOUT	-
PJ5	ETH2_MII_TX_ER	LCD_R6	DVP1_D9	-	ATIM4_BKIN2	LPTIM5_ETR	-	-	-	-	-	-	-	-	EVENTOUT	-
PJ6	FEMC_D2	LCD_R7	DVP2_D8	ATIM2_CH2	FDCAN7_TX	-	-	-	-	-	-	-	-	-	EVENTOUT	-
PJ7	FEMC_D3	LCD_G0	DVP2_D9	ATIM2_CH2N	FDCAN7_RX	-	-	-	-	-	-	-	-	-	EVENTOUT	TRGIN
PJ8	ETH2_MII_RXD2	LCD_G1	DVP2_D10	ATIM1_CH3N	ATIM2_CH1	USART8_CTS	UART12_TX	UART14_RTS	FDCAN8_TX	I2C8_SDA	-	-	-	-	EVENTOUT	-
PJ9	ETH2_MII_RXD3	LCD_G2	DVP2_D11	ATIM1_CH3	ATIM2_CH1N	USART8_RTS	UART12_RX	UART14_CTS	FDCAN8_RX	I2C8_SCL	-	-	-	-	EVENTOUT	-
PJ10	FEMC_D5/ FEMC_DA5	LCD_G3	DVP2_D12	SPI5_MOSI	ATIM1_CH2N	ATIM2_CH2	UART12_CTS	UART14_RX	I2C8_SMBA	-	-	-	-	-	EVENTOUT	-
PJ11	FEMC_D6/ FEMC_DA6	LCD_G4	DVP2_D13	SPI5_MISO	ATIM1_CH2	ATIM2_CH2N	UART12_RTS	UART14_TX	-	-	-	-	-	-	EVENTOUT	-
PJ12	SDMMC1_SEL	FEMC_BAA	LCD_B0	LCD_G3	DVP2_D15	ATIM4_CH3	I2C10_SMBA	-	-	-	-	-	-	-	EVENTOUT	TRGOUT
PJ13	SDMMC2_SEL	FEMC_NBL0	LCD_B1	LCD_B4	DVP2_D14	ATIM4_CH3N	I2C10_SDA	-	-	-	-	-	-	-	EVENTOUT	-
PJ14	FEMC_CRE	LCD_B2	DVP2_D13	ATIM4_CH4	I2C10_SCL	-	-	-	-	-	-	-	-	-	EVENTOUT	-
PJ15	FEMC_BAA	LCD_B3	DVP2_D12	ATIM4_CH4N	-	-	-	-	-	-	-	-	-	-	EVENTOUT	-

NSING Technologies Pte. Ltd.
Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

3.3.9 GPIOK Multiplexing Functions

Table 0-12 GPIOK Multiplexing Functions

Port	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PK0	ETH2_MII_COL	LCD_G5	DVP2_D7	SPI5_SCK	ATIM1_CH1N	ATIM2_CH3	I2C3_SCL	-	-	-	-	-	-	-	EVENTOUT	-
PK1	ETH2_MII_CRS	LCD_G6	DVP2_D6	SPI5_NSS	ATIM1_CH1	ATIM2_CH3N	I2C3_SDA	-	-	-	-	-	-	-	EVENTOUT	-
PK2	FEMC_A11	LCD_G7	DVP2_D5	ATIM1_BKIN1	ATIM2_BKIN1	I2C3_SMBA	-	-	-	-	-	-	-	-	EVENTOUT	-
PK3	xSPI2_IO6	FEMC_D7	LCD_B4	DVP2_D0	ATIM4_BKIN2	I2C10_SDA	-	-	-	-	-	-	-	-	EVENTOUT	-
PK4	xSPI2_IO7	FEMC_D9	LCD_B5	DVP2_D1	GTIMA6_CH1	I2C10_SCL	-	-	-	-	-	-	-	-	EVENTOUT	-
PK5	xSPI2_NCS1	FEMC_D11	LCD_B6	DVP2_D2	GTIMA6_CH2	I2C10_SMBA	-	-	-	-	-	-	-	-	EVENTOUT	-
PK6	xSPI2_DQS	FEMC_A12	LCD_B7	DVP2_D3	GTIMA6_CH3	I2C10_SDA	-	-	-	-	-	-	-	-	EVENTOUT	-
PK7	-	FEMC_A15	LCD_DE	DVP2_D4	GTIMA6_CH4	I2C10_SCL	-	-	-	-	-	-	-	-	EVENTOUT	-

NSING Technologies Pte. Ltd.
Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

4 Electrical Characteristics

4.1 Test Conditions

Unless otherwise specified, all voltages are referenced to VSS.

4.1.1 Minimum and Maximum Values

For Beta versions, minimum and maximum values are based on design simulations.

Notes under each table indicate data obtained through comprehensive evaluation, design simulation, and/or process characteristics, which will not be tested in production lines. Based on comprehensive evaluation, minimum and maximum values are derived by taking the average value from sample testing, plus or minus three times the standard distribution (average ±3∑).

4.1.2 Typical Values

Unless otherwise specified, typical data is based on TA=25°C and VDD=3.3V (voltage range 1.8V ≤ VDD ≤ 3.6V). These data are provided only as design guidance and are not tested.

4.1.3 Typical Curves

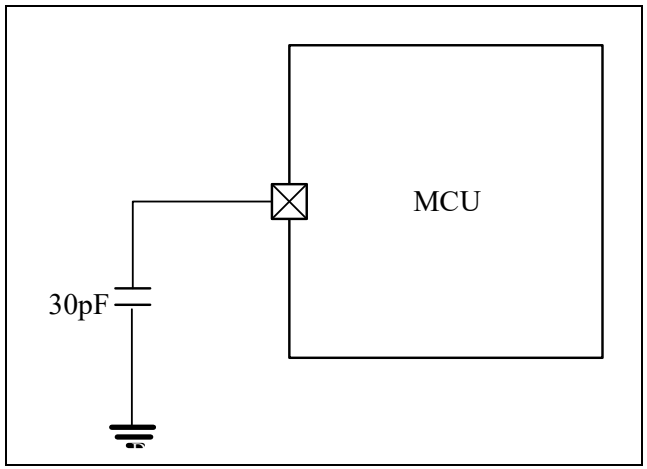
Unless otherwise specified, typical curves are provided only as design guidance and are not tested.

4.1.4 Load Capacitance

The load conditions for measuring pin parameters are shown in Figure 4-1.

NSING Technologies Pte. Ltd.
Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

Figure 4-1: Load Conditions for Pins



4.1.5 Pin Input Voltage

The method for measuring input voltage on pins is shown in Figure 4-2.

Figure 4-2: Pin Input Voltage

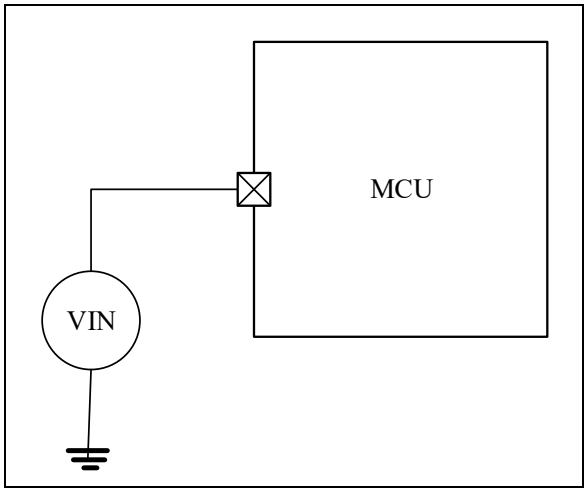
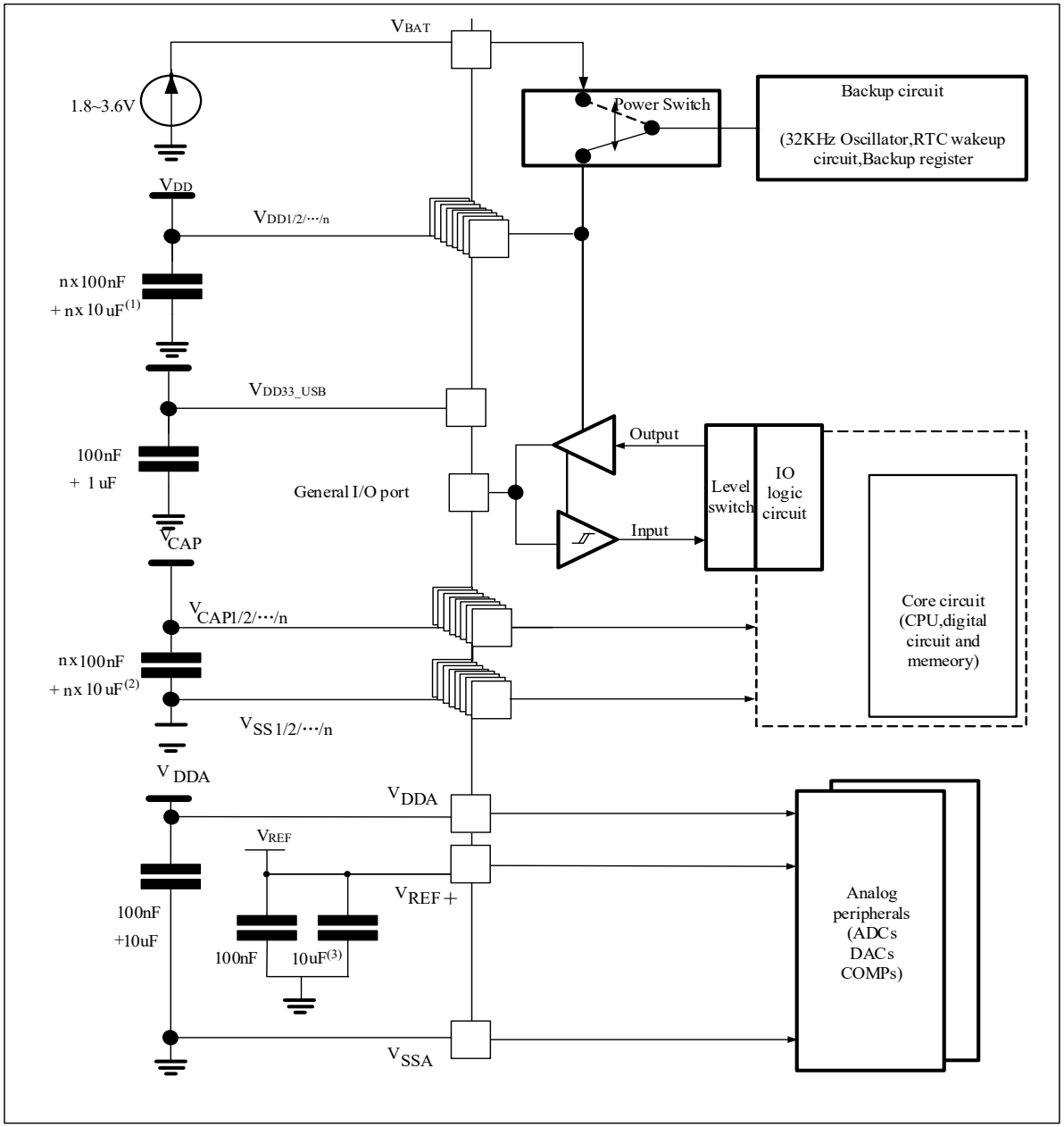


Figure 4-3 Power Supply Scheme

NSING Technologies Pte. Ltd.
Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

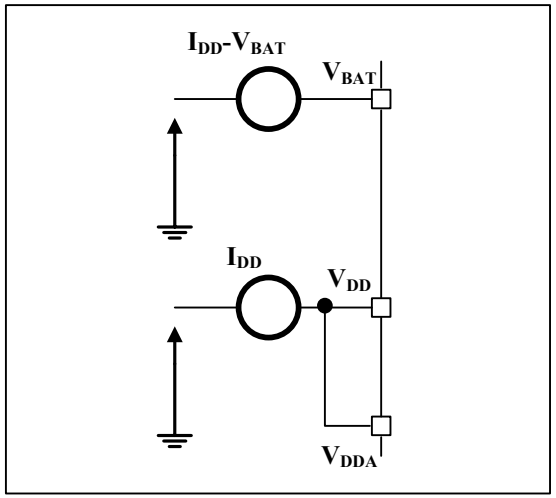


NSING Technologies Pte. Ltd.
Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

Note: 1. The 10μF capacitor in the above figure must be connected to the specified VDD.

4.1.7 Current Consumption Measurement

Figure 4-4: Current Consumption Measurement Scheme 0-1



4.2 Absolute Maximum Ratings

Loads applied to the device that exceed the values given in the "Absolute Maximum Ratings" tables (Table 4-1, Table 4-2, Table 4-3) may cause permanent damage to the device. These values only indicate the maximum tolerable loads and do not imply that the device will function correctly under these conditions. Long-term operation at maximum values will affect device reliability.

Table 4-1: Voltage Characteristics

Symbol	Description	Minimum	Maximum	Unit
V_{DD} - V_{SS}	External main supply voltage (including V_{DDA}和V_{DD})(1)	-0.3	4.0	V
V_{IN}	Input voltage on 5V-tolerant pins (3)	V_{SS}-0.3	5.5	
	Input voltage on other pins (2)	V_{SS}-0.3	V_{DD} + 0.3	
$\lvert \Delta V_{DDx} \rvert$	Voltage difference between different supply pins	-	50	mV
$\lvert V_{SSx} - V_{SS} \rvert$	Voltage difference between different ground pins	-	50	
$V_{ESD(HBM)}$	ESD electrostatic discharge voltage (human body model)	See Section **Error! Reference source not found.**		

1. All power supply (VDD, VDDA) and ground (VSS, VSSA) pins must always be connected to an external power system within the allowable range.
2. VIN should not exceed its maximum value; for current characteristics, refer to Table 4-2.

NSING Technologies Pte. Ltd.
Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

3. When a 5V-tolerant pin receives 5.5V input, VDD cannot be lower than 2.25V.

Table 4-2: Current Characteristics

Symbol	Description	Maximum (1)	Unit
I_{VDD}	Total current through VDD/VDDA power lines (supply current) (1)(4)	TBD	mA
I_{VSS}	Total current through VSS ground lines (output current) (1)(4)	TBD	
I_{IO}	Output sink current on any I/O and control pin	12	
	Output source current on any I/O and control pin	-12	
$I_{INJ(PIN)}$(2)(3)	Injection current for NRST pin	-5/0	
	Injection current for other pins	+/-5	

1. All power supply (VDD, VDDA) and ground (VSS, VSSA) pins must always be connected to an external power system within the allowable range.
2. When VIN > VDD, there is a forward injection current; when VIN < VSS, there is a reverse injection current. IINJ(PIN) should not exceed its maximum value; for voltage characteristics, refer to Table 4-1.
3. Reverse injection current will interfere with the device's analog performance. See Section 4.3.27.
4. When maximum current occurs, the maximum allowed VDD voltage drop is 0.1VDD.

Table 4-3: Temperature Characteristics

Symbol	Description	Value	Unit
T_{STG}	Storage temperature range	-40 ~ + 150	℃
T_J	Maximum junction temperature	125	℃

4.3 Operating Conditions

4.3.1 General Operating Conditions

Table 4-4: General Operating Conditions

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
f_{CPU}	Arm® Cortex®-M7 clock frequency	VCORE = 0.9V	-	600	MHz
f_{ACLK}	AXI clock frequency	VCORE = 0.9V	-	300	
f_{HCLK}	AHB clock frequency	VCORE = 0.9V	-	300	

NSING Technologies Pte. Ltd.
Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

f_{PCLK}	APB clock frequency	VCORE = 0.9V	-	150	
V_{DD}	Standard operating voltage	-	2.3	3.63	V
V_{DDA}	Analog section operating voltage	Must be the same as VDD(1)	2.3	3.63	V
V_{BAT}	Backup section operating voltage	-	1.8	3.63	V
T_A	Ambient temperature (temperature grade 7)	Maximum power consumption	-40	TBD	℃
T_J	Junction temperature range	Temperature [7]	-40	125	℃

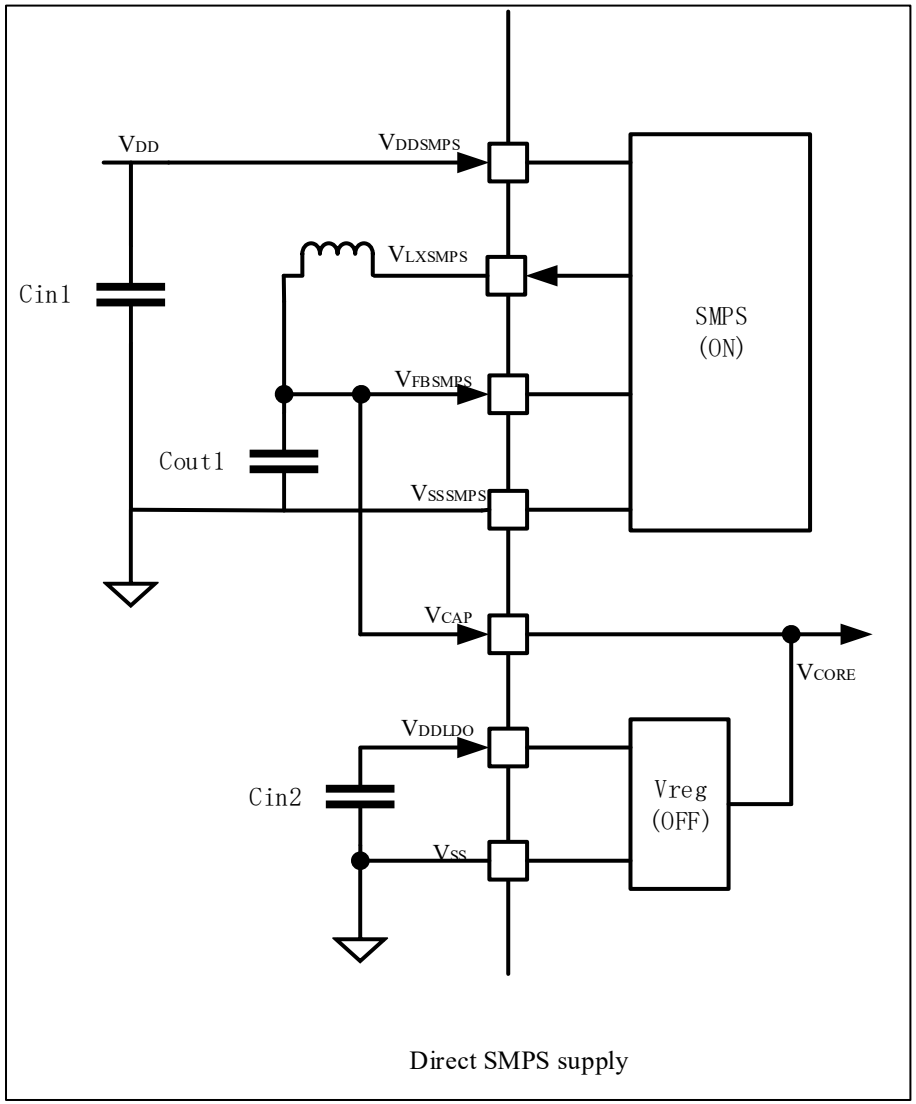
1. It is recommended to use the same power supply for VDD and VDDA. During power-up and normal operation, a maximum difference of 300mV is allowed between VDD and VDDA.

4.3.2 SMPS Buck Converter

The characteristics of the externally used SMPS are shown in Table 4-6

NSING Technologies Pte. Ltd.
Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

Figure 4-5 External components of the SMPS Buck Converter



NSING Technologies Pte. Ltd.
Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

Table 4-5 Characteristics of externally used SMPS Buck Converter

Symbol	Condition	Minimum	Typical	Maximum	Unit
V_{DDSMPS}		2.3	-	3.6	V
V_{OUT}	I_{OUT}=1A	0.72	-	0.99	V
I_{OUT}		-	-	1	A
RDS_{ON}	PMOS	-	56	116	mΩ
	NMOS	-	100	131	mΩ
I_{DDSMPS_Q}	Quiescent current	-	630	TBD	nA
T_{SMPS_START}	Iload=0mA	-	-	1.2	ms

Table 4-6 Characteristics of external components required for SMPS Buck Converter

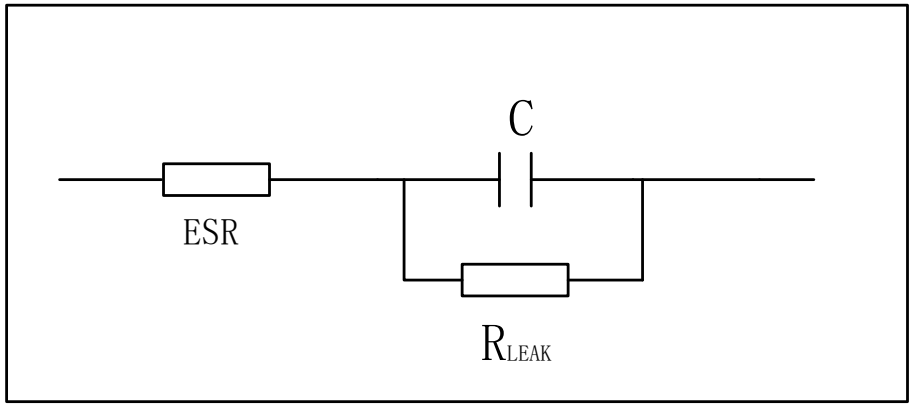
Symbol	Parameter	Condition
Cin	Value of external capacitor on VDDSMPS	47 uF
	ESR of external capacitor	10mΩ
Cout	Value of external capacitor on VFBSMPS	47 uF
	ESR of external capacitor	10mΩ
L	Static current	1uH
-	Serial DC resistance	10mΩ

4.3.3 VCAP External Capacitor

The stability of the main regulator can be achieved by connecting an external capacitor CEXT to the VCAP pin. Table 4-5 specifies CEXT. Two external capacitors can be connected to the VCAP pin.

NSING Technologies Pte. Ltd.
Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

Figure 4-6: External Capacitor C_{EXT}



1. ESR is Equivalent Series Resistance

Table 4-8: VCAP Operating Conditions

Symbol	Parameter	Conditions
C_{EXT}	V_{DD} rise rate	TBD
ESR	External capacitor ESR	TBD

4.3.4 Operating Conditions During Power-up and Power-down

The parameters given in the table below are tested at the ambient temperature (25°C) listed in Table 4-4.

Table 4-9: Operating Conditions During Power-up and Power-down

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
t_{VDD}	V_{DD} rise rate	-	TBD	∞	µs/V
	V_{DD} fall rate		TBD	∞	

4.3.5 Embedded Reset and Power Control Module Characteristics

The parameters given in the table below are tested at the ambient temperature (25°C) and VDD supply voltage listed in Table 4-4.

NSING Technologies Pte. Ltd.
Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

Table 4-9: Embedded Reset and Power Control Module Characteristics

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{PVD}	Programmable voltage detector level selection	PRS[2:0]=000 (Rising edge)	1.7	1.78	1.86	V
		PRS[2:0]=000 (Falling edge)	1.6	1.68	1.76	V
		PRS[2:0]=001 (Rising edge)	1.8	1.88	1.96	V
		PRS[2:0]=001 (Falling edge)	1.7	1.78	1.86	V
		PRS[2:0]=010 (Rising edge)	1.9	1.98	2.06	V
		PRS[2:0]=010 (Falling edge)	1.8	1.88	1.96	V
		PRS[2:0]=011 (Rising edge)	2	2.08	2.16	V
		PRS[2:0]=011 (Falling edge)	1.9	1.98	2.06	V
		PRS[2:0]=100 (Rising edge)	2.09	2.18	2.26	V
		PRS[2:0]=100 (Falling edge)	2.28	2.38	2.46	V
		PRS[2:0]=101 (Rising edge)	2.19	2.28	2.36	V
		PRS[2:0]=101 (Falling edge)	2.38	2.48	2.56	V
		PRS[2:0]=110 (Rising edge)	2.28	2.38	2.46	V
		PRS[2:0]=110 (Falling edge)	2.46	2.58	2.66	V
		PRS[2:0]=111 (Rising edge)	2.36	2.48	2.56	V
		PRS[2:0]=111 (Falling edge)	2.56	2.68	2.76	V
	Programmable voltage detector level selection	PRS[2:0]=000 (Rising edge)	2.46	2.58	2.66	V
		PRS[2:0]=000 (Falling edge)	2.66	2.78	2.86	V
		PRS[2:0]=001 (Rising edge)	2.56	2.68	2.76	V
		PRS[2:0]=001 (Falling edge)	2.76	2.88	2.96	V
		PRS[2:0]=010 (Rising edge)	2.66	2.78	2.86	V
		PRS[2:0]=010 (Falling edge)	2.6	2.68	2.76	V
		PRS[2:0]=011 (Rising edge)	2.8	2.88	2.96	V
		PRS[2:0]=011 (Falling edge)	2.7	2.78	2.86	V

NSING Technologies Pte. Ltd.
Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

		PRS[2:0]=100 (Rising edge)	3.2	3.28	3.36	V
		PRS[2:0]=100 (Falling edge)	3.1	3.18	3.26	V
		PRS[2:0]=101 (Rising edge)	3.3	3.38	3.46	V
		PRS[2:0]=101 (Falling edge)	3.2	3.28	3.36	V
		PRS[2:0]=110 (Rising edge)	3.4	3.48	3.56	V
		PRS[2:0]=110 (Falling edge)	3.2	3.28	3.36	V
		PRS[2:0]=111 (Rising edge)	3.5	3.58	3.66	V
		PRS[2:0]=111 (Falling edge)	3.4	3.48	3.56	V
$V_{PVDhyst}$(1)	PVD hysteresis	-	-	100	-	mV
V_{POR}	VDD power-on/power-down reset threshold	-	-	1.62	-	V
V_{BOR}	BOR power-on/power-down reset threshold	BOR_CFG[2:0]=000(Rising edge)	1.7	1.72	1.75	V
		BOR_CFG [2:0]=000(Falling edge)	1.65	1.67	1.69	V
		BOR_CFG[2:0]=001(Rising edge)	1.85	1.9	1.95	V
		BOR_CFG[2:0]=001(Falling edge)	1.75	1.8	1.85	V
		BOR_CFG[2:0]=010(Rising edge)	2.15	2.2	2.25	V
		BOR_CFG[2:0]=010(Falling edge)	2.05	2.1	2.15	V
		BOR_CFG[2:0]=011(Rising edge)	2.45	2.5	2.55	V
		BOR_CFG[2:0]=011(Falling edge)	2.35	2.4	2.45	V
		BOR_CFG[2:0]=100(Rising edge)	2.75	2.8	2.85	V
		BOR_CFG[2:0]=100(Falling edge)	2.65	2.7	2.75	V
$T_{RSTTEMPO}$(1)	Reset duration	-	-	0.1		ms

1. Guaranteed by design, not tested in production.

4.3.6 Built-in Bandgap Reference Voltage

The parameters given in the table below are tested at the ambient temperature (25°C) and VDD supply voltage listed in Table 4-4.

NSING Technologies Pte. Ltd.
Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

Table 4-10: Built-in Reference Voltage

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{BG}	Built-in bandgap reference voltage	-40°C< T_J< +125°C	1.164	1.2	1.236	V
T_{S_BG}(1)	ADC sampling time when reading internal bandgap reference voltage		-	5.1	17.1(2)	µs
ΔV_{BG}	Internal voltage drift over the full temperature range	VDD = 3.3V -40°C< T_J< +125°C	-	-	10	mV
T_{coeff}	Temperature coefficient	-40°C< T_J< +125°C	-	-	48	ppm/°C

1. The minimum sampling time is obtained through multiple cycles in the application.
2. Guaranteed by design, not tested in production.

4.3.7 Supply Current Characteristics

Current consumption is a comprehensive indicator of various parameters and factors, including operating voltage, ambient temperature, I/O pin load, product software configuration, operating frequency, I/O pin switching rate, program location in memory, and executed code.

For current consumption measurement method details, see Figure 4-4.

All current consumption measurements in running modes given in this section are performed while executing a simplified set of code.

4.3.7.1 Maximum Current Consumption

The microcontroller is under the following conditions:

- All I/O pins are in input mode and connected to a static level—VDD or VSS (no load).
- All peripherals are turned off, unless otherwise specified.
- TCM memory access time is adjusted to the fastest frequency that can be run.
- Instruction prefetch function is enabled (Note: this parameter must be set before setting the clock and bus dividers).
- When peripherals are enabled: AXI, AHB, APB clock frequencies are configured to maximum.
- VDD=3.63V, junction temperature equals 125°C.

The parameters given in Tables 4-9 and 4-10 are tested at the ambient temperature (25°C) and VDD supply voltage listed in Table 4-4.

NSING Technologies Pte. Ltd.
Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

Table 0-11 **Maximum Current Consumption in Run Mode, Data Processing Code Running from Internal Flash**

Symbol	Parameter	Conditions		f_{HCLK}	Typical (1)	Maximum (1)				Unit
						T_J = 25℃	T_J = 85℃	T_J = 105℃	T_J = 125℃	
I_{DD}	Supply current in run mode	External clock, all peripherals enabled	0.9V	TBD	TBD	TBD	TBD	TBD	TBD	mA
				TBD	TBD	TBD	TBD	TBD	TBD	
			0.8V	TBD	TBD	TBD	TBD	TBD	TBD	
				TBD	TBD	TBD	TBD	TBD	TBD	
		External clock, all peripherals disabled	0.9V	TBD	TBD	TBD	TBD	TBD	TBD	
				TBD	TBD	TBD	TBD	TBD	TBD	
			0.8V	TBD	TBD	TBD	TBD	TBD	TBD	
				TBD	TBD	TBD	TBD	TBD	TBD	

1. Derived from comprehensive evaluation, not tested in production.

Table 4-12: Maximum Current Consumption in Sleep Mode

Symbol	Parameter	Conditions	f_{HCLK}	Typical (1)		Unit
				TBD	T_J = 125℃	
I_{DD}	Supply current in sleep mode	External clock, all peripherals enabled	TBD	TBD	TBD	mA
			TBD	TBD	TBD	
			TBD	TBD	TBD	
			TBD	TBD	TBD	
		External clock, all peripherals disabled	TBD	TBD	TBD	
			TBD	TBD	TBD	
			TBD	TBD	TBD	
			TBD	TBD	TBD	

1. Guaranteed by comprehensive evaluation results, not tested in production.

4.3.7.2 Low-power Mode Current Consumption

MCU is under the following conditions:

NSING Technologies Pte. Ltd.
Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

- All I/O pins are in input mode and connected to a static level—VDD or VSS (no load).
- All peripherals are turned off unless specifically stated.

Table 4-12 Typical and maximum current consumption in stop and standby

Symbol	Parameter	Conditions	Typical Value (1)	Unit
			T_J =25℃	
I_{DD}	Supply current in STOP0 mode	Main power domain VDDDMAIN is in running mode, low-speed and high-speed internal RC oscillators and high-speed oscillator are in off state (no independent watchdog)	TBD	μA
	Supply current in STOP2 mode	Retention domain (VDDDRET) power remains on, main power domain VDDDMAIN off, low-speed and high-speed internal RC oscillators and high-speed oscillator are in off state (no independent watchdog)	TBD	
	Supply current in STANDBY mode	Low-speed oscillator on, RTC on, IWDG on, Backup SRAM retained	TBD	
		Low-speed oscillator on, RTC off, IWDG off, Backup SRAM retained	TBD	
		Low-speed oscillator on, RTC off, IWDG off, Backup SRAM not retained	TBD	
I_{DD_VBAT}	Supply current in VBAT mode	Low-speed oscillator and RTC are on	TBD	

1. Guaranteed by comprehensive evaluation results, not tested in production.

4.3.8 External Clock Source Characteristics

4.3.8.1 High-Speed External Clock Source (External Clock)

High-speed external user clock is generated from an external source. In bypass mode, the HSE oscillator is turned off, and the input pin functions as a standard I/O. The external clock signal must comply with Table 4-12, and the recommended clock input waveform is shown in Figure 4-6.

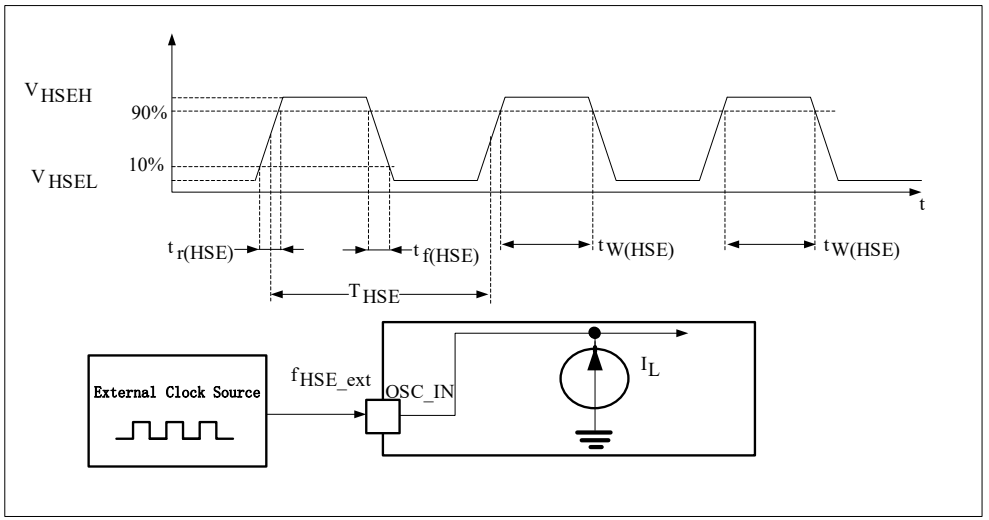
NSING Technologies Pte. Ltd.
Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

Table 4-14 High-Speed External User Clock Characteristics(1)

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
$f_{HSE-ext}$	User external clock frequency (1)	VDD=3.3V, T_A= -40~105℃	4	25	50	MHz
V_{HSEH}	OSC_IN input pin high level voltage		0.7VDD	-	VDD	V
V_{HSEL}	OSC_IN input pin low level voltage		Vss	-	0.3VDD	V
$t_{w(HSE)}$	OSC_IN high or low time (1)		7	-	-	ns

1. Guaranteed by design..

Figure 4-7 AC timing diagram for external high-speed clock source



4.3.8.2 Low-Speed External Clock Source (External Clock)

In bypass mode, the LSE oscillator is turned off, and the input pin functions as a standard I/O. The external clock signal must comply with Table 4-13, and the recommended clock input waveform is shown in Figure 4-7.

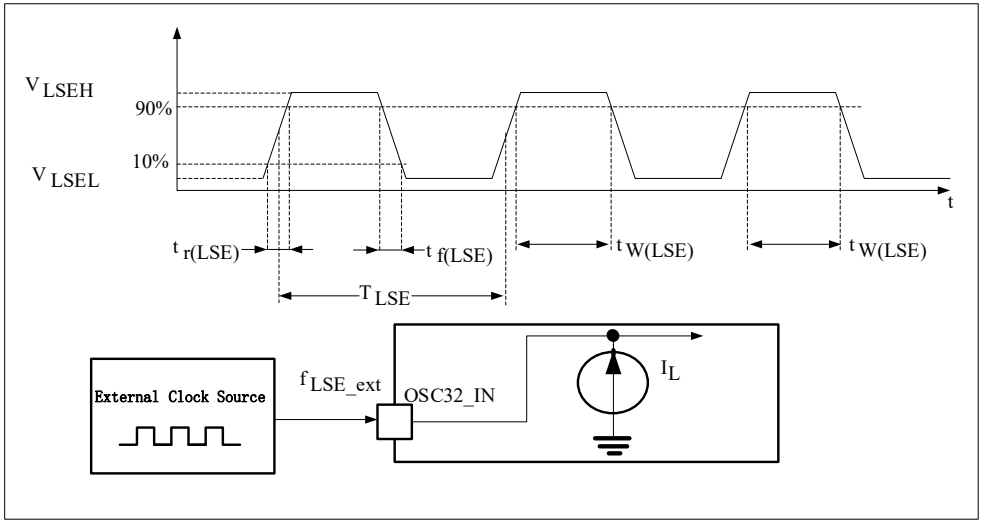
NSING Technologies Pte. Ltd.
Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

Table 4-15 Low-Speed External User Clock Characteristics(1)

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
$f_{LSE-ext}$	User external clock frequency (1)	VDD=3.3V, T_A= -40~105℃	-	32.768	1000	KHz
V_{LSEH}	OSC32_IN input pin high level voltage		0.7VDD	-	VDD	V
V_{LSEL}	OSC32_IN input pin low level voltage		Vss	-	0.3VDD	V
$t_{w(LSE)}$	OSC32_IN high or low time (1)		250	-	-	ns

1. Guaranteed by design..

Figure 4-8 AC timing diagram for external low-speed clock source



4.3.8.3 High-Speed External Clock Source (External Crystal/Ceramic)

The high-speed external (HSE) clock can be provided by a 4 to 48 MHz crystal/ceramic resonator oscillator. All information given in this section is based on the analysis results of typical external component characteristics specified in the table below. In applications, the resonator and load capacitors must be placed as

NSING Technologies Pte. Ltd.
Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

close as possible to the oscillator pins to minimize output distortion and startup stabilization time. For more details on resonator characteristics (frequency, package, accuracy), please consult the crystal resonator manufacturer.

Table 4-16 HSE 4~48MHz Oscillator Characteristics(1)

Symbol	Parameter	Conditions [2]	Minimum	Typical	Maximum	Unit
f	Oscillator frequency	-	4	25	48	MHz
R	Feedback resistance	-	-	200	-	KΩ
IDD_{HSE}	HSE drive current	启动中[3]	-	-	4	mA
		VDD=3 V, Rm=30 Ω, CL=10 pF at 4 MHz	-	0.8	-	
		VDD=3 V, Rm=30 Ω, CL=10 pF at 8 MHz	-	1.2	-	
		VDD=3 V, Rm=30 Ω, CL=10 pF at 16 MHz	-	1.5	-	
		VDD=3 V, Rm=30 Ω, CL=10 pF at 32 MHz	-	1.65	-	
		VDD=3 V, Rm=30 Ω, CL=10 pF at 48 MHz	-	2	-	
$Gm_{critmax}$	Maximum oscillator transconductance	Startup	-	-	1.5	mA/V
$t_{SU(HSE)}$[4]	Startup time	VDD already stable	-	2	5	ms

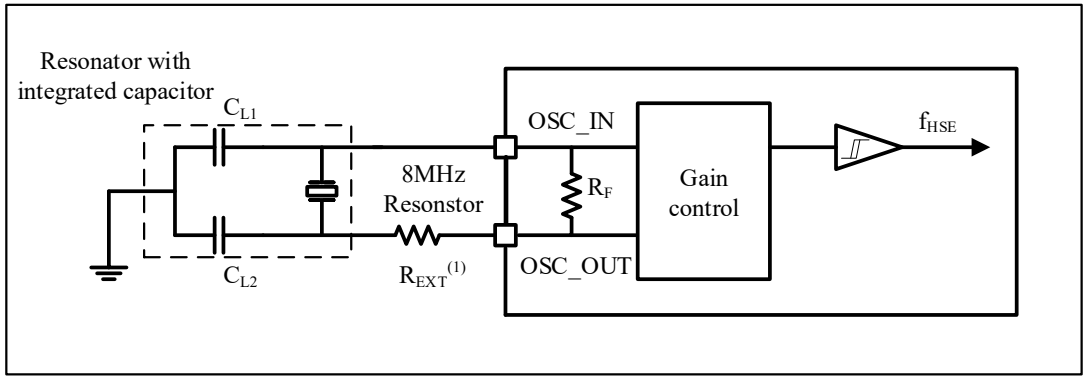
1. Guaranteed by design.
2. Resonator characteristic parameters are provided by the crystal/ceramic resonator manufacturer.
3. Time consumption occurs during the first 2/3 phase of the tSU(HSE) startup time.
4. tSU(HSE) is the startup time, measured from when HSE is enabled by software until a stable 8MHz oscillation is obtained. This value is measured on a standard crystal resonator and may vary considerably depending on the crystal manufacturer.

Note: For CL1 and CL2, it is recommended to use high-quality external ceramic capacitors in the range of 5 pF to 25 pF (typical values), which are designed for high-frequency applications, and their selection should meet the requirements of the crystal or resonator (see Figure 4-8). CL1 and CL2 are typically the same size. Crystal manufacturers usually specify a load capacitance, which is the series combination of CL1 and CL2. When determining the size of CL1 and CL2, the PCB and MCU pin capacitance must be taken into account (10 pF can be used as a rough

NSING Technologies Pte. Ltd.
Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

estimate for the combined pin and circuit board capacitance).

Figure 4-9 Typical application using an 8MHz crystal



1. The value of R_{EXT} is determined by the characteristics of the crystal.

4.3.8.4 Low-Speed External Clock Source (External Crystal/Ceramic Resonator)

The low-speed external clock (LSE) can be generated using an oscillator consisting of a 32.768kHz crystal or ceramic resonator (crystal mode).
The information provided in this section is based on comprehensive characteristic evaluations using typical external components listed in the table below.
In applications, the resonator and load capacitors must be placed as close as possible to the oscillator pins to minimize output distortion and startup stabilization time.
For detailed parameters of the crystal resonator (such as frequency, package, accuracy, etc.), please consult the respective manufacturers.
(Note: The "crystal resonator" mentioned here refers to a standard passive crystal oscillator.)
Note: For CL1 and CL2, it is recommended to use high-quality ceramic capacitors and to select crystals or resonators that meet the required specifications. Typically, CL1 and CL2 have the same specifications.
Crystal manufacturers usually specify the load capacitance parameters based on the series combination of CL1 and CL2.
The load capacitance **CL** is calculated as follows:
$C_L = C_{L1} \times C_{L2} / (C_{L1} + C_{L2}) + C_{stray}$
is the stray capacitance associated with the pins and PCB (Printed Circuit Board).
Example:
If a resonator with a specified load capacitance **CL = 6pF** is selected and **Cstray = 2pF**, then **CL1 = CL2 = 8pF**.

NSING Technologies Pte. Ltd.
Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

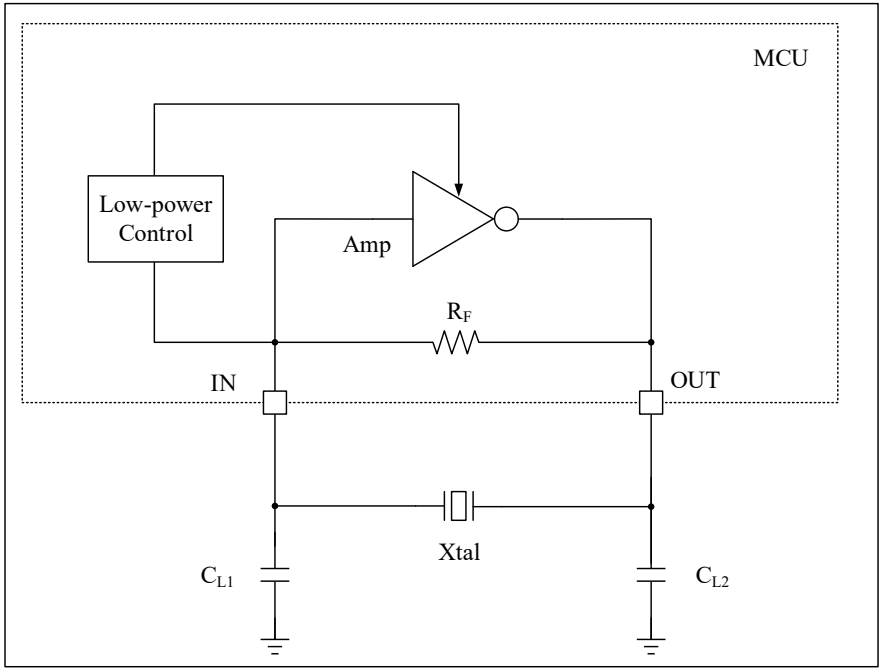
Table 4-17 LSE Oscillator Characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f	Oscillator Frequency	-	-	32.768	-	KHz
R	Feedback Resistor	-	-	100	-	KΩ
IDD_{LSE}	LSE Drive Current	Low drive capability	-	300	-	nA
		Medium-low drive capability	-	400	-	
		Medium-high drive capability	-	550	-	
		High drive capability	-	1000	-	
$Gm_{critmax}$	Maximum Oscillator Transconductance	Low drive capability	-	-	0.5	uA/V
		Medium-low drive capability	-	-	1	
		Medium-high drive capability	-	-	2	
		High drive capability	-	-	3	
t_{SU}	Startup Time	After VDD stabilizes	-	2	-	s

1. Guaranteed by comprehensive evaluation, not tested in production.
2. **tSU (LSE)** is the startup time measured from the moment LSE is enabled via software until a stable 32.768kHz oscillation is achieved. This value is measured with a standard crystal resonator and may vary significantly depending on the crystal manufacturer.

NSING Technologies Pte. Ltd.
Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

Figure 4-10 Typical Application Using a 32.768kHz Crystal



4.3.9 Internal Clock Source Characteristics

Error! Reference source not found.

4.3.9.1 64MHz High-Speed Internal Oscillator (HSI64)

Table 4-18 HSI64 Oscillator Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI64}	Frequency	VDD-3.3V, T_{JS} 25 degrees C, after calibration	63.68	64	64.32	MHz

NSING Technologies Pte. Ltd.
Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

TRIM	User calibration step size	-	-	0.5	-	%
USER TRIM COVERAGE	User calibration coverage	± 32 steps	±4.79	±5.60	-	%
ACC_{HSI64}	HSI64 Oscillator Accuracy	VDD=3.3V,T_J= -40~125℃, including temperature drift and reflow effects	-2	-	2	%
		VDD=3.3V,T_J= -20~105℃, including temperature drift and reflow effects	-1.5	-	1.5	%
ΔVDD(HSI48)	HSI64 Oscillator frequency drift with VDD	VDD=3 to 3.6 V	-	0.025	0.05	%
		VDD=2.3 V to 3.6 V	-	0.05	0.1	
$t_{SU(HSI64)}$	HSI Oscillator startup time	-	1	6	10	μs
DuCy(HSI64)	Duty cycle	-	45	50	55	%
$I_{DD(HSI64)}$	HSI Oscillator power consumption	-	-	250	350	μA
N_T jitter	Next transition jitter (accumulated over 28 cycles)	-	-	TBD	-	μs
P_T jitter	Paired transition jitter (accumulated over 56 cycles)	-	-	TBD	-	μs

NSING Technologies Pte. Ltd.
Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

4.3.9.2 Multi-Speed Internal Oscillator (MSI)

Table 0-19 MSI Oscillator Characteristics

Symbol	Parameter	Conditions	Mn	Typ	Max	Unit
f_{MSI}	Frequency	VDD = 3.3V, TJs = 25°C, after calibration, default MSI = 16MHz	15.84	16	16.16	MHz
TRIM	User calibration step size	-	-	0.175	-	%
USER TRIM COVERAGE	User calibration coverage	± 32 steps	±4.79	±5.60	-	%
ACC_{MSI}	MSI Oscillator Accuracy	VDD = 3.3V, TJ = -40~125°C, including temperature drift and reflow effects	-2	-	2	%
		VDD = 3.3V, TJ = -20~105°C, including temperature drift and reflow effects	-1.5	-	1.5	%
$t_{SU(MSI)}$	MSI Oscillator startup time	-	-	4	6	µs
DuCy(MSI)	Duty cycle	-	45	50	55	%
$I_{DD(MSI)}$	MSI Oscillator power consumption	-	-	150	200	µA

4.3.9.3 Low-Speed Internal Oscillator (LSI)

Table 4-20 LSI Oscillator Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit

NSING Technologies Pte. Ltd.
Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

f_{LSI}(2)	Output frequency	25℃ calibration, VDD =3.3V	31.36	32	32.64	KHz
		VDD =1.8V ~3.6V, T_J = -40~105℃	30.4	32	33.6	KHz
$t_{SU(LSI)}$ (3)	LSI Oscillator startup time	-	-	30	80	μs
$t_{stab(LSI)}$	LSI Oscillator stabilization time (within 5% of final value)	-	-	-	-	-
$I_{DD(LSI)}$ (3)	LSI Oscillator power consumption	-	-	1.2	2.4	μA

4.3.10 Wake-up Time from Low-Power Modes

Error! Reference source not found.

Table 4-21 Wake-up Times for Low-Power Modes

Symbol	Parameter	Typical Value (1)	Unit
$t_{WUSLEEP}$	Wake-up from Sleep mode	TBD	Cycles
$t_{WUSTOP0}$	Wake-up from Stop 0 mode	TBD	μs
	Wake-up from Stop 2 mode	TBD	μs
$t_{WUSTDBY}$	Wake-up from Standby mode	TBD	μs

4.3.11 PLL Characteristics

The parameters listed in Table 4-19 and Table 4-21 were measured under ambient temperature (25°C) and supply voltage conditions as specified in Table 4-4.

4.3.11.1 PLL1/2/3 Characteristics

Table 0-22 PLL Characteristics

Symbol	Parameter	Value			Unit
		Min	Typ	Max(1)	
f_{PLL_IN}	PLL input clock (2)	8	25	64	MHz

NSING Technologies Pte. Ltd.
Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

	PLL input clock duty cycle	40	50	60	%
f_{PLL_OUT}	PLL multiplied output clock	440	-	800	MHz
t_{LOCK}	PLL Ready signal output time	-	-	150	µs
Jitter	Rms cycle-to-cycle jitter @800MHz	-	±4	-	ps
f_{VCO_OUT}	PLL VCO output	440	-	800	MHz
I_{PLL}	Operating Current of PLL @200MHz VCO frequency.	-	3	-	uA

1. Obtained from characterization; not tested in production.
2. Care must be taken to use the correct multiplication factor so that the fPLL_OUT remains within the allowed range according to the PLL input clock frequency.

4.3.11.2 SHRPLL Characteristics

Table 0-23 SHRPLL Characteristics

Symbol	Parameter	Value			Unit
		Min	Typ	Max(1)	
f_{SHRPLL_IN}	SHRPLL input clock (2)	8	25	64	MHz
	SHRPLL input clock duty cycle	40	50	60	%
f_{SHRPLL_OUT}	SHRPLL multiplied output clock	440	-	1250	MHz
t_{LOCK}	SHRPLL Ready signal output time	10	62.5	125	µs
Jitter	Rms period jitter @1250MHz	-	±2	-	±ps
I_{SHRPLL}	Operating Current of SHRPLL @1250MHz VCO frequency.	-	6	-	mA

1. Results based on comprehensive evaluation, not tested in production.
2. Attention must be paid to using the correct multiplication factor to ensure that the `fSHRPLL_OUT` falls within the permissible range based on the input clock frequency.

4.3.12 Absolute Maximum Ratings (Electrical Sensitivity)

NSING Technologies Pte. Ltd.
Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

Based on different tests (ESD, LU), specific measurement methods are used to evaluate the chip's performance regarding electrical sensitivity.

Electrostatic Discharge (ESD)

An electrostatic discharge (one positive pulse followed by one negative pulse after one second) is applied to all pins of all samples.

Table 4-23 ESD Absolute Maximum Ratings

Symbol	Parameter	Conditions	Type	Max(1)	Unit
$V_{ESD(HBM)}$	ESD Voltage (Human Body Model)	TA = +25°C, per MIL-STD-883K Method 3015.9	3A	2000	V
$V_{ESD(CDM)}$	ESD Voltage (Charged Device Model)	TA = +25°C, per ESDA/JEDEC JS-002-2018	C3	200	

1. Results based on comprehensive evaluation, not tested in production.

Latch-Up (LU)

To evaluate latch-up performance, two complementary static latch-up tests are performed on six samples:

- Provide an over-limit supply voltage to each power pin.
- Inject current into each input, output, and configurable I/O pin.

This test complies with EIA/JESD78A IC latch-up standard.

Table 0-2 Static Latch-Up

Symbol	Parameter	Conditions	Type	Min(1)
LU	Static Latch-Up Class	T_A = +105°C，perJESD 78E	Class II A	±200mA, 1.5*VDDMAX

1. Tested under room temperature conditions.

4.3.13 I/O Port Characteristics

General Input/Output Characteristics

Unless otherwise specified, parameters listed below are measured under the conditions in Table 4-4. All I/O ports are CMOS and TTL compatible.

NSING Technologies Pte. Ltd.
Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

Table 4-24 I/O Static Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Input low level voltage	V_{DD}=3.3V	2	-	V_{DD}	V
		V_{DD}=2.5V	1.7	-	V_{DD}	
		V_{DD}=1.8V	0.7 V_{DD}	-	V_{DD}	
V_{IH}	Input high level voltage	V_{DD}=3.3V	VSS	-	0.8	
		V_{DD}=2.5V	VSS	-	0.7	
		V_{DD}=1.8V	VSS	-	0.3 V_{DD}	
Vhys	Schmitt trigger hysteresis voltage (1)	V_{DD}=3.3V	200	-	-	mV
		V_{DD}=2.5V	165	-	-	
		V_{DD}=1.8V	165	-	-	
I_{lkg}	Input leakage current (3)	V_{DD}=Maximum	-5	-	5	μA
		V_{PAD}=0 或 V_{PAD}=V_{DD}(5)				
R_{PU}	Weak pull-up equivalent resistance (4)	VDD=3.3v,V_{IN}= Vss	16	-	61.4	kΩ
		VDD=1.8~3.3v,V_{IN}= Vss	16	-	142.6	kΩ
R_{PD}	Weak pull-down equivalent resistance (4)	VDD=3.3v,V_{IN}= VDD	16	-	61.4	kΩ
		VDD=1.8~3.3v,VIN= VDD	16	-	142.6	kΩ
C_{IO}	I/O pin capacitance	-	-	5	-	pF

1. Schmitt trigger hysteresis voltage at switching level. Results based on evaluation, not tested in production.
2. At least 100mV.
3. If there is reverse current injection between adjacent pins, leakage current may exceed the maximum value.
4. Pull-up and pull-down resistors are implemented via switchable PMOS/NMOS.
5. VPAD refers to the I/O pin input voltage.

All I/O ports are **CMOS and TTL compatible** (no software configuration required). Their characteristics consider stringent CMOS process or TTL parameters:

Output Drive Current

NSING Technologies Pte. Ltd.
Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

GPIO (General Purpose I/O ports) can sink or source up to ±12mA of current. In user applications, the number of I/O pins must ensure that the drive current does not exceed the absolute maximum ratings defined in Section 4.2:

- The total current drawn from VDD by all I/O ports plus the MCU's maximum operating current must not exceed IVDD (Table 4-2).
- The total current sunk into VSS by all I/O ports plus the MCU's maximum current sourced to VSS must not exceed IVSS (Table 4-2).

Output Voltage

Unless otherwise specified, parameters in Table 4-27 are measured at room temperature (25°C) and under supply voltages per Table 4-4. All I/O ports are CMOS and TTL compatible.

Table 0-27 FT IO Drive Capability Table(1)

Drive Level	I_{OH}, VDD=3.3V	I_{OL}, VDD=3.3V	I_{OH}, VDD=2.5V	I_{OL}, VDD=2.5V	I_{OH}, VDD=1.8V	I_{OL}, VDD=1.8V	Unit
2	2.7	3.3	TBD	TBD	1.4	1.5	mA
4	5.7	6.6	TBD	TBD	3	3.1	mA
8	11.2	13.3	TBD	TBD	6	6.3	mA
12	16.8	19.9	TBD	TBD	9	9.5	mA

1. Guaranteed by design, not tested in production

Table 4-28 TC IO Drive Capability Table(1)

Drive Level	I_{OH}, VDD=3.3V	I_{OL}, VDD=3.3V	I_{OH}, VDD=2.5V	I_{OL}, VDD=2.5V	I_{OH}, VDD=1.8V	I_{OL}, VDD=1.8V	Unit
2	8.1	6.1	3.1	4.5	2.6	3.8	mA
4	16.2	12.2	6.2	9.1	3	3.1	mA
8	28.3	21.4	10.9	16	9.2	13.1	mA
12	44.1	33.5	17.2	25.2	14.5	19.9	mA

1. Guaranteed by design, not tested in production.

Table 4-29 Output Voltage Characteristics(3)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}(1)	Output low level voltage	V_{DD}=3.3V，I_{OL}(4)= 2/4/8/12	VSS	0.4	V
		V_{DD}=2.5V，I_{OL}(4)= 2/4/8/12	VSS	0.4	

NSING Technologies Pte. Ltd.
Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

		V_{DD}=1.8V，I_{OL}[4]= 2/4/8/12	VSS	0.2* V_{DD}	
V_{OH}[2]	Output high level voltage	V_{DD}=3.3V，I_{OH}[4]= 2/4/8/12	2.4	V_{DD}	
		V_{DD}=2.5V，I_{OH}[4]= 2/4/8/12	2	V_{DD}	
		V_{DD}=1.8V，I_{OH}[4]= 2/4/8/12	0.8*V_{DD}	V_{DD}	

1. IIO current drawn by the chip must comply with the absolute maximum ratings in Table 4-2. Total IIO for all I/O and control pins must not exceed IVSS.
2. IIO current output by the chip must comply with absolute maximum ratings. Total IIO must not exceed IVDD.
3. Results based on evaluation, not tested in production.
4. Actual drive capability, see Table 4-25.
5. PC13, PC14, and PC15 are excluded.

Output Buffer Timing Characteristics

Unless otherwise specified, the parameters listed in Tables 4-28 and 4-29 are measured at 25°C and under supply voltages per Table 4-4.

Table 4-30 Output Timing Characteristics (TC IO) [1]

PMODE	Symbol	Parameter	Conditions	Min	Max	Unit
00	Fmax[2]	Maximum Frequency	C=50 pF, 2.7 V≤ V_{DD}≤3.6 V	-	19	MHz
			C=50 pF, 2.3 V≤V_{DD}≤2.7 V	-	10	
			C=30 pF, 2.7 V≤V_{DD}≤3.6 V	-	31	
			C=30 pF, 2.3 V≤V_{DD}≤2.7 V	-	16	
			C=10 pF, 2.7 V≤V_{DD}≤3.6 V	-	84	
			C=10 pF, 2.3 V≤V_{DD}≤2.7 V	-	48	
	t_r/t_f[3]	Fall time from high level to low level and rise time from low level to high level	C=50 pF, 2.7 V≤ V_{DD}≤3.6 V	-	17.9	ns
			C=50 pF, 2.3 V≤V_{DD}≤2.7 V	-	33.5	
			C=30 pF, 2.7 V≤V_{DD}≤3.6 V	-	11	
			C=30 pF, 2.3 V≤V_{DD}≤2.7 V	-	20.6	
			C=10 pF, 2.7 V≤V_{DD}≤3.6 V	-	4.1	
			C=10 pF, 2.3 V≤V_{DD}≤2.7 V	-	7.7	

NSING Technologies Pte. Ltd.
Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

01	Fmax[2]	Maximum frequency	C=50 pF, 2.7 V≤ V_{DD}≤3.6 V	-	51	MHz
			C=50 pF, 2.3 V≤V_{DD}≤2.7 V	-	32	
			C=30 pF, 2.7 V≤V_{DD}≤3.6 V	-	85	
			C=30 pF, 2.3 V≤V_{DD}≤2.7 V	-	45	
			C=10 pF, 2.7 V≤V_{DD}≤3.6 V	-	222	
			C=10 pF, 2.3 V≤V_{DD}≤2.7 V	-	118	
	t_r/t_f[3]	Fall time from high level to low level and rise time from low level to high level	C=50 pF, 2.7 V≤ V_{DD}≤3.6 V	-	6.6	ns
			C=50 pF, 2.3 V≤V_{DD}≤2.7 V	-	9.9	
			C=30 pF, 2.7 V≤V_{DD}≤3.6 V	-	4.1	
			C=30 pF, 2.3 V≤V_{DD}≤2.7 V	-	7.7	
			C=10 pF, 2.7 V≤V_{DD}≤3.6 V	-	1.7	
			C=10 pF, 2.3 V≤V_{DD}≤2.7 V	-	3.1	
10	Fmax[2]	Maximum frequency	C=50 pF, 2.7 V≤V_{DD}≤3.6 V[4]	-	87	MHz
			C=50 pF, 2.3 V≤V_{DD}≤2.7 V[4]	-	46	
			C=30 pF, 2.7 V≤V_{DD}≤3.6 V[4]	-	143	
			C=30 pF, 2.3 V≤V_{DD}≤2.7 V[4]	-	75	
			C=10 pF, 2.7 V≤V_{DD}≤3.6 V[4]	-	339	
			C=10 pF, 2.3 V≤V_{DD}≤2.7 V[4]	-	185	
	t_r/t_f[3]	Fall time from high level to low level and rise time from low level to high level	C=50 pF, 2.7 V≤V_{DD}≤3.6 V[4]	-	3.92	ns
			C=50 pF, 2.3 V≤V_{DD}≤2.7 V[4]	-	7.52	
			C=30 pF, 2.7 V≤V_{DD}≤3.6 V[4]	-	2.41	
			C=30 pF, 2.3 V≤V_{DD}≤2.7 V[4]	-	4.61	
			C=10 pF, 2.7 V≤V_{DD}≤3.6 V[4]	-	1.06	
			C=10 pF, 2.3 V≤V_{DD}≤2.7 V[v]	-	1.98	
11	Fmax[2]	Maximum frequency	C=50 pF, 2.7 V≤V_{DD}≤3.6 V[v]	-	138	MHz
			C=50 pF, 2.3 V≤V_{DD}≤2.7 V[4]	-	69	
			C=30 pF, 2.7 V≤V_{DD}≤3.6 V[v]	-	215	

NSING Technologies Pte. Ltd.
Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

			C=30 pF, 2.3 V≤V_{DD}≤2.7 V[4]	-	122	
			C=10 pF, 2.7 V≤V_{DD}≤3.6 V[4]	-	467	
			C=10 pF, 2.3 V≤V_{DD}≤2.7 V[4]	-	260	
	t_r/t_f[3]	Fall time from high level to low level and rise time from low level to high level.	C=50 pF, 2.7 V≤V_{DD}≤3.6 V[4]	-	2.52	ns
			C=50 pF, 2.3 V≤V_{DD}≤2.7 V[4]	-	5.05	
			C=30 pF, 2.7 V≤V_{DD}≤3.6 V[4]	-	1.6	
			C=30 pF, 2.3 V≤V_{DD}≤2.7 V[4]	-	2.9	
			C=10 pF, 2.7 V≤V_{DD}≤3.6 V[4]	-	0.77	
			C=10 pF, 2.3 V≤V_{DD}≤2.7 V[4]	-	1.385	

1. Design guaranteed.
2. The definition conditions for the maximum frequency are as follows:
   (tr + tf) ≤ 2/3 T
   Skew ≤ 1/20 T
   45% < Duty Cycle < 55%
3. The fall time and rise time are defined respectively as the time between 90% and 10% of the output waveform, and between 10% and 90%.
4. Compensation system enabled.

Table 4-31 Output Timing Characteristics (FT IO) [1]

PMODE	Symbol	Parameter	Conditions	Min	Max	Unit
00 Fast	Fmax[2]	Maximum Frequency	C=50 pF, 2.7 V≤ V_{DD}≤3.6 V	-	13	MHz
			C=50 pF, 2.3 V≤V_{DD}≤2.7 V	-	6	
			C=30 pF, 2.7 V≤V_{DD}≤3.6 V	-	20	
			C=30 pF, 2.3 V≤V_{DD}≤2.7 V	-	10	
			C=10 pF, 2.7 V≤V_{DD}≤3.6 V	-	46	
			C=10 pF, 2.3 V≤V_{DD}≤2.7 V	-	24	
	t_r/t_f[3]	Fall time from high to low and rise time from low to high	C=50 pF, 2.7 V≤ V_{DD}≤3.6 V	-	26.4	ns
			C=50 pF, 2.3 V≤V_{DD}≤2.7 V	-	48.8	
			C=30 pF, 2.7 V≤V_{DD}≤3.6 V	-	17	
			C=30 pF, 2.3 V≤V_{DD}≤2.7 V	-	31.1	

NSING Technologies Pte. Ltd.
Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

			C=10 pF, 2.7 V≤V_{DD}≤3.6 V	-	7.7	
			C=10 pF, 2.3 V≤V_{DD}≤2.7 V	-	13.6	
01 Fast	Fmax(2)	Maximum Frequency	C=50 pF, 2.7 V≤ V_{DD}≤3.6 V	-	26	MHz
			C=50 pF, 2.3 V≤V_{DD}≤2.7 V	-	13	
			C=30 pF, 2.7 V≤V_{DD}≤3.6 V	-	40	
			C=30 pF, 2.3 V≤V_{DD}≤2.7 V	-	21	
			C=10 pF, 2.7 V≤V_{DD}≤3.6 V	-	86	
			C=10 pF, 2.3 V≤V_{DD}≤2.7 V	-	46	
	t_r/t_f(3)	Fall time from high to low and rise time from low to high	C=50 pF, 2.7 V≤ V_{DD}≤3.6 V	-	13.2	ns
			C=50 pF, 2.3 V≤V_{DD}≤2.7 V	-	24.8	
			C=30 pF, 2.7 V≤V_{DD}≤3.6 V	-	8.6	
			C=30 pF, 2.3 V≤V_{DD}≤2.7 V	-	16.1	
			C=10 pF, 2.7 V≤V_{DD}≤3.6 V	-	4	
			C=10 pF, 2.3 V≤V_{DD}≤2.7 V	-	7.3	
10	Fmax(2)	Maximum frequency	C=50 pF, 2.7 V≤V_{DD}≤3.6 V(4)	-	50	MHz
			C=50 pF, 2.3 V≤V_{DD}≤2.7 V(4)	-	36	
			C=30 pF, 2.7 V≤V_{DD}≤3.6 V(4)	-	75	
			C=30 pF, 2.3 V≤V_{DD}≤2.7 V(4)	-	39	
			C=10 pF, 2.7 V≤V_{DD}≤3.6 V(4)	-	151	
			C=10 pF, 2.3 V≤V_{DD}≤2.7 V(4)	-	83	
	t_r/t_f(3)	Fall time from high to low and rise time from low to high	C=50 pF, 2.7 V≤V_{DD}≤3.6 V(4)	-	6.97	ns
			C=50 pF, 2.3 V≤V_{DD}≤2.7 V(4)	-	9.65	
			C=30 pF, 2.7 V≤V_{DD}≤3.6 V(4)	-	4.66	
			C=30 pF, 2.3 V≤V_{DD}≤2.7 V(4)	-	8.4	
			C=10 pF, 2.7 V≤V_{DD}≤3.6 V(4)	-	2.26	
			C=10 pF, 2.3 V≤V_{DD}≤2.7 V(v)	-	4	
11	Fmax(2)	Maximum frequency	C=50 pF, 2.7 V≤V_{DD}≤3.6 V(v)	-	72	MHz

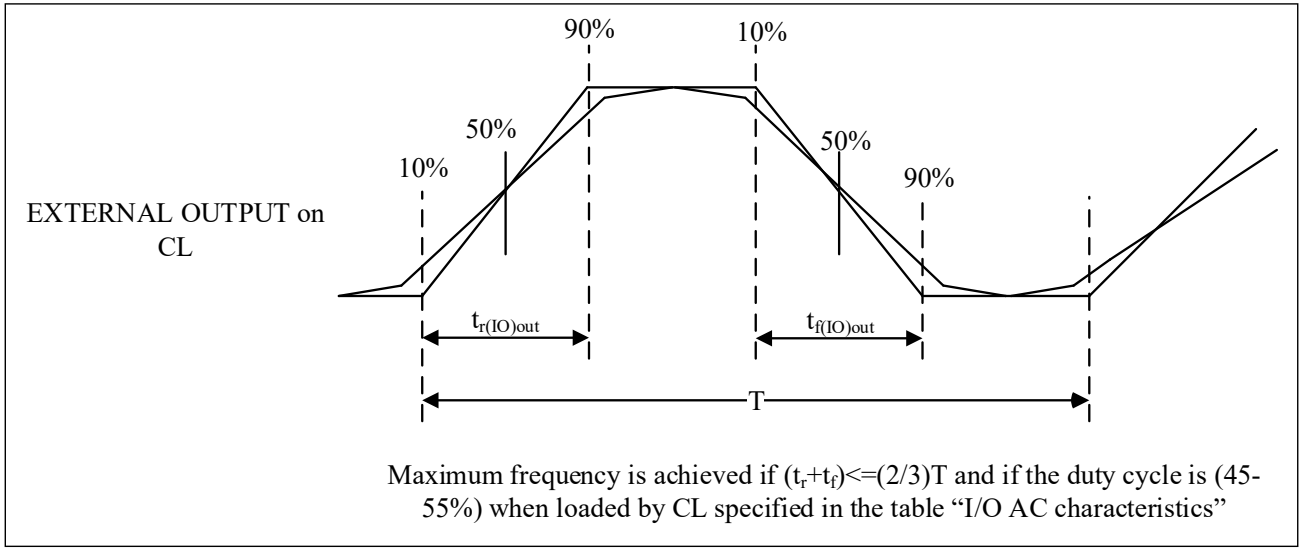
NSING Technologies Pte. Ltd.
Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

Fast			C=50 pF, 2.3 V≤V_{DD}≤2.7 V[4]	-	38	
			C=30 pF, 2.7 V≤V_{DD}≤3.6 V[v]	-	106	
			C=30 pF, 2.3 V≤V_{DD}≤2.7 V[4]	-	56	
			C=10 pF, 2.7 V≤V_{DD}≤3.6 V[4]	-	202	
			C=10 pF, 2.3 V≤V_{DD}≤2.7 V[4]	-	113	
	t_r/t_f[3]	Fall time from high to low and rise time from low to high	C=50 pF, 2.7 V≤V_{DD}≤3.6 V[4]	-	4.82	ns
			C=50 pF, 2.3 V≤V_{DD}≤2.7 V[4]	-	8.9	
			C=30 pF, 2.7 V≤V_{DD}≤3.6 V[4]	-	3.28	
			C=30 pF, 2.3 V≤V_{DD}≤2.7 V[4]	-	5.93	
			C=10 pF, 2.7 V≤V_{DD}≤3.6 V[4]	-	1.65	
			C=10 pF, 2.3 V≤V_{DD}≤2.7 V[4]	-	2.98	

1. Design guarantee.
2. The definition conditions for the maximum frequency are as follows:
   (tr + tf) ≤ 2/3 T
   Skew ≤ 1/20 T
   45% < Duty Cycle < 55%
3. The fall time and rise time are defined as the time between 90% and 10% of the output waveform, and between 10% and 90% of the waveform, respectively.
4. Enable compensation system.

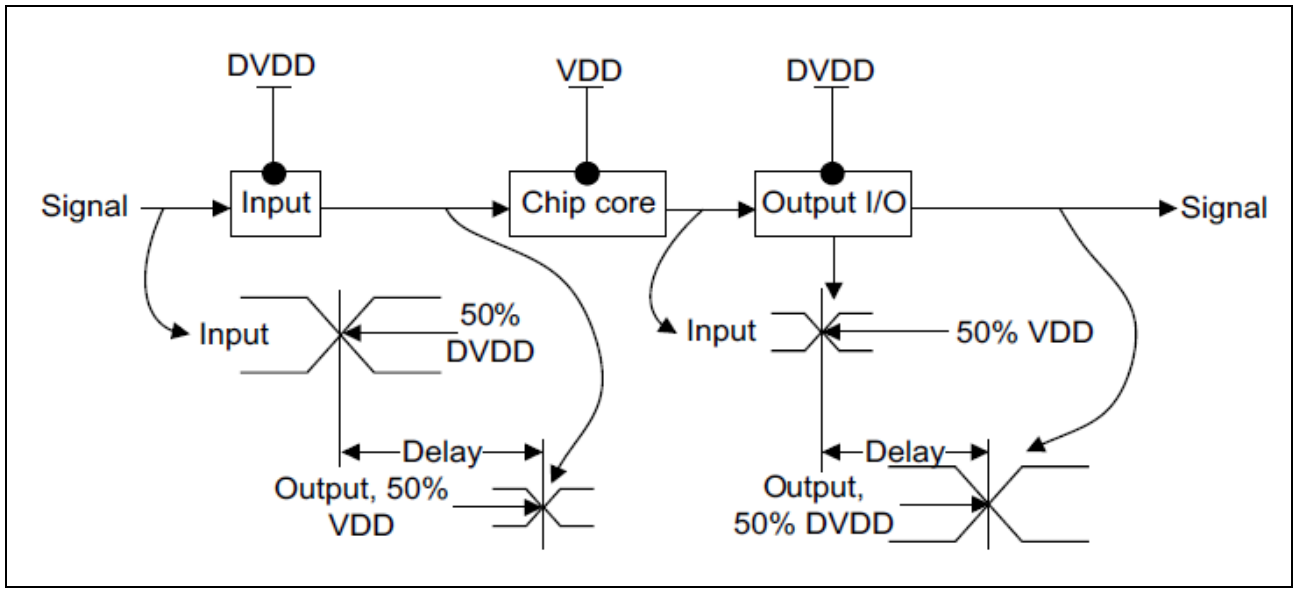
NSING Technologies Pte. Ltd.
Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

Figure 4-11: Definition of Input/Output AC Characteristics



NSING Technologies Pte. Ltd.
Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

Figure 0-12 Transmission Delay



4.3.14 NRST Pin Characteristics

The NRST pin input drive uses CMOS technology, and an internal non-removable pull-up resistor, RPU (see Table 4-30), is integrated. Unless otherwise specified, the parameters listed in Table 4-30 are measured under conditions where the ambient temperature is 25°C, and the supply voltage meets the conditions specified in Table 4-4.

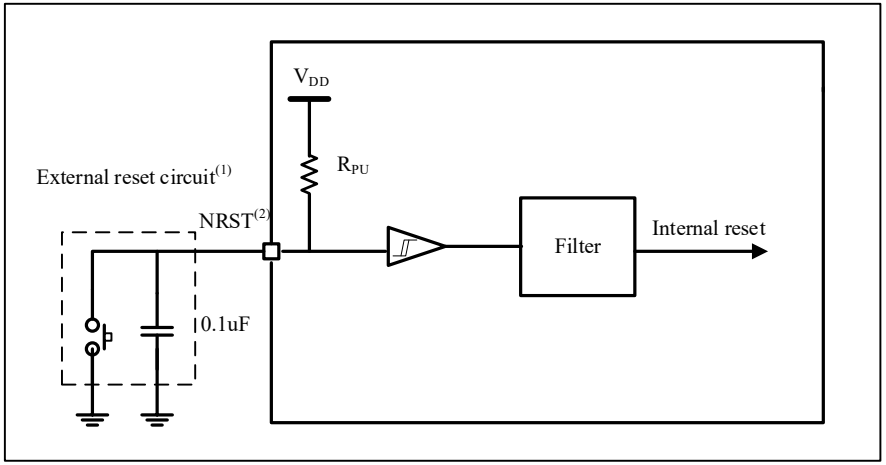
NSING Technologies Pte. Ltd.
Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

Table 4-32 NRST Pin Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$V_{IL(NRST)}$(1)	NRST Input Low Voltage	-	VSS	-	0.3* V_{DD}	V
$V_{IH(NRST)}$(1)	NRST Input High Voltage	-	0.7* V_{DD}	-	V_{DD}	
$V_{hys(NRST)}$	NRST Schmitt Trigger Hysteresis	-	200	-	-	mV
R_{PU}	Weak Pull-up Equivalent Resistance (2)	V_{IN}= V_{SS}	30	50	70	kΩ
$V_{F(NRST)}$(1)	NRST Input Filtered Pulse	VDD=3.3V	-	-	100	ns
$V_{NF(NRST)}$(1)	NRST Input Non-Filtered Pulse	VDD=3.3V	300	-	-	ns

1. Guaranteed by design, not tested during production.
2. The pull-up resistor is designed as a true resistor in series with a switchable PMOS. The resistance of the PMOS/NMOS switch is very small (about 10%).

Figure 4-13: Recommended NRST Pin Protection



1. 滤波作用。
2. 用户必须保证NRST引脚的电位能够低于**Error! Reference source not found.**中列出的最大VIL(NRST)以下，否则MCU不能得到复位。

NSING Technologies Pte. Ltd.
Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

4.3.15 TIM Timer Characteristics

The parameters listed in Tables 4-31, 4-32, 4-33, and 4-34 are guaranteed by design.

For details on the characteristics of input/output multiplexing function pins (output compare, input capture, external clock, PWM output), please refer to section 4.3.12.

Table 4-33: ATIM1/2/3/4 Characteristics (1)

Symbol	Parameter	Condition	Min	Max	Unit
$t_{res(TIM)}$	Timer Resolution Time	-	1	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$= 300MHz	3.33	-	ns
f_{EXT}	External Clock Frequency for CH1 to CH4	-	0	$f_{TIMxCLK}/2$	MHz
		$f_{TIMxCLK}$= 300MHz	0	150	MHz
Res_{TIM}	Timer Resolution	-	-	16	bit
$t_{COUNTER}$	16-bit Counter Clock Cycle (Internal Clock)	-	1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$= 300MHz	0.00333	218	μs
t_{MAX_COUNT}	Maximum Possible Count	-	-	65536x65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$= 300MHz	-	14.3	s

1. Guaranteed by design, not tested during production.

Table 4-34: GTIMA1/2/3/4/5/6/7 Characteristics (1)

Symbol	Parameter	Condition	Min	Max	Unit
$t_{res(TIM)}$	Timer Resolution Time	-	1	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$= 300MHz	3.33	-	ns
f_{EXT}	External Clock Frequency for CH1 to CH4	-	0	$f_{TIMxCLK}/2$	MHz
		$f_{TIMxCLK}$= 300MHz	0	150	MHz
Res_{TIM}	Timer Resolution	-	-	16	bit
$t_{COUNTER}$	16-bit Counter Clock Cycle (Internal Clock)	-	1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$= 300MHz	0.00333	218	μs
t_{MAX_COUNT}	Maximum Possible Count	-	-	65536x65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$= 300MHz	-	14.3	s

NSING Technologies Pte. Ltd.
Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

1. Guaranteed by design, not tested during production.

Table 4-33: GTIMB1/2/3 Characteristics (1)

Symbol	Parameter	Condition	Min	Max	Uint
$t_{res(TIM)}$	Timer Resolution Time	-	1	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$= 300MHz	3.33	-	ns
f_{EXT}	External Clock Frequency for CH1 to CH4	-	0	$f_{TIMxCLK}/2$	MHz
		$f_{TIMxCLK}$= 300MHz	0	150	MHz
ResTIM	External Clock Frequency for CH1 to CH4	-	-	16	bit
$t_{COUNTER}$	16-bit Counter Clock Cycle (Internal Clock)	-	1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$= 300MHz	0.00333	218	μs
t_{MAX_COUNT}	Maximum Possible Count	-	-	65536x65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$= 300MHz	-	14.3	s

1. Guaranteed by design, not tested during production.

Table 4-34: LPTIM1/2/3/4/5 Characteristics (1)

Symbol	Parameter	Condition	Min	Max	Unit
$t_{res(TIM)}$	Timer Resolution Time	-	1	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$= 150MHz	6.67	-	ns
f_{EXT}	External Clock Frequency for CH1 to CH4	-	0	$f_{TIMxCLK}/2$	MHz
		$f_{TIMxCLK}$= 150MHz	0	75	MHz
ResTIM	Timer Resolution	-	-	16	bit
$t_{COUNTER}$	16-bit Counter Clock Cycle (Internal Clock)	-	1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$= 150MHz	0.00667	437	μs
t_{MAX_COUNT}	Maximum Possible Count	-	-	128x65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$= 150MHz	-	55.9	ms

1. Guaranteed by design, not tested during production.

4.3.16 SHRTIM Timer Characteristics

Unless specifically stated, the parameters in Table 4-37 are measured using ambient temperature and supply voltage that comply with the conditions in Table 4-4.

NSING Technologies Pte. Ltd.
Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

Table 4-37 SHRTIM Characteristics(1)

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
TA	Timer ambient temperature range	fSHRTIM = 250 MHz	-40	-	105	°C
fSHRTIM	SHRTIM input clock for PLL calibration	As per TA conditions	-	-	250	MHz
tSHRTIM			4	-	-	ns
tRES(SHRTIM)	High resolution step	fSHRTIM = 250 MHz, TA from -40 to 105°C	-	125	-	ps
ResSHRTIM	Timer resolution		-	-	16	bit
tDTG	Dead time generator clock period		0.125	-	16	tSHRTIM
		fSHRTIM = 250 MHz	0.5	-	64	ns
|tDTR| / |tDTF| max	Dead time range (absolute value)		-	-	511	tDTG
		fSHRTIM = 250 MHz	-	-	34.07	µs
fCHPFRQ	Chopper stage clock frequency		1/256	-	1/16	fSHRTIM
t1STPW	Chopper first pulse length	fSHRTIM = 250 MHz	0.976 16	- -	15.625 256	MHz tSHRTIM
		fSHRTIM = 250 MHz	0.064	-	1.024	µs

NSING Technologies Pte. Ltd.
Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

1. Data based on characterization results, not tested in production.

Table 4-38 SHRTIM Output Response to Fault Protection(1)

Symbol	Parameter	Condition	Minimum	Typical	Maximum(2)	Unit
tLAT(DF)	Digital fault response delay	Propagation delay from SHRTIM_FALTINx digital input to SHRTIM_CHxy output pin	-	9	12	ns
TW(FALT)	Minimum fault pulse width		8	-	-	
tLAT(AF)	Analog fault response delay	Propagation delay from comparator COMPx_INP input pin to SHRTIM_CHxy output pin	-	22	38	

1. Refer to the fault protection paragraph in the SHRTIM chapter of the user manual.
2. Data based on characterization results, not tested in production.

Table 4-39 SHRTIM Output Response to External Events 1 to 10 (Low Latency Mode(1))

Symbol	Parameter	Condition	Minimum	Typical(2)	Maximum(2)	Unit
tLAT(DEEV)	Digital external event response delay	Propagation delay from SHRTIM_EXEVx digital input to SHRTIM_CHxy output pin (30pF load)	-	11	17	ns
TW(EEV)	Minimum external event pulse width		8	-	-	
tLAT(AEEV)	Analog external event response delay	Propagation delay from comparator COMPx_INP input pin to SHRTIM_CHxy output pin (30pF load)	-	24	42	

1. Refer to the external event delay paragraph in the SHRTIM chapter of the user manual.
2. Data based on characterization results, not tested in production.

NSING Technologies Pte. Ltd.
Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

Table 4-40 SHRTIM Output Response to External Events 1 to 10 (Synchronous Mode(1))

Symbol	Parameter	Condition	Minimum	Typical	Maximum(2)	Unit
tLAT(DEEV)	Digital external event response delay	Propagation delay from SHRTIM_EXEVx digital input pin to SHRTIM_CHxy output pin (30pF load)(3)	-	47	51	ns
tLAT(AEEV)	Analog external event response delay	Propagation delay from COMPx_INP input pin to SHRTIM_CHxy output pin (30pF load)(3)	-	58	71	ns
tW(EEV)	Minimum external event pulse width		8	-	-	ns
TJIT(EEV)	External event response jitter	Delay jitter from SHRTIM_EXEVx digital input or COMPx_INP to SHRTIM_CHxy output pin	-	-	1	tSHRTIM(4)

1. Refer to the external event delay paragraph in the SHRTIM section of the user manual.
2. Data based on characterization results, not tested in production.
3. This parameter is given at fSHRTIM = 250 MHz.
4. tSHRTIM = 1 / fSHRTIM, fSHRTIM = 250 MHz.

Table 4-41 SHRTIM Synchronization Input/Output(1)

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
tW(SYNCIN)	Minimum pulse width for synchronization input (including SHRTIM_SCIN)		1	-	-	tSHRTIM
tRES(ESR)	Response time to external synchronization request		-	-	3	tSHRTIM

NSING Technologies Pte. Ltd.
Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
tW(SYNCOUT)	Pulse width of SHRTIM_SCOUT output		-	16	-	tSHRTIM
		fSHRTIM=250 MHz	-	64	-	ns

1. Guaranteed by design, not tested in production.

NSING Technologies Pte. Ltd.
Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

4.3.28 4.3.17 SDRAM Characteristics

Figure 4-14: SDRAM Read Timing Diagram

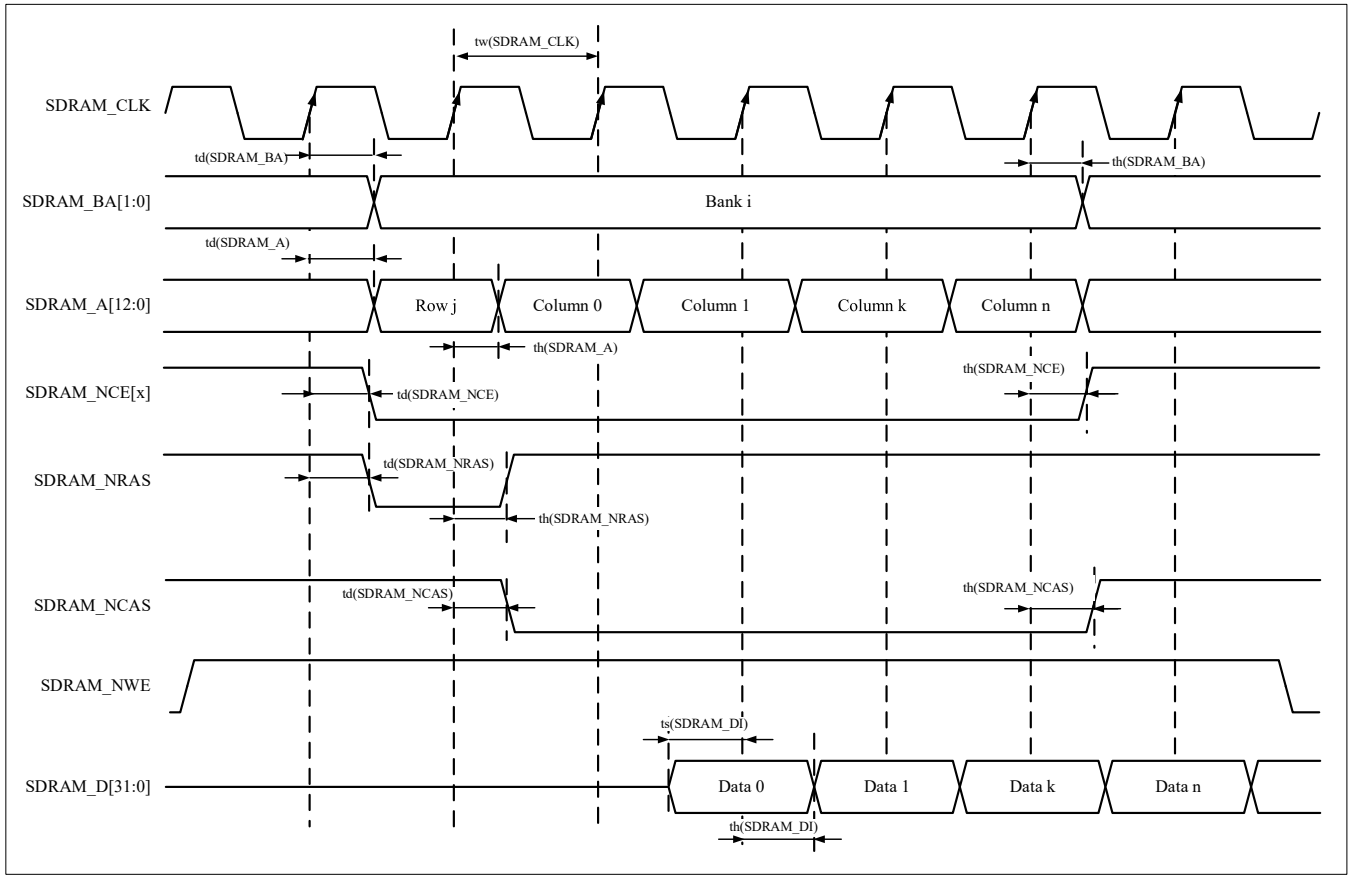


Table 4-42 SDRAM Read Timing (1)

Symbol	Parameter	Min	Max	Unit
t_w(SDRAM_CLK)	SDRAM_CLK Period	7.51(133M)	-	ns
t_d(SDRAM_BA)	Bank Address Valid Time	-	4.0	
t_h(SDRAM_BA)	Bank Address Hold Time	2.0	-	

NSING Technologies Pte. Ltd.
Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

t_d(SDRAM_A)	Address (Row/Column) Valid Time	-	4.0	
t_h(SDRAM_A)	Address (Row/Column) Hold Time	2.0	-	
t_d(SDRAM_NCE)	Chip Select Valid Time	-	4.0	
t_h(SDRAM_NCE)	Chip Select Hold Time	2.0	-	
t_d(SDRAM_NRAS)	SDRAM_NRAS Valid Time	-	4.0	
t_h(SDRAM_NRAS)	SDRAM_NRAS Hold Time	2.0	-	
t_d(SDRAM_NCAS)	SDRAM_NCAS Valid Time	-	4.0	
t_h(SDRAM_NCAS)	SDRAM_NCAS Hold Time	2.0	-	
t_s(SDRAM_DI)	Data Input Setup Time	1.2	-	
t_h(SDRAM_DI)	Data Input Hold Time	1.5	-	

NSING Technologies Pte. Ltd.
Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

Figure 4-15: SDRAM Write Timing Diagram

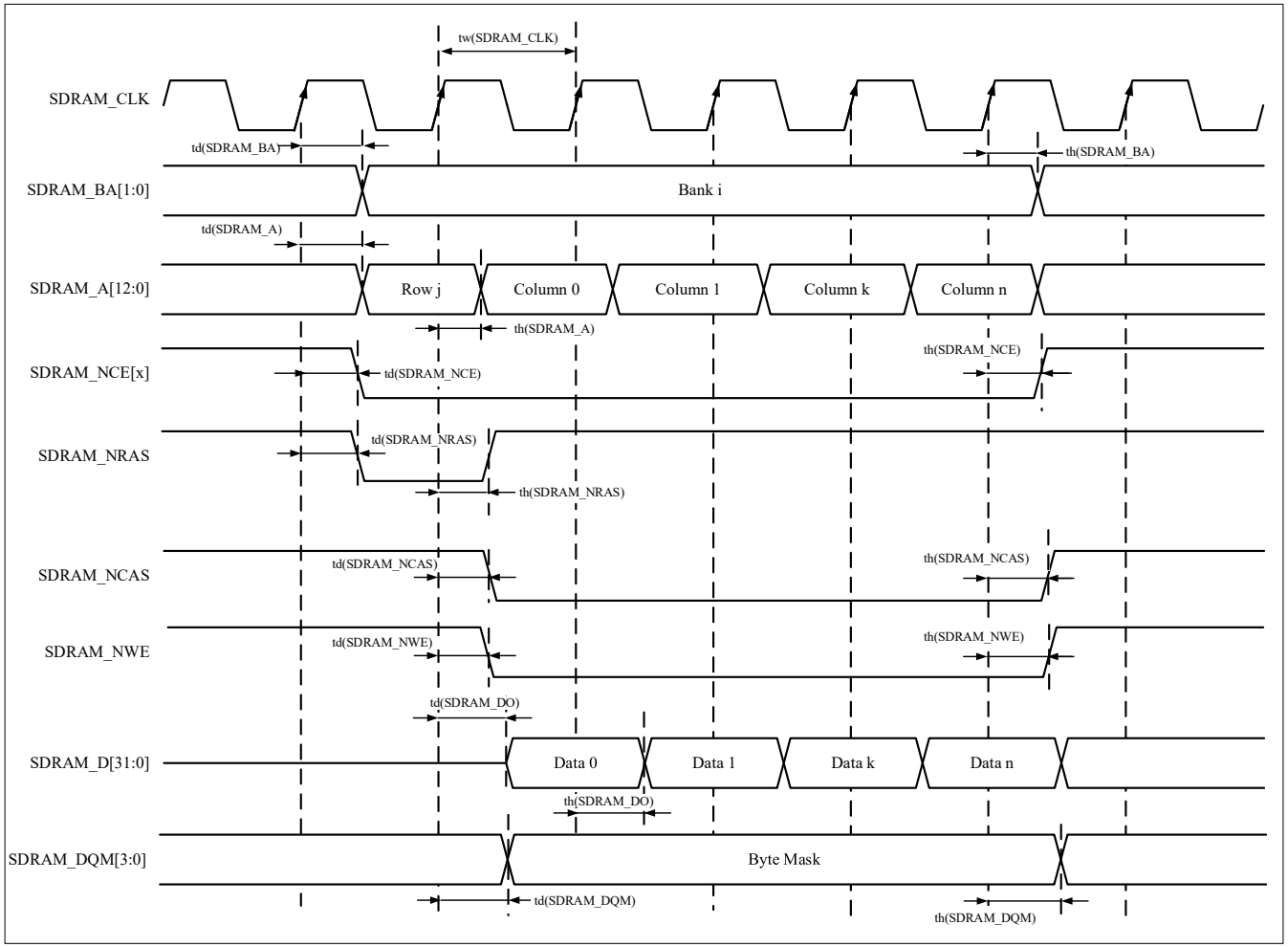


Table 4-43 SDRAM Write Timing (1)

Symbol	Parameter	Min	Max	Unit
t_w(SDRAM_CLK)	SDRAM_CLK Period	7.51(133M)	-	ns
t_d(SDRAM_BA)	Bank Address Hold Time	-	4.0	

NSING Technologies Pte. Ltd.
Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

t_h(SDRAM_BA)	Bank Address Hold Time	2.0	-	
t_d(SDRAM_A)	Address (Row/Column) Hold Time	-	4.0	
t_h(SDRAM_A)	Address (Row/Column) Hold Time	2.0	-	
t_d(SDRAM_NCE)	Chip Select Hold Time	-	4.0	
t_h(SDRAM_NCE)	Chip Select Hold Time	2.0	-	
t_d(SDRAM_NRAS)	SDRAM_NRAS Hold Time	-	4.0	
t_h(SDRAM_NRAS)	SDRAM_NRAS Hold Time	2.0	-	
t_d(SDRAM_NCAS)	SDRAM_NCAS Hold Time	-	4.0	
t_h(SDRAM_NCAS)	SDRAM_NCAS Hold Time	2.0	-	
t_d(SDRAM_NWE)	Write Enable Hold Time	-	4.0	
t_h(SDRAM_NWE)	Write Enable Hold Time	2.0	-	
t_d(SDRAM_DO)	Data Output Hold Time	7.51(133M)	-	
t_h(SDRAM_DO)	Data Output Hold Time	-	4.0	
t_d(SDRAM_DQM)	Output Byte Mask Hold Time	2.0	-	
t_h(SDRAM_DQM)	Output Byte Mask Hold Time	-	4.0	

4.3.29 4.3.18 Watchdog Features

Table 4-44 IWDG Maximum and Minimum Count Reset Times (LSI = 32 KHz)

Prescaler	PD[2:0]	Minimum Duration RL[11:0]=0	Maximum Duration RL[11:0]=0xFFF	Unit
/4	000	0.125	512	ms
/8	001	0.25	1024	
/16	010	0.5	2048	
/32	011	1.0	4096	
/64	100	2.0	8192	

NSING Technologies Pte. Ltd.
Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

/128	101	4.0	16384	
/256	11x	8.0	32768	

1. Guaranteed by design, not tested in production.

Table 4-45 WWDG Maximum and Minimum Count Reset Times (PCLK1 = 150MHz)

Prescaler	TIMERB[1:0]	Minimum Timeout	Maximum Timeout	Unit
/1	0	0.02728	445.54	ms
/2	1	0.05456	891.07	
/4	2	0.1088	1782.14	
/8	3	0.2184	3564.29	

1. Guaranteed by design, not tested in production.

4.3.30 4.3.19 I2C Interface Features

Unless specified otherwise, the parameters listed in **Table 4-46** are measured with environmental temperature, fPCLK1 frequency, and VDD supply voltage meeting the conditions in **Table 4-4**.

This product's I2C interface complies with the standard I2C communication protocol, but with the following limitations: SDA and SCL are not "true" open-drain pins. When configured for open-drain output, the PMOS transistor between the pin and VDD is turned off, but still exists.

For detailed characteristics of I2C pins (SDA and SCL) and input/output multiplexing features, refer to section 4.3.12.

NSING Technologies Pte. Ltd.
Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

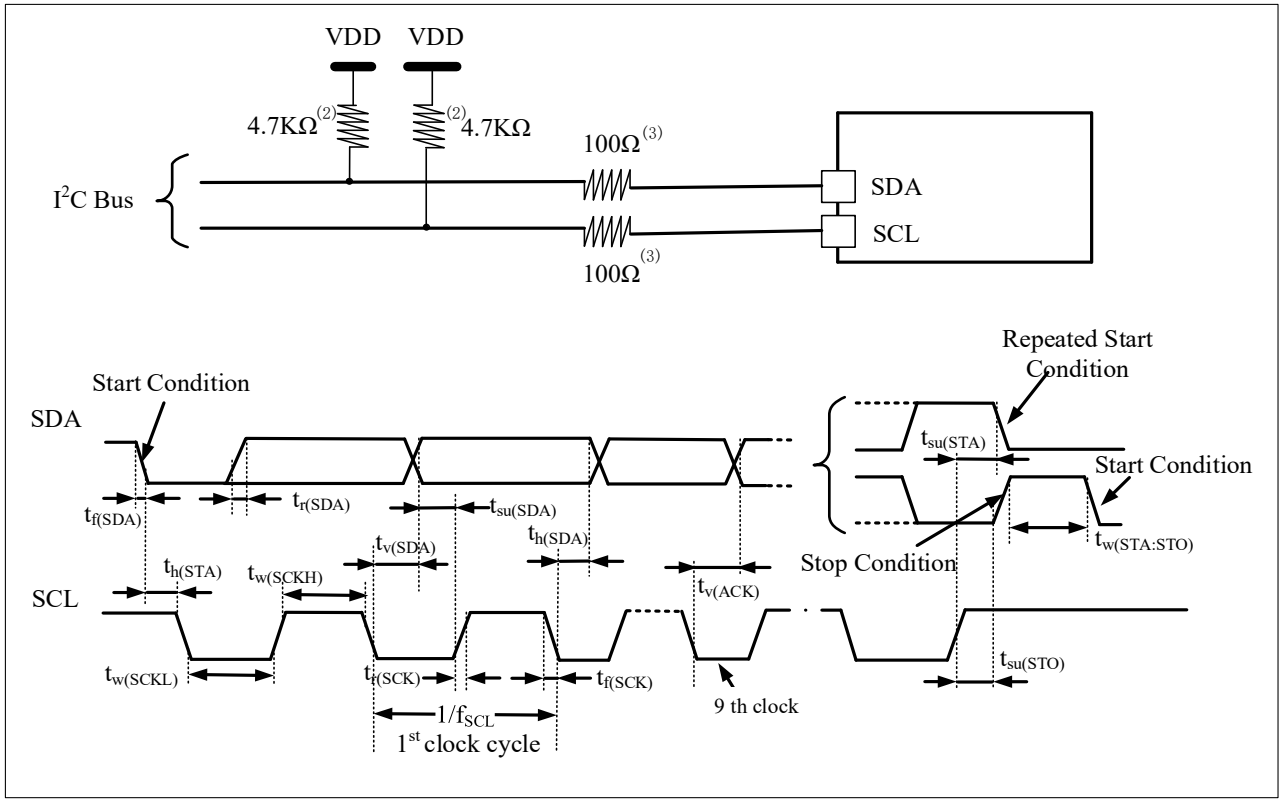
Table 4-46 I2C Interface Features ([1]

Symbol	Parameter	Standard Mode		Fast Mode		Fast+Mode		High-speed mode		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
f_{SCL}	I2C Interface Frequency	0.0	100	0	400	0	1000	0	3400	KHz
$t_{h(STA)}$	Start Condition Hold Time	4.0	-	0.6	-	0.26	-	0.16	-	μs
$t_{w(SCLL)}$	SCL Clock Low Time	4.7	-	1.3	-	0.5	-	0.16	-	μs
$t_{w(SCLH)}$	SCL Clock High Time	4.0	-	0.6	-	0.26	-	0.06	-	μs
$t_{su(STA)}$	Repeated Start Condition Setup Time	4.7	-	0.6	-	0.26	-	0.16	-	μs
$t_{h(SDA)}$	SDA Data Hold Time	0	-	0	-	0	-	0	-	μs
$t_{su(SDA)}$	SDA Setup Time	250.0	-	100	-	50	-	10	-	ns
$t_{r(SDA)}$ $t_{r(SCL)}$	SC, SDA Rise Time	-	1000	20	300	-	120	10	SCL=40 SDA=80	ns
$t_{f(SDA)}$ $t_{f(SCL)}$	SCL, SDA Fall Time	-	300	-	300	-	120	10	SCL=40 SDA=80	ns
$t_{su(STO)}$	Stop Condition Setup Time	4.0	-	0.6	-	0.26	-	0.16	-	μs
$t_{w(STO:STA)}$	Stop Condition to Start Condition Time (Bus Idle)	4.7	-	1.3	-	0.5	-		-	μs
Cb	Capacitive Load per Bus	-	400	-	400	-	400		400	pf
$t_{v(SDA)}$	Data Valid Time	-	3.45	-	0.9	-	0.45		0.1	μs
$t_{v\ (ACK)}$	Acknowledge Valid Time	-	3.45	-	0.9	-	0.45		0.1	μs
t_{SP}	Input Filter Spike Pulse Width Suppression	0	Analog filter: 35ns. Digital filter: up to 15 I2CCLK period	0	Analog filter: 35ns. Digital filter: up to 15 I2CCLK period	0	Analog filter: 35ns. Digital filter: up to 15 I2CCLK period	0	Analog filter: 35ns. Digital filter: up to 15 I2CCLK period	ns

1. Guaranteed by design, not tested in production.

NSING Technologies Pte. Ltd.
Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

Figure 4-16 I2C Bus AC Waveform and Measurement Circuit (1)



1. 测量点设置于CMOS电平：$0.3V_{DD}$和$0.7V_{DD}$。
2. 上拉电阻阻值取决于I2C接口速度。
3. 电阻值取决于实际电气特性，可以不连接串行电阻，信号线直连。

4.3.31 4.3.20 SPI/I2S Interface Characteristics

Unless otherwise specified, the SPI parameters listed in Table 4-47 and the I2S parameters listed in Table 4-41 are measured at ambient temperature (25°C), fPCLKx frequency, and VDD supply voltage meeting the conditions in Table 4-4.

NSING Technologies Pte. Ltd.
Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

For details on the characteristics of input/output multiplexed function pins (NSS, SCLK, MOSI, MISO for SPI; WS, CLK, SD for I2S), refer to Section 4.3.12 (IO Port Characteristics).

Table 4-47 SPI Characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCK}	SPI clock frequency	Master mode 2.3<VDD<3.6 V SPI1, 2, 3	-	-	80	MHz
		Master mode 2.7<VDD<3.6 V SPI1, 2, 3	-	-	100	
		Master mode 2.3<VDD<3.6 V SPI4, 5, 6	-	-	50	
		Slave receive 2.3<VDD<3.6 V	-	-	100	
		Slave transmit mode/full 2.7<VDD<3.6 V	-	-	31	
		Slave transmit mode/full 2.3 <VDD<3.6 V			29	
$t_{su(NSS)}$(1)	NSS setup time	Slave mode	2	-	-	-
$t_{h(NSS)}$ (1)	NSS hold time	Slave mode	1	-	-	
$t_{w(SCKH)}$ (1) $t_{w(SCKL)}$ (1)	SCK high and low time	Master mode	T_{pclk}-2	T_{pclk}	T_{pclk}+2	
$t_{su(MI)}$ (1)	Data input setup time	Master mode	1	-	-	ns
$t_{su(SI)}$ (1)		Slave mode	1	-	-	
$t_{h(MI)}$ (1)	Data input hold time	Master mode	4	-	-	
$t_{h(SI)}$ (1)		Slave mode	2	-	-	
$t_{a(SO)}$ (1) (2)	Data output access time	Slave mode	9	13	27	

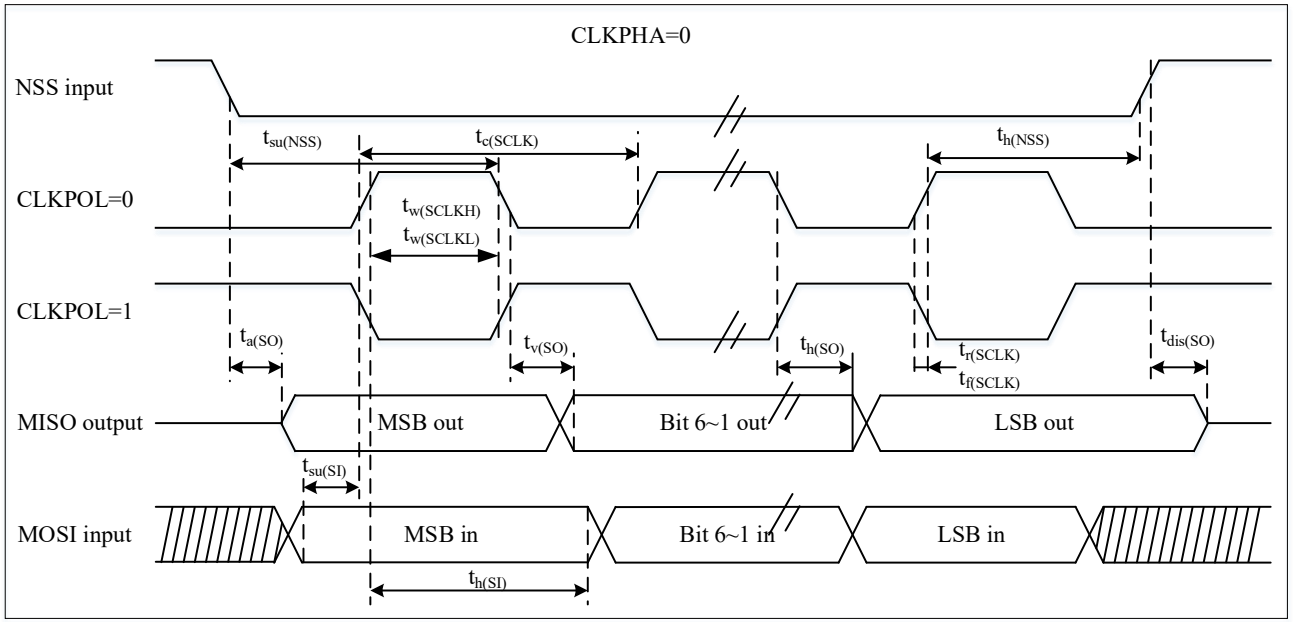
NSING Technologies Pte. Ltd.
Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

$t_{dis(SO)}$ (1) (3)	Data output disable time	Slave mode	0	1	5	
$t_{v(SO)}$ (1)	Data output valid time	Slave mode 2.7<VDD<3.6 V	-	12.5	16	
$t_{v(MO)}$ (1)		Slave mode 2.3<VDD<3.6 V	-	12.5	17	
		Master mode	-	1	3	
$t_{h(SO)}$ (1)	Data output hold time	Slave mode 2.3<VDD<3.6 V	10	-	-	
$t_{h(MO)}$ (1)		Master mode	0	-	-	

1. Guaranteed by design, not tested in production.
2. Minimum value indicates the minimum time to drive the output, maximum value indicates the maximum time to correctly acquire the data.
3. Minimum value indicates the minimum time to turn off the output, maximum value indicates the maximum time to place the data line in high impedance state.

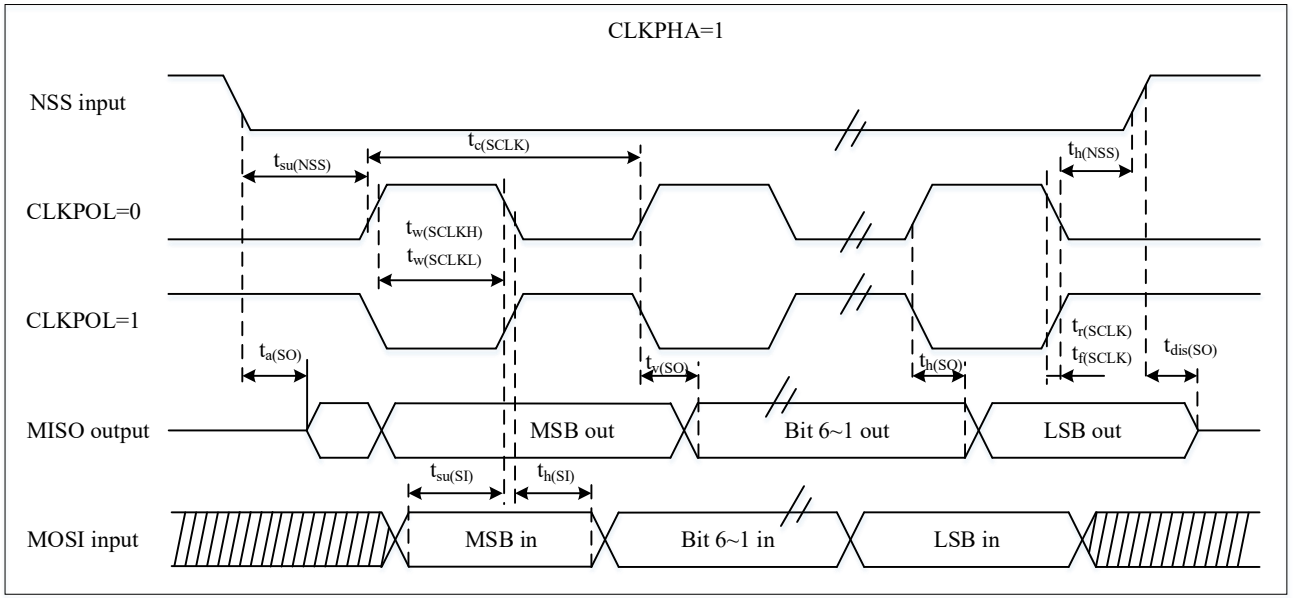
NSING Technologies Pte. Ltd.
Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

Figure 4-17 SPI Timing Diagram - Slave Mode and CLKPHA=0



NSING Technologies Pte. Ltd.
Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

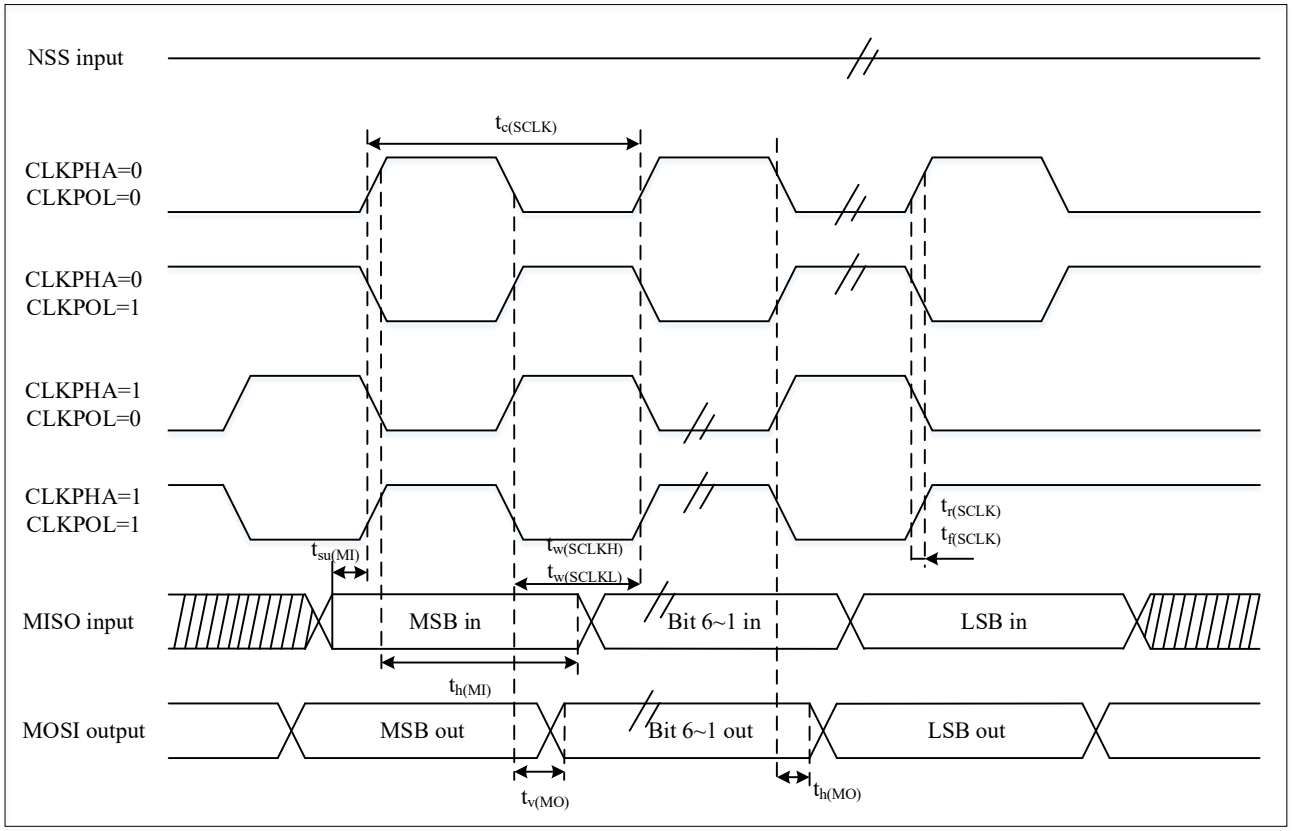
Figure 4-17 SPI Timing Diagram — Slave Mode and CLKPHA=1 (1)



1. Guaranteed by design, not tested in production.

NSING Technologies Pte. Ltd.
Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

Figure 4-18 SPI Timing Diagram — Master Mode (1)



Note: Measurement points are set at 0.5VDD, with external load capacitance (CL) of 30pF.

NSING Technologies Pte. Ltd.
Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

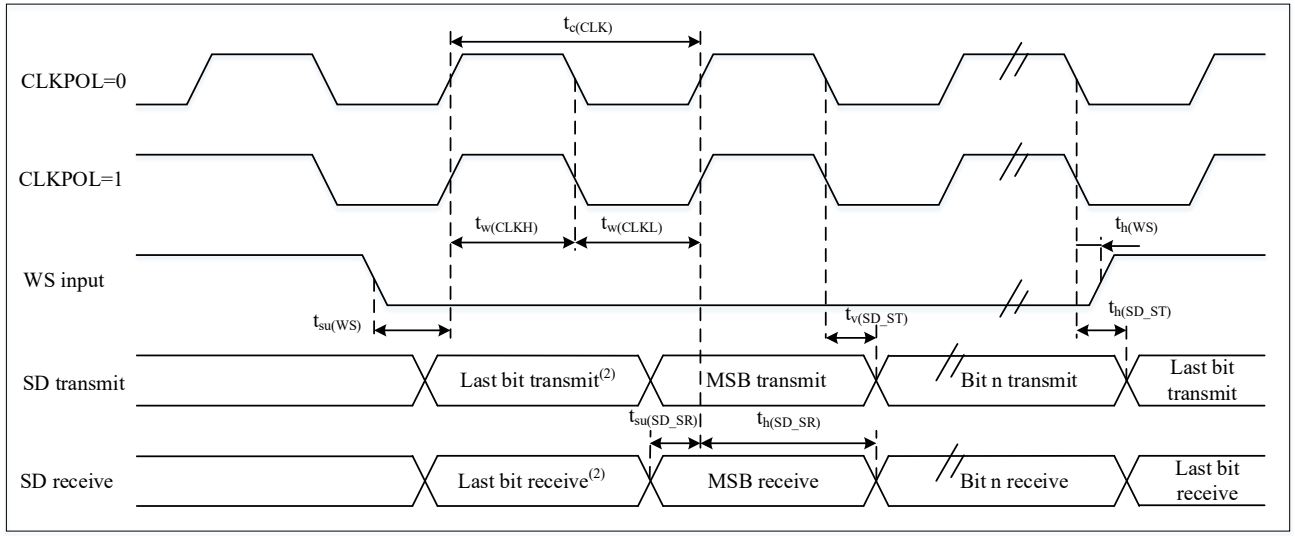
Table 4-48 I2S Characteristics (1)

Symbol	Parameter	Conditions		Min	Max	Unit
f_{MCLK}	I^2S master clock frequency	Master mode		256x8K	256Fs(3)	MHz
f_{CLK} $1/t_{c(CLK)}$	I^2S clock frequency	Master mode (32bit)		-	64Fs(3)	
		Slave mode (32bit)		-	64Fs(3)	
DuCy(SCK)	I2S slave input clock duty cycle	I2S slave mode		30	70	%
$t_{v(WS)}$ (1)	WS valid time	Master mode	I2S2	-	6	
			I2S3	-	6	
$t_{h(WS)}$(1)	WS hold time	Master mode	I2S2	2	-	
			I2S3	2		
$t_{su(WS)}$ (1)	WS setup time	Slave mode	I2S2	7	-	
			I2S3	7	-	
$t_{h(WS)}$(1)	WS hold time	Slave mode	I2S2	0	-	
			I2S3	0	-	
$t_{w(CLKH)}$(1)	CLK high and low time	-		312.5	-	
$t_{w(CLKL)}$(1)				345	-	
$t_{su(SD\_MR)}$(1)	Data input setup time	Master receiver	I2S2	6	-	
			I2S3	6	-	
$t_{su(SD\_SR)}$(1)		Slave receiver	I2S2	7	-	
			I2S3	7	-	
$t_{h(SD\_MR)}$(1)(2)	Data output hold time	Master receiver	I2S2	0	-	
			I2S3	0		
$t_{h(SD\_SR)}$(1)(2)		Slave receiver	I2S2	1	-	
			I2S3	1		
$t_{v(SD\_ST)}$(1)(2)	Data output valid time	Slave transmitter (after enable edge)	I^2S2	-	15	
			I^2S3	-	15	
$t_{h(SD\_ST)}$(1)	Data output hold time	Slave transmitter (after enable edge)	I^2S2	4	-	
			I^2S3	4	-	
$t_{v(SD\_MT)}$(1)(2)	Data output valid time	Master transmitter (after enable edge)	I2S2	-	6	
			I2S3	-	6	
$t_{h(SD\_MT)}$(1)	Data output hold time	Master transmitter (after enable edge)	I2S2	0	-	
			I2S3	0	-	

Notes:
1. *Guaranteed by design, not tested in production.*
2. *Dependent on fPCLK.*
3. *Audio sampling frequency.*

NSING Technologies Pte. Ltd.
Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

Figure 4-20 I2S Slave Mode Timing Diagram (Philips Protocol) (1)

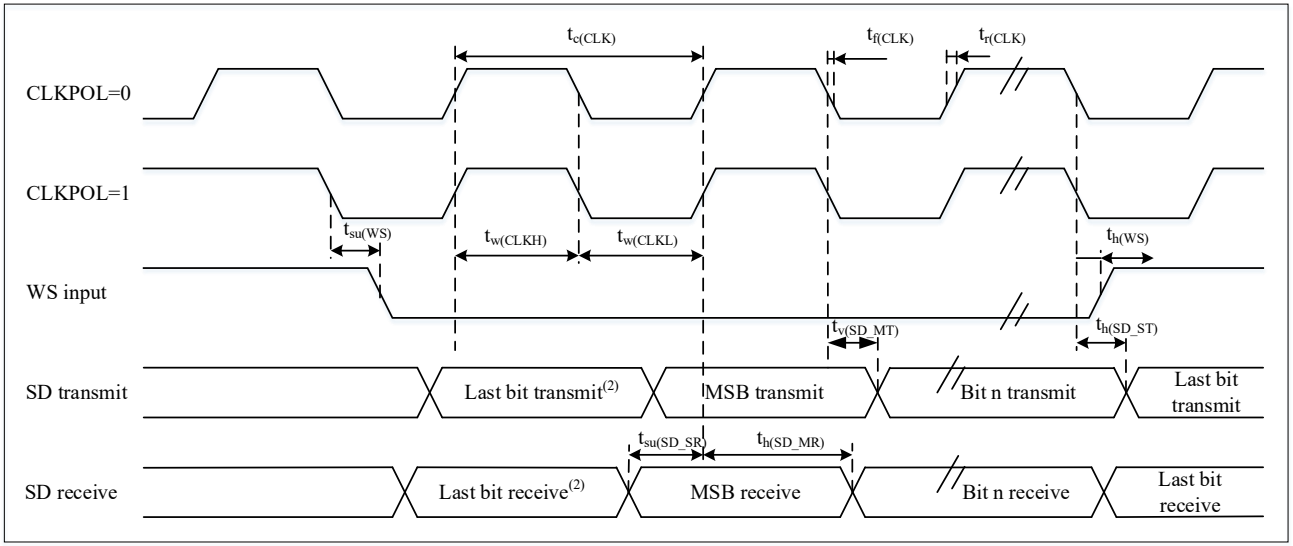


Notes:

1. *Measurement points are set at 0.3VDD and 0.7VDD.*
2. *The least significant bit of the previous byte is transmitted/received. There is no transmission/reception of this least significant bit before the first byte.*

NSING Technologies Pte. Ltd.
Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

Figure 4-21 I2S Master Mode Timing Diagram (Philips Protocol) (1)



Notes:

1. *Measurement points are set at 0.3VDD and 0.7VDD.*
2. *The least significant bit of the previous byte is transmitted/received. There is no transmission/reception of this least significant bit before the first byte.*

4.3.32 4.3.21 xSPI Interface Characteristics

Table 4-49 xSPI Characteristics in SDR Mode(1)(2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$F_{(CLK)}$	QSPI clock frequency	2.3V < V_{DD} < 3.6 V, VOS0, C_{LOAD} = 15 pF	-	-	92	MHz
		2.3 V < V_{DD} < 3.6 V, VOS0, C_{LOAD} =20 pF	-	-	90	
		2.7 V < V_{DD} < 3.6 V, VOS0, C_{LOAD} = 20 pF	-	133	140	
$t_{w(CKH)}$	QSPI clock high/low time,	PRESCALER[7:0] = n	$t_{(CK)}/2$	-	$t_{(CK)}/2+1$	ns

NSING Technologies Pte. Ltd.
Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

$t_{w(CKL)}$	even division	= 0,1,3,5	$t_{(CK)}/2–1$	-	$t_{(CK)}/2$	
$t_{w(CKH)}$	QSPI clock high/low time, odd division	PRESCALER[7:0] = n = 2,4,6,8	$(n/2)*t_{(CK)}/ (n+1)$	-	$(n/2)*t_{(CK)}/ (n+1)+1$	
$t_{w(CKL)}$			$(n/2+1)*t_{(CK)}/ (n+1)–1$	-	$(n/2+1)*t_{(CK)}/(n+1)$	
$t_{s(IN)}$	Input data setup time	-	3	-	-	
$t_{h(IN)}$	Input data hold time	-	1.5	-	-	
$t_{v(OUT)}$	Output data valid time	-	-	0.5	1	
$t_{h(OUT)}$	Output data hold time	-	0	-	-	

Notes:

1. *All values apply to both eight-line and four-line SPI modes.*
2. *Guaranteed by design, not tested in production.*

Figure 4-22 xSPI Read/Write Timing in SDR Mode

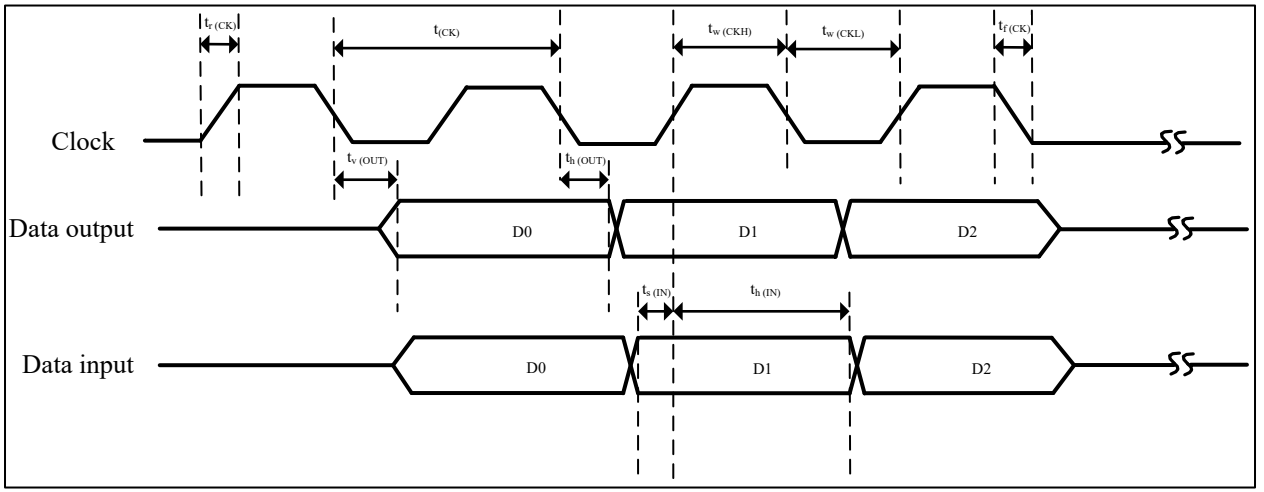


Table 4-50 xSPI Characteristics in DTR Mode (non-DQS)(1)(2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F_{CK}	xSPI clock frequency	2.3V < VDD < 3.6 V, VOS0, CLOAD = 15 pF	-	-	90	MHz

NSING Technologies Pte. Ltd.
Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

		2.3V < VDD < 3.6 V, VOS0, CLOAD = 20 pF	-	-	87	
		2.7 V < VDD < 3.6 V, VOS0, CLOAD = 20 pF	-	-	110	
$t_{w(CKH)}$	QSPI clock high/low time, even division	TBD	$t_{(CK)}/2$	-	$t_{(CK)}/2+1$	ns
$t_{w(CKL)}$			$t_{(CK)}/2–1$	-	$t_{(CK)}/2$	
$t_{w(CKH)}$	QSPI clock high/low time, odd division	TBD	$(n/2)*t_{(CK)}/ (n+1)$	-	$(n/2)*t_{(CK)}/ (n+1)+1$	
$t_{w(CKL)}$			$(n/2+1)*t_{(CK)}/ (n+1)–1$	-	$(n/2+1)*t_{(CK)}/(n+1)$	
$t_{sr(IN)}$ $t_{sf(IN)}$	Input data setup time	-	3.0	-	-	
$t_{hr(IN)}$ $t_{hf(IN)}$	Input data hold time	-	1.50	-	-	
$t_{vr(OUT)}$ $t_{vf(OUT)}$	Output data valid time	TBD	-	6	7	
		TBD	-	$t_{pclk}/4+ 1$	$t_{pclk}/4+1.25$	
$t_{hr(OUT)}$ $t_{hf(OUT)}$	Output data valid time	TBD	4.5	-	-	
		TBD	$t_{pclk}/4$	-	-	

Notes:

3. All values apply to both eight-line and four-line SPI modes.
4. Guaranteed by design, not tested in production.

NSING Technologies Pte. Ltd.
Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

Figure 4-23 xSPI Timing in DTR Mode

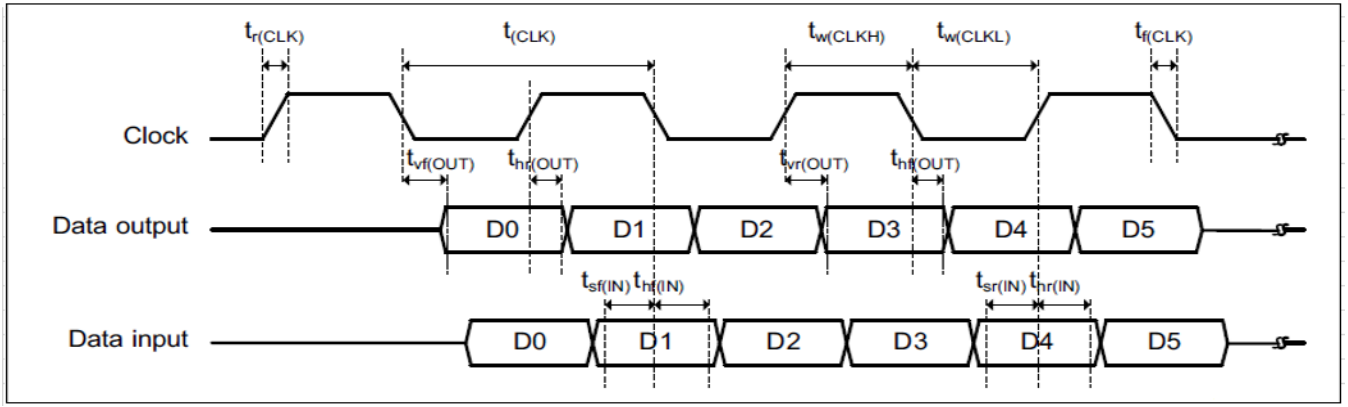


Table 4-51 xSPI Characteristics in DTR Mode (with DQS)/Eight-line and Hyperbus Protocol (1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F_{CK}(2)(3)	xSPI clock frequency	2,7 V < V_{DD} < 3.6 V, VOS0, C_{LOAD} = 20 pF	-	-	**100**	MHz
		2.3V < V_{DD} < 3.6 V, VOS0, C_{LOAD} = 20 pF	-	-	**100**	
$t_{w(CKH)}$	QSPI clock high/low time, even division	TBD	$t_{(CK)}$/2	-	$t_{(CK)}$/2+1	ns
$t_{w(CKL)}$			$t_{(CK)}$/2–1	-	$t_{(CK)}$/2	
$t_{w(CKH)}$	QSPI clock high/low time, odd division	TBD	(n/2)*$t_{(CK)}$/ (n+1)	-	(n/2)*$t_{(CK)}$/ (n+1)+1	ns
$t_{w(CKL)}$			(n/2+1)*$t_{(CK)}$/ (n+1)–1	-	(n/2+1)*$t_{(CK)}$/(n+1)	
$t_{v(CK)}$	Clock valid time	-	-	-	$t_{(CK)}$+1	
$t_{h(CK)}$	Clock hold time	-	$t_{(CK)}$/2	-	-	
$V_{ODr(CK)}$	CKrising edge, CK and $\overline{ck}$ *crossing level*	VDD = 2.3 V	922	-	1229	mV
$V_{ODf(CK)}$	CK falling edge, CK and $\overline{ck}$ crossing level	VDD = 2.3 V	1000	-	1277	
$t_{w(CS)}$	Chip select high level time	-	3 * $t_{(CK)}$	-	-	ns

NSING Technologies Pte. Ltd.
Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

$t_{v(DQ)}$	Input datavalid data	-	0	-	-	
$t_{v(DS)}$	Input datastrobevalid data	-	0	-	-	
$t_{h(DS)}$	Input datastrobehold time	-	0	-	-	
$t_{v(RWDQ)}$	Output data strobevalid data	-	-	-	3 x $t_{(CK)}$	
$t_{sr(DQ)}$	Input data setup time	Rising edge	0	-	-	
$t_{sf(DQ)}$		Falling edge	0	-	-	
$t_{hr(DQ)}$	Input data hold time	Rising edge	1	-	-	
$t_{hf(DQ)}$		Falling edge	1	-	-	
$t_{vr(OUT)}$	Output data Rising edgevalid data	TBD	-	6	7	
		TBD	-	t_{pclk}/4+ 1	t_{pclk}/4+1.25	
$t_{vf(OUT)}$	Output data Falling edgevalid data	TBD	-	5.5	6	
		TBD	-	t_{pclk}/4+ 0.5	t_{pclk}/4+0.75	
$t_{hr(OUT)}$	Output data Rising edgehold time	TBD	4.5	-	-	
		TBD	t_{pclk}/4	-	-	
$t_{hf(OUT)}$	Output data Falling edgehold time	TBD	4.5	-	-	
		TBD	t_{pclk}/4	-	-	

Notes:

1. *Guaranteed by design, not tested in production.*
2. *The maximum deviation for the maximum frequency values given from RWDS to DQ is +/-1.0ns*
3. *To achieve this frequency, the corresponding register must be activated.*

NSING Technologies Pte. Ltd.
Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

Figure 4-24 xSPI Hyperbus Clock Timing Diagram0-2 xSPI Hyperbus

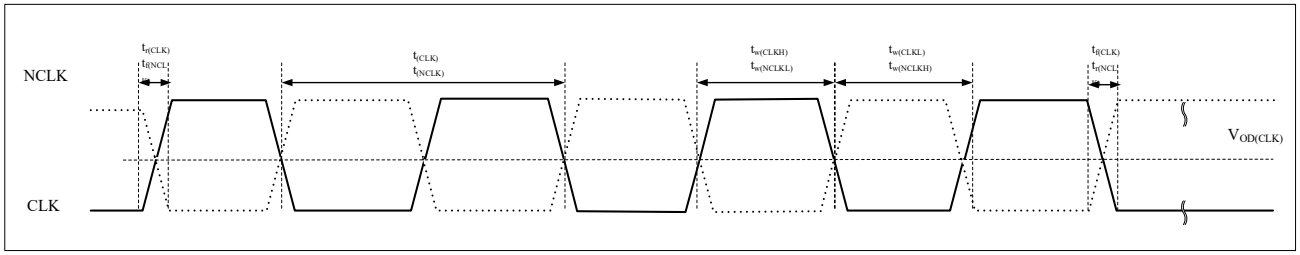
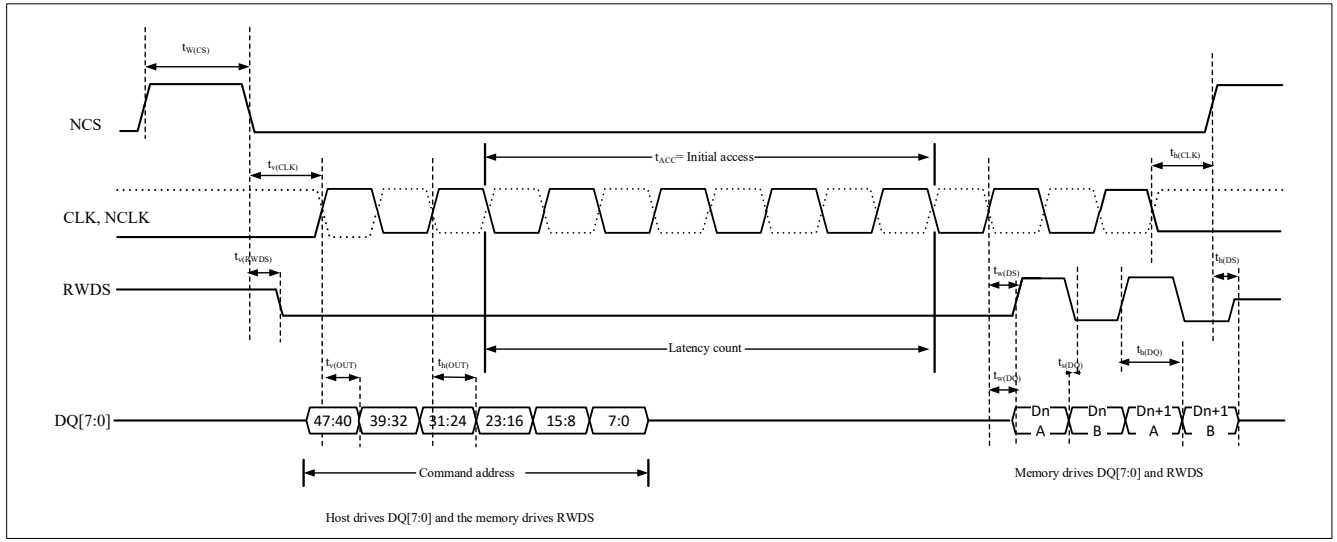
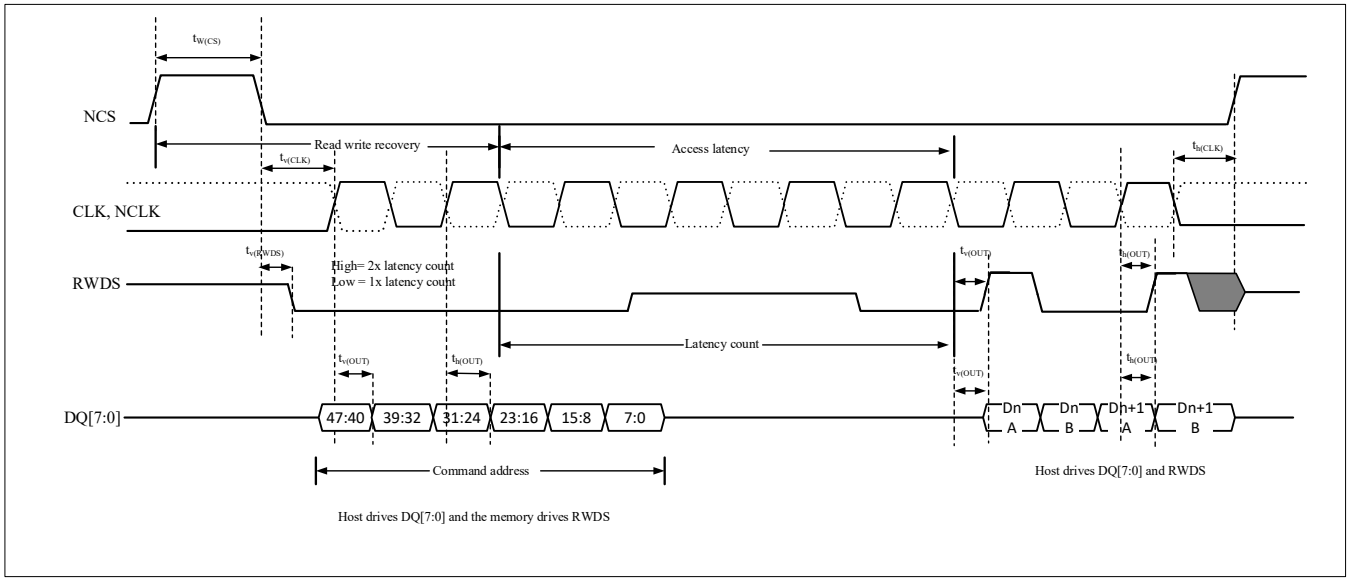


Figure 4-25 xSPI Hyperbus Clock Read Timing Diagram0-3 xSPI Hyperbus



NSING Technologies Pte. Ltd.
Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

Figure 4-26 xSPI Hyperbus Clock Write Timing Diagram0-4 xSPI Hyperbus



4.3.33 4.3.22 FEMC Characteristics

- Asynchronous Waveforms and Timing

Figures 4-26 to 4-29 show the asynchronous waveforms, and Tables 4-45 to 4-48 provide the corresponding timing parameters.

NSING Technologies Pte. Ltd.
Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

Figure 4-27 Asynchronous Non-Multiplexed Bus SRAM/PSRAM/NOR Read Operation Waveform

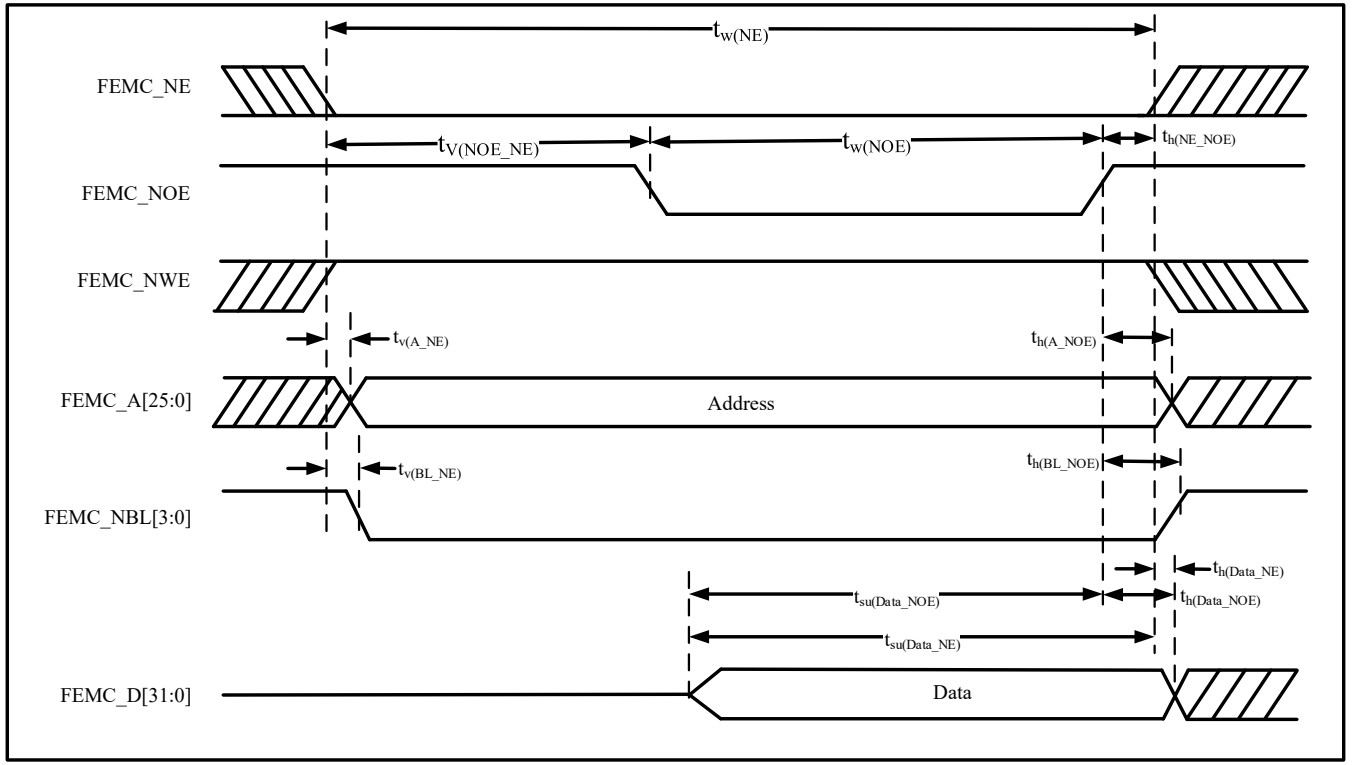


Table 4-52 Asynchronous Non-Multiplexed Bus SRAM/PSRAM/NOR Read Operation Timing (1)(2)

Symbol	Parameter	Min(3)	Max(3)	Unit
$t_{w(NE)}$	FEMC_NE low time	TBD	TBD	ns
$t_{v(NOE\_NE)}$	FEMC_Nex low to FEMC_NOElow	TBD	TBD	ns
$t_{w(NOE)}$	FEMC_NOE low time	TBD	TBD	ns
$t_{h(NE\_NOE)}$	FEMC_NOE high to FEMC_NE high hold time	TBD	TBD	ns
$t_{v(A\_NE)}$	FEMC_Nex low to FEMC_A valid	TBD	TBD	ns
$t_{h(A\_NOE)}$	Address hold time after FEMC_NOE high	TBD	TBD	ns
$t_{v(BL\_NE)}$	FEMC_NEx low to FEMC_NBL valid	TBD	TBD	ns

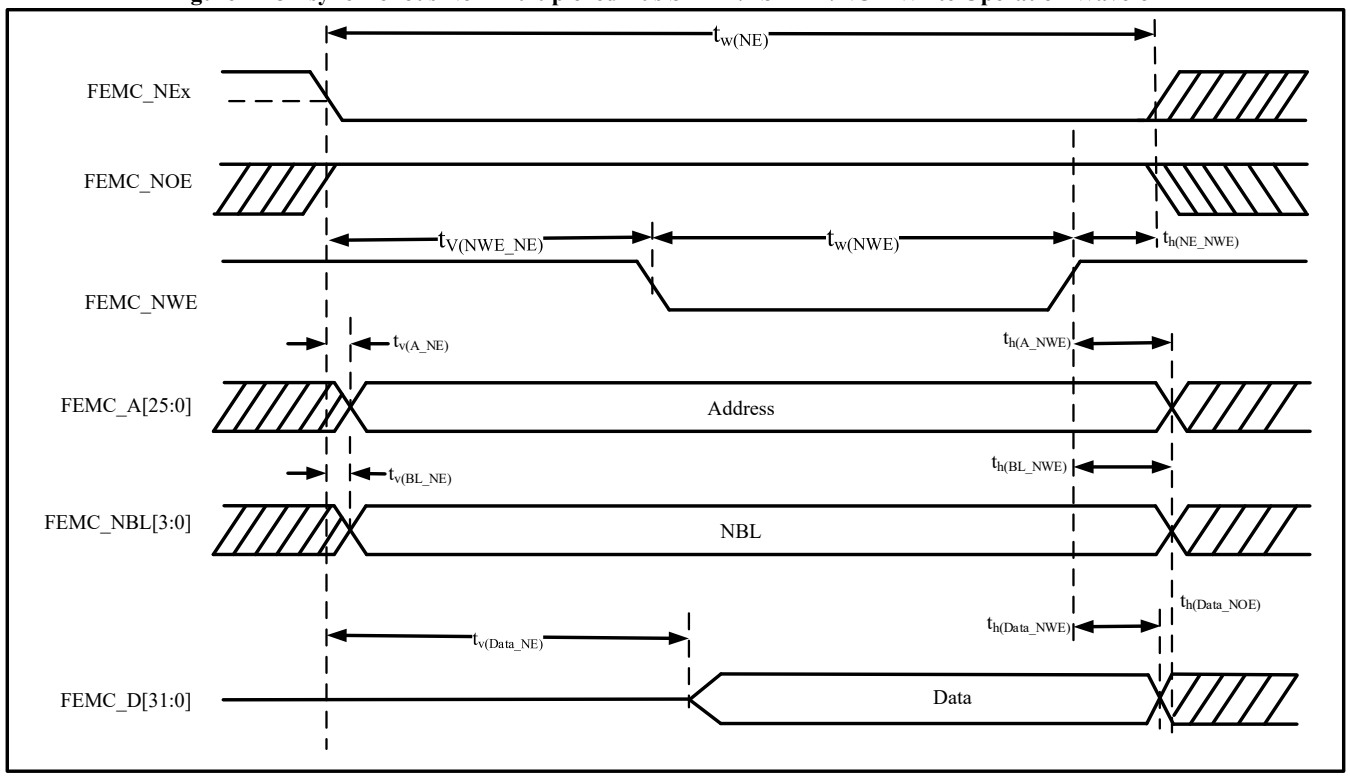
NSING Technologies Pte. Ltd.
Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

$t_{h(BL\_NOE)}$	FEMC_NBL hold time after FEMC_NOE high	TBD	TBD	ns
$t_{su(Data\_NE)}$	Data setup time to FEMC_NEx high	TBD	TBD	ns
$t_{su(Data\_NOE)}$	Data setup time to FEMC_NOEx high	TBD	TBD	ns
$t_{h(Data\_NOE)}$	Data hold time after FEMC_NOE high	TBD	TBD	ns
$t_{h(Data\_NE)}$	Data hold time after FEMC_NEx high	TBD	TBD	ns

Notes:

1. *IO drive strength = 8 mA, capacitive load = 30 pF*
2. *Measurement point set at CMOS level: 0.5 VDD*
3. *tHCLK ≥ 1 / 240 MHz*

Figure 4-28 Asynchronous Non-Multiplexed Bus SRAM/PSRAM/NOR Write Operation Waveform



NSING Technologies Pte. Ltd.
Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

Table 4-53 Asynchronous Non-Multiplexed Bus SRAM/PSRAM/NOR Write Operation Timing [1][2]

Symbol	Parameter	Min[3]	Max[3]	Unit
$t_{w(NE)}$	FEMC_NE low time	TBD	TBD	ns
$t_{v(NWE\_NE)}$	FEMC_NEx low to FEMC_NWE low	TBD	TBD	ns
$t_{w(NWE)}$	FEMC_NWE low time	TBD	TBD	ns
$t_{h(NE\_NWE)}$	Hold time from FEMC_NWE high to FEMC_NE high	TBD	TBD	ns
$t_{v(A\_NE)}$	FEMC_NEx low to FEMC_A valid	TBD	TBD	ns
$t_{h(A\_NWE)}$	Address hold time after FEMC_NWE high	TBD	TBD	ns
$t_{v(BL\_NE)}$	FEMC_NEx low to FEMC_NBL valid	TBD	TBD	ns
$t_{h(BL\_NWE)}$	FEMC_NBL hold time after FEMC_NWE high	TBD	TBD	ns
$t_{v(Data\_NE)}$	FEMC_NEx low to data valid	TBD	TBD	ns
$t_{h(Data\_NWE)}$	Data hold time after FEMC_NWE high	TBD	TBD	ns

Notes:

1. *IO drive strength = 8 mA, capacitive load = 30 pF*
2. *Measurement point set at CMOS level: 0.5 VDD*
3. *tHCLK ≥ 1 / 240 MHz*

NSING Technologies Pte. Ltd.
Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

Figure 4-29 Asynchronous bus multiplexing PSRAM/NOR read operation waveform

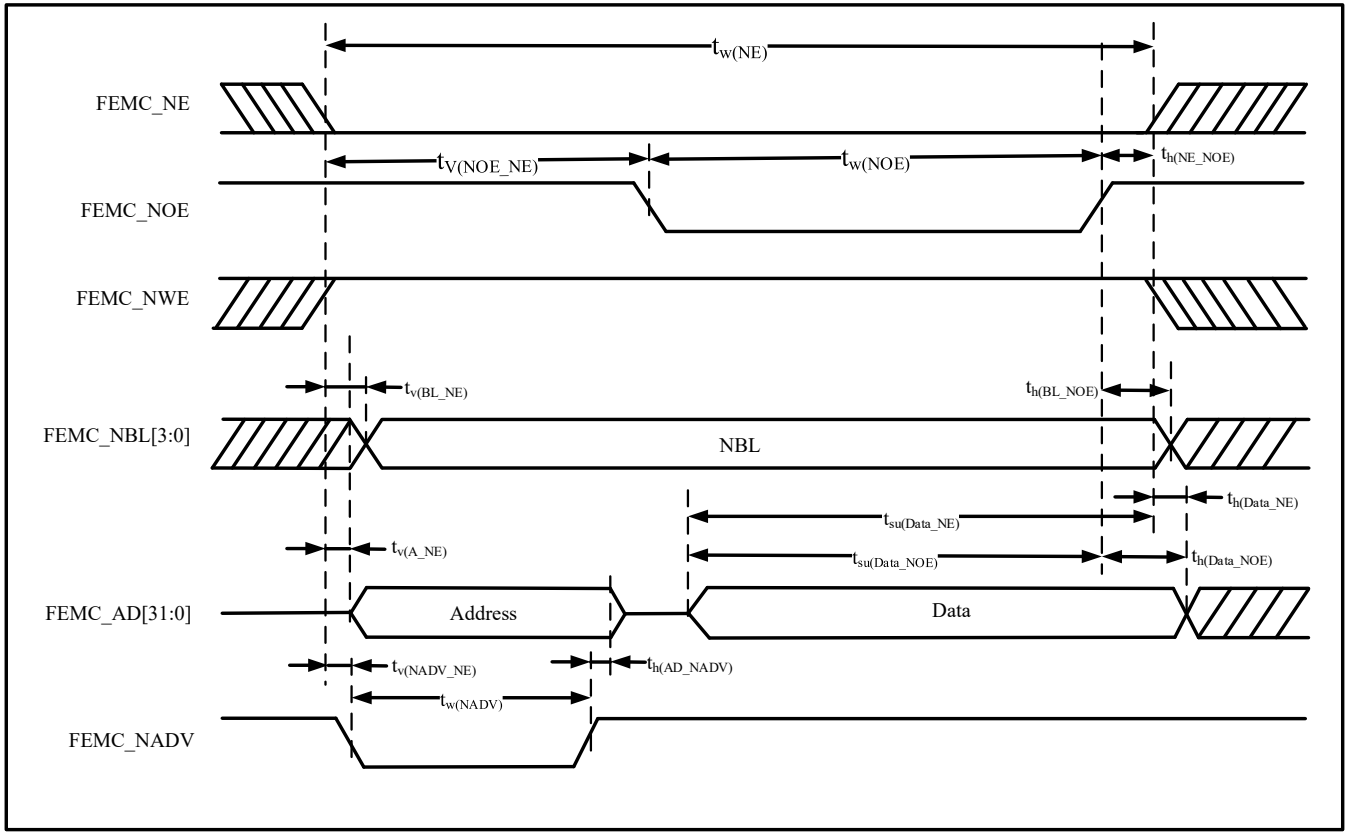


Table 4-54 Asynchronous Bus-Multiplexed PSRAM/NOR Read Operation Timing (1)(2)

Symbol	Parameter	Min(3)	Max(3)	Unit
$t_{w(NE)}$	FEMC_NE Low Time	TBD	TBD	ns
$t_{v(NOE\_NE)}$	FEMC_NEx Low to FEMC_NOE Low	TBD	TBD	ns
$t_{w(NOE)}$	FEMC_NOE Low Time	TBD	TBD	ns
$t_{h(NE\_NOE)}$	Hold Time from FEMC_NOE High to FEMC_NE High	TBD	TBD	ns
$t_{v(A\_NE)}$	FEMC_NEx Low to FEMC_A Valid	TBD	TBD	ns

NSING Technologies Pte. Ltd.
Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

$t_{v(NADV\_NE)}$	FEMC_NEx Low to FEMC_NADV Low	TBD	TBD	ns
$t_{w(NADV)}$	FEMC_NADV Low Time	TBD	TBD	ns
$t_{h(AD\_NADV)}$	Hold Time of FEMC_AD (Address) after FEMC_NADV High	TBD	TBD	ns
$t_{h(A\_NOE)}$	Address Hold Time after FEMC_NOE High	TBD	TBD	ns
$t_{h(BL\_NOE)}$	FEMC_NBL Hold Time after FEMC_NOE High	TBD	TBD	ns
$t_{v(BL\_NE)}$	FEMC_NEx Low to FEMC_NBL Valid	TBD	TBD	ns
$t_{su(Data\_NE)}$	Data Setup Time before FEMC_NEx High	TBD	TBD	ns
$t_{su(Data\_NOE)}$	Data Setup Time before FEMC_NOE High	TBD	TBD	ns
$t_{h(Data\_NE)}$	Data Hold Time after FEMC_NEx High	TBD	TBD	ns
$t_{h(Data\_NOE)}$	Data Hold Time after FEMC_NOE High	TBD	TBD	ns

Notes:

1. *IO drive strength: 8mA, Capacitive load = 30 pF*
2. *Measurement point set at CMOS level: 0.5 × VDD*
3. *tHCLK ≥ 1/240MHz*

NSING Technologies Pte. Ltd.
Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

Figure 4-30 Asynchronous Bus-Multiplexed PSRAM/NOR Write Operation Waveform

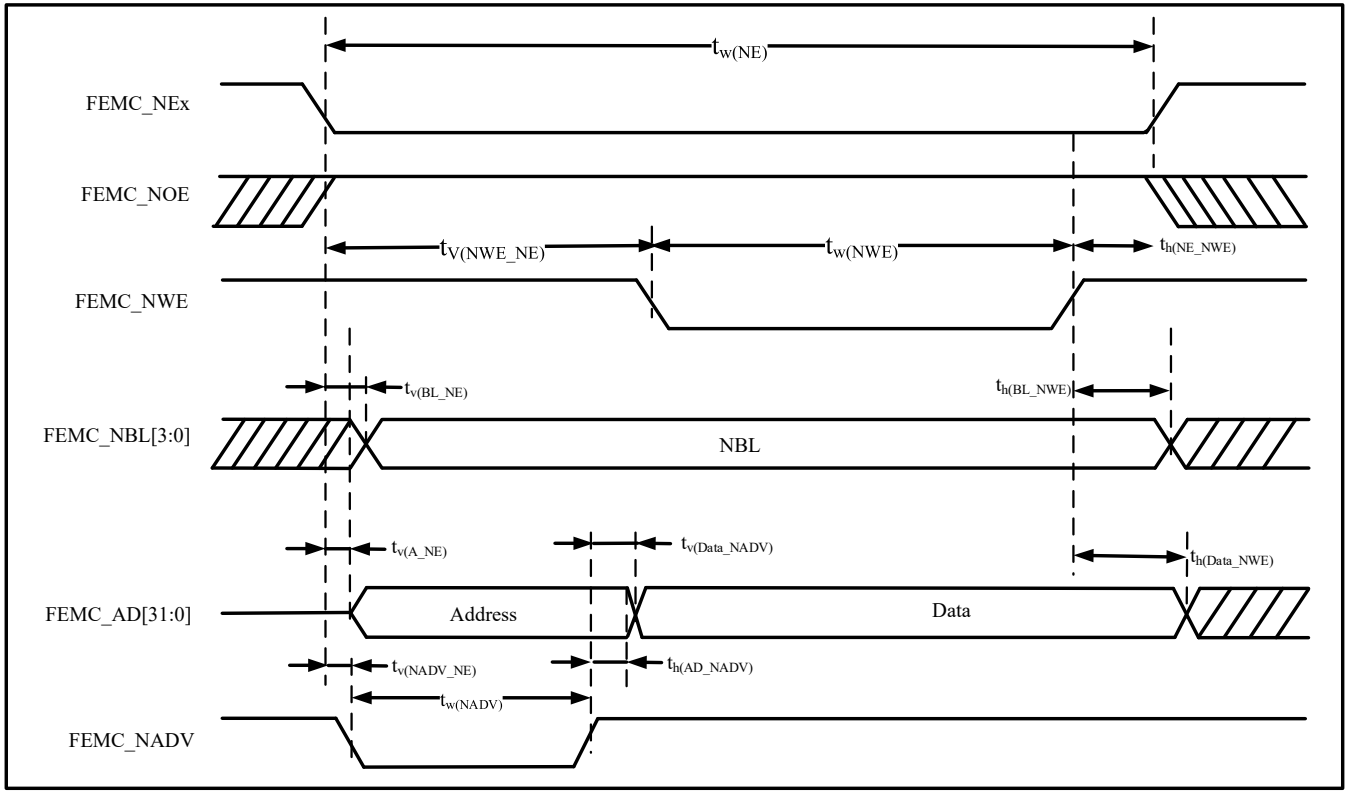


Table 4-55 Asynchronous Bus-Multiplexed PSRAM/NOR Read Operation Timing (1)(2)

Symbol	Parameter	Min(3)	Max(3)	Unit
$t_{w(NE)}$	FEMC_NE low time	TBD	TBD	ns
$t_{v(NWE\_NE)}$	FEMC_NEx low to FEMC_NOE low	TBD	TBD	ns
$t_{w(NWE)}$	FEMC_NOE low time	TBD	TBD	ns
$t_{h(NE\_NWE)}$	Hold time from FEMC_NOE high to FEMC_NE high	TBD	TBD	ns
$t_{v(A\_NE)}$	FEMC_NEx low to FEMC_A valid	TBD	TBD	ns
$t_{v(NADV\_NE)}$	Hold time of FEMC_AD (address) valid after FEMC_NADV high	TBD	TBD	ns

NSING Technologies Pte. Ltd.
Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

$t_{w(NADV)}$	Address hold time after FEMC_NOE high	TBD	TBD	ns
$t_{h(AD\_NADV)}$	FEMC_NBL hold time after FEMC_NOE high	TBD	TBD	ns
$t_{h(A\_NWE)}$	FEMC_NEx low to FEMC_NBL valid	TBD	TBD	ns
$t_{v(BL\_NE)}$	Data setup time to FEMC_NEx high	TBD	TBD	ns
$t_{h(BL\_NWE)}$	Data setup time to FEMC_NOE high	TBD	TBD	ns
$t_{v(Data\_NADV)}$	Data hold time after FEMC_NEx high	TBD	TBD	ns
$t_{h(Data\_NWE)}$	Data hold time after FEMC_NOE high	TBD	TBD	ns

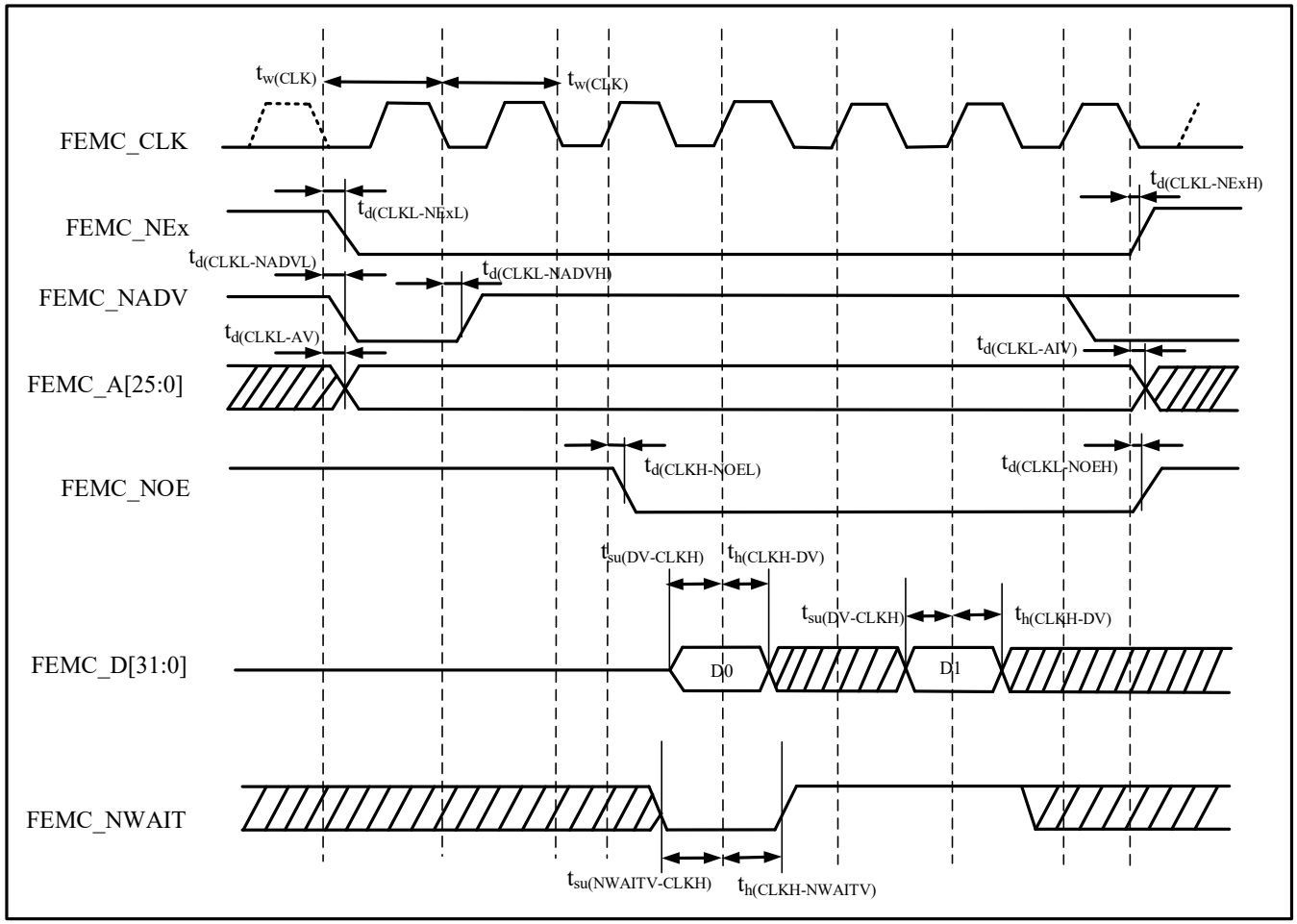
Notes:

1. *IO drive strength = 8 mA, capacitive load = 30 pF*
2. *Measurement point set at CMOS level: 0.5 VDD*
3. *tHCLK ≥ 1 / 240 MHz*

- **Synchronous Waveforms and Timing**

Figure 4-31 Synchronous Non-Bus-Multiplexed NOR/PSRAM Read Timing

NSING Technologies Pte. Ltd.
Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg



NSING Technologies Pte. Ltd.
Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

Table 4-56 Synchronous Non-Bus-Multiplexed NOR/PSRAM Read Timing[1][2]

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FEMC_CLK period	9.8	-	ns
$t_{d(CLKL-NExL)}$	FEMC_CLK low to FEMC_NEx low (x = 1…4)	-	2.0	ns
$t_{d(CLKL-NExH)}$	FEMC_CLK low to FEMC_NEx high (x = 1…4)	2.0		ns
$t_{d(CLKL-NADVL)}$	FEMC_CLK low to FEMC_NADV low	-	2.0	ns
$t_{d(CLKL-NADVH)}$	FEMC_CLK low to FEMC_NADV high	2.0		ns
$t_{d(CLKL-AV)}$	FEMC_CLK low to FEMC_Ax valid (x = 0…25)	-	3.0	ns
$t_{d(CLKL-AIV)}$	FEMC_CLK low to FEMC_Ax invalid (x = 0…25)	2.0		ns
$t_{d(CLKL-NOEL)}$	FEMC_CLK low to FEMC_NOE low	-	2.0	ns
$t_{d(CLKL-NOEH)}$	FEMC_CLK low to FEMC_NOE high	2.0	-	ns
$t_{su(DV-CLKH)}$	Data valid (FEMC_D[31:0]) setup time before FEMC_CLK high	2.6	-	ns
$t_{h(CLKH-DV)}$	Data valid (FEMC_D[31:0]) hold time after FEMC_CLK high	0.3	-	ns
$t_{su(NWAITV-CLKH)}$	FEMC_NWAIT valid setup time before FEMC_CLK high	2.6	-	ns
$t_{h(CLKH-NWAITV)}$	FEMC_NWAIT valid hold time after FEMC_CLK high	0.3	-	ns

Notes:

1. *IO drive strength: 8mA, Capacitive load = 30pF*
2. *Measurement point set at CMOS level: 0.5VDD*

NSING Technologies Pte. Ltd.
Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

Figure 4-32 Synchronous Non-Multiplexed PSRAM Write Timing

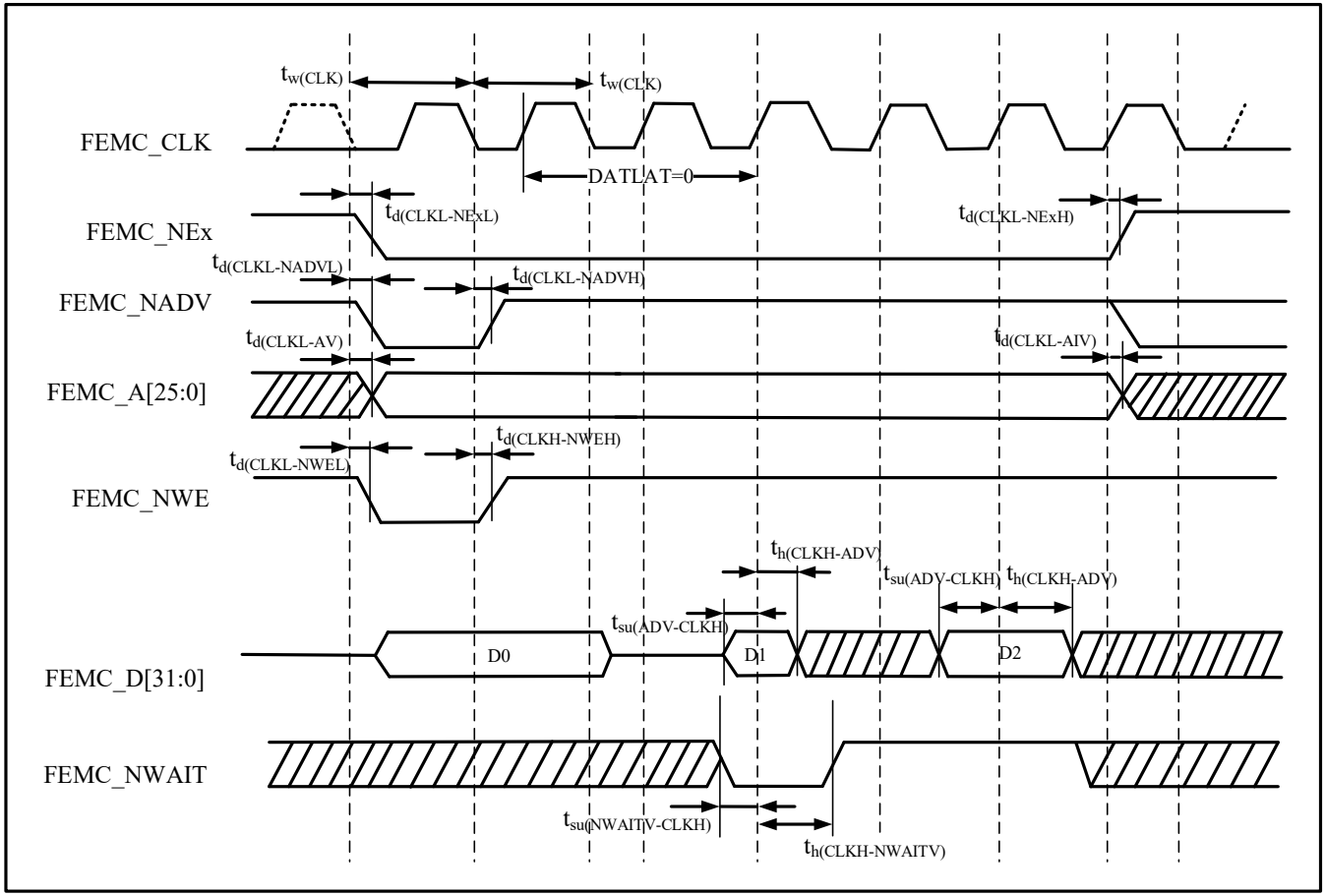


Table 4-57 Synchronous Non-Multiplexed PSRAM Write Timing (1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FEMC_CLK period	9.8	-	ns
$t_{d(CLKL-NExL)}$	FEMC_CLK low to FEMC_NEx low (x = 1…4)	-	2.0	ns
$t_{d(CLKL-NExH)}$	FEMC_CLK low to FEMC_NEx high (x = 1…4)	2.0	-	ns

NSING Technologies Pte. Ltd.
Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

$t_{d(CLKL-NADVL)}$	FEMC_CLK low to FEMC_NADV low	-	2.0	ns
$t_{d(CLKL-NADVH)}$	FEMC_CLK low to FEMC_NADV high	2.0	-	ns
$t_{d(CLKL-AV)}$	FEMC_CLK low to FEMC_Ax valid (x = 0…25)	-	3.0	ns
$t_{d(CLKH-AIV)}$	FEMC_CLK high to FEMC_Ax invalid (x = 0…25)	2.0	-	ns
$t_{d(CLKL-NWEL)}$	FEMC_CLK low to FEMC_NWE low	-	2.0	ns
$t_{d(CLKH-NWEH)}$	FEMC_CLK high to FEMC_NWE high	2.0	-	ns
$t_{d(CLKL-Data)}$	FEMC_CLK low to FEMC_D[31:0] valid data	-	3.0	ns
$t_{su(NWAITV-CLKH)}$	FEMC_NWAIT valid setup time before FEMC_CLK high	2.6	-	ns
$t_{h(CLKH-NWAITV)}$	FEMC_NWAIT valid hold time after FEMC_CLK high	0.3	-	ns

1. *IO drive strength: 8mA, Capacitive load = 30pF*
2. *Measurement point set at CMOS level: 0.5VDD*

NSING Technologies Pte. Ltd.
Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

Figure 4-33 Synchronous Bus-Multiplexed NOR/PSRAM Read Timing

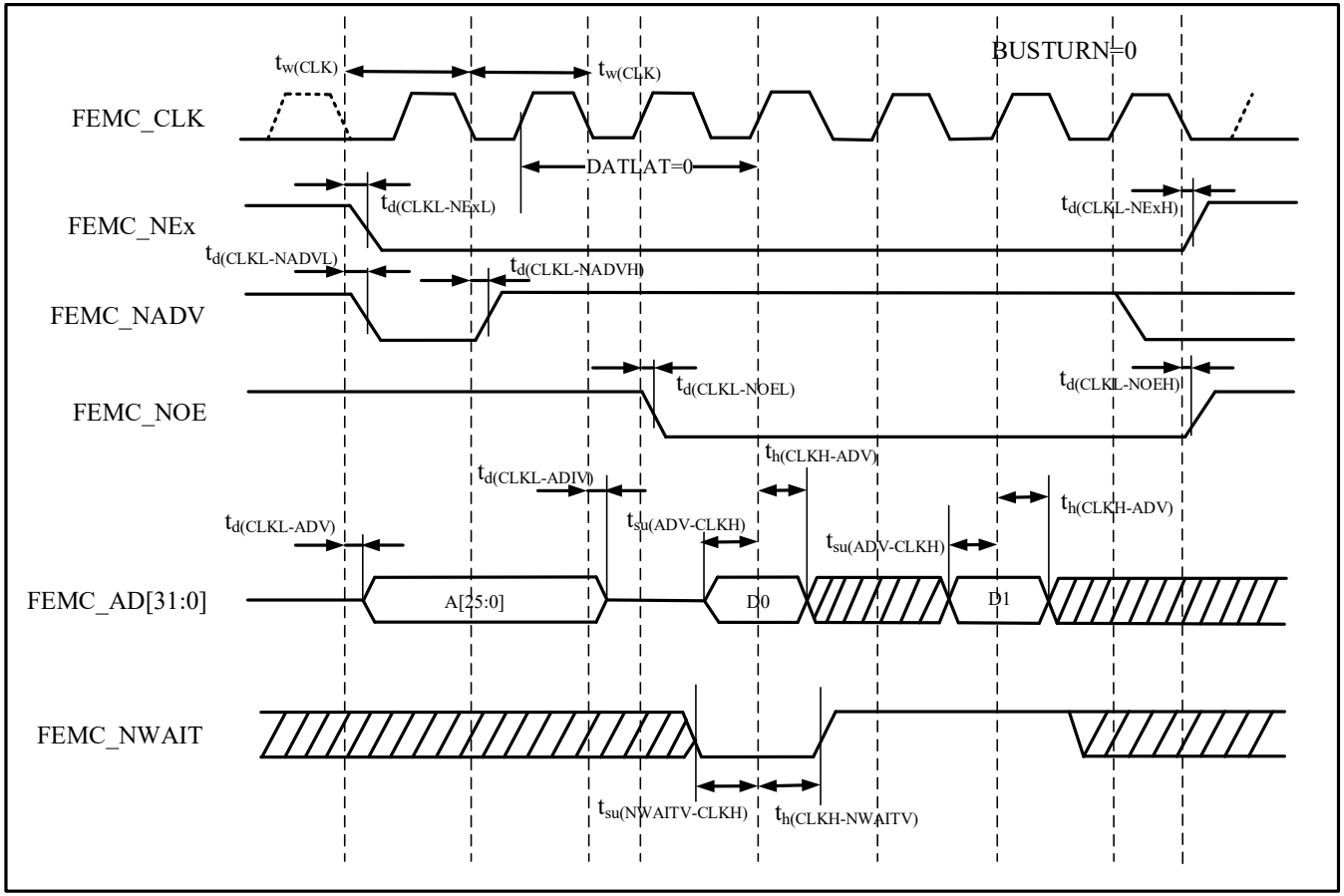


Table 4-58 Synchronous Bus-Multiplexed NOR/PSRAM Read Timing (1)(2)

Symbol	Parameter	Min(3)	Max	Unit
$t_{w(CLK)}$	FEMC_CLK period	9.8	-	ns
$t_{d(CLKL-NExL)}$	FEMC_CLK low to FEMC_NEx low (x = 1…4)	-	2.0	ns
$t_{d(CLKL-NExH)}$	FEMC_CLK low to FEMC_NEx high (x = 1…4)	2.0	-	ns
$t_{d(CLKL-NADVL)}$	FEMC_CLK low to FEMC_NADV low	-	2.0	ns

NSING Technologies Pte. Ltd.
Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

$t_{d(CLKL-NADVH)}$	FEMC_CLK low to FEMC_NADV high	2.0	-	ns
$t_{d(CLKL-NOEL)}$	FEMC_CLK low to FEMC_NOE low	-	2.0	ns
$t_{d(CLKL-NOEH)}$	FEMC_CLK low to FEMC_NOE high	2.0	-	ns
$t_{d(CLKL-ADV)}$	FEMC_CLK low to FEMC_AD[31:0] valid	-	3.0	ns
$t_{d(CLKL-ADIV)}$	FEMC_CLK low to FEMC_AD[31:0] invalid	2.0	-	ns
$t_{su(ADV-CLKH)}$	FEMC_AD[31:0] valid data setup time before FEMC_CLK high	2.6	-	ns
$t_{h(CLKH-ADV)}$	FEMC_AD[31:0] valid data hold time after FEMC_CLK high	0.3	-	ns
$t_{su(NWAITV-CLKH)}$	FEMC_NWAIT valid setup time before FEMC_CLK high	2.6	-	ns
$t_{h(CLKH-NWAITV)}$	FEMC_NWAIT valid hold time after FEMC_CLK high	0.3	-	ns

1. *IO drive strength: 8mA, Capacitive load = 30pF*
2. *Measurement point set at CMOS level: 0.5VDD*
3. *tHCLK ≥ 1/300MHz*

NSING Technologies Pte. Ltd.
Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

Figure 4-34 Synchronous Bus-Multiplexed PSRAM Write Timing

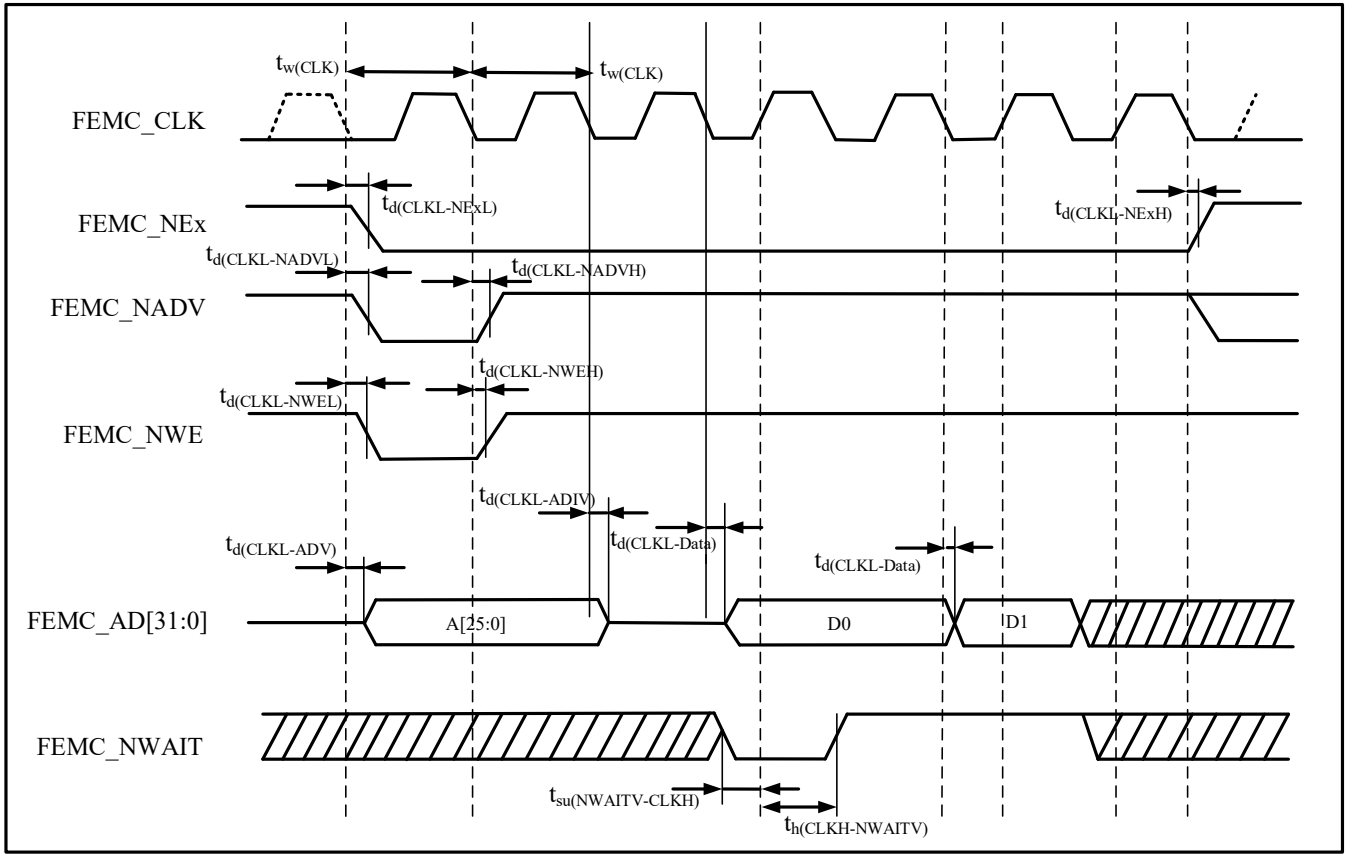


Table 4-59 Synchronous Multiplexed PSRAM Write Timing (1)(2)

Symbol	Parameter	Min(3)	Max	Unit
$t_{w(CLK)}$	FEMC_CLK cycle	9.8	-	ns
$t_{d(CLKL-NExL)}$	FEMC_CLK low to FEMC_NEx low (x = 1…4)	-	2.0	ns
$t_{d(CLKL-NExH)}$	FEMC_CLK low to FEMC_NEx high (x = 1…4)	2.0	-	ns
$t_{d(CLKL-NADVL)}$	FEMC_CLK low to FEMC_NADV low	-	2.0	ns
$t_{d(CLKL-NADVH)}$	FEMC_CLK low to FEMC_NADV high	2.0	-	ns

NSING Technologies Pte. Ltd.
Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

$t_{d(CLKL-NWEL)}$	FEMC_CLK low to FEMC_NWE low	-	2.0	ns
$t_{d(CLKL-NWEH)}$	FEMC_CLK low to FEMC_NWE high	2.0	-	ns
$t_{d(CLKL-ADV)}$	FEMC_CLK low to FEMC_AD[31:0] valid	-	3.0	ns
$t_{d(CLKL-ADIV)}$	FEMC_CLK low to FEMC_AD[31:0] invalid	2.0	-	ns
$t_{d(CLKL-Data)}$	FEMC_CLK low then FEMC_AD[31:0] valid	-	3.0	ns
$t_{su(NWAITV-CLKH)}$	FEMC_CLK high before FEMC_NWAIT valid	2.6	-	ns
$t_{h(CLKH-NWAITV)}$	FEMC_CLK high after FEMC_NWAIT valid	0.3	-	ns

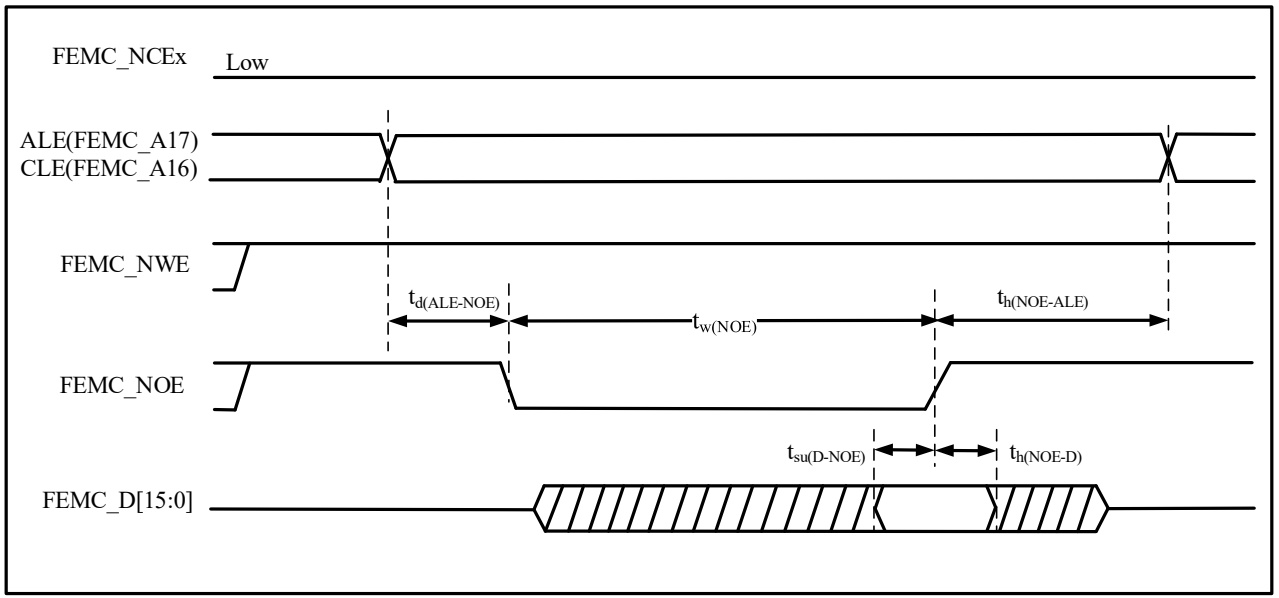
Notes:

1. *IO drive capability 8mA, Capacitive load = 30 pF*
2. *Measurement points at CMOS level: 0.5VDD*
3. *tHCLK ≥ 1/300MHz*

- **NAND Controller Waveforms and Timing**

Figures 4-35 to 4-36 show the waveforms for NAND operations.

Figure 4-35 NAND Controller Read Operation Waveform



NSING Technologies Pte. Ltd.
Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

Figure 4-36 NAND Controller Write Operation Waveform

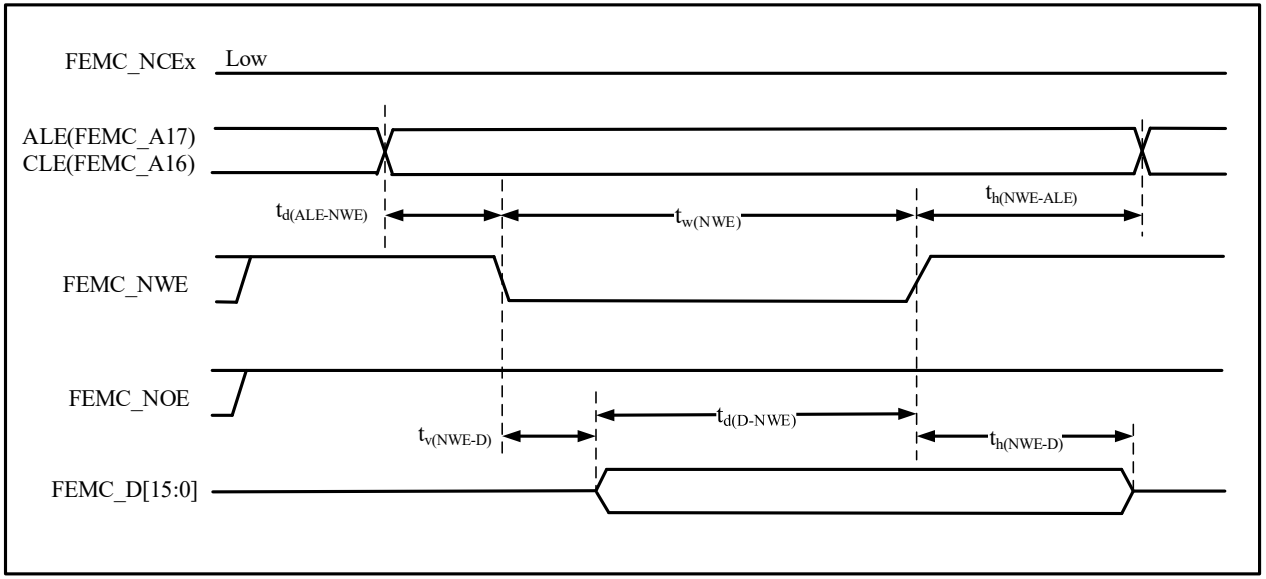


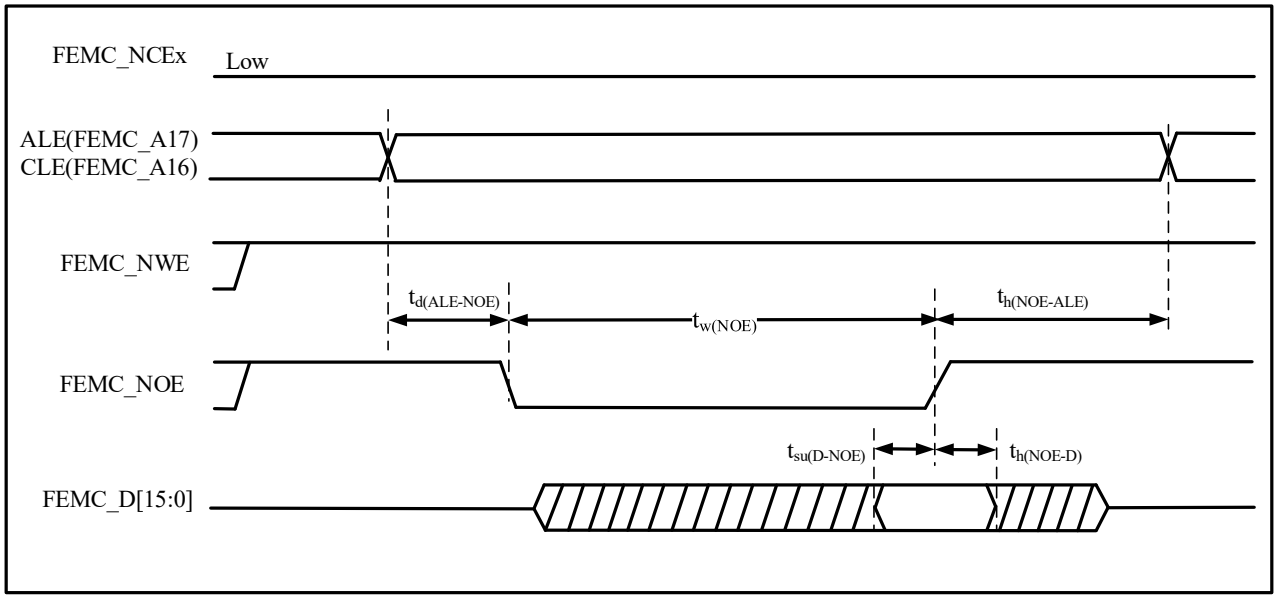
Table 4-60 NAND Flash Read Cycle Timing Characteristics (1)

Symbol	Parameter	Min	Max	Unit
$t_{w(NOE)}$	FEMC_NOE low time	TBD	TBD	ns
$t_{su(D-NOE)}$	Data valid before FEMC_NOE goes high	TBD	TBD	ns
$t_{h(NOE-D)}$	Data valid after FEMC_NOE goes high	TBD	TBD	ns
$t_{d(ALE-NOE)}$	ALE valid before FEMC_NOE goes low	TBD	TBD	ns
$t_{h(NOE-ALE)}$	ALE invalid after FEMC_NOE goes high	TBD	TBD	ns

Note: Guaranteed by design, not tested in production.

Figure 4-37 NAND Controller Read Operation Waveform

NSING Technologies Pte. Ltd.
Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg



NSING Technologies Pte. Ltd.
Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

Figure 4-38 NAND Controller Write Operation Waveform

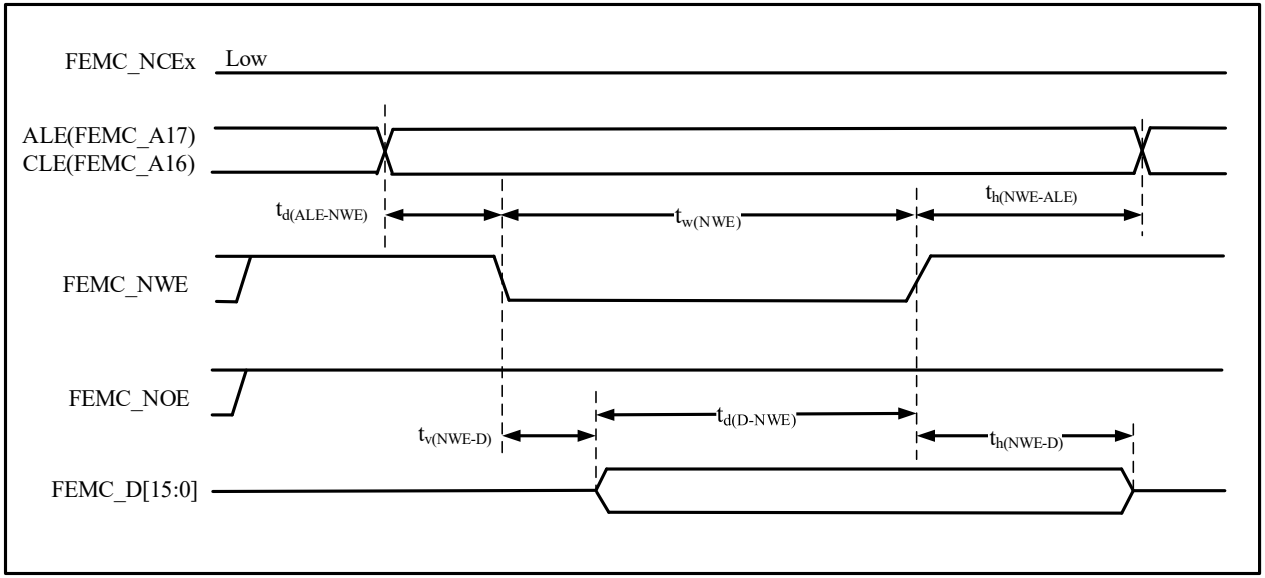


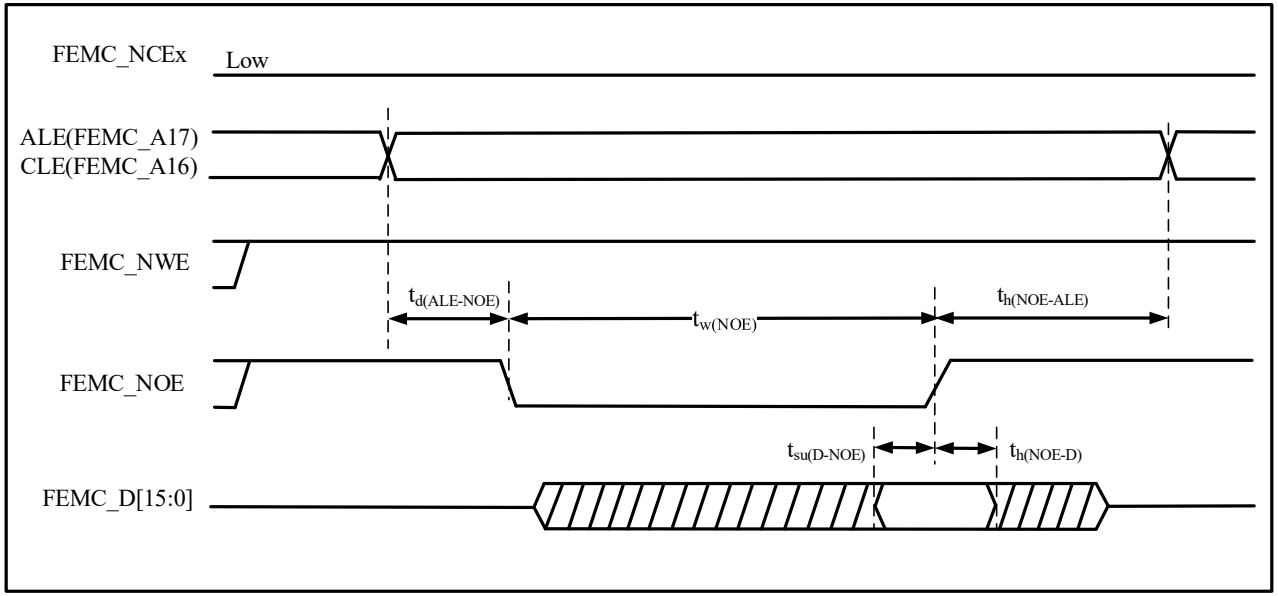
Table 4-61 NAND Flash Read Cycle Timing Characteristics (1)

Symbol	Parameter	Min	Max	Unit
$t_{w(NOE)}$	FEMC_NOE low time	TBD	TBD	
$t_{su(D-NOE)}$	Data valid before FEMC_NOE goes high	TBD	TBD	
$t_{h(NOE-D)}$	Data valid before FEMC_NOE goes high	TBD	TBD	
$t_{d(ALE-NOE)}$	ALE valid before FEMC_NOE goes low	TBD	TBD	
$t_{h(NOE-ALE)}$	ALE invalid after FEMC_NOE goes high	TBD	TBD	

Note: Guaranteed by design, not tested in production.

NSING Technologies Pte. Ltd.
Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

Figure 4-39 NAND Controller Read Operation Waveform



NSING Technologies Pte. Ltd.
Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

Figure 4-40 NAND Controller Write Operation Waveform

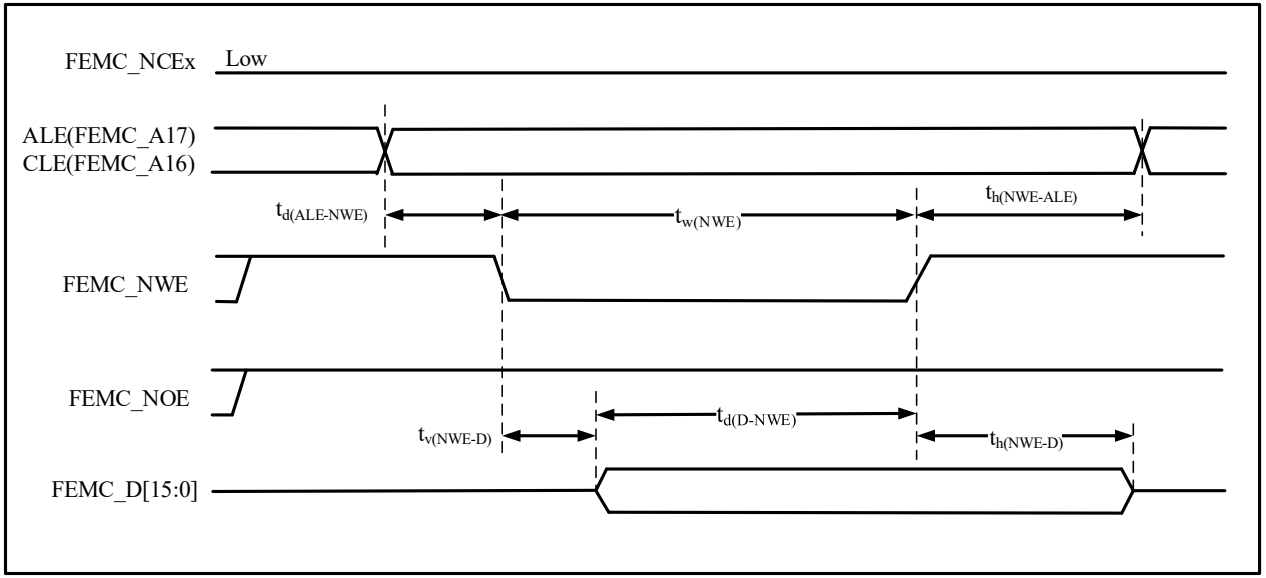


Table 4-62 NAND Flash Read Cycle Timing Characteristics (1)

Symbol	Parameter	Min	Max	Unit
$t_{w(NOE)}$	FEMC_NOE low time	TBD	TBD	ns
$t_{su(D-NOE)}$	Data valid before FEMC_NOE goes high	TBD	TBD	ns
$t_{h(NOE-D)}$	Data valid after FEMC_NOE goes high	TBD	TBD	ns
$t_{d(ALE-NOE)}$	ALE valid before FEMC_NOE goes low	TBD	TBD	ns
$t_{h(NOE-ALE)}$	ALE invalid after FEMC_NOE goes high	TBD	TBD	ns

Note: Guaranteed by design, not tested in production.

Table 4-63 NAND Flash Read/Write Cycle Timing Characteristics (1)

Symbol	Parameter	Min	Max	Unit
$t_{d(D-NWE)}$	Data valid before FEMC_NWE goes high	TBD	TBD	ns
$t_{w(NOE)}$	FEMC_NOE low time	TBD	TBD	ns
$t_{su(D-NOE)}$	Data valid before FEMC_NOE goes high	TBD	TBD	ns
$t_{h(NOE-D)}$	Data valid after FEMC_NOE goes high	TBD	TBD	ns

NSING Technologies Pte. Ltd.
Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

$t_{w(NWE)}$	FEMC_NWE low time	TBD	TBD	ns
$t_{v(NWE-D)}$	Data valid after FEMC_NWE goes low	TBD	TBD	ns
$t_{h(NWE-D)}$	Data invalid after FEMC_NWE goes high	TBD	TBD	ns
$t_{d(ALE-NWE)}$	ALE valid before FEMC_NWE goes low	TBD	TBD	ns
$t_{h(NWE-ALE)}$	ALE invalid after FEMC_NWE goes high	TBD	TBD	ns
$t_{d(ALE-NOE)}$	ALE valid before FEMC_NOE goes low	TBD	TBD	ns
$t_{h(NOE-ALE)}$	ALE invalid after FEMC_NOE goes high	TBD	TBD	ns

Note: Guaranteed by design, not tested in production.

4.3.34 4.3.23 USB_HS_DualRole Characteristics

Table 4-64 USBHS DC Electrical Characteristics

Symbol		Parameter	Conditions	Min	Typ	Max	Unit
V_{DD} (1)		USB Operating Voltage	-	3	-	3.6	V
LS/FS FUNCTIONALITY							
Input Voltage (1)	V_{DIFS}	Differential Input Sensitivity (FS/LS)	-	0.2	-	-	V
	V_{CMFS}	Differential Common-Mode Range (FS/LS)	包括 V_{DI} 范围	0.8	-	2.5	
	V_{ILSE}	Single-Ended Receive Low Voltage (FS/LS)	-	-	-	0.8	
	V_{IHSE}	Single-Ended Receive High Voltage (FS/LS)	-	2.0	-	-	
Output Voltage(1)	V_{OLFS}	Static Output Low Level (FS/LS)	R_L of 1.5kΩ to 3.6V	-	-	0.3	
	V_{OHFS}	Static Output High Level (FS/LS)	R_L of 15 kΩ to V_{SS}	2.8	3.3	3.6	
R_{PD}(1)		USBHS_DM/DP	$V_{IN} = V_{DD}$	-	15	-	kΩ
R_{PU}(1)		USBHS_DM/DP	$V_{IN} = V_{SS}$	-	1.5	-	
Z_{HSDRV}(1)		Drive Output Impedance	Steady state drive	-	45	-	Ω
HS FUNCTIONALITY							
Input Voltage (1)	I_{DIHS}	Differential Input Sensitivity (HS)	-	0.1	-	-	V
	V_{CMHS}	Differential Common-Mode Range (HS)	-	-50	-	500	mV
	V_{HSSQ}	HS Squelch Detection Threshold	-	100	-	150	
	V_{HSDSC}	HS Disconnect Threshold	-	525	-	625	

NSING Technologies Pte. Ltd.
Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

Output Voltage (1)	VOLHS	High-Speed Low-Level Output Voltage	45Ω load	-10	-	10	
	VOHHS	High-Speed High-Level Output Voltage	45Ω load	360	400	440	

Note: Guaranteed by design, not tested in production.

Table 4-65 USBHS Dynamic Characteristics (1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
TFR	Rise Time (FS/LS)	CL = 50 pF	4	-	20	ns
THSR	Differential Rise Time (HS)	-	500	-	-	ps
TFF	Fall Time (FS/LS)	CL = 50 pF	4	-	20	ns
THSF	Differential Fall Time (HS)	-	500	-	-	ps
VCRS	Output Single Crossing Voltage (FS/LS)	-	1.3	-	2	V

Note: Guaranteed by design, not tested in production

4.3.35 4.3.24 Controller Area Network (CAN) Electrical Characteristics

For detailed characteristics of the input/output multiplexed pins (CAN_TX and CAN_RX), refer to section 4.3.12.

4.3.36 4.3.25 Secure Digital Multimedia Card (SDMMC) Characteristics

Unless otherwise specified, the parameters in Table 4-66 are measured under the environmental temperature, fHCLK frequency, and VDDA supply voltage conditions defined in Table 4-4.

Table 4-66 SD/MMC Characteristics, VDD = 2.7V to 3.6V (1)(2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{pp}	Clock frequency in data transfer mode	-	-	-	104	MHz
$t_{W(CKL)}$	Clock low time	f_{pp}=50MHz	8.6	9.6	-	ns
$t_{W(CKH)}$	Clock high time		8.6	9.6	-	ns
CMD, D input in MMC Legacy/SDR/DDR and SD HS/SDR/DDR modes (referenced to CK)						

NSING Technologies Pte. Ltd.
Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

t_{ISU}	Input setup time HS	$f_{PP} \geq 50$ MHz	2.87	-	-	ns
t_{IH}	Input hold time HS		1.3	-	-	ns
t_{IDW}(3)	v		TBD	-	-	ns
CMD, D output in MMC Legacy/SDR/DDR and SD HS/SDR/DDR modes (referenced to CK)						
t_{OV}	Output valid dataHS	$f_{PP} \geq 50$ MHz	-	-	2.74	ns
t_{OH}	Output hold timeHS		3.0	-	-	ns
CMD, D input in SD default mode (referenced to CK)						
t_{ISUD}	Input setup time SD	f_{pp}=25MHz	2.87	-	-	ns
t_{IHD}	Input hold time SD		1.3	-	-	ns
CMD, D output in SD default mode (reference CK)						CMD, D output in SD default mode (reference CK)
t_{OVD}	Output valid default time SD	f_{pp}=25MHz	-	-	2.74	ns
t_{OHD}	Output hold default time SD		3.0	-	-	ns

1. Guaranteed by design, not tested in production.
2. CL = 20 pF.
3. In tuning mode, minimum time window where data must remain stable for correct sampling.

Table 4-67 eMMC Characteristics，VDD=1.71 to 1.9V (1)(2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{pp}	Clock frequency in data transfer mode	-	TBD	TBD	TBD	MHz
$t_{W(CKL)}$	Clock low time	f_{pp}=50MHz	TBD	TBD	TBD	ns
$t_{W(CKH)}$	Clock high time		TBD	TBD	TBD	ns

NSING Technologies Pte. Ltd.
Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

CMD, D input in eMM mode (referenced to CK)						
t_{ISU}	Input setup time HS HS	$f_{PP} \geq 50$ MHz	TBD	TBD	TBD	ns
t_{IH}	Input hold time HS		TBD	TBD	TBD	ns
t_{IDW}(3)	Input valid window (variable window)		TBD	TBD	TBD	ns
CMD, D output in eMMC mode (reference CK)						
t_{OV}	Output valid dataHS	$f_{PP} \geq 50$ MHz	TBD	TBD	TBD	ns
t_{OH}	Output hold timeHS		TBD	TBD	TBD	ns

1. *Guaranteed by design, not tested in production.*
2. *CL = 20 pF.*
3. *In tuning mode, minimum time window where data must remain stable for correct sampling.*

NSING Technologies Pte. Ltd.
Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

Figure 4-41 SD high speed mode

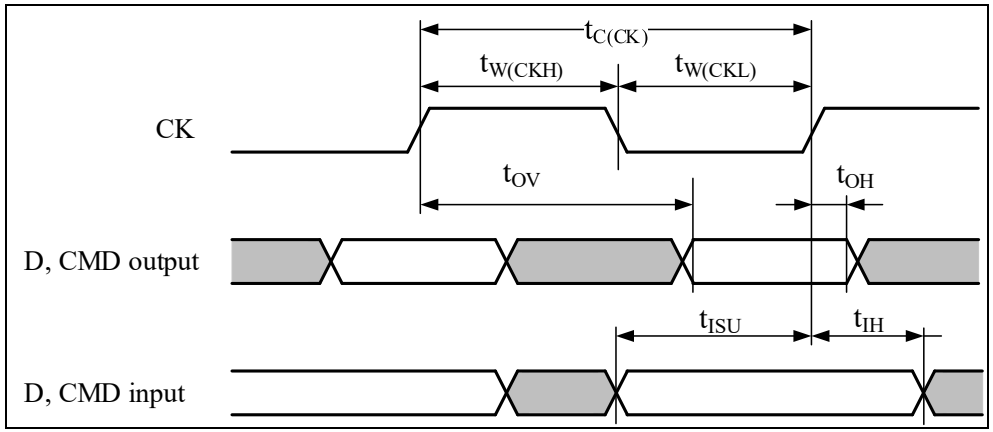
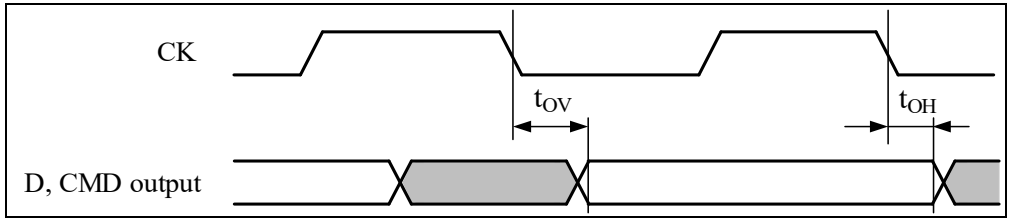
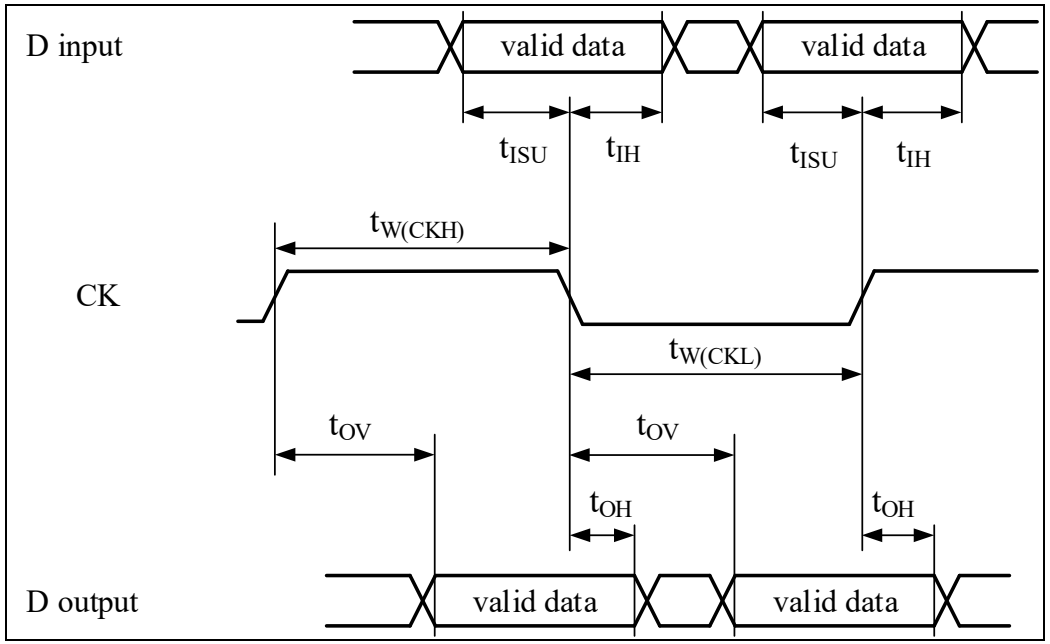


Figure 4-41 SDMMC DDR Mode



NSING Technologies Pte. Ltd.
Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

Figure 4-42 SDMMC DDR Mode



4.3.37 4.3.26 Ethernet Interface Characteristics

Unless otherwise specified, parameters in Tables 4-68, 4-69, 4-70, and 4-71 are measured under the environmental temperature (25°C), fHCLK frequency, and VDD supply voltage defined in Table 4-4.

Table 4-68 MDIO/SMA Timing

Symbol	Parameter	Min	Typ	Max	Unit
t_{MDC}	MDC period time（2.5 MHz）	-	2.5	-	MHz
$t_{d(MDIO)}$	Valid write data delay	-	-	5	ns
$t_{su(MDIO)}$	Read data setup time	17	-	-	ns
$t_{h(MDIO)}$	Read data hold time	0	-	-	ns

NSING Technologies Pte. Ltd.
Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

Figure 4-44 MDIO/SMA Timing Diagram

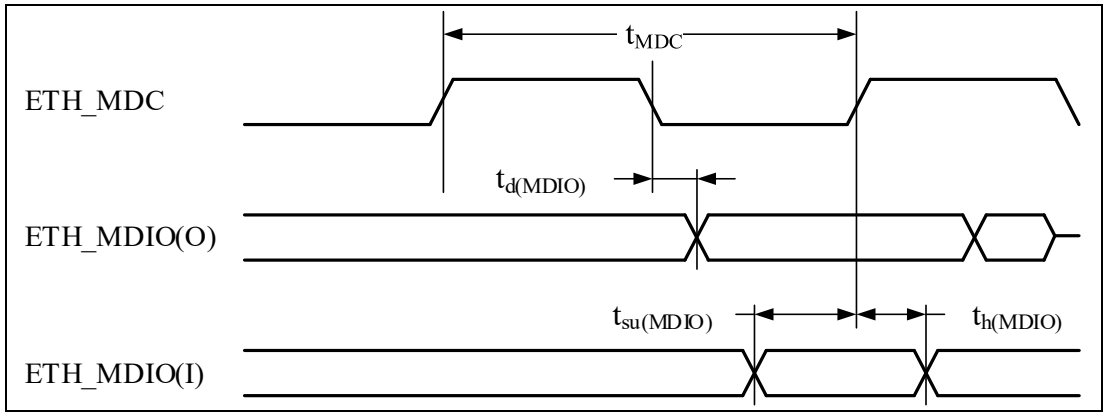


Table 4-69 RMII Timing

Symbol	Parameter	Min	Typ	Max	Unit
$t_{su(RXD)}$	Receive data setup time	2	-	-	ns
$t_{ih(RXD)}$	Receive data hold time	1.6	-	-	ns
$t_{su(CRS\_DV)}$	Carrier sense/data valid setup time	2	-	-	ns
$t_{ih(CRS\_DV)}$	Carrier sense/data valid hold time	1.6	-	-	ns
$t_{d(TXEN)}$	Transmit enable valid delay time	-	-	9.3	ns
$t_{d(TXD)}$	Transmit data valid delay time	-	-	9.3	ns

NSING Technologies Pte. Ltd.
Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

Figure 4-44 RMII Timing Diagram

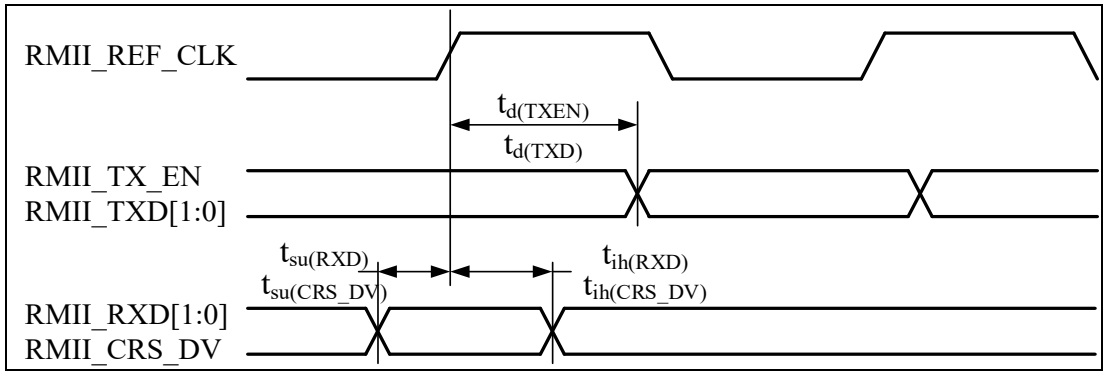


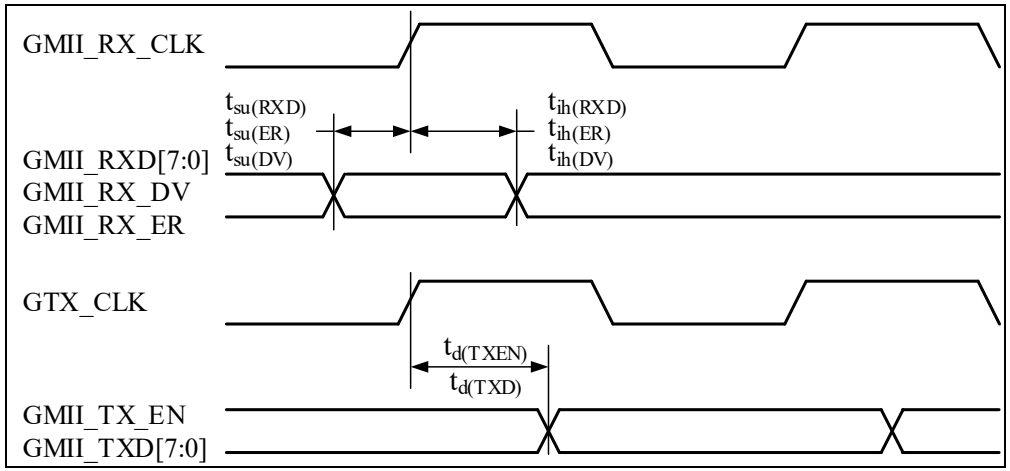
Table 4-71 lists the Ethernet MAC timing of MII and Figure 4-46 shows the corresponding timing diagram.

Table 4-71 MII Timing

Symbol	Parameter	Min	Typ	Max	Unit
$t_{su(RXD)}$	Receive data setup time	2.5	-	-	ns
$t_{ih(RXD)}$	Receive data hold time	0.5	-	-	ns
$t_{su(DV)}$	Data valid setup time	2.5	-	-	ns
$t_{ih(DV)}$	Data valid hold time	0.5	-	-	ns
$t_{su(ER)}$	Error setup time	2.5	-	-	ns
$t_{ih(ER)}$	Error hold time	0.5	-	-	ns
$t_{d(TXEN)}$	Transmit enable valid delay time	-	-	12.0	ns
$t_{d(TXD)}$	Transmit data valid delay time	-	-	12.0	ns

NSING Technologies Pte. Ltd.
Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

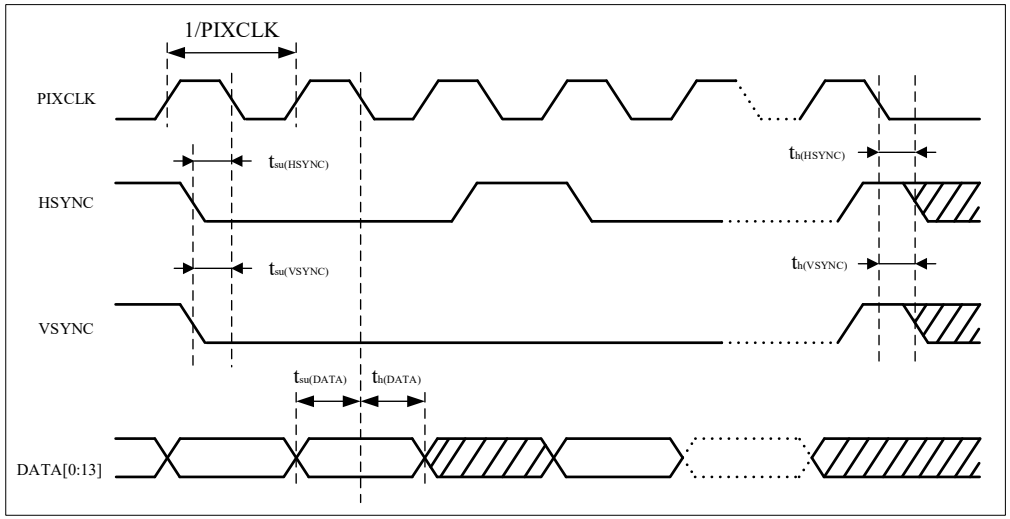
Figure 4-46 MII Timing Diagram



4.3.38 4.3.27 Digital Video Port (DVP) Interface

Table 4-72 shows the characteristics of the DVP interface signals, and Figure 4-48 illustrates the related timing.

Figure 4-48 DVP Interface Timing Diagram



NSING Technologies Pte. Ltd.
Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

Table 4-72 DVP Signal Dynamic Characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
PCLK	Pixel clock input	-	-	110	MHz
Dpixel	Pixel clock input duty cycle	-	30	70	-
$t_{su(DATA)}$	Data input setup time	-	3	-	ns
$t_{h(DATA)}$	Data input hold time	-	1	-	
$t_{su(HSYNC)}$, $t_{su(VSYNC)}$	HSYNC/VSYNC input setup time	-	3	-	
$t_{h(HSYNC)}$, $t_{h(VSYNC)}$	HSYNC/VSYNC input hold time	-	1	-	

NSING Technologies Pte. Ltd.
Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

4.3.39 Digital Filter Unit Based on Σ-Δ Modulator (DSMU) Characteristics

Unless otherwise specified, the **Parameters** in Table 4-73 are measured under the environmental conditions (ambient temperature 25 °C, fHCLK frequency, and VDD supply voltage) conforming to Table 4-4. Additional test conditions are as follows:

- Port switching speed configuration: DSy[1:0] = 2b10, SRy = 1b0
- Load capacitance CL = 30 pF
- Reference CMOS level standards, I/O measurement point at 0.5 VDD

For more details on the characteristics of ports (DSMU_CKINx, DSMU_DATINx, DSMU_CKOUT), please refer to the I/O Port Characteristics section 4.3.13.

Table 4-73 DSMU Timing Parameters

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{DSMU} ($1/T_{DSMU}$)	DSMU clock	2.3V < VDD < 3.63V		TBD	TBD	TBD	MHz
f_{CKIN} ($1/T_{CKIN}$)	Input clock frequency	2.3V < VDD < 3.63V, SPI interface (SITP[1:0] = 0,1), external clock mode (SPICLKSEL[1:0] = 0)		TBD	TBD	TBD	
		2.3V < VDD < 3.63V, SPI interface (SITP[1:0] = 0,1), external clock mode (SPICLKSEL[1:0] = 0)		TBD	TBD	TBD	
		2.3V < VDD < 3.63V, SPI interface (SITP[1:0] = 0,1), internal clock mode (SPICLKSEL[1:0] ≠ 0)		TBD	TBD	TBD	
		2.3V < VDD < 3.63V, SPI interface (SITP[1:0] = 0,1), internal clock mode (SPICLKSEL[1:0] ≠ 0)		TBD	TBD	TBD	
f_{CKOUT}	Output clock frequency	2.3V < VDD < 3.63V		TBD	TBD	TBD	
$Duty_{CKOUT}$	Output clock duty cycle	2.3V < VDD < 3.63V	TBD	TBD	TBD	TBD	%
			TBD	TBD	TBD	TBD	
t_{wh}(CKIN) t_{wl}(CKIN)	Input clock high/low pulse width	2.3V < VDD < 3.63V, SPI interface (SITP[1:0] = 0,1), external clock mode (SPICLKSEL[1:0] = 0)		TBD	TBD	TBD	ns
t_{su}	Input data setup time	2.3V < VDD < 3.63V, SPI interface (SITP[1:0] = 0,1), external clock mode (SPICLKSEL[1:0] = 0)		TBD	TBD	TBD	

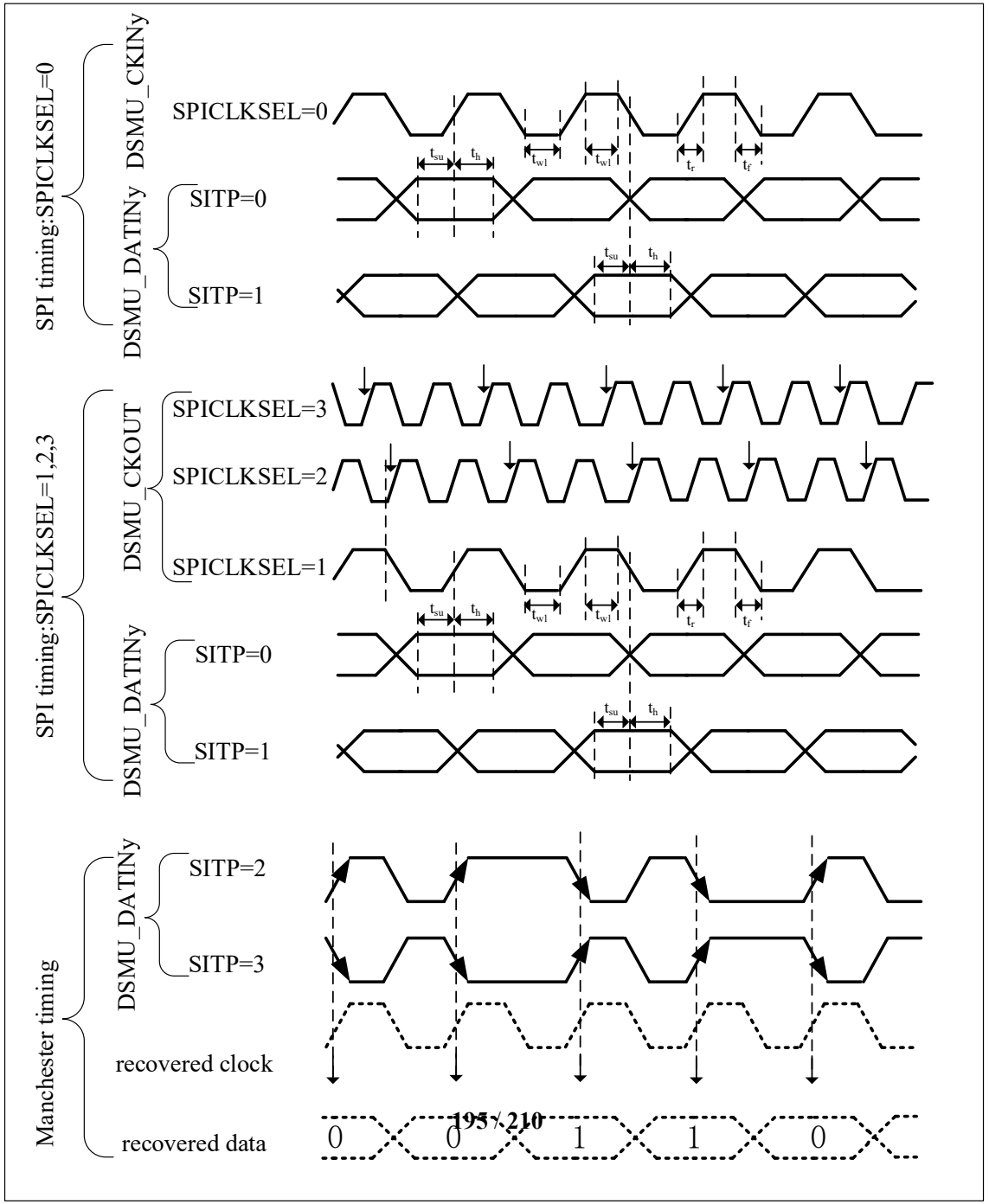
NSING Technologies Pte. Ltd.
Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

t_h	Input data hold time	2.3V < VDD < 3.63V, SPI interface (SITP[1:0] = 0,1), external clock mode (SPICLKSEL[1:0] = 0)	TBD	TBD	TBD	
$T_{Manchester}$	Manchester data period (self-recovery clock period)	2.3V < VDD < 3.63V, Manchester interface (SITP[1:0] = 2,3), internal clock mode (SPICLKSEL[1:0] ≠ 0)	TBD	TBD	TBD	

NSING Technologies Pte. Ltd.
Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

Figure 4-49 DSMU Channel Transceiver Timing Diagram

NSING Technologies Pte. Ltd.
Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg



195×210

NSING Technologies Pte. Ltd.
Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

4.3.29 12-bit Analog-to-Digital Converter (ADC) Electrical Characteristics

Unless otherwise specified, the parameters in **Table 4-74** are measured under the environmental conditions (ambient temperature 25 °C), fHCLK frequency, and VDDA supply voltage specified in **Table 4-4**.

Note: It is recommended to perform a calibration each time after power-up.

Table 4-74 ADC Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Supply voltage	-	2.3	-	3.6	V
V_{REF+}	Positive reference voltage	-	2.3	-	V_{DDA}	V
f_{ADC}	ADCclock frequency	-	-	-	20	MHz
f_s	Sampling rate (1)	-	-	-	5	Msps
V_{AIN}	Conversion voltage range (2)	-	0(VSSA or VREF- tied to ground)	-	V_{REF+}	V
R_{ADC}	Sample switch resistance	2.4~3.3V	-	250		ohm
		2.3~2.4V	-	350		
C_{ADC}	Internal sample and hold capacitor	-	-	1.5	-	pF
SNDR	Singal noise distortion ration	-	-	TBD	-	dBFS
T_{cal}	Calibration time	-	74			$1/f_{ADC}$
ts	Sampling time	f_{ADC} = 20 MHz	0.05	-	7	us
Ts			1	-	-	$1/f_{ADC}$
t_{STAB}	Power-up time	-	0	0	20	μs
t_{CONV}(2)	Total conversion time (including sampling time)	-	4~400 (sampling tS + successive approximation 3)			$1/f_{ADC}$

Notes:

1. *Guaranteed by design, not tested in production.*
2. *Depending on the package, VREF+ may be internally connected to VDDA, and VREF- may be internally connected to VSSA.*
3. *The relationship between maximum input impedance Rin and sampling time is detailed in **Table 4-67**.*

NSING Technologies Pte. Ltd.
Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

Table 4-75 ADC Sampling Time [(1)(2)]

Resolution	Rin（kΩ）	Minimum Sampling Time（ns）
12-bit	0	50
	0.45	100
	0.7	150
	0.95	200
	1.95	400
	2.95	600
	3.95	800
	4.95	1000
	9.95	2000
10-bit	TBD	TBD
	TBD	TBD
	TBD	TBD
	TBD	TBD
	TBD	TBD
	TBD	TBD
	TBD	TBD
	TBD	TBD
	TBD	TBD

Notes:

1. *Guaranteed by design, not tested in production.*
2. *Test conditions: Vdda = 2.4V to 3.6V, Vddd = 0.9V, Tjunction = 125°C, fclk = 20 MHz.*

NSING Technologies Pte. Ltd.
Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

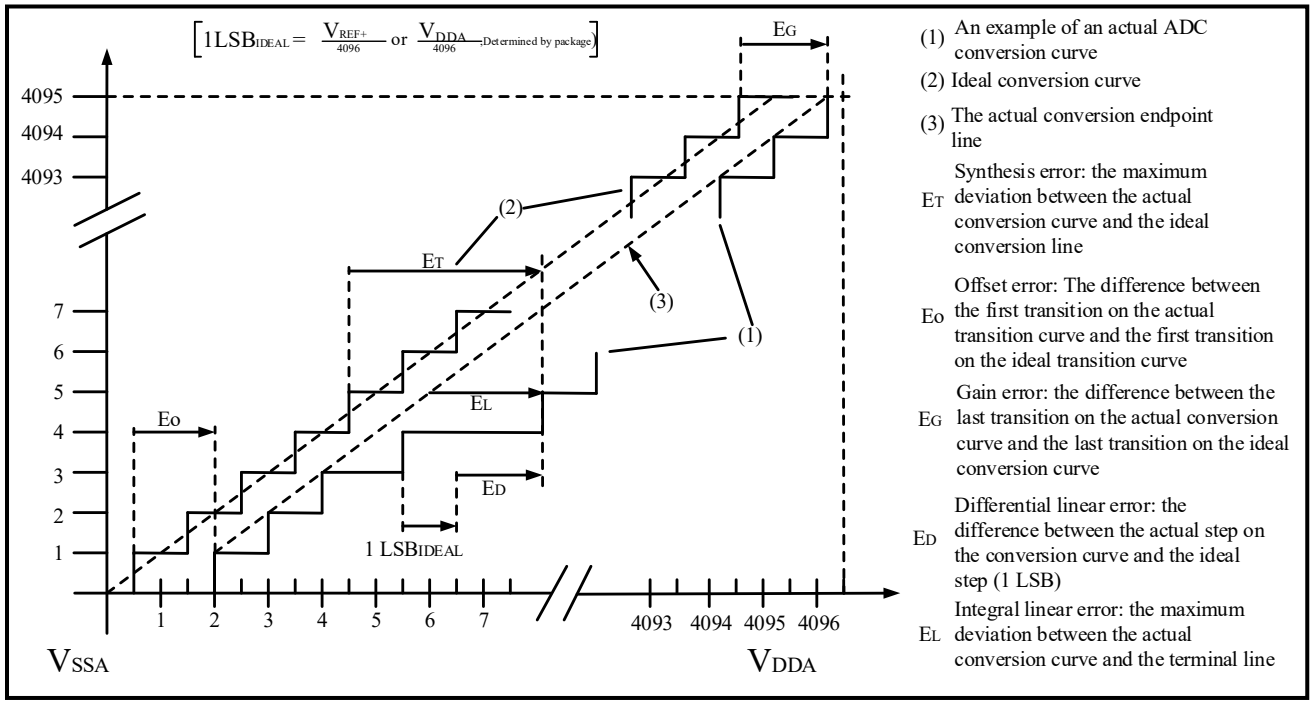
Table 4-76 ADC Accuracy – Limited Test Conditions(1)(2)

Symbol	Parameter	Test Conditions	Typ	Max(3)	Unit
ET(4)	Total Error	fHCLK = 200 MHz, fADC = 20 MHz, sample rate = 3Msps, VDDA = 3.3V, TA = 25°C. Measurement is performed after ADC calibration. VREF+ = 2.5V	TBD	TBD	LSB
EO(4)	Offset Error		TBD	TBD	
ED	Differential Non-Linearity Error		TBD	TBD	
EL	Integral Non-Linearity Error		TBD	TBD	

Notes:

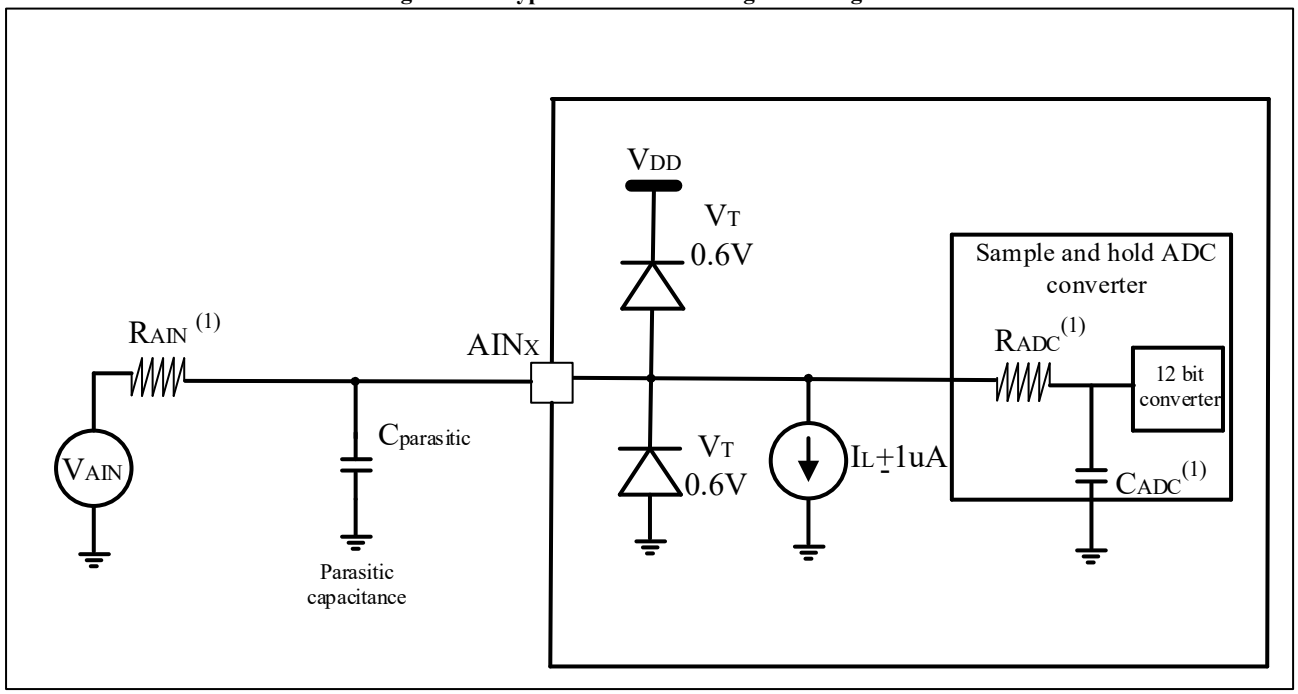
1. *ADC DC accuracy values are measured after internal calibration.*
2. *Relationship between ADC accuracy and reverse injection current: avoid injecting reverse currents on any standard analog input pins, as it significantly degrades the conversion accuracy of other analog inputs. It is recommended to add a Schottky diode (between the pin and ground) on any analog input pins that may have reverse injection currents.*
3. *Forward injection currents within the IINJ(PIN) range specified in Section 4.2 will not affect ADC accuracy.*
4. *Guaranteed by overall evaluation, not tested in production.*

Figure 4-50 ADC Accuracy Characteristics



NSING Technologies Pte. Ltd.
Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

Figure 4-51 Typical Connection Diagram Using ADC



Notes:

1. *For values of RAIN, RADC, and CADC, refer to Table 4-66.*
2. *Cparasitic refers to the parasitic capacitance (approximately 7pF) on the PCB and solder pads (related to soldering and PCB layout quality). A larger Cparasitic value will reduce conversion accuracy. The solution is to lower fADC.*

4.3.30 12-bit Digital-to-Analog Converter (DAC) Electrical Parameters

Unless otherwise specified, the parameters in **Table 4-69** are measured under environmental conditions specified in **Table 4-4** (ambient temperature 25°C), **fHCLK** frequency, and **VDDA** supply voltage.

Table 4-77 DAC 1MSPS Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	DAC output buffer off, output internal only	2.3	-	3.6	V
V_{REF+}	Positive reference voltage	DAC output buffer off, output internal only	2.3	-	VDDA	

NSING Technologies Pte. Ltd.
Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

V_{REF-}	Negative reference voltage	-		VSSA			
R_L	Load resistance when buffer is on	DAC output	Connected to VSSA	5	-	-	kΩ
		Buffer on	Connected to VDDA	25	-	-	
Ro	Output impedance	DAC output buffer off		-	15	-	kΩ
C_L	Load capacitance	-		-	-	50	pF
DAC_OUT Max	DAC_OUT output voltage	Output buffer on		0.2	-	V_{REF+} - 0.2	V
		Output buffr off		TBD	TBD	TBD	-
I_{DD}	DAC DC consumption in idle (standby mode) (VDDD+VDDA+VREF+)	-		TBD	TBD	TBD	μA
		-		TBD	TBD	TBD	μA
$t_{SETTLING}$	Settling time (full range: 12-bit input code from min to max, DAC_OUT reaches final value ±1 LSB)	DAC buffer on CL ≤ 50 pF,RL ≥ 5 kΩ		-	3	4.1	μs
		DAC buffer off		-	2.1	2.6	
t_{WAKEUP}	Wake-up time from shutdown (DAC enabled to DAC_OUT reaches final value ±1 LSB)	DACbuffer on,CL ≤ 50 pF, RL ≥ 5 kΩ		-	6.5	10	μs
		DACbuffer on，CL ≤ 10 pF		-	2.1	5	
PSRR	Power Supply Rejection Ratio (relative to VDD33A) (static DC measurement)	DACbuffer on，CL ≤ 50 pF, RL ≥ 5 kΩ		TBD	TBD	TBD	dB
TW_to_W	Minimum time between two consecutive writes to DACx_DATO register to ensure correct DAC_OUT(1 LSB)。 DACxy_CTRL.EXOUT = 1, DACxy_CTRL. BxEN = 1	CL ≤ 50 pF, RL ≥ 5 kΩ		TBD	-	-	μs
	DACxy_CTRL.EXOUT = 1, DACxy_CTRL. BxEN = 0 或 DACxy_CTRL.INOUT = 1, DACxy_CTRL. BxEN = 0	CL ≤ 10 pF		TBD	-	-	
Voffset	Middle code offset for 1 trim code step	VREF+ =3.6V		-	-	1500	μV

NSING Technologies Pte. Ltd.
Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

$I_{DDA(DAC)}$	DAC consumption from VDDA	Output buffer on	No load，input mid 0x800	TBD	TBD	TBD	µA
			No load，input Max 0xF1C	TBD	TBD	TBD	
		Output buufer off	No load，input mod 0x800	TBD	TBD	TBD	
$I_{DDV(DAC)}$	DAC consumption from VREF+	Output buffer on	No load，input mid 0x800	TBD	TBD	TBD	µA
			No load	TBD	TBD	TBD	
		Output buffer off	No load，input mid 0x800	TBD	TBD	TBD	
DNL	Differential Non-Linearity)	-		-	TBD	TBD	TBD
INL	Integral Non-Linearity	-		-	TBD	TBD	TBD
Offset	Offset error (measured at code 0x800)	Output buffer on,CL ≤ 50 pF,RL ≥ 5 kΩ	VREF+ =3.6V	TBD	TBD	TBD	LSB
			VREF+ =1.8V	TBD	TBD	TBD	
		Output buffer off,CL ≤ 50 pF, no RL		-	TBD	TBD	
Gain error	Gain error	-		-	TBD	TBD	TBD

Note: *Guaranteed by characterization, not tested in production.*

4.3.31 Comparator (COMP) Characteristics

Unless otherwise specified, the parameters in **Table 4-78** are measured under environmental conditions specified in **Table 4-4** (ambient temperature 25°C), **fHCLK** frequency, and **VDDA** supply voltage.

Table 4-78 Comparator Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	-	2.3	-	3.6	V
V_{IN}	Input voltage range	-	0	-	VDDA	
V_{REF}	6bit DAC offset voltage	DAC mid output，VREFP = 3.3V	-	±5	±12	mV
I_{REF}	6bit DAC static consumption from VREFP	DAC mid output，VREFP = 3.3V	-	TBD	TBD	uA
		DAC max output，VREFP = 3.3V	-		TBD	uA

NSING Technologies Pte. Ltd.
Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

T_{START}	Comparator start-up settling time	VDDA>=2.7	-	-	5	us
		VDDA<2.7V	-	-	7	
t_D	Propagation delay for 200 mV step with 100 mV overdrive	VDDA>=2.7	-	30	-	ns
		VDDA<2.7V	-	20	-	
V_{OFFSET}	Comparator input offset error	Full common mode range	-	-	±10	mV
Vhys	Comparator hysteresis	No hysteresis	-	0	-	mV
		Low hysteresis	-	20	-	
		Medium hysteresis	-	30	-	
		High hysteresis	-	50	-	
I_{DDA}	Comparator consumption from VDDA	Static	-	140	-	µA
		With 50 kHz ±100 mV overdrive square signal	-	150	-	

Note: *Guaranteed by design, not tested in production.*

4.3.32 Voltage Reference Buffer (VREFBUF) Characteristics

Unless otherwise specified, the parameters in **Table 4-71** are measured under environmental conditions specified in **Table 4-4** (ambient temperature 25°C), **fHCLK** frequency, and **VDDA** supply voltage.

Table 4-79 Voltage Reference Buffer Characteristics (1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	-	2.3	-	3.6	V
V_{REFBUF_OUT}	Reference voltage output	VS= 00 & VDDA ≥ 2.8V	2.494	2.498	2.51	
		VS= 01 & VDDA ≥ 2.4V	2.022	2.024	2.034	
		VS=10 & VDDA ≥ 2.3V	1.801	1.802	1.811	
		VS=11 & VDDA ≥ 2.3V	1.496	1.497	1.505	
TRIM	Trim step resolution	-	-	±0.05	±0.1	%

NSING Technologies Pte. Ltd.
Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

CL	Load capacitance	-	0.5	1	2	µF
R_{ESR}	Equivalent Series Resistance	-	0	0	2	Ω
PSRR	Power Supply Rejection Ratio	DC	37.54	49.72	TBD	dB
		100KHz	12.1	70.36	TBD	
t_{START}	Start-up time	CL =1 µF	-	366.1	1080	µs
$I_{DDA(VREFBUF)}$	VREFBUF consumption from VDDA	Iload <= 10 mA	-	48	TBD	µA
I_{INRUSH}	Max IDDA(VREFBUF) at startup phase	Iload = 0	7.42	18.88	TBD	mA

Note: *Guaranteed by design, not tested in production.*

4.3.33 Temperature Sensor (TS) Characteristics

Unless otherwise specified, the parameters in **Table 4-72** are measured under environmental conditions specified in **Table 4-4** (ambient temperature 25°C), **fHCLK** frequency, and **VDDA** supply voltage.

Table 4-80 Temperature Sensor Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_L(1)	Linearity V_{SENSE} with respect to temperature	-	±3	TBD	ºC
Avg_Slope(1)	Average slope	TBD	-3.4	TBD	mV/ºC
V_{25}(1)	Voltage at 25°C	-	1.37	-	V
t_{START}(1)	Start-up time	4	-	10	µs
T_{S_temp}(2)(3)	ADC sampling time when reading temperature	8.2	-	17.1	µs

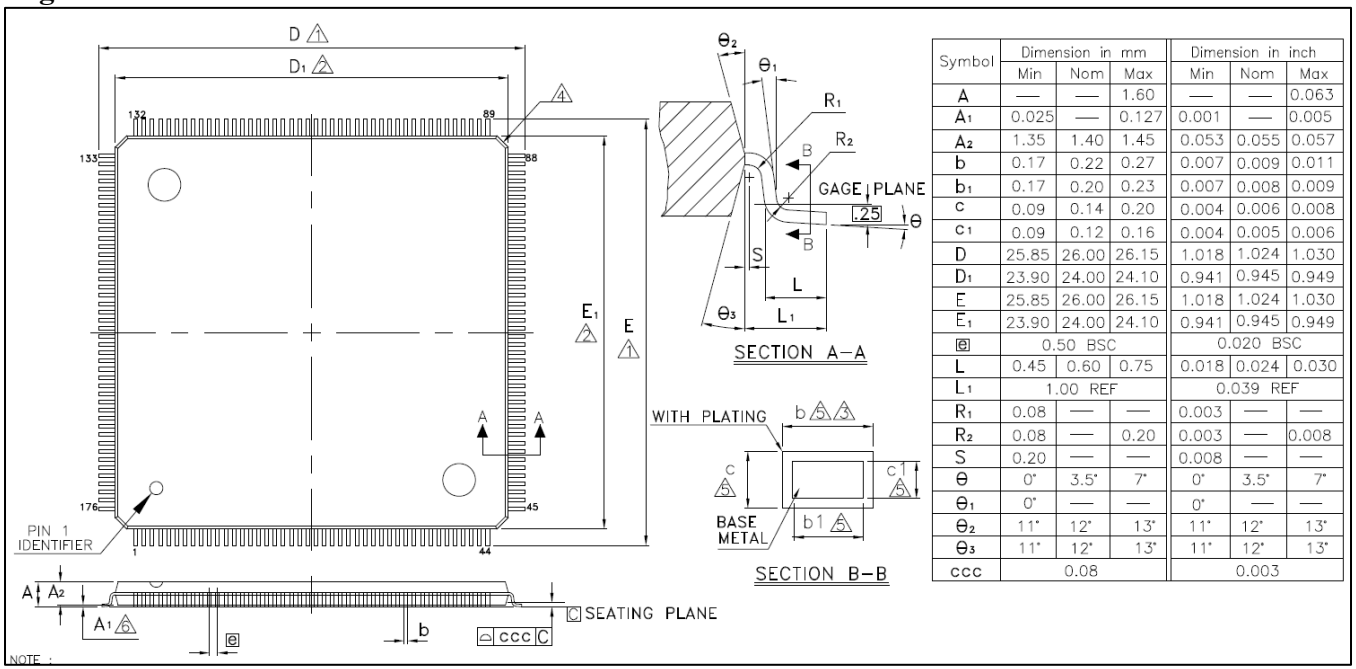
Notes:

1. *Guaranteed by characterization, not tested in production.*
2. *Guaranteed by design, not tested in production.*
3. *The minimum sampling time can be determined by multiple loop cycles in the application.*

NSING Technologies Pte. Ltd.
Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

5 Package Size

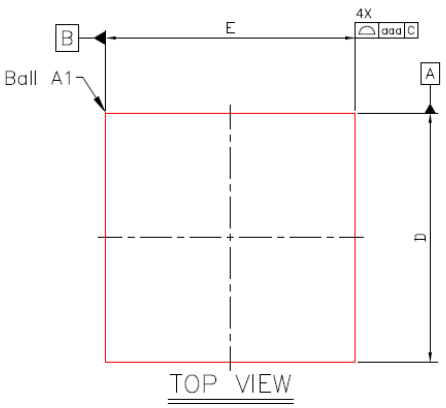
5.1 LQFP176 Package Size

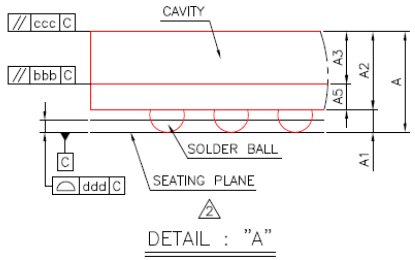


Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	—	—	1.60	—	—	0.063
A_1	0.025	—	0.127	0.001	—	0.005
A_2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.17	0.22	0.27	0.007	0.009	0.011
b_1	0.17	0.20	0.23	0.007	0.008	0.009
c	0.09	0.14	0.20	0.004	0.006	0.008
c_1	0.09	0.12	0.16	0.004	0.005	0.006
D	25.85	26.00	26.15	1.018	1.024	1.030
D_1	23.90	24.00	24.10	0.941	0.945	0.949
E	25.85	26.00	26.15	1.018	1.024	1.030
E_1	23.90	24.00	24.10	0.941	0.945	0.949
e	0.50 BSC			0.020 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L_1	1.00 REF			0.039 REF		
R_1	0.08	—	—	0.003	—	—
R_2	0.08	—	0.20	0.003	—	0.008
S	0.20	—	—	0.008	—	—
θ	0°	3.5°	7°	0°	3.5°	7°
θ_1	0°	—	—	0°	—	—
θ_2	11°	12°	13°	11°	12°	13°
θ_3	11°	12°	13°	11°	12°	13°
ccc	0.08			0.003		

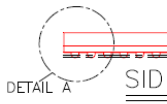
NSING Technologies Pte. Ltd.
Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

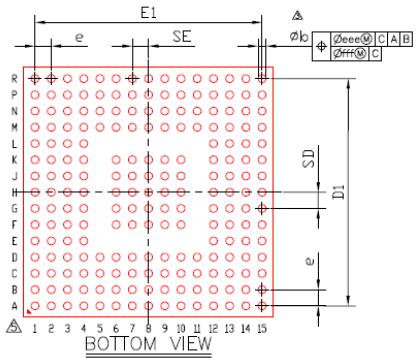
5.2 UFBGA176+25 Package Size





Symbol	Dimension in mm			Dimension in Inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.919	1.000	1.081	0.036	0.039	0.043
A1	0,160	0,210	0,260	0,006	0,008	0,010
A2	0.726	0.790	0.854	0.029	0.031	0.034
A3	0,480	0,530	0,580	0,019	0,021	0,023
A5	0.220	0.260	0.300	0.009	0.010	0.012
E	9,900	10,000	10,100	0,390	0,394	0,398
D	9.900	10.000	10.100	0.390	0.394	0.398
E1	—	9,100	—	—	0,358	—
D1	—	9.100	—	—	0.358	—
e	—	0,650	—	—	0,026	—
b	0.260	0.310	0.360	0.010	0.012	0.014
aaa		0,150			0,006	
bbb		0.100			0,004	
ccc		0,100			0,004	
ddd		0.100			0.004	
eee		0.150			0.006	
fff		0.080			0,003	
MD/ME		15/15				
SE		0.650			0.026	
SD		0.650			0.026	



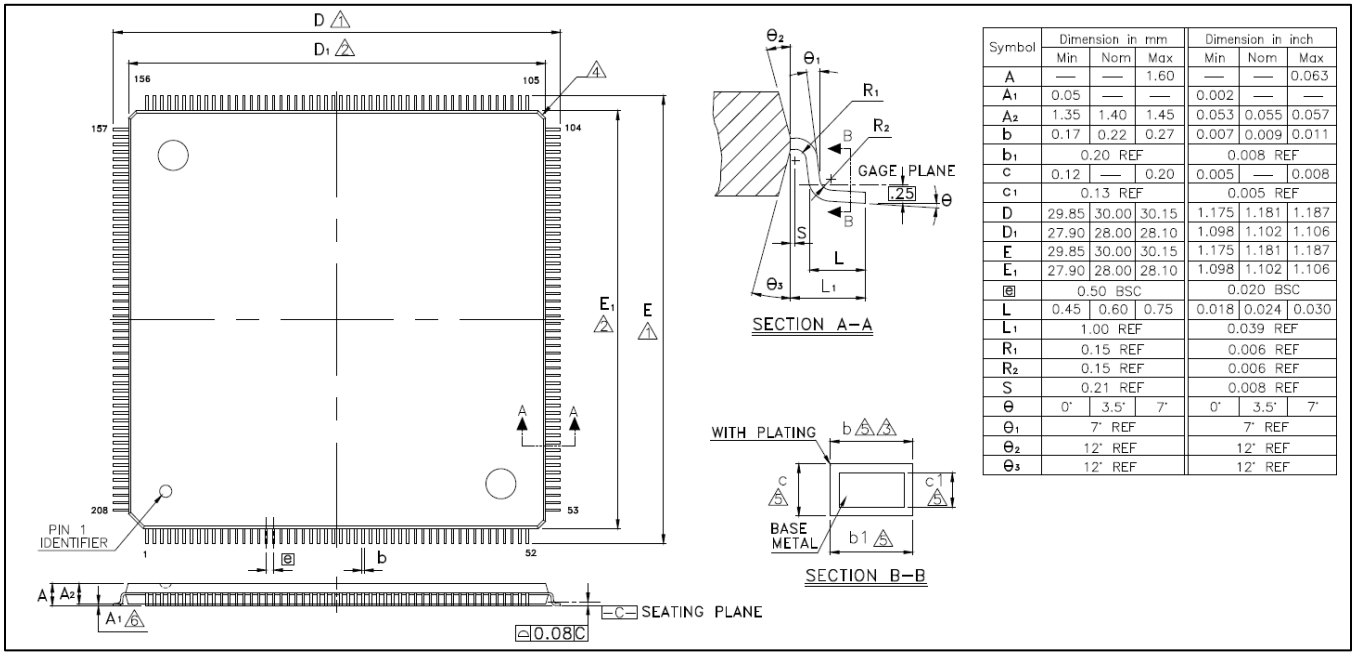


NOTE :

1. CONTROLLING DIMENSION : MILLIMETER.
2. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.
4. SPECIAL CHARACTERISTICS C CLASS: ccc & ddd (SPIL STANDARD).
5. THE PATTERN OF PIN 1 FIDUCIAL IS FOR REFERENCE ONLY.
6. BALL PLACEMENT USE 0.300 mm SOLDER BALL. BGA PAD SOLDER MASK OPENING = 0.275 mm.

NSING Technologies Pte. Ltd.
Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

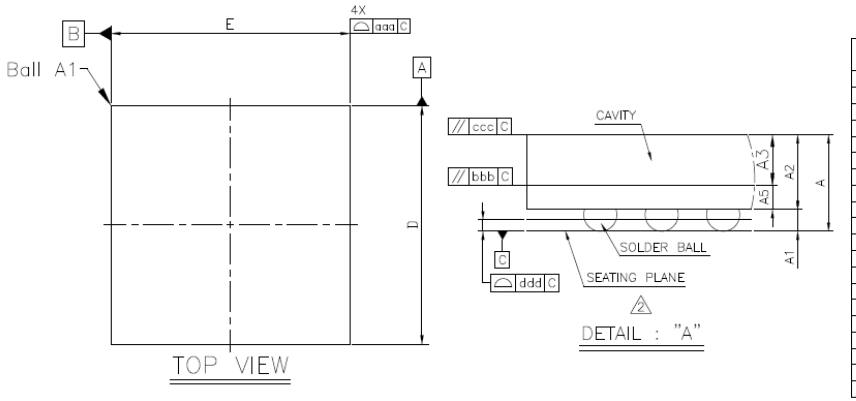
5.3 LQFP208 Package Size



Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	—	—	1.60	—	—	0.063
A1	0.05	—	—	0.002	—	—
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.17	0.22	0.27	0.007	0.009	0.011
b1	0.20 REF			0.008 REF		
c	0.12	—	0.20	0.005	—	0.008
c1	0.13 REF			0.005 REF		
D	29.85	30.00	30.15	1.175	1.181	1.187
D1	27.90	28.00	28.10	1.098	1.102	1.106
E	29.85	30.00	30.15	1.175	1.181	1.187
E1	27.90	28.00	28.10	1.098	1.102	1.106
e	0.50 BSC			0.020 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
R1	0.15 REF			0.006 REF		
R2	0.15 REF			0.006 REF		
S	0.21 REF			0.008 REF		
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	7° REF			7° REF		
θ2	12° REF			12° REF		
θ3	12° REF			12° REF		

NSING Technologies Pte. Ltd.
Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

5.4 TFBGA240+25 Package Size

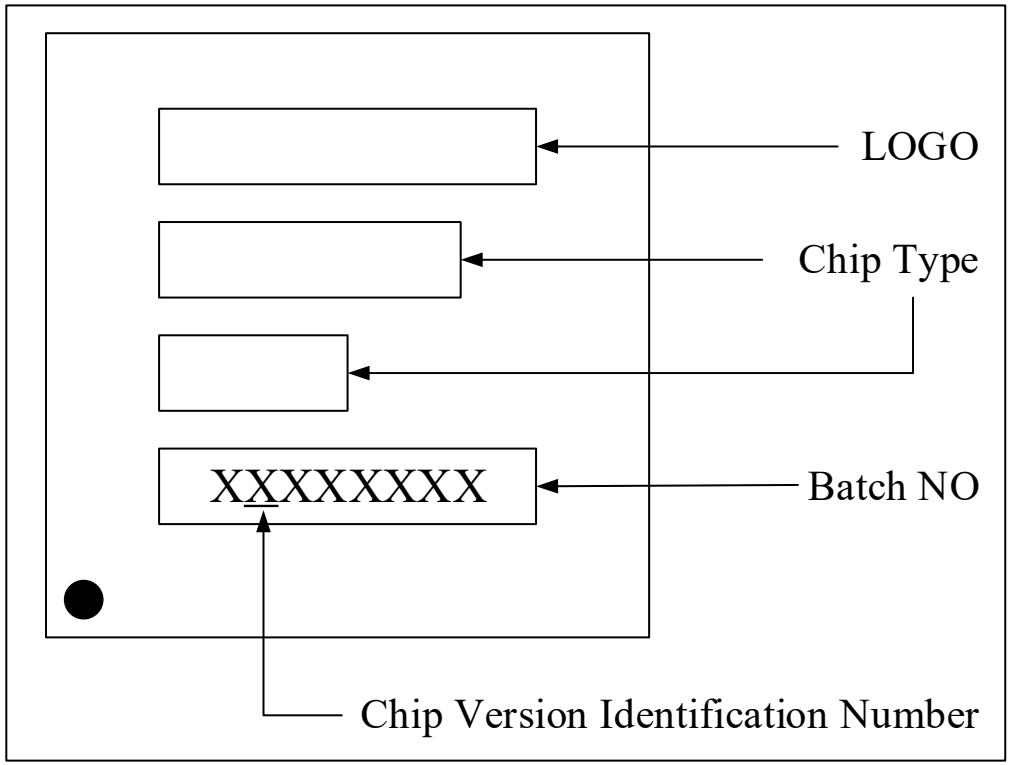


Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.009	1.090	1.171	0.040	0.043	0.046
A1	0.250	0.300	0.350	0.010	0.012	0.014
A2	0.726	0.790	0.854	0.029	0.031	0.034
A3	0.480	0.530	0.580	0.019	0.021	0.023
A5	0.220	0.260	0.300	0.009	0.010	0.012
E	13.900	14.000	14.100	0.547	0.551	0.555
D	13.900	14.000	14.100	0.547	0.551	0.555
E1	---	12.800	---	---	0.504	---
D1	---	12.800	---	---	0.504	---
e	---	0.800	---	---	0.031	---
b	0.360	0.410	0.460	0.014	0.016	0.018
aaa		0.150			0.006	
bbb		0.100			0.004	
ccc		0.100			0.004	
ddd		0.130			0.005	
eee		0.150			0.006	
fff		0.080			0.003	
MD/ME		17/17				
SE		0.800			0.031	
SD		0.800			0.031	

NSING Technologies Pte. Ltd.
Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

5.5 Silk Screen Description

Figure 0-1 Silk Screen Diagram



NSING Technologies Pte. Ltd.
Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

6 Verson History

Version	Date	Changes
V1.0.0	2025.05.20	First release

NSING Technologies Pte. Ltd.
Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg

7 Disclaimer

This document is the exclusive property of NSING TECHNOLOGIES PTE. LTD. (Hereinafter referred to as NSING). This document, and the product of NSING described herein (Hereinafter referred to as the Product) are owned by NSING under the laws and treaties of Republic of Singapore and other applicable jurisdictions worldwide. The intellectual properties of the product belong to Nations Technologies Inc. and Nations Technologies Inc. does not grant any third party any license under its patents, copyrights, trademarks, or other intellectual property rights. Names and brands of third party may be mentioned or referred thereto (if any) for identification purposes only. NSING reserves the right to make changes, corrections. enhancements, modifications, and improvements to this document at any time without notice. Please contact NSING and obtain the latest version of this document before placing orders. Although NATIONS has attempted to provide accurate and reliable information, NATIONS assumes no responsibility for the accuracy and reliability of this document. It is the responsibility of the user of this document to properly design, program, and test the functionality and safety of any application made of this information and any resulting product. In no event shall NATIONS be liable for any direct, indirect, incidental, special, exemplary, or consequential damages arising in any way out of the use of this document or the Product. NATIONS Products are neither intended nor warranted for usage in systems or equipment, any malfunction or failure of which may cause loss of human life, bodily injury or severe property damage. Such applications are deemed, Insecure Usage'. Insecure usage includes, but is not limited to: equipment for surgical implementation, atomic energy control instruments, airplane or spaceship instruments, all types of safety devices, and other applications intended to supporter sustain life. All Insecure Usage shall be made at user's risk. User shall indemnify NATIONS and hold NATIONS harmless from and against all claims, costs, damages, and other liabilities, arising from or related to any customer's Insecure Usage Any express or implied warranty with regard to this document or the Product, including, but not limited to. The warranties of merchantability, fitness for a particular purpose and non-infringement are disclaimed to the fullest extent permitted by law. Unless otherwise explicitly permitted by NATIONS, anyone may not use, duplicate, modify, transcribe or otherwise distribute this document for any purposes, in whole or in part.

NSING Technologies Pte. Ltd.
Address: 20 Science Park, #03-15/16
Teleteck Park, East Wing, Singapore 117674
Email: sales@nsing.com.sg