N32H762 Product Brief

N32H762 series uses an ARM Cortex-M7 core, operating at frequencies up to 600MHz, supporting double-precision floating-point calculations and DSP instructions. It features (2/4MB) of on-chip FLASH, integrates up to 1504KB of SRAM (including 1024KB TCM SRAM and 480KB SRAM) + 4KB Backup SRAM. It integrates 3 12-bit 5Msps ADCs, 4 high-speed comparators, 6 12-bit DACs, multiple high-speed U(S)ARTs, I2C, xSPI, SPI, USBFS Dual Role, USBHS Dual Role, CAN-FD, SDRAM, FEMC, SDMMC, and 10/100/1000M Ethernet communication interfaces. It supports Digital Camera Interface (DVP), TFT-LCD graphical interface, JPEG hardware codec, and GPU. It has a built-in high-performance encryption algorithm hardware acceleration engine, supporting AES/TDES, SHA algorithms, TRNG true random number generator, and CRC8/16/32. It supports up to 166 GPIOs, with package types including LQFP176, UFBGA176+25, LQFP208, and TFBGA240+25 packages.

Key Features

- **Core CPU**
  - 32-bit ARM Cortex-M7 core with double-precision floating-point unit, supporting DSP instructions and MPU
  - Built-in 32KB instruction cache and 32KB data cache with ECC
  - Maximum clock frequency of 600MHz, 1284 DMIPS
- **Encrypted Memory**
  - 2M/4M Byte on-chip Flash, supporting encrypted storage with automatic decryption during program execution
  - 1504KB built-in SRAM with ECC verification
    - 1024KB TCM SRAM, configurable as D-TCM, I-TCM, or SRAM
    - 480KB on-chip SRAM
- **Operating Modes**
  - Run mode
  - SLEEP mode: AXI enabled, AHB enabled
  - Stop0 mode: SRAM, TCM, RTC, LSE, IWDG enabled
  - Stop2 mode: Flash in standby mode; SRAM, TCM, RTC, LSE, IWDG, Backup SRAM, backup registers enabled; I/O state preserved
  - Standby mode: Backup SRAM, RTC, IWDG, LSE, backup registers enabled; SRAM, TCM disabled
  - VBAT mode: Backup SRAM, RTC, LSE, backup registers enabled
- **Clock System**
  - 4MHz~48MHz external high-speed crystal
  - 4MHz~50MHz external clock input
  - 32.768KHz external low-speed crystal
  - Built-in 3 high-speed PLLs

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- Built-in MSI clock, supporting configurable frequencies: 31.25K/62.5K/125K/250K/500K/1M/2M/4M/8M/16MHz
- Internal high-speed RC 64MHz
- Internal low-speed RC 32KHz

- **Reset**
  - Power-on/power-down/external pin reset support
  - Watchdog reset and software system reset support
  - Programmable voltage detection
- **High-Speed Communication Interfaces**
  - 8 USART interfaces/7 UART interfaces, supporting ISO7816, IrDA, LIN
  - 2 LPUART interfaces
  - 7 SPI interfaces, supporting master/slave modes, up to 50 MHz
  - 10 I2C interfaces, up to 3.4 MHz, configurable master/slave modes, dual address response in slave mode
  - 1 USBHS Dual Role interface with built-in high-speed PHY
  - 1 USBFS Dual Role interface
  - 4 CAN-FD bus interfaces
  - 2 Ethernet MAC interfaces: ETH1 supports 10M/100M/1000M communication rates, ETH2 supports 10M/100M rates, both support IEEE 1588 time synchronization protocol
- **High-Performance Analog Interfaces**
  - 3 12-bit 5Msps ADCs, supporting 12-bit, 10-bit resolution, hardware oversampling up to 16-bit, up to 55 external single-ended input channels, 5 internal single-ended input channels, supporting single-ended mode and differential mode
  - 4 high-speed analog comparators
  - 6 12-bit DACs: 2 1Msps DACs support buffered and unbuffered external output, internal output only supports unbuffered mode; simultaneous internal and external output requires buffer; 4 additional DACs support only internal chip output with 15Msps sampling rate, unbuffered output
  - 2 MCO outputs, configurable to output SYSCLK, HSE, MSI, LSE, LSI, HSI64, or PLL clock division
  - Support for 1 reference voltage VREFBUF (configurable to 1.5V/1.8V/2.048V/2.5V)
  - 1 temperature sensor
- **Audio Interfaces**
  - 4 I2S interfaces, supporting master/slave modes, audio sampling frequencies from 8KHz to 192KHz
  - 8 PDM digital microphone interfaces built into the DSMU

1 **Memory Expansion Interfaces**

- 1 FEMC (Flexible External Memory Controller) interface, 100 MHz bus rate, SRAM/PSRAM/NOR Flash supporting configurable 16/32-bit data width, NAND Flash supporting configurable 8/16-bit data width
- 1 xSPI interface, supporting 1/2/4/8-bit data width, master/slave configurable, up to 133 MHz, usable for external SRAM, PSRAM, and Flash expansion, supporting XIP

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- 1 SDRAM interface, up to 133 MHz
- 2 SDMMC interfaces, supporting SD/SDIO 3.0, eMMC 4.51 format, up to 104MHz

- **Image Processing Interfaces**
  - 2 digital camera interfaces (DVP), supporting 8/10/12/16-bit, up to 110MHz
  - 1 TFT-LCD display interface, supporting up to 24-bit parallel digital RGB LCD with all signal interfaces, direct connection to various LCD and TFT panels, resolution up to 1920x1080
  - Built-in 2.5D graphics processor, supporting image scaling, rotation, mixing, anti-aliasing, texture mapping, etc.
  - Hardware JPEG encoder/decoder
- **GPIO and Control Features**
  - Maximum support for 166 GPIOs, low-speed GPIOs supporting 5V voltage tolerance (under VDD = 3.3V ±10% condition)
  - Motor control Cordic accelerator, supporting trigonometric and hyperbolic functions acceleration, supporting floating-point input and output
  - Delta Sigma Module Unit (DSMU)
  - Built-in filtering algorithm accelerator FMAC, supporting FIR, IIR filtering
  - 3 high-speed DMA controllers, each supporting 8 channels, 1 MDMA supporting 16 channels, freely configurable channel source and destination addresses
- **Real-Time Clock and Timers**
  - RTC real-time clock, supporting leap year perpetual calendar, alarm events, periodic wakeup, internal/external clock calibration
  - Timer counters:
  - 2 16-bit ultra-high precision timer counters (SHRTIM1/SHRTIM2), highest control precision 100ps, each with 1 master timer and 6 16-bit slave timer units. Each timer unit has 2 independent channels, supporting 12 independent PWM outputs or 6 pairs of complementary PWM outputs
  - 4 16-bit advanced timer counters, supporting input capture, complementary output, quadrature encoding input, etc., highest control precision 3.3ns; each timer has 6 independent channels, 4 of which support 4 pairs of complementary PWM output
  - 10 16-bit general-purpose timers (GTIMA13), each with 4 independent channels, supporting input capture, output compare, PWM generation
  - 4 32-bit basic timer counters (BTIM1~4)
  - 5 16-bit low-power timers (LPTIM1~5), operational in Stop2 mode
  - 1x 24-bit SysTick, 1x 14-bit window watchdog (WWDG), 1x 12-bit independent watchdog (IWDG)
- **Programming Methods**
  - Support for SWD/JTAG online debugging interfaces
  - Support for USB, UART Bootloader
- **Security Features**

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- FLASH has up to 4 encryption partitions, supporting storage encryption
- Support for write protection (WRP), multiple read protection (RDP) levels (L0/L1/L2)
- Built-in cryptographic algorithm hardware acceleration engine, supporting AES/TDES, SHA, SM4 algorithms
- TRNG true random number generator, CRC8/16/32 calculation
- Support for secure boot, encrypted program download, secure update, external high-speed and low-speed clock failure detection
- Support for tamper detection

- **128-bit UCID supported in OTP condition**
- **Operating Conditions**
  - Operating voltage range: 2.3V~3.6V
  - Chip junction temperature range: -40°C to 125°C
- **Certification**
  - USB IF
  - IEC61508 SIL2
- **Packages**
  - LQFP176(24mm x 24mm)
  - UFBGA176+25(10mm x 10mm)
  - LQFP208(28mm x 28mm)
  - TFBGA240+25(14mm x 14mm)
- **Ordering Models**

Series	Model
N32H762xxx7	N32H762IKL7, N32H762IIL7, N32H762IKB7, N32H762IIB7, N32H762BKL7, N32H762BIL7, N32H762XKB7, N32H762XIB7

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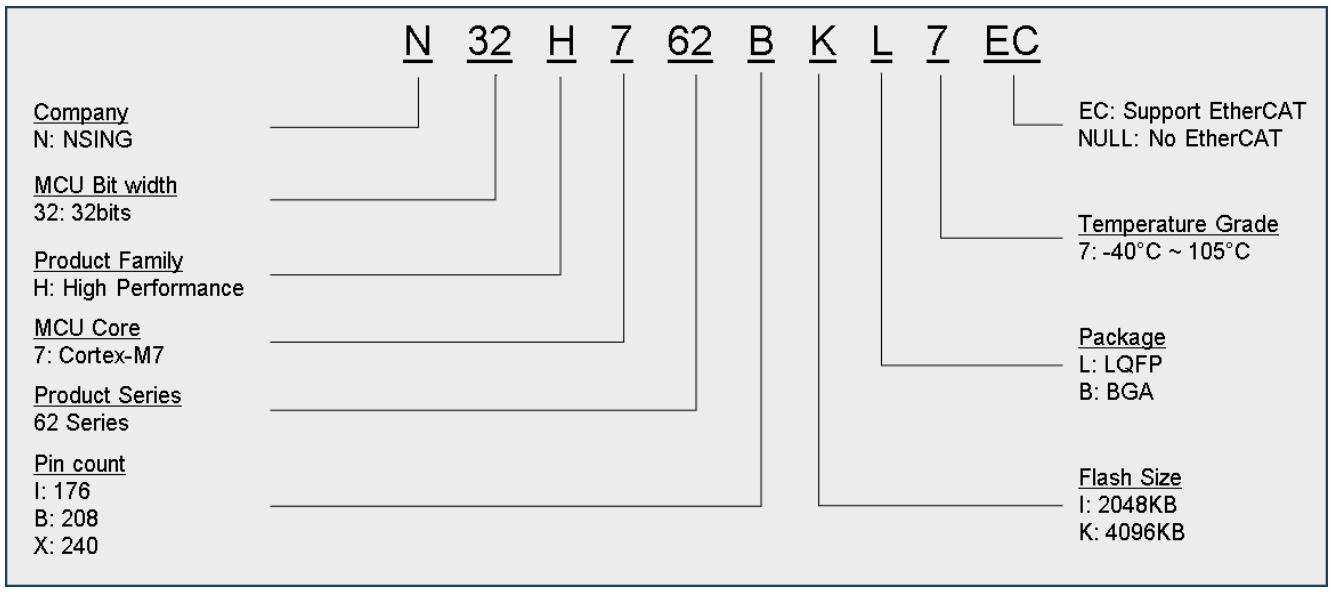
Naming Convention



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Product Model Resource Configuration

Table 0-1 N32H762 Series Resource Configuration

DeviceModel		N32H762 IKL7	N32H762 IIL7	N32H762 IKB7	N32H762 IIB7	N32H762 BKL7	N32H762 BIL7	N32H762 XKB7	N32H762 XIB7
Flash（KB）		4096	2048	4096	2048	4096	2048	4096	2048
SRAM（KB）	TCM	1024							
	System RAM	480							
	Backup RAM	4							
Core	M7	600MHz							
Operating Voltage		2.3V~3.6V							
Coprocessors	Cordic	Yes							
	DSMU	Yes							
	FMAC	Yes							
Timers	SHRTIM	2							
	ADTIM	4							
	GPTIM	10							
	BSTIM	4							
	LPTIM	5							
	SysTick timer	1							
	WWDG	1*14bit							
	IWDG	1*12bit							
	RTC	Yes							
Communication Interfaces	SPI/I2S	7/4							
	I2C	10							
	USART	7				8			
	UART	7							
	LPUART	2							
	USBHS Dual Role	1							
	USBFS Dual Role	1							
	CAN FD	4							
	10/100M ETH	1							
	10/100/1000M ETH	1							
Expanded Storage	SDRAM	Yes							
	xSPI	1							
	FEMC	Yes							
	SDMMC	2							
Analog	12bit ADC	3							
	12bit DAC	2+4(1) 2 External channels							

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	Number of channels				
	比较器	4			
	VREFBUF	Yes			
Imaging	LCDC	Yes			
	GPU	Yes			
	JPEG	Yes			
	DVP	2			
GPIO		138		166	
DMA Number of channels		3 24 Channel			
MDMA Number of channels		1 16 Channel			
Algorithm Support		DES/3DES, AES, SHA1/SHA224/SHA256, CRC8/16/CRC32			
Security Protection		Read/write protection (RDP/WRP), storage encryption, secure boot			
Package		LQFP176	UFBGA176+25	LQFP208	TFBGA240+25

Note： 4 DACs only support internal connection and cannot output to GPIO

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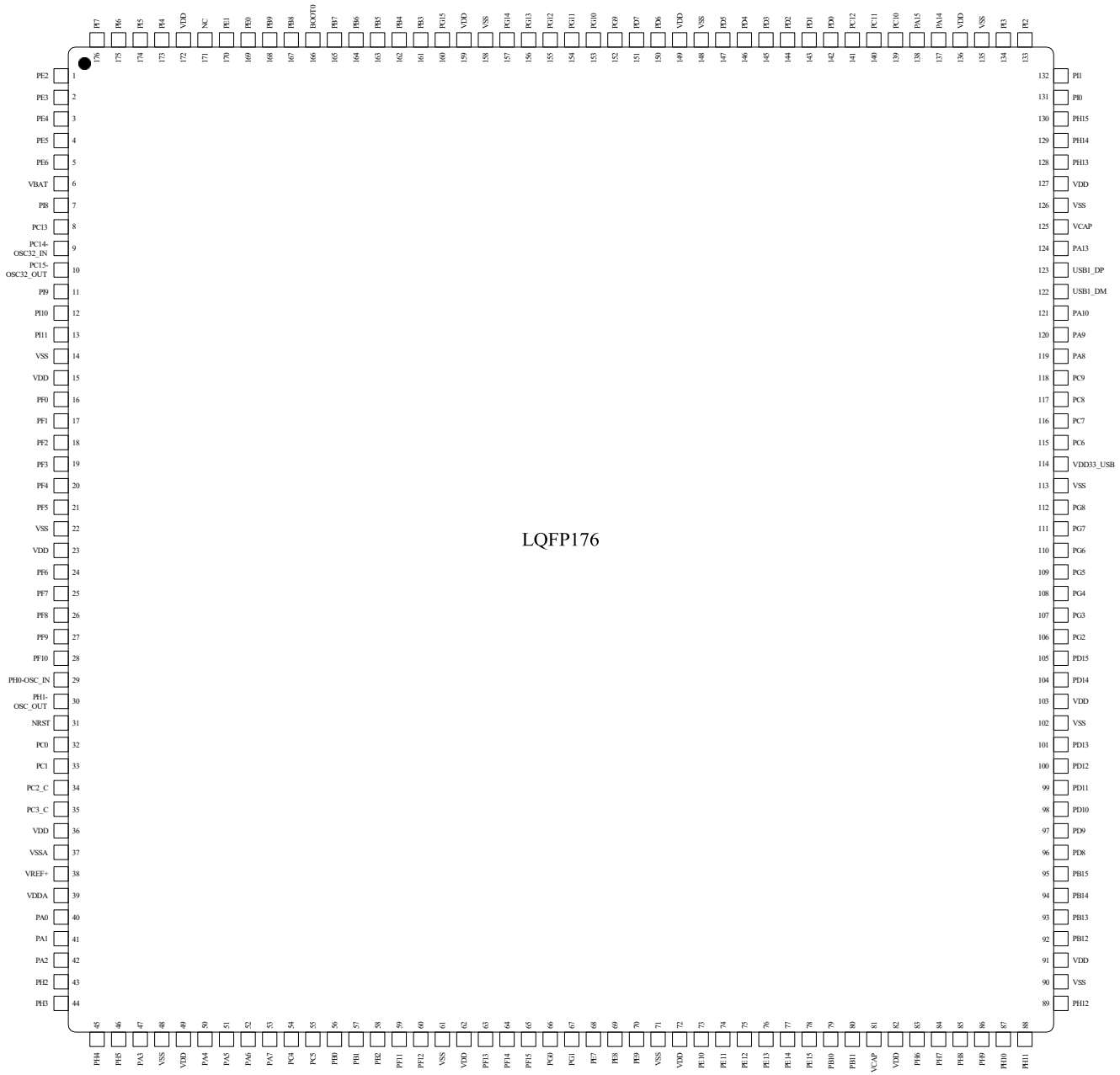
Package Information

LQFP176 Package

LQFP176 Pin Distribution



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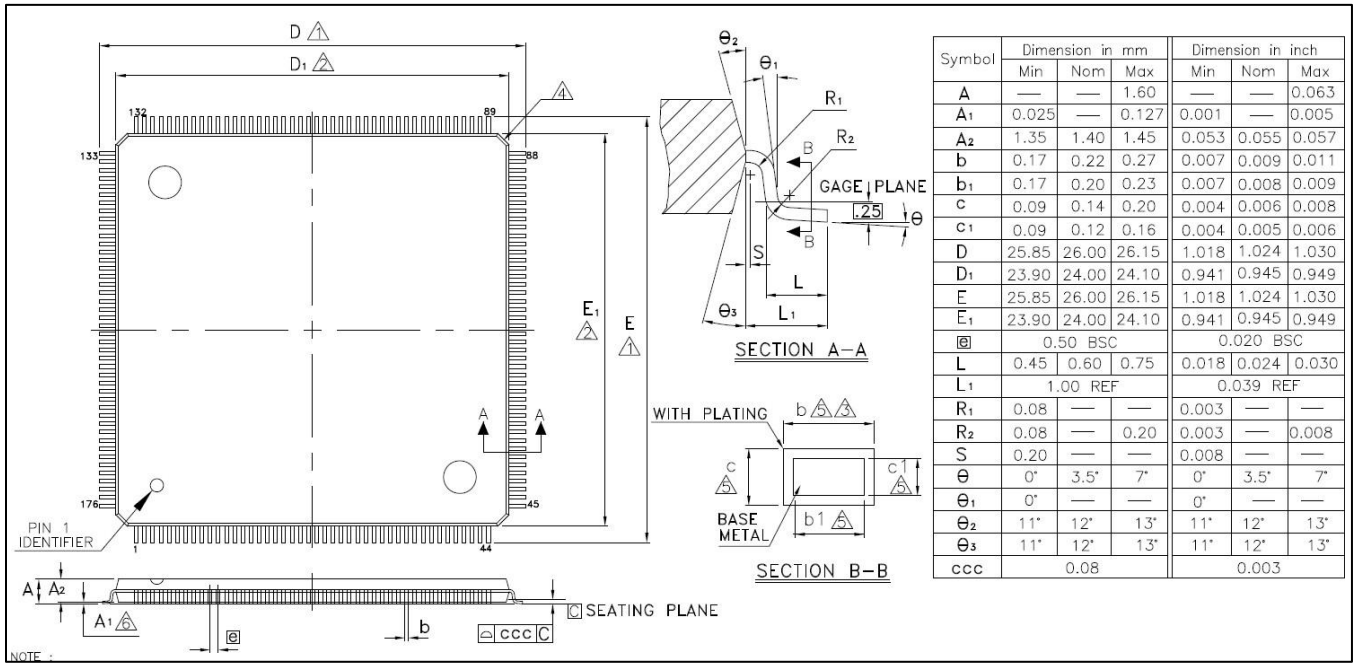
LQFP176 Package Size



Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	—	—	1.60	—	—	0.063
A_1	0.025	—	0.127	0.001	—	0.005
A_2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.17	0.22	0.27	0.007	0.009	0.011
b_1	0.17	0.20	0.23	0.007	0.008	0.009
c	0.09	0.14	0.20	0.004	0.006	0.008
c_1	0.09	0.12	0.16	0.004	0.005	0.006
D	25.85	26.00	26.15	1.018	1.024	1.030
D_1	23.90	24.00	24.10	0.941	0.945	0.949
E	25.85	26.00	26.15	1.018	1.024	1.030
E_1	23.90	24.00	24.10	0.941	0.945	0.949
e	0.50 BSC			0.020 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L_1	1.00 REF			0.039 REF		
R_1	0.08	—	—	0.003	—	—
R_2	0.08	—	0.20	0.003	—	0.008
S	0.20	—	—	0.008	—	—
θ	0°	3.5°	7°	0°	3.5°	7°
$θ_1$	0°	—	—	0°	—	—
$θ_2$	11°	12°	13°	11°	12°	13°
$θ_3$	11°	12°	13°	11°	12°	13°
ccc	0.08			0.003		

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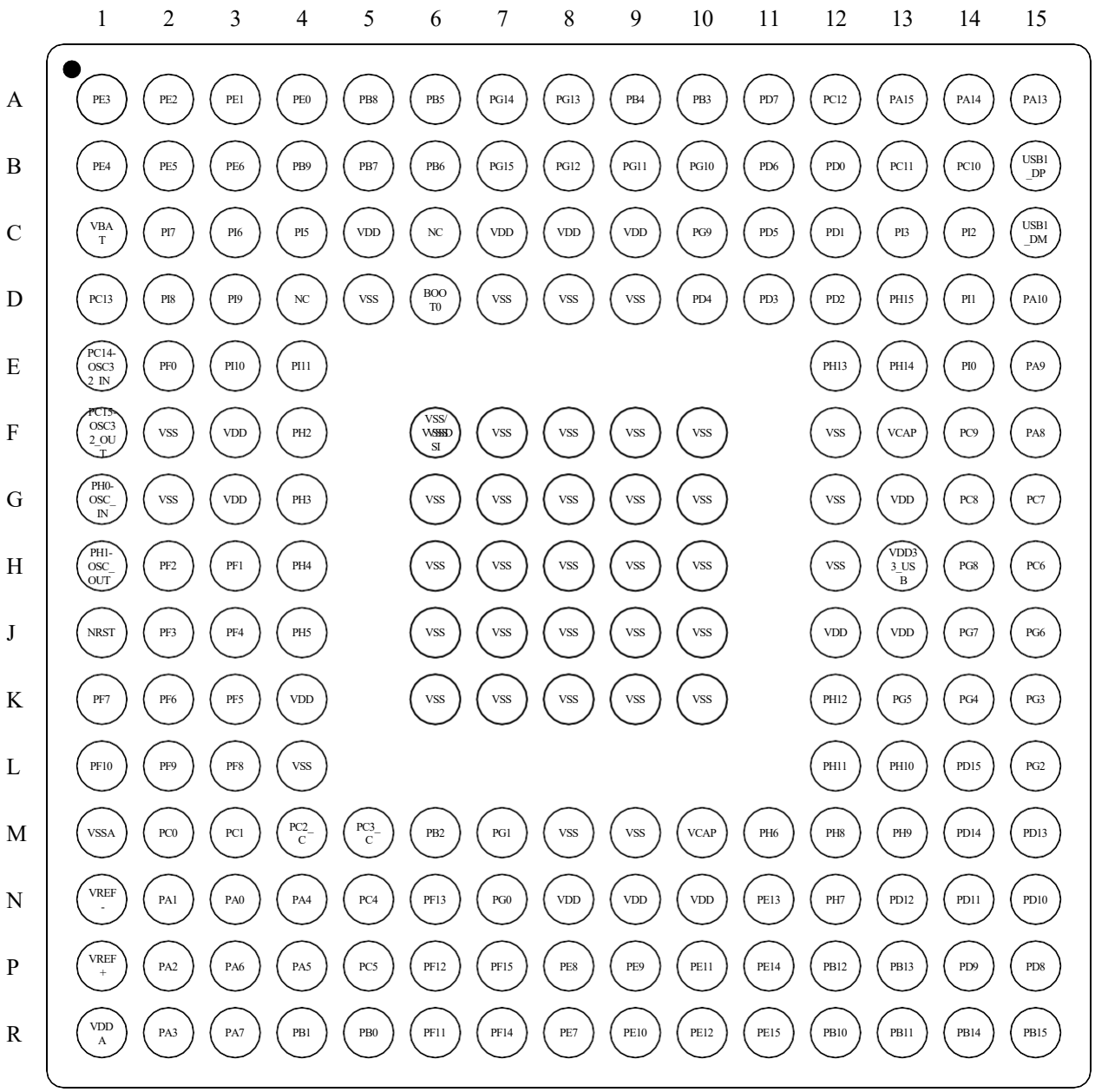
UFBGA176+25 Package

UFBGA176+25 Pin Distribution



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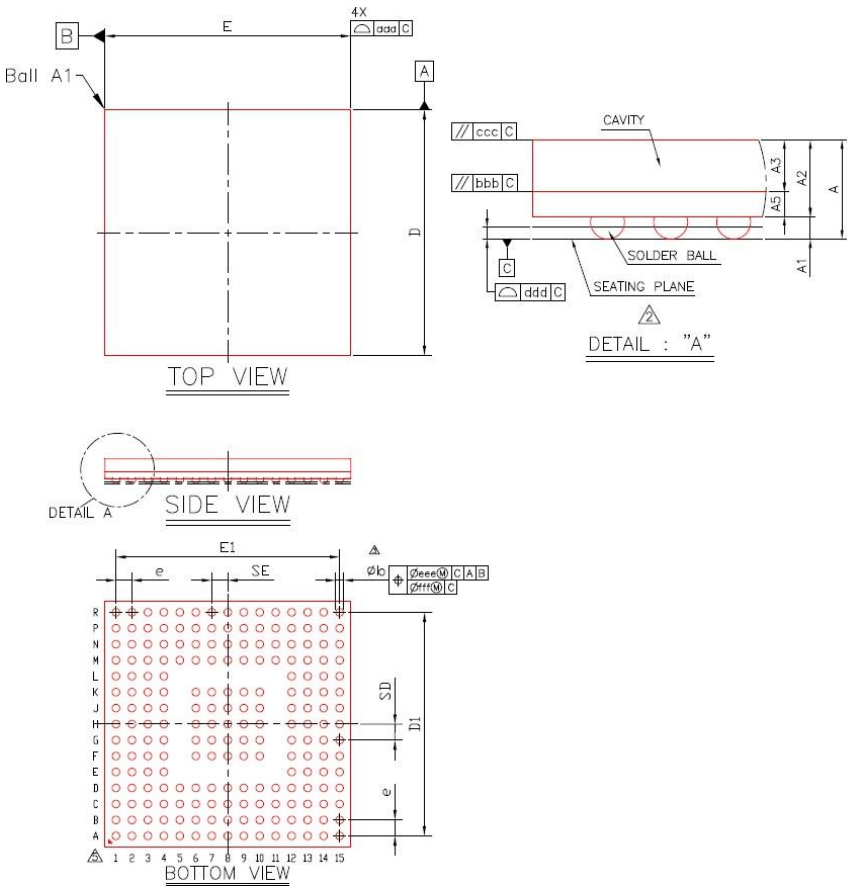
UFBGA176+25 Package Size



Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0,919	1,000	1,081	0,036	0,039	0,043
A1	0.160	0.210	0.260	0,006	0,008	0,010
A2	0,726	0,790	0,854	0,029	0,031	0,034
A3	0.480	0.530	0.580	0,019	0,021	0,023
A5	0,220	0,260	0,300	0,009	0,010	0,012
E	9.900	10.000	10.100	0.390	0.394	0.398
D	9.900	10.000	10.100	0.390	0.394	0.398
E1	—	9.100	—	—	0,358	—
D1	—	9.100	—	—	0.358	—
e	—	0,650	—	—	0,026	—
b	0.260	0.310	0.360	0.010	0.012	0.014
aaa		0.150			0,006	
bbb		0.100			0.004	
ccc		0.100			0,004	
ddd		0.100			0,004	
eee		0.150			0.006	
fff		0,080			0,003	
MD/ME		15/15				
SE		0,650			0,026	
SD		0.650			0.026	

NOTE :

1. CONTROLLING DIMENSION : MILLIMETER.
2. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.
4. SPECIAL CHARACTERISTICS C CLASS: ccc & ddd (SPIL STANDARD).
5. THE PATTERN OF PIN 1 FIDUCIAL IS FOR REFERENCE ONLY.
6. BALL PLACEMENT USE 0.300 mm SOLDER BALL. BGA PAD SOLDER MASK OPENING = 0.275 mm.

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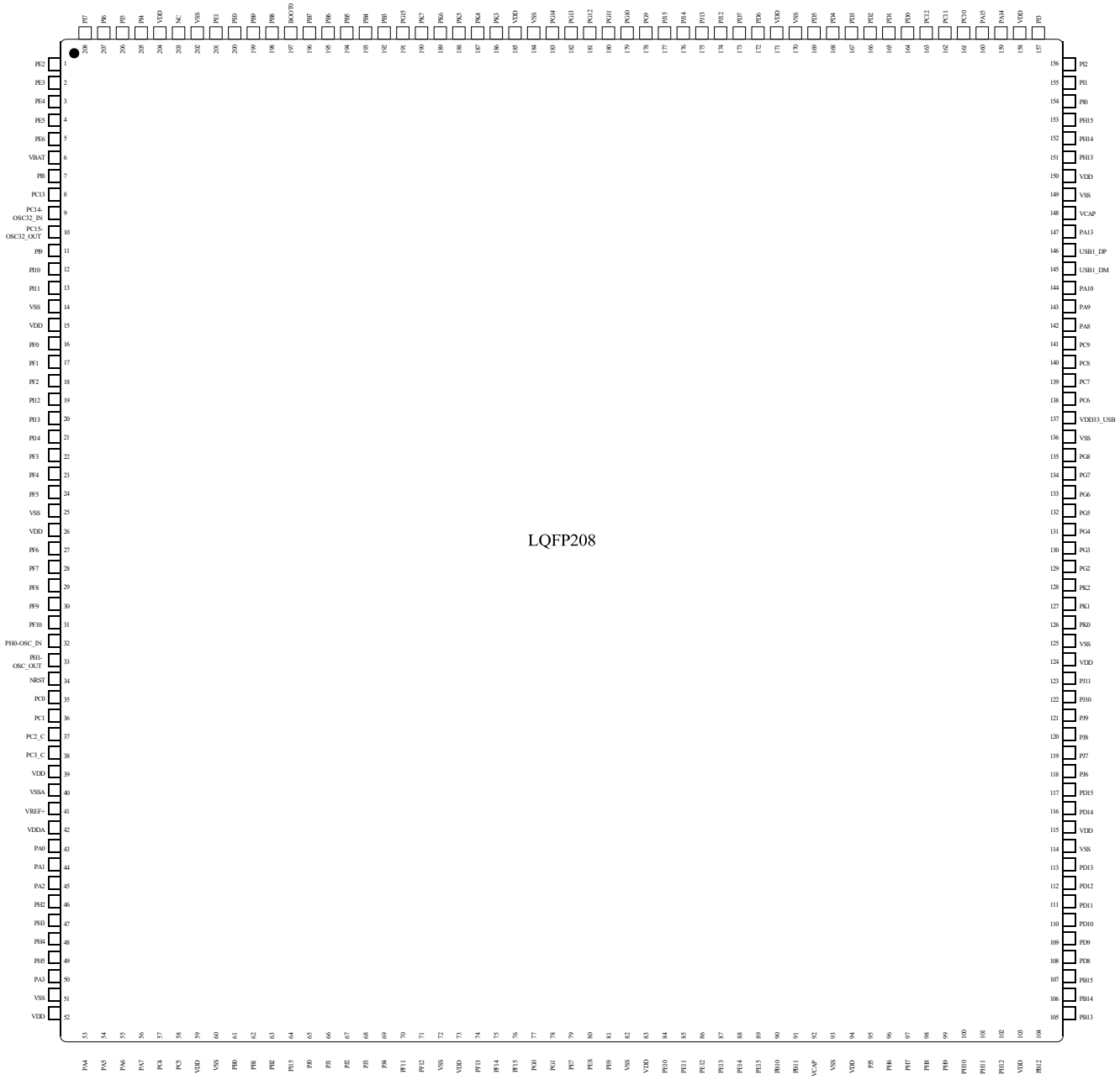
LQFP208 Package

LQFP208 Pin Distribution



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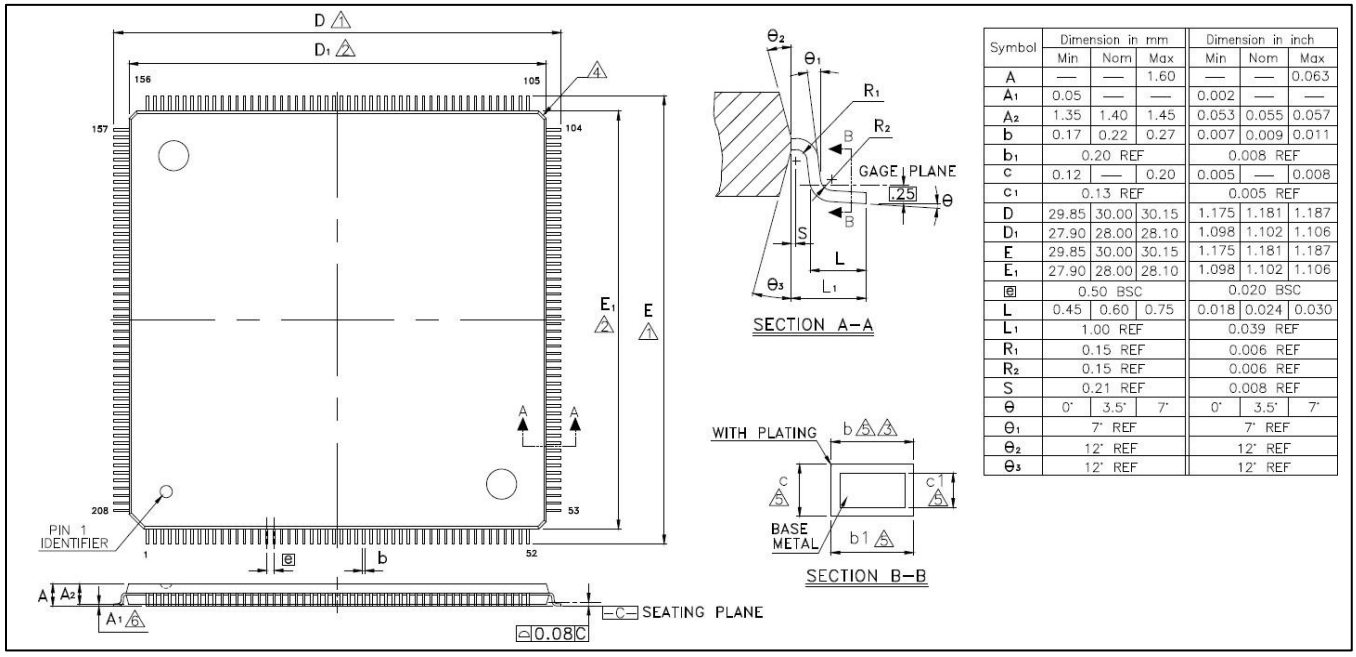
LQFP208 Package Size



Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	—	—	1.60	—	—	0.063
A1	0.05	—	—	0.002	—	—
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.17	0.22	0.27	0.007	0.009	0.011
b1	0.20 REF			0.008 REF		
c	0.12	—	0.20	0.005	—	0.008
c1	0.13 REF			0.005 REF		
D	29.85	30.00	30.15	1.175	1.181	1.187
D1	27.90	28.00	28.10	1.098	1.102	1.106
E	29.85	30.00	30.15	1.175	1.181	1.187
E1	27.90	28.00	28.10	1.098	1.102	1.106
e	0.50 BSC			0.020 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
R1	0.15 REF			0.006 REF		
R2	0.15 REF			0.006 REF		
S	0.21 REF			0.008 REF		
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	7° REF			7° REF		
θ2	12° REF			12° REF		
θ3	12° REF			12° REF		

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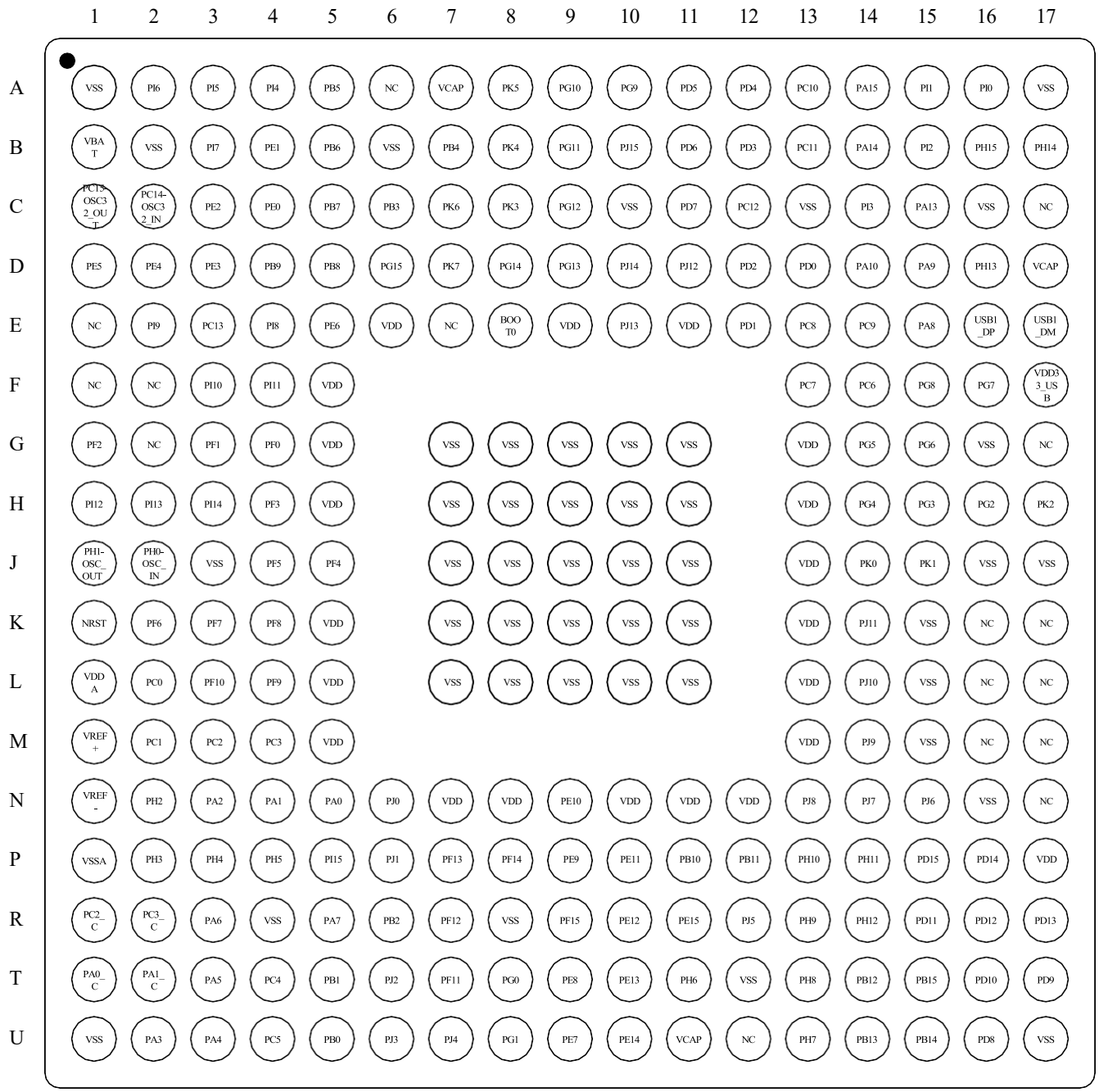
TFBGA240+25 Package

TFBGA240+25 Pin Distribution



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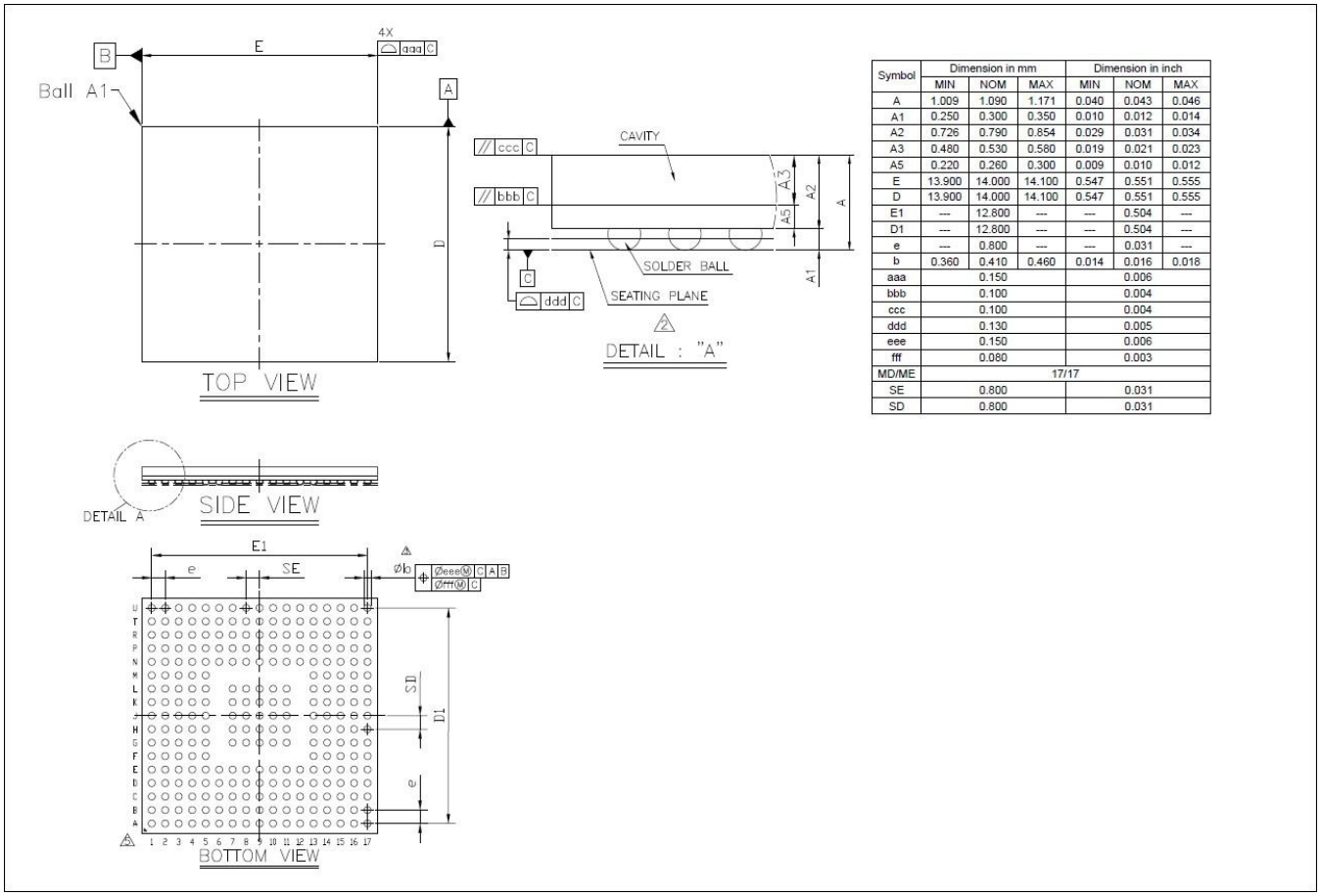
TFBGA240+25 Package Size



Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.009	1.090	1.171	0.040	0.043	0.046
A1	0.250	0.300	0.350	0.010	0.012	0.014
A2	0.726	0.790	0.854	0.029	0.031	0.034
A3	0.480	0.530	0.580	0.019	0.021	0.023
A5	0.220	0.260	0.300	0.009	0.010	0.012
E	13.900	14.000	14.100	0.547	0.551	0.555
D	13.900	14.000	14.100	0.547	0.551	0.555
E1	---	12.800	---	---	0.504	---
D1	---	12.800	---	---	0.504	---
e	---	0.800	---	---	0.031	---
b	0.360	0.410	0.460	0.014	0.016	0.018
aaa		0.150			0.006	
bbb		0.100			0.004	
ccc		0.100			0.004	
ddd		0.130			0.005	
eee		0.150			0.006	
fff		0.080			0.003	
MD/ME	17/17					
SE		0.800			0.031	
SD		0.800			0.031	

Version History

Version	Date	Changes
V1.0.0	2025.4.17	First release

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