

N32H760

Product Brief

The N32H760 series features an ARM Cortex-M7 core with a maximum operating frequency of 600MHz, supporting double-precision floating-point operations and DSP instructions. It includes (2/4MB) of on-chip FLASH and up to 1504KB of SRAM (comprising 1024KB TCM SRAM and 480KB SRAM) + 4KB Backup SRAM. It integrates three 12-bit 5Msps ADCs, four high-speed comparators, four 12-bit DACs, multiple high-speed U(S)ARTs, I2C, xSPI, SPI, USBFS Dual Role, CAN-FD, SDRAM, FEMC, SDMMC, 10/100 Ethernet communication interfaces, a digital camera interface (DVP), TFT-LCD graphical interface, JPEG hardware codec, and GPU. It also includes a high-performance hardware acceleration engine for encryption algorithms, supporting AES/TDES, and SHA as well as a TRNG true random number generator and CRC8/16/32. It supports up to 114 GPIOs and comes in TFBGA100, LQFP100, and LQFP144 package options.

Key Features

- **CPU Core**
 - 32-bit ARM Cortex-M7 core, double-precision floating-point unit, DSP instructions and MPU support
 - Built-in 32KB instruction cache and 32KB data cache with ECC
 - Maximum frequency of 600MHz, 1284 DMIPS
- **Encrypted Memory**
 - 2M/4M Byte on-chip Flash, supporting encrypted storage with automatic program decryption during execution
 - 1504KB built-in SRAM, supporting ECC verification
 - 1024KB TCM SRAM, configurable as D-TCM, I-TCM, or SRAM
 - 480KB on-chip SRAM
 - 4KB Backup SRAM, supporting ECC
- **Working Modes**
 - Run mode
 - SLEEP mode: AXI enabled, AHB enabled
 - Stop0 mode: SRAM, TCM, RTC, LSE, IWDG enabled
 - Stop2 mode: Flash in standby mode, SRAM, TCM, RTC, LSE, IWDG, Backup SRAM, backup registers enabled, I/O maintained
 - Standby mode: Backup SRAM, RTC, IWDG, LSE, backup registers enabled, SRAM, TCM closed
 - VBAT mode: Backup SRAM, RTC, LSE, backup registers enabled
- **Clock**

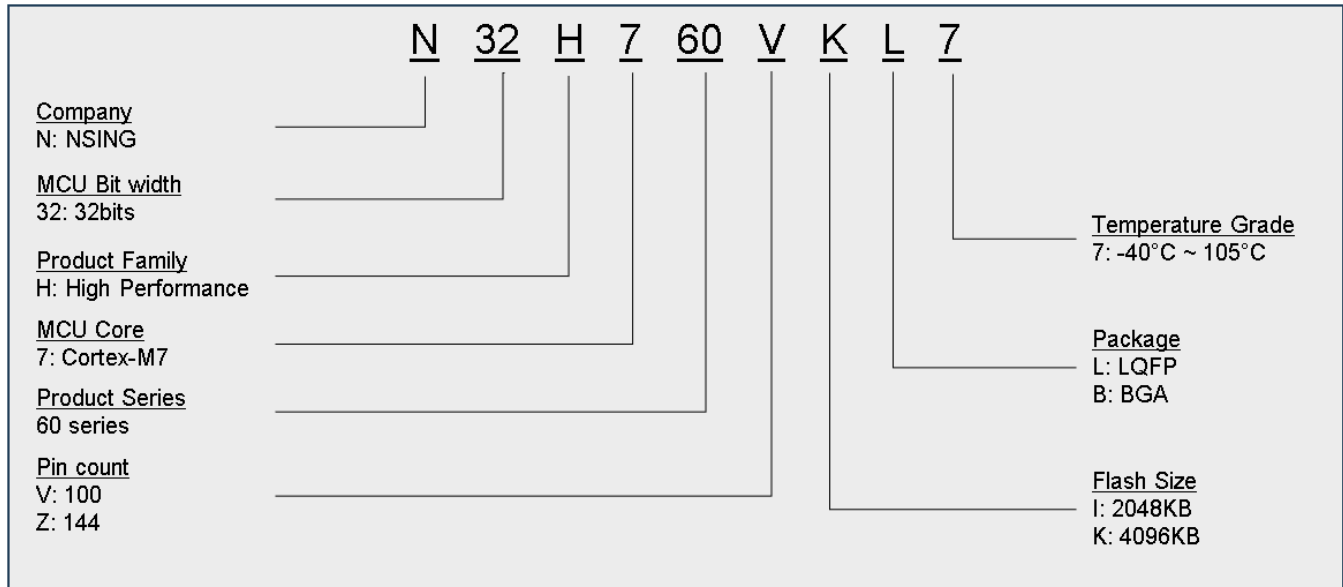
- 4MHz~48MHz external high-speed crystal
- 4MHz~50MHz external clock input
- 32.768KHz external low-speed crystal
- Three built-in high-speed PLLs
- Built-in MSI clock, supporting configurable
31.25K/62.5K/125K/250K/500K/1M/2M/4M/8M/16MHz clocks
- Internal high-speed RC 64MHz
- Internal low-speed RC 32KHz
- **Reset**
 - Supports power-on/power-down/external pin reset
 - Supports watchdog reset and software system reset
 - Supports programmable voltage detection
- **High-Speed Communication Interfaces**
 - 7 USART interfaces/5 UART interfaces, supporting ISO7816, IrDA, LIN
 - 2 LPUART interfaces
 - 6 SPI interfaces, supporting master/slave modes, speeds up to 50 MHz
 - 8 I2C interfaces, speeds up to 3.4 MHz, configurable master/slave modes, dual address response in slave mode
 - 2 USBFS Dual Role interfaces
 - 6 CAN-FD bus interfaces
 - 1 Ethernet MAC interface, supporting 10M/100M communication rates, IEEE 1588 time synchronization protocol
- **High-Performance Analog Interfaces**
 - 3 12-bit 5Msps ADCs, supporting 12-bit, 10-bit resolution, hardware oversampling to 16-bit, up to 55 external single-ended input channels, 5 internal single-ended input channels, supporting single-ended and differential modes
 - 4 high-speed analog comparators
 - 4 12-bit DACs, including 2 1Msps DACs supporting output with or without Buffer, and 2 DACs for internal chip connection only, with 15Msps sampling rate
 - 2 MCO outputs, configurable to output SYSCLK, HSE, MSI, LSE, LSI, HSI64, or PLL clock division
 - 1 reference voltage VREFBUF (configurable as 1.5V/1.8V/2.048V/2.5V)
 - 1 temperature sensor
- **Audio Interfaces**

- 4 I2S, supporting master/slave modes, audio sampling frequencies from 8KHz~192KHz
- 8 PDM digital microphone interfaces built into DSMU
- **Memory Expansion Interfaces**
 - 1 FEMC (Flexible External Memory Controller) interface, bus rate 100 MHz, SRAM/PSRAM/Nor Flash supporting 16/32-bit data width configuration, NAND Flash supporting 8/16-bit data width configuration
 - 1 xSPI interface, supporting 1/2/4/8-bit data width, configurable master/slave, speeds up to 133 MHz, usable for expanding SRAM, PSRAM, and Flash, supporting XIP
 - 1 SDRAM interface, speeds up to 133 MHz
 - 2 SDMMC interfaces, supporting SD/SDIO 3.0, eMMC 4.51 format, speeds up to 104MHz
- **Image Processing Interfaces**
 - 1 Digital Camera Interface (DVP), supporting 8/10/12/16bit, speeds up to 110MHz
 - 1 TFT-LCD display interface, supporting up to 24-bit parallel digital RGB LCD, providing all signal interfaces for direct connection to various LCD and TFT panels, resolution up to 1920x1080
 - Built-in 2.5D graphics processor, supporting image scaling, rotation, mixing, anti-aliasing, texture mapping, etc.
 - Hardware JPEG encoder/decoder
- **Up to 114 GPIOs, low-speed GPIOs support 5V tolerance (under VDD=3.3V±10% conditions)**
- **Cordic accelerator for motor control, supporting trigonometric and hyperbolic functions, floating-point input and output**
- **Delta Sigma Module Unit (DSMU)**
- **Built-in filter algorithm accelerator FMAC, supporting FIR, IIR filtering**
- **3 high-speed DMA controllers, each supporting 8 channels, 1 MDMA supporting 16 channels, configurable channel source and destination addresses**
- **RTC real-time clock, supporting leap year perpetual calendar, alarm events, periodic wake-up, internal and external clock calibration**
- **Timer Counters**
 - 2 16-bit advanced timer counters, supporting input capture, complementary output, quadrature encoder input, with precision up to 3.3ns; each timer has 6 independent channels, with 4 channels supporting 4 pairs of complementary PWM outputs
 - 10 16-bit general-purpose timers (GTIM1~10), each with 4 independent channels, supporting input capture, output compare, PWM generation
 - 4 32-bit basic timer counters (BTIM1~4)

- 5 16-bit low-power timers (LPTIM1~5), operational in Stop2 mode
- 1x 24-bit SysTick, 1x 14-bit window watchdog (WWDG), 1x 12-bit independent watchdog (IWDG)
- **Programming Methods**
 - Supports SWD/JTAG online debugging interfaces
 - Supports USB, UART Bootloader
- **Security Features**
 - FLASH has up to 4 encryption partitions, supporting storage encryption
 - Supports write protection (WRP), multiple read protection (RDP) levels (L0/L1/L2)
 - Built-in password algorithm hardware acceleration engine, supporting AES/TDES, SHA, SM4 algorithms
 - TRNG true random number generator, CRC8/16/32 operations
 - Supports secure boot, encrypted program download, secure update, external high-speed and low-speed clock failure detection
 - Supports tamper detection
- **128-bit UCID supported in OTP**
- **Working Conditions**
 - Operating voltage range: 2.3V~3.6V
 - Chip junction temperature range: -40°C~125°C
- **Certification**
 - USB IF
 - IEC61508 SIL2
- **Packages**
 - TFBGA100 (8mm x 8mm)
 - LQFP100 (14mm x 14mm)
 - LQFP144 (20mm x 20mm)
- **Ordering Models**
 - N32H760xxx7: N32H760VIB7, N32H760VKB7, N32H760VIL7, N32H760VKL7, N32H760ZIL7, N32H760ZKL7

Series	Model
N32H760xxx7	N32H760VIB7, N32H760VKB7, N32H760VIL7, N32H760VKL7, N32H760ZIL7, N32H760ZKL7

1 Naming Convention



2 Product Model Resource Configuration

Table 0-1 N32H760 Series Resource Configuration

Device Model		N32H760 VIB7	N32H760 VKB7	N32H760 VIL7	N32H760 VKL7	N32H760 ZIL7	N32H760 ZKL7
Flash（KB）		2048	4096	2048	4096	2048	4096
SRAM（KB）	TCM	1024					
	System RAM	480					
	Backup RAM	4					
Core	M7	600MHz					
Operating Voltage		2.3V~3.6V					
Coproductors	Cordic	Yes					
	DSMU	Yes					
	FMAC	Yes					
Timers	ADTIM	2					
	GPTIM	10					
	BSTIM	4					
	LPTIM	5					
	SysTick timer	1					
	WWDG	1*14bit					
	IWDG	1*12bit					
	RTC	Yes					
Communication Interfaces	SPI/I2S	5/4				6/4	
	I2C	8					
	USART	3				7	
	UART	5					
	LPUART	2					
	USBFS Dual Role	2					
	CAN FD	4					
	10/100M ETH	1					
Expanded Storage	SDRAM	No				Yes	
	xSPI	1					
	FEMC	Yes					
	SDMMC	2					
Analog	12bit ADC	3					
	12bit DAC	2+2 ⁽¹⁾					
	Number of channels	2 External channels					
	Comparator	4					
Imaging	VREFBUF	Yes					
	LCDC	Yes					
	GPU	Yes					

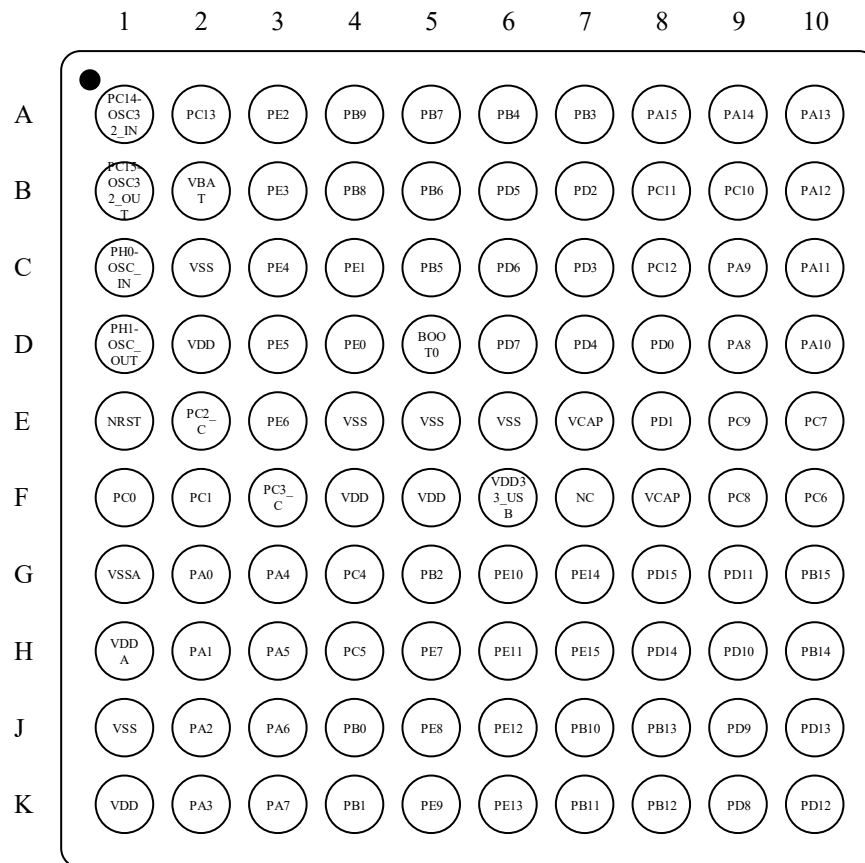
	JPEG	Yes	
	DVP	1	
GPIO		82	114
DMA Number of channels		3 24Channel	
MDMA Number of channels		1 16Channel	
Algorithm Support		DES/3DES, AES, SHA1/SHA224/SHA256, CRC8/16/CRC32	
Security Protection		Read/write protection (RDP/WRP), storage encryption, secure boot	
Package		TFBGA100	LQFP100 LQFP144

Note: 2 DACs only support internal connection and cannot output to GPIO.

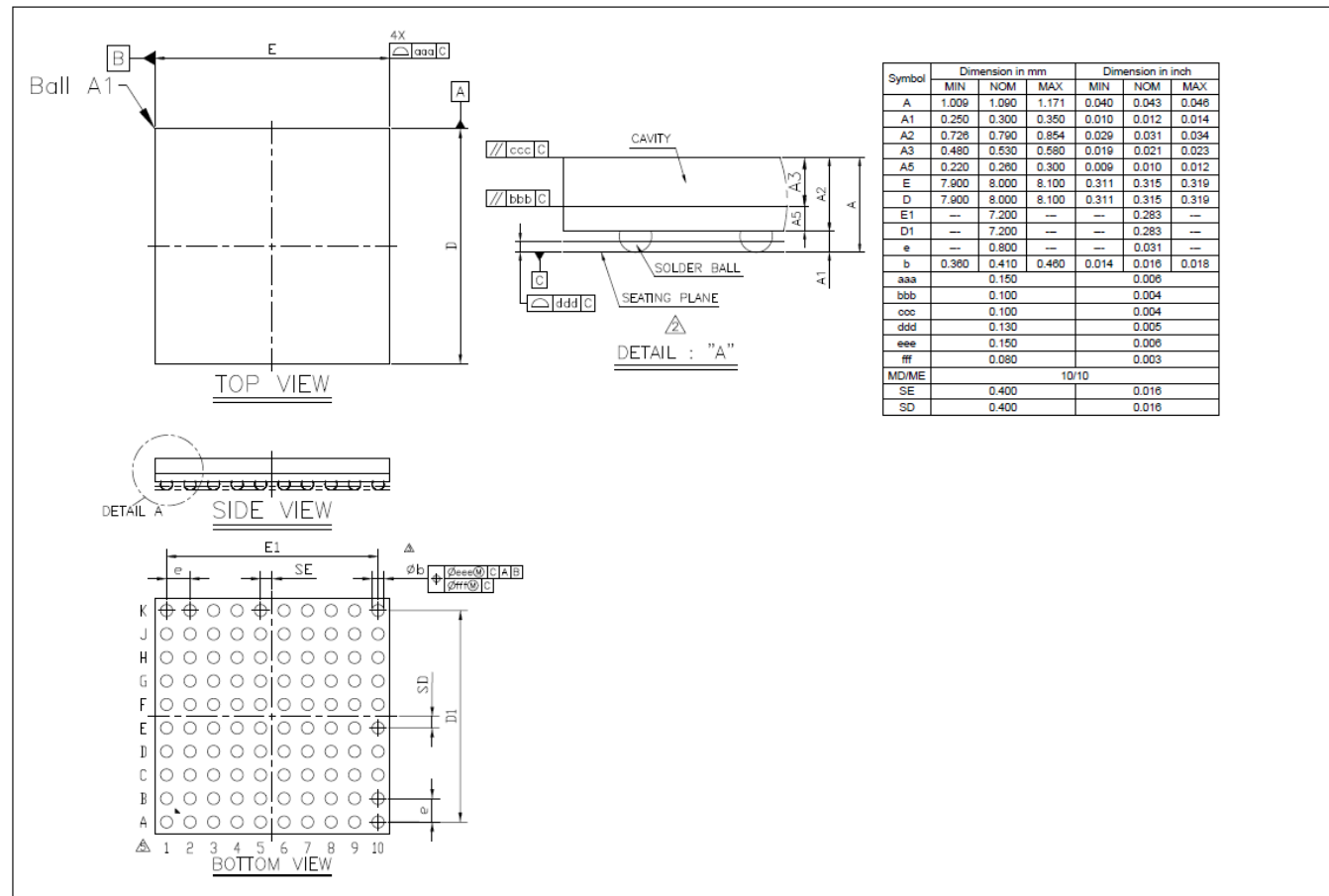
3 Package Information

TFBGA100 Package

TFBGA100 Pin Distribution

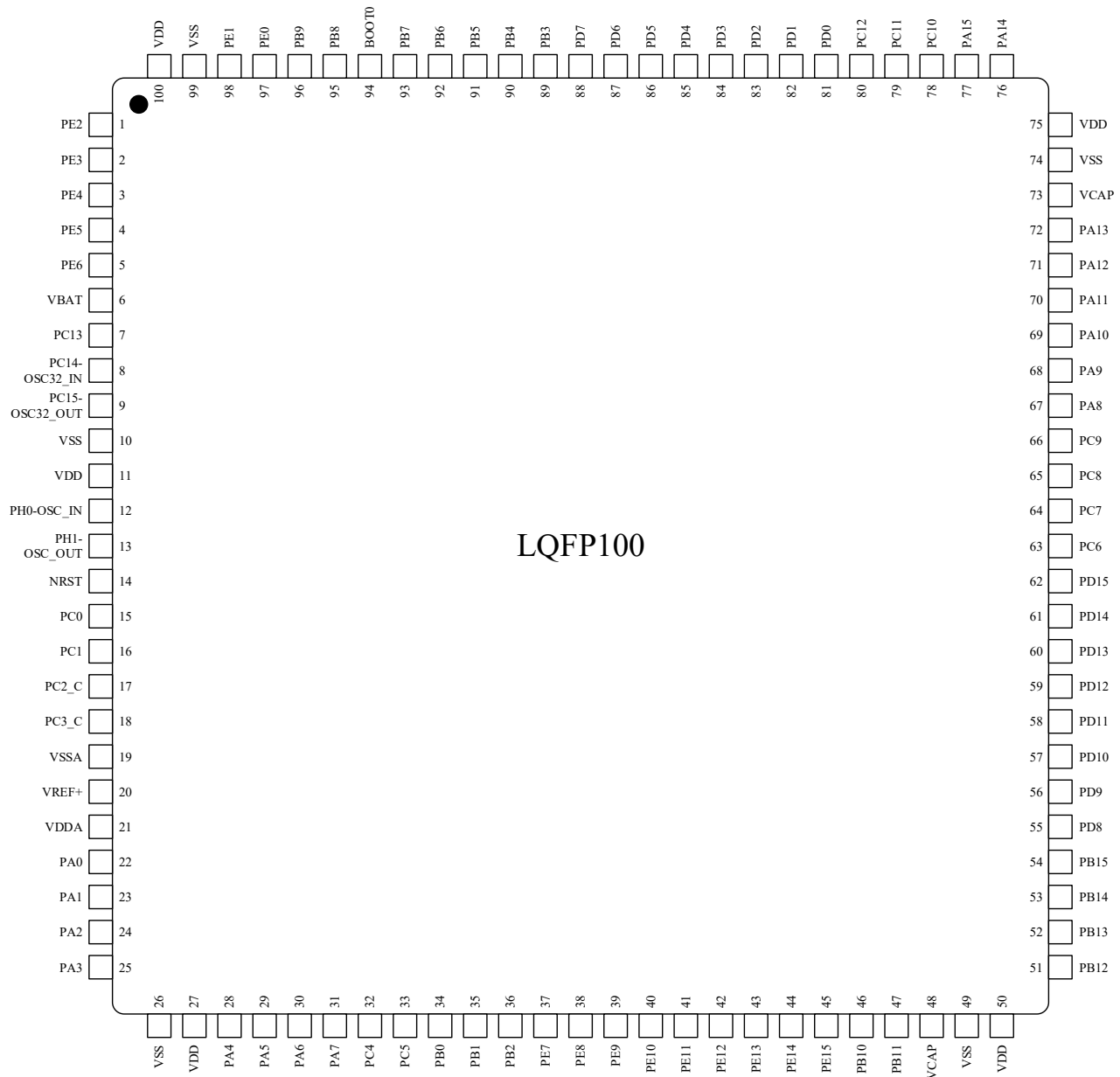


TFBGA100 Package Size

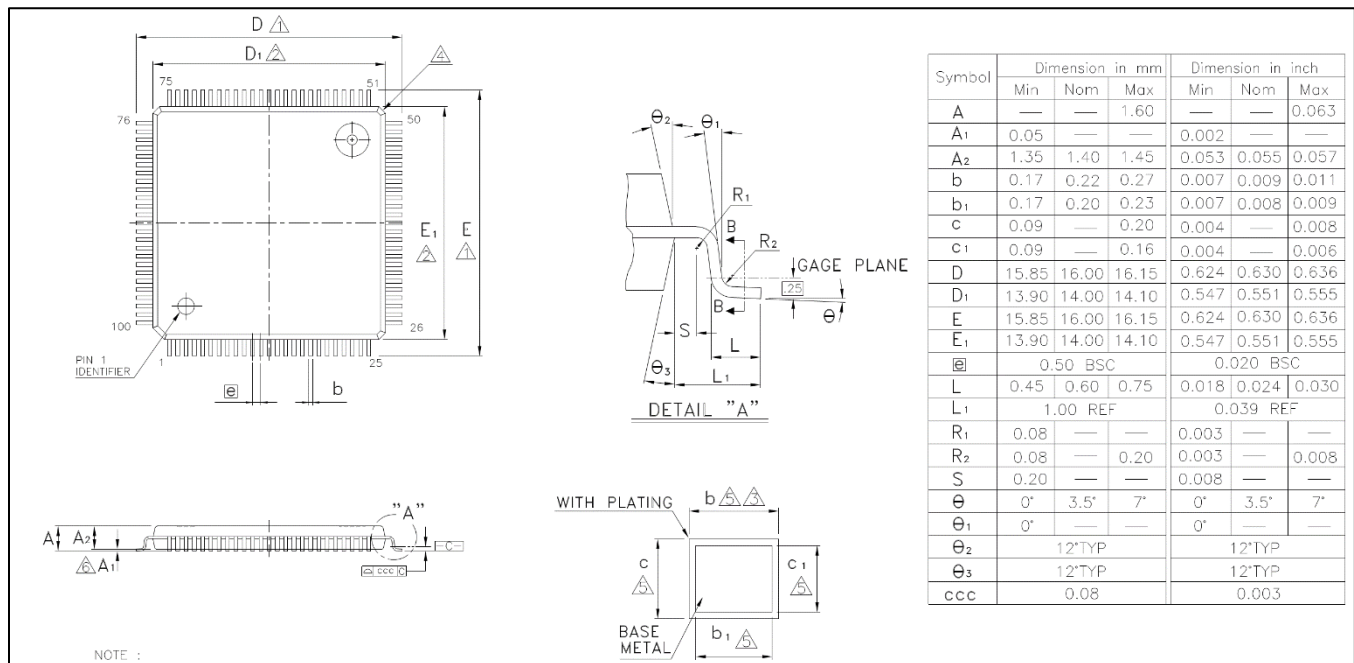


LQFP100 Package

LQFP100 Pin Distribution

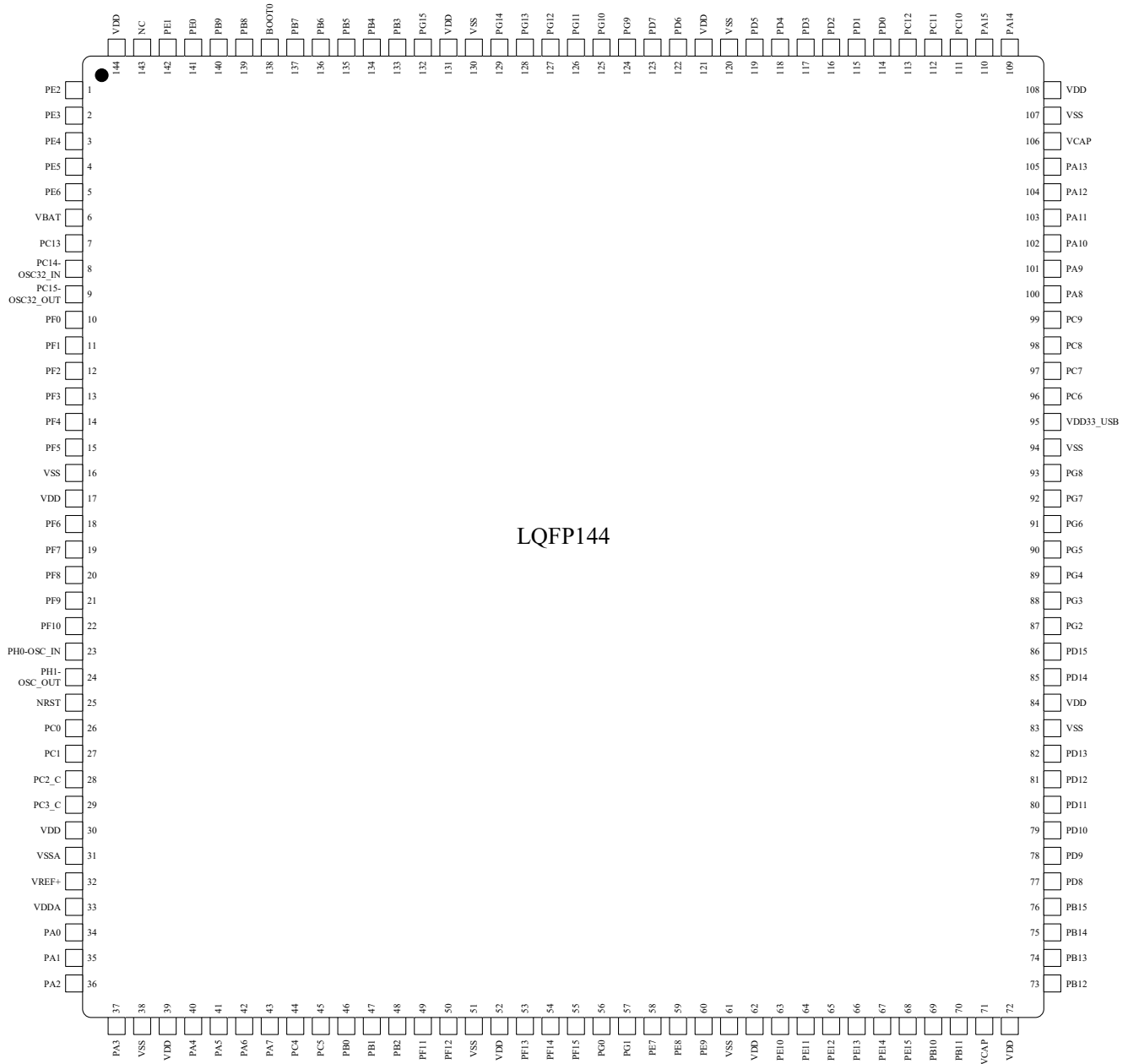


LQFP100 Package Size

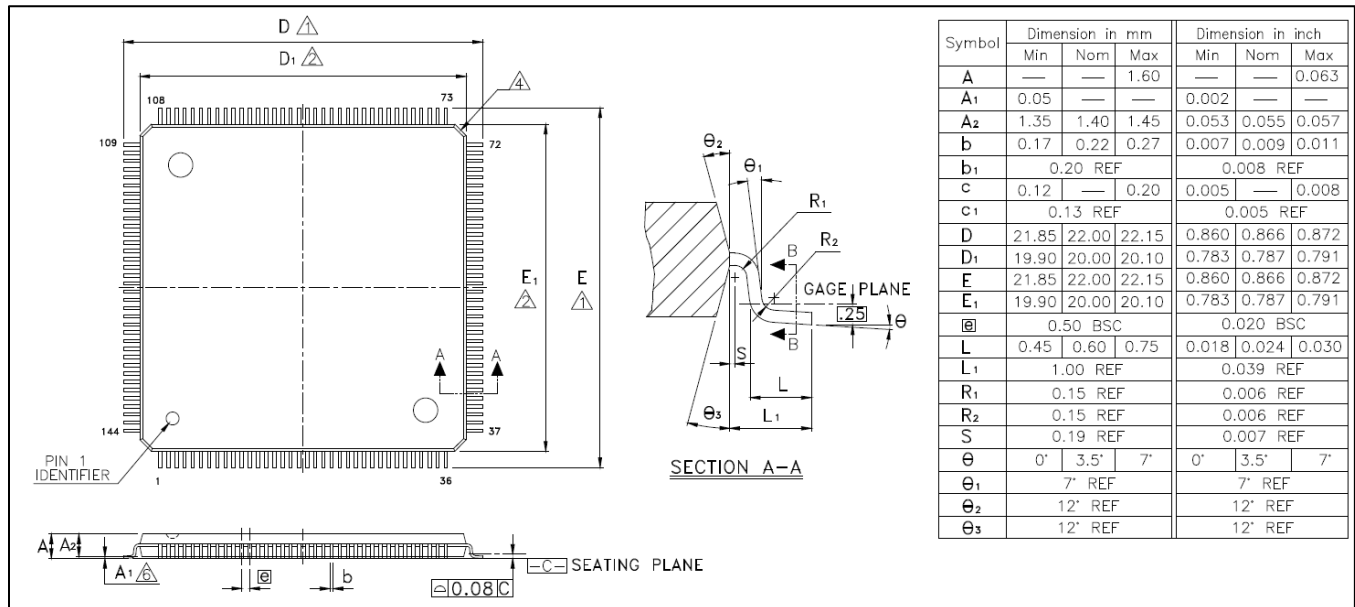


LQFP144 Package

LQFP144 Pin Distribution



LQFP144 Package Size



4 Version History

Version	Date	Changes
V1.0.0	2025.4.17	First release

5 Disclaimer

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