# N32H47x_48x Series Errata Sheet V0.7.0



**NSING Technologies Pte. Ltd.**
Add: NSING, Teletech Park #02-28, 20 Science Park Road,
Singapore 117674
Tel: +65 69268090
Email: sales@nsing.com.sg

# Contents



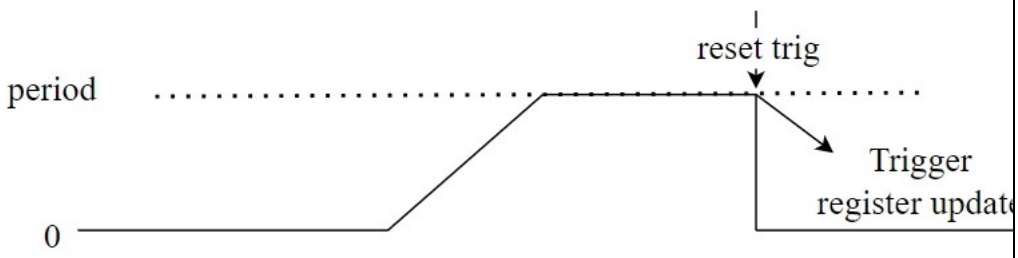


**NSING Technologies Pte. Ltd.**
Add: NSING, Teletech Park #02-28, 20 Science Park Road,
Singapore 117674
Tel: +65 69268090
Email: sales@nsing.com.sg

**NSING Technologies Pte. Ltd.**
Add: NSING, Teletech Park #02-28, 20 Science Park Road,
Singapore 117674
Tel: +65 69268090
Email: sales@nsing.com.sg

# 1 Errata List

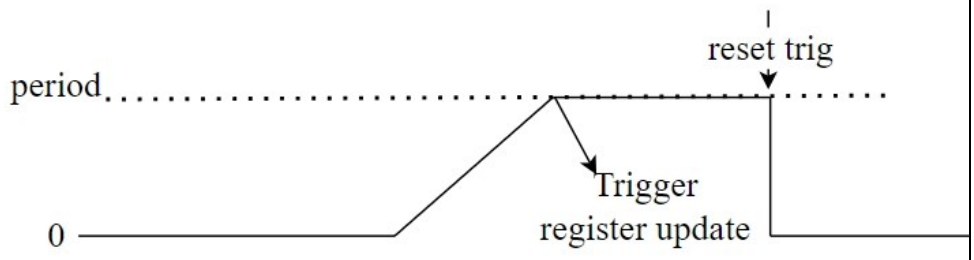
**Table 1-1 Overview of Errata**

| Errata link | | Chip Version | |
|---|---|---|---|
| | | Version A | Version B |
| GPIO and AFIO | **Error! Reference source not found.**. | • | Modify |
| SRAM | Error! Not **a valid bookmark self-reference.** (include CCM SRAM) initialization | • | • |
| SHRTIM | Issue with TIMx counter reset update | | |
| | Issue with counter reset in the half-trigger mode | | |
| | Issue with rollover in up/down single mode | | |
| | Issue with Issue with TIMx counter reset update<br>**Description**<br>When preload is enabled, SHRTIM_TxCTRL.RSTROUEN is enabled, and the TIMx counter resets or flips to 0, triggering register update. However, in reality, the register update is triggered when the counter counts to the period value.<br>If it is in continuous counting mode, this issue does not affect the usage. If it is in single-count mode, this issue will affect the usage. As shown in the following figure.<br>Correct:<br>  <br> | • | • |



NSING Technologies Pte. Ltd.
Add: NSING, Teletech Park #02-28, 20 Science Park Road, Singapore 117674
Tel: +65 69268090
Email: sales@nsing.com.sg

Wrong：




**Workaround**

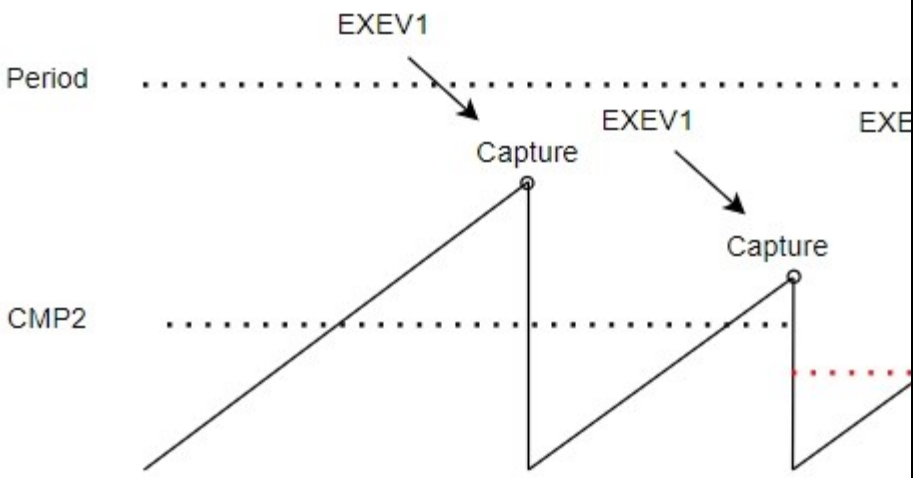
None

## 1.1 Issue with counter reset in the half-trigger mode

**Description**

In the half-trigger mode, when a capture event occurs, the counter is not reset, and the CMP2 is updated to half of the captured value.

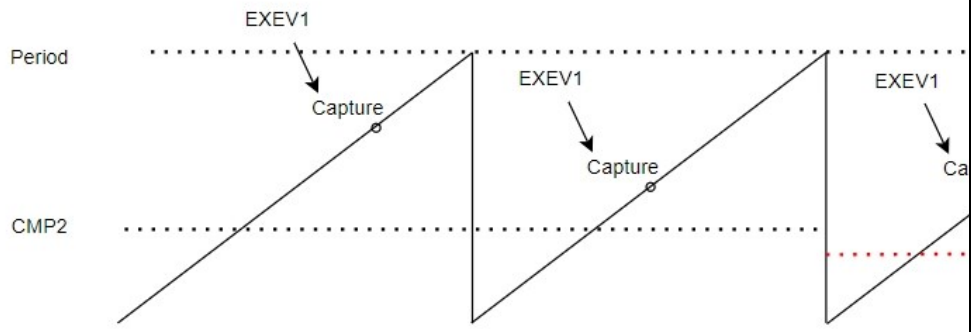
Correct：




Wrong：



**NSING Technologies Pte. Ltd.**
Add: NSING, Teletech Park #02-28, 20 Science Park Road,
Singapore 117674
Tel: +65 69268090
Email: sales@nsing.com.sg




**Workaround**

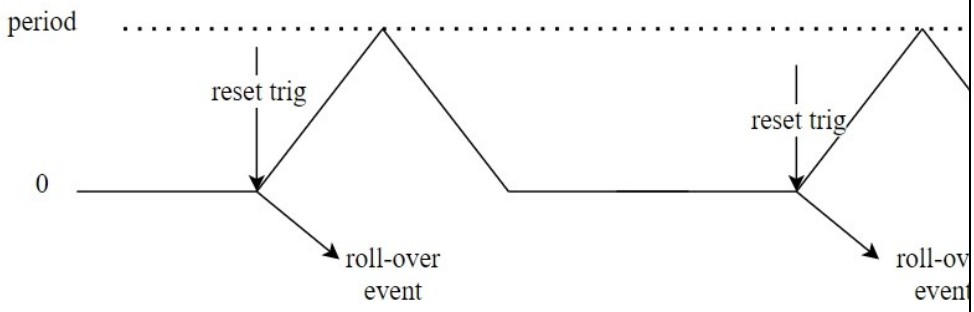
None

## 1.2 Issue with rollover in up/down single mode

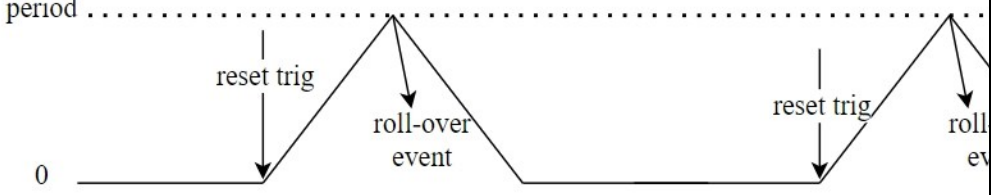
**Description**

In up/down single mode, the rollover event occurs when the counter resets or flips to 0. However, in reality, it occurs when counting to the period value. As shown in the following figure.

Correct：




Wrong：






NSING Technologies Pte. Ltd.
Add: NSING, Teletech Park #02-28, 20 Science Park Road,
Singapore 117674
Tel: +65 69268090
Email: sales@nsing.com.sg

| | | | |
|---|---|---|---|
| | **Workaround**<br>None | | |
| | Issue with external event window in up/down mode | | |
| | Workaround<br>None | • | • |
| | **Error! Reference source not found.** | • | • |
| | Issue with periodic event triggering ADC | • | Modify |
| | In greater than mode, preload function of all registers is disabled | • | Modify |
| | Delayed idle cannot be enabled before the first output enable | • | • |
| | Issue with IDLE state transitioning to FAULT state | • | Modify |
| | External fault source is still valid, and the fault flag can be cleared | | |
| | When the fault is not restored, the FAULT flag cannot be set while the second fault signal is valid | | |
| TIM | **Error! Reference source not found.** | • | • |
| U(S)ART | Issue with inability to send data properly in 485+DMA mode | • | Modify |
| ADC | Issue with multiple ADCs operating in synchronous regular and alternate mode with oversampling and reset mode enabled | • | Modify |
| USB | **Error! Reference source not found.** | • | • |
| SPI | Issue with SPI receives FIFO underflow flag | • | Modify |



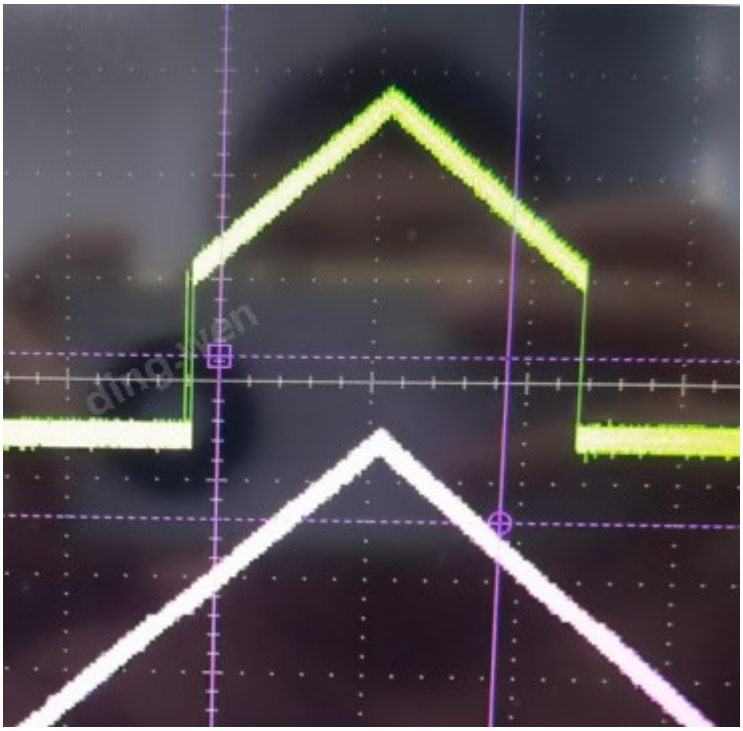
**NSING Technologies Pte. Ltd.**
Add: NSING, Teletech Park #02-28, 20 Science Park Road, Singapore 117674
Tel: +65 69268090
Email: sales@nsing.com.sg

# 2 GPIO and AFIO

## 2.1 NRST generates glitches during power-up and power-down

**Description**

During the chip power-up process, when VDD rises near the BOR voltage, the NRST pin produce the glitch as shown in the figure below, but the program will not run at this time. As VDD continues to rise, NRST will be pulled high normally, and the chip will operate as expected.



Red signal：*VDD;*

Yellow signal：*NRST*

**Workaround**

None



**NSING Technologies Pte. Ltd.**
Add: NSING, Teletech Park #02-28, 20 Science Park Road,
Singapore 117674
Tel: +65 69268090
Email: sales@nsing.com.sg

# 3 SRAM

## 3.1 Error! Not a valid bookmark self-reference. **(include CCM SRAM)**

**Description**

When using the SRAM (including CCM SRAM) one-click initialization function, if the initialization address range includes the address of the most recent write, the content at that address will not be successfully initialized, while the content at other addresses will be initialized normally.

**Workaround**

Write initial values to the address of the most recent SRAM write, then perform a one-click initialization.

# 4 SHRTIM

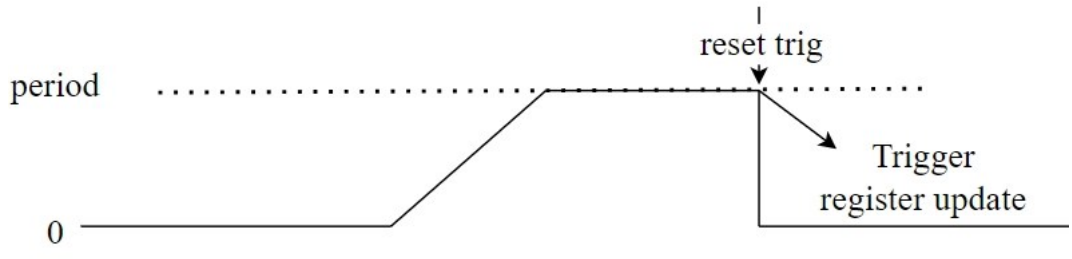
## 4.1 Issue with TIMx counter reset update

**Description**

When preload is enabled, SHRTIM_TxCTRL.RSTROUEN is enabled, and the TIMx counter resets or flips to 0, triggering register update. However, in reality, the register update is triggered when the counter counts to the period value.

If it is in continuous counting mode, this issue does not affect the usage. If it is in single-count mode, this issue will affect the usage. As shown in the following figure.

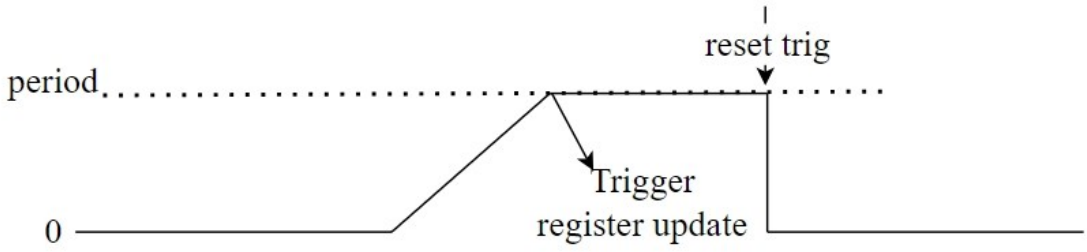
Correct:




Wrong：



NSING Technologies Pte. Ltd.
Add: NSING, Teletech Park #02-28, 20 Science Park Road,
Singapore 117674
Tel: +65 69268090
Email: sales@nsing.com.sg




**Workaround**

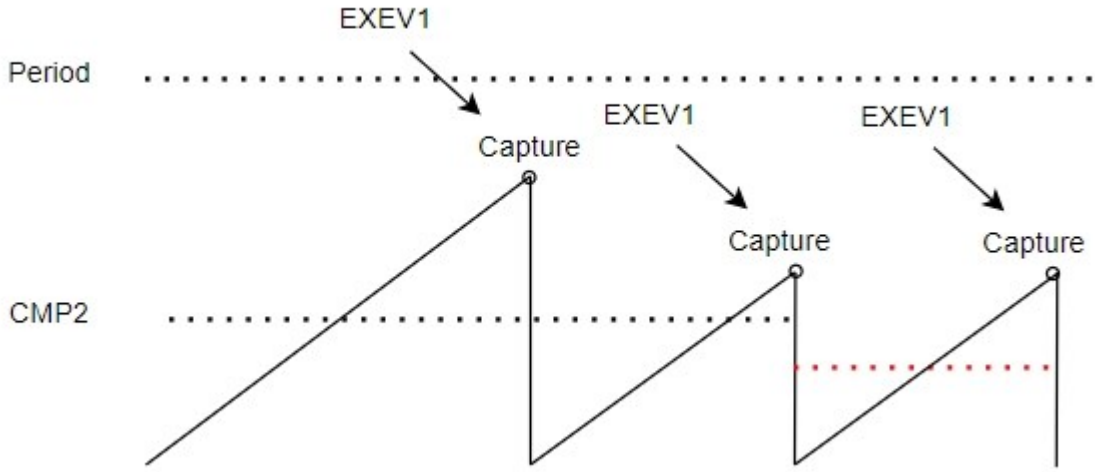
None

## 4.2 Issue with counter reset in the half-trigger mode

**Description**

In the half-trigger mode, when a capture event occurs, the counter is not reset, and the CMP2 is updated to half of the captured value.

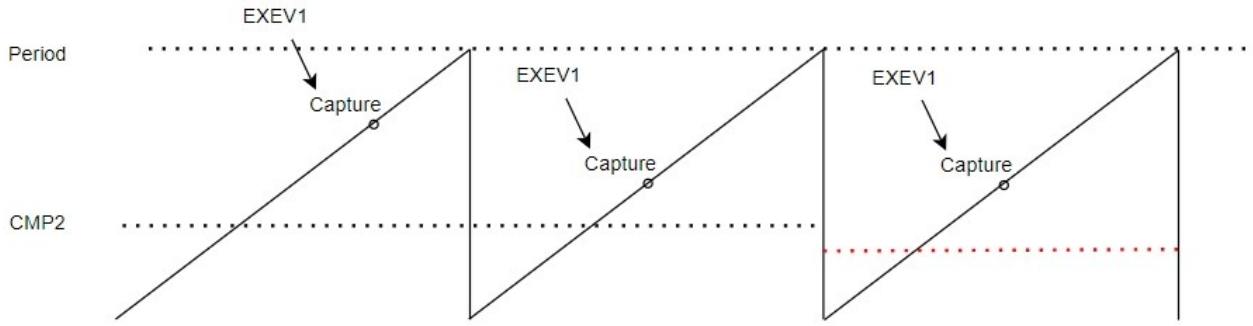
Correct：




Wrong：



NSING Technologies Pte. Ltd.
Add: NSING, Teletech Park #02-28, 20 Science Park Road,
Singapore 117674
Tel: +65 69268090
Email: sales@nsing.com.sg




**Workaround**

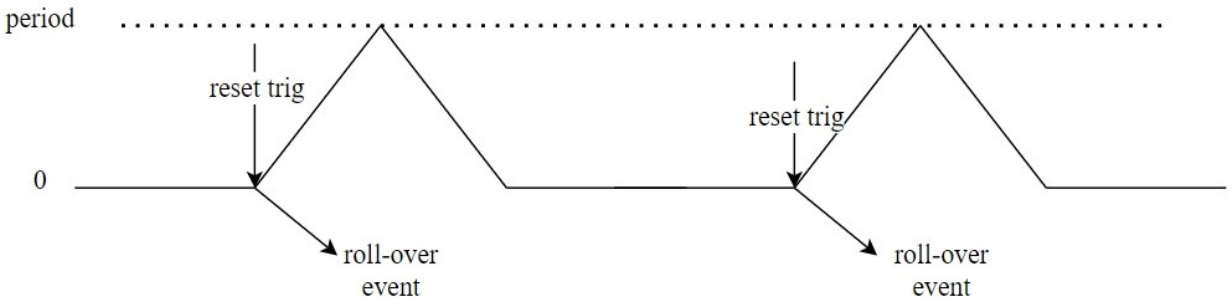
None

## 4.3 Issue with rollover in up/down single mode

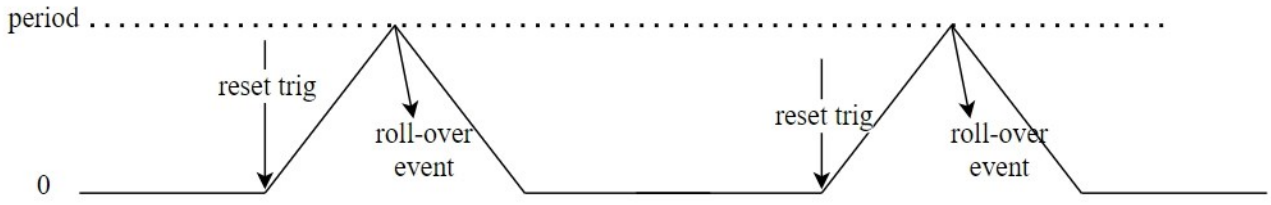
**Description**

In up/down single mode, the rollover event occurs when the counter resets or flips to 0. However, in reality, it occurs when counting to the period value. As shown in the following figure.

Correct：




Wrong：




**Workaround**



NSING Technologies Pte. Ltd.
Add: NSING, Teletech Park #02-28, 20 Science Park Road,
Singapore 117674
Tel: +65 69268090
Email: sales@nsing.com.sg

None

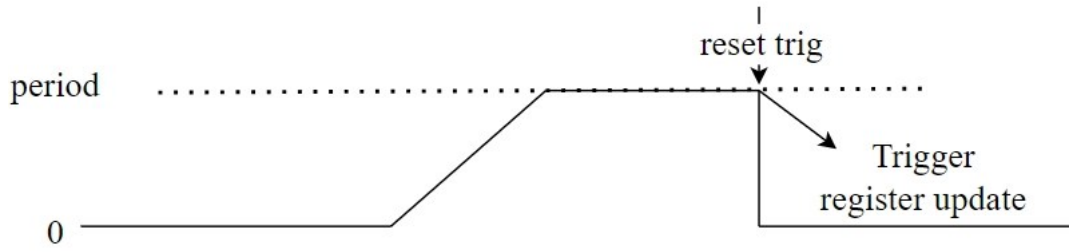
## 4.4 Issue with Issue with TIMx counter reset update

**Description**

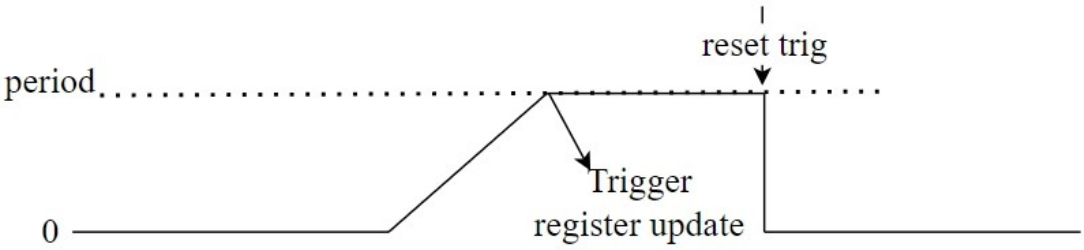
When preload is enabled, SHRTIM_TxCTRL.RSTROUEN is enabled, and the TIMx counter resets or flips to 0, triggering register update. However, in reality, the register update is triggered when the counter counts to the period value.

If it is in continuous counting mode, this issue does not affect the usage. If it is in single-count mode, this issue will affect the usage. As shown in the following figure.

Correct:




Wrong：




**Workaround**

None

## 4.5 Issue with counter reset in the half-trigger mode

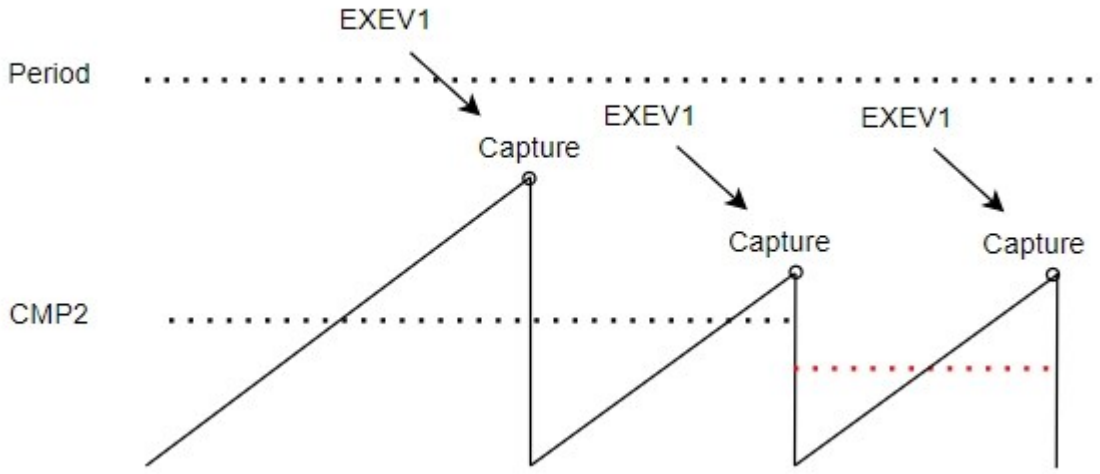
**Description**

In the half-trigger mode, when a capture event occurs, the counter is not reset, and the CMP2 is updated to half of the captured value.

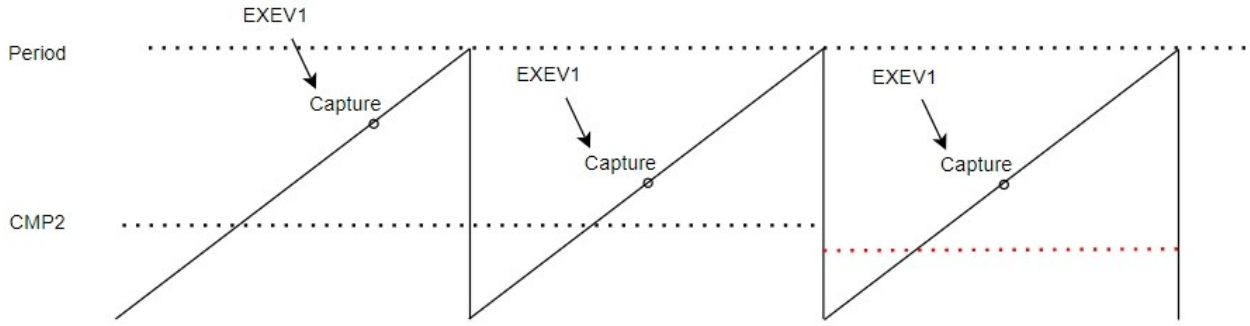
Correct：



NSING Technologies Pte. Ltd.
Add: NSING, Teletech Park #02-28, 20 Science Park Road,
Singapore 117674
Tel: +65 69268090
Email: sales@nsing.com.sg




Wrong：




**Workaround**

None

## 4.6 Issue with rollover in up/down single mode

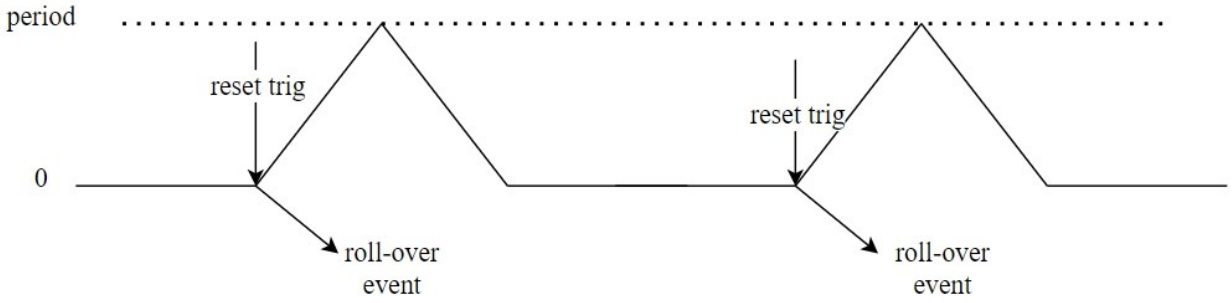
**Description**

In up/down single mode, the rollover event occurs when the counter resets or flips to 0. However, in reality, it occurs when counting to the period value. As shown in the following figure.

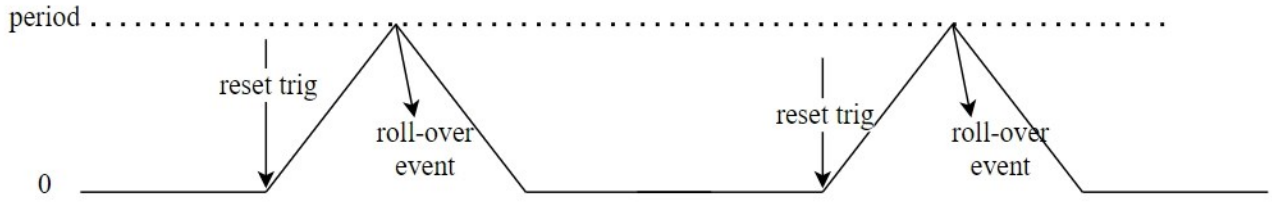
Correct：



NSING Technologies Pte. Ltd.
Add: NSING, Teletech Park #02-28, 20 Science Park Road,
Singapore 117674
Tel: +65 69268090
Email: sales@nsing.com.sg




Wrong：




**Workaround**

None

## 4.7 Issue with unavailability of IDLEMx (x = 1, 2) bits in burst mode

**Description**

In up/down mode, when the counter is disabled during a downcount (TxCNTEN reset), if the counter is re-enabled, it will continue to count up.

**Workaround**

None

## 4.8 Issue with external event window in up/down mode

**Description**

In up/down mode, the SHRTIM_TxEXEVFLTy.EXEVzFLT[4:1] is set 4b’1111, The window filter duration is from the point of setting the count up time CMP2 to the point of setting the count down time CMP3. But CMP2 comes from another timer unit (from TIMWIN source), not from the timer unit itself.

**Workaround**

None



NSING Technologies Pte. Ltd.
Add: NSING, Teletech Park #02-28, 20 Science Park Road,
Singapore 117674
Tel: +65 69268090
Email: sales@nsing.com.sg

## 4.9 Issue with unavailability of balanced idle

**Description**

Balanced idle is unavailable.

**Workaround**

None

## 4.10 Issue with unavailability of IDLEMx (x = 1, 2) bits in burst mode

**Description**

N32 does not have the IDLEMy bit, that is, when burst mode is enabled in N32, it is equivalent to IDLEMy = 1. If IDLEMy = 0 is needed, then disable burst mode to prevent timer unit output from being controlled by Burst mode. However, N32 cannot configure one output channel of the timer unit to be unaffected by Burst mode, while the other output channel is controlled by Burst mode.

| | | |
|---|---|---|
| [0] | IDLEM1 | Output 1 Idle Mode<br>This bit selects Output 1 Idle Mode<br>0: No effect; the output is not controlled by Burst Mode<br>1: When selected by the Burst Mode Controller, the output is in Idle Mode. |

| | | |
|---|---|---|
| [18] | IDLEM2 | Output 2 Idle Mode<br>This bit selects Output 2 Idle Mode<br>0: No effect, the output is not controlled by Burst Mode<br>1: When selected by the Burst Mode Controller, the output is in Idle Mode” |

**Workaround**

None



NSING Technologies Pte. Ltd.
Add: NSING, Teletech Park #02-28, 20 Science Park Road,
Singapore 117674
Tel: +65 69268090
Email: sales@nsing.com.sg

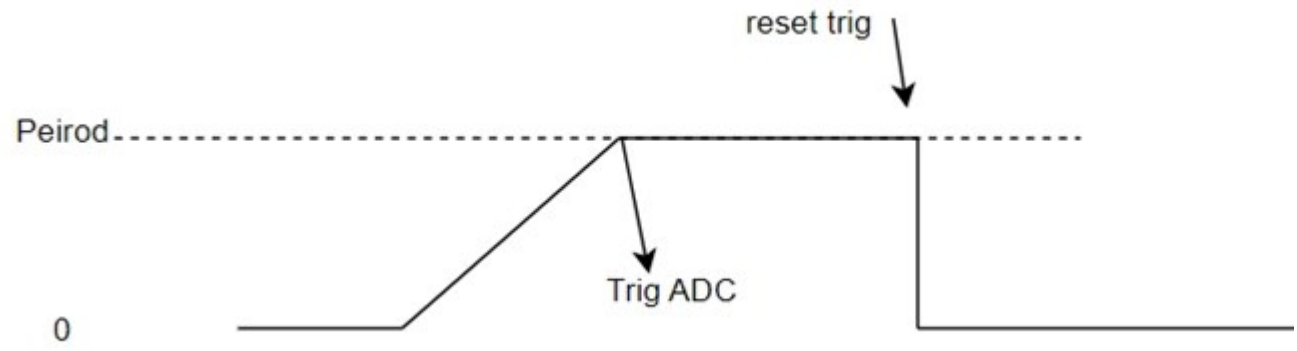
## 4.11 Issue with periodic event triggering ADC

### Description

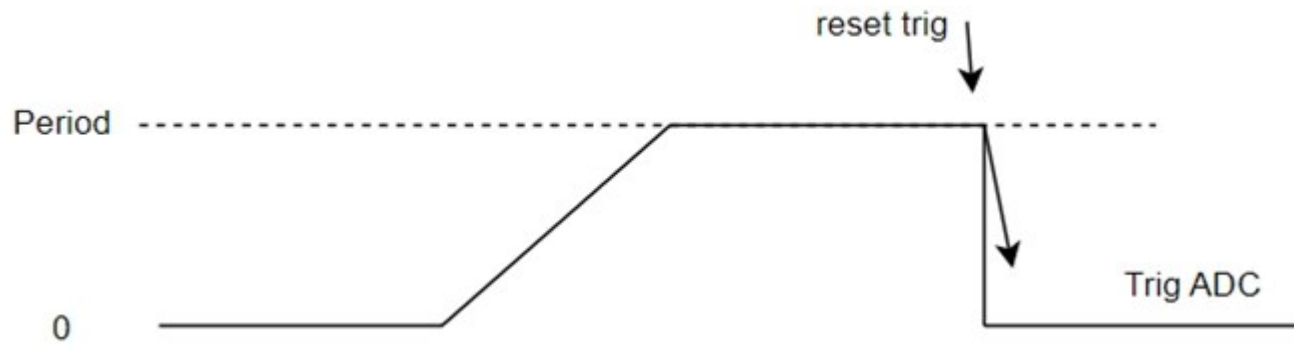
When the periodic event is used for ADC triggering, the trigger signal should be generated when the counter counts to the period value. However, in reality, the trigger signal is generated only when the counter value flips from the period value to zero.

If it is in continuous counting mode, this issue does not affect the usage. If it is in single-count mode, this issue will affect the usage. As shown in the following figure.

Correct：




Wrong：




### Workaround

Use another trigger source (such as CMP5) instead of the periodic trigger.



NSING Technologies Pte. Ltd.
Add: NSING, Teletech Park #02-28, 20 Science Park Road,
Singapore 117674
Tel: +65 69268090
Email: sales@nsing.com.sg

## 4.12 In greater-than mode, preload function of all registers is disabled

**Description**

In greater-than mode，the preload function of all registers is disabled. The correct design is to only disable the preload of registers SHRTIM_TxCMP1DAT and SHRTIM_TxCMP3DAT.

**Workaround**

None

## 4.13 Delayed idle cannot be enabled before the first output enable

**Description**

If delayed idle is enabled before the first output enable, then after the output enable, it will immediately enter delayed idle, even without the trigger of delayed idle.

**Workaround**

Enable delayed idle after the first output enable.

## 4.14 Issue with IDLE state transitioning to FAULT state

**Description**

Transitioning from the IDLE state to the FAULT state requires meeting OEN = 1 before transitioning to the FAULT state. In reality, even when OEN = 0, the FAULT trigger can transition the IDLE state to the FAULT state.

**Workaround**

Matching the levels of the IDLE state and FAULT state to be the same level, this issue has no practical impact on the application.

## 4.15 External fault source is still valid, and the fault flag can be cleared

**Description**

Fault level is valid。After the SHRTIM output enters the fault state, if the input signal of the fault remains valid, the fault flag can be cleared and cannot be set. Merely by checking the fault flag, it is not possible to transition the SHRTIM from the fault state back to the run state.

**Workaround**

Further check the level of the fault input signal.



NSING Technologies Pte. Ltd.
Add: NSING, Teletech Park #02-28, 20 Science Park Road,
Singapore 117674
Tel: +65 69268090
Email: sales@nsing.com.sg

Example of restoration method:

FAULTchecks valid level. Main program loop waits for the FAULT flag, when the FAULT flag is valid，check if the input source signal of FAULT has become invalid（If the analog comparator is the source of FAULT, then check if the analog comparator is outputting an invalid level; if GPIO is the source, then check if the GPIO is outputting an invalid level）. If it is an invalid level, clear the FAULT flag, then enable the output; if it is a valid level, continue looping to wait for the FAULT flag.

Example code for the restoration method:

```
while (1)
{
    while(SHRTIM1->sCommonRegs.INTSTS & SHRTIM_INTSTS_FALT1ITF)
    {

        if((GPIOA->PID & (uint32_t)GPIO_PIN_12) == 0)
        {
            SHRTIM1->sCommonRegs.INTCLR = SHRTIM_INTCLR_FALT1IC;

            SHRTIM1->sCommonRegs.OEN = SHRTIM_OEN_TD1OEN | SHRTIM_OEN_TA1OEN;
        }
    }
}
```

## 4.16 FAULT flag can’t be set if the fault is not restored and the second fault signal is valid

**Description**

The first valid fault signal places the SHRTIM output in the fault state. If the fault is not restored from the fault state, but the fault flag is cleared, the subsequent second valid fault signal will not set the fault flag.

**Workaround**

None

# 5 TIM

## 5.1 Issue with switching from 100% duty cycle PWM mode to another mode

**Description**



NSING Technologies Pte. Ltd.
Add: NSING, Teletech Park #02-28, 20 Science Park Road,
Singapore 117674
Tel: +65 69268090
Email: sales@nsing.com.sg

All ATIM/GTIM cannot function properly when switching from 100% duty cycle PWM mode to forced inactive mode (OC1MD[2:0]=100) or setting channel 1 to invalid level mode when matched (OC1MD[2:0]=010).

**Workaround**

After the first output of a 100% duty cycle PWM waveform, each time CC4E is configured as 1, configure CC4P as 1; each time CC4E is configured as 0, configure CC4P as 0, to achieve normal waveform switching.

# 6 U(S)ART

## 6.1 Issue with inability to send data properly in 485+DMA mode

**Description**

Data loss occurs when using USART in 485+DMA mode for transmission.

**Workaround**

Configure USART_CTRL1.DEDT as 0, and read the USART_STS register before setting USART_CTRL1.UEN to 1.

Note: If you want to use the 485+non-DMA function, when DEDT is not 0, the TXDE interrupt is not available. You need to determine data transmission completion by checking the TXC transmission complete flag, write data after checking TXC=1. When DEDT is 0, the TXDE interrupt can be used.

# 7 ADC

## 7.1 Issue with multiple ADCs in synchronous regular and alternate modes with oversampling and reset enabled

**Description**

When multiple ADCs (dual ADC or triple ADC) are operating in synchronous regular and alternate trigger mode, and the reset mode is enabled (ADC_CTRL3.OSRMD = 1) along with oversampling, the sampling results may be incorrect.

**Workaround**



NSING Technologies Pte. Ltd.
Add: NSING, Teletech Park #02-28, 20 Science Park Road,
Singapore 117674
Tel: +65 69268090
Email: sales@nsing.com.sg

1. Replace synchronous regular and alternate trigger mode with synchronous regular and injected mode, and retain only the required data in the software.

2. Replace reset mode (ADC_CTRL3.OSRMD = 1) with continuous mode (ADC_CTRL3.OSRMD = 0)

# 8 USB

## 8.1 Issue with USB Full Speed waking up in STOP0 mode

**Description**

When the main frequency is above 144MHz and configured to use the USB FS Wakeup signal to wake up from STOP mode, there may be a situation where the device is immediately woken up after the first entry into STOP, but unable to wake up after the second entry into STOP; other wakeup signals work properly.

**Workaround**

Reduce the main frequency to 144MHz or below before entering STOP mode.

# 9 SPI

## 9.1 Issue with SPI receive FIFO underflow flag

**Description**

Reading the RX FIFO of SPI2/3 when it is empty is invalid, the UDR flag cannot be set. However, for SPI1/4/5/6, reading the RX FIFO when it is empty can set the UDR flag.

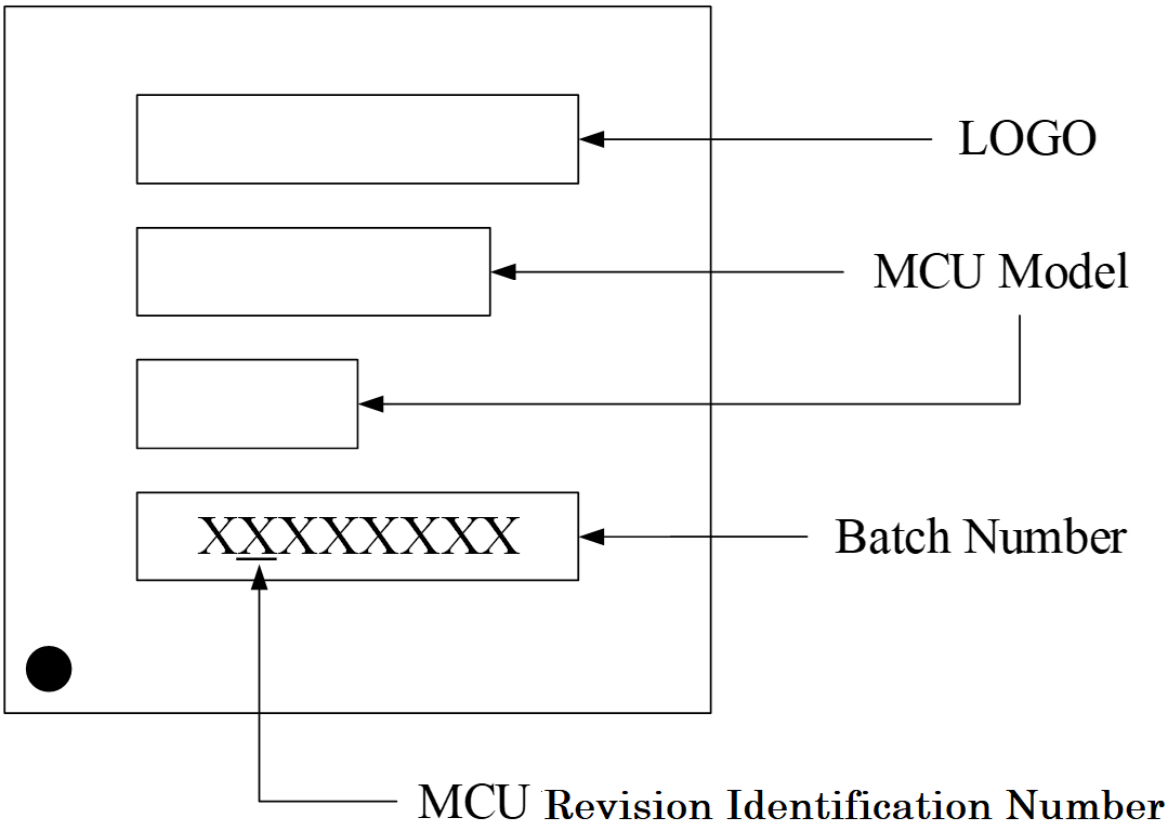
**Workaround**

Software workaround: Use the RXFIFO half-full or full flag instead of the UDR flag to determine if all data has been read. If all data has been read, reset the RXFIFO half-full or full flag.



NSING Technologies Pte. Ltd.
Add: NSING, Teletech Park #02-28, 20 Science Park Road,
Singapore 117674
Tel: +65 69268090
Email: sales@nsing.com.sg

# 10 Chip Screen Printing and Version Description






**NSING Technologies Pte. Ltd.**
Add: NSING, Teletech Park #02-28, 20 Science Park Road,
Singapore 117674
Tel: +65 69268090
Email: sales@nsing.com.sg

# 11 Version History

| Version | Date | Changes |
|---|---|---|
| V1.0.0 | 2024.11.27 | Initial release |



**NSING Technologies Pte. Ltd.**
Add: NSING, Teletech Park #02-28, 20 Science Park Road,
Singapore 117674
Tel: +65 69268090
Email: sales@nsing.com.sg

# 12 Disclaimer

This document is the exclusive property of NSING TECHNOLOGIES PTE. LTD.(Hereinafter referred to as NSING). This document, and the product of NSING described herein (Hereinafter referred to as the Product) are owned by NSING under the laws and treaties of Republic of Singapore and other applicable jurisdictions worldwide. The intellectual properties of the product belong to Nations Technologies Inc. and Nations Technologies Inc. does not grant any third party any license under its patents, copyrights, trademarks, or other intellectual property rights. Names and brands of third party may be mentioned or referred thereto (if any) for identification purposes only. NSING reserves the right to make changes, corrections. enhancements, modifications, and improvements to this document at any time without notice. Please contact NSING and obtain the latest version of this document before placing orders. Although NATIONS has attempted to provide accurate and reliable information, NATIONS assumes no responsibility for the accuracy and reliability of this document. It is the responsibility of the user of this document to properly design, program, and test the functionality and safety of any application made of this information and any resulting product. In no event shall NATIONS be liable for any direct, indirect, incidental, special, exemplary, or consequential damages arising in any way out of the use of this document or the Product.

NATIONS Products are neither intended nor warranted for usage in systems or equipment, any malfunction or failure of which may cause loss of human life, bodily injury or severe property damage. Such applications are deemed, Insecure Usage'. Insecure usage includes, but is not limited to: equipment for surgical implementation, atomic energy control instruments, airplane or spaceship instruments, all types of safety devices, and other applications intended to supporter sustain life. All Insecure Usage shall be made at user's risk. User shall indemnify NATIONS and hold NATIONS harmless from and against all claims, costs, damages, and other liabilities, arising from or related to any customer's Insecure Usage Any express or implied warranty with regard to this document or the Product, including, but not limited to. The warranties of merchantability, fitness for a particular purpose and non-infringement are disclaimed to the fullest extent permitted by law. Unless otherwise explicitly permitted by NATIONS, anyone may not use, duplicate, modify, transcribe or otherwise distribute this document for any purposes, in whole or in part.



**NSING Technologies Pte. Ltd.**
Add: NSING, Teletech Park #02-28, 20 Science Park Road,
Singapore 117674
Tel: +65 69268090
Email: sales@nsing.com.sg