

N32L40xx8/xB

Datasheet

N32L40x series uses 32-bit ARM Cortex-M4F core, operating frequency up to 64MHz, supporting floating-point unit and DSP instructions. The device integrates up to 128KB of encrypted flash, and up to 24KB of SRAM. The series features rich of high-performance interface, built-in 1x12bit 4.5Msps ADC, 2x independent rail-to-rail operational amplifiers, 2x high-speed comparators, 1x 1Msps 12bit DAC, Integrate up to 320 Segment LCD driver, Integrated multi-channel U(S)ART, I2C, SPI, USB, CAN and other digital communication interfaces, built-in hardware acceleration engine for cryptographic algorithm.

Key Features

- **CPU Core**
 - 32-bit ARM Cortex-M4 core with FPU, supporting single-cycle multiplication and hardware divide DSP instructions and MPU.
 - Built-in 2KB instruction Cache supports Flash accelerator unit for zero-wait program execution.
 - Maximum frequency of 64MHz, with 80DMIPS
- **Memories**
 - Up to 128 KByte on-chip Flash, supports encrypted storage function, partition management and data protection, supports hardware ECC check, 100,000 erase/write cycles, 10-year data retention.
 - Up to 24 KByte of SRAM with hardware parity check, including 16Kbyte SRAM1(Stop2 mode can be configured as retention) and 8 Kbyte SRAM2(both Standby and Stop2 modes can be configured as retention)
- **Low Power Management**
 - STANDBY mode: 1.5uA, all backup registers retention, IO retention, optional RTC Run, 8KByte SRAM2 retention, fast wake up
 - STOP2 mode: 3uA, RTC Run, 8KByte SRAM2 retention, CPU register retention, IO retention, fast wake up
 - RUN mode: 60uA/MHz@64MHz
 - LPRUN mode: PLL off, MSI as the system master clock, MR off, LPR on, USB/CAN/SAC power off, other peripherals are optional
- **Segment LCD display driver, support up to 176 segments (4x44) or 320 segments (8x40)**
- **Analog Interface**
 - 1x 12bit ADC with 4.5Msps,
 - configurable resolution,
 - up to 16 external single-ended input channels, supports differential mode
 - 2x rail-to-rail operational amplifiers with built-in maximum 32x programmable gain amplifier
 - 2x high-speed analog comparators, built-in 64-level adjustable comparison reference, COMP1 support working in STOP2 mode
 - 1x 12bit DAC, sampling rate 1Msps
 - Internal 2.048V reference voltage source
 - Internal integrated low-voltage detection unit
- **Clock**
 - HSE: 4MHz~32MHz external high-speed crystal
 - LSE: 32.768KHz External low-speed crystal
 - HSI: High-speed internal RC 16MHz

- MSI: Multi-speed internal RC 100K~4MHz
- LSI: Low-speed internal RC 40KHz
- Built-in high speed PLL
- MCO: Support 1-channel clock output, configurable as low-speed or high-speed divisional output
- **Reset**
 - Support power-on/brown-out/external pin reset
 - Support watchdog reset
- **Support up to 64 GPIOs**
- **Communication Interface**
 - 5x U(S)ART interfaces,
 - 3x USART interfaces (support 1xISO7816, 1xIrDA, LIN)
 - 2x UART interfaces
 - 1x LPUART, support wake-up MCU in STOP2 mode
 - 2x SPI interfaces, up to 16 Mbps, support I2S
 - 2x I2C interfaces, up to 1 MHz, master-slave mode is configurable, slave mode support dual-address response
 - 1x USB2.0 FS Device interface
 - 1x CAN 2.0A/B bus interface
- **DMA controller**
 - 1x high-speed DMA controller, each controller supports 8 channels, with arbitrary configurable channel source and destination addresses.
- **RTC , support leap year perpetual calendar, alarm event, periodic wake up, support internal and external clock calibration**
 - supports leap-year perpetual calendar, alarm event, periodic wakeup.
 - supports internal and external clock calibration
- **Timer**
 - 2x 16bit advanced control timers with maximum control precision of 9.25ns,
 - support input capture, complementary output, quadrature encoding input etc.
 - Each timer has 4 independent channels, 3 of which support 6-channel complementary PWM output.
 - 5x 16-bit general purpose timers
 - each timer with 4 independent channels
 - support input capture/output comparison /PWM output
 - 2x 16-bit basic timers
 - 1x 16-bit low-power timer , support double pulse counting function, can work in STOP2 mode
 - 1x 24-bit SysTick timer
 - 1x 7-bit Window Watchdog (WWDG)

- 1x 12-bit Independent Watchdog (IWDG)

- **Programming Methods**

- Support SWD/JTAG debugging interface
- Support UART and USB Bootloader

- **Security Features**

- Built-in cryptographic algorithm hardware acceleration engine
- Support AES, DES, TDES, SHA1/224/256, SM1, SM3, SM4, and SM7 algorithms
- Flash storage encryption, Multi-user partition Management Unit (MMU)
- true random number generator(TRNG)
- CRC16/32 operation
- Support write protection (WRP), multiple read protection (RDP) levels (L0/L1/L2)
- Support secure boot , , secure firmwareupdate
- Support external clock failure detection, tamper detection

- **96-bit UID and 128-bit UCID**

- **operating Conditions**

- Operating voltage range: 1.8V~3.6V
- Operating temperature range: -40°C ~ 105°C
- ESD: ±4KV (HBM model), ±1KV (CDM model)

- **Packages**

- QFN32(4mm×4mm)
- QFN32(5mm×5mm)
- QFN48(6mm×6mm)
- LQFP48(7mm×7mm)
- QFN64(8mm×8mm)
- LQFP64(10mm×10mm)
- LQFP80(12mm×12mm)

- **Ordering Information**

Reference	Part Number
N32L402	N32L402C8Q7, N32L402C8L7, N32L402R8L7, N32L402CBQ7, N32L402CBL7, N32L402RBL7
N32L403	N32L403K8Q7, N32L403KBQ7, N32L403KBQ7-1 ⁽¹⁾
N32L406	N32L406C8Q7, N32L406R8Q7, N32L406CBL7, N32L406RBL7, N32L406MBL7

Note: (1): The package is QFN32 (5mm x 5mm)

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Introduction

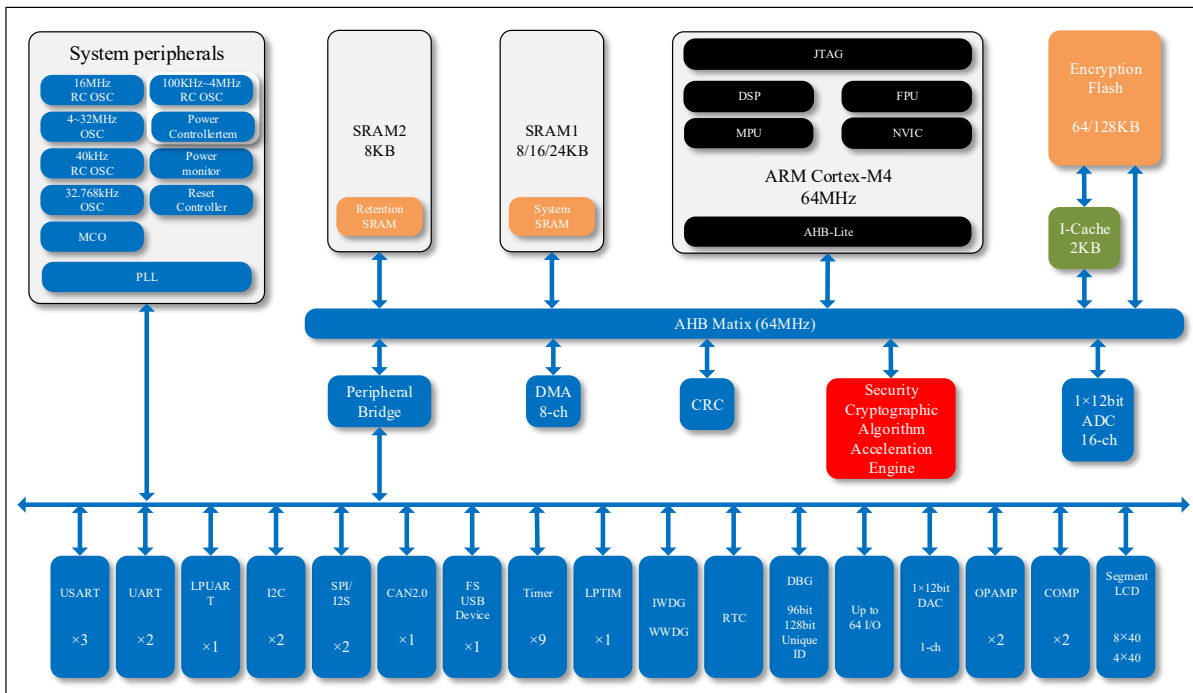
N32L40x microcontrollers family features a high-performance 32-bit ARM Cortex™-M4F core with an integrate floating point operation unit(FPU) and digital signal processing(DSP). It supports parallel computing instructions and operates at a maximum frequency of 64MHz.The in-chip encrypted storageFlash can hold up to 128KB, supporting multi-user partition permission management. Additionally, it includes up to 24KB of embedded SRAM, including 8KB of Retention RAM.

The device is equipped with internal high speed bus(AHB), along with two low speed peripherals clockbus (APB) and bus matrix. It offers support up to 64 alternate I/Os and features a diverse range of high performance analog interfaces. These include 12-bit 4.5MSPS ADC with up to 16 external input channels and 3 internal channels, and a 12-bit DAC with a 1MSPS sampling rate., as well as up to 320 Segment LCD driver interfaces.

For digital communication, the N32L40x provides 5x U(S)ART, 1x LPUART, 2x I2C, 2x SPI/ I2S, 1x FS USB 2.0 device, 1x CAN 2.0B communication interface. It also integrates a hardware acceleration engine, supporting various international encryption algorithm.

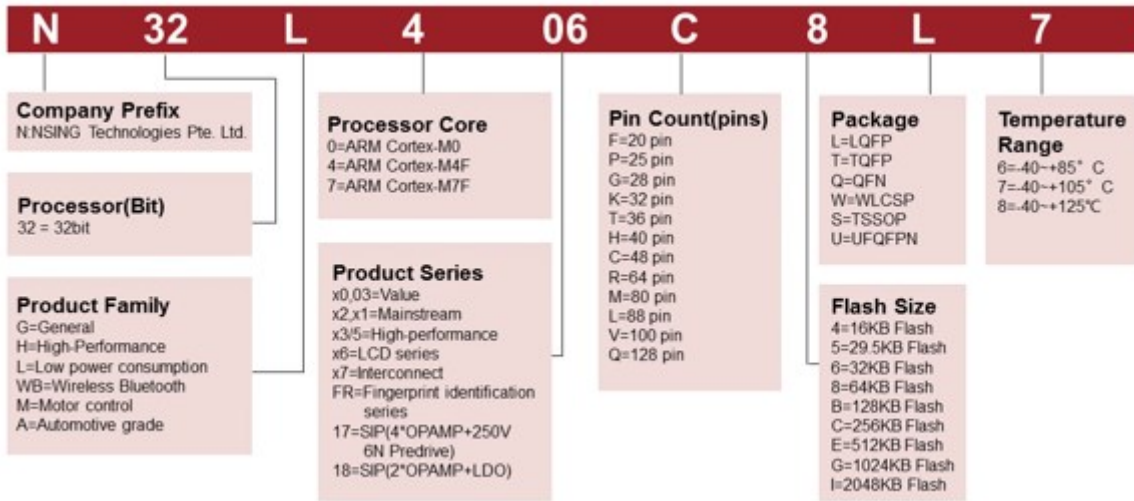
The N32L40x series operates reliable in the temperature range of -40°C to +105°C and supply voltage from 1.8V to 3.6V. It offers multiple power modes to cater to low-power applications. Available in 32/48/64/80 pin package, the peripheral configuration varies based on the package type.

Figure 0-1 N32L40x Series Block Diagram



1.1 Naming Convention

Figure 0-2 N32L406C8L7 Series Part Number Information



1.2 Product Configurations

Table 0-1 N32L40x Series Product Configuration

Device	N32L402C8/B		N32L402R8/B		N32L403K8/BQ7		N32L403 KBQ7-1 ⁽⁵⁾	N32L406C8/B		N32L406R8/B		N32L406MB
Flash (KB)	64	128	64	128	64	128	128	64	128	64	128	128
SRAM (KB)	16	16	16	16	16	24	24	16	24	16	24	24
CPU frequency	ARM Cortex-M4 @ 64MHz, 80DMIPS											
Operating environment	1.8~3.6V/-40~105°C											
Timer	General	5										
	Advanced	2										
	Basic	2										
	LPTIM	1										
Communication interface	SPI ⁽¹⁾	2	2	2	2	1	2					
	I2S ⁽¹⁾	2	2	2	2	1	2					
	I2C	2										
	UART	2										
	USART	3	3	2	2	3						
	LPUART	1										
	USB	1				No		1				
	CAN	No	No	1								
GPIO	38	52	26		29		38	52	64			
DMA Number of Channels	1x 8 Channel											
12bit ADC Number of Channels	1x 10Channel	1x 16Channel	1x 10Channel	1x 10Channel	1x 10Channel	1x 10Channel	1x 16Channel	1x 16Channel	1x 16Channel			
12bit DAC Number of Channels	1x 1 Channel											
OPAMP/COMP	2/2	2/2	2/2	2/2	2/2	2/2	2/2	2/2	2/2			
Segment LCD	4x20	4x34/8x30 ⁽²⁾ ⁽³⁾	No				4x20	4x34/8x30 ⁽²⁾ ⁽³⁾	4x44/8x40 ⁽³⁾			
Algorithm support	DES/TDES, AES, SHA1/SHA224/SHA256, SM1, SM3, SM4, SM7, CRC16/CRC32, TRNG											
Security protection	Read-write protection (RDP/WRP), storage encryption, partition protection, secure boot											
Package	LQFP48/QFN48	LQFP64	QFN32 ⁽⁴⁾		QFN32 ⁽⁵⁾		LQFP48/QFN48	LQFP64/QFN64	LQFP80			

1. SPI1 and SPI2 interfaces have the flexibility to switch between SPI mode and I2S audio mode.
2. LQFP64/QFN64 package version B chips do not support LCD 1/8 duty cycle mode (8x30).
3. In 1/8 duty cycle mode, B and C chip LCDs do not support 1/4 bias.
4. The package size is QFN32(4mm x 4mm)
5. The package size is QFN32(5mm x 5mm)

2 Function Introduction

2.1 Processor Core

The N32L40x series integrates the latest generation of embedded ARM Cortex™-M4F processors. It features a floating point processing unit (FPU), DSP and parallel computing instructions, providing excellent performance of 1.25DMIPS/MHZ. At the same time, its efficient signal processing capabilities combined with low power consumption, low cost, and ease of use. It is able to be used in application scenarios that require a blend of control and signal processing capabilities while being user-friendly.

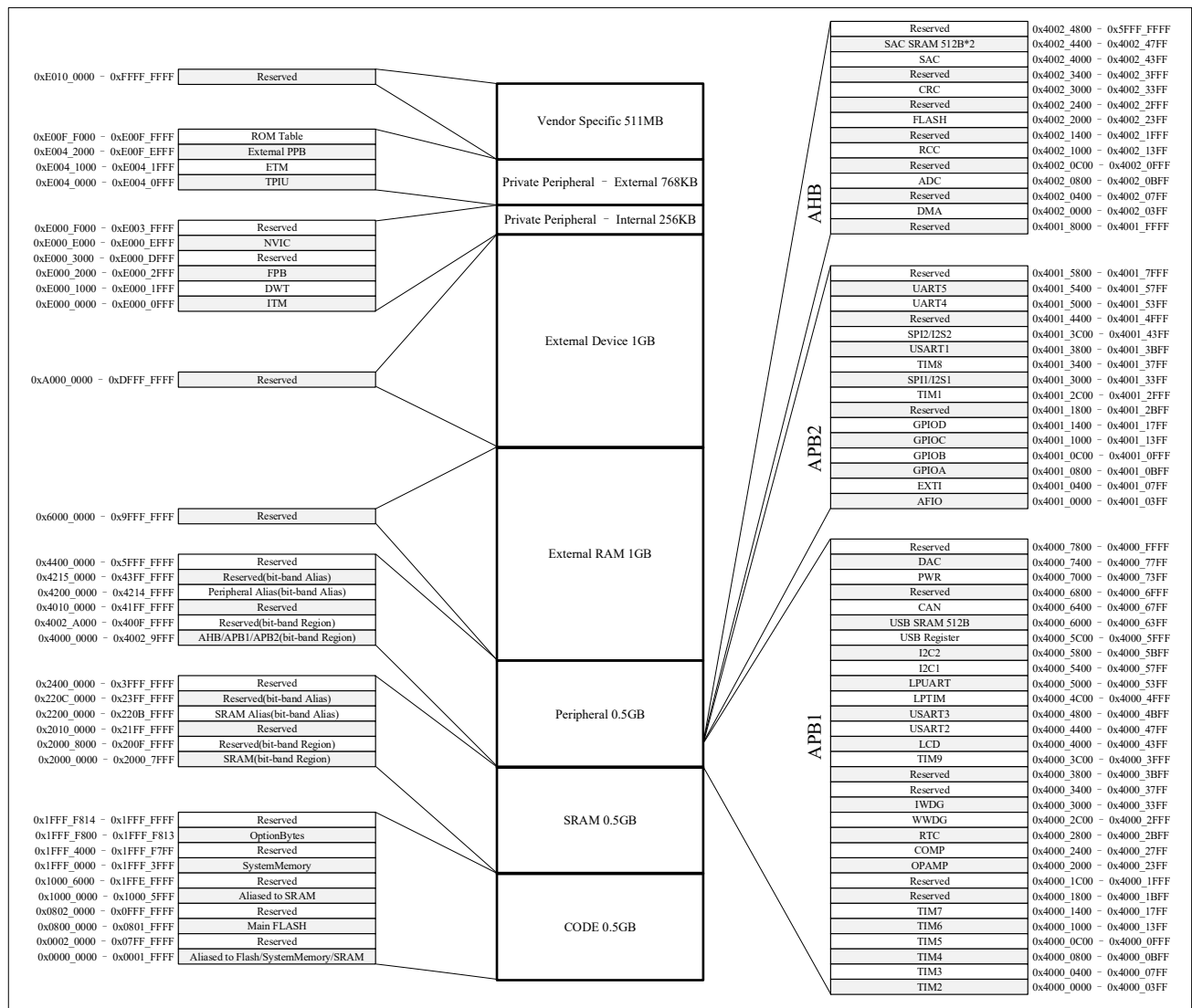
The ARM Cortex™-M4F 32-bit compact instruction set processor provides excellent code efficiency.

Note: Cortex-M4F is backward compatible with Cortex-M3 code.

2.2 Memories

N32L40x series include embedded encrypted Flash memory and embedded SRAM.

Figure 2-1 Memory Map



2.2.1 Embedded FLASH Memory

Up to 128K bytes embedded encryption Flash. It used to store programs and data, page size of 2Kbyte, supporting page erasing, word writing, word reading, half word reading, byte reading operations.

Support storage encryption protection, write automatic encryption, read automatic decryption (including program execution operation).

Support user partition management, can be divided into a maximum of three user partitions, different users cannot access each other's data (only executable code).

2.2.2 Embedded SRAM

The chip integrates a built-in -SRAM of up to 24K bytes, comprising SRAM1 and SRAM2. SRAM1 has a maximum size of 16K bytes, while SRAM2 has a maximum of 8K bytes. Both SRAM1 and SRAM2 can retain data in Stop2 mode. In STANDBY mode, only SRAM2 can retain data.

2.2.3 Nested Vector Interrupt Controller (NVIC)

The built-in nested vector interrupt controller can handle up to 66 maskable interrupt channels (excluding the 16 Cortex™-M4F interrupts) and 16 priorities.

- The tightly coupled NVIC enables low-latency interrupt response processing
- Interrupt vector entry address directly access the kernel
- Tightly coupled NVIC interface
- Allows early processing of interrupts
- Processing late arriving higher-priority interrupts
- Support interrupt tail-chaining functionality
- Automatically saves processor state
- Automatically resumes when interrupt returns with no instruction overhead

This module offers flexible interrupt management with minimal interrupt latency.

2.3 Extended Interrupt/Event Controller (EXTI)

The extended interrupt/event controller contains 27 edge detectors for generating interrupt/event requests. Each interrupt line can be independently configured with its trigger event (rising edge, falling edge or both) and can be individually masked. There is a suspended register that maintains the state of all interrupt requests. EXTI can detect clock cycles with pulse widths smaller than internal APB2. Up to 64 universal I/O ports are connected to 16 external interrupts.

2.4 Clock System

The device offers various clock options for users to choose from, including:

- High speed internal RC oscillator (HSI) at 16MHz.
- Multi-speed internal RC oscillator (MSI) ranging from 100K to 4MHz, configurable.
- Low speed internal RC oscillator (LSI) at 40KHz.
- High speed external crystal (HSE) ranging from 4MHz to 32MHz.
- Low speed external crystal (LSE) at 32.768KHz.
- Phase-Locked Loop (PLL).

Upon reset, the internal MSI clock is set as the default CPU clock, user can choose the external HSE clock with fail function. When an external clock failure is detected, it will be isolated, the system will automatically switch to MSI. If interrupts are enabled, software can receive corresponding interrupt. Similarly the system will automatically switch to MSI when the PLL clock was adopted and external oscillator fails.

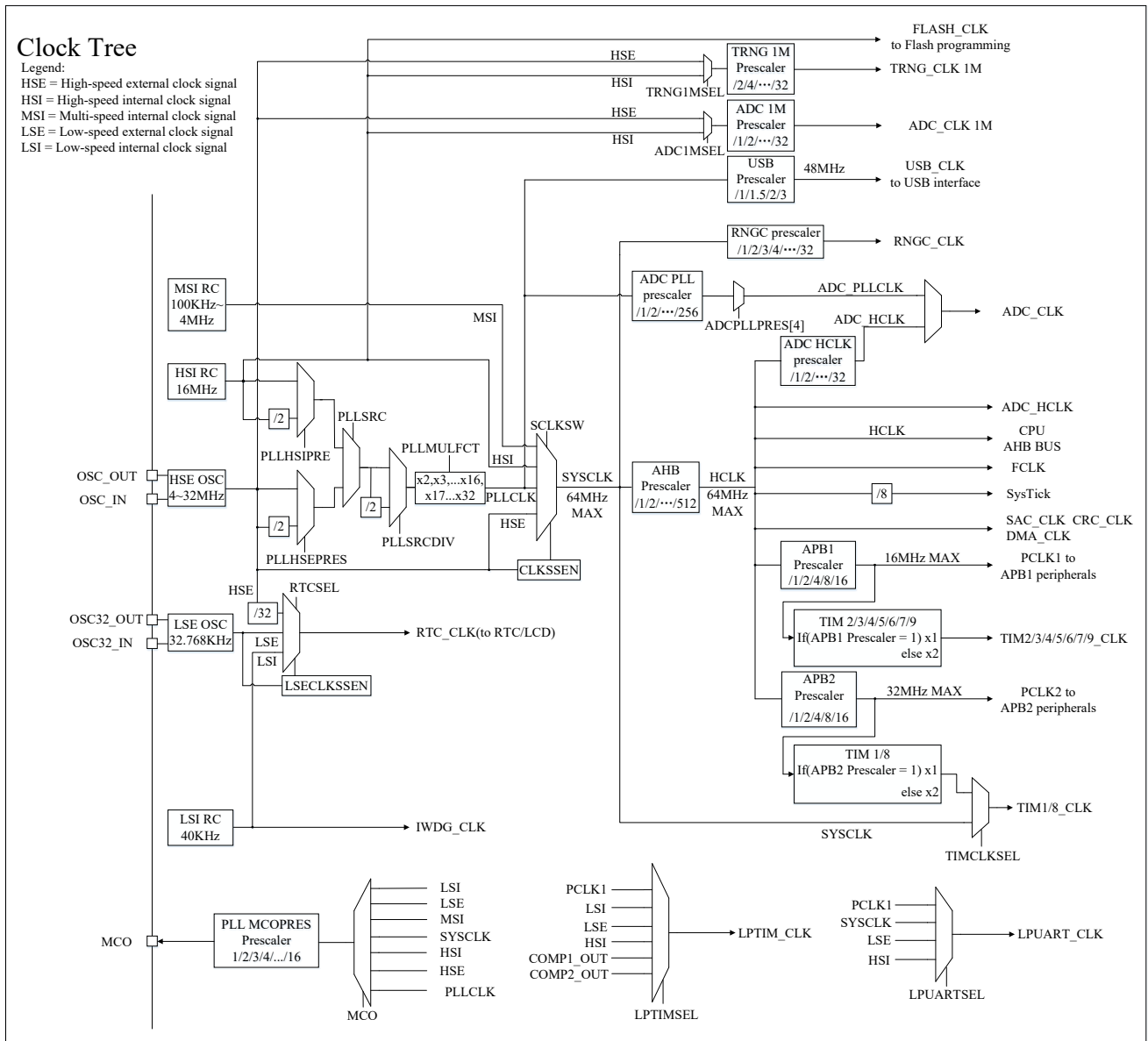
The MSI clock can be used for fast wake up and instruction execution in STOP2 state, or to provide clock for the system in low power operation state, and some other scenarios with low clock accuracy and high power consumption requirements.

There is a built-in clock security system, when enables by the user, can detect in real-time whether the HSE or LSE has fails. Once an external clock failure is detected, the system automatically switches to the internal clock and generates an interrupt alert.

Multiple prescalers are used to configure the AHB frequency, high speed APB (APB2) and low speed APB (APB1) regions. The AHB has a maximum frequency of 64MHz, APB2 has a maximum frequency of 32MHz and APB1 has a maximum frequency of 16MHz.

When using USB function (Only N32L403 and N32L406 series support USB), both HSE and PLL must be used and the CPU frequency must be 48MHz.

Figure 2-2 Clock Tree



2.5 Boot Mode

During startup, the BOOT after reset can be selected through the BOOT0 pin and option byte BOOT configuration (USER2):

- Boot from Flash memory
- Boot from system memory
- Boot from internal SRAM

The Bootloader is stored in the system memory and can program the Flash memory through USART1 or USB interface.

2.6 Power Supply Scheme

- $V_{DD} = 1.8\sim 3.6V$: The V_{DD} pin supplies power to the I/O pin and the internal voltage regulator.
- V_{LCD} supplies power to the Segment LCD module, and two power supply modes, internal and external, are configured through registers. When using LCD internal boost mode power supply, a 1 μ F capacitor must be connected to the V_{LCD} pin, or an external input power supply can be used directly to power the LCD module.
- $V_{DDA} = 1.8\sim 3.6V$: provides power supply for ADC, DAC, OPAMP and COMP.
- V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS} respectively. See **Figure 4-3 Power Supply Scheme**.

2.7 Reset

POR and BOR circuits are built in the device. This part of the circuit ensures that the system works stably when the power supply exceeds 1.8V. When V_{DD} falls below a set threshold ($V_{POR/BOR}$), the device goes into reset state without using an external reset circuit.

2.8 Programmable Voltage Detector

The device has a built-in programmable voltage detector (PVD), which monitors the power supply of V_{DD} and compares it with the threshold V_{PVD} . When V_{DD} is lower or higher than the threshold V_{PVD} , an interrupt will be generated. The interrupt handler can send a warning message, and the PVD function needs to be enabled through the program. See **Table 4-6** for values of $V_{POR/PDR}$ and V_{PVD} .

2.9 Voltage Regulator

The voltage regulator has two control modes:

- Main mode: The MCU operates in RUN, SLEEP modes
- Low power mode: The MCU operates in LP RUN, LP SLEEP, STOP2, and STANDBY modes

The voltage regulator is always in the main mode after the MCU reset.

2.10 Low Power Mode

The N32L40x series supports five low-power modes.

- LP-RUN mode

In LP-RUN (Low Power RUN) mode, the CPU operates using MSI clock, executing programs in Flash or SRAM, with the PLL turned off. USB/CAN/algorithm (SAC) module are disabled, while other peripherals can be configurable as needed.

- SLEEP mode

In SLEEP mode, only the CPU is stopped, all peripherals remain operational. They can wake up the CPU when an interrupt/event occurs.

- LP-SLEEP mode

In LP-SLEEP (Low Power SLEEP) mode, the CPU is stopped, the PLL is turned off, and the USB/CAN/SAC module are disabled. Other peripherals can be configurable as needed, and all IOs remain in the same state as in RUN mode.

- STOP2 mode

In STOP2 mode all the core digital logic areas are powered off.

- The Main voltage regulator (MR) is turned off,
- HSE/HSI/MSI/PLL is turned off.
- CPU registers are retained.
- LSE/LSI can be configured to operate.
- GPIOs are retained,
- SRAM1 and SRAM2 can be retained
- SPI, USART/UART, I2C, WWDG are retained.
- 80 byte backup register are retained.
- RET and low power domains operate normally.

Wakeup: The device can be woken up from STOP2 mode by any of the 16 external EXTI signals (I/O related), WKUP pin wakeup, RTC periodic wake up, RTC alarm, RTC tamper, RTC timestamp, NRST reset, IWDG reset.

- STANDBY mode

In STANDBY mode, the device can achieve a lower current consumption. The internal voltage regulator is turned off, as well as PLL, HSI RC oscillator and HSE crystal oscillator, only LSE and LSI can optionally work. Upon entering STANDBY mode, the contents of the main domain register will be lost, SRAM2 can optionally be retained, the STANDBY circuit still works.

External reset signal on the NRST, IWDG reset, rising/falling edge on the WKUP pin, RTC alarm, RTC timestamp and RTC tamper can wake up the microcontroller from STANDBY mode.

Note: RTC, IWDG and corresponding clock can not be stopped when entering standby mode.

2.11 Direct Memory Access (DMA)

The device integrates a flexible general-purpose DMA controller that supports eight DMA channels. It can manage data transfers from memory to memory, peripherals to memory, and memory to peripherals. The DMA controller supports the management of ring buffers, thus avoiding interrupts when the controller reaches the end of the buffer.

Each channel has dedicated hardware DMA request logic, and each channel can be triggered by software. The transmission length, source address and destination address of each channel can be set separately by software.

DMA can be used with major peripherals: SPI, I2C, USART, TIMx (general, basic and advanced timers), DAC, I2S and ADC.

2.12 Real Time Clock (RTC)

The RTC is a set of continuously running counters with a built-in calendar clock module that provides a perpetual calendar function, as well as alarm interrupt and periodic interrupt (with a minimum 2 clock cycles). The RTC will not be reset by the system or power reset source, nor will it be reset when woken up from STANDBY mode.

The RTC can be driven by either a 32.768kHz external crystal oscillator, an internal low-power 40kHz RC oscillator, or a high-speed external clock with 128 frequency divisions.

For application scenarios requiring very high timing accuracy, it is recommended to use an external 32.768kHz clock as the clock source. To compensate for the clock deviation of natural crystal, a 256Hz signal can be output to calibrate the clock of RTC.

The RTC features a 22-bit prescaler for a time-based clock. By default, when the clock is set to 32.768kHz, it generates a 1-second time reference. In addition, the RTC can be used to trigger wake up in low-power mode.

2.13 Timer And Watchdog

Up to 2 advanced control timers, 5 general-purpose timers and 2 basic timers, 1 low power timer, 2 watchdog timers and 1 system tick timer.

The following table compares the functions of advanced control timer, general-purpose timer and basic timer:

Table 2-1 Comparison Of Timer Functions

Timer	Counter resolution	Counter type	Prescaler factor	Generate DMA requests	Capture/compare channels	Complementary output
TIM1 TIM8	16	Up, down, up/down	Any integer between 1 and 65536	Y	4	Y
TIM2 TIM3 TIM4 TIM5 TIM9	16	Up, down, up/down	Any integer between 1 and 65536	Y	4	N
TIM6 TIM7	16	up	Any integer between 1 and 65536	Y	0	N

2.13.1 Low Power Timer (LPTIM)

The LPTIM is a 16-bit timer with multiple clock sources. It can keep running in all power modes except for Standby mode. LPTIM can operate without an internal clock source, it can be used as a “Pulse Counter”. Also, the LPTIM can wake up the system from low-power modes, to realize “Timeout functions” with extreme low power consumption.

Main features:

- 16-bit up counter
- 3-bit prescaler, 8 kinds of prescaler factors (1, 2, 4, 8, 16, 32, 64, 128)
- Multiple clock sources:
 - Internal clock source: LSE, LSI, HSI, PCLK1, COMP1_OUT or COMP2_OUT
 - External clock source: External clock source through LPTIM Input1 (operating without LP oscillator, for pulse counter applications)
- 16-bit auto-load register (LPTIM_ARR)
- 16-bit compare register (LPTIM_COMP)
- Continuous or one-shot mode counting mode
- Programmable software or hardware input trigger
- Programmable digital filter for glitch filtering
- Configurable output (square wave, PWM)
- Configurable IO polarity

- Encoder mode
- Pulse counting mode, support single pulse counting, double pulse counting (quadrature and non-quadrature)

2.13.2 Basic Timer (TIM6 and TIM7)

TIM6 and TIM7 all contain a 16-bit auto-reload counter. These two timers are independent of each other and do not share any resources. The basic timer can provide a time reference for general purpose timers, and for a digital-to-analog converter (DAC). The basic timer is directly connected to the DAC inside the chip and drives the DAC directly through the trigger output.

Main features:

- 16-bit auto-reload up-counting counters
- 16-bit programmable prescaler. (The prescaler factor can be configured with any value between 1 and 65536)
- Synchronization circuit for triggering DAC
- The events that generate the interrupt/DMA are as follows:
 - Update event

2.13.3 General-Purpose Timer (TIMx)

The general-purpose timers (TIM2, TIM3, TIM4, TIM5 and TIM9) are mainly used in the following occasions: counting the input signal, measuring the pulse width of the input signal and generating the output waveform, etc.

Main features:

- 16-bit auto-reload counters. (It can realize up-counting, down-counting, up/down counting)
- 16-bit programmable prescaler. (The prescaler factor can be configured with any value between 1 and 65536)
- TIM2, TIM3, TIM4, TIM5 and TIM9 up to 4 channels
- Channel's working modes: PWM output, output compare, one-pulse mode output, input capture
- The events that generate the interrupt/DMA are as follows:
 - Update event
 - Trigger event
 - Input capture
 - Output compare
- Timers can be controlled by external signal
- Timers can be linked together internally for timer synchronization or chaining
- Incremental (quadrature) encoder interface: used for tracking motion and resolving rotation direction and position
- Hall sensor interface: used to do three-phase motor control
- Supports capture of internal comparator output signals. TIM9 supports capture of internal HSE, LSI, and LSE signals

2.13.4 Advanced Control Timer (TIM1 and TIM8)

The advanced control timers (TIM1 and TIM8) are mainly used in the following occasions: counting the input signal, measuring the pulse width of the input signal and generating the output waveform, etc.

Advanced timers have complementary output function with dead-time insertion and break function. Suitable for motor control.

Main features:

- 16-bit auto-reload counters. (It can realize up-counting, down-counting, up/down counting)
- 16-bit programmable prescaler. (The prescaler factor can be configured with any value between 1 and 65536)
- Programmable Repetition Counter
- TIM1 and TIM8 up to 4 capture/compare channels:
 - PWM output
 - Output compare
 - One-pulse mode output
 - Input capture
- The events that generate the interrupt/DMA are as follows:
 - Update event
 - Trigger event
 - Input capture
 - Output compare
 - Break input
- Complementary outputs with adjustable dead-time
 - For TIM1 and TIM8, channel 1,2,3 support this feature
- Timer can be controlled by external signal
- Timers can be linked together internally for timer synchronization or chaining
- TIM1_CC5 and TIM8_CC5 for COMP blanking
- TIM1_CC6 is used to switch the input channel of OPAMP1 and OPAMP2; TIM8_CC6 can switch the input channel of OPAMP2
- Incremental (quadrature) encoder interface: used for tracking motion and resolving rotation direction and position
- Hall sensor interface: used to do three-phase motor control

2.13.5 SysTick Timer (SysTick)

This timer is dedicated to real-time operating systems and can also be used as a standard down-counter.

Main features:

- 24 bit down-counter
- Automatic reloading function
- A maskable system interrupt is generated when the counter is 0
- Programmable clock source

2.13.6 Watchdog (WDG)

The device supports independent watchdog (IWDG) and window watchdog (WWDG). Two watchdogs provide increased security, time accuracy, and flexibility in use.

Independent watchdog (IWDG)

The independent watchdog is based on a 12-bit down-counter and a 3-bit prescaler. It is driven by a separate low-speed RC oscillator that remains active even if the master clock fails and operates in STOP2 and STANDBY modes. Once activated, if the dog is not fed (clears the watchdog counter) within the set time, the IWDG generates a reset

when the counter counts to 0x000. It can be used to reset the entire system in the event of an application problem, or as a free timer to provide time-out management for applications. The option byte can be configured to start the watchdog software or hardware. Reset and low power wake up are available.

Window watchdog (WWDG)

A window watchdog is usually used to detect software failures caused by an application deviating from the normal running sequence due to external interference or unforeseen logical conditions. Unless the down-counter value is flushed before the T6 bit becomes 0, the watchdog circuit generates an MCU reset when the preset time period is reached. If the 7-bit down-counter value (in the control register) is flushed before the down-counter reaches the window register value, then an MCU reset will also occur. This indicates that the down-counter needs to be refreshed in a finite time window.

Main features:

- The clock of the window watchdog (WWDG) is obtained by dividing the APB1 clock frequency by 4096.
- Programmable free-running down-counter
- Reset condition:
 - When the down-counter is less than 0x40, a reset occurs (if the watchdog is started)
 - A reset occurs when the down-counter is reloaded outside the window (if the watchdog is started)
 - If the watchdog is enabled and interrupts are allowed, an early wake up interrupt (EWINT) occurs when the down-counter equals 0x40, which can be used to reload the counter to avoid WWDG reset

2.14 I²C Bus Interface

Up to two independent I2C bus interfaces can operate in multi-host mode.. It control all I2C bus-specific timing, protocol, arbitration and timeout. Supports multiple communication rate modes (up to 1MHz), supports DMA operations and is compatible with SMBus 2.0. The I2C module provides multiple functions, including CRC generation and verification, SMBus (System Management Bus) and PMBus (Power Management Bus).

Main features:

- Multi-master function: this module can be used as master device or slave device
- I2C master device function:
 - Generate a clock
 - Generate start and stop signals
- I2C slave device function:
 - Programmable address detection
 - The I2C interface supports 7-bit or 10-bit addressing and dual-slave address response capability in 7-bit slave mode
 - Stop bit detection
- Generate and detect 7-bit/10-bit addresses and broadcast calls
- Support different communication speeds
 - Standard speed (up to 100 kHz)
 - Fast (up to 400 kHz)
 - Fast+ (up to 1MHz)
- Status flags:
 - Transmitter/receiver mode flag

- Byte transfer complete flag
- I2C bus busy flag
- Error flags:
 - Arbitration loss in master mode
 - Acknowledge (ACK) fail after address/data transfer
 - Error start or stop condition detected
 - Overrun or underrun when clock extending is disable
- Two interrupt vectors:
 - 1 interrupt for address/data communication success
 - 1 interrupt for an error
- Optional extend clock function
- DMA of single-byte buffers
- Generation or verification of configurable PEC(Packet error detection)
- In transmit mode, the PEC value can be transmitted as the last byte
- PEC error check for the last received byte
- SMBus 2.0 compatible
 - Timeout delay for 25ms clock low
 - 10ms accumulates low clock extension time of master device
 - 25ms accumulates low clock extension time of slave device
 - PEC generation/verification of hardware with ACK control
 - Support address resolution protocol (ARP)
- Compatible with the PMBus

2.15 Universal Synchronous/Asynchronous Transceiver (USART)

N32L40x series products integrate up to 5 serial transceiver interfaces, including 3 universal synchronous/asynchronous transceivers (USART1, USART2 and USART3) and 2 universal asynchronous transceivers (UART4 and UART5). All five interfaces provide asynchronous communication, support for IrDA SIR ENDEC transmission codec, multi-processor communication mode, single-wire half-duplex communication mode, and LIN master/slave function.

The USART1, USART2, and USART3 interfaces have hardware CTS and RTS signal management, ISO7816-compatible smart card mode, and similar to SPI communication mode, all of which can use DMA operations.

Main features:

- Full duplex, asynchronous communication
- NRZ standard format
- Fractional baud rate generator system, baud rate programmable, used for sending and receiving
- Programmable data word length (8 or 9 bits)
- Configurable stop bit, supporting 1 or 2 stop bits
- LIN master's ability to send synchronous interrupters and LIN slave's ability to detect interrupters. When USART hardware is configured as LIN, it generates 13 bit interrupters and detects 10/11 bit interrupters

- Output clock for synchronous transmission
- IRDA SIR encoder decoder, supports 3/16 bit duration in normal mode
- Smart card simulation function:
 - The smart card interface supports the asynchronous smart card protocol defined in ISO7816-3
 - 0.5 and 1.5 stop bits for smart cards
- Single-wire half duplex communication
- Configurable multi-buffer communication using DMA, receiving/sending bytes in SRAM using centralized DMA buffer
- Independent transmitter and receiver enable bits
- Detect flag:
 - Receive buffer is full
 - Send buffer empty
 - Transmission complete
- Parity control:
 - Send parity bit
 - Check the received data
- Four error detection flags:
 - Overflow error
 - Noise error
 - Frame error
 - Parity error
- 10 USART interrupt sources with flags:
 - CTS change
 - LIN break detection
 - Send data register empty
 - Send complete
 - Received data register is full
 - Bus was detected to be idle
 - Overflow error
 - Frame error
 - Noise error
 - Parity error
- Multi-processor communication, if the address does not match, then enter the silent mode
- Wake up from silent mode (via idle bus detection or address flag detection)
- Mode configuration:

USART modes	USART1	USART2	USART3	UART4	UART5
Asynchronous mode	support	support	support	support	support
Hardware flow control	support	support	support	nonsupport	nonsupport
Multiple buffer communication (DMA)	support	support	support	support	support
Multiprocessor communication	support	support	support	support	support
Synchronous mode	support	support	support	nonsupport	nonsupport
Smart card	support	support	support	nonsupport	nonsupport
Half duplex (Single wire mode)	support	support	support	support	support
IrDA	support	support	support	support	support
LIN	support	support	support	support	support

2.16 Low Power Asynchronous Transceiver (LPUART)

The device integrates a low-power asynchronous serial transceiver (LPUART), which can receive data in STOP2 state (maximum baud rate 9600) and wake up MCU after generating an interrupt event. In addition, by configuring the clock as a high-speed clock (such as APB or HSE clock), it can be used as a regular asynchronous serial port to support higher baud rate.

Main features:

- Provide standard asynchronous communication bits (start, parity, and stop bits)
 - Generates 1 start bit
 - Generates 1-bit parity bit (odd or even parity can be set) or no parity bit
 - Generates 1 stop bit
 - Bytes are transmitted from the lowest to the highest
- Support 32 bytes receive FIFO and 1 byte Transmit FIFO
- Provides transmit mode control bits
- Programmable baud rate
- Full duplex communication
- Support data communication and error handling interruption
- Access to status bits can be done in two ways: query or interrupt
- Parity error flag
- Baud rate parameter register
- Support hardware flow control
- Support DMA data transfer
- Support the following interrupt event sources to wake up the MCU in STOP2 state:
 - Start bit detection
 - Receive buffer non-empty detection
 - Received the specified 1 bytes of data
 - Received the specified 4 bytes of data

2.17 Serial Peripheral Interface (SPI)

The device integrates two SPI interfaces, which allow the chip to communicate with peripheral devices in a half/full duplex, synchronous, serial manner modes. This interface can be configured in master mode and provides a communication clock (SCK) for external slave devices. Interfaces can also work in a multi-master configuration. It can be used for a variety of purposes, including two-line simplex synchronous transmission using a two-way data line, and reliable communication using CRC checks.

Main features:

- 3-wire full-duplex synchronous transmission
- Two-wire simplex synchronous transmission with or without a third bidirectional data line
- 8 or 16 bit transmission frame format selection
- Master or slave operations
- Support multi-master mode
- 8 master mode baud rate prescaler coefficient ($\text{Max } f_{\text{CLK}}/2$)
- Slave mode frequency ($\text{Max } f_{\text{CLK}}/2$)
- Fast communication between master mode and slave mode
- NSS can be managed by software or hardware in both master and slave modes: dynamic change of master/slave modes
- Programmable clock polarity and phase
- Programmable data order, MSB before or LSB before
- Dedicated send and receive flags that trigger interrupts
- SPI bus busy flag
- Hardware CRC for reliable communication:
 - In send mode, the CRC value can be sent as the last byte
 - In full-duplex mode, CRC is automatically performed on the last byte received
- Master mode failures, overloads, and CRC error flags that trigger interrupts
- Single-byte send and receive buffer with DMA capability: generates send and receive requests
- Maximum interface speed: 16Mbps

2.18 Serial Audio Interface (I²S)

I²S is a 3-pin synchronous serial interface communication protocol. The device integrates two standard I²S interfaces (multiplexed with SPI) and can operate in master or slave mode. The two interfaces can be configured for 16-bit, 24-bit or 32-bit transmission, or as input or output channels, supporting audio sampling frequencies from 8kHz to 96kHz. It supports four audio standards, including Philips I²S, MSB and LSB alignment, and PCM.

In half duplex communication, it can operate in two modes: master and slave. When it acts as a master device, it provides clock signals to external slave devices through an interface.

Main features:

- Simplex communication (send or receive only)
- Master or slave operations
- 8-bit linear programmable prescaler for accurate audio sampling frequencies (8KHz to 96KHz)

- The data format is 16, 24, or 32 bits
- Audio packet frame is 16 bit (16 bit data frame) or 32 bit (16, 24 or 32 bit data frame)
- Programmable clock polarity (steady state)
- The overflows flag bit in slave sending mode and the overflows flag bit in master/slave receiving mode
- 16-bit data registers are used for sending and receiving, with one register at each end of the channel
- Supported I²S protocols:
 - I²S Philips standard
 - MSB alignment standard (left aligned)
 - LSB alignment standard (right aligned)
 - PCM standard (16-bit channel frame with long or short frame synchronization or 16-bit data frame extension to 32-bit channel frame)
- The data direction is always MSB first
- Both send and receive have DMA capability
- The master clock can be output to external audio devices at a fixed rate of 256xFs(Fs is the audio sampling frequency)

2.19 Controller Area Network (CAN)

Device integrates a CAN bus interface compatible with 2.0A and 2.0B (active) specifications, with bit rates up to 1Mbps. It can receive and send 11 bit standard frames identifiers, as well as extended frames with 29-bit identifiers.

Main features:

- Support CAN protocol 2.0A and 2.0B active mode
- Baud rate up to 1Mbps
- Supports time-triggered communication
- Send:
 - Three sending mailboxes
 - The priority of sent packets can be configured by software
 - Records the timestamp of the time when the SOF was sent
- Receive:
 - Level 3 depth of 2 receiving FIFO
 - Variable filter group
 - There are 14 filter groups
 - Identifier list
 - The FIFO overflow processing mode is configurable
 - Record the time stamp of the receipt of the SOF
- Time-triggered communication mode:
 - Disable automatic retransmission mode
 - 16-bit free run timer

- Timestamp can be sent in the last 2 bytes of data
- Management:
 - Interrupt masking
 - The mailbox occupies a separate address space to improve software efficiency

2.20 Universal Serial Bus (USB)

Device is embedded with a full speed USB compatible device controller.. The endpoint can be configured by software and support suspend/resume function. The USB dedicated 48MHz clock is generated by internal PLL.

Main features:

- Comply with the technical specifications of USB2.0 full-speed equipment
- 1 to 8 USB endpoints can be configured
- CRC(cyclic redundancy check) generation/check, reverse non-return to zero (NRZI) encoding/decoding and bit filling
- Double buffer mechanism for bulk/isochronous endpoints
- Support USB suspend/resume operation
- Frame lock clock pulse generation
- Integrated USB DP signal line pull-up 1.5K resistor (user can enable or disable through software control)

2.21 General Purpose Input/Output Interface (GPIO)

Up to 64 GPIO, which can be divided into four groups (GPIOA/GPIOB/GPIOC/GPIOD). There are 16 ports for each group. Each GPIO pin can be configured by software as an output (push pull or open drain), input (with or without pull-up or pull-down), or alternate peripheral function port. Most GPIO pins are shared with digital or analog alternate peripherals, and some I/O pins are multiplexed with clock pins. All GPIO pins except ports with analog input capability have high current passing capability.

Main features:

- Each bit of the GPIO port can be configured separately by the software into multiple modes:
 - Input floating
 - Input pull up (weak pull up)
 - Input pull down (weak pull down)
 - Analog function
 - Open drain output
 - Push-pull output
 - Push-pull alternate function
 - Open drain alternate function
- General I/O (GPIO)
 - During and just after reset, the alternate function is not enabled, except for BOOT0 (which is an input pull-down), and the I/O port is configured to analog input mode

- After reset, the default state of pins associated with the debug system is enable SWJ, the JTAG pin is placed in input pull-up or pull-down mode:
 - JTDI in pull-up mode
 - JTCK in pull-down mode
 - JTMS in pull-up mode
 - NJTRST in pull-up mode
- When configured as output, values written to the output data registers are output to the appropriate I/O pins. Can be output in push pull mode or open drain mode
- Separate bit setting or bit clearing functions
- External interrupt/wake up: All ports have external interrupt capability. In order to use external interrupts, ports must be configured in input mode
- Alternate function: (port bit configuration register must be programmed before using default alternate function)
- GPIO lock mechanism, which freezes I/O configurations. When a LOCK is performed on a port bit, the configuration of the port bit cannot be changed until the next reset

2.22 Segment LCD Driver (Segment LCD)

The LCD controller is suitable for monochrome passive Segment LCD, with a maximum of 8 common terminals (COM) and 44 Segment terminals (SEG), the specific number of terminals depends on the package of pin. The Segment LCD consists of a number of segments that can be turned on or off. Each segment contains a layer of liquid crystal molecules aligned between the two electrodes. The corresponding segment is visible when a voltage greater than the threshold voltage is applied to the liquid crystal. To avoid electrophoretic effects in the liquid crystal, the segment voltage must be AC. The LCD controller can work in low power mode except STANDBY mode.

Main features:

- Frame rate is configurable
- Duty cycle is configurable: static, 1/2, 1/3, 1/4 and 1/8 duty cycle are supported
- Voltage bias can be configured: static, 1/2, 1/3 and 1/4 bias are supported
- Double buffering mechanism allows the user to update the data (pixel active/inactive information) in the display memory registers at any time
- LCD power supply optional: add power supply from V_{LCD} pin (you can also connect V_{LCD} directly to VDD); Use a built-in DC-DC step-up converter (external 1 μ F capacitor is required)
- LCD clock source Optional: HSE/32, LSI, or LSE
- Two contrast control methods: adjust dead time of up to 7 phase cycles between frames; adjust V_{LCD} in $V_{LCDmin} \sim V_{LCDmax}$ range (when using internal step-up converter only)
- Built-in resistor network is used to generate LCD intermediate voltage, which can be configured by software to match the capacitive load of LCD panel
- Built-in voltage output buffer
- It can be displayed in SLEEP, LOW-POWER RUN, LOW-POWER SLEEP, and STOP2 modes. It can also be disabled in these modes for lower POWER consumption
- Built-in phase inversion reduces electromagnetic interference (EMI) and power consumption

- Support blink function: 1, 2, 3, 4, 8 or all pixels can blink at the specified frequency (0.5Hz, 1Hz, 2Hz or 4Hz)
- Pins used for SEG and COM functions should be configured with the appropriate AFIO

2.23 Analog/Digital Converter (ADC)

The device embeds a 12-bit 4.5MSPS successive approximation register ADC

Main features:

- Single-end and differential mode inputs
- 16 external channels and 3 internal channels
- 4 resolutions with maximum conversion rate:
 - 12 bit: 5.14MSPS
 - 10bit: 6MSPS
 - 8bit: 7.2MSPS
 - 6bit: 9MSPS
- Three clock sources for ADC:
 - Operating clock, configured by AHB_CLK, up to 108MHz
 - Sampling clock source:
 - configured by PLL, up to 72MHz, multiple division factors : 1,2,4,6,8,10,12,16,32,64,128,256
 - configured by AHB_CLK, up to 72MHz, multiple division factors : 1,2,4,6,8,10,12,16,32,
- 1MHz fix clock for ADC internal timing function timer trigger ADC sampling
- 2.048V internal reference voltage $V_{REFBUFFER}$
- Interruption generated when regular or injection channel conversion ends Single and continuous conversion modes
- Automatic scan mode from channel 0 to channel N
- for self-calibration
- Data alignment with embedded data consistency
- Sampling intervals can be programmed separately for each channel
- Both regular conversions and injection conversions have external triggering options
- Discontinuous mode ADC power supply range: 1.8V to 3.6V
- ADC input range: $V_{REF-} \leq V_{IN} \leq V_{REF+}$
- ADC can use DMA operations, and DMA requests are generated during regular channel conversion

Analog watchdog for monitoring one, multiple, or all selected channels with great precision. When the monitored signal exceeds the preset threshold, an interruption will be generated

-

2.24 Operational Amplifier (OPAMP)

The device embeds 2 independent operational amplifiers with capability

Main features:

- rail to rail input
- Forward and reverse input checkboxes
 - operationg mode Independent mode (external gain setting)
 - PGA mode, programmable gain 2X, 4X, 8X, 16X, 32X
 - Follower mode

The internally connected ADC channel is used to measure the output signal of the operational amplifier

2.25 Analog Comparator (COMP)

The device embeds 2 comparators, among which COMP1 supports low power mode and can work in STOP2 state. It can be used as a separate device (all ports of the comparator are plugged into the I/O) or in combination with a timer. In the case of motor control, it can be combined with the PWM output from the timer to form periodic current control.

Main features:

- Rail to rail comparators
- The reverse and forward sides of the comparator support the following inputs
 - External I/O
 - DAC channel output
 - Internal 64 level adjustable voltage:
 - VREF1 is a low-power voltage reference source, which can only be used for COMP1
 - VREF2 is a non-low power voltage reference source, which can be used for COMP1 and COMP2
- Programmable hysteresis : no hysteresis, low hysteresis, medium hysteresis, and high hysteresis
- The comparator can output to EITHER I/O or timer input for triggering
 - Capture events
 - OCREF_CLR events (for periodic current control)
 - The brake events
- output filtering, including analog and digital filtering
- COMP1/COMP2 can form a window comparator
- output with blanking, Timer1_OC5, Timer8_OC5 can be choose as blanking input. Blanking function can be disabled
- interrupt wake up capability, wake up from SLEEP mode, COMP1 can wake up from STOP2
-

2.26 Digital/Analog Converter (DAC)

The device embeds a 12bit digital to analog converter, with internal buffer output channel. DAC can be referenced via V_{DDA} or $V_{REFBUFFER}$.

Main features:

- built-in Buffer output channel
- 8/12-bits output mode
- left or right data alignment in 12-bit mode
- Synchronizes update function
- noise wave generation
- triangular wave generation
- DMA capability

External trigger for conversion

2.27 Temperature Sensor (TS)

The temperature sensor generates a voltage that varies linearly with temperature in the range of $1.8V < V_{DDA} < 3.6V$. The temperature sensor is internally connected to the ADC_IN17 input channel for converting the output of the temperature sensor to digital values.

2.28 Cyclic Redundancy Check Calculation unit (CRC)

The device integrates CRC32 and CRC16 functionalities. The cyclic redundancy check (CRC) calculation unit is based on a fixed generation polynomial to obtain any CRC calculation results. In many applications, CRC-based techniques are used to verify data transfer or storage consistency. Within the scope of the EN/IEC 60335-1 standard, which provides a means of detecting Flash memory errors. The CRC unit can be used to calculate signatures of software in real time and compare them with signatures generated when link-time and generating of the software.

Main features:

- CRC16: supports polynomials $X^{16} + X^{15} + X^2 + 1$
- CRC32: supports polynomials $X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$
- CRC16 calculation time: 1 AHB clock cycles (HCLK)
- CRC32 calculation time: 1 AHB clock cycles (HCLK)
- The initial value for cyclic redundancy computing is configurable
- Support DMA mode

2.29 Security Acceleration Engine (SAC)

The device features an embedded algorithm hardware acceleration engine. It supports a variety of international algorithms hash cryptography algorithm acceleration, which can greatly improve the speed of encryption and decryption compared with pure software algorithm.

The hardware supports the following algorithms:

- Supports DES symmetric algorithms
 - DES and 3DES encryption and decryption operations are supported
 - TDES supports 2KEY and 3KEY mode
 - Supports CBC and ECB mode
- Supports the SYMMETRIC AES algorithm
 - Supports 128bits, 192bits, or 256bits key length
 - Supports CBC, ECB, and CTR mode
- SHA hash algorithm is supported
 - Supports SHA1, SHA244, SHA256
- Supports the MD5 digest algorithm
- Supports symmetric SM1, SM4, SM7 algorithm and SM3 hash algorithm

2.30 Unique Device Serial Number (UID)

The N32L40x series products have two built-in unique device serial numbers of different lengths, which are 96-bit unique device ID (UID) and 128-bit unique customer ID (UCID). These two device serial numbers are stored in the system configuration block of Flash memory. The information they contain is written at the time of delivery and is guaranteed to be unique to any of the N32L40x series microcontrollers under any circumstances and can be read by user applications or external devices through the CPU or JTAG/SWD interface and cannot be modified.

The 96-bit UID is usually used as a serial number or password. When writing Flash memory, this unique identifier is combined with software encryption and decryption algorithm to further improve the security of code in Flash memory. It can also be used to activate Secure Bootloader with security functions.

The UCID is 128-bit, which complies with the definition of national technology chip serial number. It contains the information related to chip production and version.

2.31 Serial Single-Wire JTAG Debug Port (SWJ-DP)

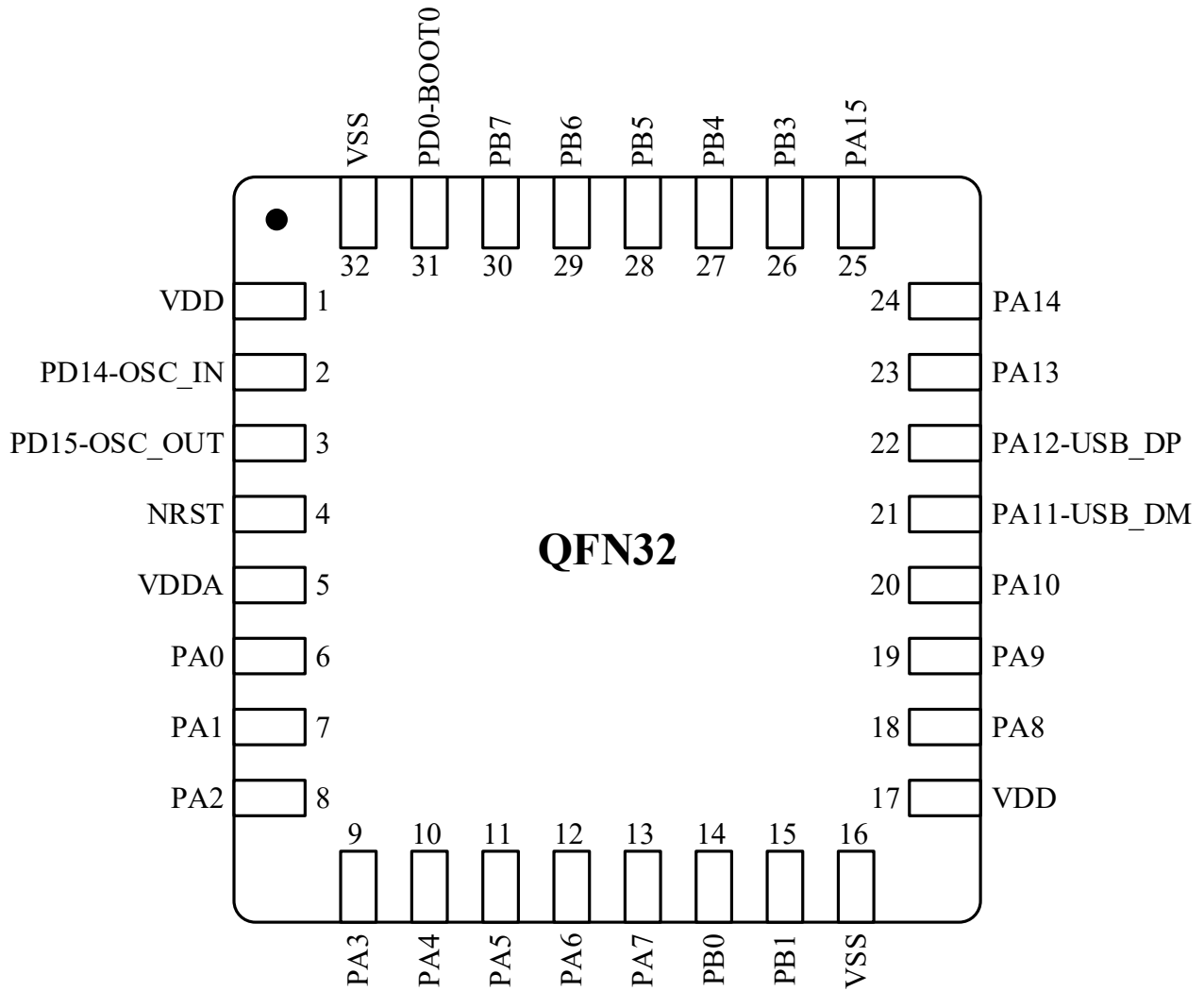
The device has an embedded ARM SWJ-DP interface, which is a combination of JTAG and serial single-wire debugging interface, can achieve serial single-line debugging interface or JTAG interface connection. The JTMS and JTCK signals of JTAG share pins with SWDIO and SWCLK respectively, and a special signal sequence on the JTMS pin is used to switch between JTAG-DP and SW-DP.

3 Pin and description

3.1 Pinouts

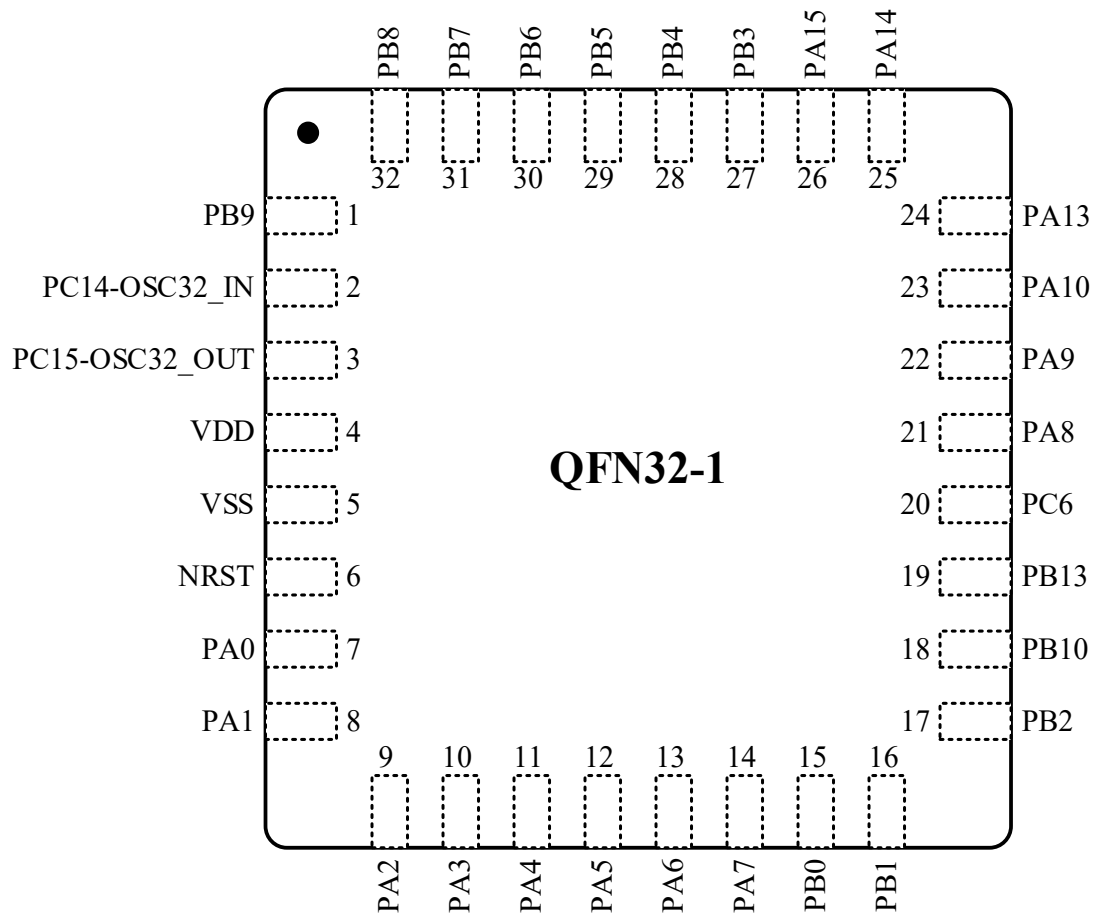
3.1.1 QFN32 (4mm x 4mm)

Figure 3-1 N32L403 (4mm x 4mm) Series QFN32 Pinout



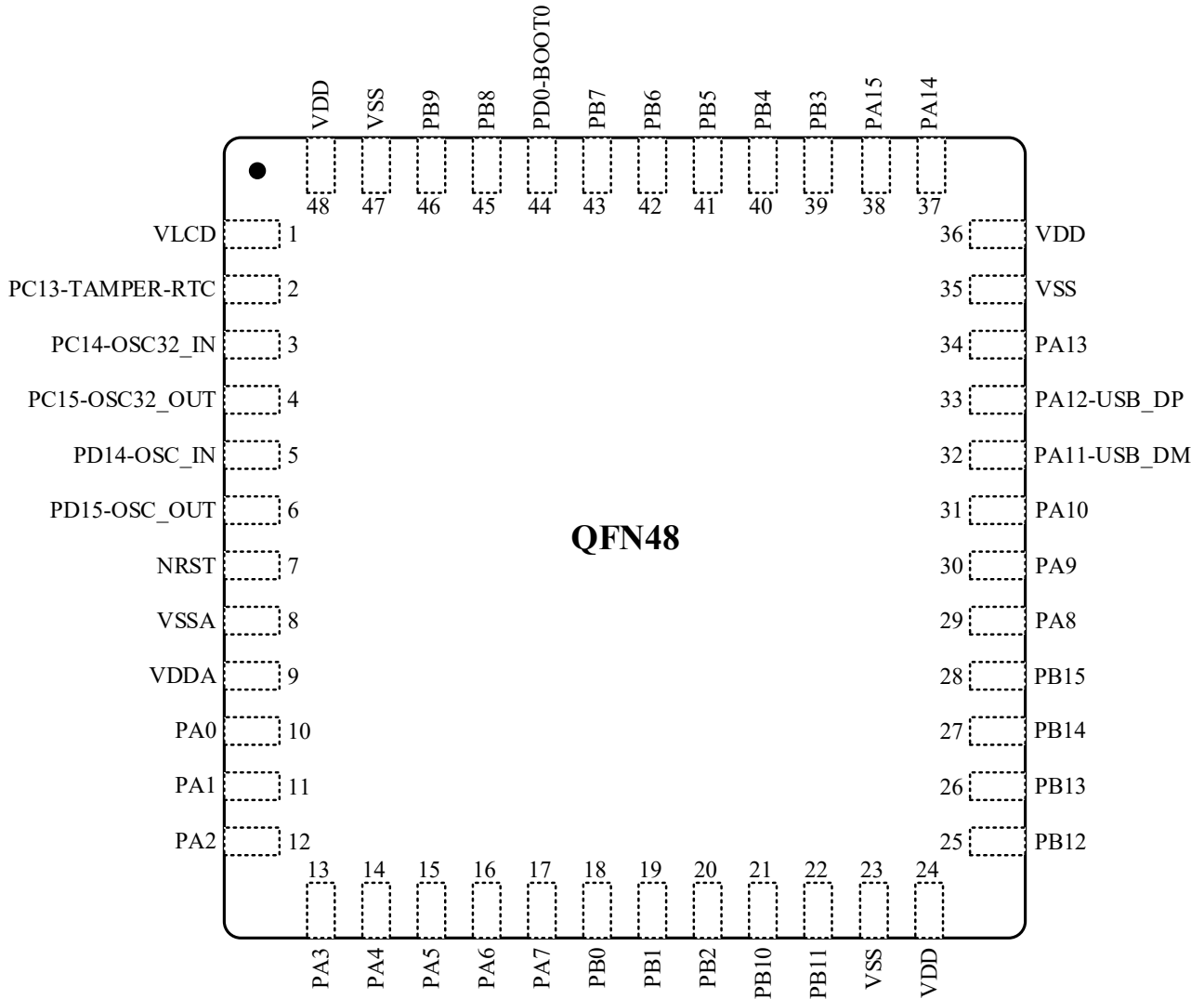
3.1.2 QFN32 (5mm x 5mm)

Figure 3-2 N32L403 (5mm x 5mm) Series QFN32 pinout



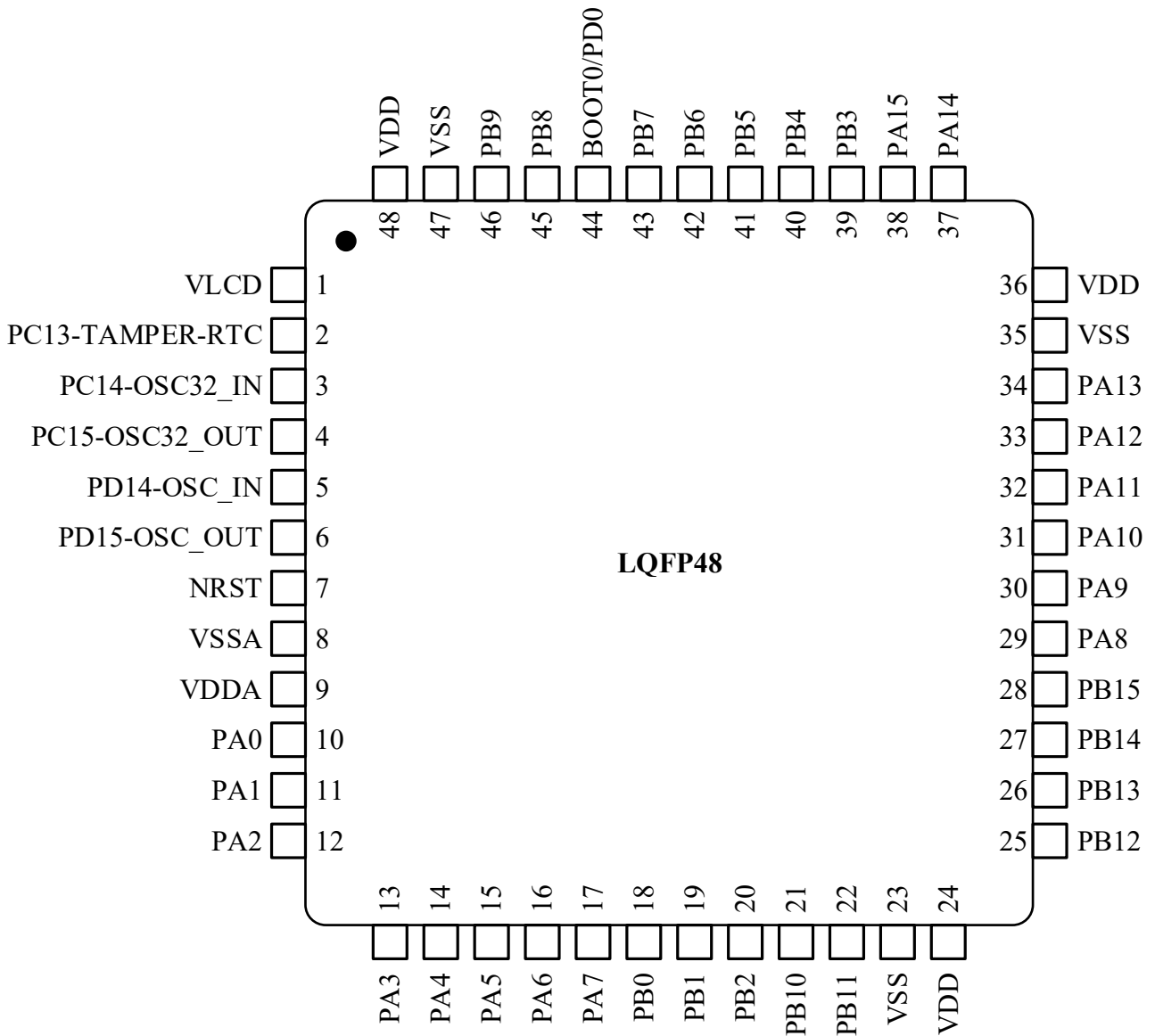
3.1.3 QFN48 (with LCD)

Figure 3-3 N32L402/N32L406 Series QFN48 Pinout



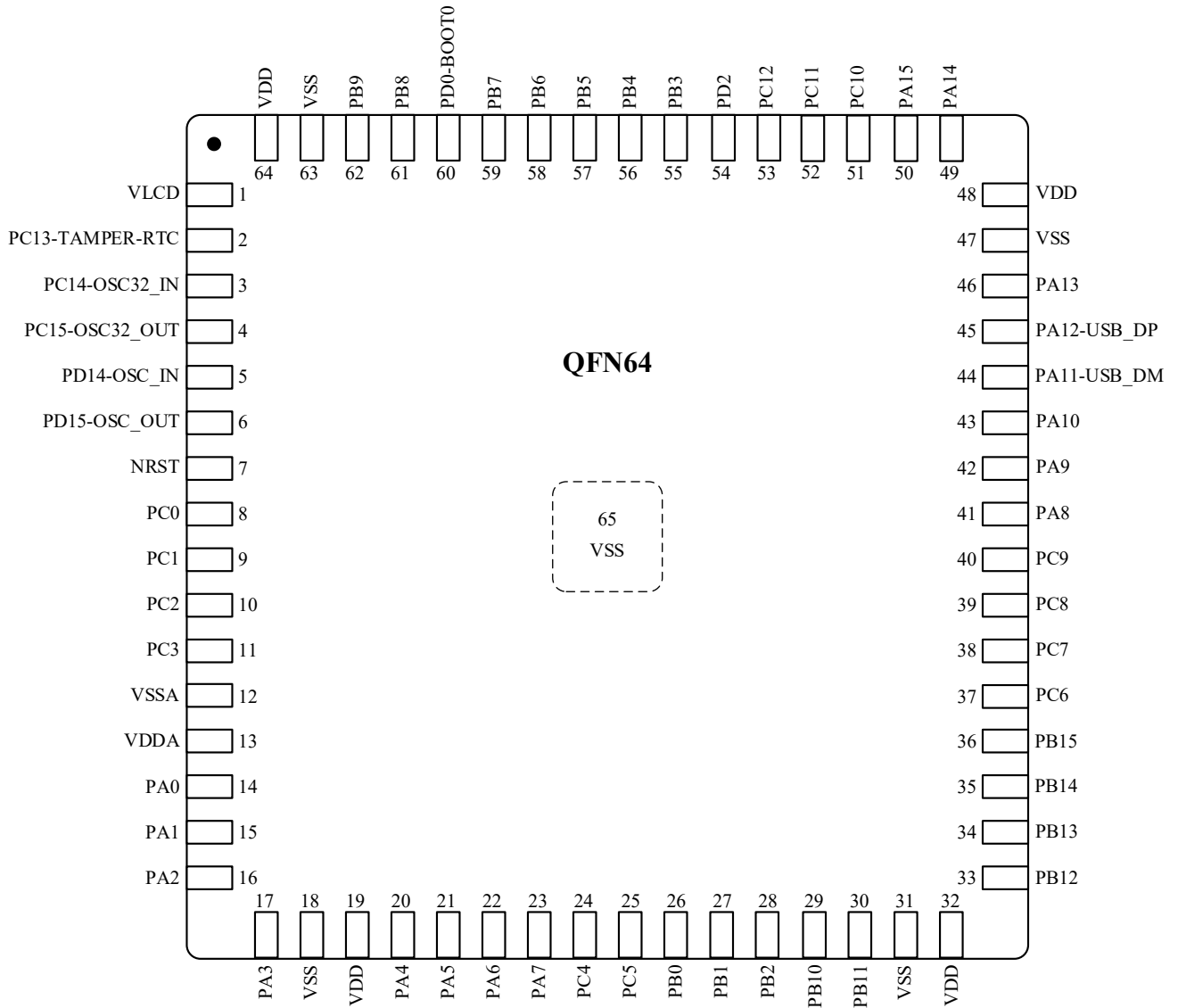
3.1.4 LQFP48 (with LCD)

Figure 3-4 N32L402/N32L406 Series LQFP48 Pinout



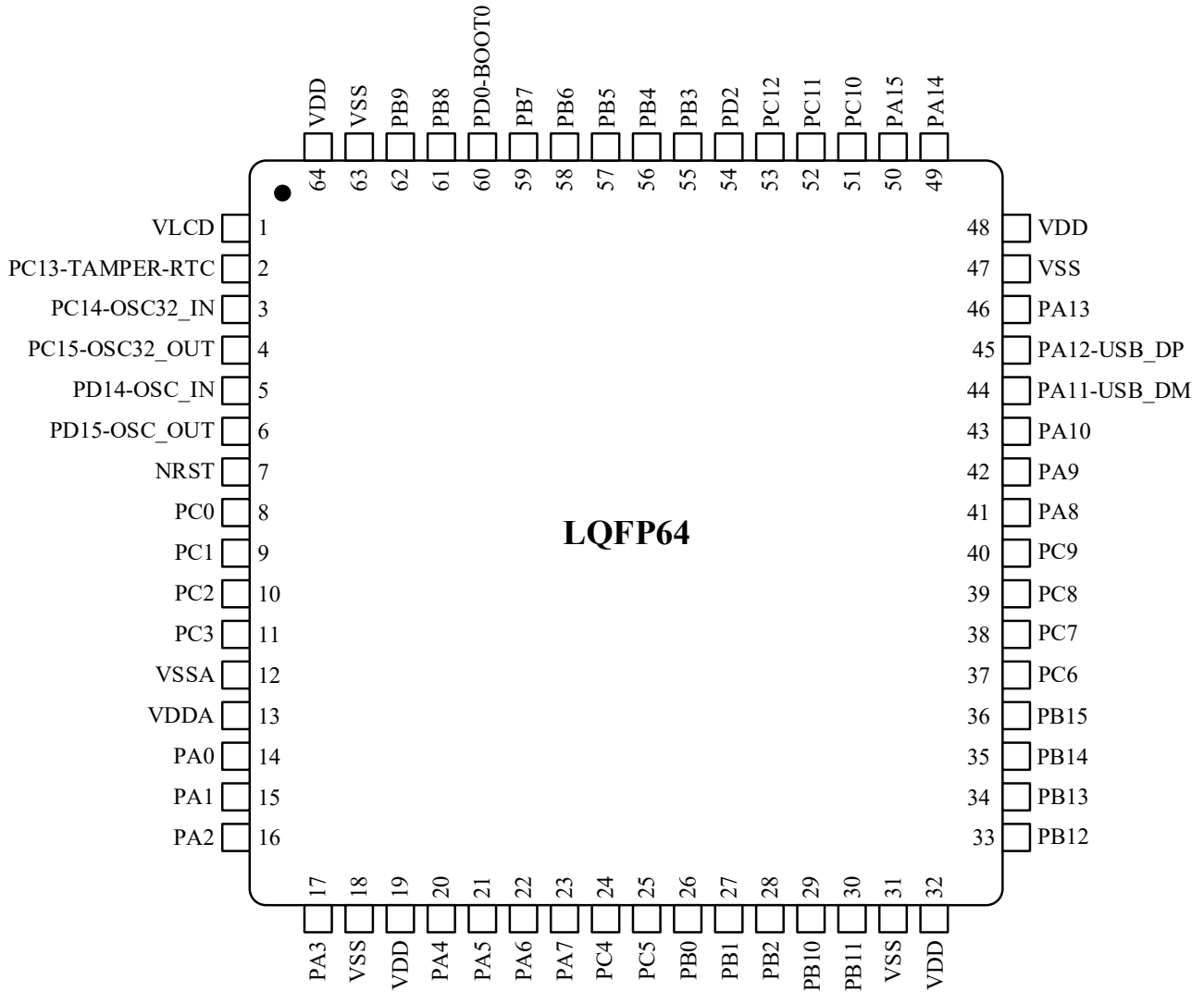
3.1.5 QFN64 (8mm x 8mm)

Figure 3-5 N32L406 (8mm x 8mm) Series QFN64 Pinout



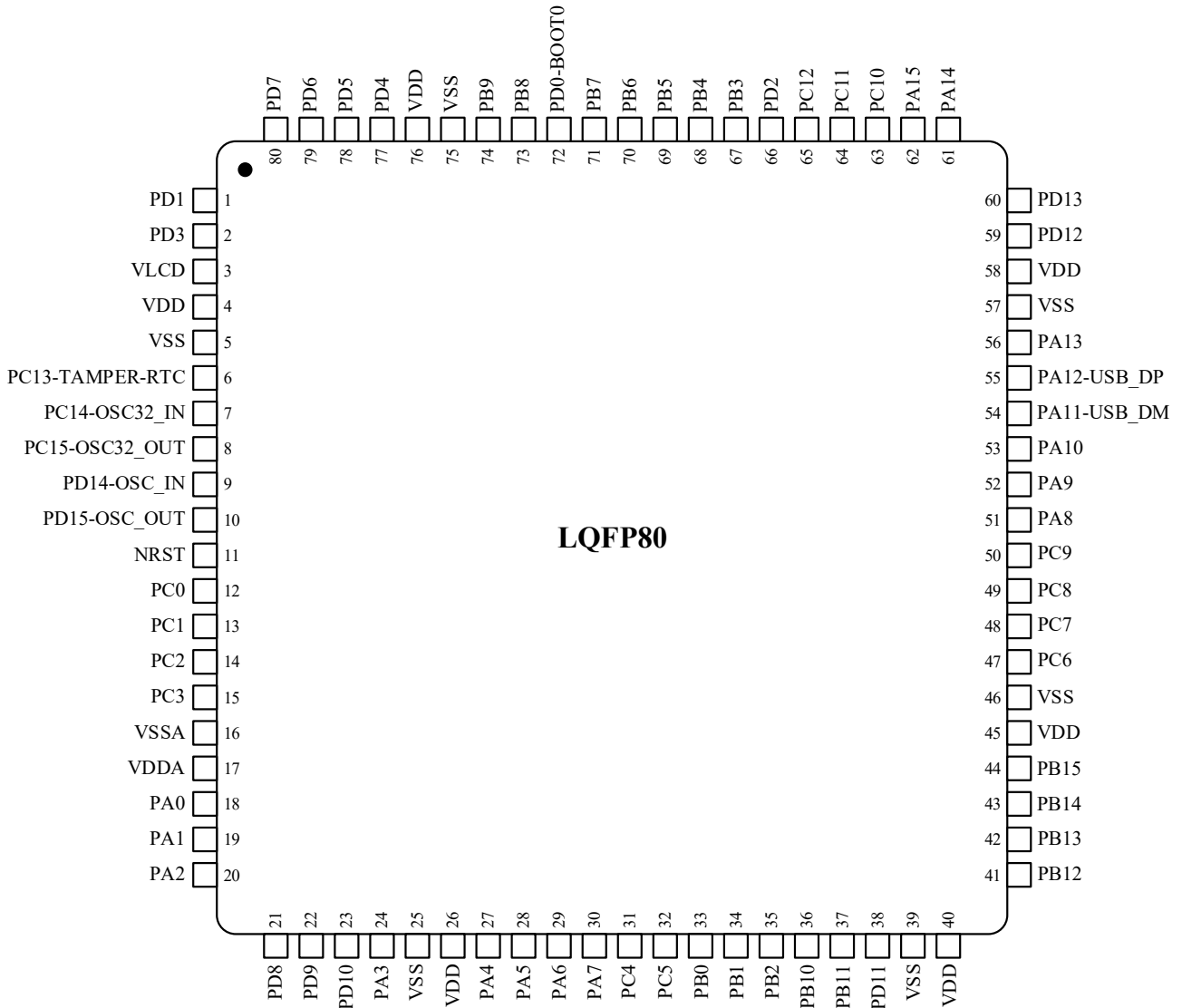
3.1.6 LQFP64 (10mm x 10mm)

Figure 3-6 N32L402/N32L406 (10mm x 10mm) Series LQFP64 Pinout



3.1.7 LQFP80 (12mm x 12mm)

Figure 3-7 N32L406 (12mm x 12mm) Series LQFP80 Pinout



3.2 Pin Description

Table 3-1 Pin Description

QFN32	QFN32 ⁽¹¹⁾	QFN48	LQFP48	QFN64	LQFP64	LQFP80	Pin Name (after reset)	Type ⁽¹⁾	I/O structure ⁽²⁾	Fail-safe ⁽⁴⁾ support	Alternate function ⁽³⁾	Optional function
-	-	-	-	-	-	1	PD1 ⁽¹⁰⁾	I/O	TTa	Yes	TRACED0 LCD_SEG33	-
-	-	-	-	-	-	2	PD3 ⁽¹⁰⁾	I/O	TTa	Yes	TRACED1 USART2_CTS LCD_SEG34	-
-	-	1	1	-	-	3	VLCD	S	-	-	-	-
1	4	-	-	-	-	4	VDD	S	-	-	-	-
33	5	49	65	-	-	5	VSS	S	-	-	-	-
-	-	2	2	-	-	6	PC13-TAMPER- RTC ⁽¹⁰⁾	I/O	TTa	Yes	TIM1_CH1N LCD_SEG35 EVENTOUT	TAMP1-RTC RTC_OUT WKUP2
-	2	3	3	-	-	7	PC14- OSC32_IN	I/O	TTa	Yes	-	OSC32_IN
-	3	4	4	-	-	8	PC15- OSC32_OUT	I/O	TTa	Yes	-	OSC32_OUT
2	-	5	5	-	-	9	PD14-OSC_IN	I/O	TTa	No	USART2_TX I2C2_SDA TIM1_CH3N	OSC_IN
3	-	6	6	-	-	10	PD15-OSC_OUT	I/O	TTa	No	USART2_RX I2C2_SCL	OSC_OUT
4	6	7	7	-	-	11	NRST	I	-	-	-	-
-	-	-	8	-	-	12	PC0 ⁽¹⁰⁾	I/O	TTa	Yes	I2C1_SCL LPTIM_IN1 LCD_SEG18 EVENTOUT	ADC_IN11 ⁽⁹⁾
-	-	-	9	-	-	13	PC1 ⁽¹⁰⁾	I/O	TTa	Yes	LPTIM_OUT I2C1_SDA LCD_SEG19 EVENTOUT	ADC_IN12 ⁽⁹⁾
-	-	-	10	-	-	14	PC2 ⁽¹⁰⁾	I/O	TTa	Yes	LCD_SEG20 EVENTOUT LPTIM_IN2	ADC_IN13 ⁽⁹⁾
-	-	-	11	-	-	15	PC3 ⁽¹⁰⁾	I/O	TTa	Yes	LCD_SEG21 LPTIM_ETR EVENTOUT	ADC_IN14 ⁽⁹⁾
-	5	8	12	-	-	16	VSSA/VREF-	S	-	-	-	-
5	4	9	13	-	-	17	VDDA/VREF+	S	-	-	-	-
6	7	10	14	-	-	18	PA0	I/O	TTa	Yes	USART2_CTS LPUART_RX TIM2_CH1 TIMER2_ETR TIM5_CH1 TIM8_ETR SPI1_MISO I2S1_MCK EVENTOUT COMP1_OUT	ADC_IN1 ⁽⁸⁾ COMP1_INM COMP1_INP WKUP1 TAMP2-RTC
7	8	11	15	-	-	19	PA1	I/O	TTa	Yes	USART2_RTS LPUART_TX TIM5_CH2 TIM2_CH2 LCD_SEG0 EVENTOUT	ADC_IN2 ⁽⁸⁾ COMP1_INP OPAMP1_VINP
8	9	12	16	-	-	20	PA2	I/O	TTa	Yes	USART2_TX TIM5_CH3	ADC_IN3 ⁽⁸⁾ OPAMP1_VOUT

QFN32	QFN32 ⁽¹¹⁾	QFN48	LQFP48	QFN64	LQFP64	LQFP80	Pin Name (after reset)	Type ⁽¹⁾	I/O structure ⁽²⁾	Fail-safe ⁽⁴⁾ support	Alternate function ⁽³⁾	Optional function
-	-	-	-	-	-	-					TIM2_CH3 LCD_SEG1 I2C2_SDA COMP2_OUT EVENTOUT	COMP1_INP ⁽⁶⁾ COMP2_INM
-	-	-	-	-	-	21	PD8 ⁽¹⁰⁾	I/O	TTa	Yes	LCD_SEG36	-
-	-	-	-	-	-	22	PD9 ⁽¹⁰⁾	I/O	TTa	Yes	LCD_SEG37	-
-	-	-	-	-	-	23	PD10 ⁽¹⁰⁾	I/O	TTa	Yes	LCD_SEG38	-
9	10	13	17	24			PA3	I/O	TTa	Yes	USART2_RX LPUART_RX TIM5_CH4 LCD_SEG2 I2C2_SCL EVENTOUT	ADC_IN4 ⁽⁸⁾ COMP1_INP ⁽⁷⁾ COMP2_INP OPAMP1_VINM
-	-	-	18	25			VSS	S	-	-	-	-
-	-	-	19	26			VDD	S	-	-	-	-
10	11	14	20	27			PA4	I/O	TTa	No	USART2_CK LPUART_TX I2C1_SCL SPI1_NSS I2S1_WS USART1_TX EVENTOUT	DAC_OUT ADC_IN5 ⁽⁸⁾ COMP1_INM COMP2_INM OPAMP1_VINP OPAMP2_VINP
11	12	15	21	28			PA5	I/O	TTa	Yes	SPI1_SCK I2C1_SDA I2S1_CK USART1_RX EVENTOUT	ADC_IN6 ⁽⁹⁾ COMP1_INM COMP2_INM OPAMP1_VINP OPAMP2_VINM
12	13	16	22	29			PA6	I/O	TTa	Yes	LPUART_CTS SPI1_MISO I2S1_MCK TIM8_BKIN TIM3_CH1 TIM1_BKIN LCD_SEG3 COMP2_OUT EVENTOUT	ADC_IN7 ⁽⁹⁾ OPAMP2_VOUT COMP2_INM COMP2_INP
13	14	17	23	30			PA7	I/O	TTa	Yes	SPI1_MOSI I2S1_SD TIM1_CH1N TIM8_CH1N TIM3_CH2 LCD_SEG4 COMP2_OUT EVENTOUT	ADC_IN8 ⁽⁹⁾ COMP2_INP OPAMP1_VINP OPAMP2_VINP
-	-	-	24	31			PC4 ⁽¹⁰⁾	I/O	TTa	Yes	LPUART_TX I2C1_SCL LCD_SEG22 EVENTOUT	ADC_IN15 ⁽⁹⁾
-	-	-	25	32			PC5	I/O	TTa	Yes	LPUART_RX I2C1_SDA LCD_SEG23 EVENTOUT	ADC_IN16 ⁽⁹⁾ OPAMP1_VINM OPAMP2_VINM
14	15	18	26	33			PB0	I/O	TTa	Yes	TIM1_CH2N TIM3_CH3 TIM8_CH2N LCD_SEG5	ADC_IN9 ⁽⁹⁾ OPAMP2_VINM

QFN32	QFN32 ⁽¹⁾	QFN48	LQFP48	QFN64	LQFP64	LQFP80	Pin Name (after reset)	Type ⁽¹⁾	I/O structure ⁽²⁾	Fail-safe ⁽⁴⁾ support	Alternate function ⁽³⁾	Optional function
											UART4_TX EVENTOUT	
15	16	19	27	34			PB1 ⁽¹⁰⁾	I/O	TTa	Yes	LPUART_RTS TIM1_CH3N TIM3_CH4 TIM8_CH3N LCD_SEG6 UART4_RX EVENTOUT	ADC_IN10 ⁽⁹⁾
-	17	20	28	35			PB2	I/O	TTa	Yes	LPTIM_OUT TIM9_ETR EVENTOUT	-
-	18	21	29	36			PB10	I/O	TTa	Yes	USART3_TX LPUART_TX I2C2_SCL LCD_SEG10 TIM2_CH3 EVENTOUT	COMP1_INP
-	-	22	30	37			PB11 ⁽¹⁰⁾	I/O	TTa	Yes	USART3_RX LPUART_RX I2C2_SDA TIM2_CH4 LCD_SEG11 EVENTOUT	-
-	-	-	-	38			PD11 ⁽¹⁰⁾	I/O	TTa	Yes	LCD_SEG39	-
16	-	23	31	39			VSS	S	-	-	-	-
-	-	24	32	40			VDD	S	-	-	-	-
-	-	25	33	41			PB12 ⁽¹⁰⁾	I/O	TTa	Yes	SPI2_NSS I2S2_WS I2C2_SMBA USART3_CK TIM1_BKIN LPUART_RTS LCD_SEG12 TIM9_CH1 EVENTOUT	-
-	19	26	34	42			PB13 ⁽¹⁰⁾	I/O	TTa	Yes	SPI2_SCK I2S2_CK USART3_CTS I2C2_SCL LPUART_CTS TIM1_CH1N LCD_SEG13 TIM9_CH2 EVENTOUT	-
-	-	27	35	43			PB14	I/O	TTa	Yes	SPI2_MISO I2S2_MCK TIM1_CH2N USART3_RTS I2C2_SDA LPUART_RTS LCD_SEG14 TIM9_CH3 EVENTOUT UART4_TX	OPAMP2_VINP
-	-	28	36	44			PB15 ⁽¹⁰⁾	I/O	TTa	Yes	UART4_RX SPI2_MOSI I2S2_SD	-

QFN32	QFN32 ⁽¹¹⁾	QFN48	LQFP48	QFN64	LQFP64	LQFP80	Pin Name (after reset)	Type ⁽¹⁾	I/O structure ⁽²⁾	Fail-safe ⁽⁴⁾ support	Alternate function ⁽³⁾	Optional function
											TIM1_CH3N LCD_SEG15 TIM9_CH4 EVENTOUT	
17	-	-	-	-	-	45	VDD	S	-	-	-	-
-	-	-	-	-	-	46	VSS	S	-	-	-	-
-	20	-	-	37	-	47	PC6 ⁽¹⁰⁾	I/O	TTa	Yes	SPI2_NSS I2S2_WS TIM8_CH1 TIM3_CH1 LCD_SEG24 EVENTOUT	-
-	-	-	-	38	-	48	PC7 ⁽¹⁰⁾	I/O	TTa	Yes	SPI2_SCK I2S2_CK TIM3_CH2 TIM8_CH2 LCD_SEG25 EVENTOUT	-
-	-	-	-	39	-	49	PC8 ⁽¹⁰⁾	I/O	TTa	Yes	SPI2_MISO I2S2_MCK TIM8_CH3 TIM3_CH3 LCD_SEG26	-
-	-	-	-	40	-	50	PC9 ⁽¹⁰⁾	I/O	TTa	Yes	SPI2_MOSI I2S2_SD TIM3_CH4 TIM8_CH4 LCD_SEG27 EVENTOUT	-
18	21	29	41	51			PA8 ⁽¹⁰⁾	I/O	TTa	Yes	USART1_CK I2C2_SMBA TIM1_CH1 LCD_COM0 I2C2_SDA SPI1_NSS I2S1_WS MCO EVENTOUT	WKUP0 TAMP3-RTC
19	22	30	42	52			PA9 ⁽¹⁰⁾	I/O	TTa	Yes	USART1_TX I2C2_SCL TIM1_CH2 LCD_COM1 EVENTOUT	-
20	23	31	43	53			PA10 ⁽¹⁰⁾	I/O	TTa	Yes	USART1_RX I2C2_SDA SPI1_SCK SPI2_SCK I2S1_CK I2S2_CK TIM1_CH3 LCD_COM2 EVENTOUT	-
21	-	32	44	54			PA11 ⁽¹²⁾	I/O	TTa	No	USART1_CTS SPI2_MISO I2S2_MCK CAN_RX TIM1_CH4 COMP1_OUT EVENTOUT	USB_DM COMP2_INP

QFN32	QFN32 ⁽¹⁾	QFN48	LQFP48	QFN64	LQFP64	LQFP80	Pin Name (after reset)	Type ⁽¹⁾	I/O structure ⁽²⁾	Fail-safe ⁽⁴⁾ support	Alternate function ⁽³⁾	Optional function
22	-	33	45	55			PA12 ⁽¹²⁾	I/O	TTa	No	USART1_RTS SPI2_MOSI I2S2_SD CAN_TX TIM1_ETR COMP2_OUT EVENTOUT	USB_DP COMP1_INP
23	24	34	46	56			PA13 ⁽¹⁰⁾	I/O	TTa	Yes	SWDIO-JTMS SPI2_NSS I2S2_WS EVENTOUT	-
-	-	35	47	57			VSS	S	-	-	-	-
-	-	36	48	58			VDD	S	-	-	-	-
-	-	-	-	59			PD12 ⁽¹⁰⁾	I/O	TTa	Yes	UART4_RX I2C1_SDA SPI2_SCK I2S2_CK EVENTOUT	-
-	-	-	-	60			PD13	I/O	TTa	Yes	UART4_TX I2C1_SCL EVENTOUT	OPA2_VINP
24	25	37	49	61			PA14 ⁽¹⁰⁾	I/O	TTa	Yes	SWCLK-JTCK USART2_CK I2C1_SDA COMP2_OUT	-
25	26	38	50	62			PA15	I/O	TTa	Yes	JTDI USART2_CTS I2C1_SCL SPI2_NSS I2S2_WS TIM2_CH1 TIM2_ETR LCD_SEG17 LCD_COM3 EVENTOUT	COMP2_INP
-	-	-	51	63			PC10 ⁽¹⁰⁾	I/O	TTa	Yes	USART3_TX UART4_TX LPUART_TX LCD_SEG28 LCD_SEG40 ⁽⁷⁾ LCD_COM4 ⁽⁷⁾ EVENTOUT	-
-	-	-	52	64			PC11 ⁽¹⁰⁾	I/O	TTa	Yes	USART3_RX UART4_RX LPUART_RX LCD_SEG29 LCD_SEG41 ⁽⁷⁾ LCD_COM5 ⁽⁷⁾ EVENTOUT	-
-	-	-	53	65			PC12 ⁽¹⁰⁾	I/O	TTa	Yes	USART3_CK UART5_TX LCD_SEG30 LCD_SEG42 ⁽⁷⁾ LCD_COM6 ⁽⁷⁾ EVENTOUT	-
-	-	-	54	66			PD2 ⁽¹⁰⁾	I/O	TTa	Yes	TIM3_ETR UART5_RX LPUART_RTS LCD_SEG31	-

QFN32	QFN32 ⁽¹¹⁾	QFN48	LQFP48	QFN64	LQFP64	LQFP80	Pin Name (after reset)	Type ⁽¹⁾	I/O structure ⁽²⁾	Fail-safe ⁽⁴⁾ support	Alternate function ⁽³⁾	Optional function
											LCD_SEG43 ⁽⁷⁾ LCD_COM7 ⁽⁷⁾ EVENTOUT	
26	27	39	55	67			PB3	I/O	TTa	Yes	USART2_RTS SPI1_SCK I2S1_CK TIM2_CH2 JTDO-TRACESWO LCD_SEG7 EVENTOUT	COMP1_INP COMP2_INM
27	28	40	56	68			PB4	I/O	TTa	Yes	USART2_TX SPI1_MISO I2S1_MCK TIM3_CH1 LCD_SEG8 UART5_TX EVENTOUT NJTRST	COMP1_INP
28	29	41	57	69			PB5	I/O	TTa	Yes	USART2_RX I2C1_SMBA SPI1_MOSI I2S1_SD TIM3_CH2 LCD_SEG9 UART5_RX LPTIM_IN1 EVENTOUT	COMP1_INM
29	30	42	58	70			PB6 ⁽¹⁰⁾	I/O	TTa	Yes	USART1_TX LPUART_TX I2C1_SCL SPI1_NSS I2S1_WS TIM1_CH2N TIM4_CH1 SPI2_SCK I2S2_CK LPTIM_ETR COMP1_OUT EVENTOUT	-
30	31	43	59	71			PB7	I/O	TTa	Yes	USART1_RX LPUART_RX I2C1_SDA TIM4_CH2 EVENTOUT LPTIM_IN2 PVD_IN	COMP2_INP
31	-	44	60	72			BOOT0/PD0 ⁽¹⁰⁾	I/O	TTa	Yes	LCD_SEG32	-
-	32	45	61	73			PB8 ^{(10) (12)}	I/O	TTa	Yes	I2C1_SCL CAN_RX TIM4_CH3 LCD_SEG16 USART1_TX UART5_TX COMP1_OUT EVENTOUT	-
-	1	46	62	74			PB9 ^{(10) (12)}	I/O	TTa	Yes	I2C1_SDA CAN_TX TIM4_CH4 LCD_COM3	-

QFN32	QFN32 ⁽¹⁾	QFN48	LOFP48	QFN64	LOFP64	LOFP80	Pin Name (after reset)	Type ⁽¹⁾	I/O structure ⁽²⁾	Fail-safe ⁽⁴⁾ support	Alternate function ⁽³⁾	Optional function
											UART5_RX COMP2_OUT EVENTOUT	
32	33	47	63	75			VSS	S	-	-	-	-
-	-	48	64	76			VDD	S	-	-	-	-
-	-	-	-	77			PD4	I/O	TTa	Yes	SPI1_SCK I2S1_CK LCD_SEG28 LCD_SEG40 ⁽⁶⁾ LCD_COM4 ⁽⁶⁾	COMP1_INM
-	-	-	-	78			PD5	I/O	TTa	Yes	SPI1_MISO I2S1_MCK LCD_SEG29 LCD_SEG41 ⁽⁶⁾ LCD_COM5 ⁽⁶⁾	COMP1_INP
-	-	-	-	79			PD6	I/O	TTa	Yes	SPI1_MOSI I2S1_SD LCD_SEG30 LCD_SEG42 ⁽⁶⁾ LCD_COM6 ⁽⁶⁾ TRACED2	COMP2_INM
-	-	-	-	80			PD7	I/O	TTa	Yes	SPI1_NSS I2S1_WS LCD_SEG31 LCD_SEG43 ⁽⁶⁾ LCD_COM7 ⁽⁶⁾ TRACED3	COMP2_INP

1. *I = input, O = output, S = power supply.*
2. *TTa: 3.3V Standard IO.*
3. *This alternate function can be configured by the software to other pins (if the corresponding package model has such pins). For detailed information, please refer to the alternate function I/O chapter and debug setting chapter of the N32L40xxx user reference manual.*
4. *Fail-safe indicates that when the chip has no power input, a high input level is added to the IO. The high input level does not flood into the chip, resulting in a certain voltage on the power supply and current consumption.*
5. *QFN32 packages, N32L403 series is VDD, other series is VLCD.*
6. *Only applicable to version B chips, that is, the second character in the 8-bit code in the last line of the chip silkscreen is "B".*
7. *Applicable to C version and above chips, that is, the second character in the 8-bit code in the last line of the chip silk screen is not "B".*
8. *The corresponding ADC channel is a fast channel and supports a maximum sampling rate of 4.57MSPS (12Bit).*
9. *The corresponding ADC channel is a slow channel and supports a maximum sampling rate of 3.76MSPS (12Bit).*
10. *No more than 5V can be tolerated on the pin.*
11. *The corresponding package is QFN32(5mm x5mm)*
12. *N32L402 series not support CAN module.*

4 Electrical Characteristics

4.1 Parameter Conditions

All voltages are based on V_{SS} unless otherwise specified.

4.1.1 Minimum and Maximum Values

Unless otherwise specified, all minimums and maximums will be guaranteed under the worst ambient temperature, supply voltage and clock frequency conditions by performing tests on 100% of the product on the production line at ambient temperatures $T_A = 25^\circ\text{C}$.

Note at the bottom of each form that data obtained through comprehensive evaluation, design simulation and/or process characteristics will not be tested on the production; Base on comprehensive evaluation, the minimum and maximum values are obtained by taking the average of the samples tested and adding or subtracting three times the standard distribution (mean $\pm 3\Sigma$).

4.1.2 Typical Values

Unless otherwise specified, typical data are based on $T_A = 25^\circ\text{C}$ and $V_{DD} = 3.3\text{V}$. These data are for design guidance only and not tested.

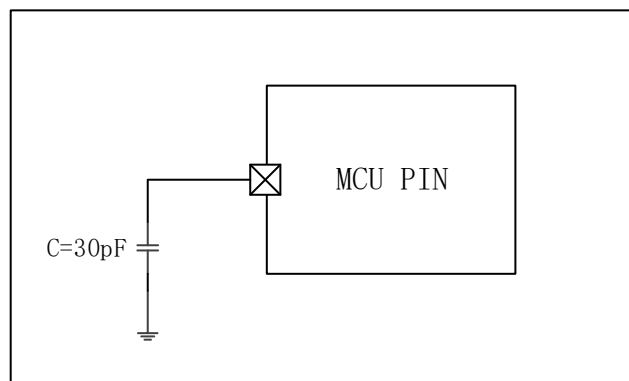
4.1.3 Typical Curves

Unless otherwise specified, typical curves are for design guidance only and not tested.

4.1.4 Loading Capacitors

The load conditions for measuring pin parameters are shown in the figure below:

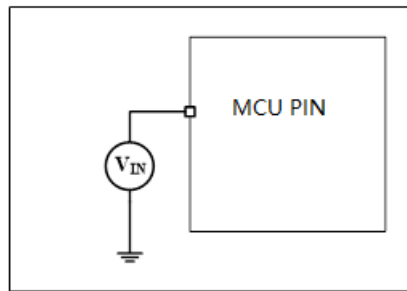
Figure 4-1 Load Conditions Of Pins



4.1.5 Pin Input Voltage

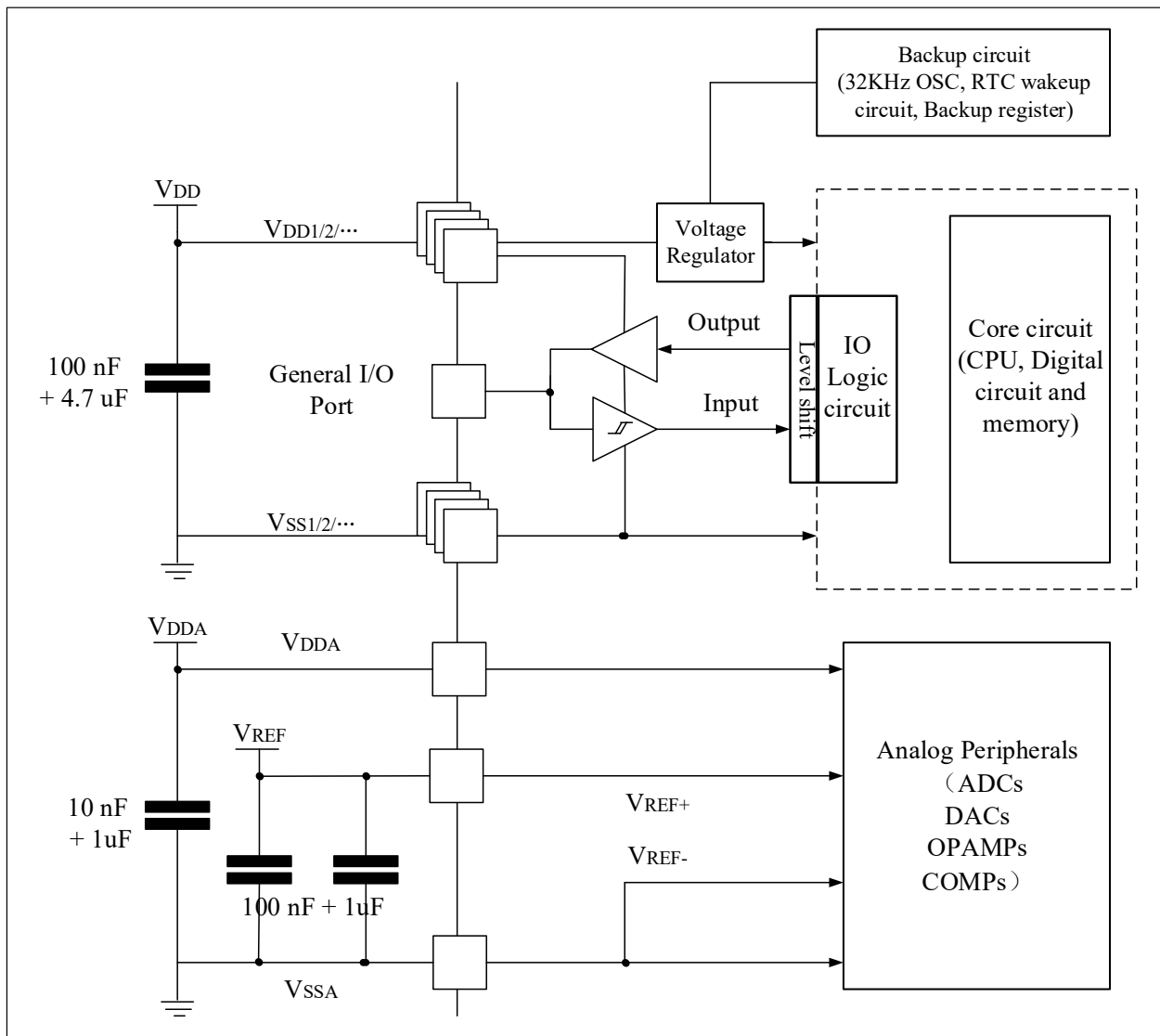
The measurement of the input voltage on the pin is shown in the figure below:

Figure 4-2 Pin Input Voltage



4.1.6 Power Supply Scheme

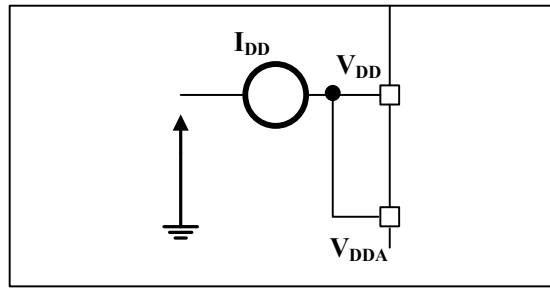
Figure 4-3 Power Supply Scheme



Note: Please refer to the hardware design guide for the capacitor connection method. V_{REF} is only available for ADC and DAC.

4.1.7 Current Consumption Measurement

Figure 4-4 Current Consumption Measurement Scheme



4.2 Absolute Maximum Rating

The load applied to the device may permanently damage the device if it exceeds the values given in the Absolute maximum rating list (Table 4-1, Table 4-2, Table 4-3). The maximum load that can be sustained is only given here, and it does not mean that the functional operation of the device under such conditions is correct. The reliability of the device will be affected when the device works for a long time under the maximum condition.

Table 4-1 Voltage Characteristics

Symbol	Describe	Min	Max	Unit
$V_{DD} - V_{SS}$	External main supply voltage (including V_{DDA} and V_{DD}) ⁽¹⁾	-0.3	4.0	V
V_{IN}	Input voltage on other pins ⁽²⁾	$V_{SS} - 0.3$	$V_{DD} + 0.3$	
$ \Delta V_{DDx} $	Voltage difference between different supply pins	-	50	mV
$ V_{SSx} - V_{SS} $	Voltage difference between different ground pins	-	50	
$V_{ESD(HBM)}$	ESD Electrostatic discharge voltage (human body model)	See section 4.3.11		

Note:

⁽¹⁾All power (V_{DD} , V_{DDA}) and ground (V_{SS} , V_{SSA}) pins must always be connected to the external power supply system within permissible limits.

⁽²⁾ V_{IN} shall not exceed its maximum value. Refer to Table 4-2 for current characteristics.

Table 4-2 Current Characteristics

Symbol	Describe	Max ⁽¹⁾	Unit
I_{VDD}	Total current through V_{DD}/V_{DDA} power line (supply current) ⁽¹⁾⁽⁴⁾	200	mA
I_{VSS}	Total current through V_{SS} ground line (outflow current) ⁽¹⁾⁽⁴⁾	200	
I_{IO}	Output current sunk by I/O and control pins	12	
	Output current source by I/O and control pins	- 12	
$I_{INJ(PIN)}^{(2)(3)}$	Injection current on NRST pin	-5/0	
	Injection current on other pins	±5	

Notes:

⁽¹⁾All power (V_{DD} , V_{DDA}) and ground (V_{SS} , V_{SSA}) pins must always be connected to the external power supply system within permissible limits.

⁽²⁾When $V_{IN} > V_{DD}$, there is a forward injection current; when $V_{IN} < V_{SS}$, there is a reverse injection current. $I_{INJ(PIN)}$ should not exceed its maximum value. Refer to Table 4-1 for voltage characteristics.

⁽³⁾Reverse injection current can interfere with the analog performance of the device. See section 4.3.19.

⁽⁴⁾When the maximum current occurs, the maximum allowable voltage drop of VDD is 0.1VDD.

Table 4-3 Temperature Characteristics

Symbol	Describe	Value	Unit
T _{STG}	Storage temperature range	- 40 ~ + 125	°C
T _J	Maximum junction temperature	125	°C

4.3 Operating Conditions

4.3.1 General Operating Conditions

Table 4-4 General Operating Conditions

Symbol	Parameter	Condition	Min	Max	Unit
f _{HCLK}	Internal AHB clock frequency	-	0	64	MHz
f _{PCLK1}	Internal APB1 clock frequency	-	0	16	
f _{PCLK2}	Internal APB2 clock frequency	-	0	32	
V _{DD}	Standard operating voltage	-	1.8	3.6	V
V _{DDA}	Analog operating of working voltage	Must be the same potential as V _{DD} ⁽¹⁾	1.8	3.6	V
T _A	Ambient temperature (temperature number 7)		- 40	105	°C
T _J	Junction temperature range	7 suffix version	- 40	125	°C

Note:

⁽¹⁾It is recommended that the same power supply be used to power the V_{DD} and V_{DDA}. During power-on and normal operation, a maximum of 300mV difference is allowed between the V_{DD} and V_{DDA}.

4.3.2 Operating Conditions at Power-on and Power-off

The parameters given in the following table are based on the ambient temperatures listed in Table 4-4.

Table 4-5 Operating Conditions At Power-On And Power-Off

Symbol	Parameter	Condition	Min	Max	Unit
t _{VDD}	V _{DD} rise time rate	Supply voltage goes from 0 to V _{DD}	20	∞	μs/V
	V _{DD} fall time rate	Supply voltage drops from V _{DD} to 0	80	∞	

4.3.3 Embedded Reset and Power Control Module Characteristics

The parameters given in the following table are based on the ambient temperature and V_{DD} supply voltage listed in Table 4-4.

Table 4-6 Features Of Embedded Reset And Power Control Modules

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{PVD}	Programmable voltage detector level selection	PVD0_rising	2.1	2.15	2.2	V
		PVD0_falling	2	2.05	2.1	V
		PVD1_rising	2.25	2.3	2.35	V
		PVD1_falling	2.15	2.2	2.25	V
		PVD2_rising	2.4	2.45	2.5	V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		PVD2_falling	2.3	2.35	2.4	V
		PVD3_rising	2.55	2.6	2.65	V
		PVD3_falling	2.45	2.5	2.55	V
		PVD4_rising	2.7	2.75	2.8	V
		PVD4_falling	2.6	2.65	2.7	V
		PVD5_rising	2.85	2.9	2.95	V
		PVD5_falling	2.75	2.8	2.85	V
		PVD6_rising	2.95	3	3.05	V
		PVD6_falling	2.85	2.9	2.95	V
V _{PVDhyst} ⁽¹⁾	PVD hysteresis		-	100	-	mV
V _{BOR}	VDD Power on/off Reset threshold	POR0	1.6	1.64	1.68	V
		PDR0	1.58	1.62	1.66	V
		POR1	2.05	2.1	2.15	V
		PDR1	1.95	2	2.05	V
		POR2	2.25	2.3	2.35	V
		PDR2	2.15	2.2	2.25	V
		POR3	2.55	2.6	2.65	V
		PDR3	2.45	2.5	2.55	V
		POR4	2.85	2.9	2.95	V
		PDR4	2.75	2.8	2.85	V
TRSTTEMPO ⁽¹⁾	Reset duration		-	0.15		ms

Note: ⁽¹⁾Guaranteed by design, not tested in production.

4.3.4 Internal Reference Voltage

The parameters given in the following table are based on the ambient temperature and V_{DD} supply voltage listed in Table 4-4.

Table 4-7 Internal Reference Voltage

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{REFINT}	Internal reference voltage	-40 °C < T _A < +105 °C	1.164	1.20	1.236	V
T _{S_vrefint} ⁽¹⁾	The sampling time of the ADC when reading the internal reference voltage	-	-	5.1	10 ⁽²⁾	µs

Notes:

⁽¹⁾The shortest sampling time is obtained through multiple loops in the application.

⁽²⁾Guaranteed by design, not tested in production.

4.3.5 Power Supply Current Characteristics

The current consumption is a combination of several parameters and factors, including operating voltage, ambient temperature, load of I/O pins, software configuration of the product, operating frequency, togglerate of I/O pins, program location in memory, and code executed.

The measurement method of current consumption is described in Figure 4-4.

All of the current consumption measurements given in this section are while executing a reduced set of code.

4.3.5.1 Maximum Current Consumption

The device is under the following conditions:

- All I/O pins are in input mode and are connected to a static level -- V_{DD} or V_{SS} (no load).
- All peripherals are disabled except otherwise noted.
- The access time of the Flash memory is adjusted to the fastest operating frequency (0 waiting periods from 0 to 32MHz, 1 waiting period from 32 to 64MHz).
- Instruction prefetch is enabled (note: this parameter must be set before setting the clock and bus divider).
- When the peripheral is enable: $f_{PCLK1} = f_{HCLK}/4$, $f_{PCLK2} = f_{HCLK}/2$.

The parameters given in Table 4-8 and Table 4-9 are based on tests at the ambient temperature and V_{DD} supply voltage listed in Table 4-4.

Table 4-8 Maximum Current Consumption In Operating Mode Where The Data Processing Code Is Run From Internal Flash

Symbol	Parameter	Condition	f_{HCLK}	Typ ⁽¹⁾	Unit
				$V_{DD}=3.3V, T_A = 105^{\circ}C$	
$I_{DD}^{(2)}$	Supply current in operation mode	Internal clock, enable all peripherals	64MHz	6.0	mA
			32MHz	3.8	
		Internal clock, disable all peripherals	64MHz	4.0	
			32MHz	2.5	

Notes:

⁽¹⁾Based on comprehensive evaluation, not tested in production.

⁽²⁾Internal clock is 8MHz, enable PLL when $f_{HCLK} > 8MHz$.

Table 4-9 Maximum Current Consumption In Sleep Mode, Code Running In Internal Flash Running

Symbol	Parameter	Conditions	f_{HCLK}	Typ ⁽¹⁾	Unit
				$V_{DD} = 3.3V, T_A = 105^{\circ}C$	
$I_{DD}^{(2)}$	Supply current in sleep mode	Internal clock, enable all peripherals	64MHz	4.2	mA
			32MHz	2.5	
		Internal clock, disable all peripherals	64MHz	2.2	
			32MHz	1.6	

Notes:

⁽¹⁾Based on comprehensive evaluation, not tested in production.

⁽²⁾Internal clock is 8MHz, enable PLL when $f_{HCLK} > 8MHz$.

4.3.5.2 Typical Current Consumption

MCU is under the following conditions:

- All I/O pins are in input mode and are connected to a static level -- V_{DD} or V_{SS} (no load).
- All peripherals are disable unless otherwise noted.
- The access time of the Flash memory is adjusted to the fastest operating frequency (0 waiting periods from 0 to 32MHz, 1 waiting period from 32 to 64MHz).
- Ambient temperature and V_{DD} supply voltage conditions are listed in Table 4-4.
- Instruction prefetch is enabled (note: this parameter must be set before setting the clock and bus divider).When the peripheral is turned on: $f_{PCLK1} = f_{HCLK} /4$, $f_{PCLK2} = f_{HCLK} /2$, $f_{ADCCLK} = f_{PCLK2} /4$.

Table 4-10 Typical Current Consumption In Operating Mode, Where Data Processing Code Is Run From Internal Flash

Symbol	Parameter	Conditions	f _{HCLK}	Typs ⁽¹⁾		Unit
				Enable all peripherals	Disable all peripherals	
I _{DD} ⁽²⁾	Supply current in operation mode	Internal clock	64MHz	5.9	3.7	mA
			32MHz	3.3	2.3	

Notes:

⁽¹⁾Typical values are measured at T_A = 25°C and V_{DD} = 3.3V.

⁽²⁾Internal clock is 8MHz, enable PLL when f_{HCLK} > 8MHz.

Table 4-11 Typical Current Consumption In Sleep Mode, Data Processing Code Is Run From Internal Flash

Symbol	Parameter	Condition	f _{HCLK}	Typ ⁽¹⁾		Unit
				Enable all peripherals ⁽²⁾	Disable all peripherals	
I _{DD} ⁽³⁾	Supply current in sleep mode	Internal clock	64MHz	3.8	2.0	mA
			32MHz	2.3	1.4	

Notes:

⁽¹⁾Typical values are measured at T_A = 25°C and V_{DD} = 3.3V.

⁽²⁾ADC additional 0.2mA current consumption is added. In the application environment, this part of the current is increased only when the ADC is turned on (set ADC_CTRL2.ON bit).

⁽³⁾Internal clock is 8MHz, enable PLL when f_{HCLK} > 8MHz.

4.3.5.3 Low Power Mode Current Consumption

The microcontroller is under the following conditions:

- All I/O pins are in input mode and are connected to a static level of -V_{DD} or V_{SS} (no load).
- All peripherals are off disabled otherwise noted.

Table 4-12 Typical And Maximum Current Consumption In Xshutdown And Standby Mode

Symbol	Parameter	Condition	Typ ⁽¹⁾		Unit
			V _{DD} = 3.3 V T _A = 25 °C	V _{DD} = 3.3 V T _A = 105 °C	
I _{DD_STOP2}	Supply current in Stop mode 2 (STOP2)	The external low-speed clock is on, the RTC is running, SRAM2 is on, all I/O states are on, and the independent watchdog is off	3 ⁽¹⁾	27 ⁽¹⁾	μA
I _{DD_STANDBY}	Supply current in STANDBY mode	Low speed internal RC oscillator and independent watchdog are on	1.6 ⁽¹⁾	7.6 ⁽¹⁾	
		The low speed internal RC oscillator is on and the independent watchdog is off	1.5 ⁽¹⁾	7.5 ⁽¹⁾	
		The low speed internal RC oscillator and independent watchdog are closed, and the low speed oscillator and RTC are closed	1.4 ⁽¹⁾	7.3 ⁽¹⁾	

Note: ⁽¹⁾Guaranteed by characterization, not tested in production.

4.3.6 External Clock Source Characteristics

4.3.6.1 High-Speed External Clock Source (HSE)

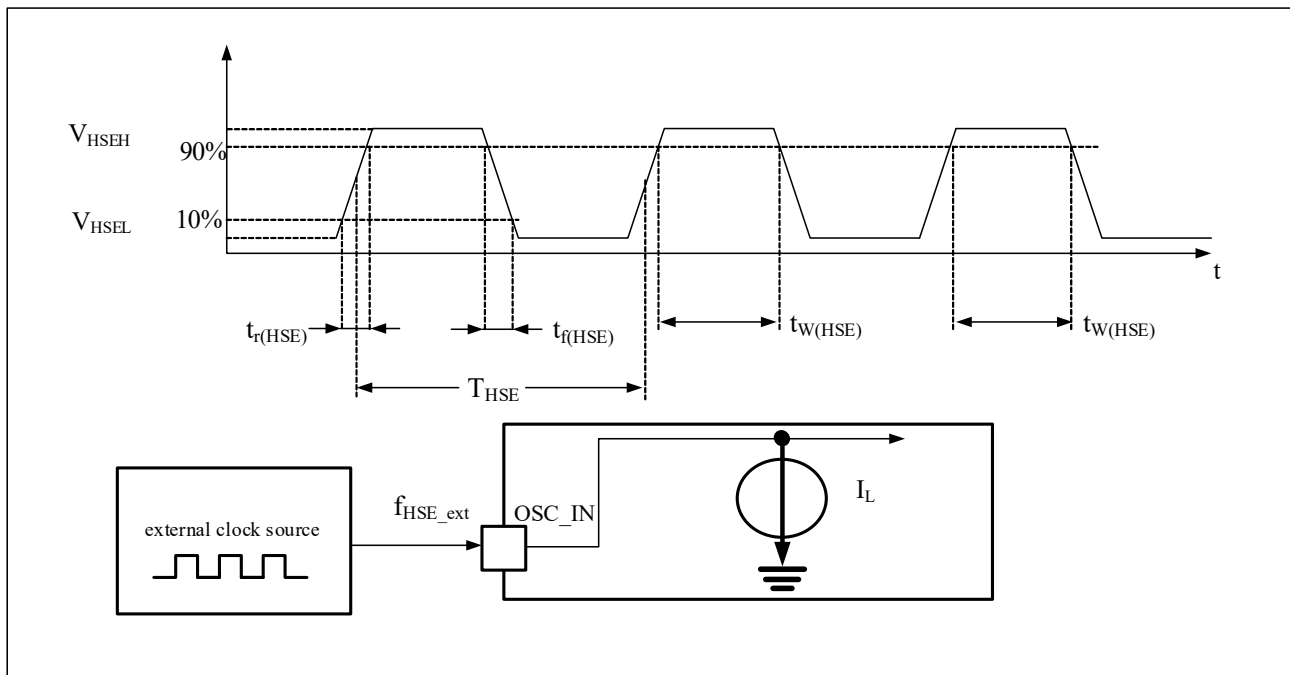
The characteristic parameters given in the following table are measured using a high-speed external clock source, and the ambient temperature and supply voltage meet the conditions specified in Table 4-4.

Table 4-13 High-Speed External User Clock Features (Bypass Mode)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE_ext}	User external clock frequency ⁽¹⁾	-	1	8	32	MHz
V_{HSEH}	OSC_IN Input pin high level voltage		0.8 V_{DD}	-	V_{DD}	V
V_{HSEL}	OSC_IN Input pin low level voltage		V_{SS}	-	0.3 V_{DD}	
$t_{w(HSE)}$	Time when OSC_IN is high or low ⁽¹⁾		16	-	-	ns
$t_{r(HSE)}$ $t_{f(HSE)}$	OSC_IN rise or fall time ⁽¹⁾		-	-	20	
DuCy _(HSE)	Duty cycle	-	45	-	55	%
I_L	OSC_IN Input leakage current	$V_{SS} \leq V_{IN} \leq V_{DD}$	-	-	± 1	μA

Note: ⁽¹⁾Guaranteed by design, not tested in production.

Figure 4-5 AC Timing Diagram Of An External High-Speed Clock Source



4.3.6.2 Low-Speed External Clock Source (LSE)

The characteristic parameters given in the following table are measured using a low speed external clock source, and the ambient temperature and supply voltage meet the conditions specified in Table 4-4.

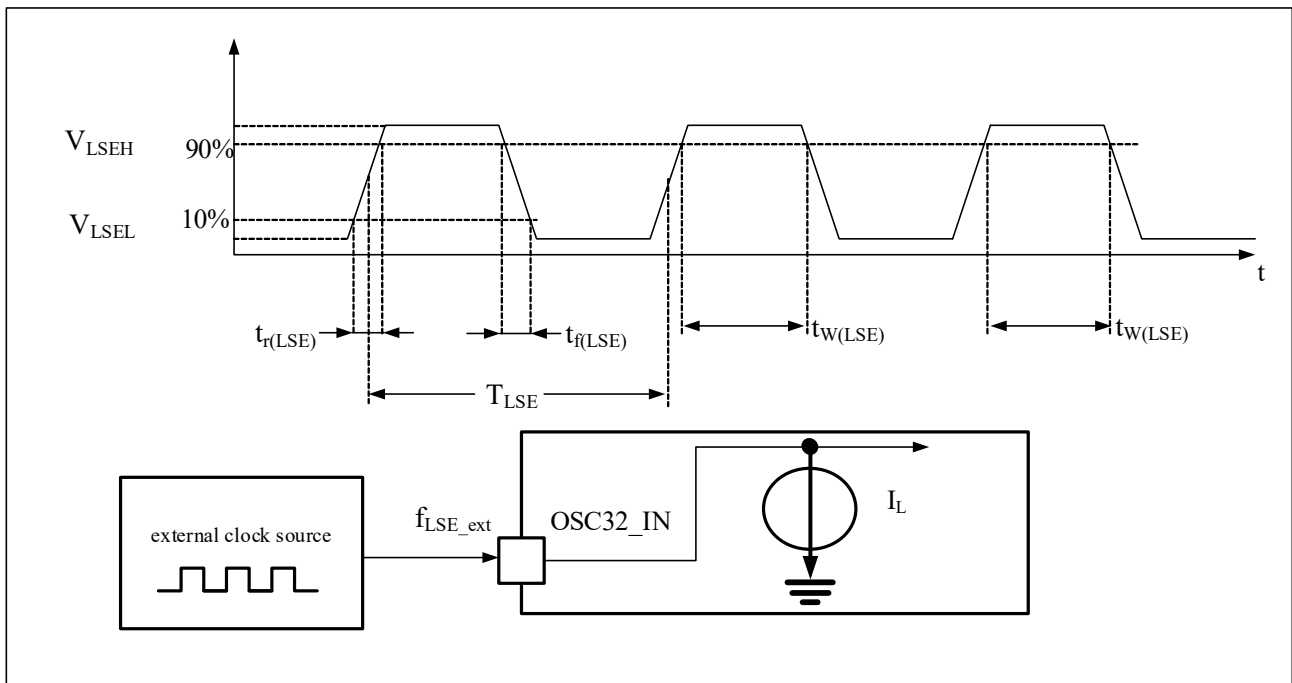
Table 4-14 Features Of A Low-Speed External User Clock (Bypass Mode)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE_ext}	User external clock frequency ⁽¹⁾		0	32.768	1000	KHz

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{LSEH}	OSC32_IN Input pin high level voltage		$0.7 V_{DD}$	-	V_{DD}	V
V_{LSEL}	OSC32_IN Input pin low level voltage		V_{SS}	-	200	mV
$t_{w(LSE)}$	OSC32_IN High or low time ⁽¹⁾		450	-	-	ns
$t_{r(LSE)}$ $t_{f(LSE)}$	OSC32_IN Rise or fall time ⁽¹⁾		-	-	50	
DuCy _(LSE)	Duty ratio		30	-	70	%
I_L	OSC32_IN Input leakage current	$V_{SS} \leq V_{IN} \leq V_{DD}$	-	-	± 1	μA

Note: ⁽¹⁾Guaranteed by design, not tested in production.

Figure 4-6 AC Timing Diagram Of An External Low Speed Clock Source



High-speed external clock generated using a crystal/ceramic resonator

High speed external clocks (HSE) can be generated using an oscillator consisting of a 4~32MHz crystal/ceramic resonator. The information presented in this section is based on a comprehensive feature evaluation using typical external components listed in the table below. In applications, the resonator and load capacitance must be as close to the oscillator pins as possible to reduce output distortion and stabilization time at startup. For detailed crystal resonator parameters (frequency, package, accuracy, etc.), please consult the appropriate manufacturer. (The crystal resonator mentioned here is usually referred to as passive crystal oscillator)

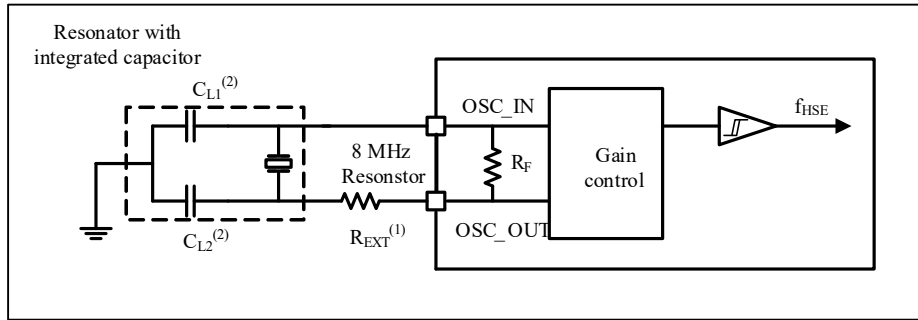
Table 4-15 HSE 4~32MHz Oscillator characteristics ^{(1) (2)}

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{OSC_IN}	Oscillator frequency		4	8	32	MHz
R_F	Feedback resistance		-	160	-	K Ω
i_2	HSE drive current	$V_{DD} = 3.3V, V_{IN} = V_{SS}$ 30 pf load	-	1.5	-	mA
g_m	Transconductance of the oscillator	Start the	-	10	-	mA/V
$t_{SU(HSE)}^{(3)}$	Startup time (8M crystal)	V_{DD} is stabilized	-	3	-	ms

Notes:

- (1)The characteristic parameters of the resonator are given by the crystal/ceramic resonator manufacturer.
- (2)Guaranteed by characterization results, not tested in production.
- (3). $t_{SU(HSE)}$ is the start time, from the time when HSE is enabled by the software to the time when a stable 8MHz oscillation is obtained. This value is measured on a standard crystal resonator and can vary widely depending on the crystal manufacturer.

Figure 4-7 Typical Application Using 8MHz Crystal



Notes:

- (1)The R_{EXT} value depends on the properties of the crystal. Typical values are 5 to 6 times R_S .
- (2)For C_{L1} and C_{L2} , it is recommended to use high quality ceramic dielectric vessels and to select crystals or resonators that meet the requirements. Usually C_{L1} and C_{L2} have the same parameters. Crystal manufacturers usually give parameters for load capacitance as serial combinations of C_{L1} and C_{L2} . When selecting C_{L1} and C_{L2} , the capacitance of PCB and MCU pins should be taken into account.

Low-speed external clock generated by a crystal/ceramic resonator

The low speed external clock (LSE) can be generated using an oscillator consisting of a 32.768 kHz crystal/ceramic resonator. The information presented in this section is based on a comprehensive feature evaluation using typical external components listed in Table 4-16. In applications, the resonator and load capacitance must be as close to the oscillator pins as possible to reduce output distortion and stabilization time at startup. For detailed crystal resonator parameters (frequency, package, accuracy, etc.), please consult the appropriate manufacturer. (The crystal resonator mentioned here is usually referred to as passive crystal oscillator)

Note: For C_{L1} and C_{L2} , it is recommended to use high quality ceramic dielectric containers, and to select crystals or resonators that meet the requirements. Usually C_{L1} and C_{L2} have the same parameters. Crystal manufacturers usually give parameters for load capacitance as serial combinations of C_{L1} and C_{L2} .

Load capacitance C_L is calculated by the following formula: $C_L = C_{L1} \times C_{L2} / (C_{L1} + C_{L2}) + C_{stray}$, where C_{stray} is the capacitance of the pin and the PCB or PCB-related capacitance.

For example: If a resonator with load capacitance $C_L = 6pF$ is selected and $C_{stray} = 2pF$, then $C_{L1} = C_{L2} = 8pF$.

Table 4-16 LSE Oscillator Characteristics ($f_{LSE} = 32.768kHz$) (1) (2) (4) (5)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_F	Feedback resistance		-	5	-	MΩ
g_m	Transconductance of the oscillator		-	15	-	μA/V
$t_{SU(LSE)}^{(3)}$	Startup time	V_{DD} is stabilized	-	2	-	s

Notes:

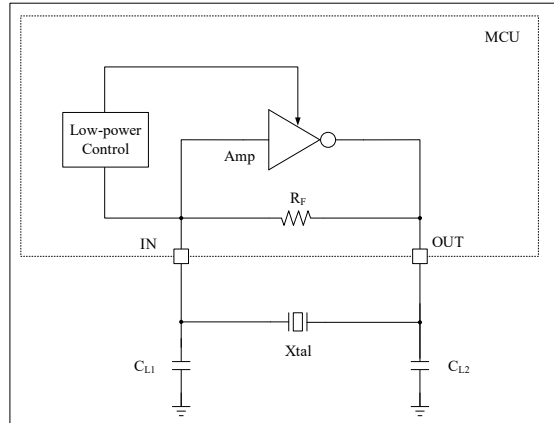
- (1)Guaranteed by design, not tested in production.
- (2)See the cautions section at the top of this form.
- (3) $t_{SU(LSE)}$ is the starting time, which is the period from the LSE enabled by the software to the stable 32.768kHz oscillation. This value is measured on a standard crystal resonator and can vary widely depending on the crystal

manufacturer.

(4)Please refer to the LSE crystal selection guide.

(5)In order to ensure the stability of crystal operation, do not turn the adjacent pins when crystal is working.

Figure 4-8 Typical Application Of 32.768kH Crystal



4.3.7 Internal Clock Source Characteristics

The characteristic parameters given in the following table were measured using ambient temperature and supply voltage in accordance with Table 4-4.

4.3.7.1 Multi-Speed Internal (MSI) RC Oscillator

Table 4-17 MSI Oscillator Characteristics ⁽¹⁾

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f _{MSI}	Range 0	MSI Frequency after Factory calibration, done at V _{DD} = 3.3V and T _A = 27 °C	-	100	-	KHz
	Range 1		-	200	-	KHz
	Range 2		-	400	-	KHz
	Range 3		-	800	-	KHz
	Range 4		-	1	-	MHz
	Range 5		-	2	-	MHz
	Range 6		3.96 ⁽⁴⁾	4 ⁽⁴⁾	4.1 ⁽⁴⁾	MHz
Δ _{TEMP} (MSI) ⁽²⁾	MSI oscillator frequency drift over temperature	T _A = 0 to 85 °C	-	±1%@4M ±1.2%@100k	-	%
		T _A = -40 to 105 °C	-	±2%@4M ±3%@100k	-	%
Δ _{VDD} (MSI) ⁽²⁾	MSI oscillator frequency drift over V _{DD} (reference is 3 V)	Range 0, V = 1.8V _{DD} to 3.6V	-	0.5 / - 1.5	-	%
		Range 6, V = 1.8V _{DD} to 3.6V	-	0.5 / - 5	-	%
t _{SU} (MSI) ⁽³⁾	MSI oscillator start-up time	Range 0 /100k	-	20	-	us
		Range 1 /200k	-	12	-	us
		Range 2 /400k	-	8	-	us
		Range 3 /800k	-	6	-	us
		Range 4 /1M	-	10	-	us
		Range 5 /2M	-	7	-	us
		Range 6 /4M	-	6	-	us
I _{DD} (MSI) ⁽³⁾	MSI oscillator power consumption	Range 0 /100k	-	1.0	-	uA
		Range 1 /200k	-	1.2	-	uA

Symbol	Parameter	Condition	Min	Typ	Max	Unit
		Range 2 /400k	-	1.8	-	uA
		Range 3 /800k	-	3.2	-	uA
		Range 4 /1M	-	6	-	uA
		Range 5 /2M	-	9	-	uA
		Range 6 /4M	-	16	-	uA

Notes:

(1) $V_{DD} = 3.3V$, $T_A = -40\sim 105^{\circ}C$ unless otherwise specified.

(2)This deviation range is the deviation of the oscillator after calibration;

(3)Guaranteed by design, not tested in production.

(4)After Reflow, the frequency will drift, and the maximum drift value is about 2.0%.

4.3.7.2 High Speed Internal (HSI) RC Oscillator

Table 4-18 HSI Oscillator Characteristics ^{(1) (2)}

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{HSI}	frequency	$V_{DD} = 3.3V$, $T_A = 25^{\circ}C$, after calibration	15.84 ⁽³⁾	16 ⁽³⁾	16.16 ⁽³⁾	MHz
ACC_{HSI}	Temperature drift of HSI oscillator	$V_{DD} = 3.3V$, $T_A = -40\sim 105^{\circ}C$, temperature drift	-2.5	-	2.5	%
		$V_{DD} = 3.3V$, $T_A = -10\sim 85^{\circ}C$, temperature drift	-1.5 ⁽⁴⁾	-	1.0 ⁽⁴⁾	
		$V_{DD} = 3.3V$, $T_A = 0\sim 70^{\circ}C$, temperature drift	-1.2 ⁽⁴⁾	-	0.7 ⁽⁴⁾	
$t_{SU(HSI)}$	HSI oscillator start time		-	-	5.0	μs
$I_{DD(HSI)}$	HSI oscillator power consumption		-	80 ⁽⁵⁾	100 ⁽⁵⁾	
			-	135 ⁽⁴⁾	160 ⁽⁴⁾	μA

Notes:

(1) $V_{DD} = 3.3V$, $T_A = -40\sim 105^{\circ}C$ unless otherwise specified.

(2)Guaranteed by design, not tested in production.

(3)After Reflow, the frequency will drift, and the maximum drift value is about +1.6%.

(4)Applicable to version F and later versions.

(5)Applicable to the previous version of version F.

4.3.7.3 Low Speed Internal (LSI) RC Oscillator

Table 4-19 LSI Oscillator Characteristics ⁽¹⁾

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$f_{LSI}^{(2)}$	Output frequency	25 $^{\circ}C$ calibration, $V_{DD} = 3.3V$	38	40	42	KHz
		$V_{DD} = 1.8V$ to 3.6V, $T_A = -40\sim 105^{\circ}C$	30	40	60	KHz
$t_{SU(LSI)}^{(2)}$	LSI oscillator startup time	-	-	40	80	μs
$I_{DD(LSI)}^{(2)}$	LSI oscillator power consumption	-	-	0.12	-	μA

Notes:

(1) $V_{DD} = 3.3V$, $T_A = -40\sim 105^{\circ}C$ unless otherwise specified.

⁽²⁾Guaranteed by characterization results, not tested in production.

4.3.8 Time To Wake Up from Low Power Mode

The wake-up time listed in Table 4-20 is measured during the wake-up phase of an 8MHz HSI RC oscillator. The clock source used when waking up depends on the current operating mode:

- STOP2 or STANDBY mode: clock source is RC oscillator
- SLEEP mode: The clock source is the clock used to enter sleep mode

All times were measured using ambient temperature and supply voltage in accordance with Table 4-4.

Table 4-20 Wake Time In Low Power Mode

Symbol	Parameter	Typ	Unit
twUSLEEP ⁽¹⁾	Wake up from SLEEP mode	10	HCLK ⁽²⁾
twUSLEEP ⁽¹⁾	Wake up from Low-Power SLEEP mode	10	HCLK ⁽²⁾
twULPRUN ⁽¹⁾	Wake up from Low-Power RUN mode	5.5	us ⁽²⁾
twUSTOP2 ⁽¹⁾	Wake up from STOP2 mode	12	us ⁽²⁾
twUSTDBY ⁽¹⁾	Wake up from STANDBY mode	50	

Notes:

⁽¹⁾The wake up time is measured from the start of the wake up event until the first instruction is read by the user program.

⁽²⁾The wake up time is obtained when MSI = 4MHz. If MSI is in other gears, the wake up time will be increased.

4.3.9 PLL Characteristics

The parameters listed in Table 4-21 are measured when the ambient temperature and power supply voltage meet the conditions in Table 4-4

Table 4-21 PLL Features

Symbol	Parameter	Value			Unit
		Min	Typ	Max ⁽¹⁾	
f _{PLL_IN}	PLL PFD input clock ⁽²⁾	4	8	32	MHz
	PLL Input clock duty cycle	40	50	60	%
f _{PLL_OUT}	PLL output clock ⁽²⁾	32	-	64	MHz
t _{LOCK}	PLL Ready indicates signal output time ⁽³⁾	-	-	150	μs
Jitter	RMS cycle-to-cycle jitter @64MHz ⁽¹⁾	-	6	-	pS
I _{pll}	Operating Current of PLL @64MHz VCO frequency. ⁽¹⁾	-	448	-	uA

Notes:

⁽¹⁾Based on comprehensive evaluation, not tested in production.

⁽²⁾Care needs to be taken to use the correct frequency doubling factor to input the clock frequency according to PLL so that f_{PLL_OUT} is within the allowable range.

⁽³⁾Guaranteed by design, not tested in production.

4.3.10 FLASH Memory Characteristics

Unless otherwise specified, all characteristic parameters are obtained at T_A = -40~105°C.

Table 4-22 Flash Memory Characteristics

Symbol	Parameter	Condition	Min ⁽¹⁾	Typ ⁽¹⁾	Max ⁽¹⁾	Unit
t _{prog}	32-bit programming time	T _A = - 40 ~ 105 °C	-	100	-	μs
t _{ERASE}	Page (2K bytes) erasure time	T _A = - 40 ~ 105 °C	-	2	20	ms
t _{ME}	Mass erase time	T _A = - 40 ~ 105 °C	-	-	100	ms
I _{DD}	The power supply current	Read mode, f _{HCLK} = 64MHz, 1 waiting cycles, V _{DD} = 3.3V	-	-	3.42	mA
		Write mode, f _{HCLK} = 64MHz, V _{DD} = 3.3V	-	-	6.5	mA
		Erase mode, f _{HCLK} = 64MHz, V _{DD} = 3.3V	-	-	4.5	mA
		Power-down/stop mode, V _{DD} = 3.3~3.6V	-	-	0.035	μA
V _{prog}	Programming voltage		1.8	-	3.6	V

Note: ⁽¹⁾Guaranteed by design, not tested in production.

Table 4-23 Flash Endurance And Data Retention Life

Symbol	Parameter	Condition	Min ⁽¹⁾	Unit
N _{END}	Endurance (note: erasure times)	T _A = -40~105°C(7 suffix versions)	100	Kcycle
t _{RET}	Data retention period	10 kcycle ⁽²⁾ at T _A = 85°C	30	Years
		10 kcycle ⁽²⁾ at T _A = 105°C	20	
		10 kcycle ⁽²⁾ at T _A = 125°C	10	

Notes:

⁽¹⁾Based on comprehensive evaluation, not tested in production.

⁽²⁾Cycling performed over the whole temperature range.

4.3.11 Absolute Maximum (Electrical Sensitivity)

Based on three different tests (ESD, LU), a specific measurement method is used to test the strength of the chip to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharge (a positive pulse followed by a negative pulse one second later) is applied to all pins of all samples, the size of which is related to the number of power pins on the chip (3 x (n+1) power pins). This test conforms to MIL-STD-883K Method 3015.9/ ESDA/JEDEC JS -002-2018 standard.

Table 4-24 Absolute Maximum ESD Value

Symbol	Parameter	Condition	Type	Max ⁽¹⁾	Unit
V _{ESD(HBM)}	Electrostatic discharge voltage (human body model)	T _A = +25 °C, In accordance with MIL-STD-883K Method 3015.9	2	4000	V
V _{ESD(CDM)}	Electrostatic discharge voltage (charging device model)	T _A = +25 °C, In accordance with ESDA/JEDEC JS - 002-2018	II	1000	

Note: ⁽¹⁾Based on comprehensive evaluation, not tested in production.

Static switch lock

To evaluate the locking performance, two complementary static locking tests were performed on six samples:

- Supply voltage exceeding limit for each power pin.
- Current is injected into each input, output, and configurable I/O pin.

This test conforms to JEDEC78E IC latch standard.

Table 4-25 Electrical Sensitivity

Symbol	Parameter	Condition	Type
LU	Static locking classes	$T_A^{(1)} = +85\text{ }^\circ\text{C}$, in accordance with JEDEC78E	II class A
		$T_A^{(2)} = +25\text{ }^\circ\text{C}$, in accordance with JEDEC78E	

Notes:

(1)Applicable to version F and later versions.

(2)Applicable to the previous version of version F.

4.3.12 I/O Port Characteristics

General input/output characteristics

Unless otherwise specified, the parameters listed in the following table are measured according to the conditions in Table 4-4. All I/O ports are CMOS and TTL compatible.

Table 4-26 I/O Static Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{IL}	Input low level voltage	TTL port	V_{SS}	-	0.8	V
V_{IH}	Input high level voltage		2	-	V_{DD}	
V_{IL}	Input low level voltage	CMOS port	V_{SS}	-	$0.35V_{DD}$	V
V_{IH}	Input high level voltage		$0.65 V_{DD}$	-	V_{DD}	
V_{hys}	Schmidt trigger voltage lag ⁽¹⁾⁽⁵⁾	-	0.1	-	-	V
V_{hys}	Schmidt trigger voltage lag ⁽¹⁾⁽⁶⁾	$V_{DD}=3.3V/2.5V$	0.2	-	-	
		$V_{DD}=1.8V$	$0.1 V_{DD}$	-	-	
I_{lkg}	Input leakage current ⁽²⁾	$V_{DD} = \text{Maximum}$ $V_{PAD} = 0$ or $V_{PAD} = V_{DD}$	-1	-	+1	μA
$I_{lkg, fail-safe}$	Input leakage current ⁽³⁾	$V_{DD} = 0$, $V_{PAD} = 3.63V$ or $V_{DD} < V_{PAD}$	-1	-	+1	μA
R_{PU}	Weak pull-up equivalent resistance ⁽⁴⁾	$V_{DD} = 3.3V$, $V_{IN} = V_{SS}$	90	-	170(190 ⁽⁷⁾)	K Ω
		$V_{DD} = 2.5V$, $V_{IN} = V_{SS}$	95	-	310	
		$V_{DD} = 1.8V$, $V_{IN} = V_{SS}$	135	-	500	
R_{PD}	Weak pull-down equivalent resistance ⁽⁴⁾	$V_{DD} = 3.3V$, $V_{IN} = V_{DD}$	75(90 ⁽⁷⁾)	-	235(200 ⁽⁷⁾)	
		$V_{DD} = 2.5V$, $V_{IN} = V_{DD}$	85	-	315	
		$V_{DD} = 1.8V$, $V_{IN} = V_{DD}$	120	-	495	
C_{IO}	Capacitance of I/O pins	-	-	5	-	pF

Notes:

(1)The hysteresis voltage of Schmitt trigger switching level. Based on comprehensive evaluation, not tested in production.

(2)The leakage current may be higher than the maximum if there is reverse current in adjacent pins.

(3)Not support fail-safe IOs include PD14, PD15, PA11, PA12, PA4, PB2.

(4)Pull-up and pull-down resistors are implemented with a switchable PMOS/NMOS.

⁽⁵⁾Applicable to version F and later versions.

⁽⁶⁾Applicable to the previous version of version F.

⁽⁷⁾Applicable to version F and later versions.

All I/O ports are CMOS and TTL compatible (no software configuration required) and their features take into account most of the strict CMOS process or TTL parameters:

- For V_{IH} :
 - If V_{DD} is between [1.8V~3.08V]; Use CMOS features but include TTL.
 - If V_{DD} is between [3.08V~3.6V]; Use TTL features but include CMOS.
- For V_{IL} :
 - If V_{DD} is between [1.8V~2.28V]; Use TTL features but include CMOS.
 - If V_{DD} is between [2.28V~3.60V]; Use CMOS features but include TTL.

Output drive current

GPIO (universal input/output port) can absorb or output up to +/-12mA current. In the user application, the number of I/O pins must ensure that the drive current does not exceed the absolute maximum ratings given in Section 4.2.

Output voltage

Unless otherwise specified, the parameters listed in Table 4-28 were measured using ambient temperature and V_{DD} supply voltage in accordance with Table 4-4. All I/O ports are CMOS and TTL compatible.

Table 4-27 IO Output Driving Ability Characteristics

Drive class	$I_{OH}^{(1)}$, $V_{DD}=3.3V$	$I_{OL}^{(1)}$, $V_{DD}=3.3V$	$I_{OH}^{(1)}$, $V_{DD}=2.5V$	$I_{OL}^{(1)}$, $V_{DD}=2.5V$	$I_{OH}^{(1)}$, $V_{DD}=1.8V$	$I_{OL}^{(1)}$, $V_{DD}=1.8V$	Unit
2	-2	2	-1.5	1.5	-1.2	1.2	mA
4	-4	4	-3	3	-2.5	2.5	mA
8	-8	8	-7	7	-5	5	mA
12	-12	12	-11	11	-7.5	7.5	mA

Note: ⁽¹⁾Guaranteed by design, not tested in production.

Table 4-28 Output Voltage Characteristics

Symbol	Parameter	Condition	Min	Max	Unit
$V_{OL}^{(1)}$	Output low level	$V_{DD} = 3.3 V$, $I_{OL}^{(3)} = 2mA, 4mA, 8mA, \text{ and } 12mA$	V_{SS}	0.4	V
		$V_{DD} = 2.5 V$, $I_{OL}^{(3)} = 1.5mA, 3mA, 7mA, \text{ and } 11mA$	V_{SS}	0.4	
		$V_{DD} = 1.8 V$, $I_{OL}^{(3)} = 1.2mA, 2.5mA, 5mA, \text{ and } 7.5mA$	V_{SS}	$0.2 * V_{DD}$	
$V_{OH}^{(2)}$	Output high level	$V_{DD} = 3.3 V$, $I_{OH}^{(3)} = -2mA, -4mA, -8mA, \text{ and } -12mA$	2.4	V_{DD}	V
		$V_{DD} = 2.5 V$, $I_{OH}^{(3)} = -1.5mA, -3mA, -7mA, \text{ and } -11mA$	2	V_{DD}	
		$V_{DD} = 1.8 V$, $I_{OH}^{(3)} = -1.2mA, -2.5mA, -5mA, \text{ and } -7.5mA$	$0.8 * V_{DD}$	V_{DD}	

Notes:

⁽¹⁾The current I_{IO} absorbed by the chip must always follow the absolute maximum rating given in Table 4-2, and the sum of I_{IO} (all I/O pins and control pins) must not exceed I_{VSS} .

⁽²⁾The current I_{IO} output from the chip must always follow the absolute maximum rating given in Table 4-2, and the sum of I_{IO} (all I/O pins and control pins) must not exceed I_{VDD} .

⁽³⁾Actual driving ability see Table 4-27.

Input/output AC characteristics

The definitions and values of the input and output AC characteristics are given in Figure 4-9 and Table 4-29 respectively.

Unless otherwise specified, the parameters listed in Table 4-29 were measured using ambient temperature and supply voltage in accordance with Table 4-4.

Table 4-29 Input/Output AC Characteristics ⁽¹⁾

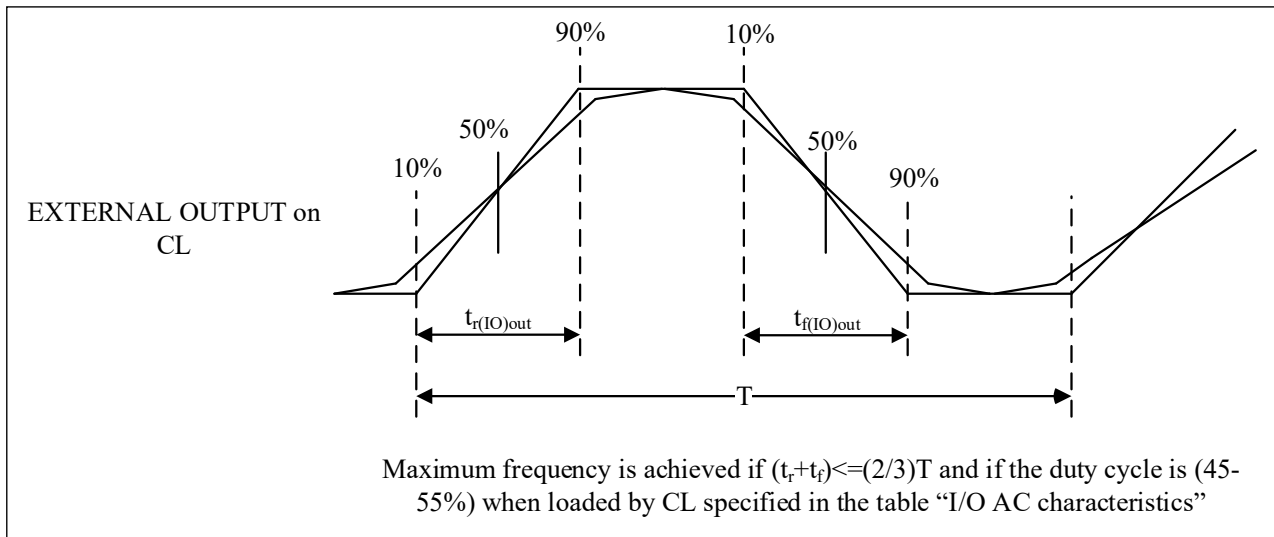
GPIOx_DS.DSy[1:0] Configuration	Symbol	Parameter	Condition	Min	Max	Unit
00 (2mA)	f _{max(IO)out}	Maximum frequency ⁽²⁾	C _L = 5pF, V _{DD} = 3.3V	-	64	MHz
			C _L = 5pF, V _{DD} = 2.5V	-	50	
			C _L = 5pF, V _{DD} = 1.8V	-	30	
	t _{(IO)out}	Output delay (A to pad)	C _L = 5pF, V _{DD} = 3.3V	-	3.66	ns
			C _L = 5pF, V _{DD} = 2.5V	-	4.72	
			C _L = 5pF, V _{DD} = 1.8V	-	7.12	
t _{(IO)in}	Input delay (pad to Y)	C _L = 50fF, V _{DD} = 2.97V, V _{DDD} = 0.81V Input characteristics at 1.8V and 2.5V are derated	-	1.2	ns	
10 (4mA)	f _{max(IO)out}	Maximum frequency ⁽²⁾	C _L = 10pF, V _{DD} = 3.3V	-	64	MHz
			C _L = 10pF, V _{DD} = 2.5V		60	
			C _L = 10pF, V _{DD} = 1.8V		40	
	t _{(IO)out}	The output delay (A to pad)	C _L = 10pF, V _{DD} = 3.3V	-	3.5	ns
			C _L = 10pF, V _{DD} = 2.5V		4.5	
			C _L = 10pF, V _{DD} = 1.8V		6.74	
t _{(IO)in}	Input delay (pad to Y)	C _L = 50fF, V _{DD} = 2.97V, V _{DDD} = 0.81V Input characteristics at 1.8V and 2.5V are derated	-	1.2	ns	
01 (8mA)	f _{max(IO)out}	Maximum frequency ⁽²⁾	C _L = 20pF, V _{DD} = 3.3V	-	64	MHz
			C _L = 20pF, V _{DD} = 2.5V		50	
			C _L = 20pF, V _{DD} = 1.8V		30	
	t _{(IO)out}	The output delay (A to pad)	C _L = 20pF, V _{DD} = 3.3V	-	3.42	ns
			C _L = 20pF, V _{DD} = 2.5V		4.73	
			C _L = 20pF, V _{DD} = 1.8V		6.53	
t _{(IO)in}	Input delay (pad to Y)	C _L = 50fF, V _{DD} = 2.97V, V _{DDD} = 0.81V Input characteristics at 1.8V and 2.5V are derated	-	1.2	ns	
11 (12mA)	f _{max(IO)out}	Maximum frequency ⁽²⁾	C _L = 30pF, V _{DD} = 3.3V	-	64	MHz
			C _L = 30pF, V _{DD} = 2.5V		50	
			C _L = 30pF, V _{DD} = 1.8V		30	
	t _{(IO)out}	The output delay (A to pad)	C _L = 30pF, V _{DD} = 3.3V	-	3.34	ns
			C _L = 3pF, V _{DD} = 2.5V		4.26	
			C _L = 3pF, V _{DD} = 1.8V		6.34	
t _{(IO)in}	Input delay (pad to Y)	C _L = 50fF, V _{DD} = 2.97V, V _{DDD} = 0.81V Input characteristics at 1.8V and 2.5V are derated	-	1.2	ns	

Notes:

⁽¹⁾The speed of the I/O port can be configured via GPIOx_DS.DSy[1:0]. Refer to the N32L40x user manual for instructions on configuring registers for GPIO ports.

⁽²⁾The maximum frequency is defined in Figure 4-9.

Figure 4-9 Definition Of Input/Output AC Characteristics



4.3.13 NRST Pin Characteristics

The NRST pin input driver uses the CMOS process, which is connected to an unbreakable pull-up resistor, R_{PU} (see Table 4-26). Unless otherwise specified, the parameters listed in Table 4-30 were measured using ambient temperature and supply voltage in accordance with Table 4-4.

Table 4-30 NRST Pin Characteristics

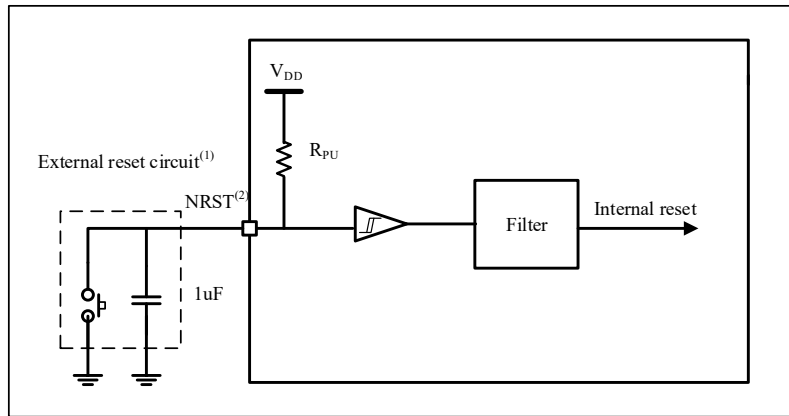
Symbol	Parameter	Condition	Min	Typ	Max	Unit
$V_{IL(NRST)}^{(1)}$	NRST input low level voltage	$V_{DD} = 3.3 \text{ V}$	V_{SS}	-	0.8	V
		$V_{DD} = 1.8 \text{ V}$	V_{SS}	-	$0.3 * V_{DD}$	
$V_{IH(NRST)}^{(1)}$	NRST input high level voltage	$V_{DD} = 3.3 \text{ V}$	2	-	V_{DD}	
		$V_{DD} = 1.8 \text{ V}$	$0.7 * V_{DD}$	-	V_{DD}	
$V_{hys(NRST)}$	NRST Schmidt trigger voltage hysteresis	$V_{DD} = 3.3 \text{ V}$	200	-	-	mV
		$V_{DD} = 1.8 \text{ V}$	$0.1 * V_{DD}$	-	-	V
R_{PU}	Weak pull-up equivalent resistance ⁽²⁾	$V_{DD} = 3.3 \text{ V}$	30	50	70	K Ω
$V_{F(NRST)}^{(1)}$	NRST input filter pulse	-	-	-	100	ns
$V_{NF(NRST)}^{(1)}$	NRST input unfiltered pulse	-	300	-	-	ns

Notes:

⁽¹⁾Guaranteed by design, not tested in production.

⁽²⁾The pull-up resistor is designed as a real resistor in series for a switchable PMOS implementation. The resistance of this PMON/NMOS switch is very small (about 10%).

Figure 4-10 Recommended NRST Pin Protection



Notes:

(1) Resetting the network is to prevent parasitic resets.

(2) The user must ensure that the NRST pin potential is below the maximum $V_{IL(NRST)}$ listed in Table 4-30, otherwise the MCU cannot be reset.

4.3.14 Timer and Watchdog Characteristics

The parameters listed in Table 4-31, Table 4-32 and Table 4-33 are guaranteed by design.

See section 0 for details on the features of the I/O alternate function pins (output comparison, input capture, external clock, PWM output).

Table 4-31 TIM1/8 Characteristics

Symbol	Parameter	Condition	Min	Typ	Unit
$t_{res(TIM)}$	Timer time resolution	-	1	-	t_{TIMCLK}
		$f_{TIMCLK} = 64MHz$	15.625	-	ns
f_{EXT}	Timer CH1 to CH2 external clock frequency	-	0	$f_{TIMCLK}/2$	MHz
		$f_{TIMCLK} = 64MHz$	0	32	MHz
ResTIM	Timer resolution	-	-	16	bits
$t_{COUNTER}$	16 bit counter clock cycle when internal clock is selected	-	1	65536	t_{TIMCLK}
		$f_{TIMCLK} = 64MHz$	0.015625	1024	μs
t_{MAX_COUNT}	Maximum count	-	-	65536×65536	t_{TIMCLK}
		$f_{TIMCLK} = 64MHz$	-	67.109	s

Table 4-32 TIM2/3/4/5/6/7/9 Characteristics

Symbol	Parameter	Condition	Min	Typ	Unit
$t_{res(TIM)}$	Timer time resolution	-	1	-	t_{TIMCLK}
		$f_{TIMCLK} = 32MHz$	31.25	-	ns
f_{EXT}	Timer CH1 to CH2 External clock frequency	-	0	$f_{TIMCLK}/2$	MHz
		$f_{TIMCLK} = 32MHz$	0	16	MHz
ResTIM	Timer resolution	-	-	16	bits
$t_{COUNTER}$	16 bit counter clock cycle when internal clock is selected	-	1	65536	t_{TIMCLK}
		$f_{TIMCLK} = 32MHz$	0.03125	2048	μs
t_{MAX_COUNT}	Maximum count	-	-	65536×65536	t_{TIMCLK}
		$f_{TIMCLK} = 32MHz$	-	134.218	s

Table 4-33 LPTIMER Characteristics

Symbol	Parameter	Condition	Min	Typ	Unit
$t_{res(LPTIM)}$	Timer time resolution	-	1	-	$t_{LPTIMCLK}$
		$f_{LPTIMCLK} = 16\text{MHz}$	62.5	-	ns
f_{EXT}	IN2 to OUT external clock frequency	-	0	16	MHz
		$f_{LPTIMCLK} = 16\text{MHz}$	0	16	MHz
$R_{ESLPTIM}$	Timer resolution	-	-	16	bits
$t_{COUNTER}$	16 bit counter clock cycle when internal clock is selected	-	1	65536	$t_{LPTIMCLK}$
		$f_{LPTIMCLK} = 16\text{MHz}$	0.0625	4096	μs
t_{MAX_COUNT}	Maximum count	-	-	65536x65536	$t_{LPTIMCLK}$
		$f_{LPTIMCLK} = 16\text{MHz}$	-	268.435	s

Table 4-34 IWDG Counting Maximum And Minimum Reset Time (LSI = 40kHz)

Prescaler	IWDG_PREDIV.PD[2:0]	Min ⁽¹⁾ IWDG_RELV.REL[11:0] = 0	Max ⁽¹⁾ IWDG_RELV.REL[11:0] = 0xFFF	Unit
/4	000	0.1	409.6	ms
/8	001	0.2	819.2	
/16	010	0.4	1638.4	
/32	011	0.8	3276.8	
/64	100	1.6	6553.6	
/128	101	3.2	13107.2	
/256	11x	6.4	26214.4	

Note: ⁽¹⁾Guaranteed by design, not tested in production.

Table 4-35 WWDG Counting Maximum And Minimum Reset Time (APB1 PCLK1 = 16MHz)

Prescaler	WWDG_CFG.TIMERB[2:0]	Min ⁽¹⁾ WWDG_CFG.W[13:0] = 0x3F	Max ⁽¹⁾ WWDG_CFG.W[13:0] = 0x3FFF	Unit
/1	00	0.256	16.38	ms
/2	01	0.512	32.77	
/3	10	1.024	65.54	
/4	11	2.048	7131.07	

Note: ⁽¹⁾Guaranteed by design, not tested in production.

4.3.15 I²C Interface Characteristics

Unless otherwise specified, the parameters listed in Table 4-36 were measured using ambient temperature, f_{PCLK1} frequency, and V_{DD} supply voltage in accordance with Table 4-4.

The I²C interface of the N32L40x product conforms to the standard I²C communication protocol, but has the following limitations: SDA and SCL are not "true" open leak pins, and when configured for open leak output, the PMOS tube between the pin and V_{DD} is closed, but still exists.

I²C interface features are listed in Table 4-36. See Section 0 for details about the features of the input/output alternate function pins (SDA and SCL).

Table 4-36 I²C Interface Characteristics

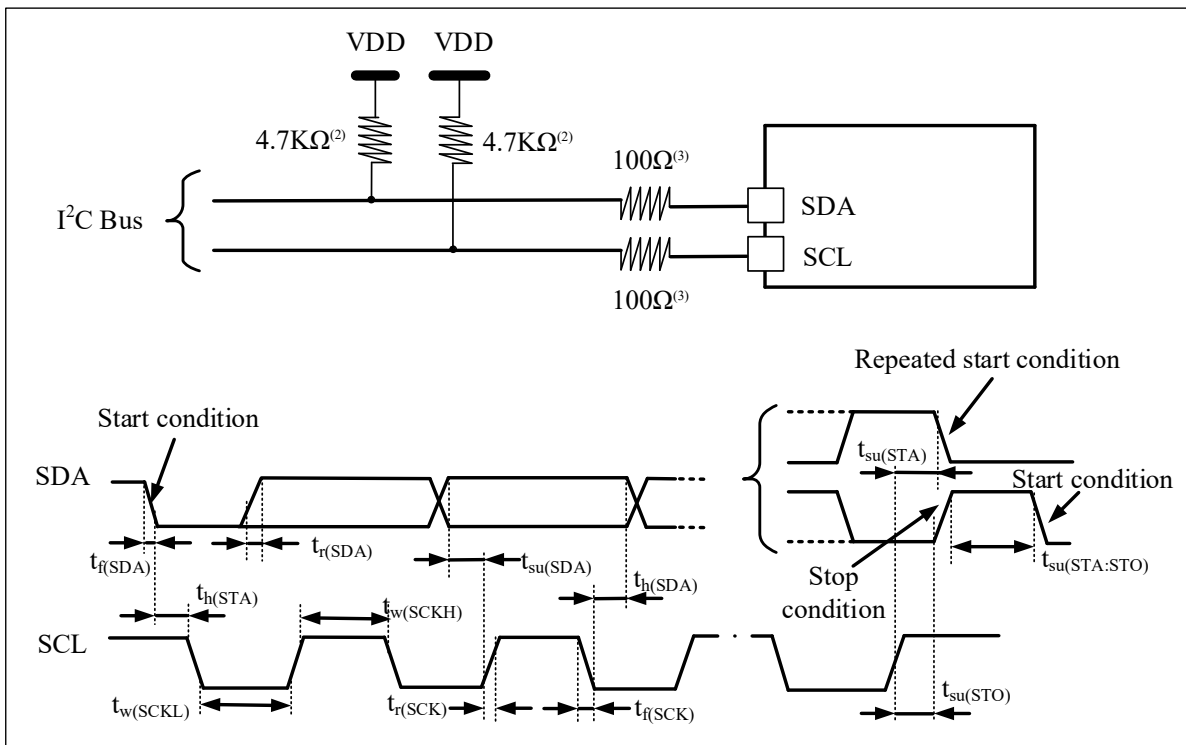
Symbol	Parameter	Standard model ^{(1) (2)}		Fast mode ^{(1) (2)}		Fast + mode ^{(1) (2)}		Unit
		Min	Max	Min	Max	Min	Max	
f _{SCL}	I2C interface frequency	0.0	100	0	400	0	1000	KHz
t _{h(STA)}	Start condition hold time	4.0	-	0.6	-	0.26	-	μs
t _{w(SCKL)}	SCL clock low time	4.7	-	1.3	-	0.5	-	μs
t _{w(SCLH)}	SCL clock high time	4.0	-	0.6	-	0.26	-	μs
t _{su(STA)}	Repeat start condition setup time	4.7	-	0.6	-	0.26	-	μs
t _{h(SDA)}	SDA data hold time	-	3.4	-	0.9	-	0.4	μs
t _{su(SDA)}	SDA setup time	250.0	-	100	-	50	-	ns
t _{r(SDA)} t _{r(SCL)}	SDA and SCL rise time	-	1000	20+ 0.1 C _b	300	-	120	ns
t _{f(SDA)} t _{f(SCL)}	SDA and SCL fall time	-	300	20+ 0.1 C _b	300	-	120	ns
t _{su(STO)}	Stop condition setup time	4.0	-	0.6	-	0.26	-	μs
t _{w(STO:STA)}	Time from stop condition to start condition (bus idle)	4.7	-	1.3	-	0.5	-	μs
C _b	Capacitive load per bus	-	400	-	400	-	100	pf
t _{v(SDA)}	Data validity time	-	3.45	-	0.9	-	0.45	μs
t _{v(ACK)}	Response time	-	3.45	-	0.9	-	0.45	μs

Notes:

⁽¹⁾Guaranteed by design, not tested in production.

⁽²⁾To achieve the maximum frequency of standard mode I2C, f_{PCLK1} must be greater than 2MHz. To achieve the maximum frequency of fast mode I2C, f_{PCLK1} must be greater than 4MHz.

Figure 4-11 I²C Bus AC Waveform And Measuring Circuit ⁽¹⁾



Notes:

⁽¹⁾The measuring point is set at the CMOS level: 0.3V_{DD} and 0.7V_{DD}.

(2)The pull-up resistance depends on the I2C interface speed.

(3)The resistance value depends on the actual electrical characteristics. The signal line can be directly connected without serial resistance.

4.3.16 SPI/I²S Interface Characteristics

Unless otherwise specified, the SPI parameters listed in Table 4-37 and the I²S parameters listed in Table 4-38 are measured using ambient temperature, f_{PCLKx} frequency, and V_{DD} supply voltage in accordance with Table 4-4.

See section 0 for details on the characteristics of the I/O reuse pins (NSS, SCLK, MOSI, MISO for SPI, WS, CLK, SD for I²S).

Table 4-37 SPI Characteristics ⁽¹⁾

Symbol	Parameter	Condition	Min	Max	Unit	
f_{SCLK} $1/t_c(SCLK)$	SPI clock frequency	Master mode	-	16	MHz	
		Slave mode	-	16		
$t_r(SCLK)$ $t_f(SCLK)$	SPI clock rise and fall time	Load capacitance: C = 30pF	-	8	ns	
DuCy(SCK)	SPI from the input clock duty cycle	SPI from the pattern	45	55	%	
$t_{su(NSS)}^{(1)}$	NSS setup time	Slave mode	$4t_{PCLK}$	-	ns	
$t_{h(NSS)}^{(1)}$	NSS hold time	Slave mode	$2t_{PCLK}$	-	ns	
$t_{w(SCLKH)}^{(1)}$ $t_{w(SCLKL)}^{(1)}$	SCLK high and low time	Master mode	t_{PCLK}	$t_{PCLK} + 2$	ns	
$t_{su(MI)}^{(1)}$	Data entry setup time	Master mode	SPI1	6.2	-	ns
			SPI2	5	-	
$t_{su(SI)}^{(1)}$		Slave mode	SPI1	6.3	-	
			SPI2	3	-	
$t_{h(MI)}^{(1)}$	Data entry hold time	Master mode	5	-	ns	
$t_{h(SI)}^{(1)}$		Slave mode	5.2	-		
$t_a(SO)^{(1)(2)}$	Data output access time	Slave mode, $f_{PCLK} = 20MHz$	0	$3t_{PCLK}$	ns	
$t_{dis(SO)}^{(1)(3)}$	Disable time of data output	Slave mode	2	10	ns	
$t_v(SO)^{(1)}$	Valid time of data output	Slave mode (after enable edge)	SPI1	-	20	ns
			SPI2	-	17	
$t_v(MO)^{(1)}$		Master mode (after enabling edge)	SPI1	-	5	
			SPI2	-	4	
$t_h(SO)^{(1)}$	Data output hold time	Slave mode (after enable edge)	6.2	-	ns	
$t_h(MO)^{(1)}$		Master mode (after enabling edge)	- 1	-		

Notes:

⁽¹⁾Guaranteed by design, not tested in production.

⁽²⁾The minimum value represents the minimum time to drive the output, and the maximum value represents the maximum time to get the data correctly.

⁽³⁾The minimum value represents the minimum time for turning off the output and the maximum value represents the maximum time for placing the data line in a high resistance state.

Figure 4-12 SPI Timing Diagram-Slave Mode And CPHA=0

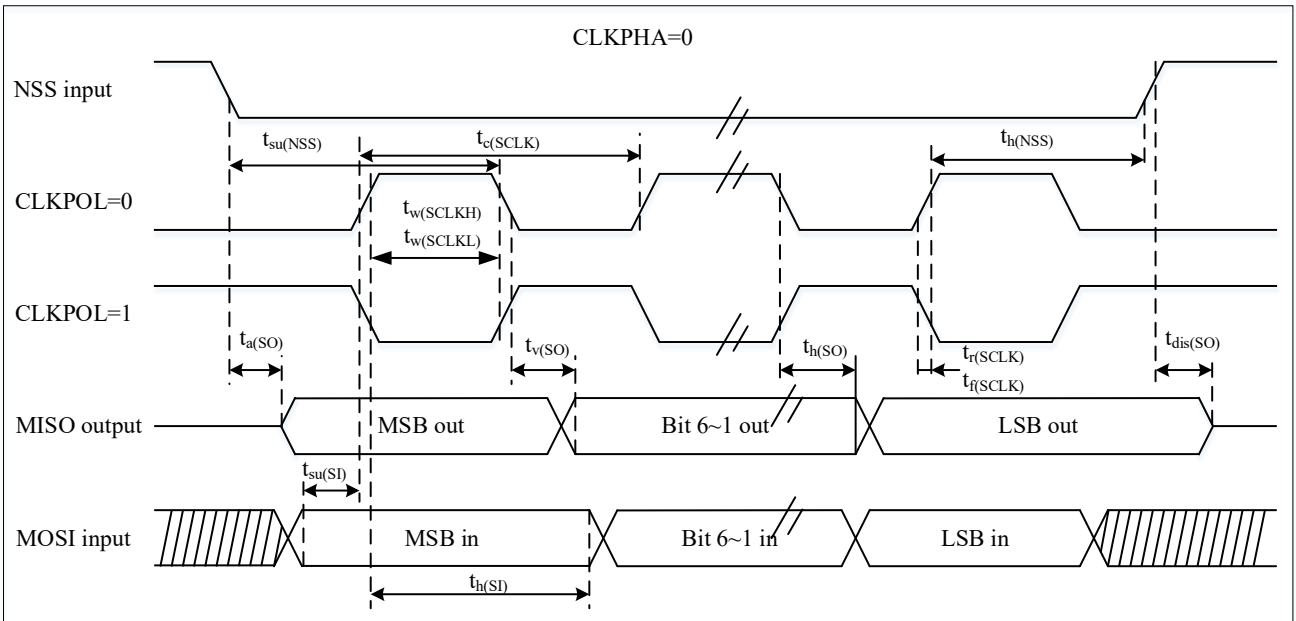
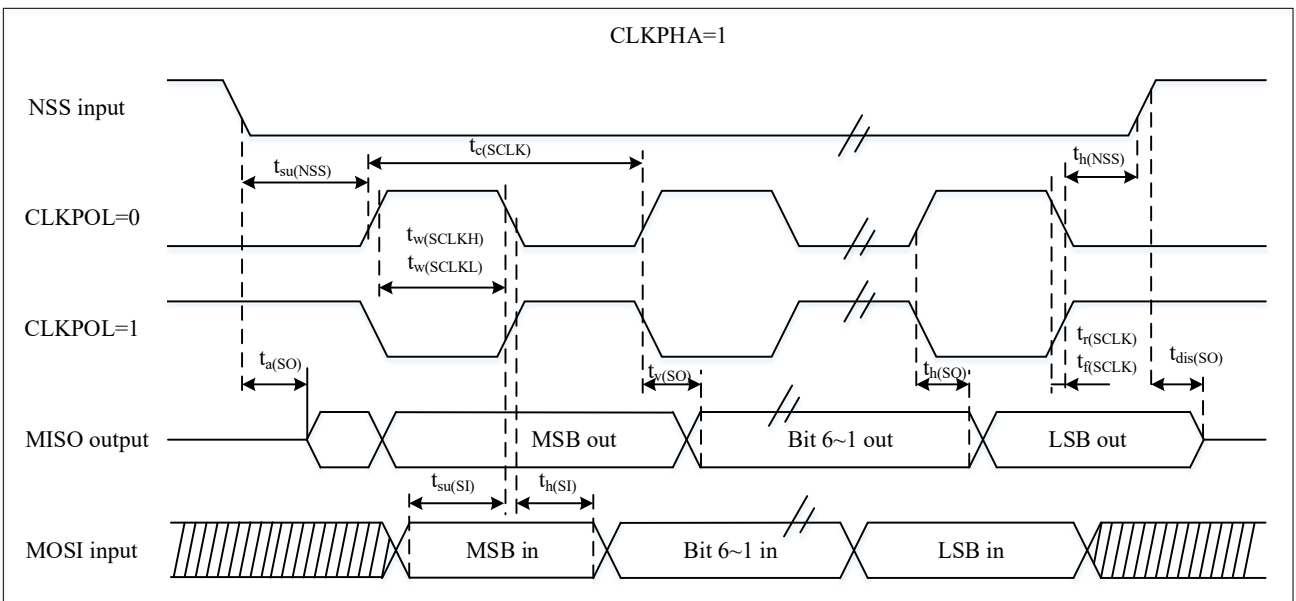
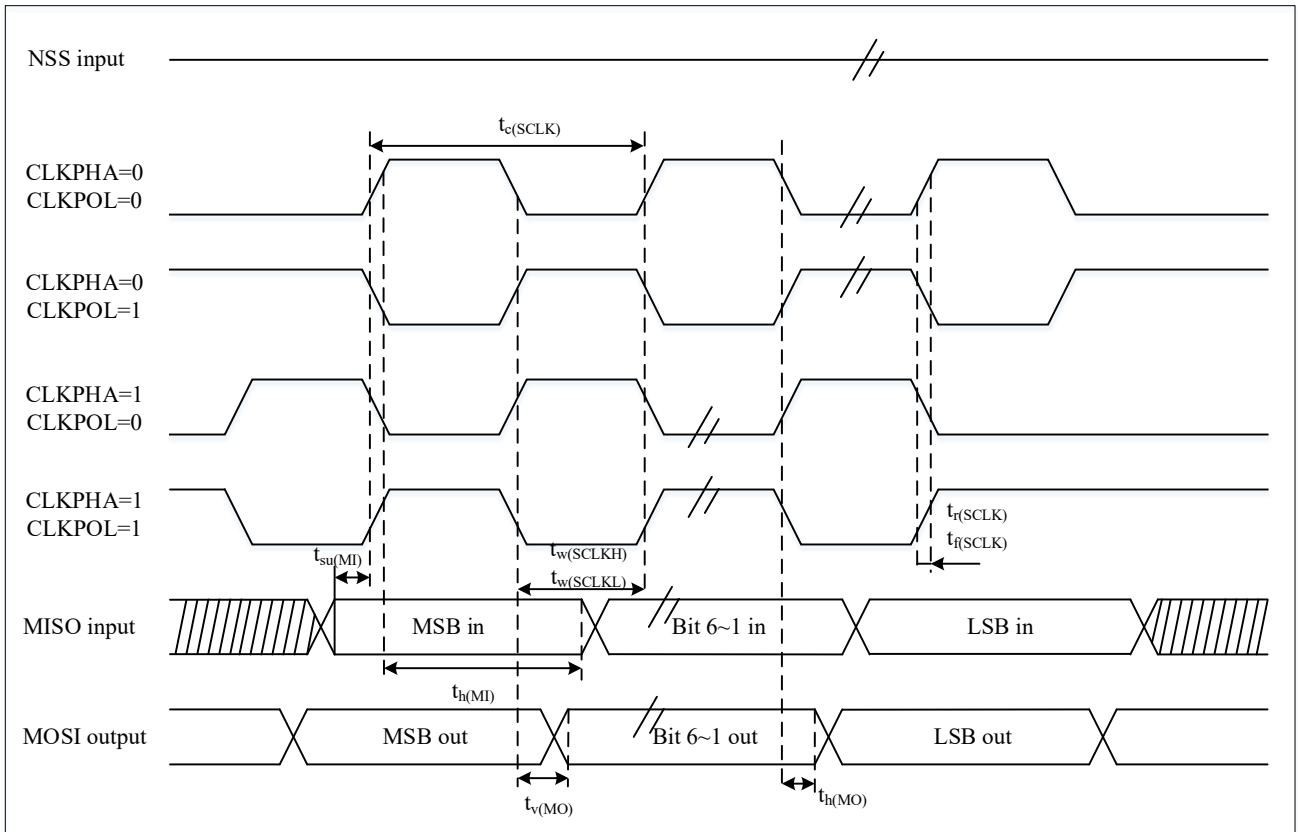


Figure 4-13 SPI Timing Diagram-Slave Mode And CPHA=1⁽¹⁾



Note: ⁽¹⁾The measuring point is set at the CMOS level: $0.3V_{DD}$ and $0.7V_{DD}$.

Figure 4-14 SPI Timing Diagram-Master Mode⁽¹⁾



Note: ⁽¹⁾The measuring point is set at the CMOS level: 0.3V and 0.7V_{DD}.

Table 4-38 I²S Characteristics ⁽¹⁾

Symbol	Parameter	Condition	Min	Max	Unit	
DuCy(SCK)	I ² S clock duty cycle	I2S Slave mode	30	70	%	
f_{CLK} $1/t_{c(CLK)}$	I ² S clock frequency	Master mode (32 bit)	-	64*F _S ⁽³⁾	MHz	
		Slave mode (32 bit)	-	64*F _S ⁽³⁾		
$t_r(CLK)$	I ² S clock rise and fall time	Load capacitance: CL = 50pF	-	8	ns	
$t_{v(WS)}^{(1)}$	WS valid time	Master mode	I2S1	5.3		-
			I2S2	5		-
$t_{h(WS)}^{(1)}$	WS hold time	Master mode	0	-		
$t_{su(WS)}^{(1)}$	WS setup time	Slave mode	I2S1	5.5		-
			I2S2	5		-
$t_{h(WS)}^{(1)}$	WS hold time	Slave mode	I2S1	7		-
			I2S2	3.6		-
$t_{w(CLKH)}^{(1)}$	CLK high and low times	Master mode, $f_{PCLK} = 16\text{MHz}$, audio 48kHz	312.5	-		
$t_{w(CLKL)}^{(1)}$			345	-		
$t_{su(SD_MR)}^{(1)}$	Data entry setup time	The main receiver	I2S1	6.5		-
			I2S2	5		-
$t_{su(SD_SR)}^{(1)}$	Data entry setup time	Slave mode	I2S1	2.5		-
			I2S2	2.5		-
$t_{h(SD_MR)}^{(1)(2)}$	Data entry hold time	Master receiver	I2S1	4.4		-
			I2S2	5.2		-
$t_{h(SD_SR)}^{(1)(2)}$	Data entry hold time	Slave mode	I2S1	4.5		-
			I2S2	5.2		-
$t_{v(SD_ST)}^{(1)(2)}$	Valid time of data output	Slave transmitter (after the enabled edge)	I2S1	-		22
			I2S2	-		22
$t_{h(SD_ST)}^{(1)}$	Data output hold time	Slave generator (after enable edge)	I2S1	4	-	
			I2S2	4	-	
$t_{v(SD_MT)}^{(1)(2)}$	Valid time of data output	Master generator (after enabling edge)	I2S1	-	5.6	
			I2S2	-	4.5	
$t_{h(SD_MT)}^{(1)}$	Data output hold time	Master generator (after enabling edge)	0.5	-		

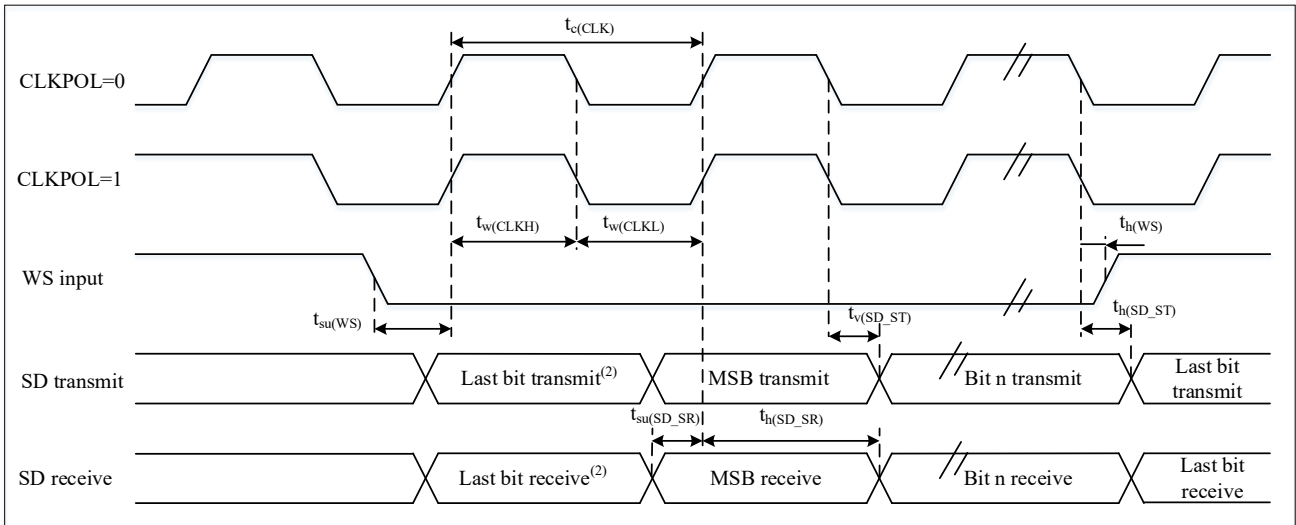
Notes:

⁽¹⁾Guaranteed by design, not tested in production.

⁽²⁾Depends on f_{PCLK} . For example, if $f_{PCLK}=16\text{MHz}$, then $T_{PCLK}=1/f_{PCLK}=125\text{ns}$.

⁽³⁾Audio sampling rate.

Figure 4-15 I²S Slave Mode Timing Diagram (Philips Protocol)⁽¹⁾

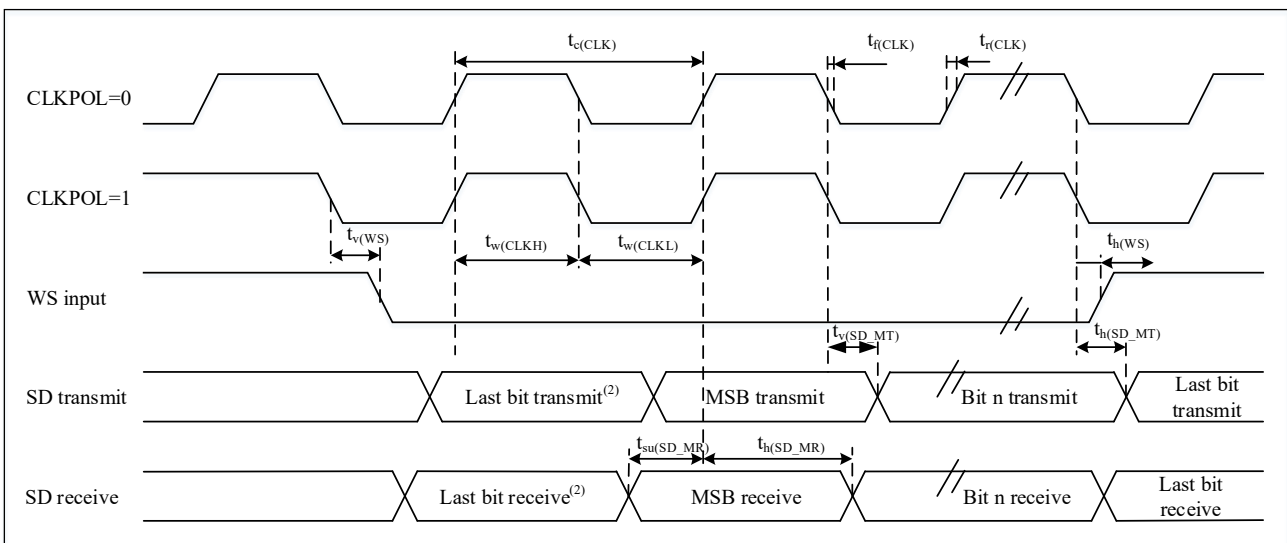


Notes:

⁽¹⁾The measuring point is set at the CMOS level: $0.3V_{DD}$ and $0.7V_{DD}$.

⁽²⁾Send/receive of the last byte. There is no least significant send/receive before the first byte.

Figure 4-16 I²S Master Mode Timing Diagram (Philips Protocol)⁽¹⁾



Notes:

⁽¹⁾The measuring point is set at the CMOS level: $0.3V_{DD}$ and $0.7V_{DD}$.

⁽²⁾Send/receive of the last byte. There is no least significant send/receive before the first byte.

4.3.17 USB Interface Characteristics

USB (full speed) interface is certified by the USB-IF.

Table 4-39 USB Startup Time

Symbol	Parameter	Max	Unit
$t_{STARTUP}^{(1)}$	USB transceiver startup time	1	μs

1. Guaranteed by design, not tested in production.

Table 4-40 USB DC Characteristics

Symbol	Parameter	Condition	Min ⁽¹⁾	Max ⁽¹⁾	Unit
Input level					
V _{DD}	USB operating voltage ⁽²⁾		3.0 ⁽³⁾	3.6	V
V _{DI} ⁽⁴⁾	Differential input sensitivity	I (USBDP and USBDM)	0.2	-	V
V _{CM} ⁽⁴⁾	Differential common mode range	Contains VDI ranges	0.8	2.5	
V _{SE} ⁽⁴⁾	Single-end receiver threshold		1.3	2.0	
Output level					
V _{OL}	Static output low level	1.5KΩ RL is connected to 3.6V ⁽⁵⁾	-	0.3	V
V _{OH}	Static output high level	15KΩ RL is connected to V _{SS} ⁽⁵⁾	2.8	3.6	

Notes:

- ⁽¹⁾All voltage measurements are based on the ground cable at the device end.
- ⁽²⁾USB operating voltage is 3.0~3.6V in order to be compatible with USB2.0 full speed electrical specification.
- ⁽³⁾The correct USB function of the N32L40x series products can be guaranteed at 2.7V, instead of dropping the electrical characteristics in the 2.7-3.0V voltage range.
- ⁽⁴⁾Based on comprehensive evaluation, not tested in production.
- ⁽⁵⁾R_L is the load attached to the USB drive.

Figure 4-17 USB Timing: Definition Of Rise And Fall Time Of Data Signal

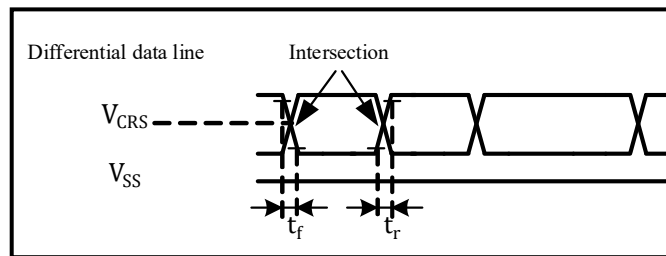


Table 4-41 Full Speed Of USB Electrical Characteristics

Symbol	Parameter	Condition	Min ⁽¹⁾	Max ⁽¹⁾	Unit
t _r	Rise time ⁽²⁾	C _L ≤ 50pF	4	20	ns
t _f	Fall time ⁽²⁾	C _L ≤ 50pF	4	20	ns
t _{rfm}	Rise and fall times match	t _r / t _f	90	111.1	%

Notes:

- ⁽¹⁾Guaranteed by design, not tested in production.
- ⁽²⁾Measured data signal from 10% to 90%. For more details, see Chapter 7 (version 2.0) of the USB specification.

4.3.18 Controller Area Network (CAN) Interface Characteristics

See Section 0 for details on the features of the input/output alternate function pins (CAN_TX and CAN_RX).

4.3.19 12-bit Analog-to-Digital Converter (ADC) Electrical Parameters

Unless otherwise specified, the parameters in Table 4-42 are measured using ambient temperature, f_{HCLK} frequency, and V_{DDA} supply voltage in accordance with the conditions in Table 4-4.

Note: It is recommended to perform a calibration at each power-on.

Table 4-42 ADC Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V _{DDA}	The power supply voltage	Use an external reference voltage	1.8	-	3.6	V
V _{REF+}	Positive reference voltage		1.8	-	V _{DDA}	V
f _{ADC}	ADC clock frequency		-	-	64	MHz
f _s ⁽¹⁾	Sampling rate	1.8V ≤ V _{DD} ≤ 3.6V, 12bit resolution	-	-	4.57	MHz
		1.8V ≤ V _{DD} ≤ 3.6V, 10bit resolution	-	-	5.33	
		1.8V ≤ V _{DD} ≤ 3.6V, 8bit resolution	-	-	6.4	
		1.8V ≤ V _{DD} ≤ 3.6V, 6bit resolution	-	-	8	
V _{AIN}	Switching voltage range ⁽²⁾		0 (V _{SSA} or V _{REF-} Connect to ground)	-	V _{REF+}	V
R _{ADC} ⁽¹⁾	Sampling switch resistance	Fast channel	-	-	0.2	KΩ
R _{ADC} ⁽¹⁾	Sampling switch resistance	Slow channel	-	-	0.5	KΩ
C _{ADC} ⁽¹⁾	Internal sampling and holding capacitors		-	5	-	pF
SNDR	Signal noise distortion ration		-	65	-	dBFS
T _{cal}	The calibration time		82			1/f _{ADC}
t _s ⁽¹⁾	Sampling time	f _{ADC} = 64MHz(fast channel)	0.0234	-	9.4	us
		f _{ADC} = 64MHz(slow channel)	0.0703	-	9.4	
T _s ⁽¹⁾	Sampling cycles	Fast track	1.5	-	601.5	1/f _{ADC}
		The slow channel	4.5	-	601.5	
t _{STAB} ⁽¹⁾	Power on time		6	10	20	μs
t _{CONV} ⁽¹⁾⁽³⁾	Total conversion time (including sampling time)	12bit resolution	14~614 (Sampling T _s + 6.5/8.5/10.5/12.5 for successive approximation)			1/f _{ADC}

Notes:

⁽¹⁾Guaranteed by design, not tested in production.

⁽²⁾V_{REF+} is connected internally to V_{DDA}, and V_{REF-} is connected internally to V_{SSA}.

⁽³⁾Single conversion mode has 3 more 1/f_{ADC} than continuous conversion mode

Formula 1: maximum R_{AIN} formula

$$R_{AIN} < \frac{T_s}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$$

The above formula (Formula 1) is used to determine the maximum external impedance so that the error can be less than 1/4 LSB. Where N=12(representing 12-bit resolution).

Table 4-43 ADC Sampling Time⁽¹⁾⁽²⁾

Input	Resolution	Rin(kΩ)	Typ of minimum sampling time (ns)	Input	Resolution	Rin(kΩ)	Typ of minimum sampling time (ns)
fast channel	12-bit	0	11	slow channel	12-bit	0	19
		0.05	12			0.05	21
		0.1	14			0.1	23
		0.2	20			0.2	30
		0.5	38			0.5	48
		1	64			1	77
		5	276			5	310
		10	543			10	607
		20	1082			20	1207
		50	2788			50	3144
		100	6162			100	8244
fast channel	10-bit	0	10	slow channel	10-bit	0	17
		0.05	11			0.05	18
		0.1	13			0.1	20
		0.2	17			0.2	25
		0.5	32			0.5	40
		1	54			1	64
		5	229			5	257
		10	448			10	499
		20	888			20	983
		50	2223			50	2457
		100	4500			100	5001
fast channel	8-bit	0	9	slow channel	8-bit	0	14
		0.05	10			0.05	16
		0.1	11			0.1	17
		0.2	14			0.2	21
		0.5	26			0.5	33
		1	43			1	52
		5	183			5	206
		10	358			10	399
		20	707			20	783
		50	1759			50	1941
		100	3523			100	3887
fast channel	6-bit	0	8	slow channel	6-bit	0	12
		0.05	8			0.05	13
		0.1	9			0.1	14
		0.2	12			0.2	17
		0.5	20			0.5	25
		1	33			1	40
		5	138			5	156
		10	269			10	300
		20	531			20	588
		50	1316			50	1451
		100	2627			100	2894

Notes:

⁽¹⁾Guaranteed by design, not tested in production.

⁽²⁾Typical values are obtained when $T_A=25$ and $V_{DD}=3.3V$.

Table 4-44 ADC Accuracy-Limited Test Conditions ⁽¹⁾⁽²⁾

Symbol	Parameter	Condition	Typ	Max ⁽³⁾	Unit
ET	Comprehensive error ⁽⁴⁾	$f_{HCLK} = 64\text{MHz}$, $f_{ADC} = 64\text{MHz}$, sample Rate = 1.75m SPS , $V_{DDA} = 3.3\text{V}$, $T_A = 25$ $^{\circ}\text{C}$ Measurements are made after the ADC is calibrated $V_{REF+} = V_{DDA}$	± 1.3	-	LSB
EO	Offset error ⁽⁵⁾		± 1	-	
ED	Differential linear error		± 0.7	-	
EL	Integral linear error		± 0.8	-	

Notes:

⁽¹⁾The DC accuracy of the ADC is measured after internal calibration.

⁽²⁾ADC accuracy versus reverse injection current: It is necessary to avoid injecting reverse current on any standard analog input pin, as this can significantly reduce the accuracy of the conversion being performed on the other analog input pin. It is recommended to add a Schottky diode (between pin and ground) to standard analog pins that may generate reverse injection current.

⁽³⁾The forward injection current does not affect the ADC accuracy as long as it is within the range of $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ given in Table 4-2

⁽⁴⁾Based on comprehensive evaluation, not tested in production.

⁽⁵⁾Guaranteed by design, not tested in production.

Figure 4-18 ADC Precision Characteristics

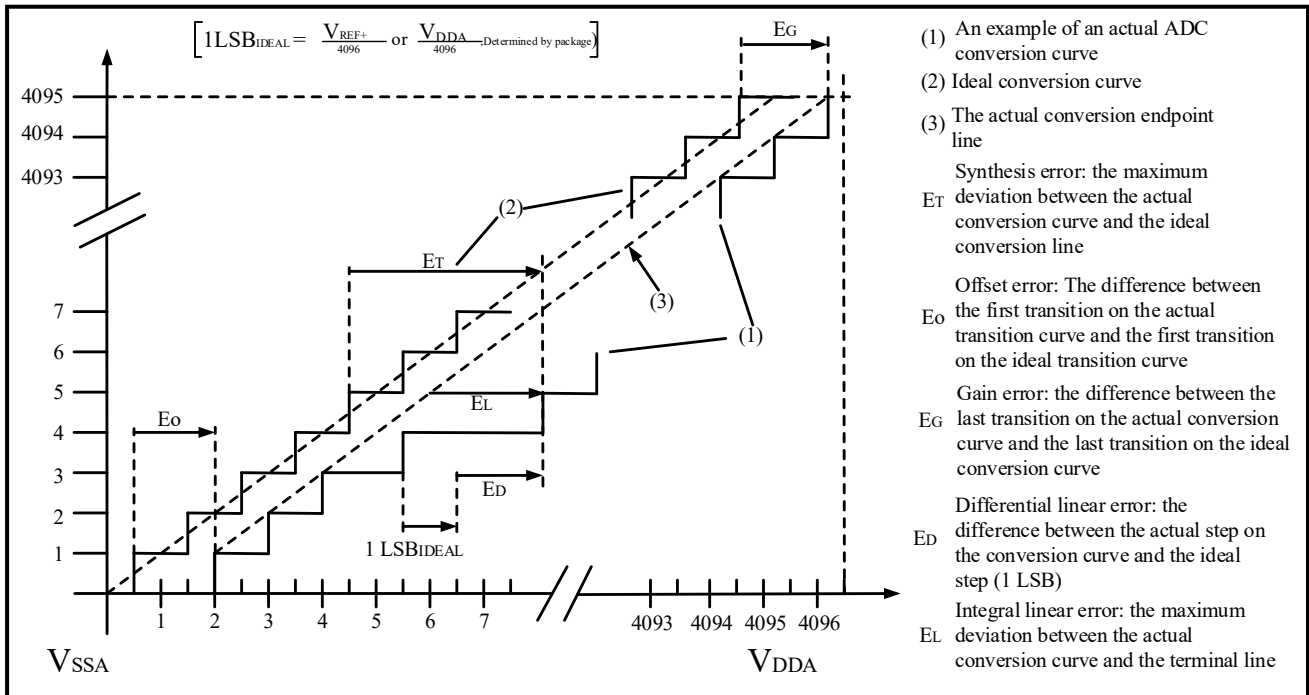
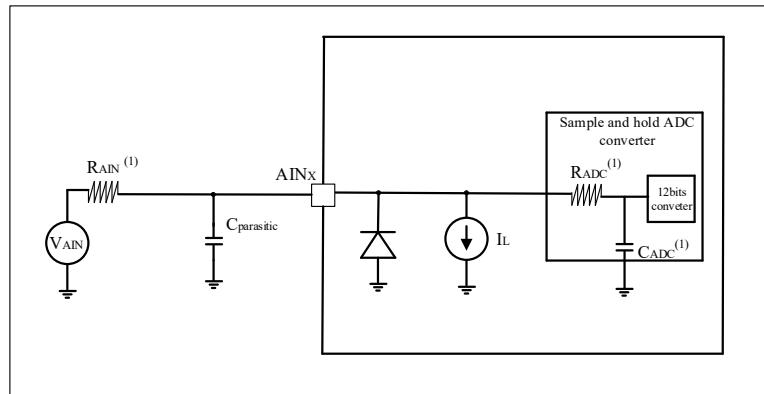


Figure 4-19 Typical Connection Diagram Using ADC



Notes:

(1) For values of R_{AIN} , R_{ADC} , and C_{ADC} , see Table 4-42.

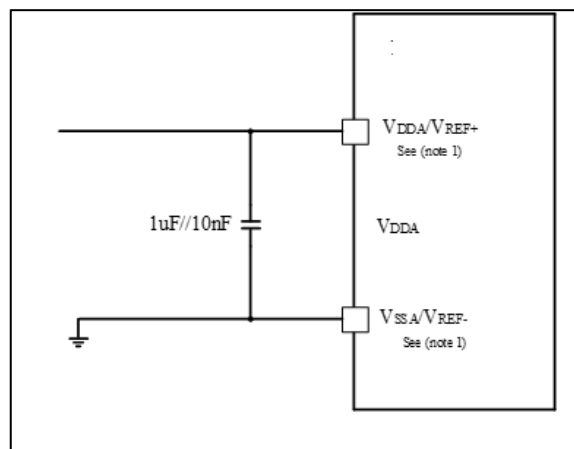
(2) $C_{parasitic}$ indicates parasitic capacitance on PCB (related to welding and PCB layout quality) and pads (approximately 7pF). A larger $C_{parasitic}$ value would reduce the accuracy of the conversion and the solution was to reduce f_{ADC} from medicine.

Note: Input voltage less than -0.2V is prohibited on ADC channel

PCB Design Suggestions

The decoupling of the power supply must be connected in accordance with Figure 4-20. The 10nF capacitors in the picture must be ceramic capacitors (good quality), and they should be as close as possible to the MCU chip.

Figure 4-20 Decoupling Circuit Of Power Supply And Reference Power Supply (V_{REF+} is connected to V_{DDA})



Note: (1) V_{REF+} and V_{REF-} are internally connected to V_{DDA} and V_{SSA} .

4.3.20 Internal Reference Source ($V_{REFBUFF}$) Electrical Parameters

Unless otherwise specified, the parameters in Table 4-45 are measured using ambient temperature, f_{HCLK} frequency and V_{DDA} supply voltage in accordance with the conditions in Table 4-4.

Table 4-45 $V_{REFBUFF}$ Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	Normal mode	2.4	-	3.6	V
$V_{REFBUFF_OUT}$	Voltage reference output	Normal mode	-	2.048	-	V

I_{DDA}	V_{REFBUF} consumption from V_{DDA}	$I_{load} = 0 \mu A$	-	600	-	μA
$t_{START}^{(1)}$	Start-up time	-	1	-	-	us

Note: ⁽¹⁾Guaranteed by design, not tested in production.

4.3.21 12-bit DAC Electrical Parameters

Unless otherwise specified, the parameters of Table 4-46 are measured using ambient temperature, f_{HCLK} frequency, and V_{DDA} supply voltage in accordance with the conditions of Table 4-4.

Table 4-46 DAC Characteristics⁽¹⁾

Symbol	Parameter	Min	Typ	Max	Unit	Annotation
V_{DDA}	Analog supply voltage	2.4	-	3.6	V	
V_{REF+}	The reference voltage	2.4	-	3.6	V	V_{REF+} must always be below V_{DDA}
V_{SSA}	Ground wire	0	-	0	V	
R_L	Load resistance when the buffer is open	5	-	-	$K\Omega$	Minimum load resistance between DAC_OUT and V_{SSA}
C_L	The load capacitance	-	-	50	pF	The maximum capacitance on the DAC_OUT pin
I_{DD}	In work mode DAC DC consumption ($V_{DDA} + V_{REF+}$)	-	425	600	μA	No load. The median value is 0x800
I_{DDQ}	In shut down mode DAC DC consumption ($V_{DDA} + V_{REF+}$)	-	5	-	nA	No load
DAC_OUT Min	The low-end DAC_OUT voltage when the buffer is closed	$V_{SS} + 1LSB$	-	-	V	Give the largest DAC output span. When $V_{REF+} = 3.6V$, corresponding to 12-bit input value 0x0E0~0xF1C. When $V_{REF+} = 2.4V$, corresponding to 12-bit input value 0x155~0xEAB.
	The low-end DAC_OUT voltage when the buffer is opened	0.2	-	-		
DAC_OUT Max	The low-end DAC_OUT voltage when the buffer is closed	-	-	$V_{REF+} - 5LSB$		
	The low-end DAC_OUT voltage when the buffer is opened	-	-	$V_{REF+} - 0.2$		
DNL	Differential non linearity (Difference between two consecutive code)	-	± 2	-	LSB	The DAC configuration is 12 bits
INL	Integral non linearity (difference between measured value at Code I and the value at Code i on a line drawn between Code 0 and last Code 4095)	-	± 7	-	LSB	The DAC configuration is 12 bits
The offset	Offset error (difference between measured value at Code (0x800) and the ideal value = $V_{REF+}/2$)	-	± 15	-	mV	The DAC configuration is 12 bits
		-	± 18	-	LSB	When V_{REF+} is 3.6V, the DAC is configured as 12 bits
Gain error	Gain error	-	± 0.5	-	%	The DAC is configured as 12 bits
amplifier gain	Amplifier gain in open loop	80	85	-	dB	5K Ω load (maximum load), input mid-value 0x800

Symbol	Parameter	Min	Typ	Max	Unit	Annotation
$t_{SETTLING}$	Settling time (full scale: for a 12-bit input code transition between the lowest and the highest input codes when DAC_OUT reaches final value $\pm 1LSB$)	-	5	7	μs	$C_{LOAD} \leq 50pF$ $R_{LOAD} \geq 5K\Omega$
Update rate	Max frequency for a correct DAC_OUT change when small variation in the input code (from code i to i+1LSB)	-	-	1	MS/s	$C_{LOAD} \leq 50pF$ $R_{LOAD} \geq 5K\Omega$
t_{WAKEUP}	Wake up time from closed state (set CHXEN bit in DAC control register)	-	6.5	10	μs	$C_{LOAD} \leq 50pF, R_{LOAD} \geq 5K\Omega$ The input code is between the minimum and maximum possible values
PSRR+	Power supply rejection ratio (to V_{DDA}) (static DC measurement)	-	-67	-40	dB	No $R_{LOAD}, C_{LOAD} \leq 50pF$

Note: ⁽¹⁾Guaranteed by design, not tested in production.

4.3.22 Operational Amplifier (OPAMP) Electrical Parameters

Unless otherwise specified, the parameters in Table 4-47 are measured using ambient temperature, f_{HCLK} frequency, and V_{DDA} supply voltage in accordance with the conditions in Table 4-4.

Table 4-47 OPAMP Characteristics⁽¹⁾

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	-	1.8	-	3.6	V
CMIR	Common mode voltage input range	-	0	-	V_{DDA}	V
V_{OFFSET}	Input offset voltage (after calibration)	-	-	± 1	± 3.5	mV
ΔV_{OFFSET}	Input offset voltage temperature drift	-	-	10	-	UV / °C
I_{LOAD}	Drive current	-	-	-	0.5	mA
I_{DDA}	Operational amplifier current consumption	No load, quiescent mode	-	-	1.5	mA
TS_OPAMP_VOUT	ADC sampling time as opamp output	-	400	-	-	ns
CMMR	Common mode rejection ratio	-	-	84	-	dB
PSRR	Power rejection ratio	-	-	100	-	dB
GBW	Gain bandwidth	-	-	4	-	MHz
SR	Conversion rate	-	-	2.5	-	V/us
RLOAD	Minimum impedance load	-	4	-	-	K Ω
CLOAD	Maximum capacitive load	-	-	-	50	pF
$t_{STARTUP}$	Start-up setup time	$C_{LOAD} \leq 50$ pf, $R_{LOAD} \geq 4$ k Ω , Follower configuration	-	3	-	μs
PGA Gain error	Programmable gain error	Input signal amplitude > 100mV	-	± 2.5	-	%
PGA BW	PGA bandwidth for different noninverting gain	PGA Gain = 2, Cload = 50pF, Rload = 4 K Ω	-	2	-	MHz
		PGA Gain = 4, Cload = 50pF, Rload = 4 K Ω	-	1	-	

Symbol	Parameter	Condition	Min	Typ	Max	Unit
		PGA Gain = 8, Cload = 50pF, Rload = 4 KΩ	-	0.5	-	
		PGA Gain = 16, Cload = 50pF, Rload = 4 KΩ	-	0.25	-	
		PGA Gain = 32, Cload = 50pF, Rload = 4KΩ	-	0.125	-	
en	Voltage noise density	@ 1KHz, Output loaded with 4 KΩ	-	111	-	nV/ $\sqrt{\text{Hz}}$
		@ 10KHz, Output loaded with 4 KΩ	-	44	-	

Note: ⁽¹⁾Guaranteed by design, not tested in production.

4.3.23 Comparator 2(COMP2) Electrical Parameters

Unless otherwise specified, the parameters in Table 4-48 are measured using ambient temperature, f_{HCLK} frequency, and V_{DDA} supply voltage in accordance with the conditions in Table 4-4.

Table 4-48 COMP2 Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	-	1.8	-	3.6	V
V_{IN}	Input voltage range	-	0	-	V_{DDA}	
$t_{\text{START}}^{(1)}$	Comparator startup setup time	-	-	10	-	us
t_{D}	Propagation delay for 200 mV step with 100 mV overdrive	-	-	70	-	ns
V_{OFFSET}	Comparator input offset error	Full common mode range	-	± 10	-	mV
V_{hys}	Comparator hysteresis	No hysteresis	-	0	-	mV
		Low hysteresis	-	10	-	
		Medium hysteresis	-	20	-	
		High hysteresis	-	30	-	
I_{DDA}	Comparator current consumption	Static	-	45	-	μA
		With 50 KHz ± 100 mV Overdrive Square Signal	-	47	-	

Note: ⁽¹⁾Guaranteed by design, not tested in production.

4.3.24 Comparator 1(COMP1) Electrical Parameters

Unless otherwise specified, the parameters in Table 4-49 and Table 4-50 are measured using ambient temperature, f_{HCLK} frequency, and V_{DDA} supply voltage in accordance with the conditions in Table 4-4.

Table 4-49 COMP1 Normal Mode Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	-	1.8	-	3.6	V
V_{IN}	Input voltage range	-	0	-	V_{DDA}	
$t_{\text{STAR}}^{(1)\text{T}}$	Comparator startup setup time	-	-	10	-	us
t_{D}	Propagation delay for 200 mV step with 100 mV overdrive	-	-	70	-	ns
V_{OFFSET}	Comparator input offset error	Full common mode range	-	± 5	± 20	mV
V_{hys}	Comparison hysteresis	No hysteresis	-	0	-	mV

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		Low hysteresis	-	10	-	
		Medium hysteresis	-	20	-	
		High hysteresis	-	30	-	
I _{DDA}	Comparator current consumption	Static	-	45	-	μA
		With 50 kHz ±100 mV overdrive square signal	-	47	-	

Note: ⁽¹⁾Guaranteed by design, not tested in production.

Table 4-50 COMP1 Low Power Mode Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V _{DDA}	Analog supply voltage	-	1.8	-	3.6	V
V _{IN}	Input voltage range	-	0	-	V _{DDA}	
t _{START} ⁽¹⁾	Comparator startup setup time	-	-	15	-	us
t _D	Propagation delay for 200 mV step with 100 mV overdrive	V _{DDA} ≥ 2.7V	-	300	-	ns
V _{OFFSET}	Comparator input offset error	V _{DDA} = 3V, 25°C	-	±10	-	mV
V _{hys}	Comparison hysteresis	No hysteresis	-	0	-	mV
		Low hysteresis	-	10	-	
		Medium hysteresis	-	20	-	
		High hysteresis	-	30	-	
I _{DDA}	Comparator current consumption	Static	-	10	-	μA
		With 50 kHz ±100 mV overdrive square signal	-	11.5	-	

Note: ⁽¹⁾Guaranteed by design, not tested in production.

4.3.25 Liquid Crystal Display Driver (Segment LCD) Interface Characteristics

Unless otherwise specified, the parameters in Table 4-51 are measured using ambient temperature, f_{HCLK} frequency and V_{DDA} supply voltage that meet the conditions in Table 4-4.

Table 4-51 LCD Controller Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V _{LCD}	LCD external voltage		-	-	3.6	V
V _{LCD0}	LCD internal reference voltage 0		-	2.588	-	
V _{LCD1}	LCD internal reference voltage 1		-	2.728	-	
V _{LCD2}	LCD internal reference voltage 2		-	2.863	-	
V _{LCD3}	LCD internal reference voltage 3		-	3.013	-	
V _{LCD4}	LCD internal reference voltage 4		-	3.154	-	
V _{LCD5}	LCD internal reference voltage 5		-	3.283	-	
V _{LCD6}	LCD internal reference voltage 6		-	3.422	-	
V _{LCD7}	LCD internal reference voltage 7		-	3.572	-	
C _{ext}	V _{LCD} external capacitance	Buffer OFF	-	1	-	μF
		Buffer ON	-	1	-	

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{LCD}	Supply current from V_{DD} at $V_{DD} = 3.0$ V	Buffer OFF	-	3	-	μ A
I_{VLCD}	Supply current from V_{LCD} ($V_{LCD} = 3$ V)	Buffer OFF (BUFEN = 0, PON = 0)	-	0.5	-	μ A
		Buffer ON (BUFEN = 1, 1/2 Bias)	-	0.6	-	
		Buffer ON (BUFEN = 1, 1/3 Bias)	-	0.8	-	
		Buffer ON (BUFEN = 1, 1/4 Bias)	-	1	-	
R_{HN}	Total High Resistor value for Low drive resistive network		-	5.5	-	M Ω
R_{LN}	Total Low Resistor value for High drive resistive network		-	240	-	K Ω
V_{44}	Segment/Common highest level voltage		-	V_{LCD}	-	V
V_{34}	Segment/Common 3/4 level voltage		-	3/4 V_{LCD}	-	
V_{23}	Segment/Common 2/3 level voltage		-	2/3 V_{LCD}	-	
V_{12}	Segment/Common 1/2 level voltage		-	1/2 V_{LCD}	-	
V_{13}	Segment/Common 1/3 level voltage		-	1/3 V_{LCD}	-	
V_{14}	Segment/Common 1/4 level voltage		-	1/4 V_{LCD}	-	
V_0	Segment/Common lowest level voltage		-	0	-	

4.3.26 Temperature Sensor (TS) Characteristics

Unless otherwise specified, the parameters in Table 4-52 are measured using ambient temperature, f_{HCLK} frequency, and V_{DDA} supply voltage in accordance with the conditions in Table 4-4.

Table 4-52 Temperature Sensor Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
$T_L^{(1)}$	V_{SENSE} linearity with temperature	-	± 1	± 4	$^{\circ}$ C
Avg_Slope ⁽¹⁾	Average slope	-	-4.0	-	mV/ $^{\circ}$ C
$V_{25}^{(1)}$	Voltage at 25 $^{\circ}$ C	-	1.32	-	V
$t_{START}^{(1)}$	Startup time	-	10	20	μ s
$T_{S_temp}^{(2)(3)}$	ADC sampling time when reading the temperature	8.3	-	-	μ s

Notes:

⁽¹⁾Based on comprehensive evaluation, not tested in production.

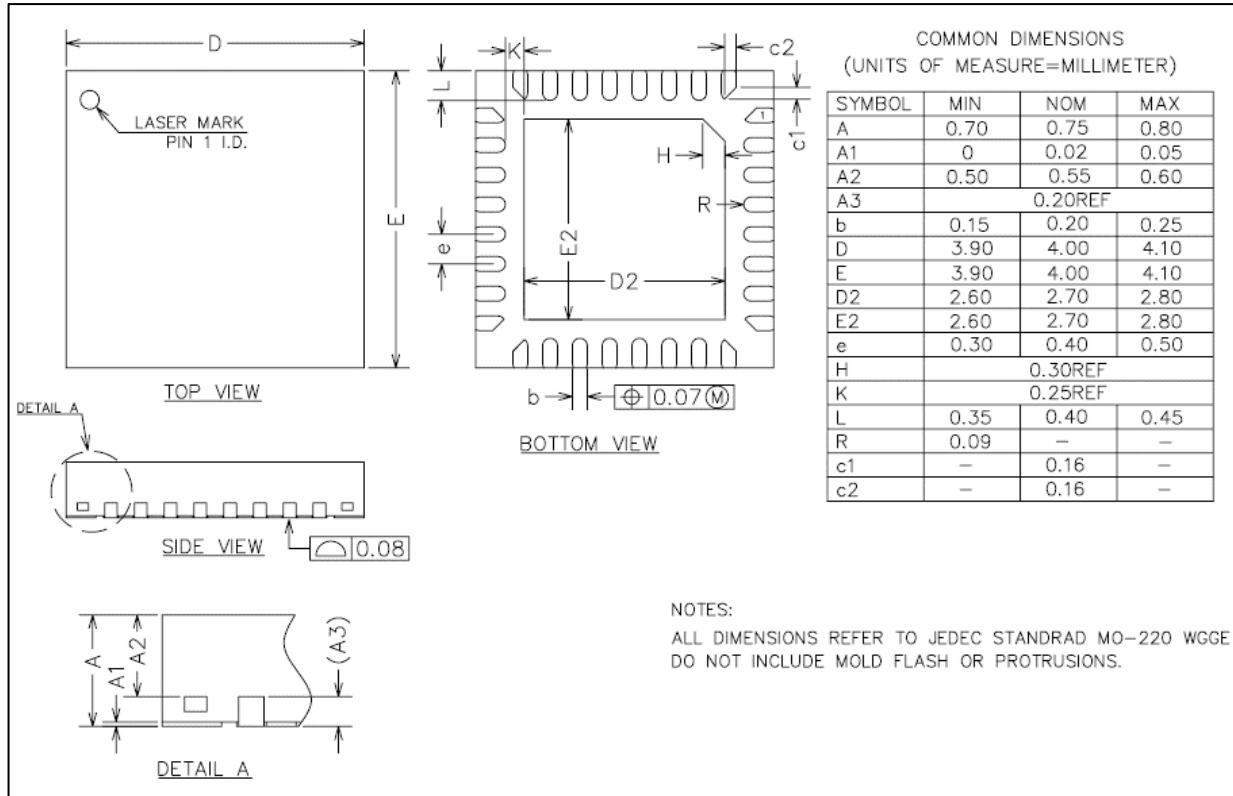
⁽²⁾Guaranteed by design, not tested in production.

⁽³⁾Shortest sampling time can be determined in the application by multiple iterations.

5 Packages

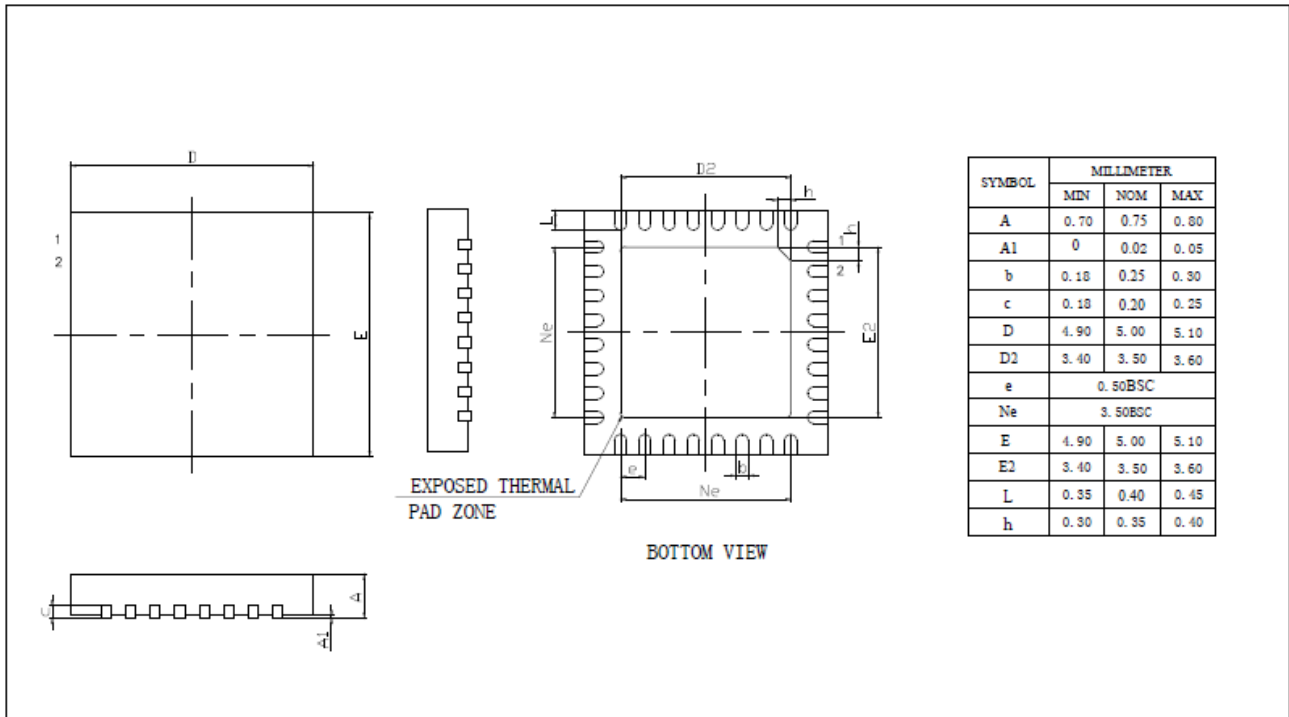
5.1 QFN32 (4mm x 4mm)

Figure 5-1 QFN32 (4mmx4mm) Package Dimensions



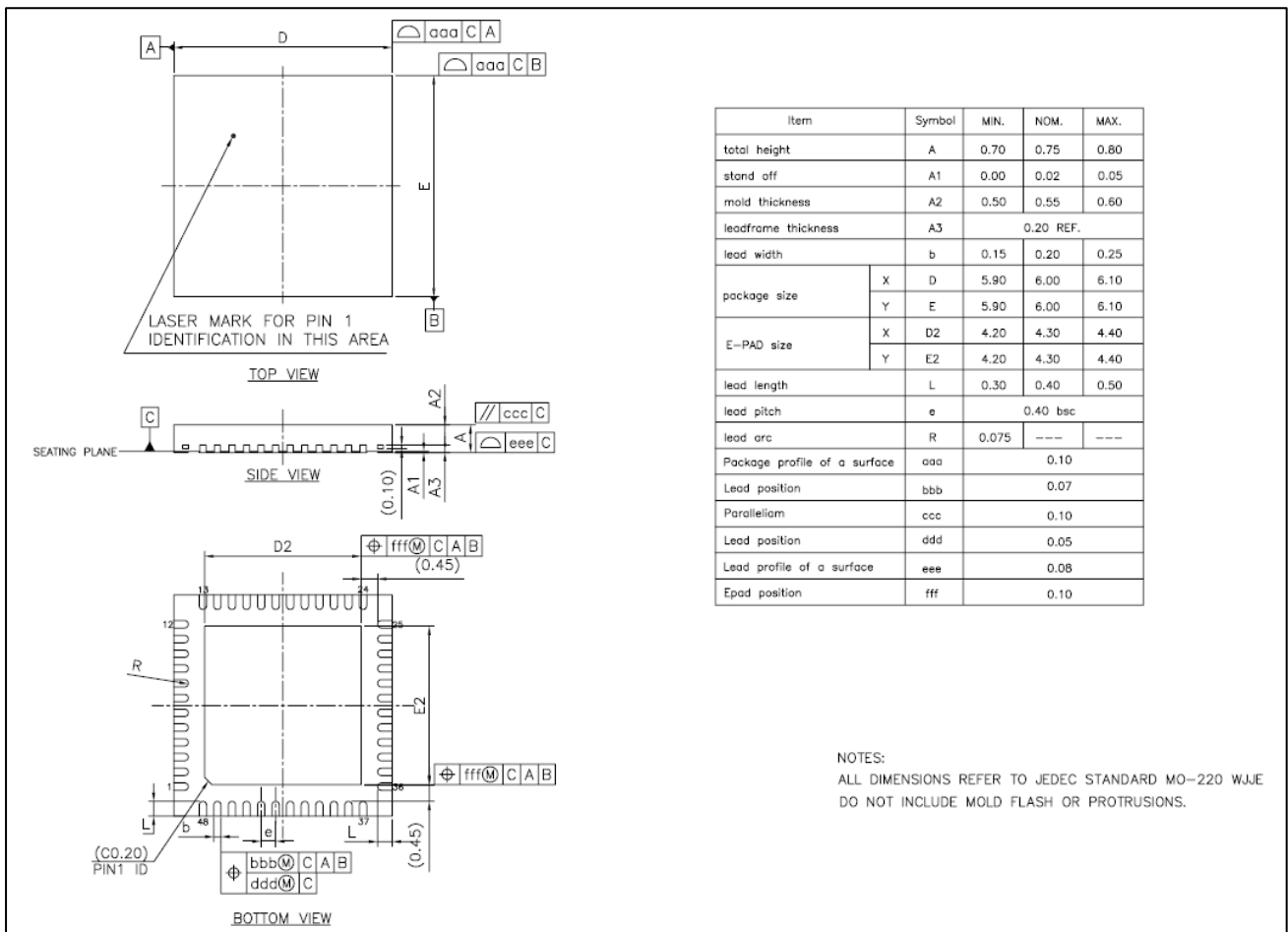
5.2 QFN32 (5mm x 5mm)

Figure 5-2 QFN32 (5mmx5mm) Package Dimensions



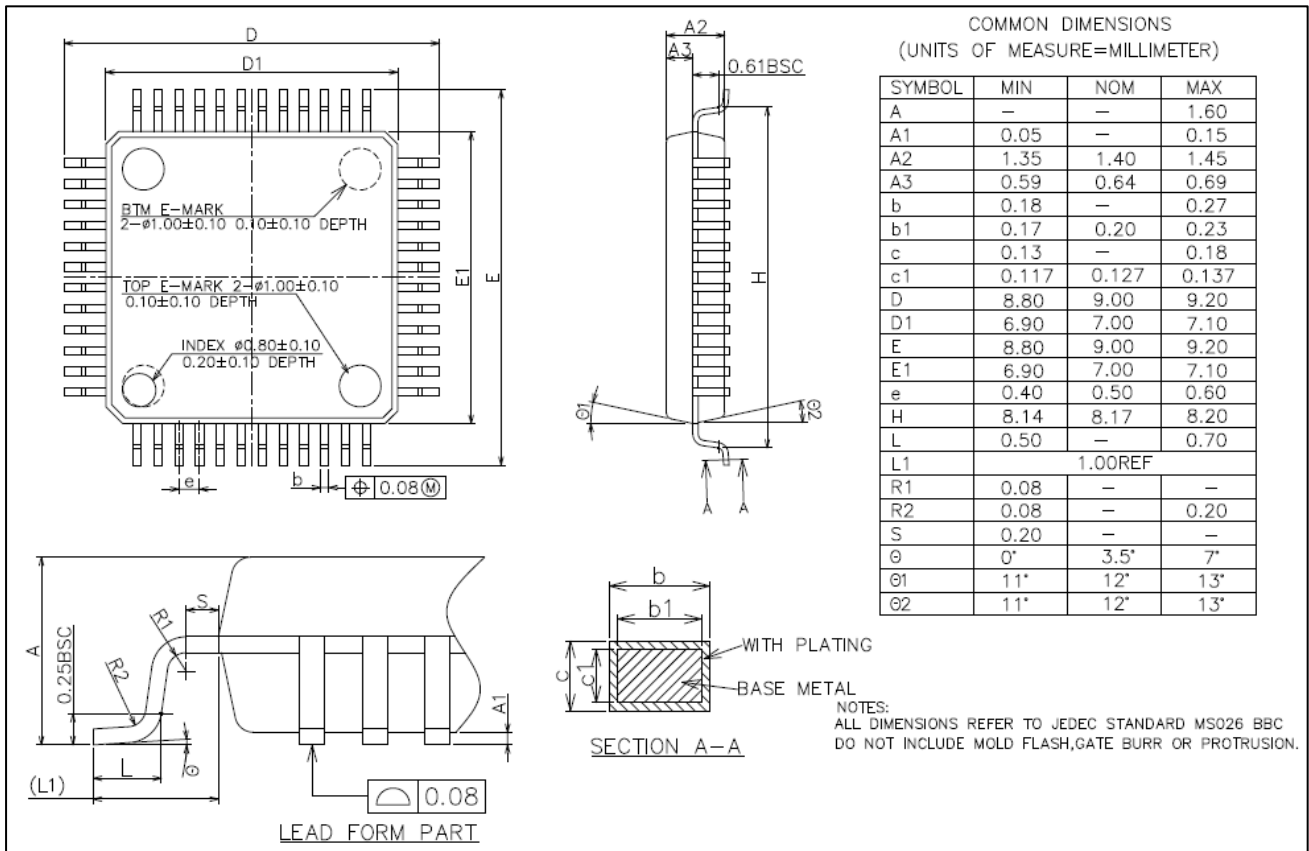
5.3 QFN48 (6mm x 6mm)

Figure 5-3 QFN48 (6mmx6mm) Package Dimensions



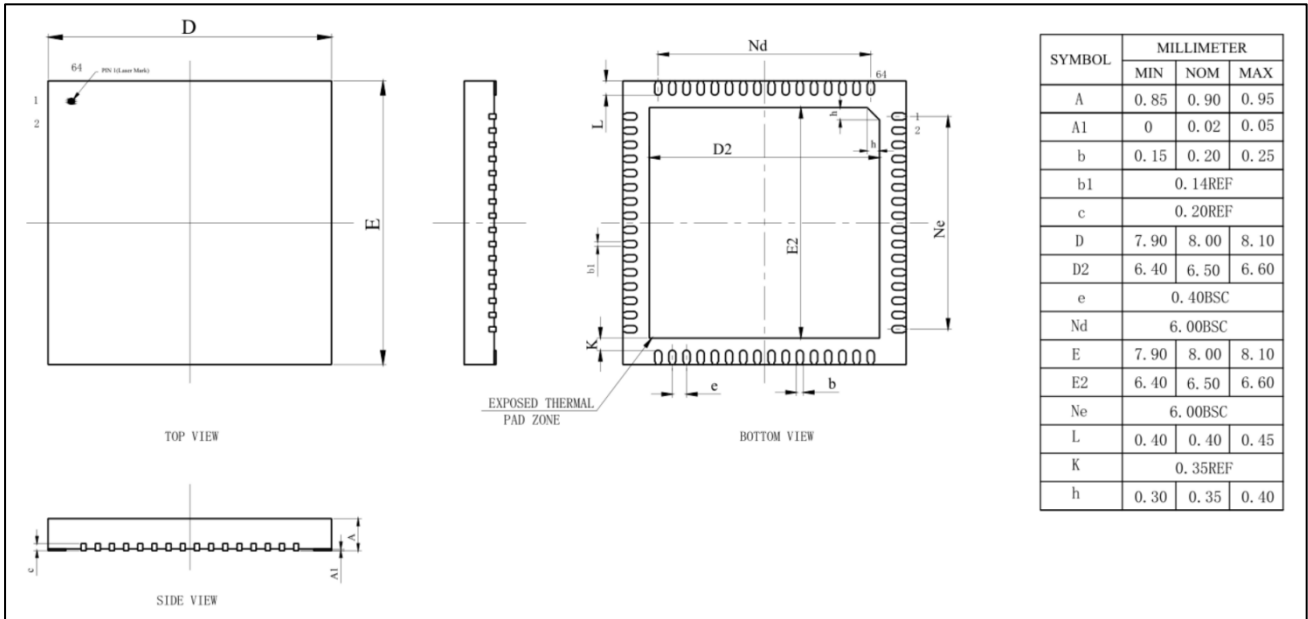
5.4 LQFP48 (7mm x 7mm)

Figure 5-4 LQFP48 (7mmx7mm) Package Dimensions



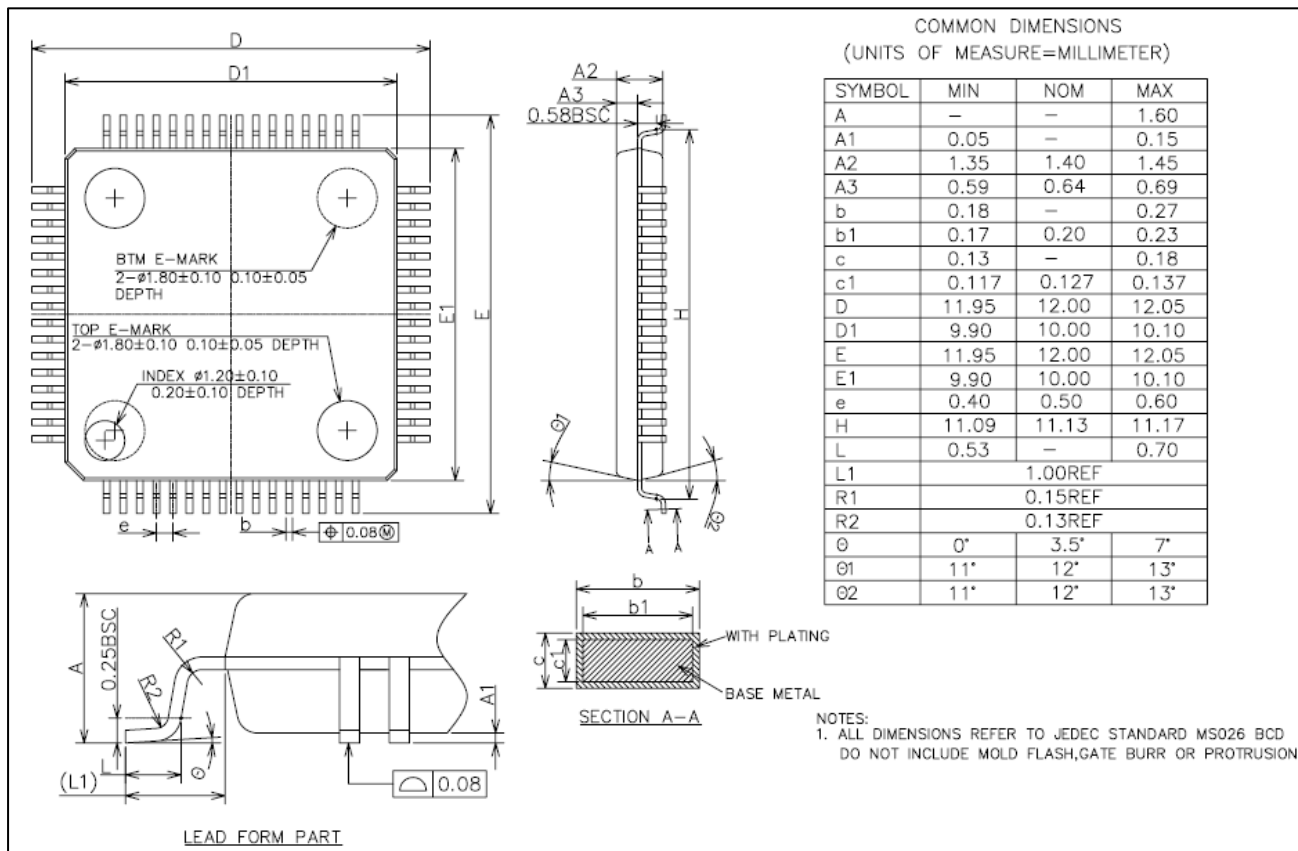
5.5 QFN64 (8mm x 8mm)

Figure 5-5 QFN64 (8mmx8mm) Package Dimensions



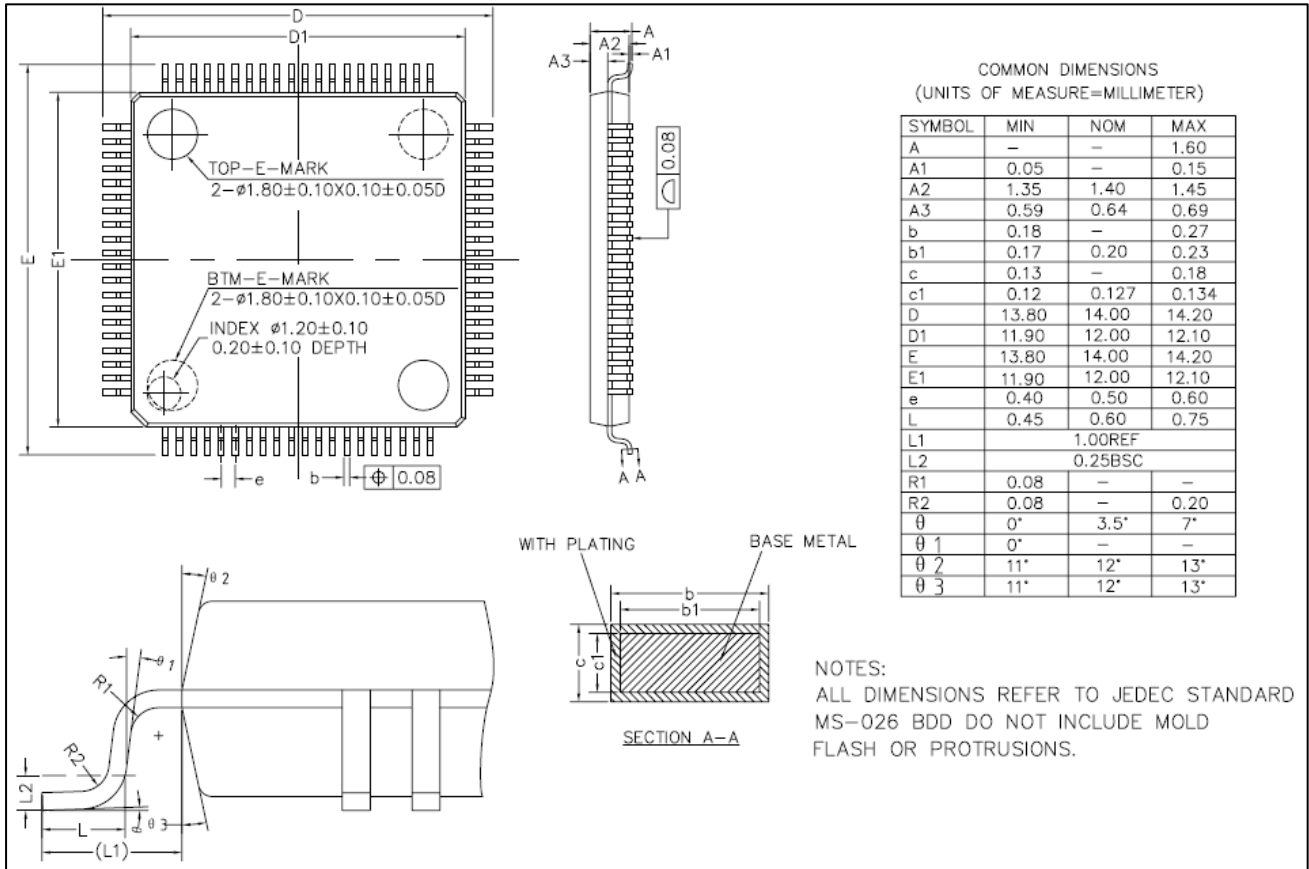
5.6 LQFP64 (10mm x 10mm)

Figure 5-6 LQFP64 (10mmx10mm) Package Dimensions



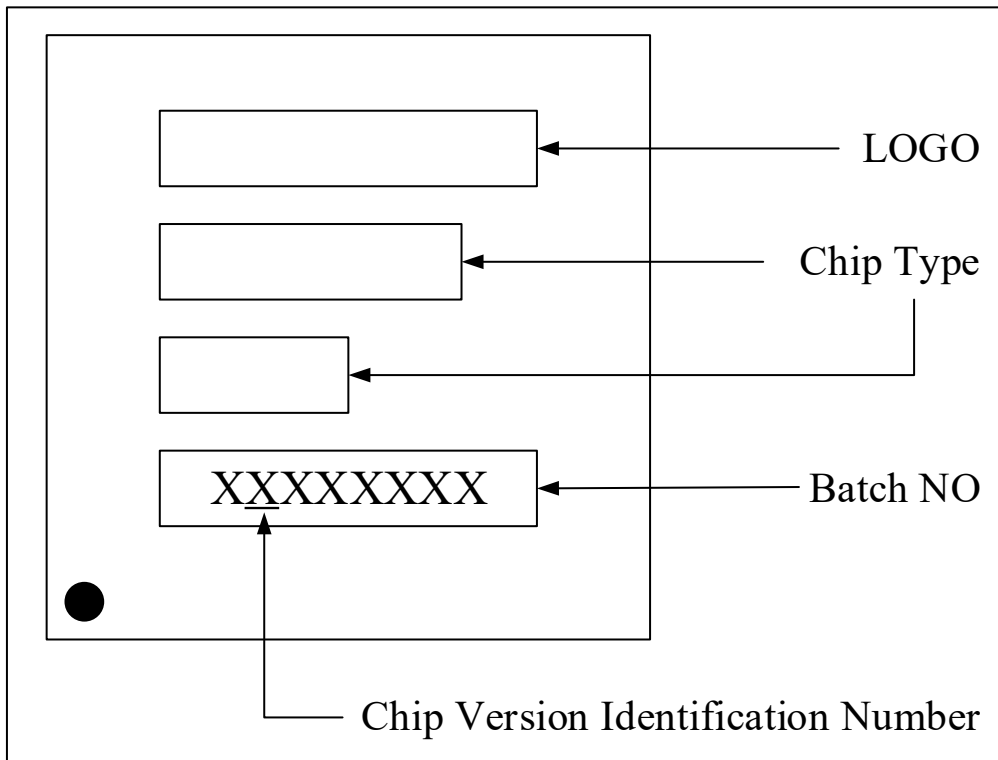
5.7 LQFP80 (12mm x 12mm)

Figure 5-7 LQFP80 (12mmx12mm) Package Dimensions



5.8 Marking Information

Figure 5-8 Marking Information



6 Version History

Version	Date	Changes
V0.8	2020.11.13	Initial release
V0.9	2021.01.25	<ol style="list-style-type: none"> Added N32L401Cx model, does not support USB, LCD, CAN bus functions Corrected the maximum frequency of APB2 is 32MHz, and the maximum frequency of APB1 is 16MHz 1.2 Device List and 3.2 Pin Alternate Definition Add PC10-13, PD2, PD4-PD7 as LCD port for special instructions Notes on adding LCD 1/8 duty cycle mode to the device list
V1.0	2021.04.15	4.3 Chapter Data Check
V1.1	2021.06.12	<ol style="list-style-type: none"> Modify the timing diagram of I2S master mode Added PA2/PA3 COMP_INP version note Add the introduction of LPRUN mode Modify 4.3.18 Figure 4-19 Remove the upper tube of the ADC pin Modify 4.3.11 I/O port characteristics Modify chapter 3.2 to redefine TT as TTA Modify 4.3.7.1 MSI maximum value Modify Figure 4-10 Revised the figure in section 3.1.2 / 3.1.3 Modify Figure 4-3 Modify Table 3 1 IO/level to IO/structure
V1.2	2022.07.11	<ol style="list-style-type: none"> Modify Table 4-18 and add Note 3 Modify Table 2-1 Timer function comparison Added 4.3.19 ADC chapter notes Deleted 3.2 Pin Alternate Definition Note 4 PC13, PC14 and PC15 pins can only sink limited current (3mA) Modify Table 4-42 ADC characteristic t_{STAB} value Modify Table 4-16 to remove ESR CL restrictions Table 3-1 Add NJTRST function Table 4-42 t_{CONV} modify Note 3 Modified Figure 4-8 Typical application using 32.768kHz crystal Add Table 4-32, Table 4-33, Table 4-34, and Table 4-35

		<ol style="list-style-type: none"> 11. Modify Table 4-2 NRST pin injection current 12. Modify the number of shielded interrupt channels of interrupt controller 13. Revise the number of edge detectors of EXTI in Section 2.3 14. Revise the CPU frequency requirements for USB usage in Section 2.4 15. Add the description of LP-sleep mode in Section 2.10 16. Add the wake up condition of STOP2 mode in 2.10 17. Revise PMBus compatibility in I2C main Features in 2.14 18. Revise CRC calculation time to 1 AHB clock cycle 19. Modify the actual frequency deviation of the HSI oscillator in Note 3 of Table 4-18 20. Modify the conditions of the power supply current in Table 4-22: Read mode, $f_{HCLK} = 64\text{MHz}$, one waiting periods 21. Revise GPIOx_DS.DSy[1:0] of 4/8mA in Table 4-28 22. Modify Table 4-37 SPI slave mode input clock duty cycle. 23. Delet N32L401 description. 24. Modify the maximum and minimum values of V_{REFINT} in Table 4-7 and delete the $V_{REFBUFFER}$ 25. Modify the minimum value of f_{HSE_ext} in Table 4-13 and add (Bypass mode) to the table name 26. Modify the maximum value of V_{LSEL} in Table 4-14 and add (Bypass mode) to the table name 27. Figure 4-5 and Figure 4-6 are modified 28. Modify the description of Table 4-15 and comments 29. Figure 4-7 Adding comment 2 30. Modify the maximum and minimum gm values in Table 4-16. Add comment 4 and comment 5 31. Modify the maximum, typical, and minimum values in Table 4-18. Add comment 4 and comment 5 32. Modify the typical and maximum values for $t_{SU(LSD)}$ and typical values for $I_{DD(LSD)}$ in Table 4-19 33. Modify the conditions listed in Table 4-24 34. Table 4-25 Added +85 °C, Added comments 1 and comment 2
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		<ol style="list-style-type: none"> 35. Modify the minimum, typical, and maximum values in Table 4-26 and modify the comments for the table 36. Added Table 4-27 and table comments 37. Modified The conditions in Table 4-28, and added comment 3 38. Delete V_{CRS} listed in Table 4-41 39. Table 4-43 and added table comments 40. Added comment 5 in Table 4-44 41. Modify Figure 4-19 42. Modify the minimum and maximum values of V_{REFBUF_OUT} ,IDDA typical value in Table 4-45 43. Table 4-46 added DAC_OUT Min and DAC_OUT Max, modified the typical values for DNL, INL, and offsets, and modified the typical values and maximum values for $t_{SETTLING}$ 44. Modify the typical value and maximum value of I_{LOAD} , typical value of SR and ,TS_temp in Table 4-47 45. Modify the typical values of LCD internal reference voltage 0 to 7 in Table 4-51 46. Modify the minimum, typical, and maximum values of Avg_Slope, tSTART and TS_temp in Table 4-52 47. Modify the condition and minimum value of t_{RET} in Table 4-23 48. Modify Figure4-16 49. Modify Table 4-48, Table 4-49, Table 4-50 tSTART,tD,VOFFSET and IDDA value. 50. Modify reset description
<p>V1.3</p>	<p>2022.09.14</p>	<ol style="list-style-type: none"> 1. Modify Table4-18 note 3 2. Modify Table4-19 LSI oscillator startup time 3. Modify Table4-26 Weak pull-up equivalent resistance 4. Modify Table4-36 rise time and fall time, and capacitive load 5. Modify Table4-43 comments 6. Modify Table4-50, add t_D condition 7. Modify Table4-52 startup time 8. Add 5V tolerated voltage pin note in chapter 3.2 9. Add the N32L403KBQ7-1

		<ol style="list-style-type: none"> 10. Modify the number of DAC channels in the resource configuration table in chapter 1.2 11. Add note 7 in chatper 4.3.12 12. Delete OPAMP2_VINP function from PB0 in chapter 3.2 13. Modify the table of Flash endurance and data retention life in chapter 4.3.10 14. Modify I2C interface characteristics table 15. Modify PC8 pin serial number in table 3-1
V1.4	2023.02.10	<ol style="list-style-type: none"> 1. Note 4 is Added to describe MSI oscillator characteristics in chapter 4.3.7.1 2. STANDBY mode wakeup delete RTC periodic wakeup in chapter 2.10 3. QFN packaging adds VSS packaging GND pin in chapter 3.2 4. Add N32L402 series type 5. Add N32L402 series not support CAN module in 3.2 chatper

7 Disclaimer

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