

# N32G030 x6/x8

# Product Brief

The N32G030 series adopts a 32-bit Cortex®-M0 core, operating frequency up to 48MHz. The devices integrate up to 64KB embedded flash, 8KB SRAM, multiple communication bus interfaces like U(S)ART, I2C, SPI, and analog interfaces such as a 12-bit 1Msps ADC, an OPAMP, a COMP

## Key Features

### ● CPU Core

- A 32-bit general-purpose microcontroller based on the Cortex®-M0 core; Single-cycle hardware multiply instruction.
- Maximum frequency up to 48MHz

### ● Memories

- Up to 64KByte of embedded Flash memory,
  - supports encrypted storage function.
  - supports hardware ECC check.
  - 100,000 erase/write cycles, 10-years data retention.
- Up to 8KByte embedded SRAM, supports hardware parity check.

### ● Low Power Management

- STOP mode: RTC Run, maximum 8KByte SRAM retention, CPU register retention, all IOs retained.
- PD (Power Down) mode: Supports NRST, PA1\_WKUP0, PA2\_WKUP1 wakeup.

### ● Clock

- HSE: 4MHz~20MHz high-speed external crystal oscillator
- LSE: 32.768KHz low-speed external crystal oscillator
- HSI: high-speed internal RC 8MHz
- LSI: low-speed internal RC 30KHz
- Embedded high-speed PL.
- Supports 2-channels clock output, configurable as system clock, HSI, HSE, LSI, LSE or PLL divisional output

### ● Reset

- Supports power-on/power-down/external pin reset.
- Supports watchdog reset.

### ● Communication Interfaces

- 3xU(S)ART interfaces with a maximum rate up to 3 Mbps,
  - 2x USART interfaces (support 1xISO7816, 1xIrDA, LIN),
  - 1x LPUART interface (supports low power mode, the maximum rate up to 9600bps in this mode, can wake up chip from STOP mode)
- 2x SPI interfaces with speed up to 18 MHz, one of which supports multiplexing with I2S.
- 2x I2C interfaces with speed up to 1 MHz, which can be configured in master/slave mode and support dual address response in slave mode.

### ● Analog Interfaces

- 1x 12bit 1Msps ADC, up to 12 external single-ended input channels

- 1x OPAMP, operational amplifier with built-in up to 32 times programmable gain amplifier (PGA)
- 1x COMP, high-speed analog comparator has an embedded 64-level adjustable reference embedded 64-level adjustable comparison reference

- **GPIO**

- Up to 40 GPIOs that support multiplexed functions.
- Support multiplexed functions.

- **DMA Controller**

- 1x high-speed DMA controller
- Each controller supports 5 channels.
- Channel source address and destination address can be configured arbitrarily.

- **RTC Real-time Clock**

- Supports leap year perpetual calendar, alarm event, periodic wake up
- Supports internal and external clock calibration.

- **Beeper**

- 1x Beeper, supports complementary output, 16mA output drive capacity.

- **Timers and Counters**

- 2x16-bit advanced timers
  - Supports input capture, complementary output, orthogonal encoding input
  - Each timer has 4 independent channels. 3 of which supports 6 pairs complementary PWM outputs.
- 1x16-bit general purpose timer
  - Supports input capture/output compare/PWM output.
  - Each timer has 4 independent channels
- 1x16-bit basic timer
- 1x16-bit low power timer
- 1x24-bit SysTick timer
- 1x7-bit Window Watchdog (WWDG)
- 1x12-bit Independent Watchdog (IWDG)

- **Programming Methods**

- Supports SWD debugging interface.
- Supports UART Bootloader

- **Hardware Divider (HDIV) and Square Root (SQRT)**

- **Security Features**

- Flash storage encryption.
- CRC16/32 computation
- Supports write protection (WRP), multiple read protection (RDP) levels (L0/L1/L2)
- Supports external clock failure detection, tamper detection.

- **96-bit UID and 128-bit UCID**

- **Operating Conditions**

- Operating voltage range: 1.8V~5.5V
- Operating temperature range: -40°C~105°C
- ESD: ±4KV (HBM model), ±1KV (CDM model)

- **Packages**

- UFQFPN20(3mm x 3mm)

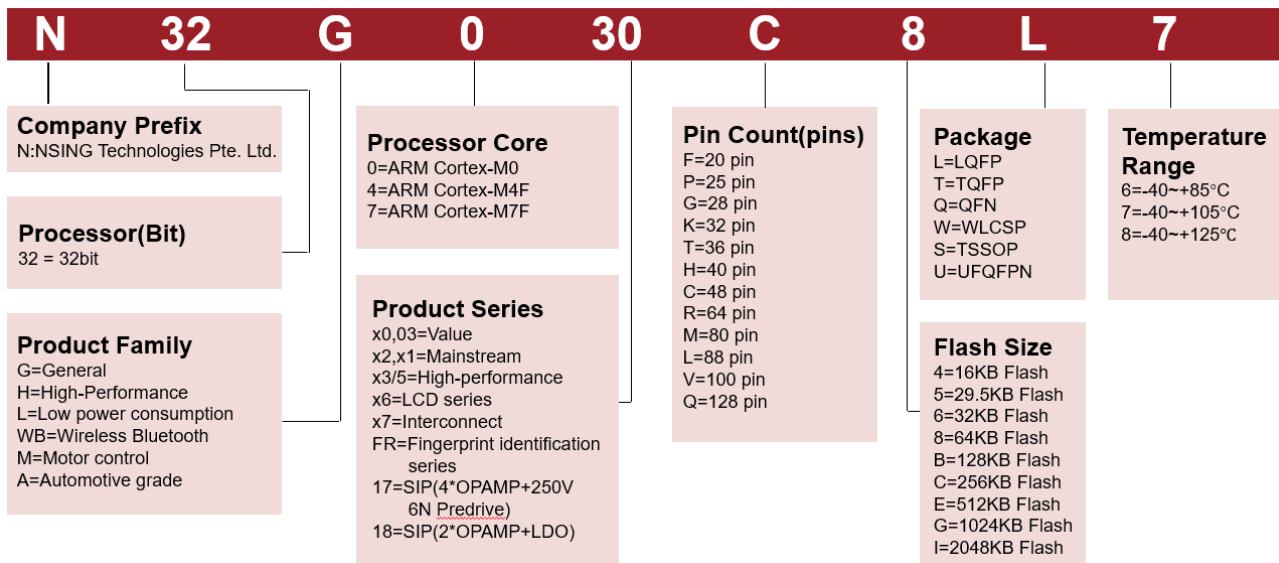
- TSSOP20(6.5mm x 4.4mm)
- QFN32(4mm x 4mm)
- QFN32(5mm x 5mm)
- LQFP32(7mm x 7mm)
- LQFP48(7mm x 7mm)
- TQFP48(7mm x 7mm)

● **Ordering Information**

Reference	Part Number
N32G030x6 N32G030x8	N32G030F6U7, N32G030F6S7 N32G030K6L7, N32G030K6Q7, N32G030K6Q7-1 N32G030K8L7, N32G030C8L7, N32G030C8T7, N32G030F8S7

# 1 Naming Convention

Figure 1-1 N32G030 Series Part Number Information



## 2 Product Configurations

Device	N32G03 0F6U7	N32G03 0F6S7	N32G03 0K6Q7	N32G030 K6Q71	N32G03 0K6L7	N32G03 0K8L7	N32G03 0C8L7	N32G03 0C8T7	N32G03 0F8S7	
Flash Capacity (KB)	32	32	32	32	32	64	64	64	64	
SRAM Capacity (KB)	8	8	8	8	8	8	8	8	8	
CPU Frequency	ARM Cortex-M0 @48MHz									
Operating Environment	1.8~5.5V/-40~105°C									
Timer	General	1								
	Advanced	2								
	Basic	1								
	LPTIM	1								
	RTC	1								
Communication Interface	SPI	2								
	I2S	1								
	I2C	2								
	USART	2								
LPUART	1									
GPIO	16		28		26		40		16	
DMA Number of Channels	5									
12bit ADC Number of channels	1x12bit 7Channel	1x12bit 9Channel	1x12bit 10Channel				1x12bit 12Channel	1x12bit 9Channel		
OPA/COMP	1/1									
Beeper	1									
Algorithm Support	CRC16/CRC32									
Security Protection	Read and Write Protection (RDP/WRP), Storage Encryption									
Package	UFQFP N20	TSSOP2 0	QFN32 <sup>(1)</sup>	QFN32 <sup>(2)</sup>	LQFP32	LQFP32	LQFP48	TQFP48	TSSOP2 0	

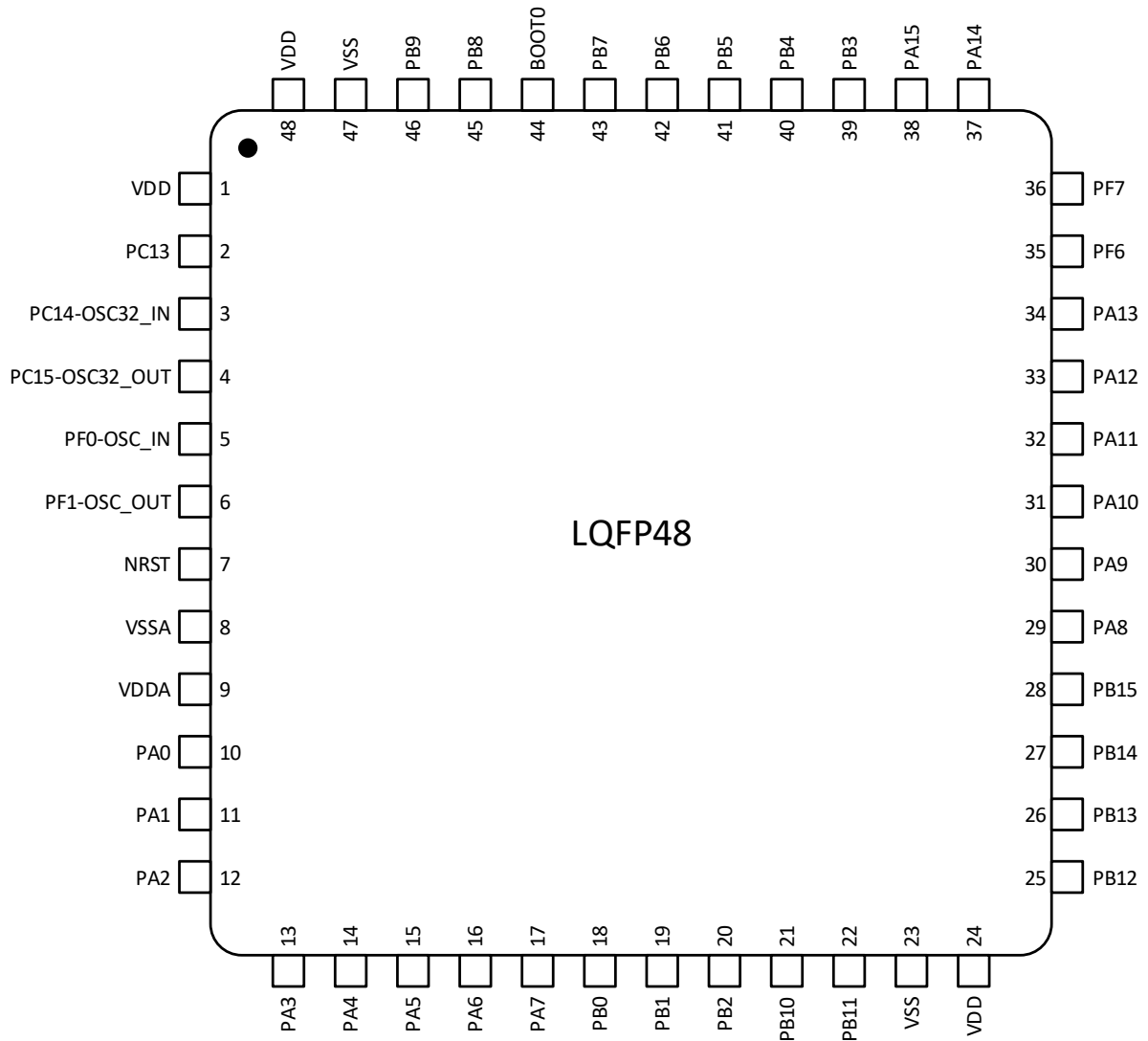
Note: <sup>(1)</sup> QFN32(5mm x 5mm)

<sup>(2)</sup> QFN32(4mm x 4mm)

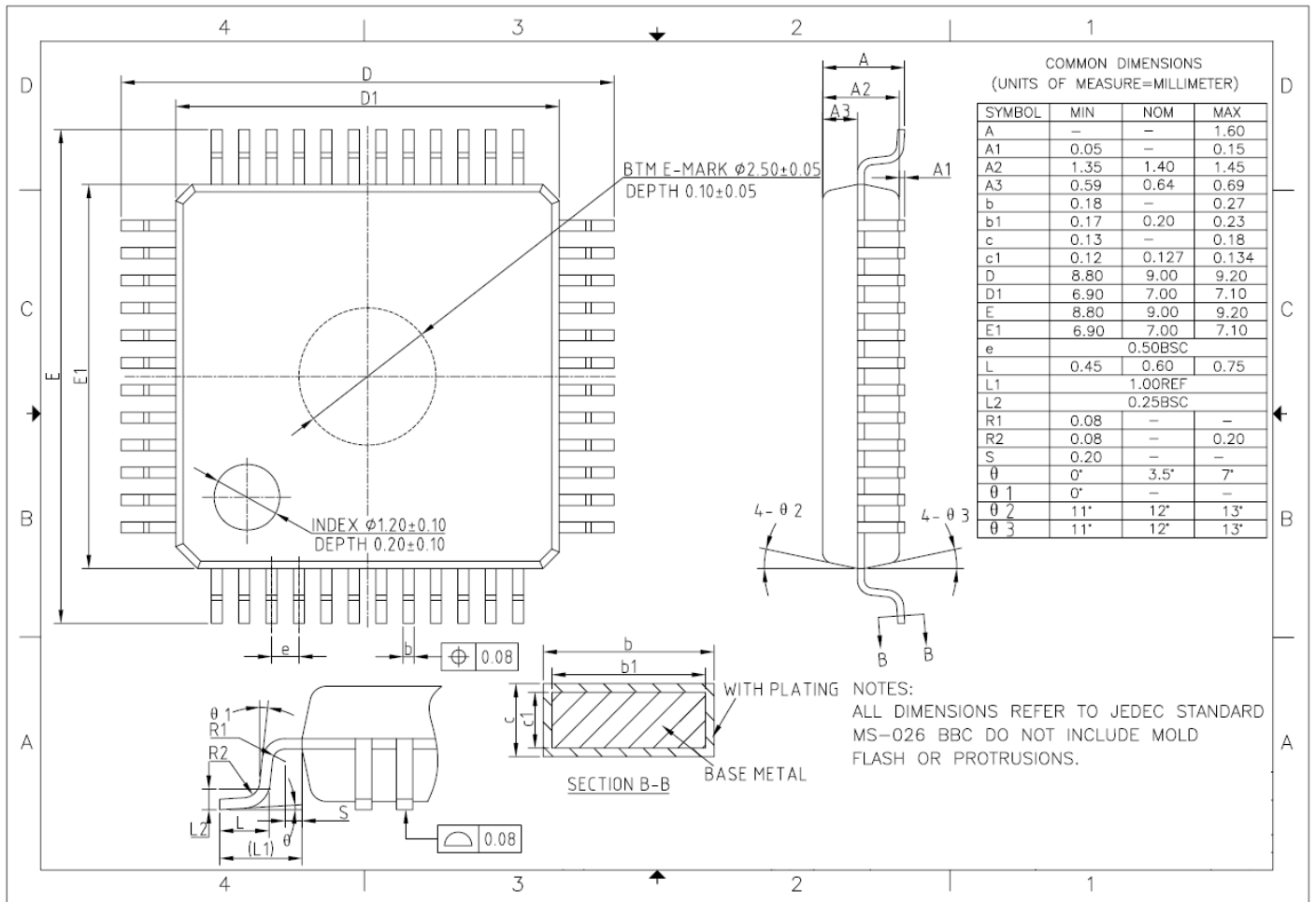
### 3 Packages

#### 3.1 LQFP48 Package

##### 3.1.1 LQFP48 Pin Assignment

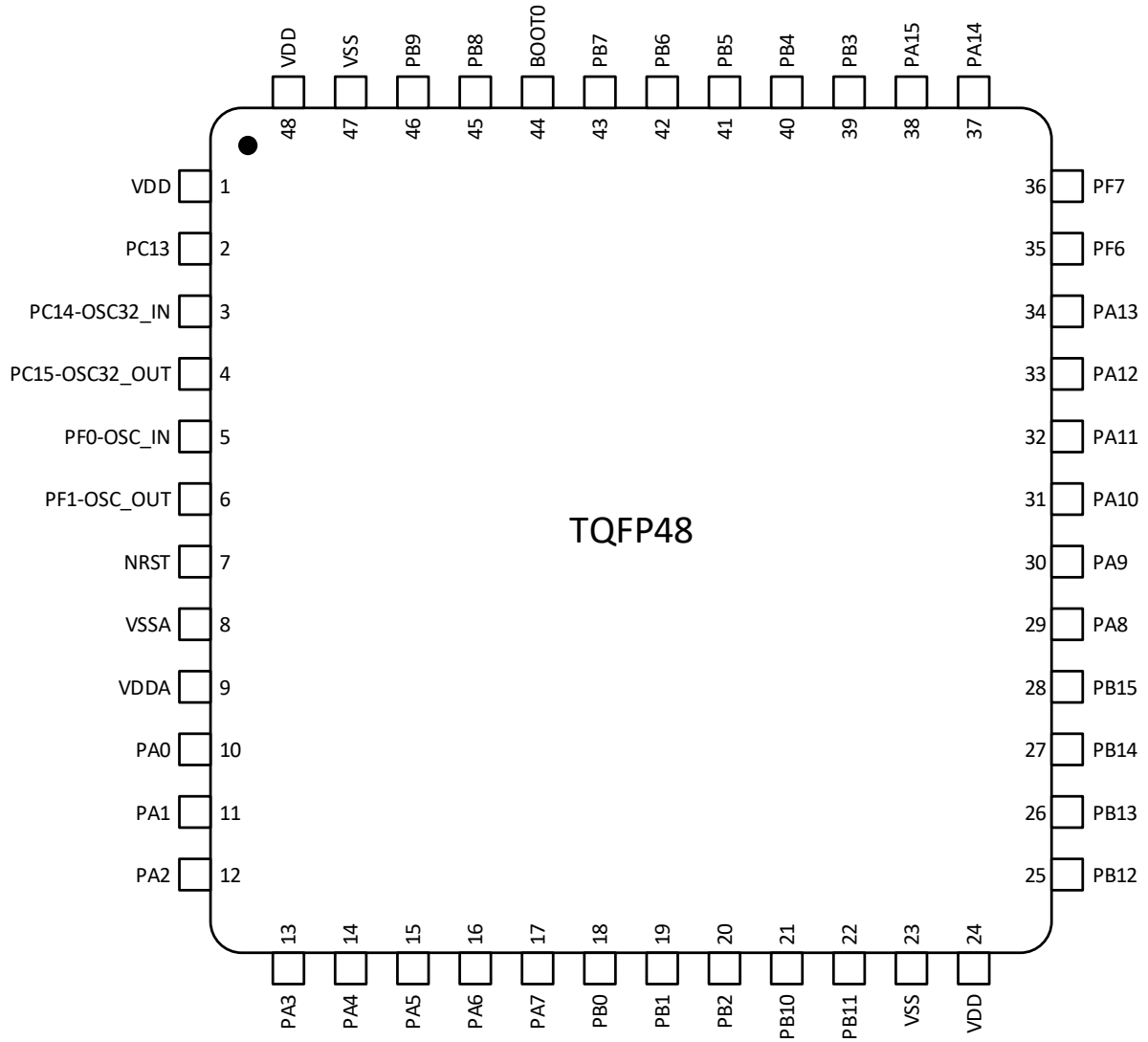


**3.1.2 LQFP48(7mm x 7mm) Package Dimensions**



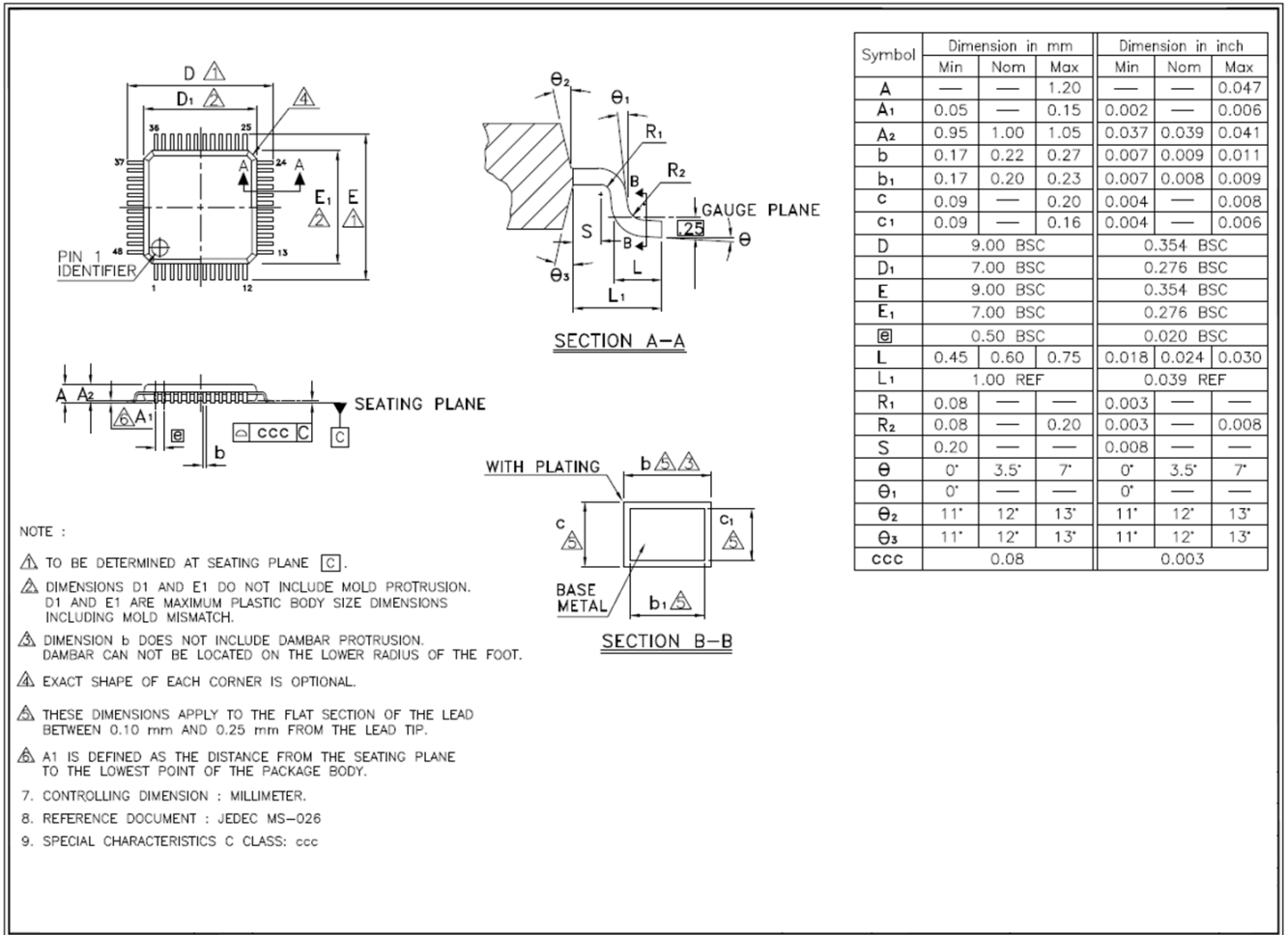
### 3.2 TQFP48 Package

#### 3.2.1 TQFP48 Pin Assignment



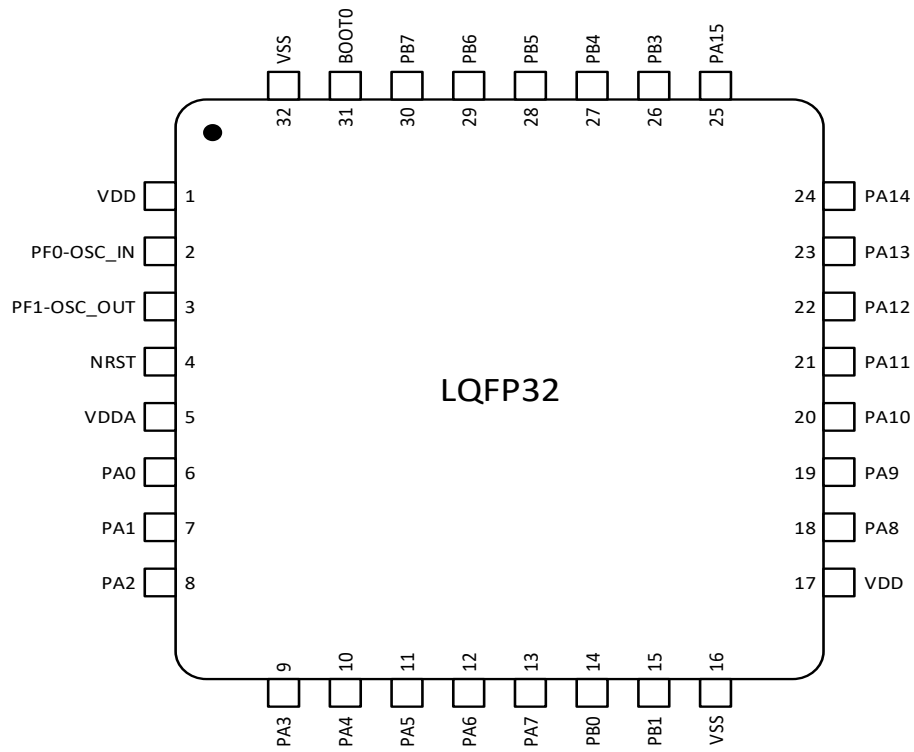


**3.2.2 TQFP48(7mm x 7mm) Package Dimensions**

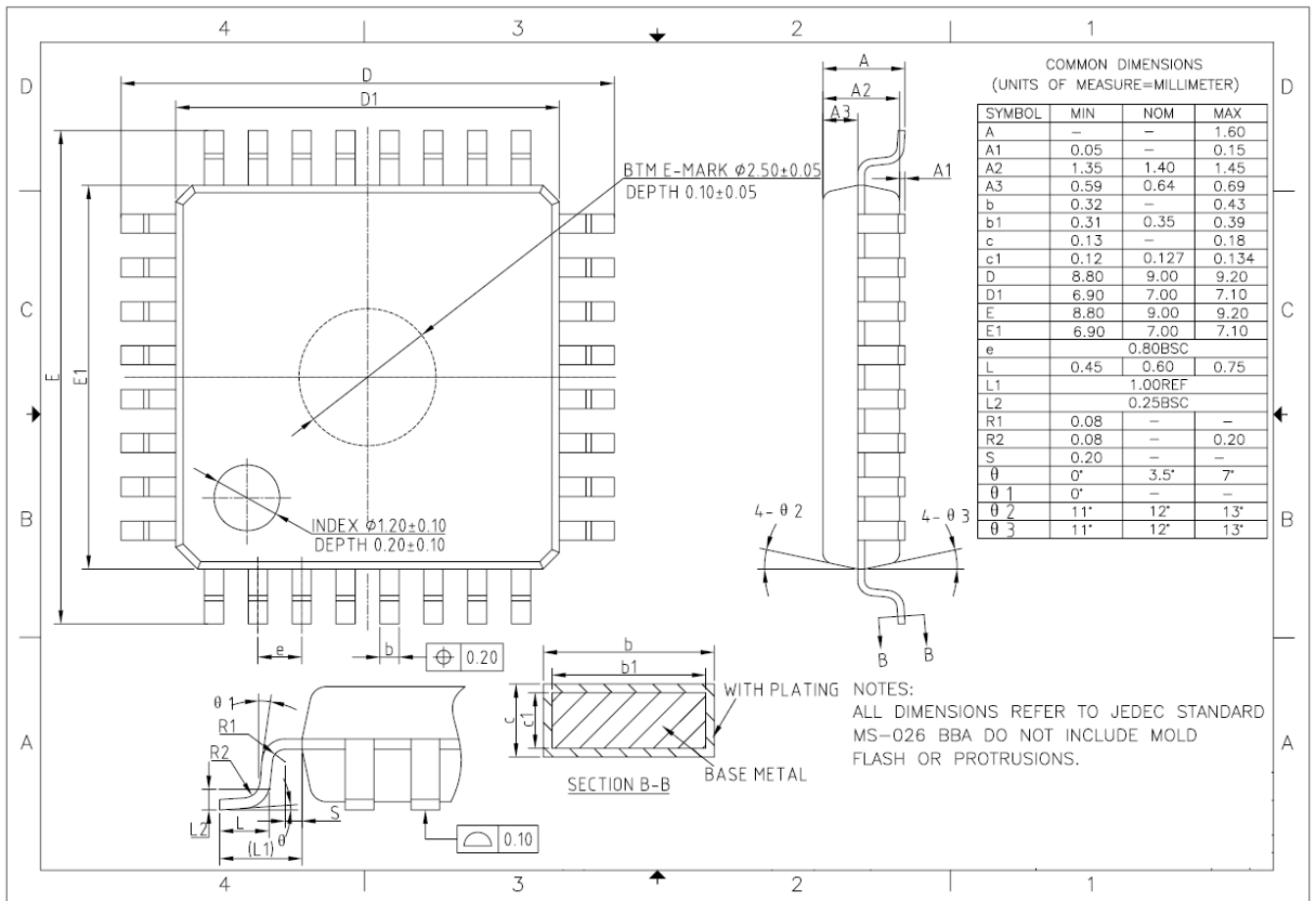


### 3.3 LQFP32 Package

#### 3.3.1 LQFP32 Pin Assignment

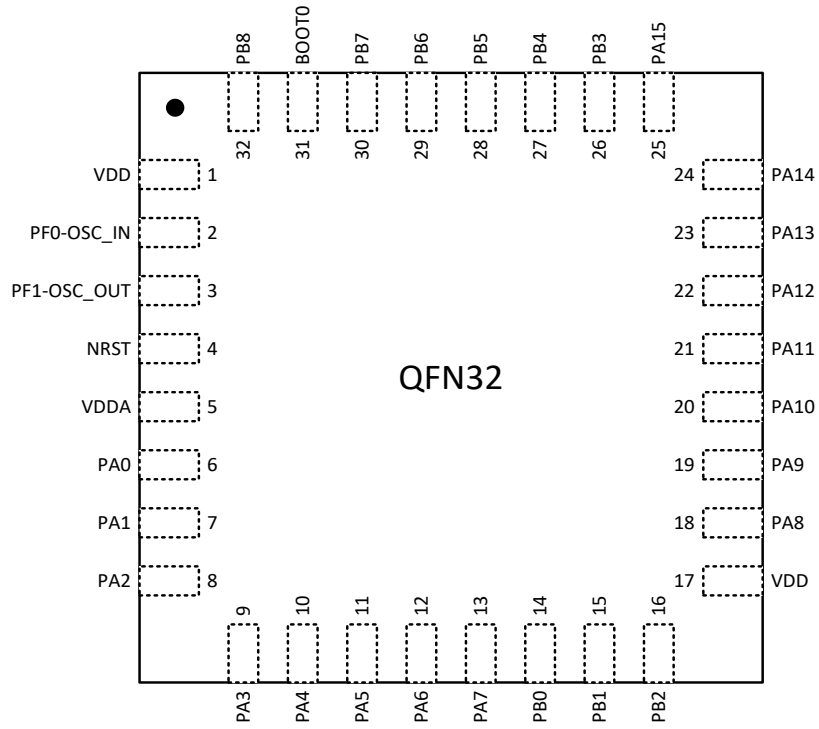


**3.3.2 LQFP32(7mm x 7mm) Package Dimensions**

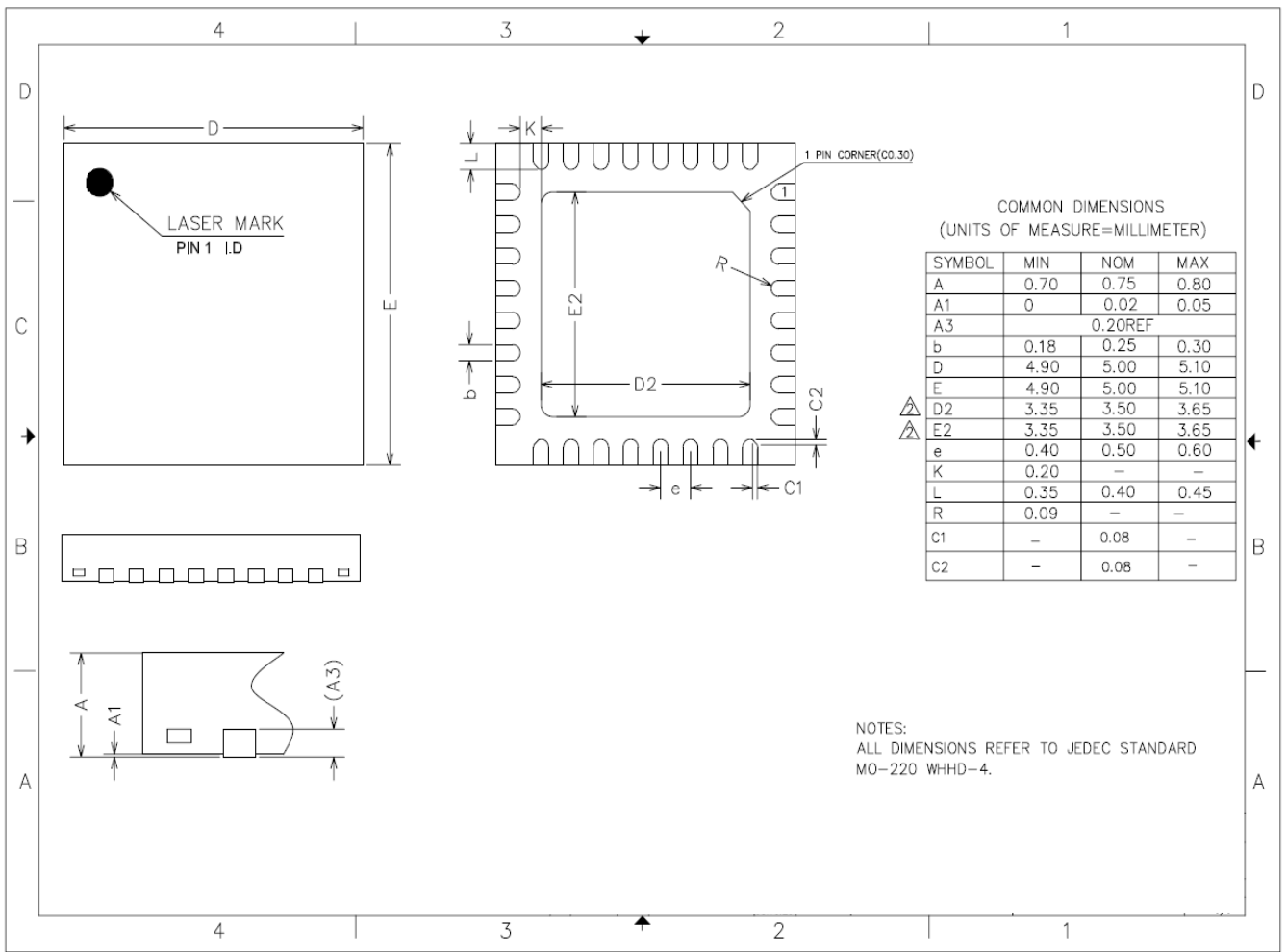


### 3.4 QFN32 Package (5mm x 5mm)

#### 3.4.1 QFN32 (5mm x 5mm) Pin Assignment

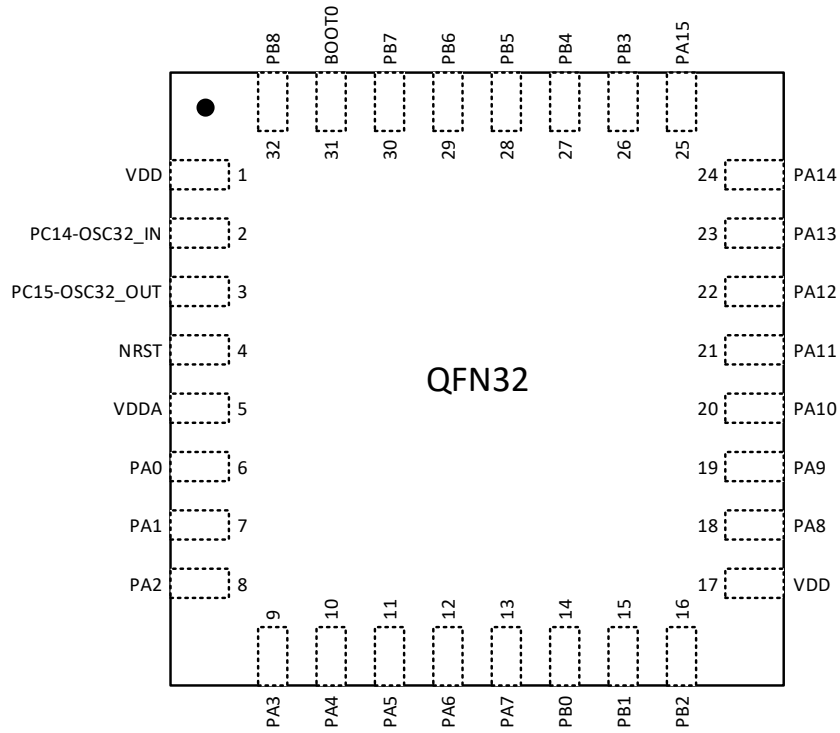


**3.4.2 QFN32 (5mm x 5mm) Package Dimensions**

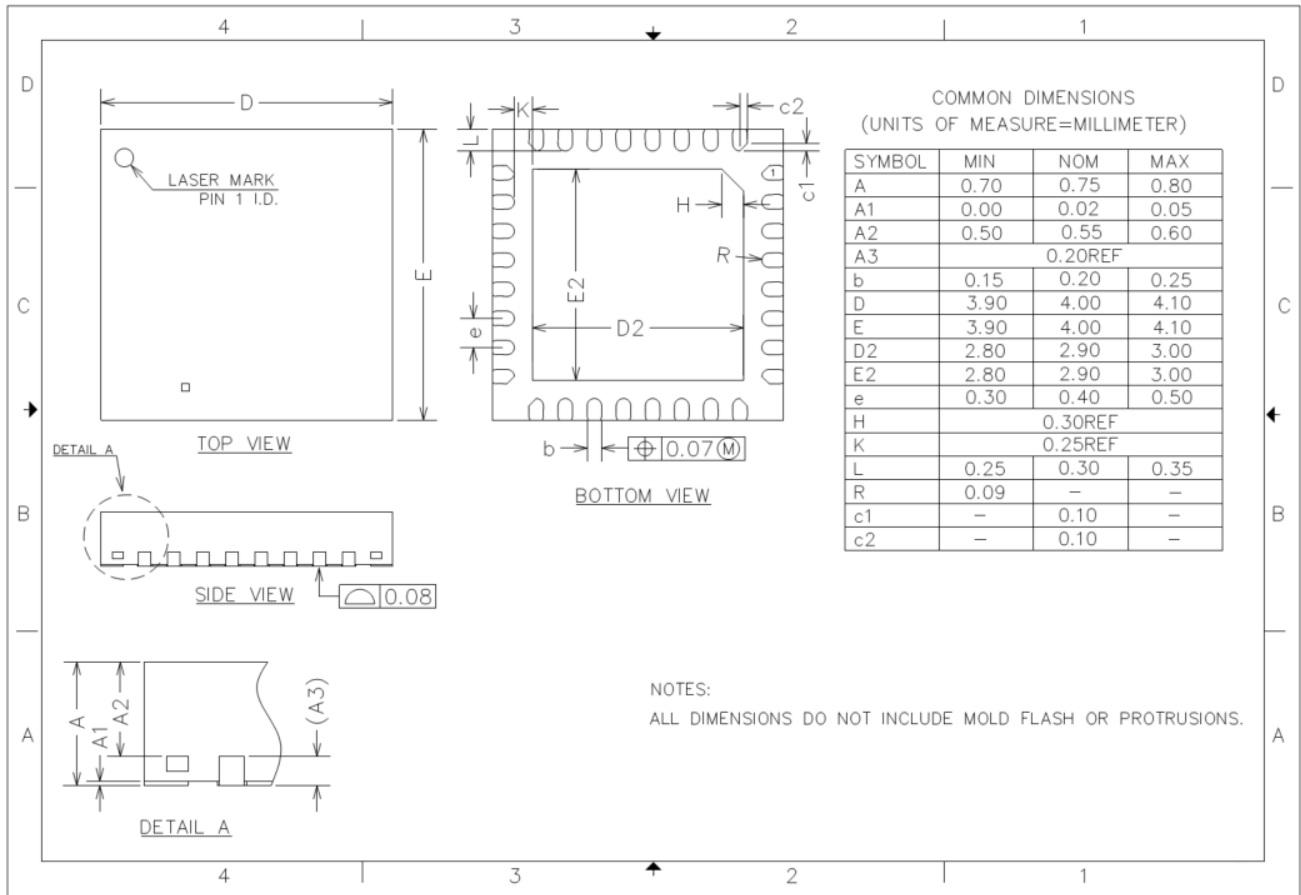


### 3.5 QFN32 Package (4mm x 4mm)

#### 3.5.1 QFN32 (4mm x 4mm) Pin Assignment

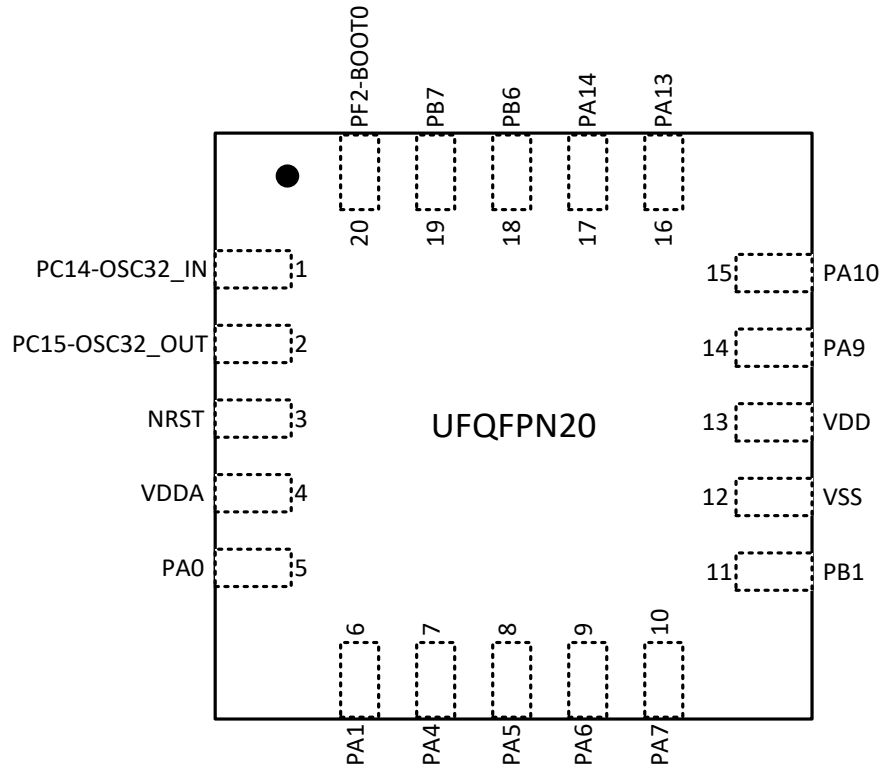


**3.5.2 QFN32 (4mm x 4mm) Package Dimensions**



### 3.6 UFQFPN20 Package

#### 3.6.1 UFQFPN20 Pin Assignment

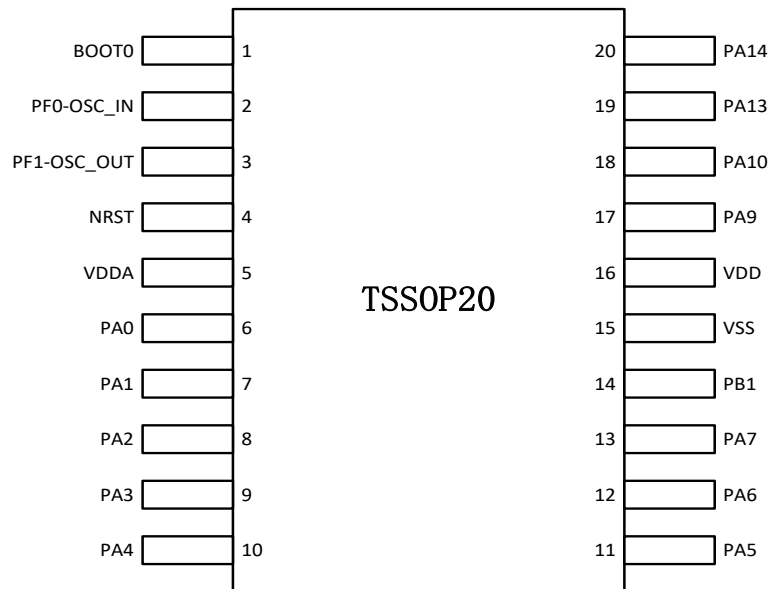




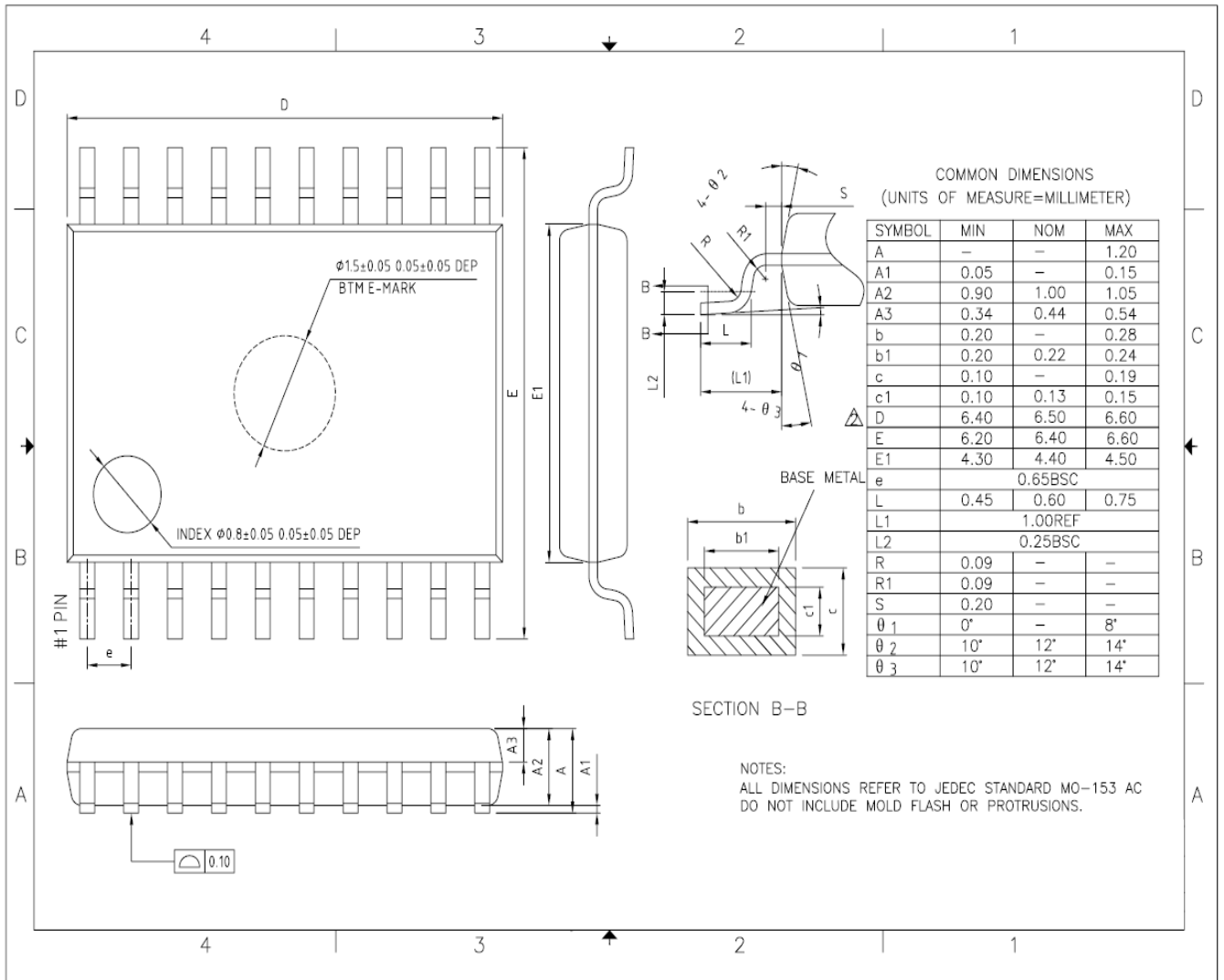


### 3.7 TSSOP20 Package

#### 3.7.1 TSSOP20 Pin Assignment



### 3.7.2 TSSOP20(6.5mm x 4.4mm) Package Dimensions



## 4 Version History

<b>Version</b>	<b>Date</b>	<b>Description</b>
V1.0	2020.12.30	Initial document
V1.1	2021.08.16	<ol style="list-style-type: none"><li>1. Modified to have only 1 comparator</li><li>2. Add TQFP48 package information</li></ol>
V1.2	2022.3.17	Modify the size of retention SRAM to 8Kbyte
V1.3	2022.7.7	<ol style="list-style-type: none"><li>1. Modify the MCO to 2-way output in key feature</li><li>2. Delete reel in part number information</li></ol>
V1.4	2022.9.13	Key feature, delete programmable low level detection and reset.
V1.5.0	2023.7.31	Section 3.5.2. Modify package dimension of QFN32(4mx4m)

## 5 Disclaimer

This document is the exclusive property of NSING TECHNOLOGIES PTE. LTD.(Hereinafter referred to as NSING). This document, and the product of NSING described herein (Hereinafter referred to as the Product) are owned by NSING under the laws and treaties of Republic of Singapore and other applicable jurisdictions worldwide. The intellectual properties of the product belong to Nations Technologies Inc. and Nations Technologies Inc. does not grant any third party any license under its patents, copyrights, trademarks, or other intellectual property rights. Names and brands of third party may be mentioned or referred thereto (if any) for identification purposes only. NSING reserves the right to make changes, corrections, enhancements, modifications, and improvements to this document at any time without notice. Please contact NSING and obtain the latest version of this document before placing orders. Although NATIONS has attempted to provide accurate and reliable information, NATIONS assumes no responsibility for the accuracy and reliability of this document. It is the responsibility of the user of this document to properly design, program, and test the functionality and safety of any application made of this information and any resulting product. In no event shall NATIONS be liable for any direct, indirect, incidental, special, exemplary, or consequential damages arising in any way out of the use of this document or the Product.

NATIONS Products are neither intended nor warranted for usage in systems or equipment, any malfunction or failure of which may cause loss of human life, bodily injury or severe property damage. Such applications are deemed, 'Insecure Usage'. Insecure usage includes, but is not limited to: equipment for surgical implementation, atomic energy control instruments, airplane or spaceship instruments, all types of safety devices, and other applications intended to supporter sustain life. All Insecure Usage shall be made at user's risk. User shall indemnify NATIONS and hold NATIONS harmless from and against all claims, costs, damages, and other liabilities, arising from or related to any customer's Insecure Usage Any express or implied warranty with regard to this document or the Product, including, but not limited to. The warranties of merchantability, fitness for a particular purpose and non-infringement are disclaimed to the fullest extent permitted by law. Unless otherwise explicitly permitted by NATIONS, anyone may not use, duplicate, modify, transcribe or otherwise distribute this document for any purposes, in whole or in part.