

# N32G031 x6/x8

# Product Instruction

N32G031 series based on Arm® Cortex®-M0, run up to 48MHz, up to 64KB embedded flash, 8KB SRAM, integrated analog interface, 1x12bit 1MSPS ADC, 1xOPAMP, 1xcomparator, integrated multi-channel U(S)ART, I2C, SPI and other digital communication interfaces.

## Key feature

### ● Core

- A 32-bit general-purpose microcontroller based on the Arm® Cortex®-M0 core, Single-cycle hardware multiply instruction
- Run up to 48MHz

### ● Encrypted memory

- Up to 64KByte embedded Flash memory, supports encrypted storage, supports hardware ECC verification, data 100,000 cycling and 10 years of data retention
- SRAM of 8KB, supporting hardware parity

### ● Low-power management

- Stop mode: RTC Run, maximum 8KByte SRAM retention, CPU register retention, all IO retention
- Power Down mode: support 3 IO wakeup

### ● Clock

- HSE: 4MHz~20MHz external high-speed crystal
- LSE: 32.768KHz external low-speed crystal
- HSI: Internal high-speed RC OSC 8MHz
- LSI: Internal low-speed RC OSC 30KHz
- Built-in high-speed PLL
- MCO: Support 2-way clock output, configurable SYSCLK, HSI, HSE, LSI, LSE, and PLL clock output that can be divided.

### ● Reset

- Support power-on/power-off/external pin reset
- Support watchdog reset

### ● Communication interface

- 3xU(S)ART, with a maximum rate of 3 Mbps, of which 2 USART interfaces (support 1xISO7816, 1xIrDA, LIN), 1 of which support low power (LPUART, the highest communication rate in this mode is 9600bps), Stop mode can be awakened
- 2xSPI, up to 18 MHz, one of which supports multiplexing with I2S
- 2xI2C, the rate is up to 1 MHz, which can be configured in master/slave mode and support dual address response in slave mode

### ● Analog interface

- 1x12bit 1MSPS ADC, up to 12 external single-ended input channels
- 1xOPAMP, internal programmable gain amplifier up to 32 times

- 1xCOMP (Comparator has an internal independent 6bit DAC)
- **Up to 40 GPIOs**
- **1xDMA, 5-channel, channel source address and destination address can be arbitrarily configurable**
- **1x RTC real-time clock, support leap year perpetual calendar, alarm event, periodic wake up, support internal and external clock calibration**
- **1xBeeper, support complementary output, 16mA output drive capacity**
- **Timer counter**
  - 2x16-bit advanced timer counters, support input capture, complementary output, orthogonal encoding input, each timer support 4 independent channels. Each timer support 3 pairs complementary PWM outputs
  - 1x16-bit general purpose timer counters, 4 independent channels, supports input capture/output compare/PWM output
  - 1x16-bit basic timer counters
  - 1x16-bit low power timer counter. support single pulse and double pulse counting function, can work in STOP mode
  - 1x24-bit SysTick
  - 1x7-bit Window Watchdog (WWDG)
  - 1x12-bit Independent watchdog (IWDG)
- **Programming mode**
  - Support SWD online debugging interface
  - Support UART Bootloader
- **Hardware Divider(HDIV)and Square Root(SQRT)**
- **Security features**
  - Flash storage encryption
  - CRC16/32 calculation
  - Support write protection(WRP), multiple read protection(RDP) levels (L0/L1/L2)
  - Support external clock failure detection, tamper detection
- **96-bit UID and 128-bit UCID**
- **Working conditions**
  - Operating voltage Range: 1.8V~5.5V
  - Operating Temperature Range: -40°C~105°C
  - ESD: ±4KV (HBM model), ±1KV (CDM model)
- **Package**
  - UFQFPN20(3mm x 3mm)
  - TSSOP20(6.5mm x 4.4mm)
  - QFN32(4mm x 4mm)
  - QFN32(5mm x 5mm)
  - LQFP32(7mm x 7mm)
  - LQFP48(7mm x 7mm)
- **Order model**

Series	Part Number
N32G031x6 N32G031x8	N32G031F6U7, N32G031F6S7, N32G031K6L7, N32G031K6Q7, N32G031K6Q7-1, N32G031F8U7, N32G031F8S7, N32G031K8L7, N32G031K8Q7, N32G031K8Q7-1, N32G031C8L7



## 2 List of devices

Table 2-1 N32G031 Series devices features and peripheral list (1)

Part Number	N32G031 F8U7	N32G031 F8S7	N32G031 K8Q7	N32G031 K8Q7-1	N32G031 K8L7	N32G031 C8L7
Flash capacity (KB)	32	32	32	32	32	64
SRAM capacity (KB)	64	64	64	64	64	64
CPU frequency	ARM Cortex-M0 @48MHz					
working environment	1.8~5.5V/-40~105 °C					
Timer	General	1				
	Advanced	2				
	Basic	1				
	LPTIM	1				
	RTC	1				
communication interface	SPI	2				
	I2S	1				
	I2C	2				
	USART	2				
	LPUART	1				
GPIO	16		28		26	40
DMA Number of Channels	16					
12bit ADC Number of channels	1x12bit 7Channel	1x12bit 9Channel	1x12bit 10Channel			1x12bit 12Channel 1
OPA/COMP	1/1					
Beeper	1					
Algorithm support	CRC16/CRC32					
security protection	Read and write protection (RDP/WRP), storage encryption					
Package	UFQFPN20	TSSOP20	QFN32 (5mmx5mm)	QFN32 (4mmx4mm)	LQFP32	LQFP48

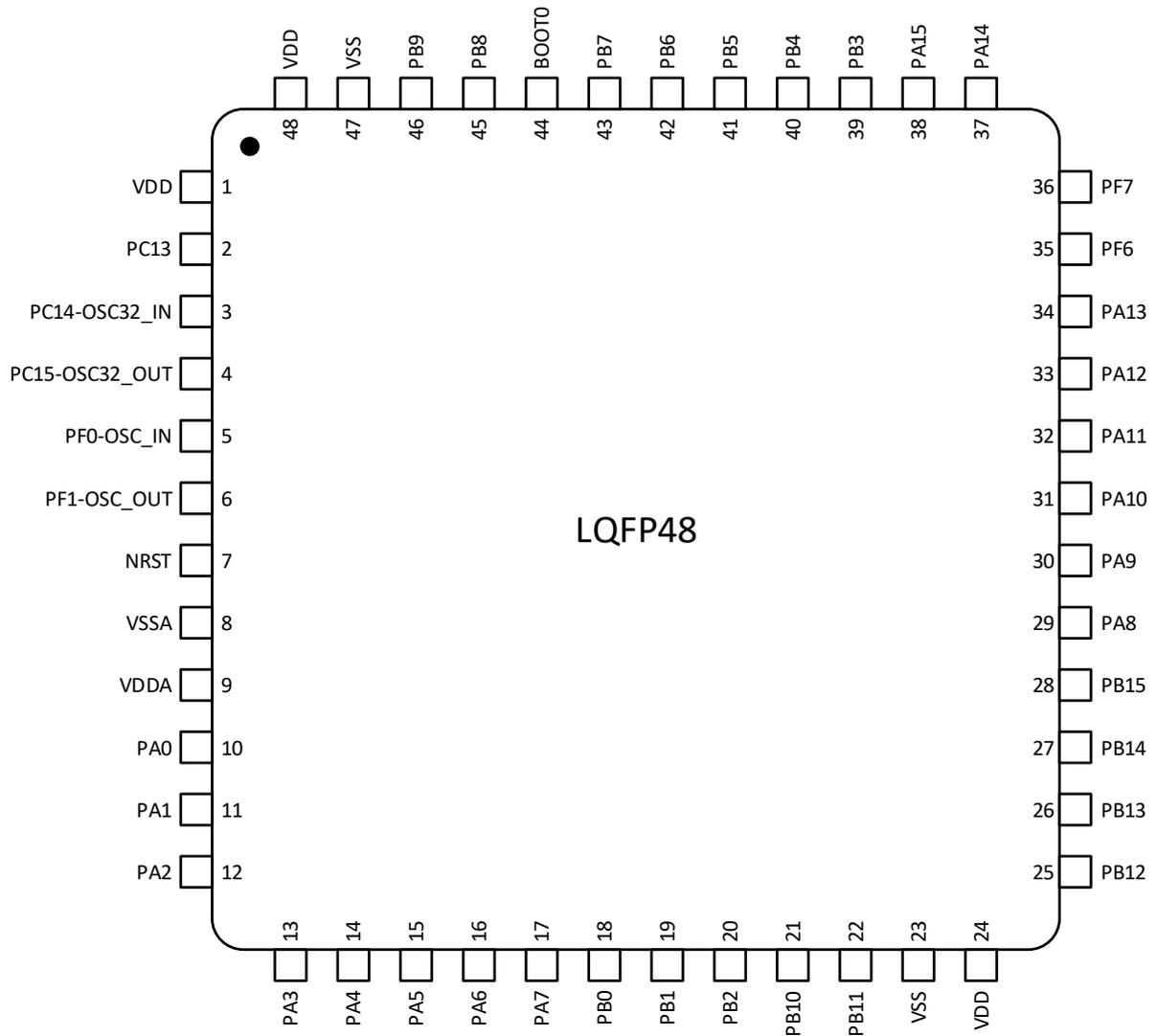
Table 2-2 N32G031 Series devices features and peripheral list (2)

Part Number		N32G031 F6U7	N32G031F 6S7	N32G031 K6Q7	N32G031 K6Q7-1	N32G031 K6L7
Flash capacity (KB)		32	32	32	32	32
SRAM capacity (KB)		8	8	8	8	8
CPU frequency		ARM Cortex-M0 @48MHz				
working environment		1.8~5.5V/-40~105°C				
Timer	General	1				
	Advanced	2				
	Basic	1				
	LPTIM	1				
	RTC	1				
communication interface	SPI	2				
	I2S	1				
	I2C	2				
	USART	2				
	LPUART	1				
GPIO		16		28		26
DMA Number of Channels		5				
12bit ADC Number of channels		1x12bit 7Channel	1x12bit 9Channel	1x12bit 10Channel		
OPA/COMP		1/1				
Beeper		1				
Algorithm support		CRC16/CRC32				
security protection		Read and write protection (RDP/WRP), storage encryption				
Package		General	TSSOP20	QFN32 (5mmx5m m)	QFN32 (4mmx4m m)	LQFP32

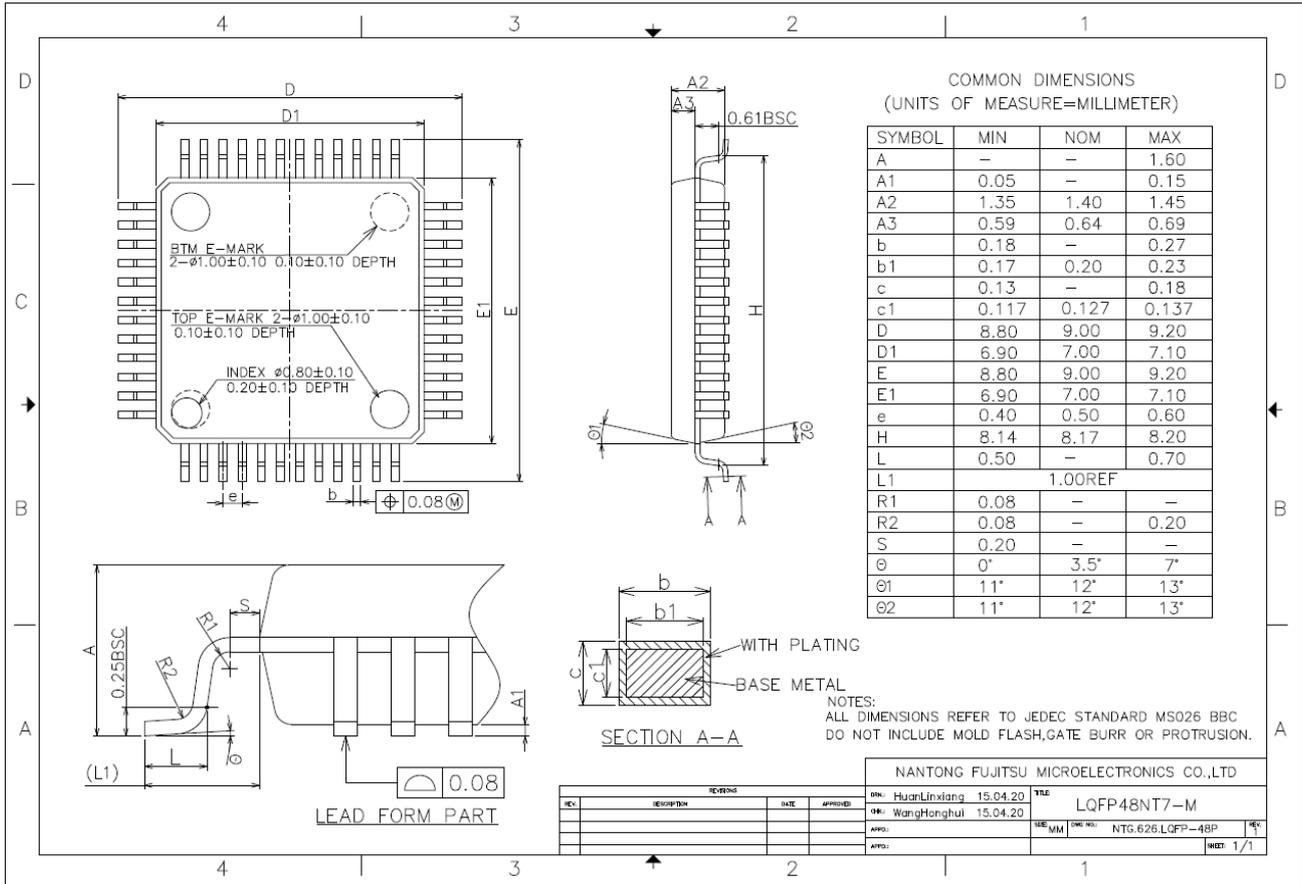
### 3 Package information

#### 3.1 LQFP48

##### 3.1.1 LQFP48 pinouts

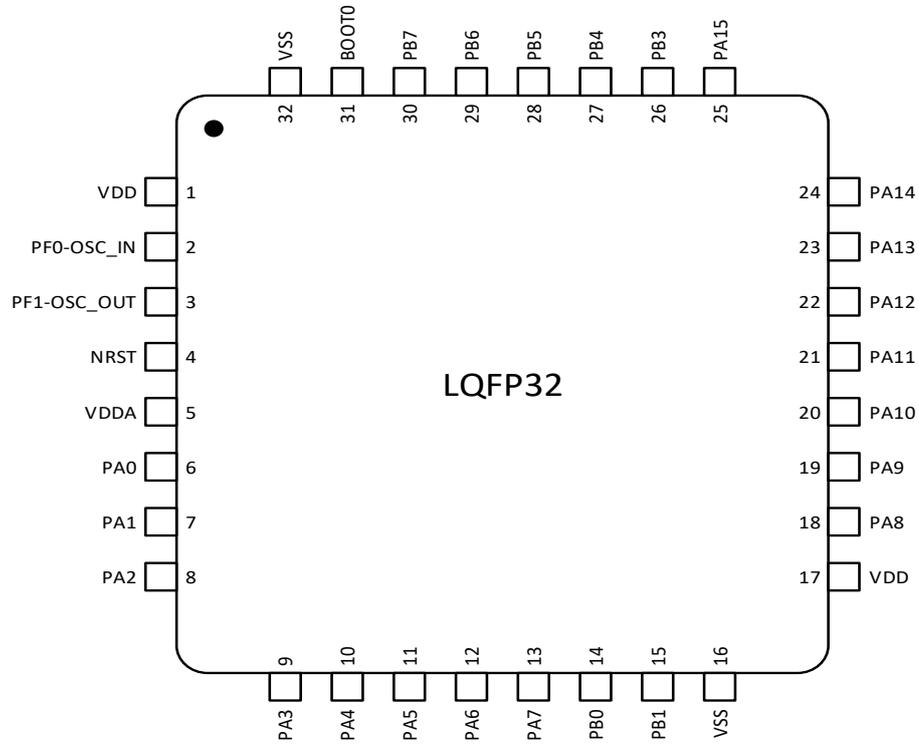


### 3.1.2 LQFP48 package

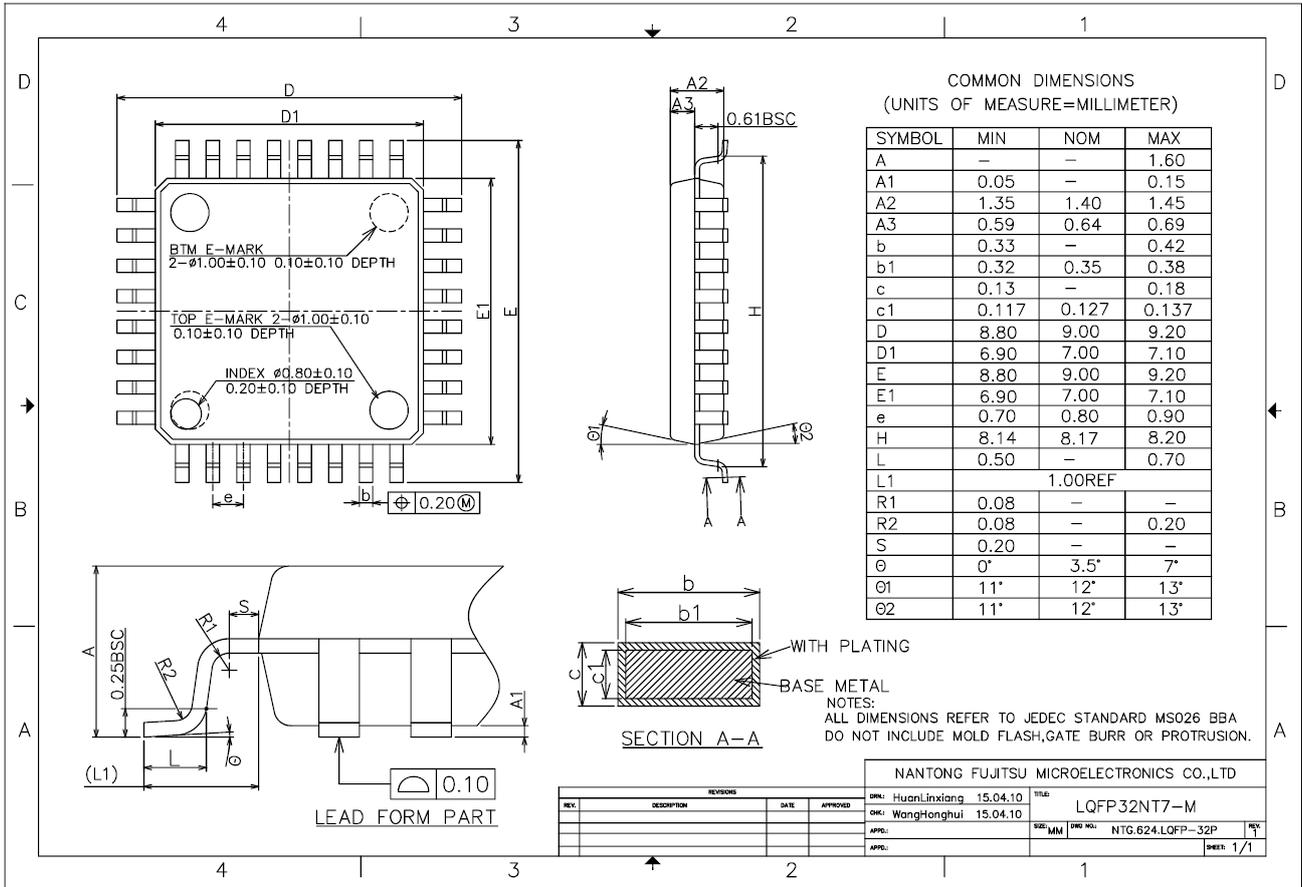


## 3.2 LQFP32

### 3.2.1 LQFP32 pinouts

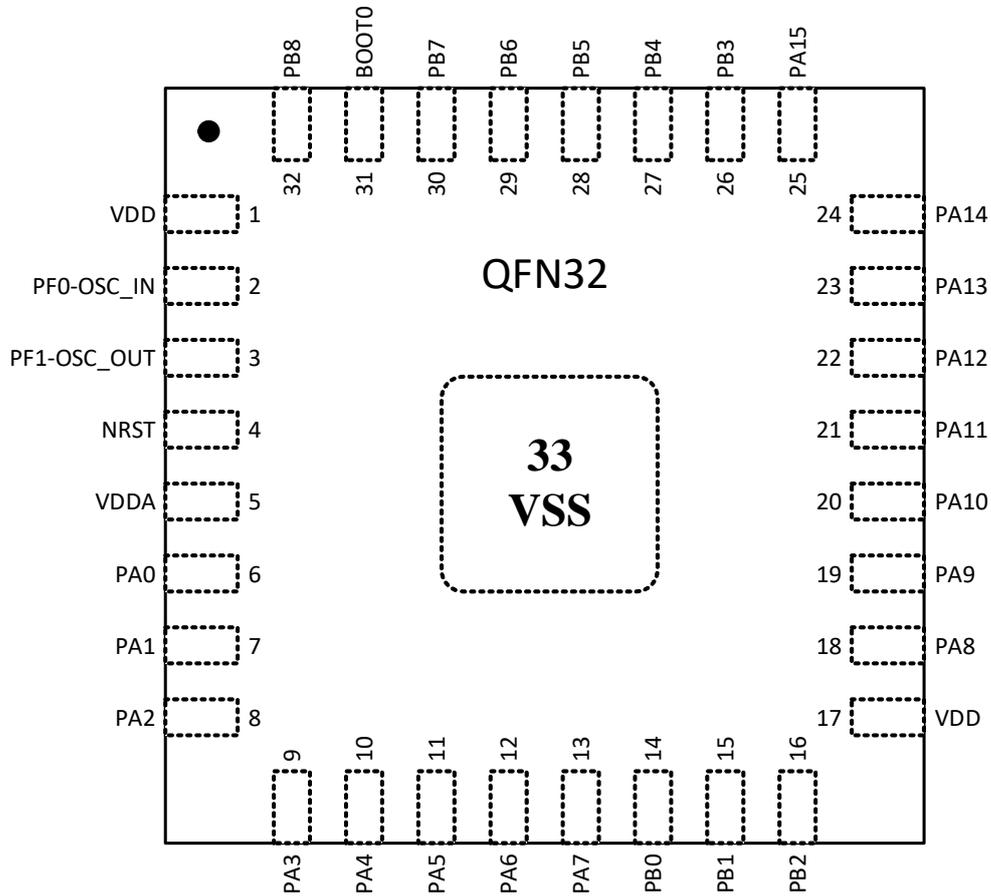


### 3.2.2 LQFP32 package

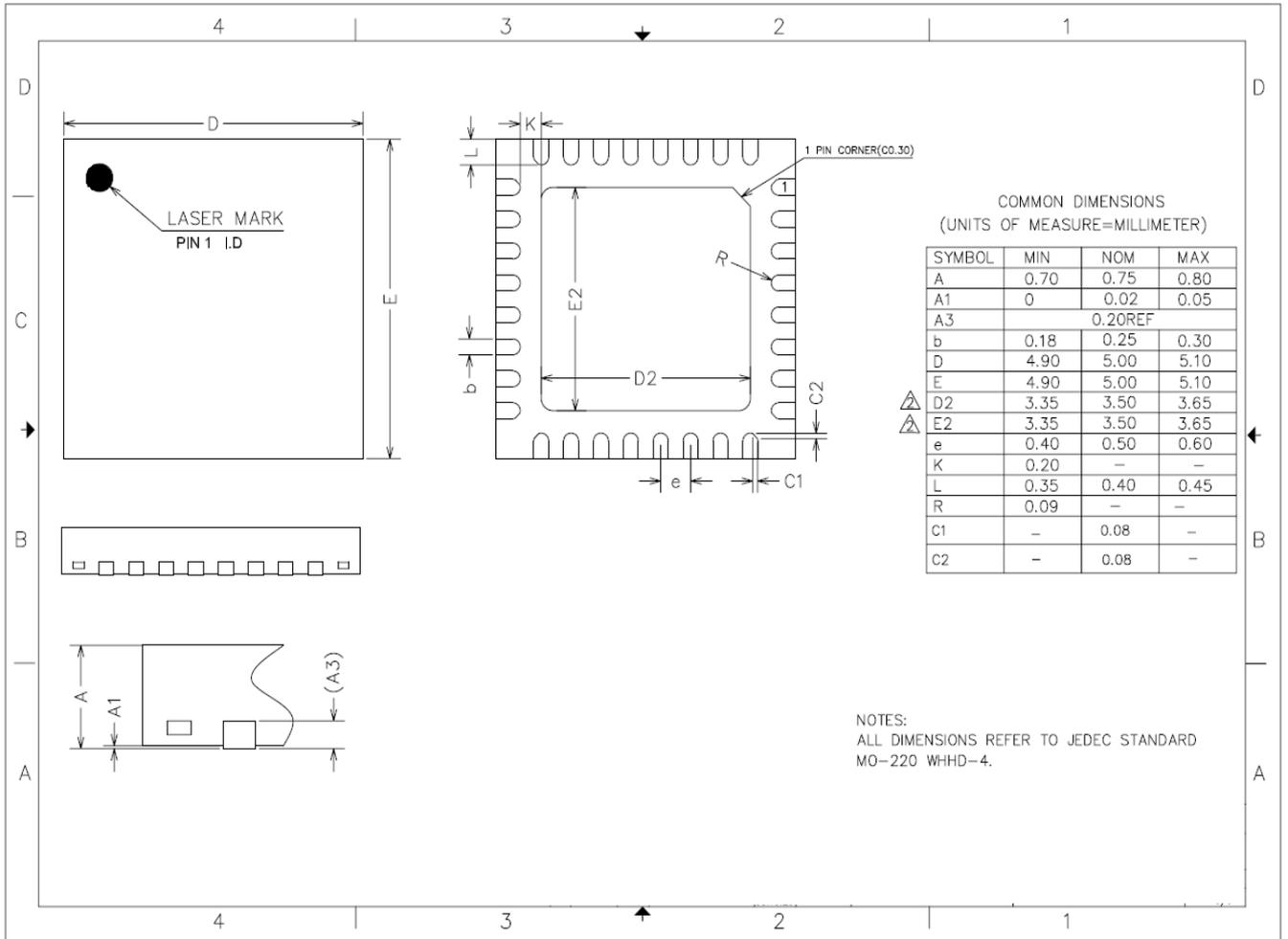


### 3.3 QFN32

#### 3.3.1 QFN32 (5mmx5mm) pinouts

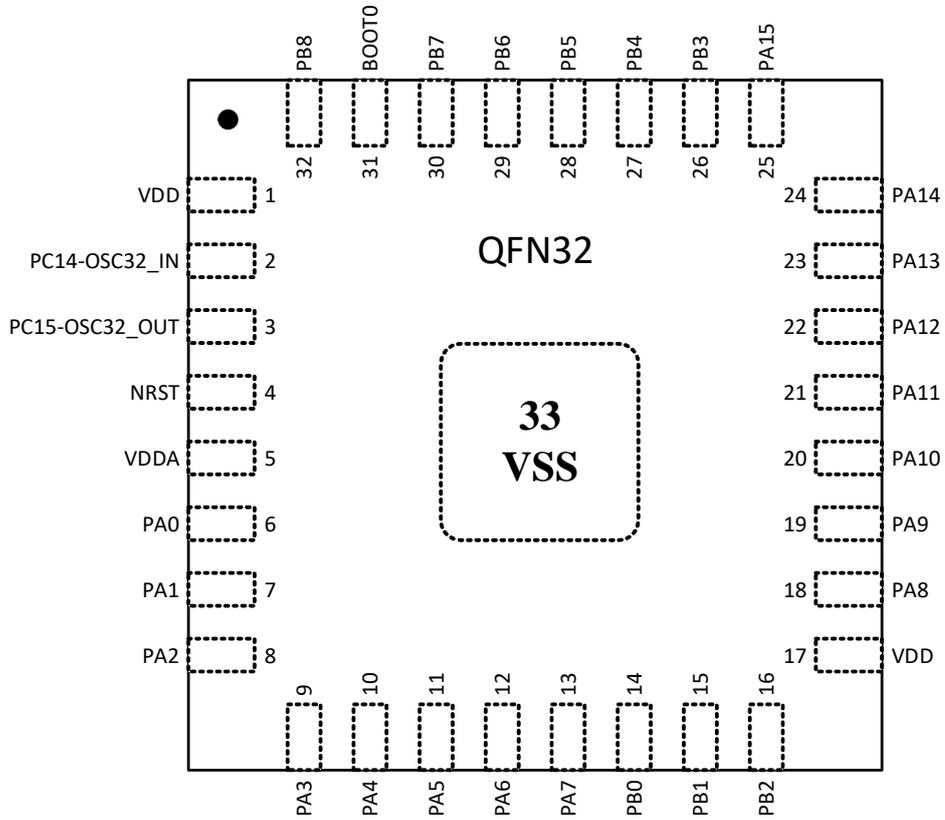


### 3.3.2 QFN32 (5mmx5mm) package

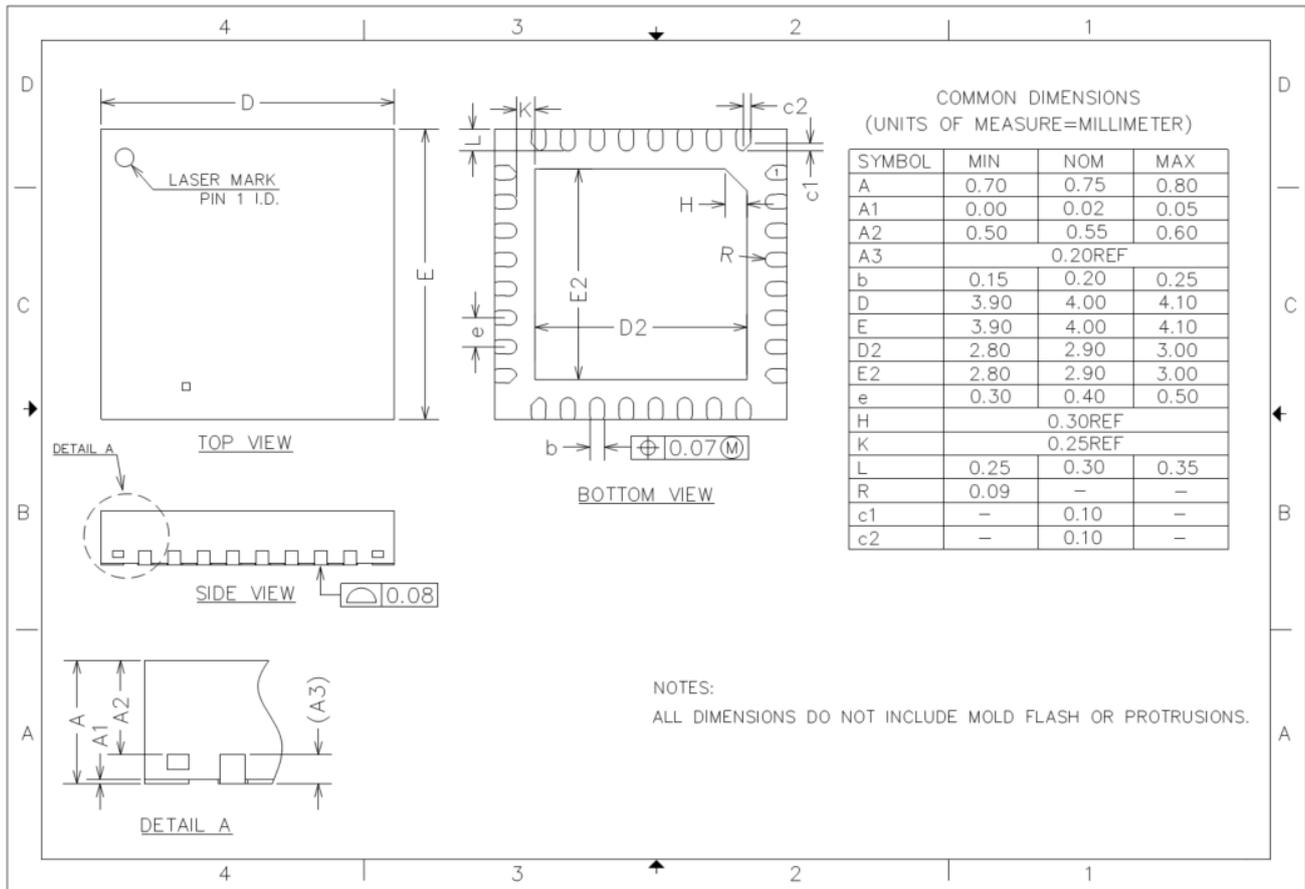


### 3.4 QFN32

#### 3.4.1 QFN32 (4mmx4mm) pinouts

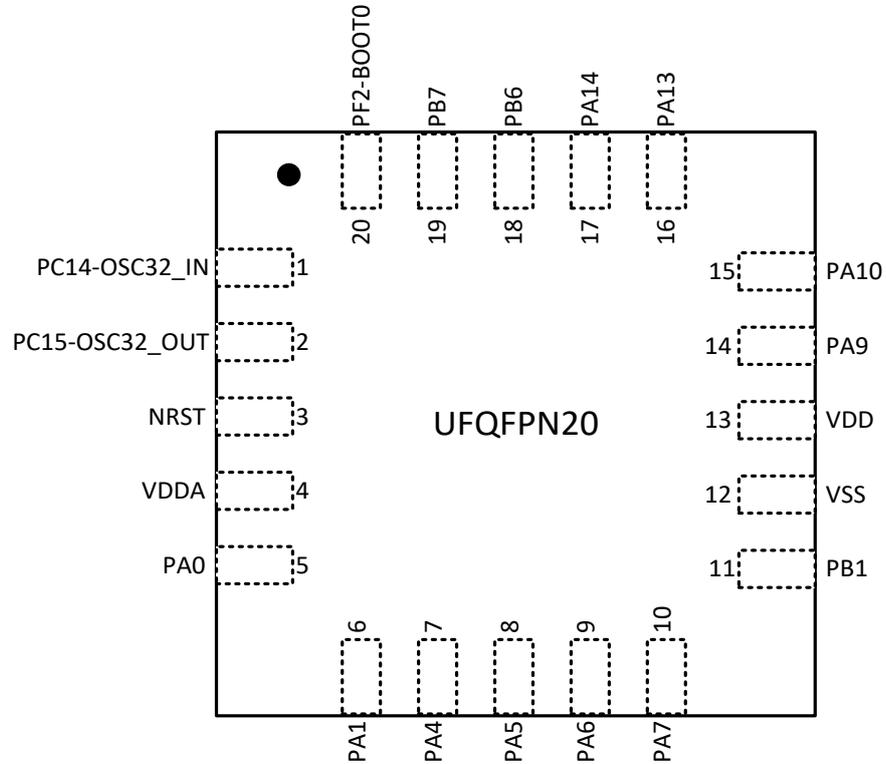


### 3.4.2 QFN32 (4mmx4mm) package

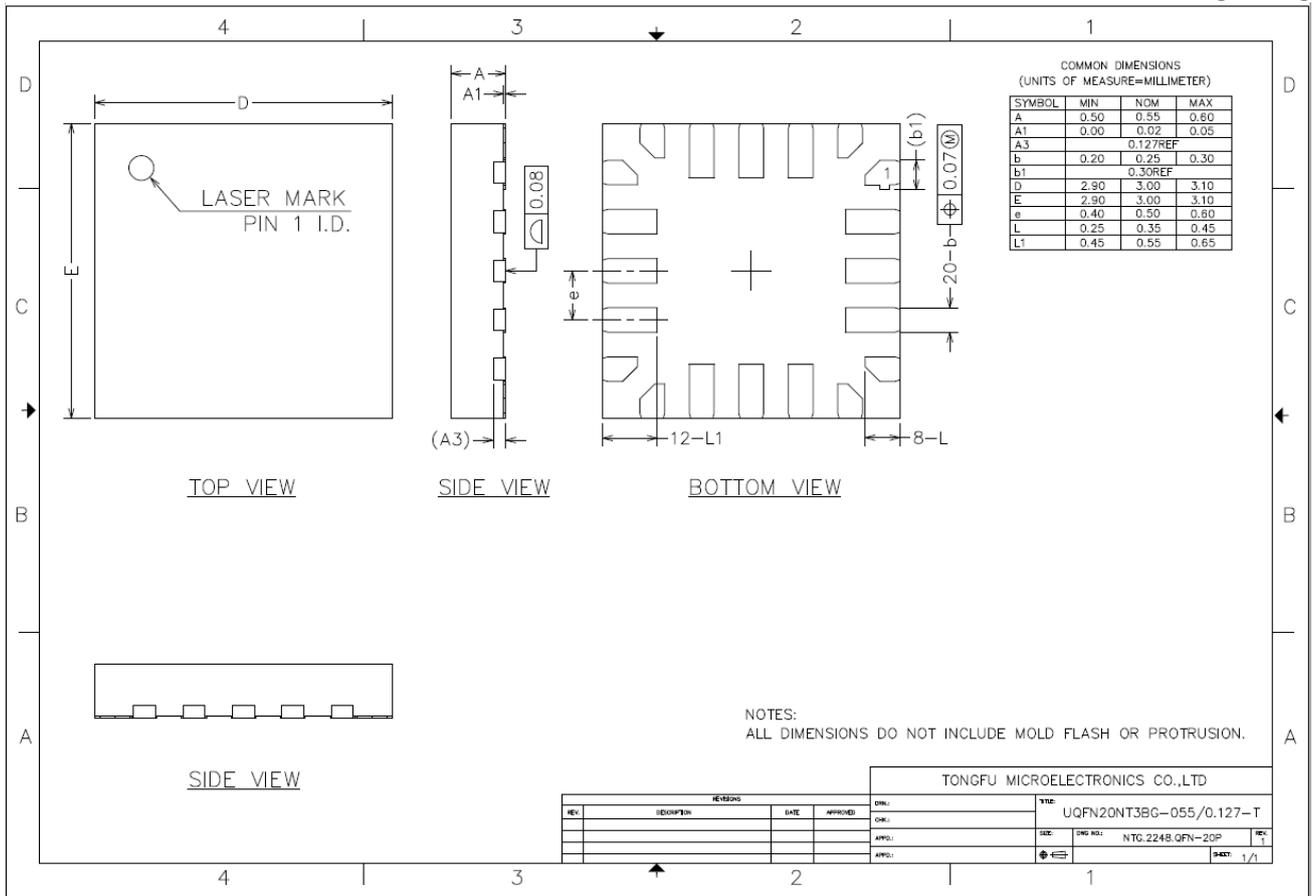


### 3.5 UFQFPN20

#### 3.5.1 UFQFPN20 pinouts

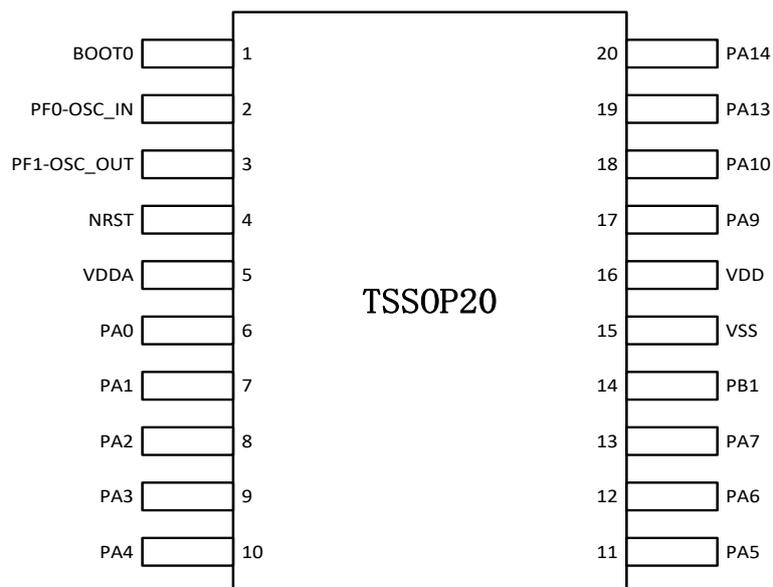


#### 3.5.2 UFQFPN20 package

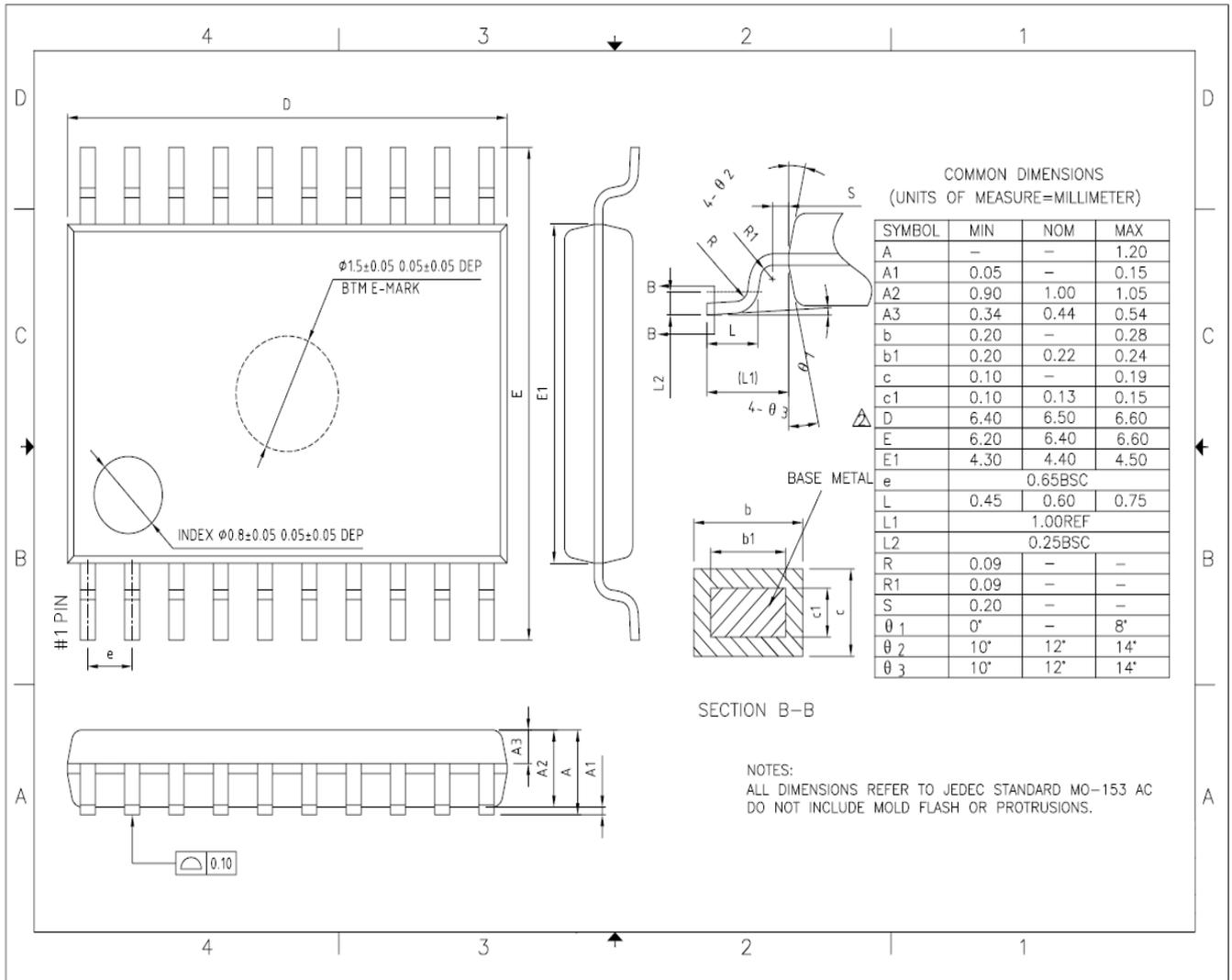


## 3.6 TSSOP20

### 3.6.1 TSSOP20 pinouts



### 3.6.2 TSSOP20 package



## 4 Revision History

<b>Version</b>	<b>Date</b>	<b>Note</b>
V1.0.0	2021.9.15	1. Initial document
V1.0.1	2022.1.13	1. Modify the size of Retention SRAM to 8Kbyte
V1.1	2022.7.5	1. Modify MCO to 2-way output in key feature 2. Delete TQFP48 3. Delete reel in part number information
V1.2	2022.9.13	1. Key feature, delete programmable low level detection and reset
V1.3.0	2023.7.31	1. Section 3.4.2. Modify package dimension of QFN32(4mmx4mm) in the package
V1.4.0	2024.7.24	1. Modify package dimension of LQFP48\LQFP32\UFQFPN20 in the package

## 5 Notice

This document is the exclusive property of NSING TECHNOLOGIES PTE. LTD. (Hereinafter referred to as NSING). This document, and the product of NSING described herein (Hereinafter referred to as the Product) are owned by NSING under the laws and treaties of Republic of Singapore and other applicable jurisdictions worldwide. The intellectual properties of the product belong to NSING Technologies Inc. and NSING Technologies Inc. does not grant any third party any license under its patents, copyrights, trademarks, or other intellectual property rights. Names and brands of third party may be mentioned or referred thereto (if any) for identification purposes only. NSING reserves the right to make changes, corrections, enhancements, modifications, and improvements to this document at any time without notice. Please contact NSING and obtain the latest version of this document before placing orders. Although NSING has attempted to provide accurate and reliable information, NSING assumes no responsibility for the accuracy and reliability of this document. It is the responsibility of the user of this document to properly design, program, and test the functionality and safety of any application made of this information and any resulting product. In no event shall NSING be liable for any direct, indirect, incidental, special, exemplary, or consequential damages arising in any way out of the use of this document or the Product. NSING Products are neither intended nor warranted for usage in systems or equipment, any malfunction or failure of which may cause loss of human life, bodily injury or severe property damage. Such applications are deemed, Insecure Usage'. Insecure usage includes, but is not limited to: equipment for surgical implementation, atomic energy control instruments, airplane or spaceship instruments, all types of safety devices, and other applications intended to supporter sustain life. All Insecure Usage shall be made at user's risk. User shall indemnify NSING and hold NSING harmless from and against all claims, costs, damages, and other liabilities, arising from or related to any customer's Insecure Usage Any express or implied warranty with regard to this document or the Product, including, but not limited to. The warranties of merchantability, fitness for a particular purpose and non-infringement are disclaimed to the fullest extent permitted by law. Unless otherwise explicitly permitted by NSING, anyone may not use, duplicate, modify, transcribe or otherwise distribute this document for any purposes, in whole or in part.