N32G031x6/x8 Product Brief

The N32G031 series adopts a 32-bit Cortex®-M0 core, operating frequency up to 48MHz. The devices integrate up to 64KB embedded flash, 8KBSRAM, multiple communication bus interfaces like U(S)ART, I²C, SPI, and analog interfaces such as 1x12bit 1Msps ADC, 1xOPAMP and 1xCOMP.

Key Features

- CPU core
  - A 32-bit general-purpose microcontroller based on the Cortex®-M0 core, single-cycle hardware multiply instruction
  - Maximum frequency up to 48MHz
- Memories
  - Up to 64KByte of embedded Flash
    1. Supports encrypted storage function
    2. Supports hardware ECC check
    3. Supports 100,000 erase/write cycles, 10 years data retention
  - Up to 8KByte of embedded SRAM, supports hardware parity check
- Low power management
  - Stop mode: RTC Run, maximum 8Kbyte SRAM retention, CPU register retention, all IO retention
  - Power Down mode: supports 3 IO wakeup
- Clock
  - HSE: 4MHz~20MHz high-speed external crystal oscillator
  - LSE: 32.768KHz low-speed external crystal oscillator
  - HSI: high-speed internal RC 8MHz
  - LSI: low-speed internal RC 30KHz
  - Embedded high-speed PLL
  - Supports 2-channels clock output, configurable as system clock, HSI, HSE, LSI, LSE or PLL divisional output.
- Reset
  - Supports power-on/power-down/external pin reset
  - Supports watchdog reset
- Communication interfaces
  - 3x U(S)ART interfaces with maximum rate up to 3 Mbps

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1. 2x USART interfaces (support 1xISO7816, 1xIrDA, LIN)
2. 1x LPUART interface (supports low power mode, the maximum rate up to 9600bps in this mode, can wake up chip from STOP mode)

- 2x SPI interfaces with speed up to 18MHz, one of which supports multiplexing with I^2S
- 2x I^2C interfaces with speed up to 1 MHz, which can be configured in master/slave mode and support dual address response in slave mode

- Analog Interfaces
  - 1x 12-bit 1Msps ADC, up to 12 external single-ended input channels
  - 1x OPAMP, operational amplifier with built-in up to 32 times programmable gain amplifier(PGA)
  - 1x COMP, the high-speed analog comparator has an embedded 64-level adjustable reference
- GPIOs
  - Up to 40 GPIOs
  - Support multiplexed functions
- DMA controller
  - 1x high-speed DMA controllers
  - Each controller supports 5 channels
  - Channel source address and destination address can be configured arbitrarily
- RTC real-time clock
  - Supports leap-year calendar, alarm events, periodic wakeup, supports internal and external clock calibration.
- Beeper
  - 1x Beeper, supports complementary output, 16mA output drive capacity
- Timers
  - 2x 16-bit advanced timers
    1. Supports input capture, complementary output, orthogonal encoding input etc
    2. Each timer has 4 independent channels, 3 of which support 6-channel complementary PWM output
  - 1x 16-bit general-purpose timer
    1. Supports input capture/output compare/PWM output
    2. Each timer has 4 independent channels
  - 1x 16-bit basic timer

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- 1x 16-bit low power timer
- 1x 24-bit SysTick timer
- 1x 7-bit Window Watchdog (WWDG)
- 1x 12-bit Independent Watchdog (IWDG)

- Programming methods
  - Supports SWD debugging interface
  - Supports UART Bootloader
- Hardware Divider(HDIV) And Square Root(SQRT)
- Security features
  - Flash storage encryption
  - CRC16/32 computation
  - Supports write protection(WRP), multiple levels of read protection(RDP) (L0/L1/L2)
  - Supports external clock failure detection, anti-tamper detection
- 96-bit UID and 128-bit UCID
- Operating conditions
  - Operating voltage range: 1.8V~5.5V
  - Operating temperature range: -40°C~105°C
  - ESD: ±4KV (HBM model), ±1KV (CDM model)
- Packages
  - UFQFPN20(3mm x 3mm)
  - TSSOP20(6.5mm x 4.4mm)
  - QFN32(4mm x 4mm)
  - QFN32(5mm x 5mm)
  - LQFP32(7mm x 7mm)
  - LQFP48(7mm x 7mm)
- Ordering information

Reference	Part Number
N32G031x6 N32G031x8	N32G031F6U7, N32G031F6S7, N32G031K6L7, N32G031K6Q7, N32G031K6Q7-1, N32G031F8U7, N32G031F8S7, N32G031K8L7, N32G031K8Q7, N32G031K8Q7-1, N32G031C8L7

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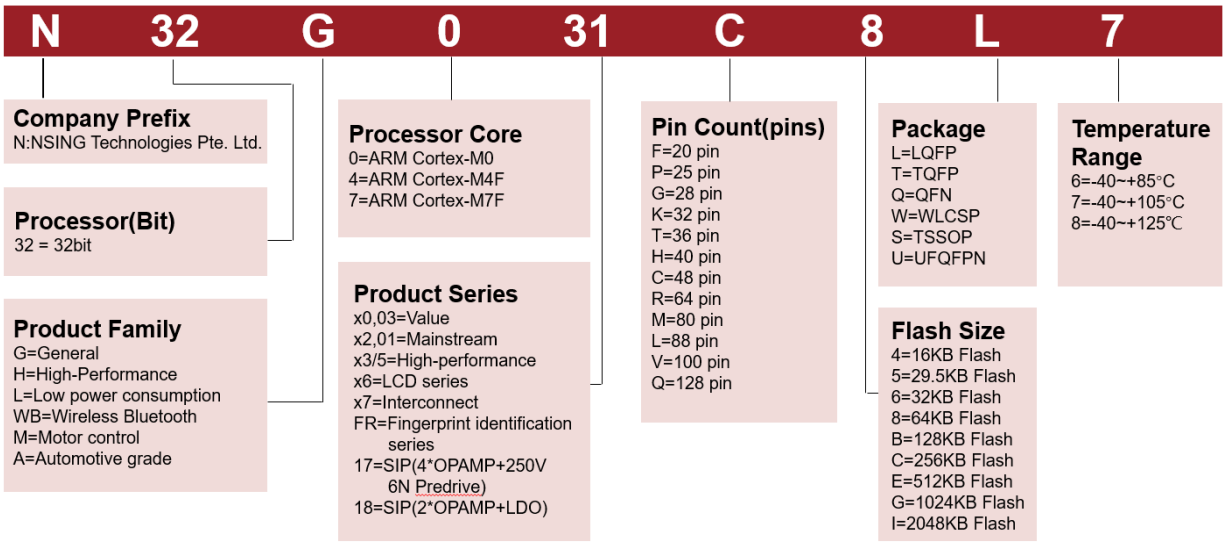
1 Naming Convention

Figure 1-1 N32G031 Series Part Number Information



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2 Product Configurations

Table 2-1 N32G031 Series Devices Features and Peripheral List(1)

Device		N32G031 F8U7	N32G031 F8S7	N32G031 K8Q7	N32G031 K8Q7-1	N32G031 K8L7	N32G031 C8L7
Flash capacity (KB)		32	32	32	32	32	64
SRAM capacity (KB)		8	8	8	8	8	8
CPU frequency		ARM Cortex-M0 @48MHz					
Operating conditions		1.8~5.5V/-40~105 ℃					
Timers	General	1					
	Advanced	2					
	Basic	1					
	LPTIM	1					
	RTC	1					
Communication interfaces	SPI	2					
	I^2S	1					
	I^2C	2					
	USART	2					
	LPUART	1					
GPIO		16		28		26	40
DMA		1					
DMA channels DMA channels		5 Channels					
12bit ADC number of channels		1x12bit 7Channel	1x12bit 9Channel	1x12bit 10Channel			1x12bit 12Channe l
OPA/COMP		1/1					
Beeper		1					
Algorithm support		CRC16/CRC32					
Security protection		Read and write protection (RDP/WRP), storage encryption					
Package		UFQFPN20	TSSOP20	QFN32(1)	QFN32(2)	LQFP32	LQFP48

Notes:

(1) QFN32(5mm x 5mm)

(2) QFN32(4mm x 4mm)

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Table 2-1 N32G031 Series Devices Features and Peripheral List(2)

Device		N32G031F6U7	N32G031F6S7	N32G031K6Q7	N32G031K6Q7-1	N32G031K6L7
Flash capacity (KB)		32	32	32	32	32
SRAM capacity (KB)		8	8	8	8	8
CPU frequency		ARM Cortex-M0 @48MHz				
Operating environment		1.8~5.5V/-40~105℃				
Timers	General	1				
	Advanced	2				
	Basic	1				
	LPTIM	1				
	RTC	1				
Communication interfaces	SPI	2				
	I^2S	1				
	I^2C	2				
	USART	2				
	LPUART	1				
GPIO		16		28		26
DMA		1				
DMA channels		5 Channels				
12bit ADC number of channels		1x12bit 7Channel	1x12bit 9Channel	1x12bit 10Channel		
OPA/COMP		1/1				
Beeper		1				
Algorithm support		CRC16/CRC32				
Security protection		Read and write protection (RDP/WRP), storage encryption				
Package		General	TSSOP20	QFN32[(1)]	QFN32[(2)]	LQFP32

Notes:

[(1)] QFN32(5mm x 5mm)

[(2)] QFN32(4mm x 4mm)

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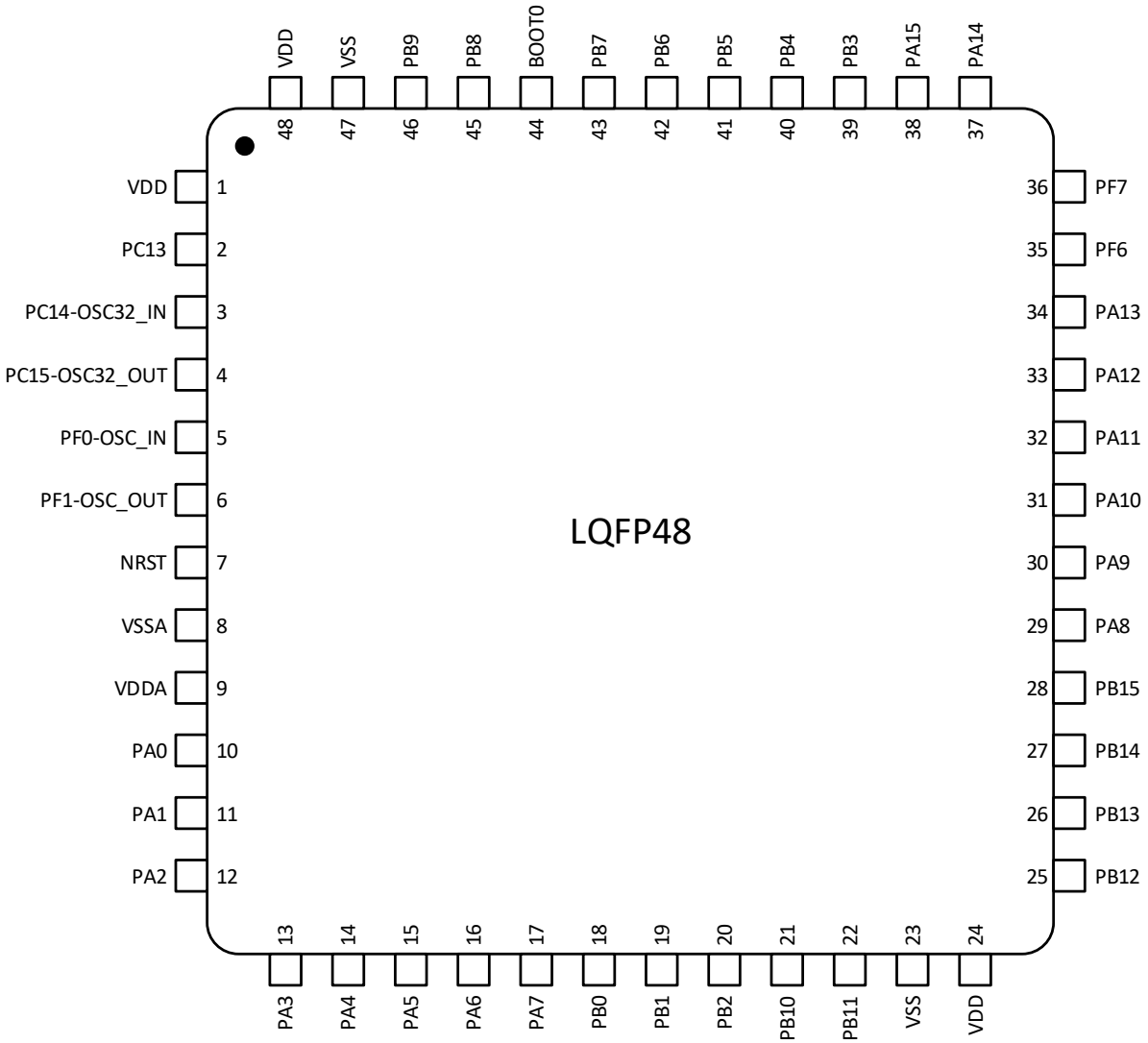
3 Packages

3.1 LQFP48 Package

3.1.1 LQFP48 Pin Assignment



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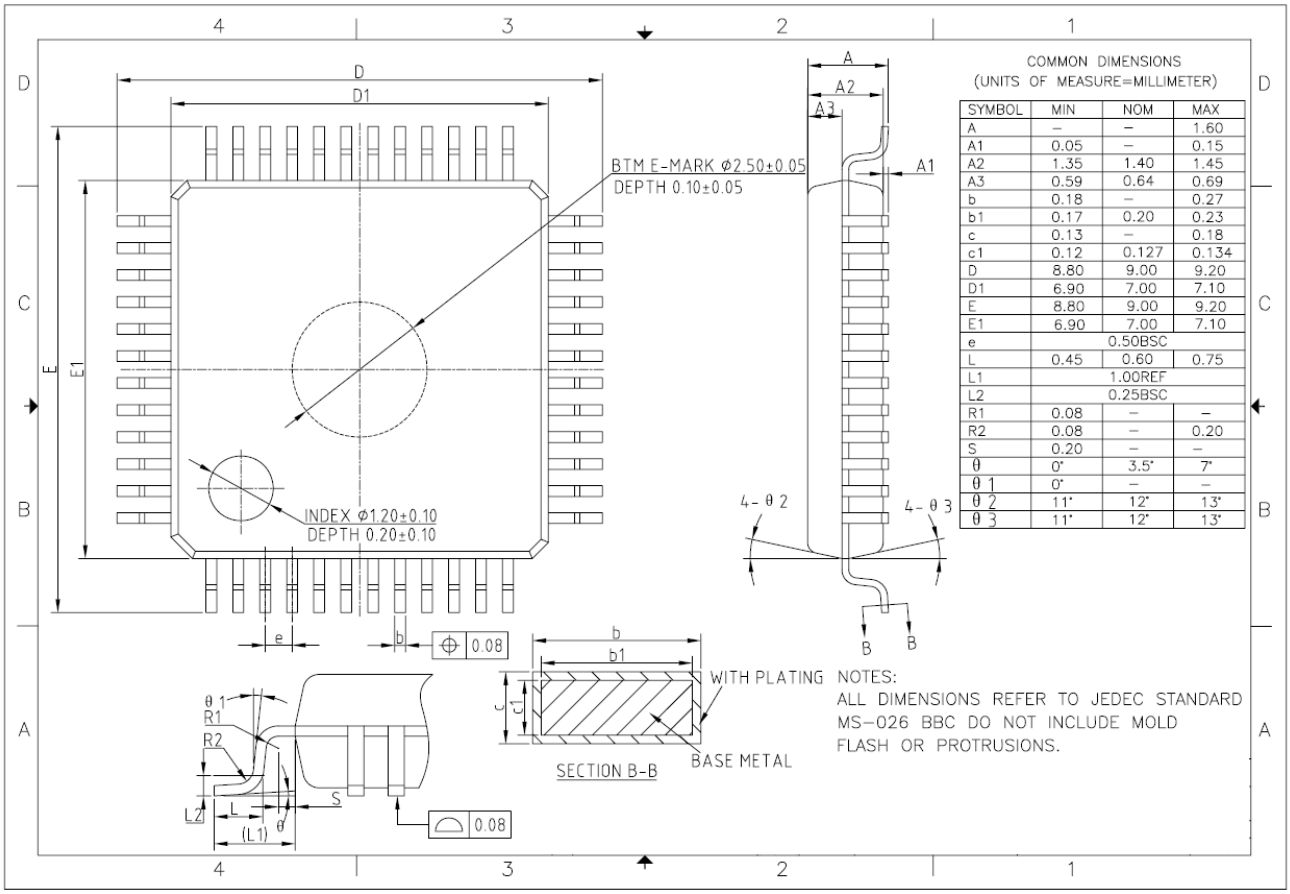
3.1.2 LQFP48(7mm x 7mm) Package Dimensions



SYMBOL	MIN	NOM	MAX
A	–	–	1.60
A1	0.05	–	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	–	0.27
b1	0.17	0.20	0.23
c	0.13	–	0.18
c1	0.12	0.127	0.134
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
e		0.50BSC	
L	0.45	0.60	0.75
L1		1.00REF	
L2		0.25BSC	
R1	0.08	–	–
R2	0.08	–	0.20
S	0.20	–	–
θ	0°	3.5°	7°
θ1	0°	–	–
θ2	11°	12°	13°
θ3	11°	12°	13°

NOTES:
ALL DIMENSIONS REFER TO JEDEC STANDARD MS-026 BBC DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.

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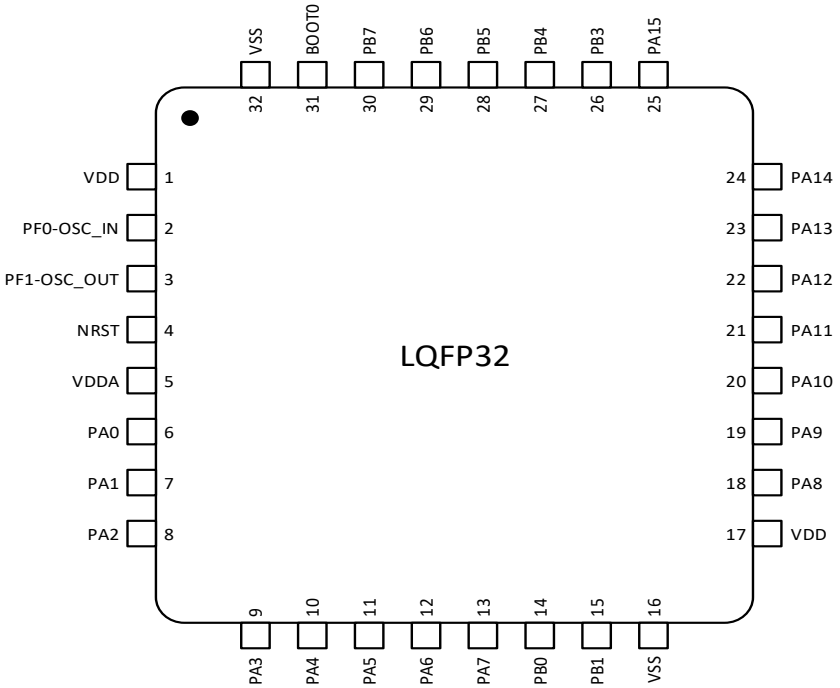
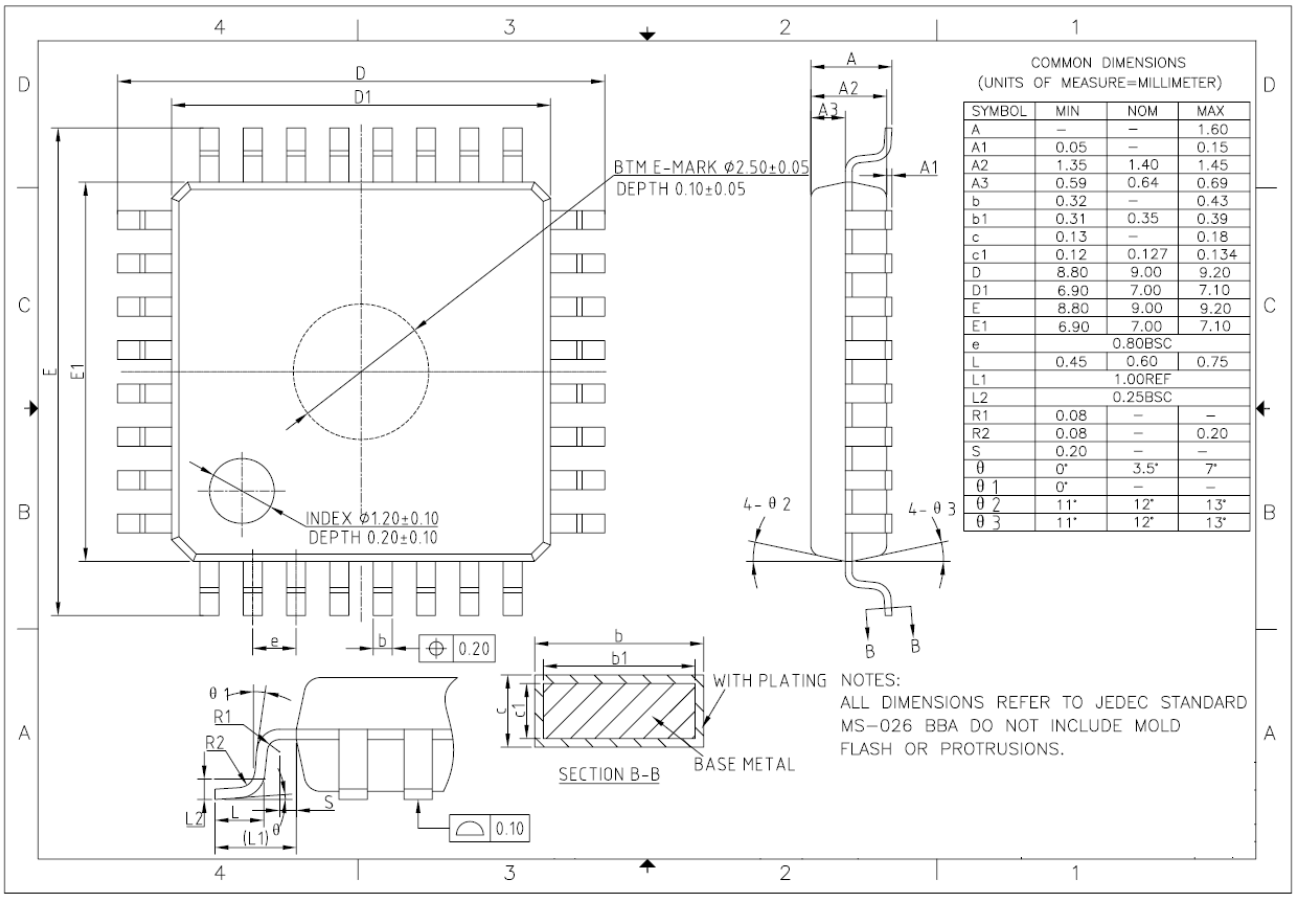
3.2 LQFP32 Package

3.2.1 LQFP32 Pin Assignment



3.2.2 LQFP32(7mm x 7mm) Package Dimensions



SYMBOL	MIN	NOM	MAX
A	–	–	1.60
A1	0.05	–	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.32	–	0.43
b1	0.31	0.35	0.39
c	0.13	–	0.18
c1	0.12	0.127	0.134
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
e	0.80BSC		
L	0.45	0.60	0.75
L1	1.00REF		
L2	0.25BSC		
R1	0.08	–	–
R2	0.08	–	0.20
S	0.20	–	–
θ	0°	3.5°	7°
θ1	0°	–	–
θ2	11°	12°	13°
θ3	11°	12°	13°

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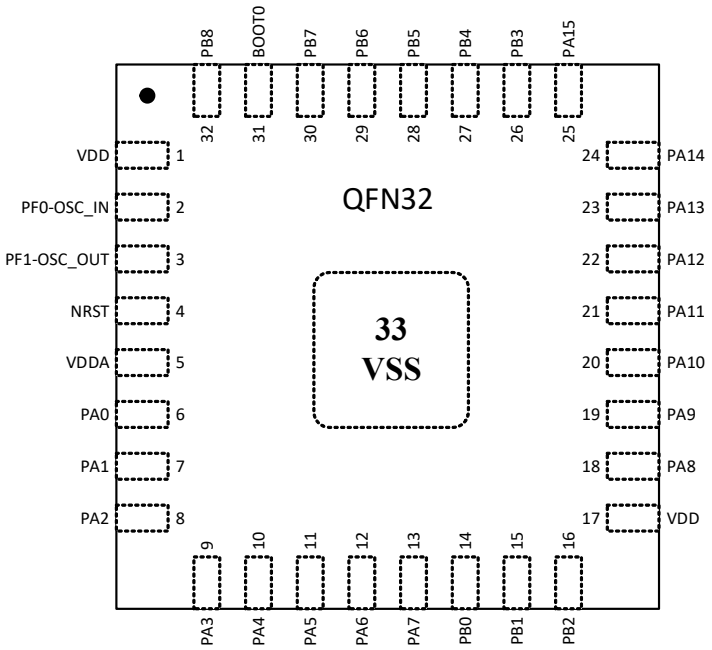
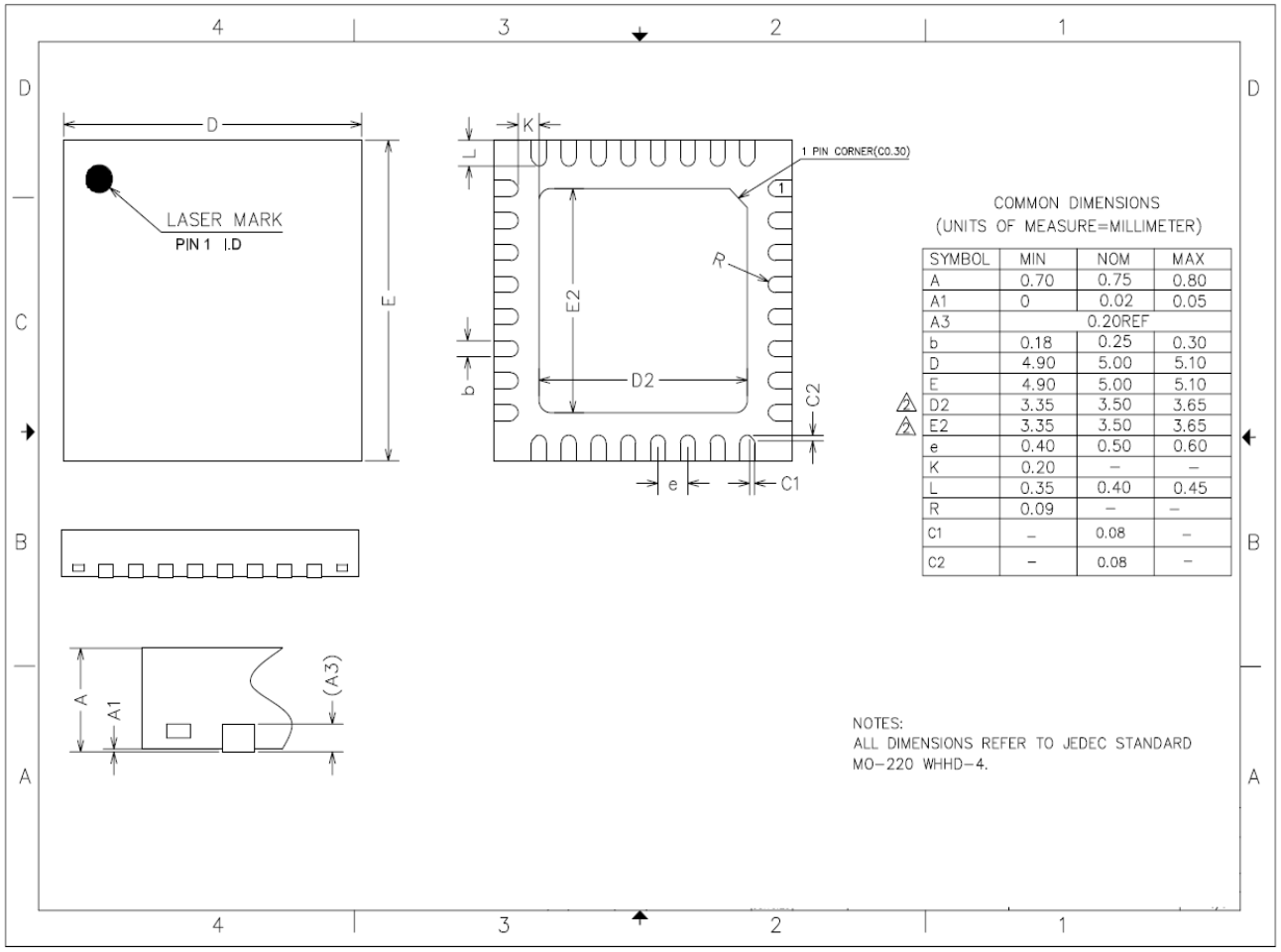
3.3 QFN32 Package

3.3.1 QFN32(5mm x 5mm) Pin Assignment



3.3.2 QFN32(5mm x 5mm) Package Dimensions



SYMBOL	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0	0.02	0.05
A3		0.20REF	
b	0.18	0.25	0.30
D	4.90	5.00	5.10
E	4.90	5.00	5.10
D2	3.35	3.50	3.65
E2	3.35	3.50	3.65
e	0.40	0.50	0.60
K	0.20	–	–
L	0.35	0.40	0.45
R	0.09	–	–
C1	–	0.08	–
C2	–	0.08	–

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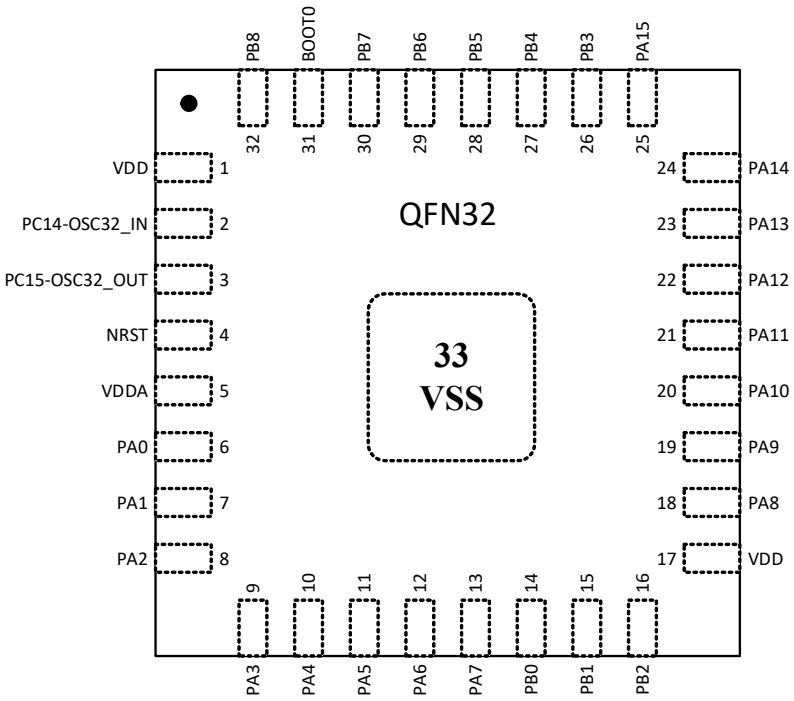
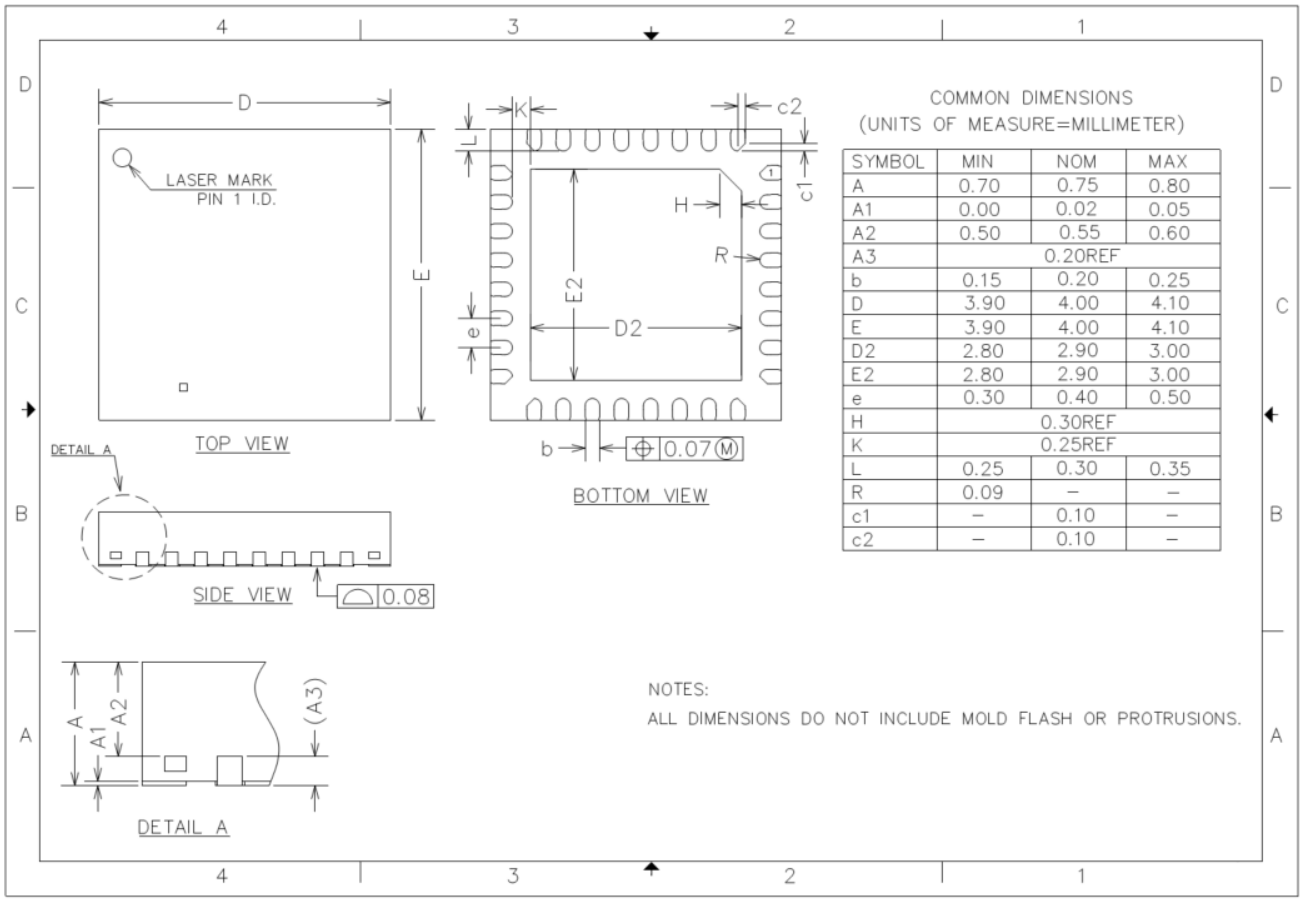
3.4 QFN32 Package

3.4.1 QFN32(4mm x 4mm) Pin Assignment



3.4.2 QFN32(4mm x 4mm) Package Dimensions



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A2	0.50	0.55	0.60
A3		0.20REF	
b	0.15	0.20	0.25
D	3.90	4.00	4.10
E	3.90	4.00	4.10
D2	2.80	2.90	3.00
E2	2.80	2.90	3.00
e	0.30	0.40	0.50
H		0.30REF	
K		0.25REF	
L	0.25	0.30	0.35
R	0.09	–	–
c1	–	0.10	–
c2	–	0.10	–

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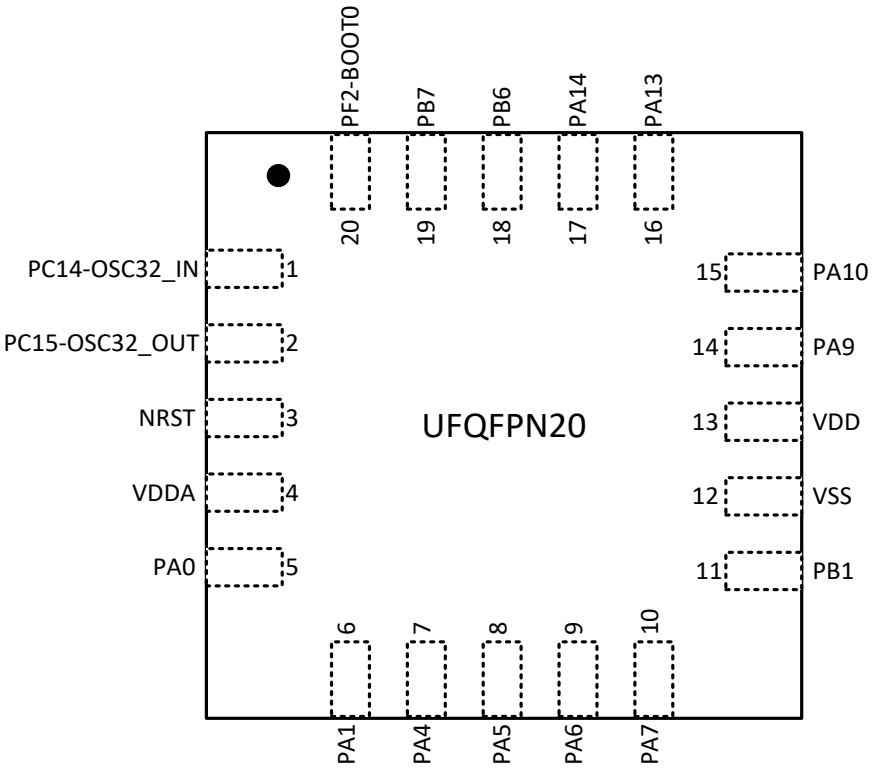
3.5 UFQFPN20 Package

3.5.1 UFQFPN20 Pin Assignment



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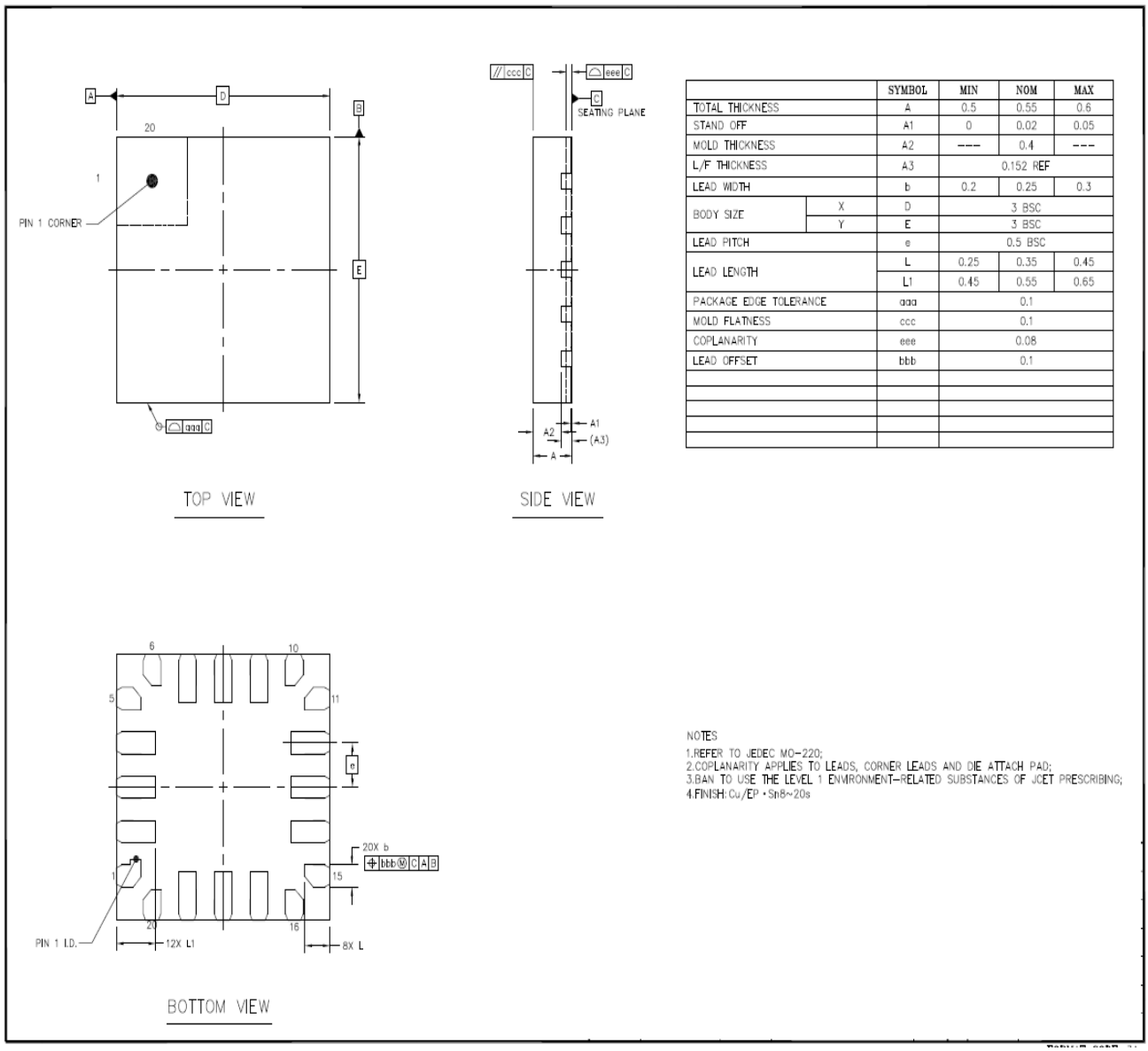
3.5.2 UFQFPN20(3mm x 3mm) Package Dimensions



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.5	0.55	0.6
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2	---	0.4	---
L/F THICKNESS		A3		0.152 REF	
LEAD WIDTH		b	0.2	0.25	0.3
BODY SIZE	X	D		3 BSC	
	Y	E		3 BSC	
LEAD PITCH		e		0.5 BSC	
LEAD LENGTH		L	0.25	0.35	0.45
		L1	0.45	0.55	0.65
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		ccc		0.1	
COPLANARITY		eee		0.08	
LEAD OFFSET		bbb		0.1	

NOTES
1.REFER TO JEDEC MO-220;
2.COPLANARITY APPLIES TO LEADS, CORNER LEADS AND DIE ATTACH PAD;
3.BAN TO USE THE LEVEL 1 ENVIRONMENT-RELATED SUBSTANCES OF JOET PRESCRIBING;
4.FINISH: Cu/EP • Sn8~20s

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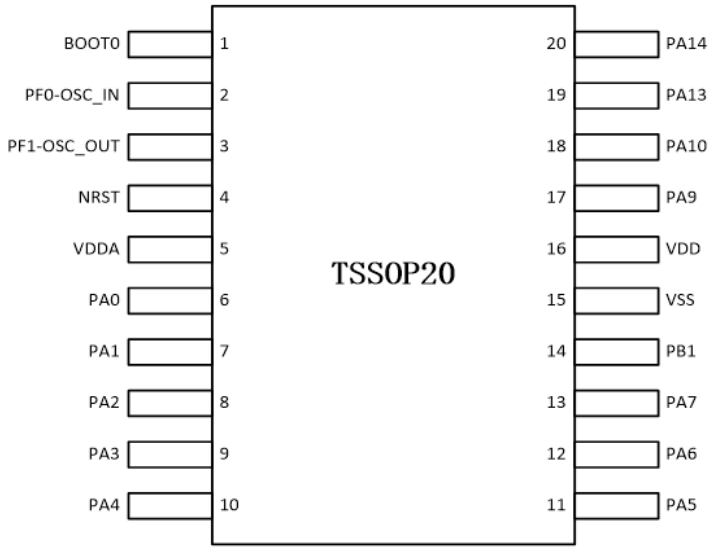
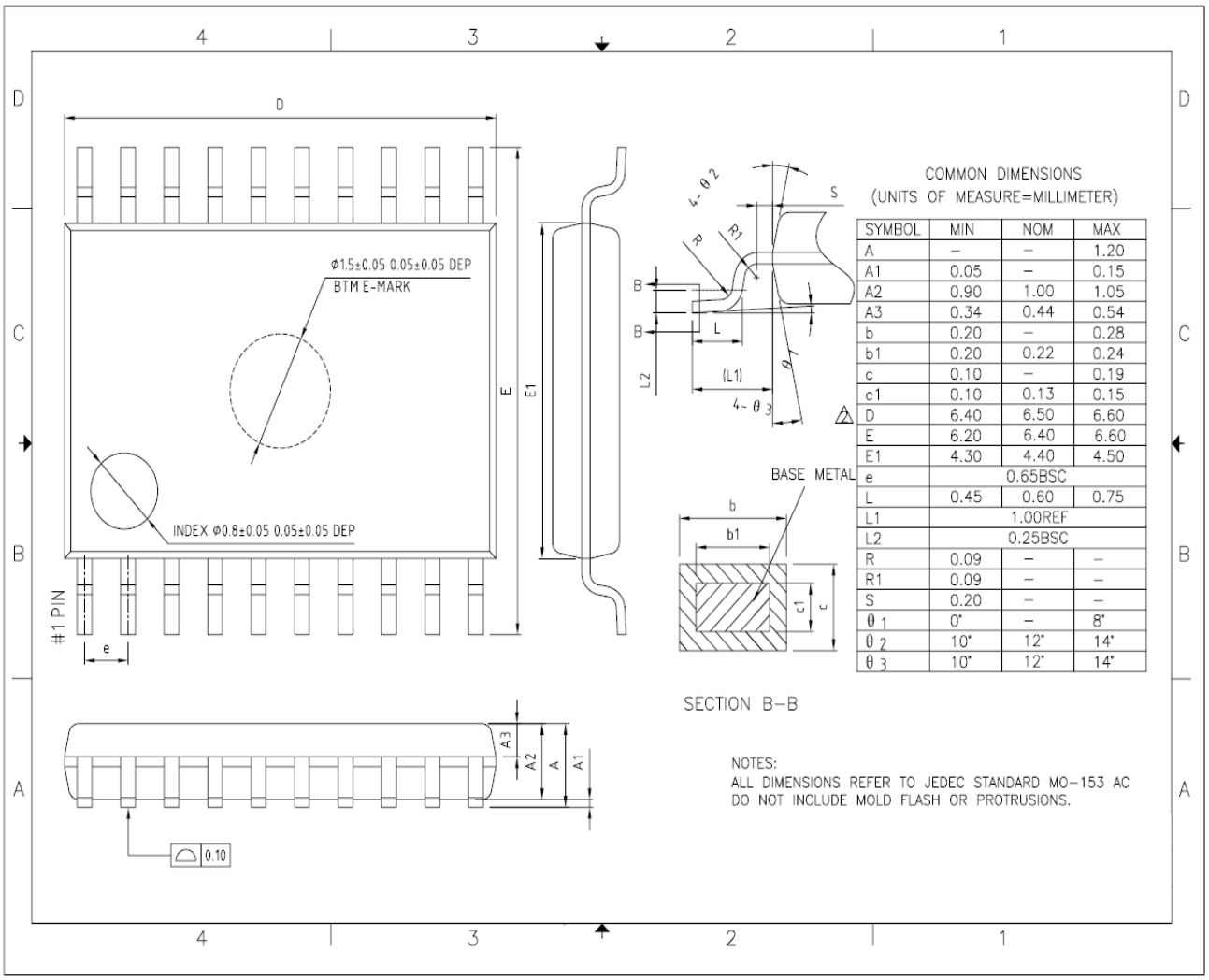
3.6 TSSOP20 Package

3.6.1 TSSOP20 Pin Assignment



3.6.2 TSSOP20(6.5mm x 4.4mm) Package Dimensions



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4 Version History

Version	Date	Changes
V1.0.0	2021.9.15	Initial release
V1.0.1	2022.1.13	Modified the size of Retention SRAM to 8Kbyte
V1.1	2022.7. 5	1) Modified MCO to 2-way output in key feature 2) Deleted TQFP48 3) Deleted reel in part number information
V1.2	2022.9.13	Key feature, deleted programmable low level detection and reset
V1.3.0	2023.7.31	Section 3.4.2. Modified package dimension of QFN32(4mmx4mm) in the package

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