N32G4FRxC/xE Product Brief

N32G4FR series uses 32-bit ARM® Cortex®-M4F core, operating frequency up to 144MHz, supporting floating-point unit and DSP instructions. The devices integrate up to 512KB of encrypted Flash and 144KB of SRAM, suitable for secure storage of fingerprint information. The series features rich of multi-channel U(S)ART, I2C, SPI, QSPI, USB, ADC, DAC, SDIO and other communication interfaces, allowing a built-in hardware acceleration engine for cryptographic algorithms. It also suitable for mainstream semiconductor fingerprint and optical fingerprint sensor.

Key Features

- **CPU Core**
  - 32-bit ARM® Cortex®-M4F core with FPU, supporting single-cycle multiplication and hardware division, DSP instructions and MPU
  - Built-in 8KB instruction Cache, supporting 0-wait-state execution from Flash memory
  - Frequency up to 144MHz with 180DMIPS
- **Memories**
  - Up to 512KByte of embedded Flash with ECC
  - Support encryption, multi-user partition and data protection
  - 100,000 erase/write cycles, and 10 years data retention
  - Up to 144Kbyte of SRAM (including 16KByte Retention RAM) with hardware parity check
- **Low Power Management**
  - STANDY mode: 3uA, 84 backup registers retained, all IOs retained, optional RTC Run, 16KByte Retention SRAM retained, supports VBAT pin independent power supply, 100us fast wake-up
  - STOP2 mode: 5uA, RTC Run, 16KByte Retention SRAM retained, CPU register retained, all IO retained, supports 40us fast wake-up
  - STOP0 mode: 120uA, RTC Run, all SRAM retained, all IO retained, supports 20us fast wake-up
- **High Performance Analog Interfaces**
  - 2x 12bit ADCs with 5Msps
    - Configurable as 12/10/8/6bit mode
    - Sampling rates up to 9Msps in 6bit mode
    - Up to 16 external single-ended input channels, support differential mode
  - 2x 12bit DACs with 1Msps
  - Support external independent reference voltage source
  - Analog voltage operation from 1.8~3.6V
- **Clock**

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- 4MHz~32MHz high-speed external crystal oscillator
- 32.768KHz low-speed external crystal oscillator
- High-speed internal RC (HSI) 8MHz
- Low-speed internal RC (LSI) 40KHz
- Built-in high-speed PLL
- Supports one clock output, which can be configured as system clock, HSE, HSI, or PLL divisional output

- **Reset**
  - Supports power-on, power-down, brown-out, and external pin reset
  - Supports watchdog reset, software reset
- **GPIOs**
  - Up to 65 GPIOs
  - Support multiplexed functions
  - Maximum toggle speed of 50Mhz
  - Most GPIOs are 5V voltage tolerant
- **Communication Interfaces**
  - 7x U(S)ART interfaces with maximum rate up to 4.5Mbps
    - 3x USART interfaces (support 1xISO7816, 1xIrDA, LIN)
    - 4x UART interfaces
  - 3x SPI interfaces, the rate is up to 36 MHz, 2 of which support I2S communication
  - 1x QSPI interface, the rate is up to 144 Mbps
  - 4x I2C interfaces, the rate is up to 1 MHz, which can be configured in master/slave mode and support dual address response in slave mode
  - 1x USB2.0 Full Speed Device interface
  - 2x CAN 2.0B bus interfaces
  - 1x SDIO interface, supports SD/MMC format
  - 1x DVP (Digital Video Port)
- **DMA controllers**
  - 2x high-speed DMA controllers
  - Each controller supports 8 channels
  - Channel source address and destination address can be configured arbitrarily
- **Real-time clock（RTC）**
  - Supports leap-year calendar, alarm events, periodic wake up
  - Supports internal and external clock calibration

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- **Timers**
  - 2x 16bit advanced timers with maximum control precision of 6.9ns
    - Support input capture, complementary output, quadrature encoding input, etc
    - Each timer has 4 independent channels, with 3 channels support 6 complementary PWM outputs
  - 4x 16bit general-purpose timers
    - Support input capture/output comparison /PWM output
    - Each timer has 4 independent channels
  - 2x 16bit basic timers
  - 1x 24bit SysTick timer
  - 1x 7bit Window Watchdog (WWDG)
  - 1x 12bit Independent Watchdog (IWDG)
- **Programming Methods**
  - Supports SWD/JTAG online debugging interface
  - Supports UART and USB Bootloader
- **Security Features**
  - Built-in hardware acceleration engine for cryptographic algorithm
  - Supports AES, DES, SHA and MD5 algorithms
  - Flash encryption, multi-user partition management (MMU)
  - True random number generator(TRNG)
  - CRC16/32 calculation
  - Supports write protection (WRP), multiple read protection (RDP) levels (L0/L1/L2)
  - Supports secure boot, program encryption download, secure update
  - Supports clock failure detection, anti-tamper detection
- **96-bit UID and 128-bit UCID**
- **Operation Conditions**
  - Operating voltage range: 1.8V~3.6V
  - Operating temperature range: -40℃ ~ 105℃
  - ESD: ±4KV (HBM model), ±1KV (CDM model)
- **Packages**
  - QFN32(4mm x 4mm)
  - QFN40(5mm x 5mm)
  - LQFP64(10mm x 10mm)

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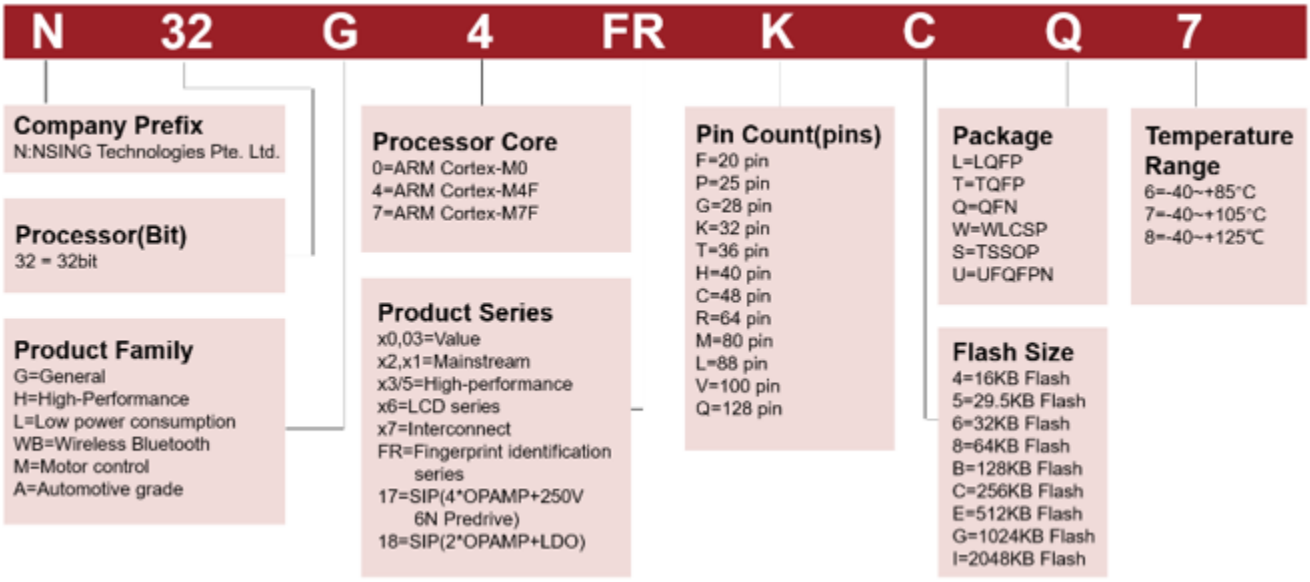
– LQFP80(12mm x 12mm)

- **Ordering Information**

Reference	Part Number
N32G4FRxC	N32G4FRKCQ7,N32G4FRHCQ7
N32G4FRxE	N32G4FRKEQ7,N32G4FRHEQ7,N32G4FRREL7,N32G4FRMEL7

1 Naming Convention



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2 Product Configurations

Device		N32G4FRKC/E		N32G4FRHC/E		N32G4FRRE	N32G4FRME
Flash Capacity（KB）		256	512	256	512	512	512
SRAM Capacity（KB）		144	144	144	144	144	144
CPU Frequency		ARM® Cortex®-M4F @144MHz,180DMIPS					
Operating Conditions		1.8~3.6V/-40~105℃					
Timers	General	4					
	Advanced	2					
	Basic	2					
Communication Interface	SPI	2		3			
	I2S	1		2			
	QSPI	1					
	I2C	3				4	
	USART	1		2		3	
	UART	3		4			
	USB	1					
	CAN	1		2			
	SDIO	No(1)				1	
	DVP	No(1)		1			
GPIO		24		32		51	65
DMA		2					
DMA Channels		16Channel					
12bit ADC		2		2		2	2
ADC Channels		7Channel		11Channel		16Channel	16Channel
12bit DAC		2					
DAC Channels		2Channel					
Algorithm Support		DES/3DES、AES、 SHA1/SHA224/SHA256, MD5, CRC16/CRC32, TRNG					
Security Protection		Read/Write Protection（RDP/WRP）, Storage Encryption, Partition Protection, Secure Boot					
Package		QFN32		QFN40		LQFP64	LQFP80

Note: (1) Not supported

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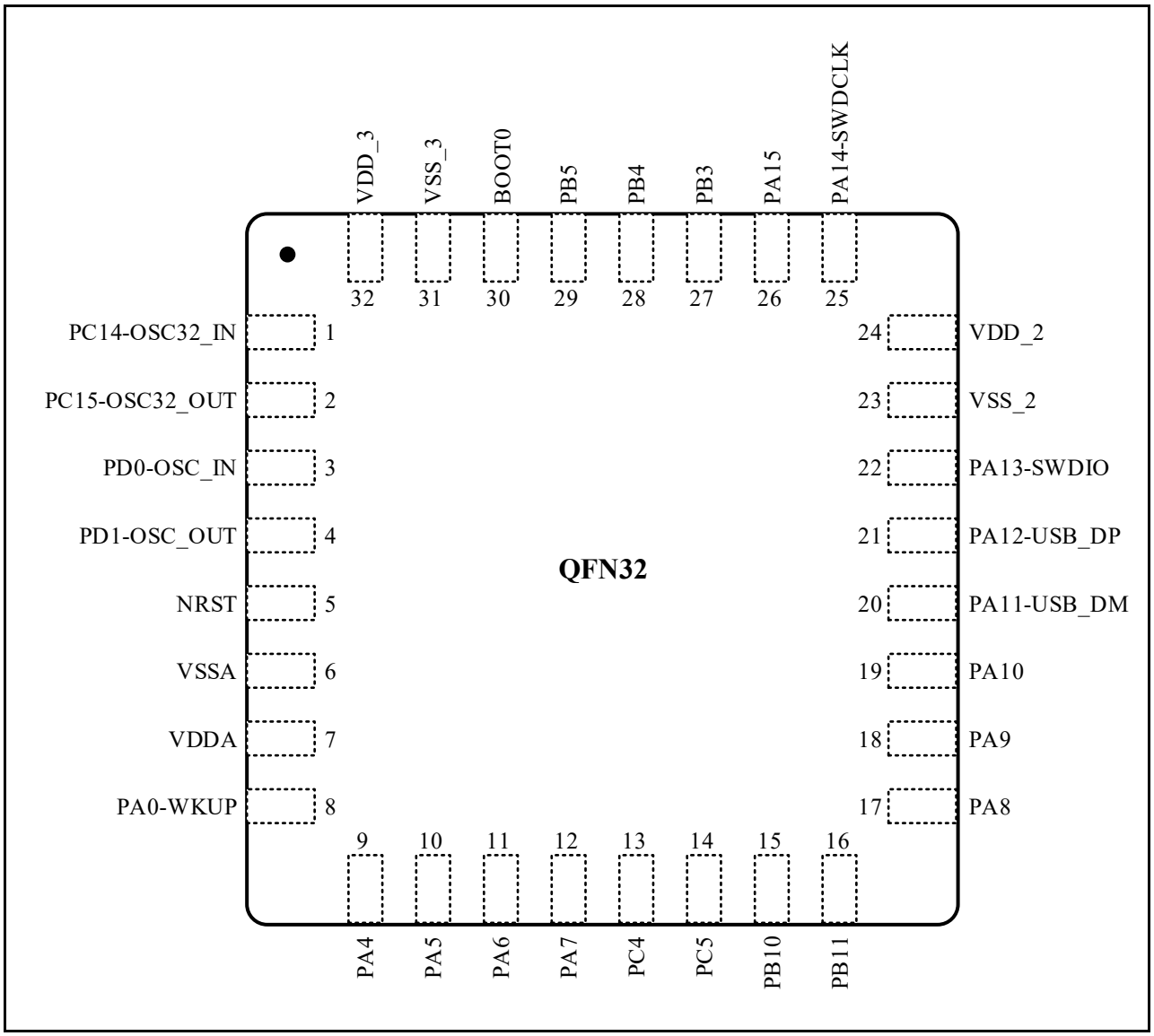
3 Packages

3.1 QFN32 Package

3.1.1 QFN32 Pin Assignment



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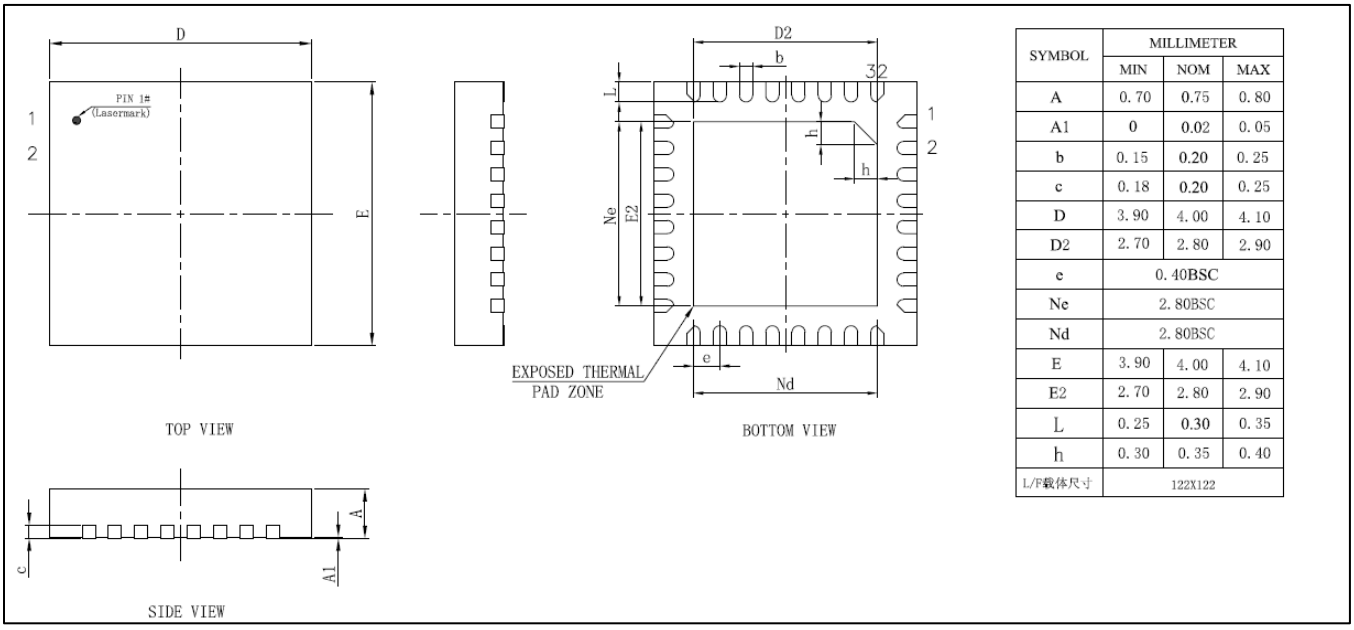
3.1.2 QFN32(4mm x 4mm) Package Dimensions



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0	0.02	0.05
b	0.15	0.20	0.25
c	0.18	0.20	0.25
D	3.90	4.00	4.10
D2	2.70	2.80	2.90
e	0.40BSC		
Ne	2.80BSC		
Nd	2.80BSC		
E	3.90	4.00	4.10
E2	2.70	2.80	2.90
L	0.25	0.30	0.35
h	0.30	0.35	0.40
L/F载体尺寸	122X122		

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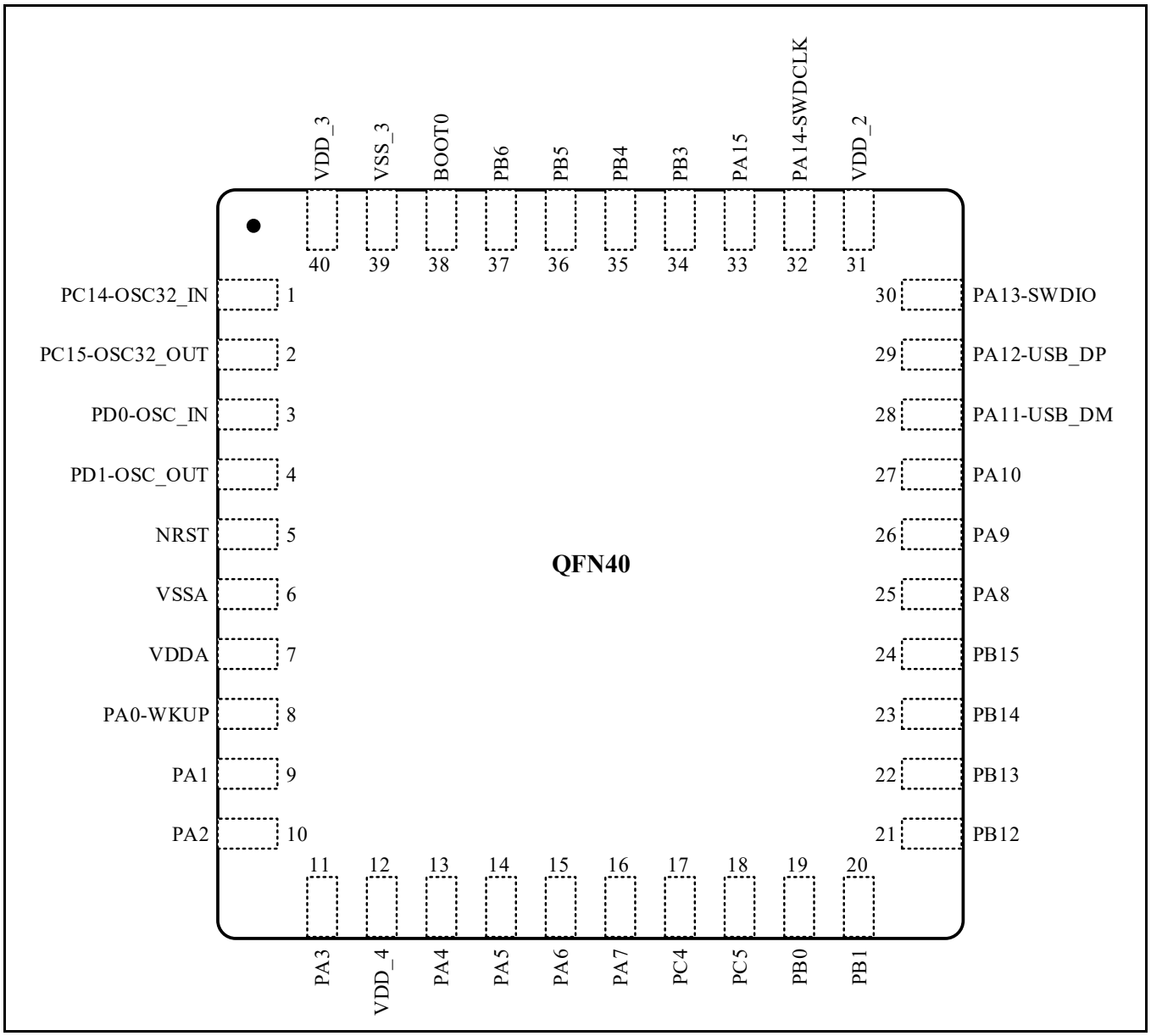
3.2 QFN40 Package

3.2.1 QFN40 Pin Assignment



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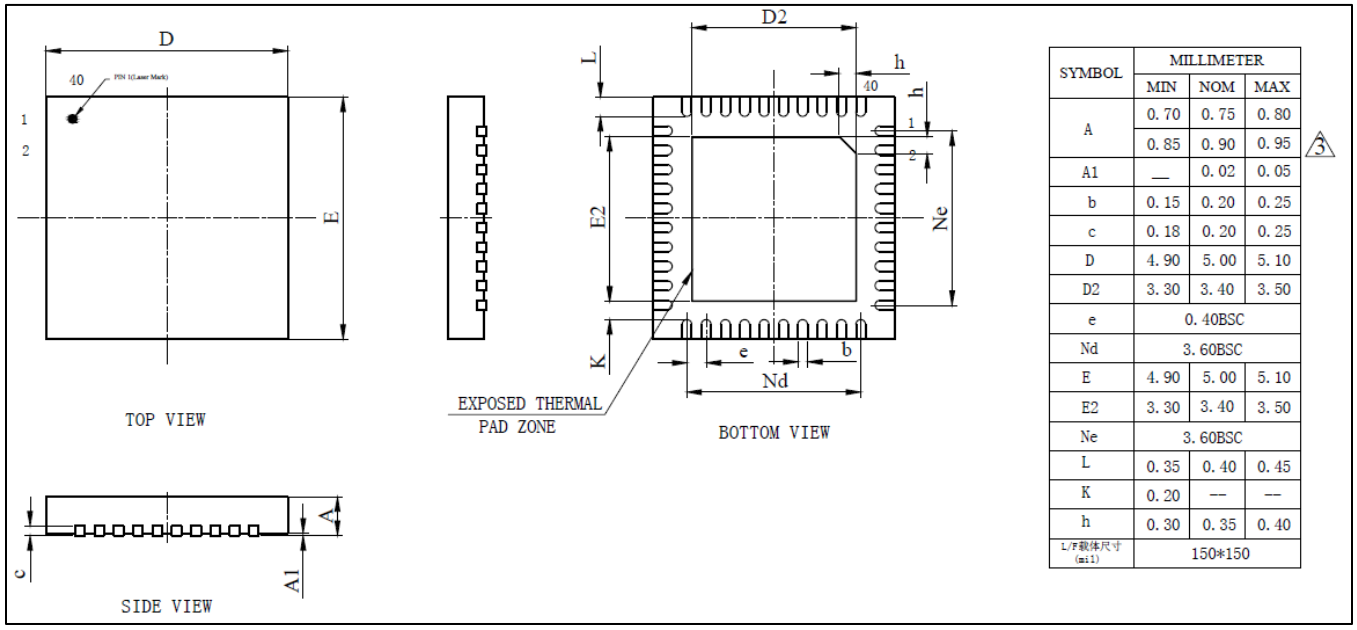
3.2.2 QFN40(5mm x 5mm) Package Dimensions



SYMBOL	MILLIMETER			
	MIN	NOM	MAX	
A	0.70	0.75	0.80	
	0.85	0.90	0.95	3
A1	—	0.02	0.05	
b	0.15	0.20	0.25	
c	0.18	0.20	0.25	
D	4.90	5.00	5.10	
D2	3.30	3.40	3.50	
e	0.40BSC			
Nd	3.60BSC			
E	4.90	5.00	5.10	
E2	3.30	3.40	3.50	
Ne	3.60BSC			
L	0.35	0.40	0.45	
K	0.20	—	—	
h	0.30	0.35	0.40	
L/F载体尺寸 (mil)	150*150			

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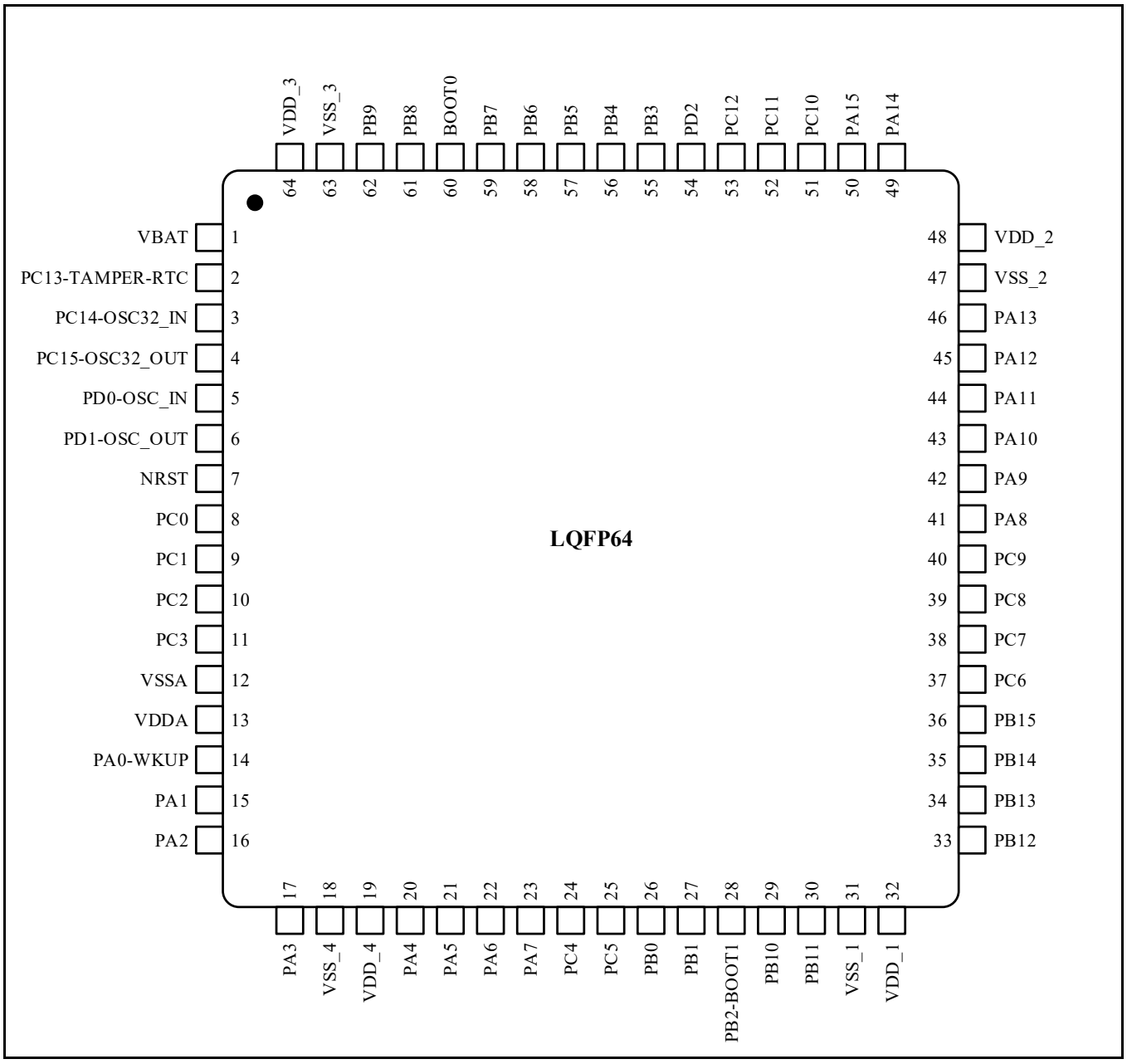
3.3 LQFP64 Package

3.3.1 LQFP64 Pin Assignment



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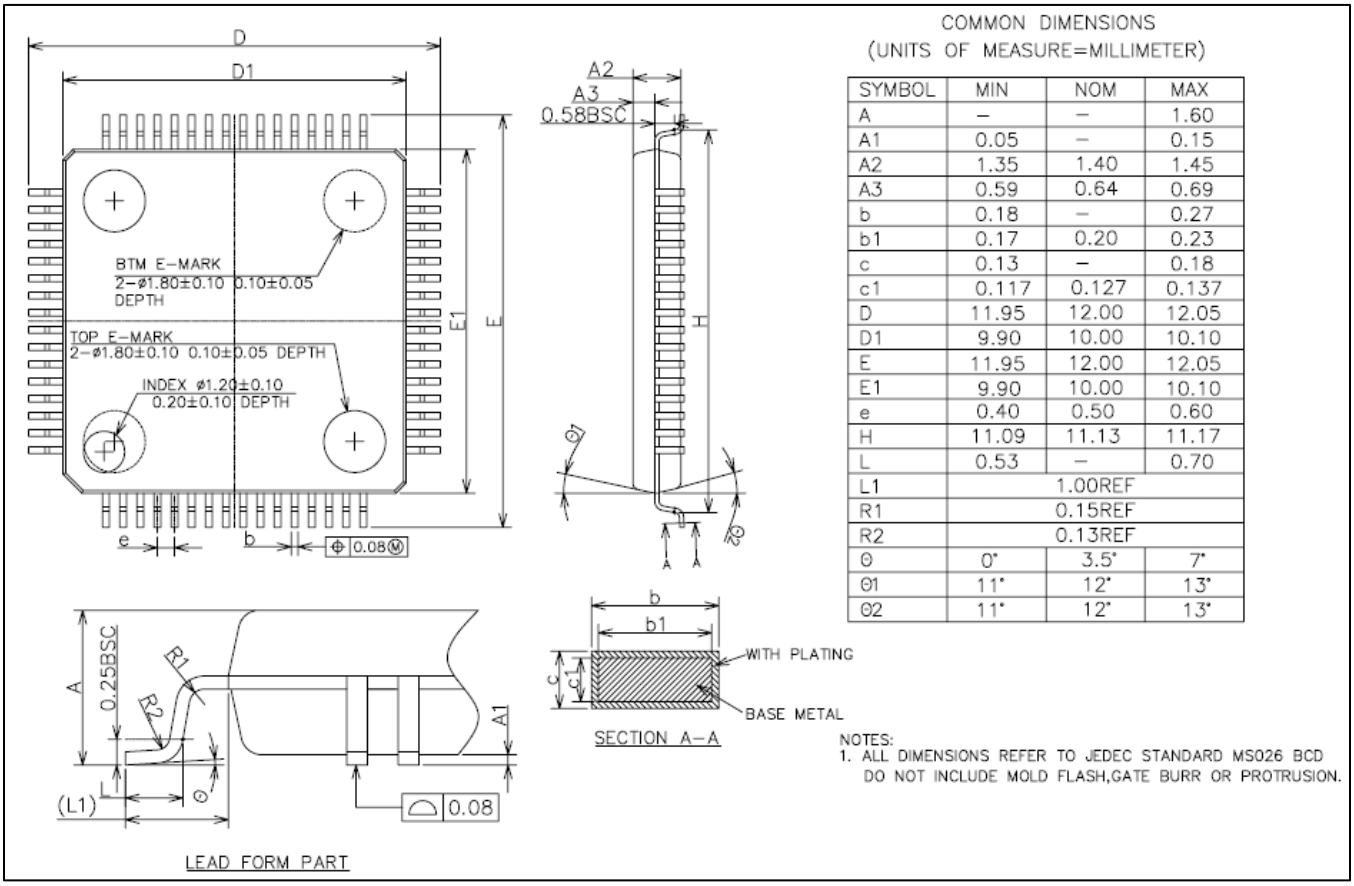
3.3.2 LQFP64(10mm x 10mm) Package Dimensions



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	–	–	1.60
A1	0.05	–	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	–	0.27
b1	0.17	0.20	0.23
c	0.13	–	0.18
c1	0.117	0.127	0.137
D	11.95	12.00	12.05
D1	9.90	10.00	10.10
E	11.95	12.00	12.05
E1	9.90	10.00	10.10
e	0.40	0.50	0.60
H	11.09	11.13	11.17
L	0.53	–	0.70
L1		1.00REF	
R1		0.15REF	
R2		0.13REF	
θ	0°	3.5°	7°
θ1	11°	12°	13°
θ2	11°	12°	13°

NOTES:
1. ALL DIMENSIONS REFER TO JEDEC STANDARD MS026 BCD
DO NOT INCLUDE MOLD FLASH,GATE BURR OR PROTRUSION.

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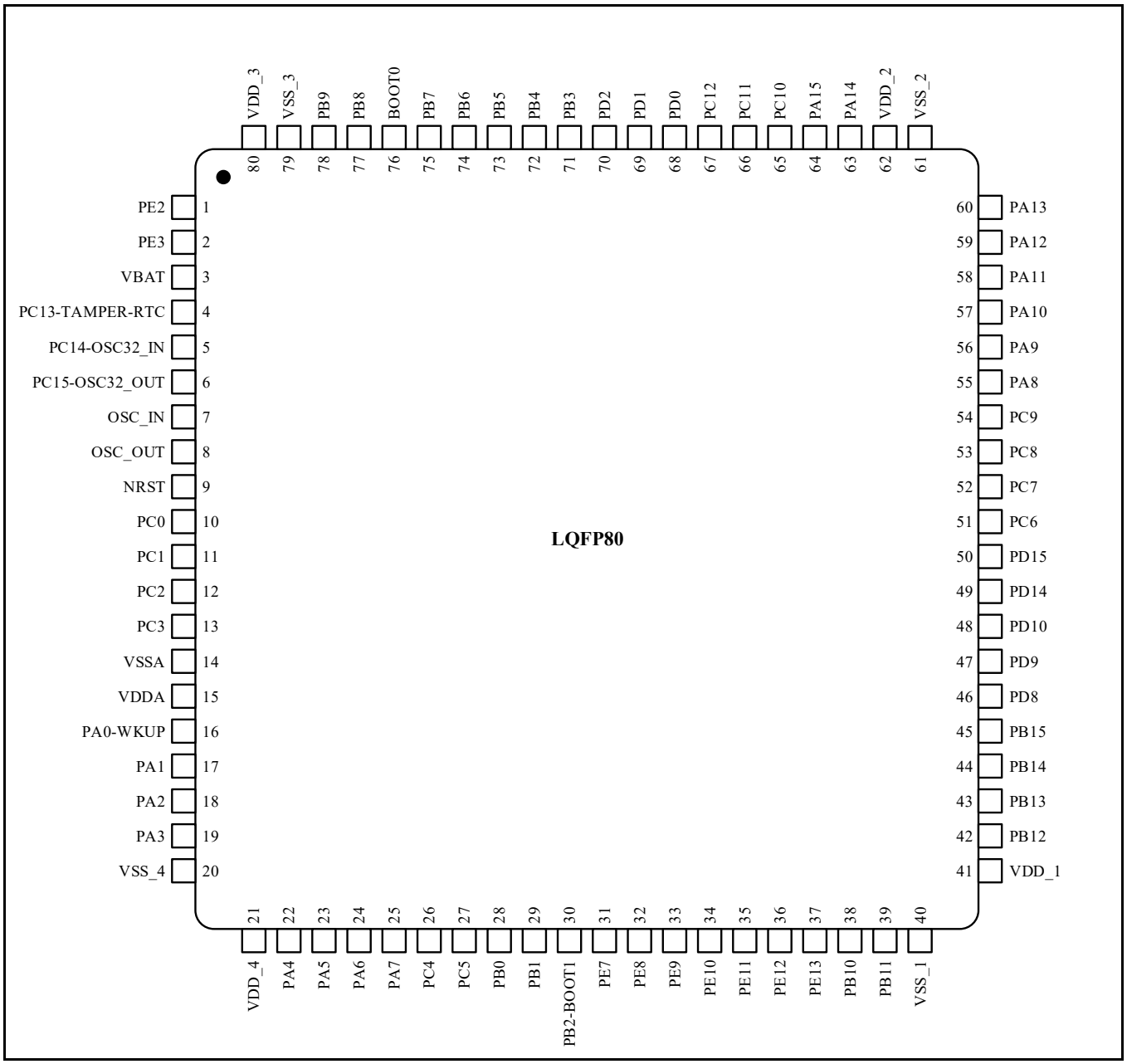
3.4 LQFP80 Package

3.4.1 LQFP80 Pin Assignment



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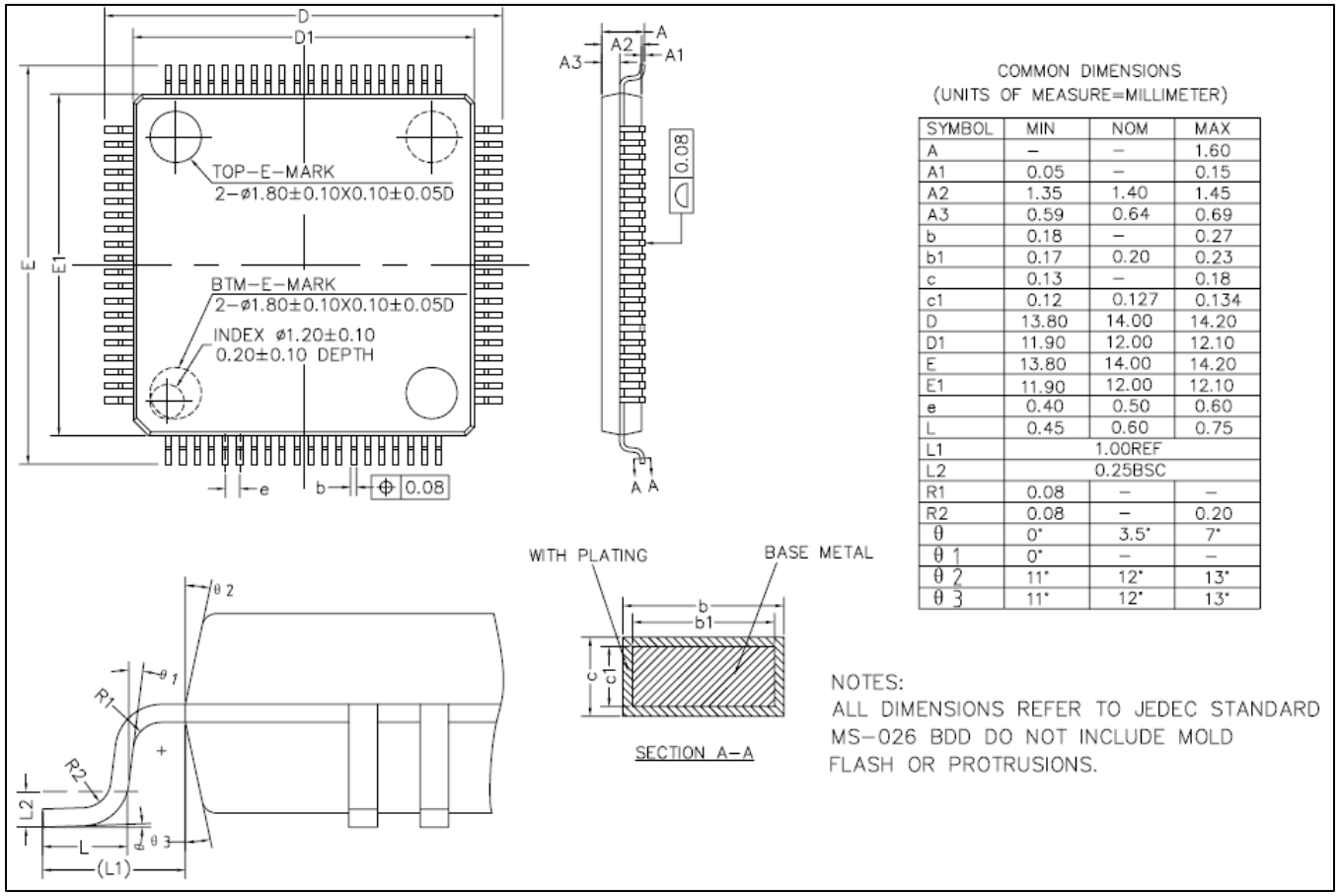
3.4.2 LQFP80(12mm x 12mm) Package Dimensions



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	–	–	1.60
A1	0.05	–	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	–	0.27
b1	0.17	0.20	0.23
c	0.13	–	0.18
c1	0.12	0.127	0.134
D	13.80	14.00	14.20
D1	11.90	12.00	12.10
E	13.80	14.00	14.20
E1	11.90	12.00	12.10
e	0.40	0.50	0.60
L	0.45	0.60	0.75
L1		1.00REF	
L2		0.25BSC	
R1	0.08	–	–
R2	0.08	–	0.20
θ	0°	3.5°	7°
θ 1	0°	–	–
θ 2	11°	12°	13°
θ 3	11°	12°	13°

NOTES:
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4 Version History

Version	Date	Changes
V1.0	2020.2.12	Initial version
V1.0.1	2020.12.15	Modify 3.1.1, 3.2.1, 3.3.1, 3.4.1 pin distribution diagram
V1.1	2022.7.6	Delete SDIO eMMC format
V1.2	2024.04.04	Error correction

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