N32G432x8/xB Product Brief

N32G432 series uses 32-bit ARM Cortex-M4F core, operating frequency up to 108MHz, supporting floating-point unit and DSP instructions. The devices integrate up to 128KB of encrypt Flash, and 32KB of SRAM. The series features rich of high-performance interfaces, including one built-in 12-bit 5Msps ADC, two independent rail-to-rail operational amplifiers, two high-speed comparators, one 1Msps 12-bit DAC, multi-channel U(S)ART, I2C, SPI, USB, CAN, and other communication interfaces, allowing a built-in hardware acceleration engine for cryptographic algorithms.

Key Features

- **CPU Core**
  - 32-bit ARM Cortex-M4F core with FPU, supporting single-cycle multiplication and hardware division, DSP instructions and MPU
  - Built-in 2KB instruction Cache, supporting 0-wait-state execution from Flash memory
  - Frequency up to 108MHz with 135DMIPS
- **Memories**
  - Up to 128KByte of embedded Flash with ECC
  - Support encryption, multi-user partition and data protection
  - 100,000 erase/write cycles, and 10 years data retention
  - Up to 32KByte of SRAM with hardware parity check, including 24Kbyte SRAM1(SRAM1 can be configured to data retention in STOP2 mode) and 8 Kbyte SRAM2(both in Standby and Stop2 modes, SRAM2 can be configured to data retention)
- **Low Power Management**
  - STANDBY mode: 2.5uA, all backup registers retained, all IOs retained, optional RTC Run, 8KByte SRAM2 retained, supports fast wake up.
  - STOP2 mode: 6uA, RTC Run, 8KByte SRAM2 and 24Kbyte SRAM1 can be configured to retention, CPU registers retained, IOs retained, supports fast wake up
  - RUN mode: 90uA/MHz@108MHz
  - LPRUN mode: PLL off, MSI as the system master clock, MR off, LPR on, USB/CAN/SAC power off, other peripherals are optional
- **High Performance Analog Interfaces**
  - 1x 12bit 5Msps ADC with 12/10/8/6 bits configurable resolution, up to 16 external single-ended input channels, supporting differential mode.
  - 1x 12bit 1Msps DAC
  - Internal 2.048V independent reference voltage source
- **Clock**

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- 4MHz~32MHz high-speed external crystal oscillator
- 32.768KHz low-speed external crystal oscillator
- High-speed internal RC(HSI) 16MHz
- Multi-speed internal RC(MSI) 100K~4MHz
- Low-speed internal RC(LSI) 40KHz
- Built-in high-speed PLL
- Supports one clock output, which can be configured as low-speed or high-speed clock

- **Reset**
  - Support power on, brown-out, and external pin reset.
  - Support watchdog reset, software reset
- **GPIOs**
  - Up to 52 GPIOs
  - Support multiplexed functions
  - Maximum toggle speed of 50 MHz
- **Communication Interfaces**
  - 5x U(S)ART interfaces, including three USART interfaces (support 1xISO7816, 1xIrDA, LIN) and two UART interfaces
  - 1x LPUART, supports waking up MCU from low-power STOP2 mode
  - 2x SPI interfaces, the rate is up to 27 Mbps, support I2S communication
  - 2x I2C interfaces, the rate is up to 1 MHz, which can be configured in master/slave mode and support dual address response in slave mode
  - 1x USB2.0 FS Device interface
  - 1x CAN 2.0A/B bus interface
- **DMA Controller**
  - 1x high-speed DMA controller
  - Each controller supports 8 channels
  - Channel source address and destination address can be configured arbitrarily
- **RTC Real-Time Clock**
  - Supports leap year perpetual calendar, alarm event, periodic wake up, support internal and external clock calibration
- **Timers**
  - 2x 16bit advanced control timers
    - Support input capture, complementary output, quadrature encoding input, the highest control accuracy is 9.25ns.
    - Each timer has four independent channels, with 3 channels supporting complementary PWM outputs.
  - 5x 16bit general-purpose timers
    - Support input capture/output comparison /PWM output.
    - Each timer has 4 independent channels.
  - 2x 16bit basic timers
  - 1x 16bit low power timer, supports double pulse counting function, can work in STOP2 mode
  - 1x 24bit SysTick timer
  - 1x 7bit window Watchdog (WWDG)

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- 1x 12bit independent Watchdog (IWDG)

- **Programming Methods**
  - Support SWD/JTAG online debugging interface
  - Support UART and USB Bootloader
- **Security Features**
  - Built-in hardware acceleration engine for cryptographic algorithms
  - Support AES, DES, TDES, SHA1/224/256 and SM7 algorithms
  - Flash storage encryption, multi-user partition management (MMU)
  - True random number generator(TRNG)
  - CRC16/32 calculation
  - Support write protection (WRP), multiple read protection (RDP) levels (L0/L1/L2)
  - Support secure boot, program encryption download, secure update
  - Support external clock failure detection, tamper detection
- **96-bit UID and 128-bit UCID**
- **Operating Conditions**
  - Operating voltage range: 1.8V~3.6V
  - Operating temperature range: -40℃ ~ 105℃
  - ESD: ±4KV (HBM model), ±1KV (CDM model)
- **Packages**
  - LQFP32(7mm x 7mm)
  - LQFP48(7mm x 7mm)
  - LQFP64(10mm x 10mm)
- **Ordering Information**

Reference	Part Number
N32G432x8	N32G432K8L7, N32G432C8L7，N32G4322R8L7
N32G432xB	N32G432KBL7, N32G432CBL7，N32G432RBL7

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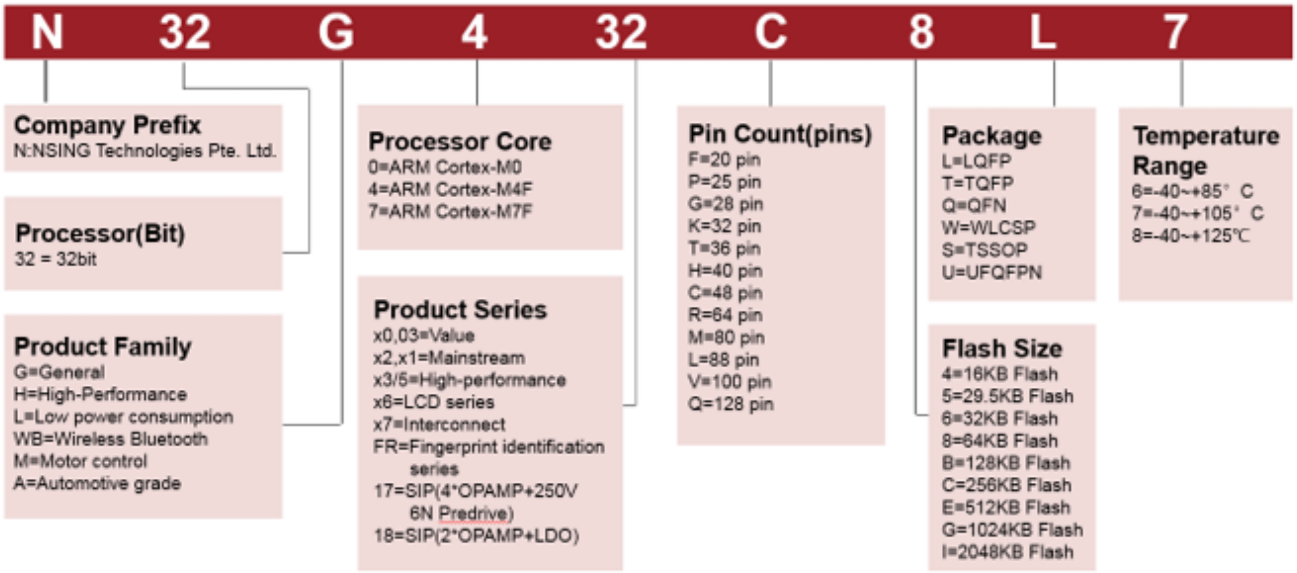
1 Naming Convention



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2 Product Configurations

Device		N32G432K8/B		N32G432C8/B		N32G432R8/B	
Flash Capacity (KB)		64	128	64	128	64	128
SRAM Capacity (KB)		24	32	24	32	24	32
CPU Frequency		ARM Cortex-M4F @108MHz,135DMIPS					
Operating Conditions		1.8~3.6V/-40~105℃					
Timers	General	5					
	Advanced	2					
	Basic	2					
	LPTIM	1					
Communication Interface	SPI	2					
	I2S	2					
	I2C	2					
	UART	2					
	USART	2		3			
	LPUART	1					
	USB	1					
	CAN	1					
GPIO		26		38		52	
DMA Number of Channels		1x 8 Channel					
12bit ADC Number of Channels		1x 10 Channel		1x 10 Channel		1x 16 Channel	
12bit DAC Number of Channels		1x 2 Channel					
Algorithm Support		DES/TDES, AES, SHA1/SHA224/SHA256 CRC16/CRC32, TRNG					
Security Protection		Read-Write Protection (RDP/WRP), Storage Encryption, Partition Protection, Security Boot					
Package		LQFP32		LQFP48		LQFP64	

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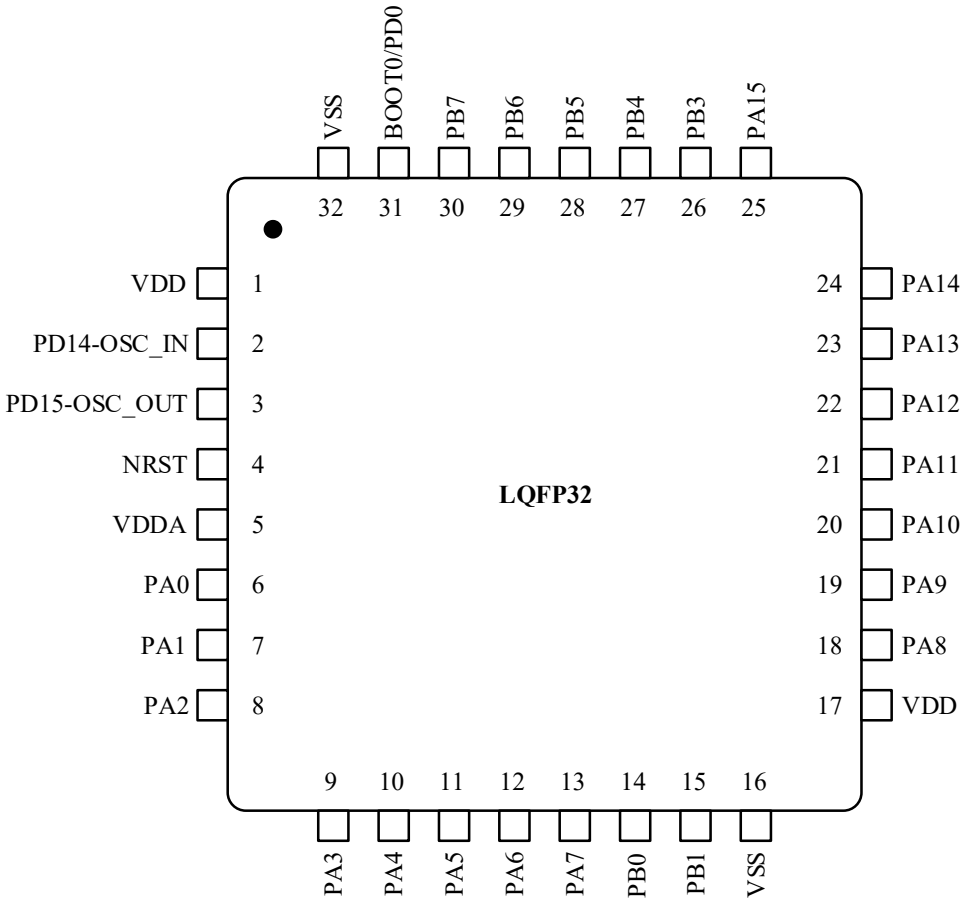
3 Packages

3.1 LQFP32 Package

3.1.1 LQFP32 Pin Assignment



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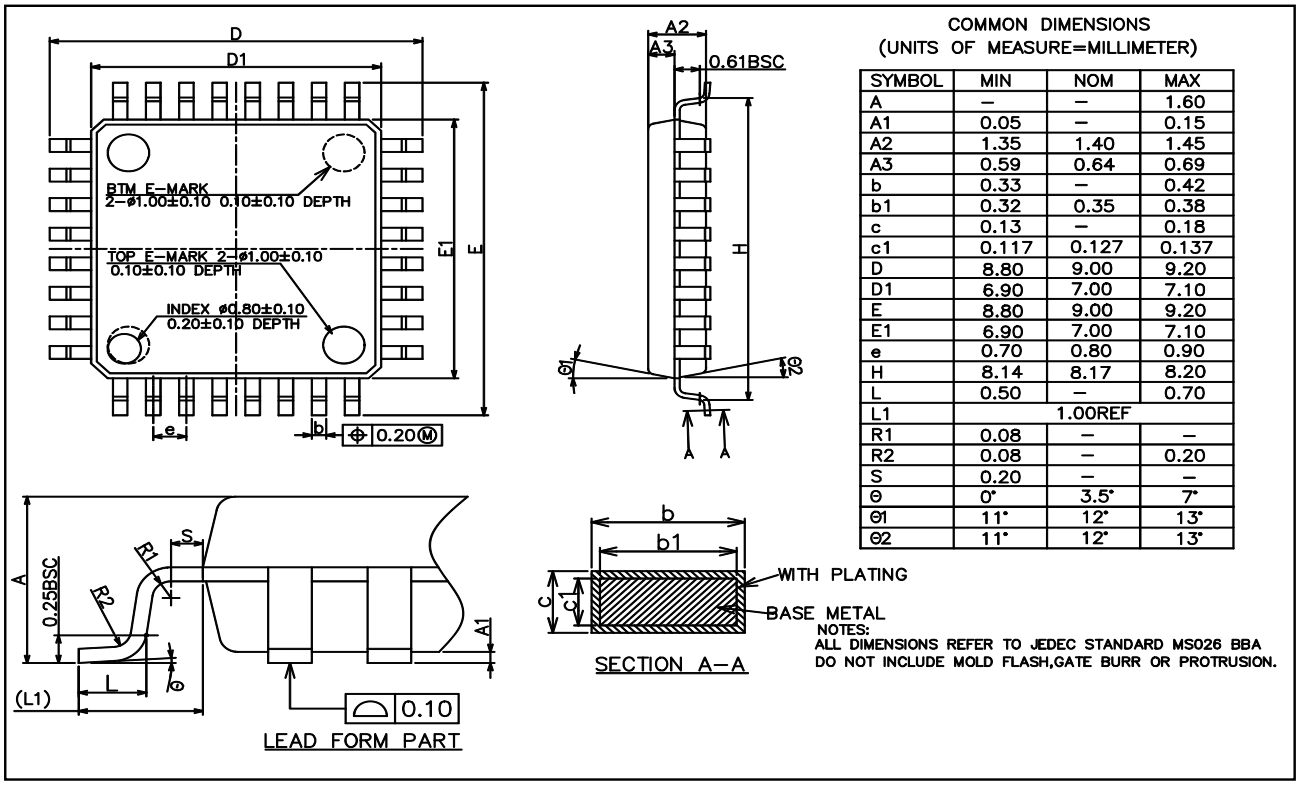
3.1.2 LQFP32(7mm x 7mm) Package Dimensions



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	–	–	1.60
A1	0.05	–	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.33	–	0.42
b1	0.32	0.35	0.38
c	0.13	–	0.18
c1	0.117	0.127	0.137
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
e	0.70	0.80	0.90
H	8.14	8.17	8.20
L	0.50	–	0.70
L1		1.00REF	
R1	0.08	–	–
R2	0.08	–	0.20
S	0.20	–	–
θ	0°	3.5°	7°
θ1	11°	12°	13°
θ2	11°	12°	13°

NOTES:
ALL DIMENSIONS REFER TO JEDEC STANDARD MS026 BBA
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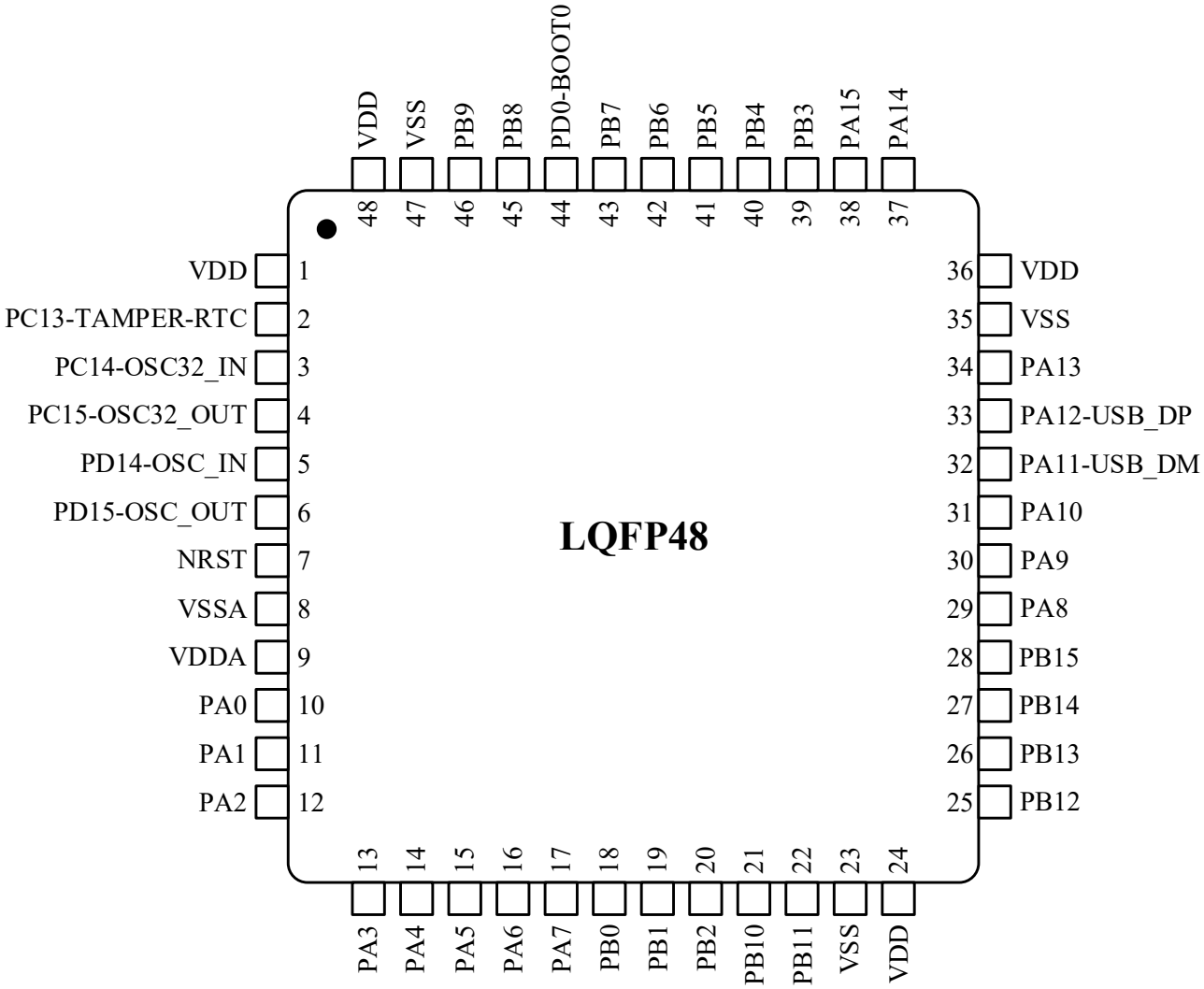
3.2 LQFP48 Package

3.2.1 LQFP48 Pin Assignment



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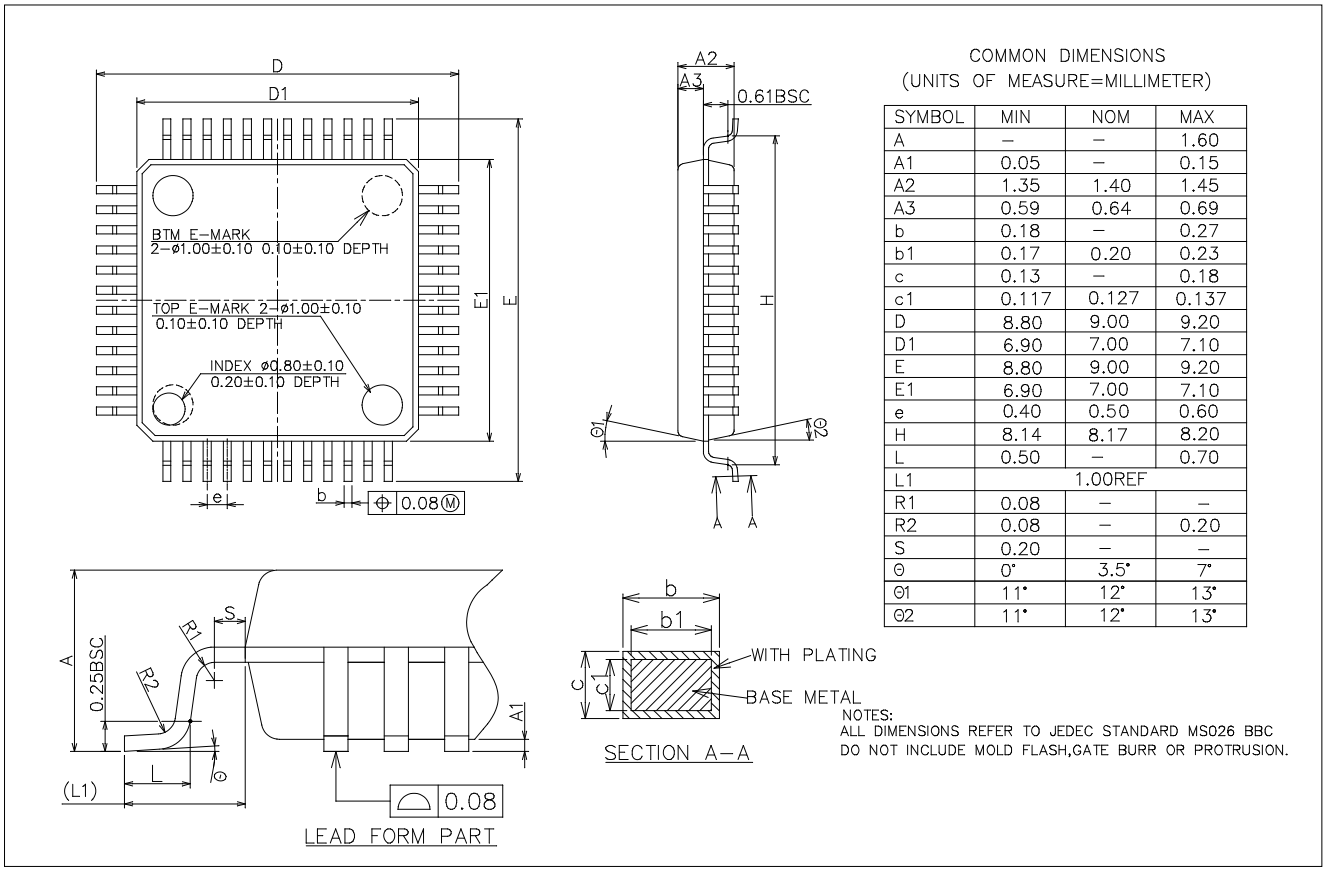
3.2.2 LQFP48(7mm x 7mm) Package Dimensions



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	–	–	1.60
A1	0.05	–	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	–	0.27
b1	0.17	0.20	0.23
c	0.13	–	0.18
c1	0.117	0.127	0.137
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
e	0.40	0.50	0.60
H	8.14	8.17	8.20
L	0.50	–	0.70
L1		1.00REF	
R1	0.08	–	–
R2	0.08	–	0.20
S	0.20	–	–
θ	0°	3.5°	7°
θ1	11°	12°	13°
θ2	11°	12°	13°

NOTES:
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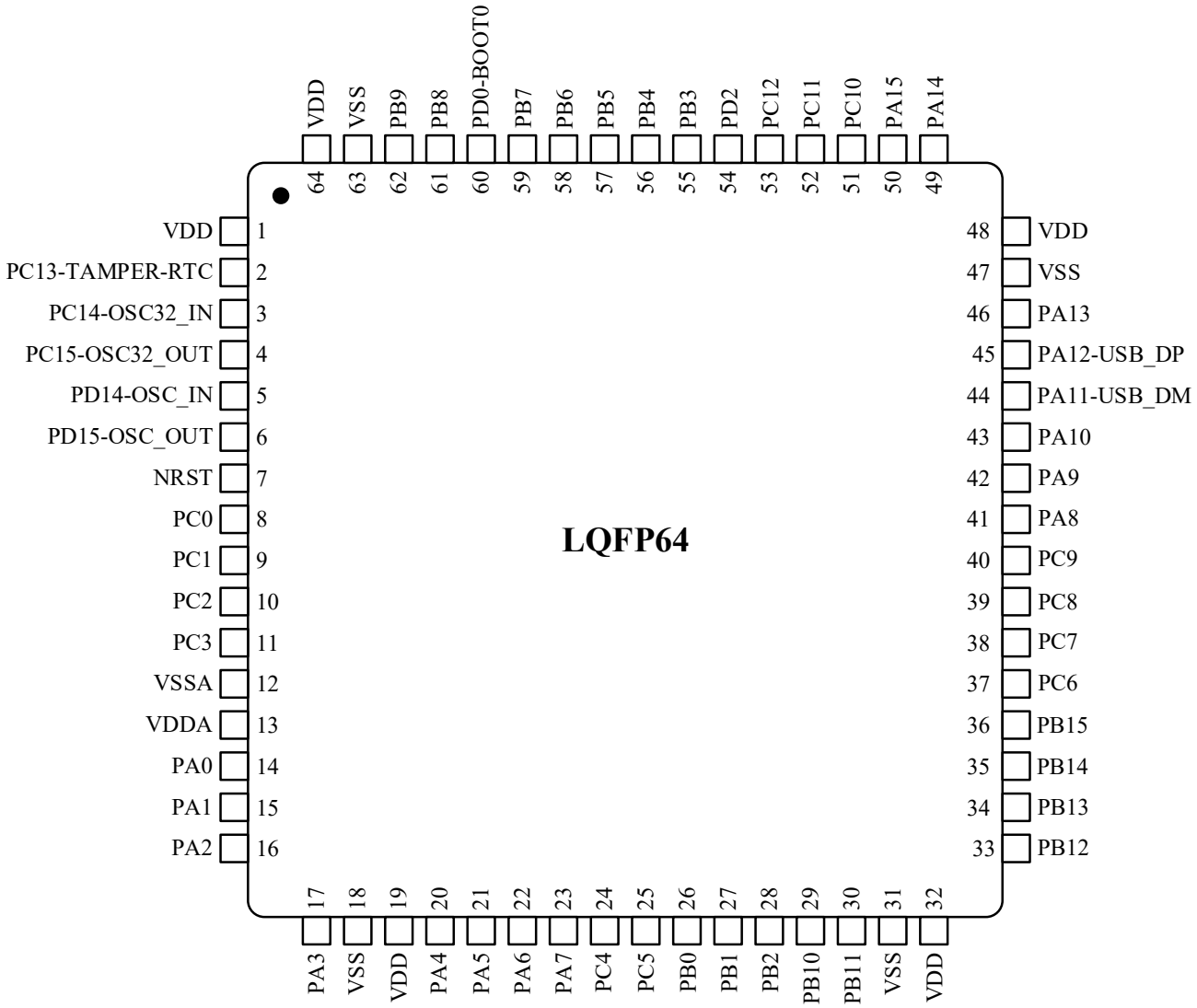
3.3 LQFP64 Package

3.3.1 LQFP64 Pin Assignment



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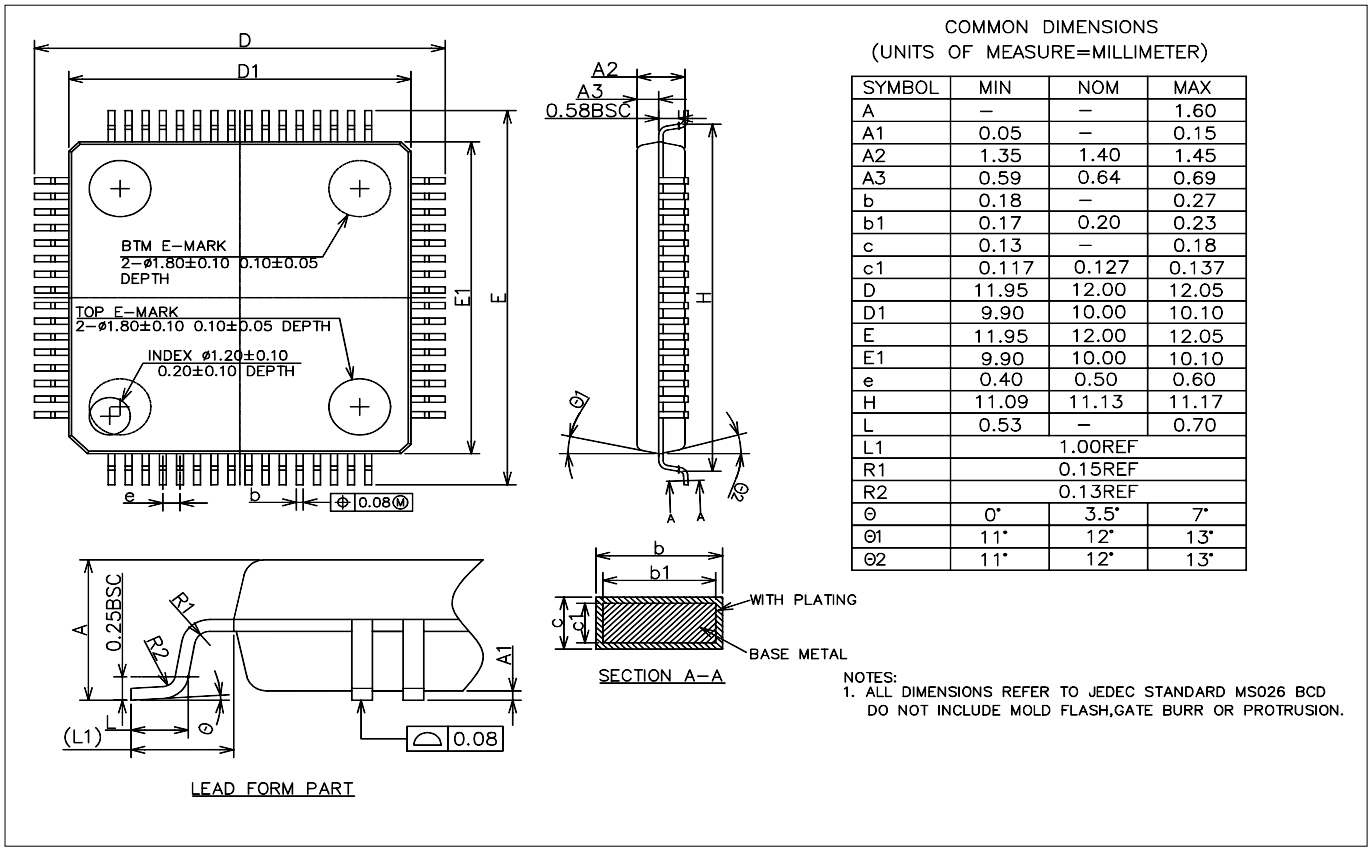
3.3.2 LQFP64(10mm x 10mm) Package Dimensions



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	–	–	1.60
A1	0.05	–	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	–	0.27
b1	0.17	0.20	0.23
c	0.13	–	0.18
c1	0.117	0.127	0.137
D	11.95	12.00	12.05
D1	9.90	10.00	10.10
E	11.95	12.00	12.05
E1	9.90	10.00	10.10
e	0.40	0.50	0.60
H	11.09	11.13	11.17
L	0.53	–	0.70
L1		1.00REF	
R1		0.15REF	
R2		0.13REF	
Θ	0°	3.5°	7°
Θ1	11°	12°	13°
Θ2	11°	12°	13°

NOTES:
1. ALL DIMENSIONS REFER TO JEDEC STANDARD MS026 BCD
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4 Version History

Version	Date	Changes
V1.0	2020.6.12	Initial release
V1.2	2021.4.14	Updated product model resource configuration
V1.3	2022.7.6	Modify the description of low power

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