

N32L43xx8/xB

Product Brief

N32L43x series uses 32-bit ARM Cortex-M4F core, operating frequency up to 108MHz, supporting floating-point unit and DSP instructions, The devices integrate up to 128KB of encrypt Flash, and 32KB of SRAM. The series features rich of high-performance interfaces, including one built-in 12-bit 5Msps ADC, two independent rail-to-rail operational amplifiers, two high-speed comparators, one 1Msps 12-bit DAC, Integrated low power flow metering module . multi-channel U(S)ART, LPUART, I2C, SPI, USB, CAN and other communication interfaces, Segment LCD Driver Interface, allowing a built-in hardware acceleration engine for cryptographic algorithms.

Key Features

- **CPU core**
 - 32-bit ARM Cortex-M4F core with FPU, supporting single-cycle multiplication and hardware division, DSP instructions and MPU.
 - Built-in 2KB instruction Cache, supporting 0-wait-state execution from Flash memory
 - Frequency up to 108MHz with 135DMIPS
- **Memories**
 - Up to 128KByte of embedded Flash with ECC
 - Support encryption, multi-user partition and data protection
 - 100,000 erase/write cycles, and 10 years data retention
 - Up to 32KByte of SRAM with hardware parity check, including 24Kbyte SRAM1(SRAM1 can be configured to data retention in STOP2 mode) and 8 Kbyte SRAM2(both in Standby and Stop2 modes, SRAM2 can be configured to retention)
- **Low Power Management**
 - STANDBY mode: 2.5uA, All backup registers retained, all IOs retained, optional RTC Run, 8KByte Retention SRAM retained, supports fast wake up.
 - STOP2 mode: 6uA, RTC Run, 8KByte SRAM2 and 24KByte SRAM1 retained, CPU registers retained, all IOs retained, supports fast wake up.
 - RUN mode: 90uA/MHz@108MHz
 - LPRUN mode: The PLL is off, MSI is used as the system master clock. MR off, LPR on. USB/CAN/SAC power off, other peripherals are optional.
 - SLEEP mode: only CPU is stopped, all peripherals are optional.
 - LP-SLEEP mode: CPU is stopped, the PLL is off, USB/CAN/SAC module are disabled, all IOs remained, other peripherals are optional.
- **High Performance Analog Interfaces**
 - 1x 12bit 5Msps ADC
 - Multiple precision configuration

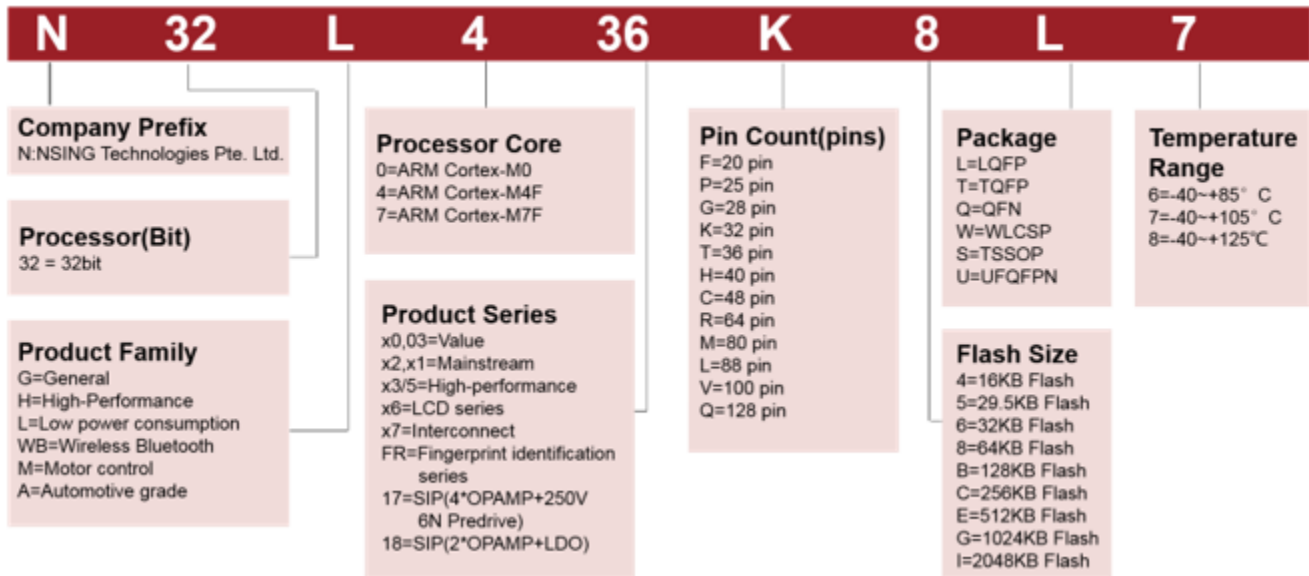
- Up to 16 external single-ended input channels
- Supports differential mode
- 2x rail-to-rail operational amplifiers with built-in up to 32 times programmable gain amplifier(PGA)
- 2x high-speed analog comparators with internal 64-level adjustable comparison reference. COMP1 can operate in low-power STOP2 mode
- 1x 12bit 1Msps DAC
- Internal 2.048V independent reference voltage source
- **Clock**
 - 4MHz~32MHz high-speed external crystal oscillator
 - 32.768KHz low-speed external crystal oscillator
 - High-speed internal RC(HSI) 16MHz
 - Multi-speed internal RC(MSI) 100K~4MHz
 - Low-speed internal RC(LSI) 40KHz
 - Built-in high-speed PLL
 - Supports one clock output, which can be configured as low-speed or high-speed clock
- **Reset**
 - Support power on, brown-out, and external pin reset
 - Support watchdog reset, software reset
- **GPIOs.**
 - Up to 52 GPIOs
 - Support multiplexed functions
 - Maximum toggle speed of 50 MHz
- **Communication Interface**
 - 5x U(S)ART interfaces
 - 3x USART interfaces (support 1xISO7816, 1xIrDA, LIN)
 - 2x UART interfaces
 - 1x LPUART, support waking up MCU from low-power STOP2 mode
 - 1x SPI interfaces, the rate is up to 27 Mbps, support I2S communication
 - 2x I2C interfaces, the rate is up to 1 MHz, which can be configured in master/slave mode and support dual address response in slave mode
 - 1x USB2.0 FS Device interface
 - 1x CAN 2.0A/B bus interface
- **Segment LCD Driver Interface**
 - Support a maximum of 320 segments (8x40) or 176 segments (4x44) monochrome passive LCD display

- Support flexible LCD refresh rate (30~102Hz)
- Support static 1/2, 1/3, 1/4, 1/8 duty cycle
- Support static 1/2, 1/3, 1/4 bias
- Support normal display in low-power STOP2 mode
- **Low-power Flow Metering Module (LPRCNT)**
 - Support waking up MCU from low-power STOP2 mode
 - Suitable for battery-powered flow metering applications
- **DMA**
 - 1x high-speed DMA controller
 - Each controller support 8 channels
 - Channel source address and destination address can be configured arbitrarily
- **RTC Real Time Clock**
 - Support leap year perpetual calendar, alarm event, periodic wake up,
 - Support internal and external clock calibration
- **Timers**
 - 2x 16bit Advanced timer counters
 - Support input capture, complementary output, quadrature encoding input, the highest control accuracy is 9.25ns.
 - Each timer has four independent channels, with 3 channels support 6 complementary PWM outputs
 - 5x 16bit General Purpose timer counters
 - Support input capture/output comparison /PWM output
 - Each timer has 4 independent channels
 - 2x 16bit Basic timer counters
 - 1x 16bit Low-power timer counter, support double pulse counting function, can work in STOP2 mode
 - 1x 24bit SysTick timer counter
 - 1x 7bit window Watchdog (WWDG)
 - 1x 12bit independent Watchdog (IWDG)
- **Programming Methods**
 - Support SWD/JTAG online debugging interface
 - Support UART and USB Bootloader
- **Security Features**
 - Built-in hardware acceleration engine for cryptographic algorithms
 - Support AES, DES, TDES, SHA1/224/256, SM1, SM3, SM4, and SM7 algorithms

- Flash storage encryption, multi-user partition management (MMU)
- True random number generator (TRNG)
- CRC16/32 calculation
- Support write protection (WRP), multiple read protection (RDP) levels (L0/L1/L2)
- Support security boot, program encryption download, secure updates
- Support external clock failure detection, tamper detection
- **96-bit UID and 128-bit UCID**
- **Operating Conditions**
 - Operating voltage range: 1.8V~3.6V
 - Operating temperature range: -40°C ~ 105°C
 - ESD: ±4KV (HBM model), ±1KV (CDM model)
- **Package**
 - LQFP32(7mm x 7mm)
 - LQFP48(7mm x 7mm)
 - LQFP64(10mm x 10mm)
 - LQFP80(12mm x 12mm)
- **Order Information**

Reference	Part Number
N32L433	N32L433K8L7, N32L433KBL7
N32L436	N32L436C8L7, N32L436R8L7, N32L436CBL7, N32L436RBL7, N32L436MBL7

1 Naming Convention



2 Product Configurations

Device		N32L433K8/B		N32L436C8/B		N32L436R8/B		N32L436MB
Flash size (KB)		64	128	64	128	64	128	128
SRAM size (KB)		24	32	24	32	24	32	32
CPU frequency		ARM Cortex-M4F @108MHz, 130DMIPS						
Operating Conditions		1.8~3.6V/-40~105°C						
Timer	General	5						
	Advanced	2						
	Basic	2						
	LPTIM	1						
Communication interface	SPI ⁽¹⁾	2						
	I2S ⁽¹⁾	2						
	I2C	2						
	UART	2						
	USART	2	3					
	LPUART	1						
	USB	1						
	CAN	1						
GPIO		26	38		52		64	
DMA		1x						
Number of Channels		8 Channel						
12bit ADC		1x		1x		1x		1x
Number of channels		10Channel		10Channel		16Channel		16Channel
12bit DAC		1x						
Number of channels		1 Channel						
LPRCNT(low-power non-magnetic metering)		No ⁽⁴⁾		1x				
OPAMP/COMP		2/2						
Segment LCD		No ⁽⁴⁾		4x20		4x34/8x30 ⁽²⁾⁽³⁾		4x44/8x40 ⁽³⁾
Algorithm support		DES/TDES、AES、SHA1/SHA224/SHA256SM1、SM3、SM4、SM7、CRC16/CRC32、TRNG						
Security and protection		Read and write protection (RDP/WRP), storage encryption, partition protection, and security startup						
Package		LQFP32		LQFP48		LQFP64		LQFP80

Notes:

⁽¹⁾ SPI1 and SPI2 interfaces can flexibly switch between SPI mode and I2S audio mode

⁽²⁾ LQFP64 package version B chips do not support LCD 1/8 duty cycle mode (8x30)

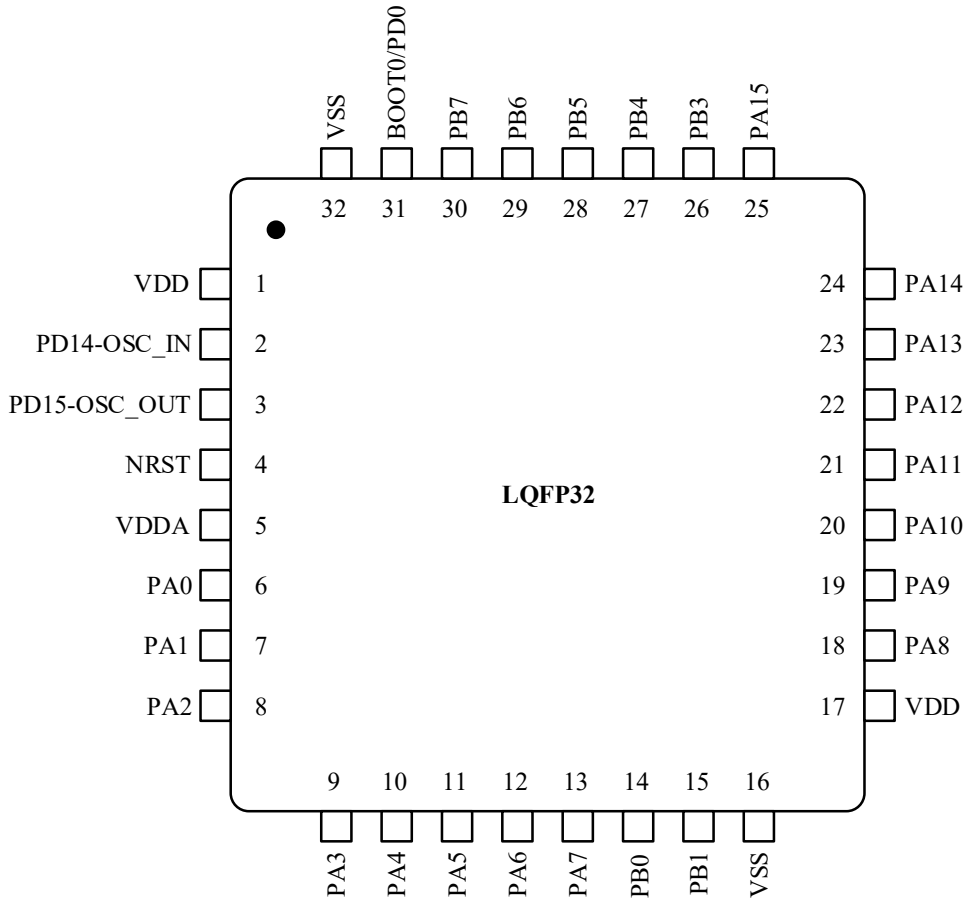
⁽³⁾ In the 1/8 duty cycle mode, the B-version and C-version chip LCDs do not support 1/4 bias

(4) It is not supported.

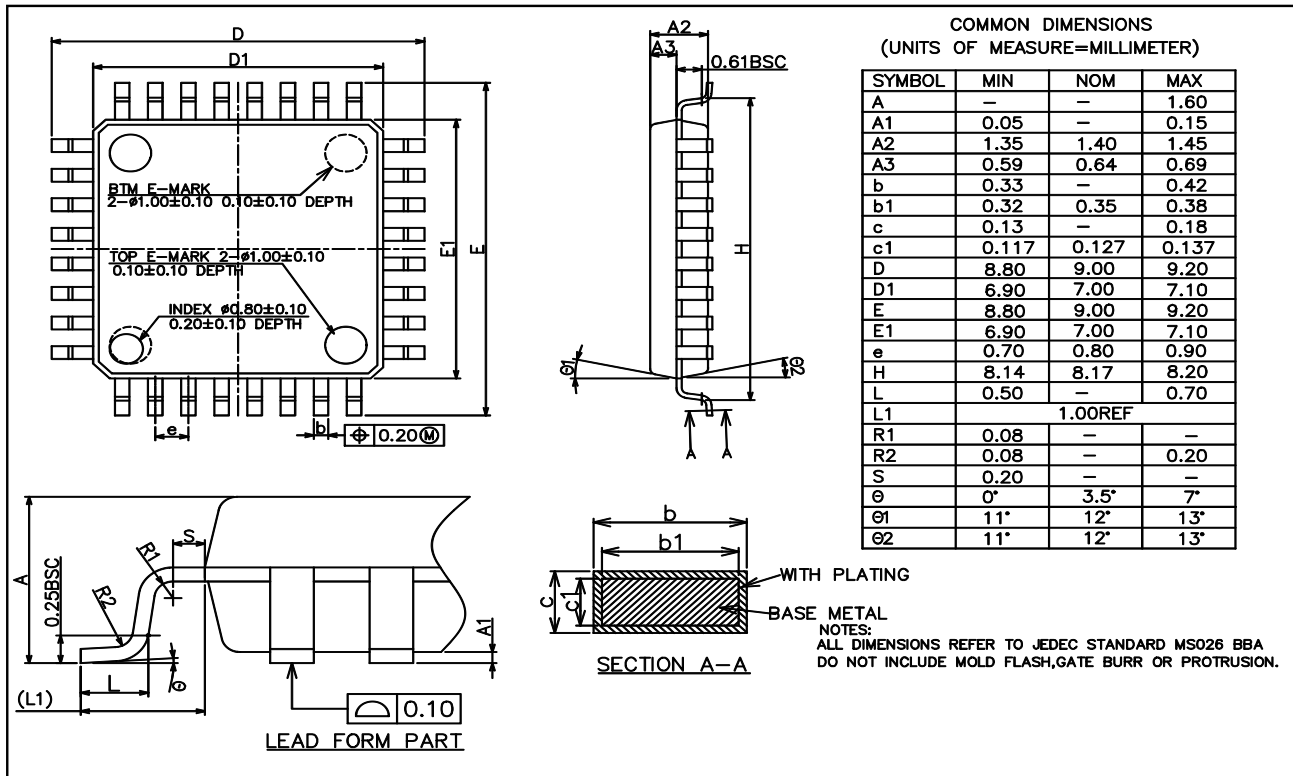
3 Package

3.1 LQFP32 Package

3.1.1 LQFP32 Pin Assignment

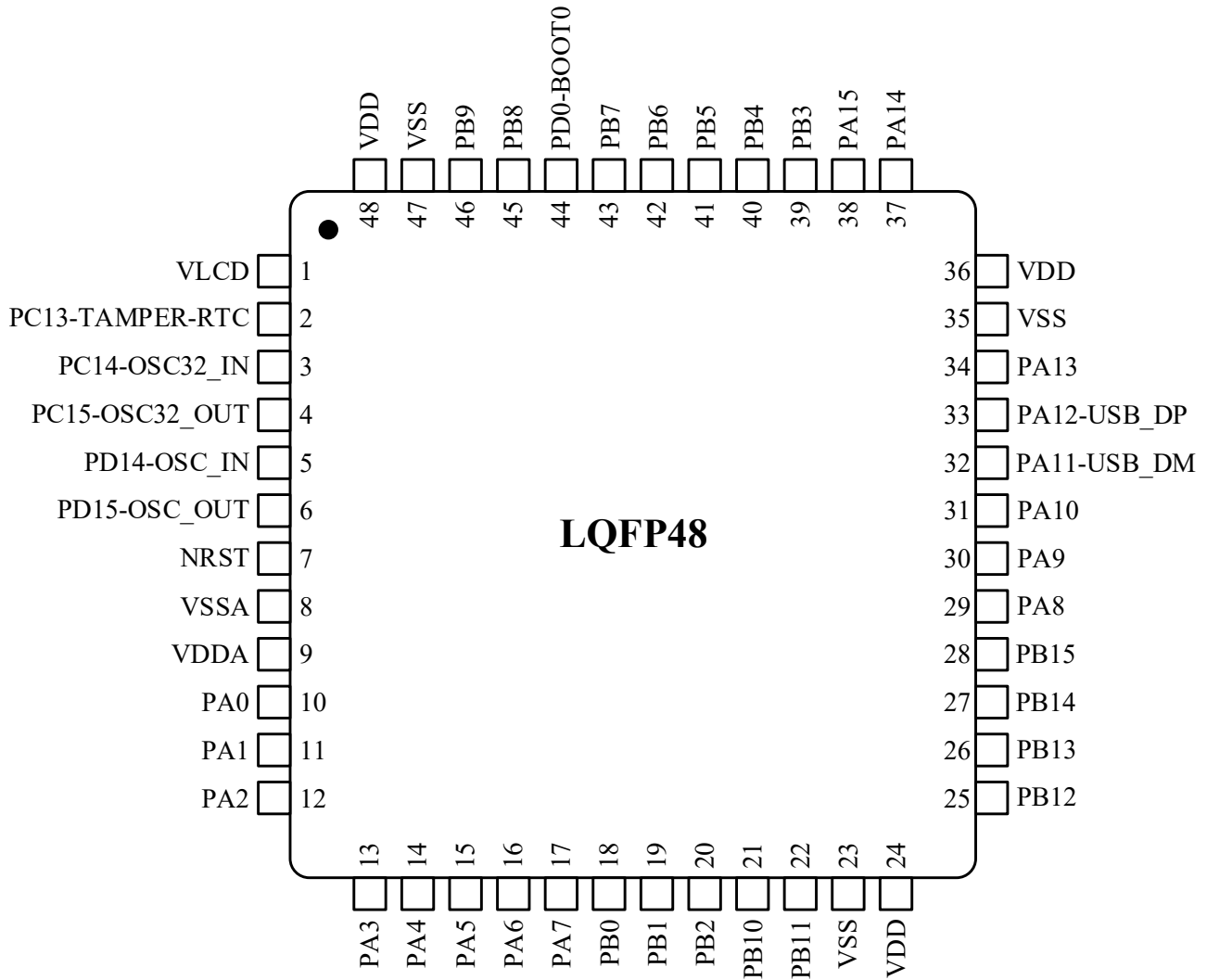


3.1.2 LQFP32(7mm x 7mm) Package Dimensions

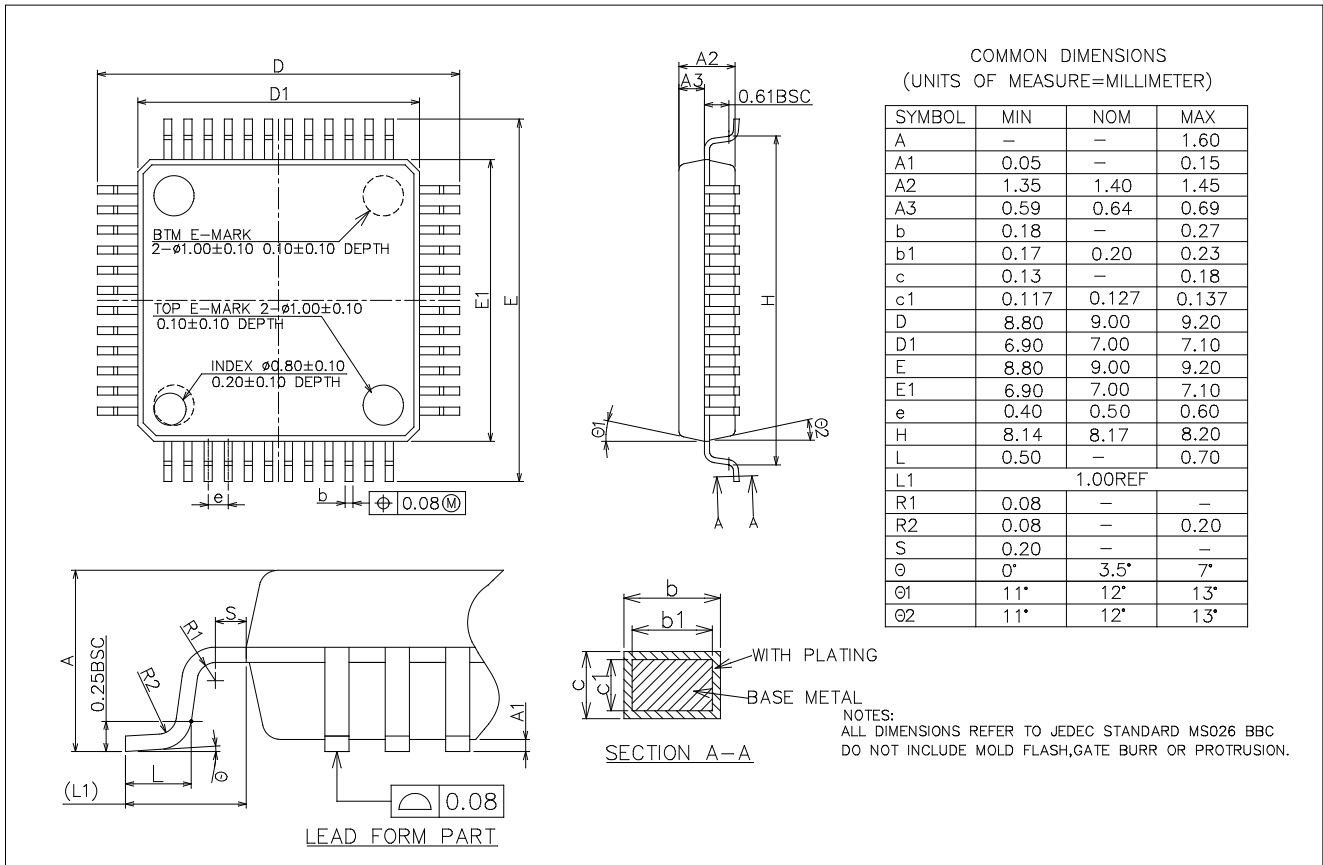


3.2 LQFP48 Package

3.2.1 LQFP48 Pin Assignment

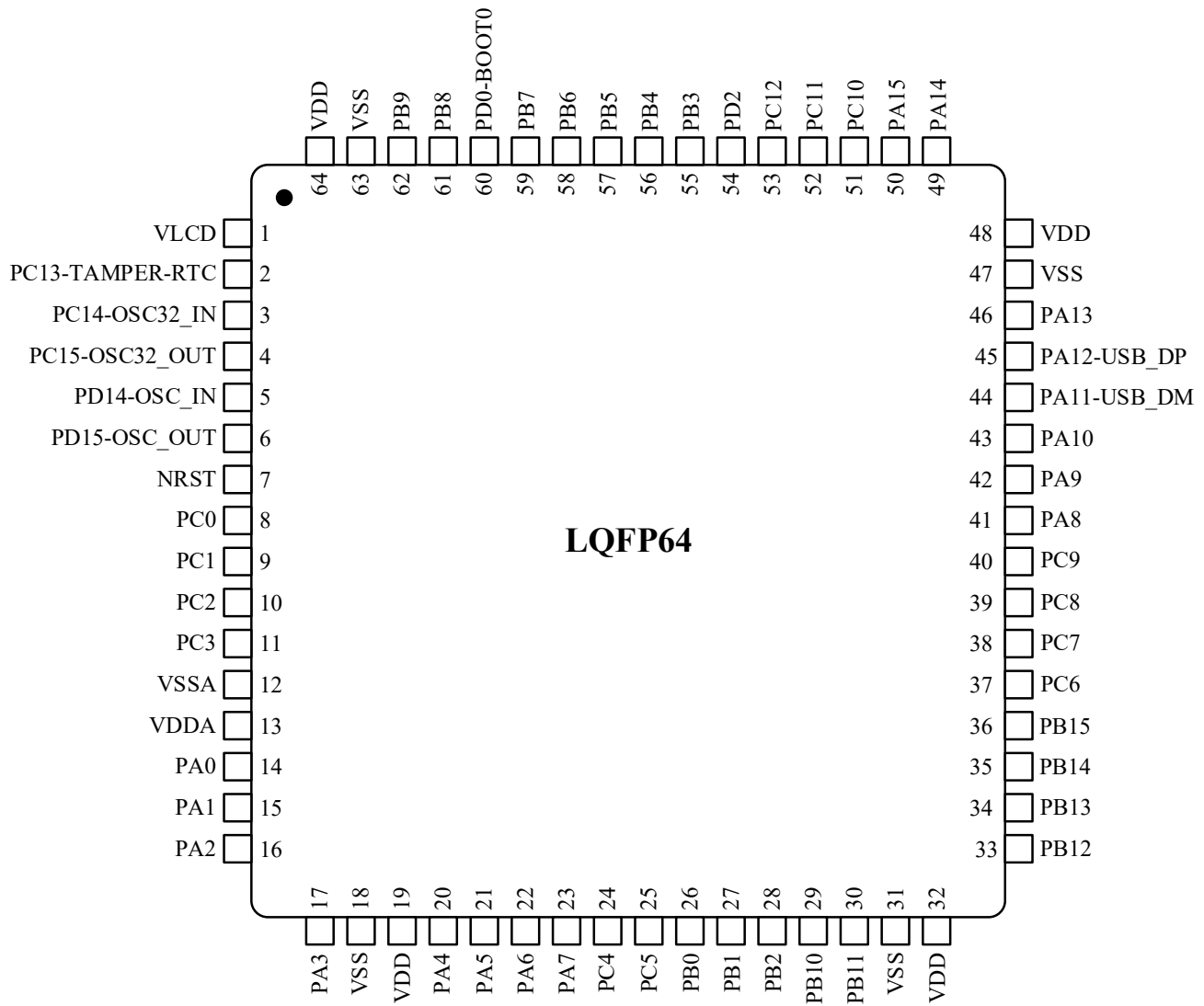


3.2.2 LQFP48(7mm x 7mm) Package Dimensions

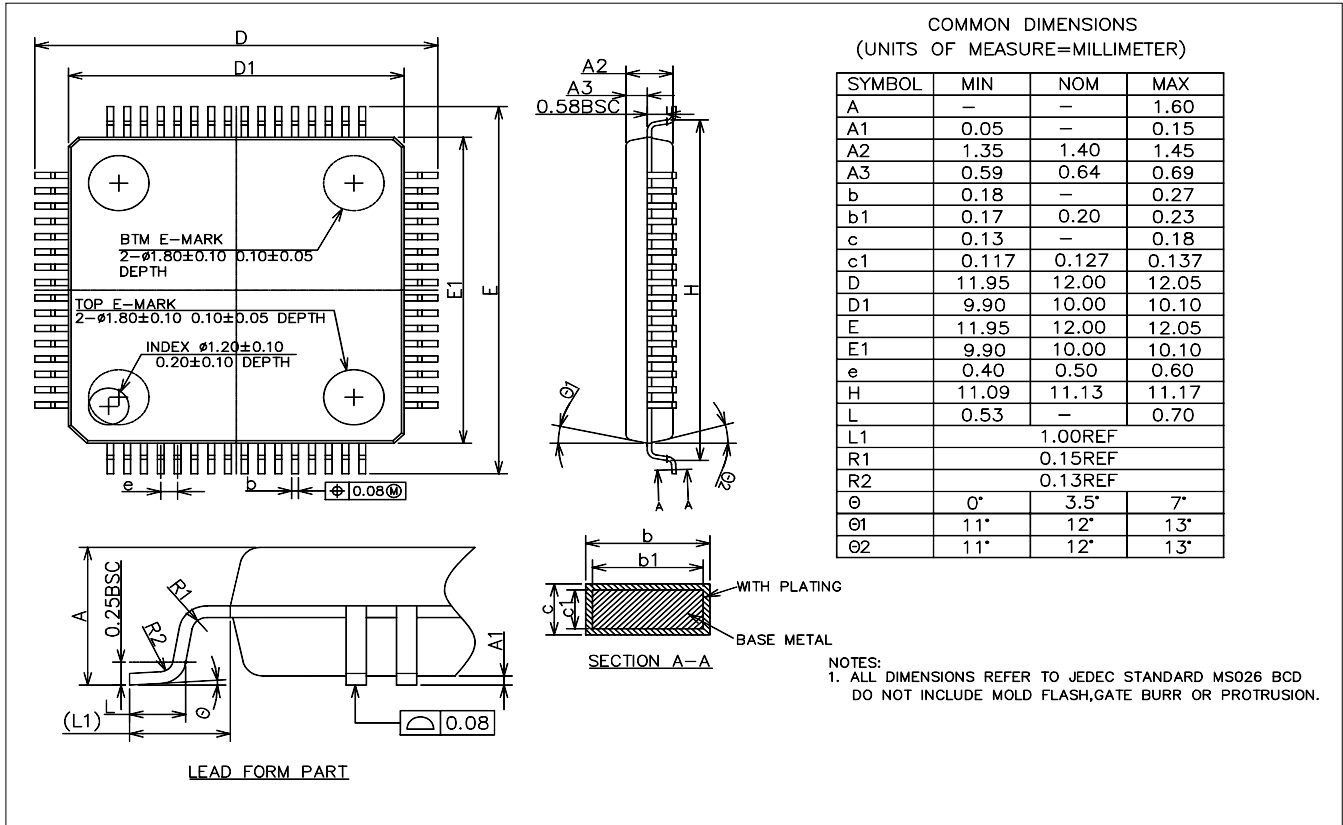


3.3 LQFP64 Package

3.3.1 LQFP64 Pin Assignment

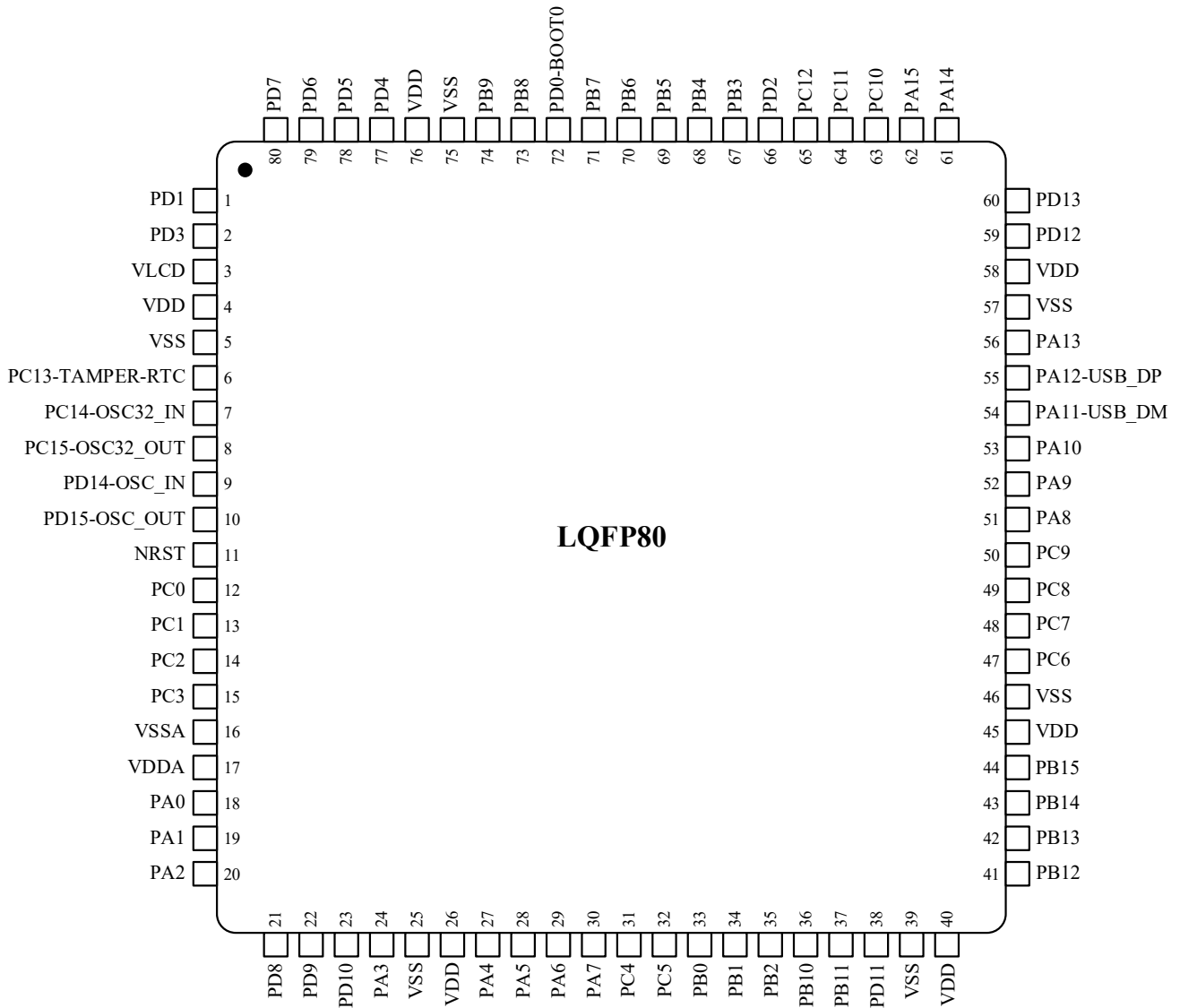


3.3.2 LQFP64(10mm x 10mm) Package Dimensions

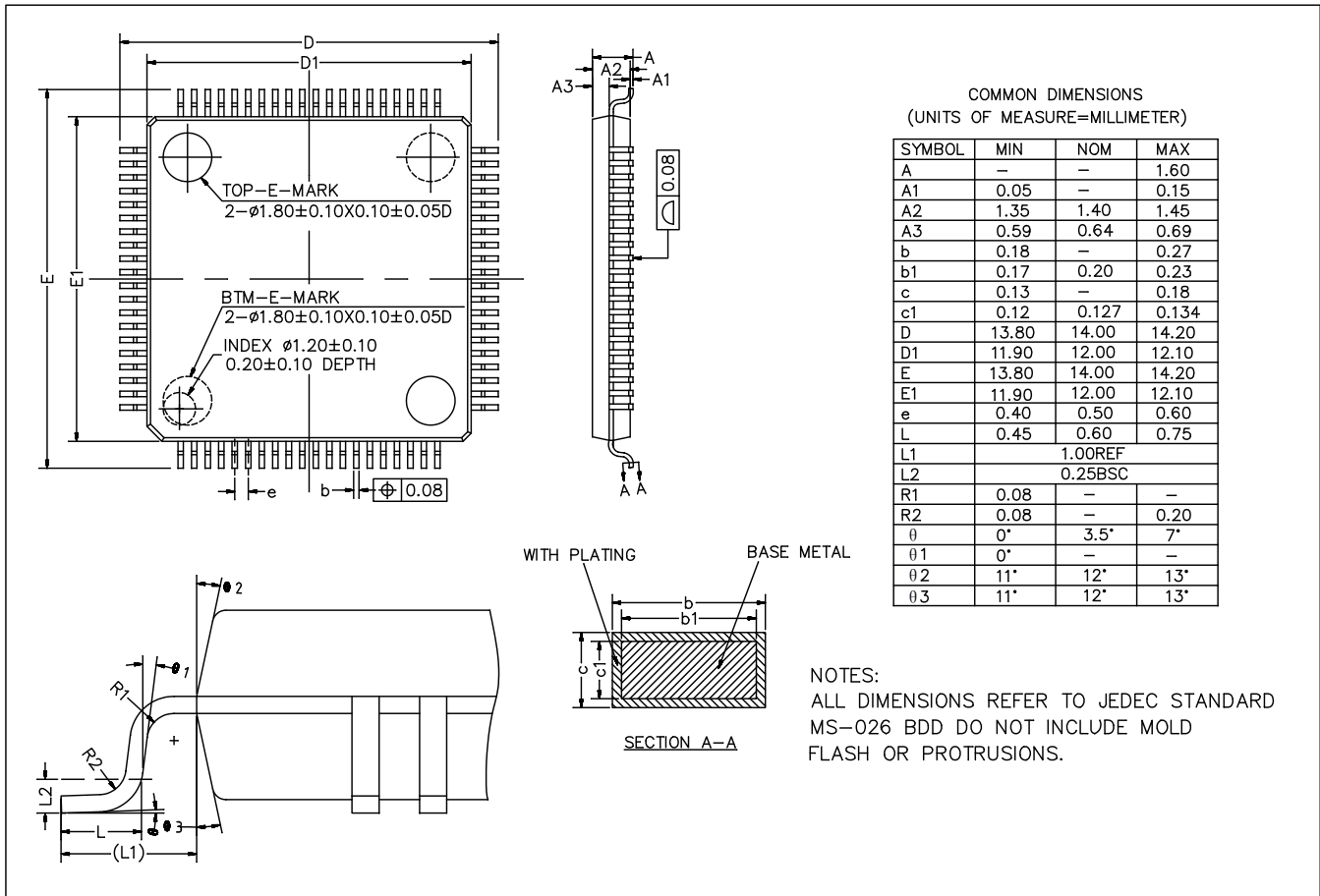


3.4 LQFP80 Package

3.4.1 LQFP80 Pin Assignment



3.4.2 LQFP80(12mm x 12mm) Package Dimensions



4 Version History

Version	Date	Changes
V1.0	2020.7.1	Initial release
V1.2	2021.4.14	1. Update the product model resource configuration 2. Update the LCD version difference description
V1.3	2021.7.6	Modify the description of low power

5 Disclaimer

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