User Guide

How to use the LSE clock security system to improve clock system robustness

Introduction

The purpose of this document is to help users understand the security monitoring function of LSE clocks, improve the robustness of the clock system, improve solution security performance, and reducing the development time and complexity.

This document is only applicable to NSING MCU products. Currently, the supported product include N32L43x, N32L40x, and N32G43x series.

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Content

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1 Introduction

1.1 Overview

In some application scenarios, LSE failures may occur. Here, a method is proposed to use LSE-CSS to monitor LSE failures. When a failure occurs, the system clock can be switched from LSE to LSI, avoid the LSE failure causing the system stop running.

1.2 Introduction to LSE Clocks

The LSE crystal is a 32.768KHz low-speed external crystal or ceramic resonator. It provides a low-power and accurate clock source for real-time clocks or other timing functions. The LSE crystal is enabled and disabled by setting the LSEEN bit in the Low Power Domain Control Register (RCC_LDCTRL). The LSERD in the Low Power Domain Control Register (RCC_LDCTRL) indicates whether the LSE crystal oscillator is stable. During the startup phase, the LSE clock signal is not released until this bit is set by hardware. If enabled in the clock interrupt register (RCC_CLKINT), an interrupt request can be generated.

1.3 Introduction to LSI Clocks

The LSI RC can provide clocks for IWDG and AWU in the STOP2 and STANDBY mode. The LSI clock frequency is about 40KHz. The LSI RC can be enabled or disabled by the LSIEN bit in the Control/Status register (RCC_CTRLSTS). The LSIRD bit in the Control/Status register (RCC_CTRLSTS) indicates whether the low-speed internal oscillator is stable. During the startup phase, the clock is not released until this bit is set by hardware. If enabled in the clock interrupt register (RCC_CLKINT), an LSI interrupt request can be generated.

1.4 Introduction to LSE Clock Security System (LSECSS)

The LSE clock security system is activated by enabling the LSECLKSSEN bit in the Low Power Domain Control Register (RCC_LDCTRL). The LSECLKSSEN bit can be cleared by a hardware reset or RTC software reset or after detection of an LSE fault. When the LSE and LSI are enabled and ready, the LSECLKSSEN bit must be enabled after configuring the RTCSEL to select the RTC clock source. If an LSE failure is detected, LSE will no longer be provided to the RTC, but the RTCSEL bits will not be modified by hardware to switch the RTC clock source. In STANDBY mode, an LSE clock failure will trigger a wakeup. In other modes, an interrupt can be generated to wakeup, and then software can clear the LSECLKSSEN bit and turn off the LSE, and changing the clock source of the RTC, and other measures to ensure application security. The frequency of the LSE oscillator must be higher than 30KHz to prevent LSECSS false detection.

1.5 Applicability

This Demo is only applicable to N32L43x, N32L40x, N32G43x series MCU, supports KEIL5 platform.

[SDK-VER 1.1.0]

Release Date: 2021-11-30

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2 Hardware Environment

2.1 Demo Function

This demo mainly shows the developer how to switch the peripheral clock source to the LSI when the LSE fails, the system monitors the LSE clock, waits for the LSE to recover, and then switches the peripheral clock source from the LSI to the LSE.

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2.2 Hardware Platform

Figure 2–1 Hardware Platform

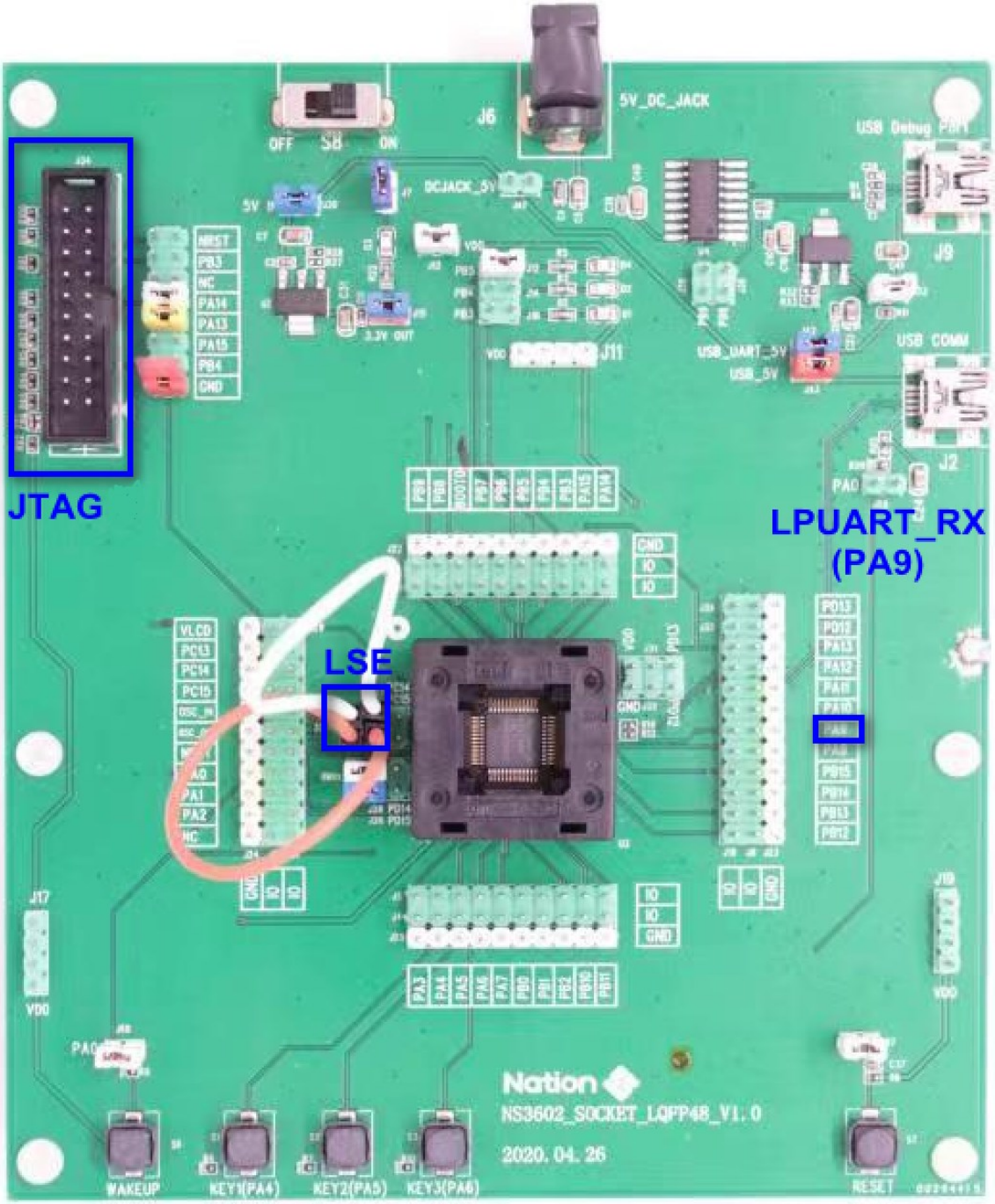

Table 2-1 Hardware List

No.	Resource	Illustrate	Remark
1	NS3602_SOCKET_LQFP48_V1.0	Nations LQFP48 package test socket	

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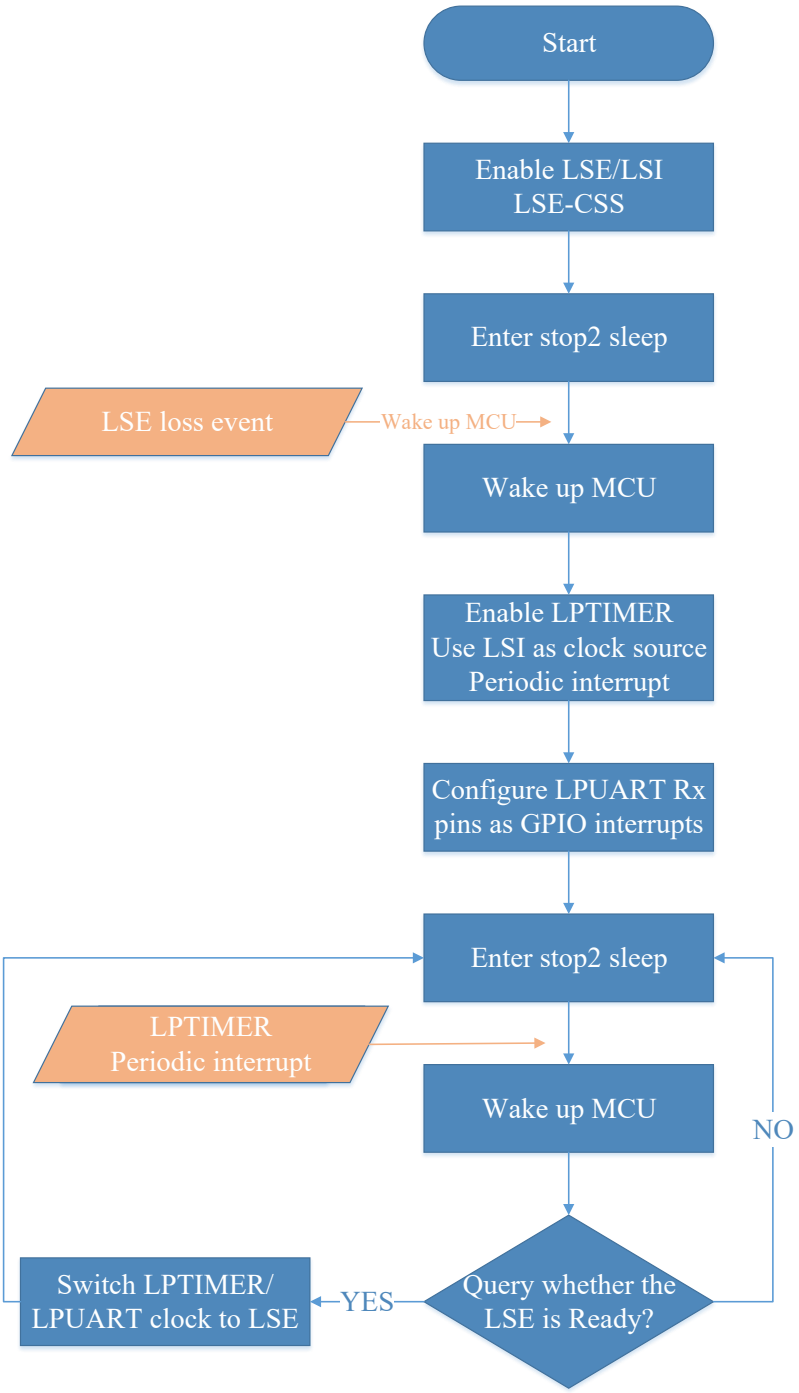
2	N32G435CBL7	MCU	

3 Demo Explain

3.1 Demo Process

Figure 3–1 Demo Flowchart



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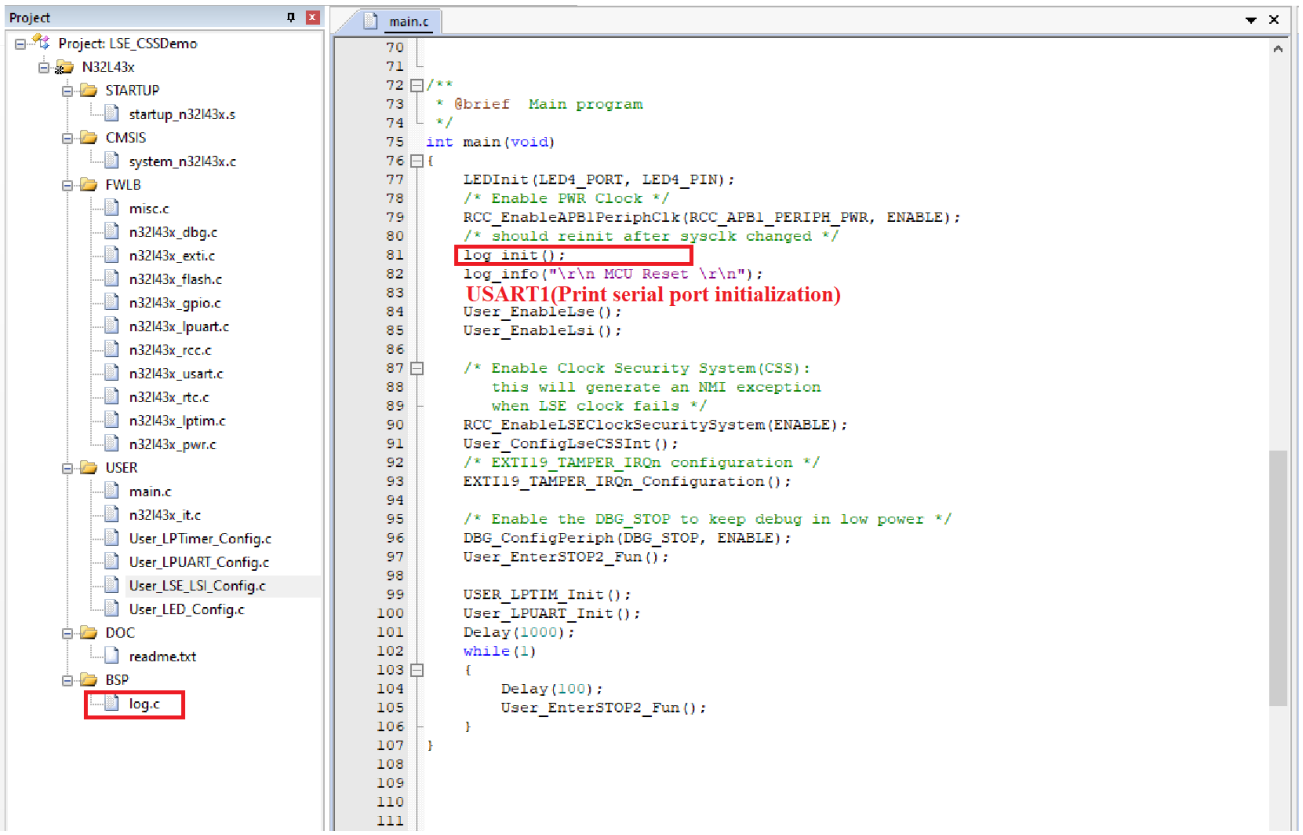
3.2 Demo Analyze

3.2.1 USART1 Log Serial Port Initialization

Figure 3–2 USART1 Serial Port Initialiaztion



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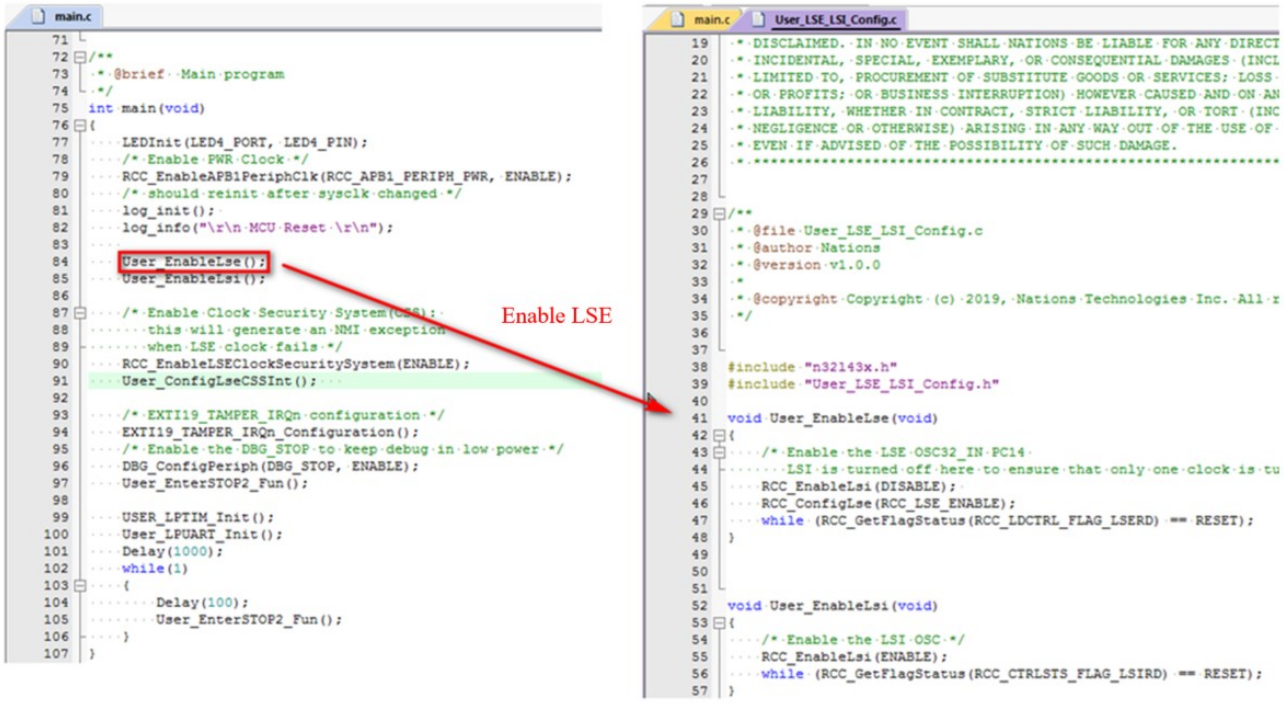
3.2.2 Enable LSE

Figure 3–3 User_EnableLse() Function



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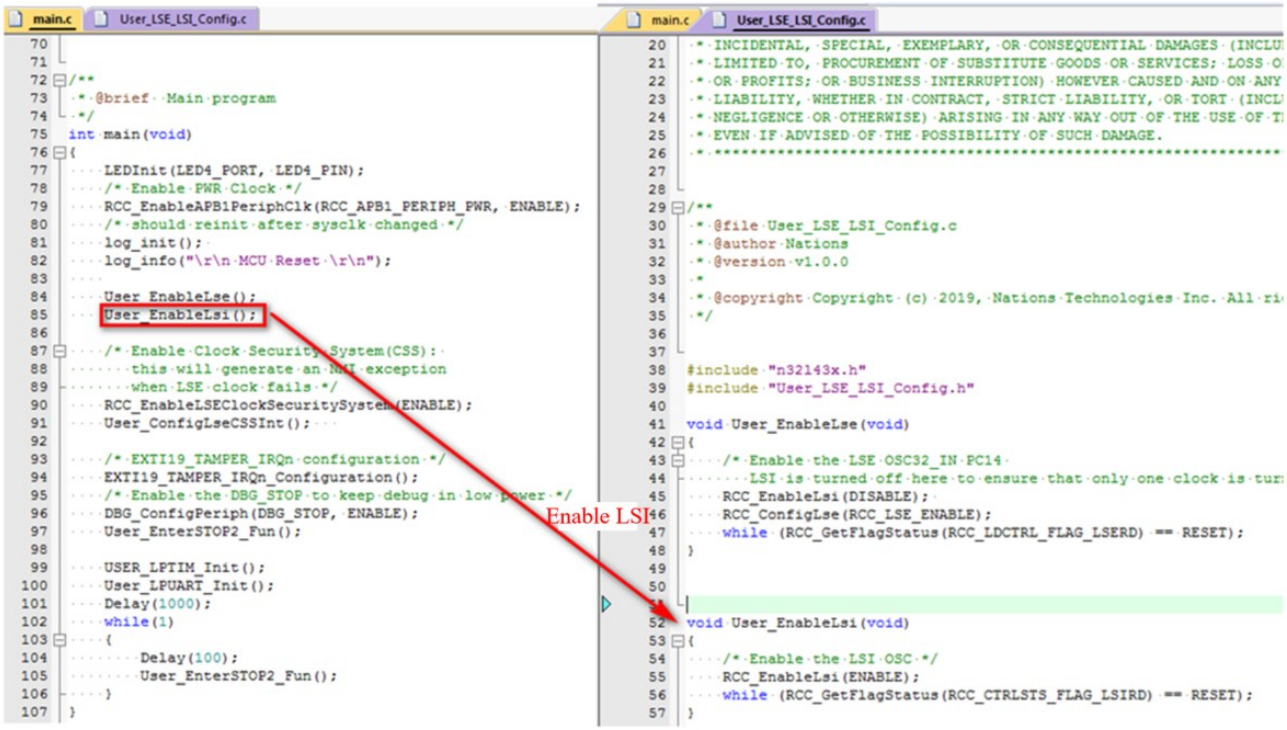
3.2.3 Enable LSI

Figure 3–4 User_EnableLsi() Function



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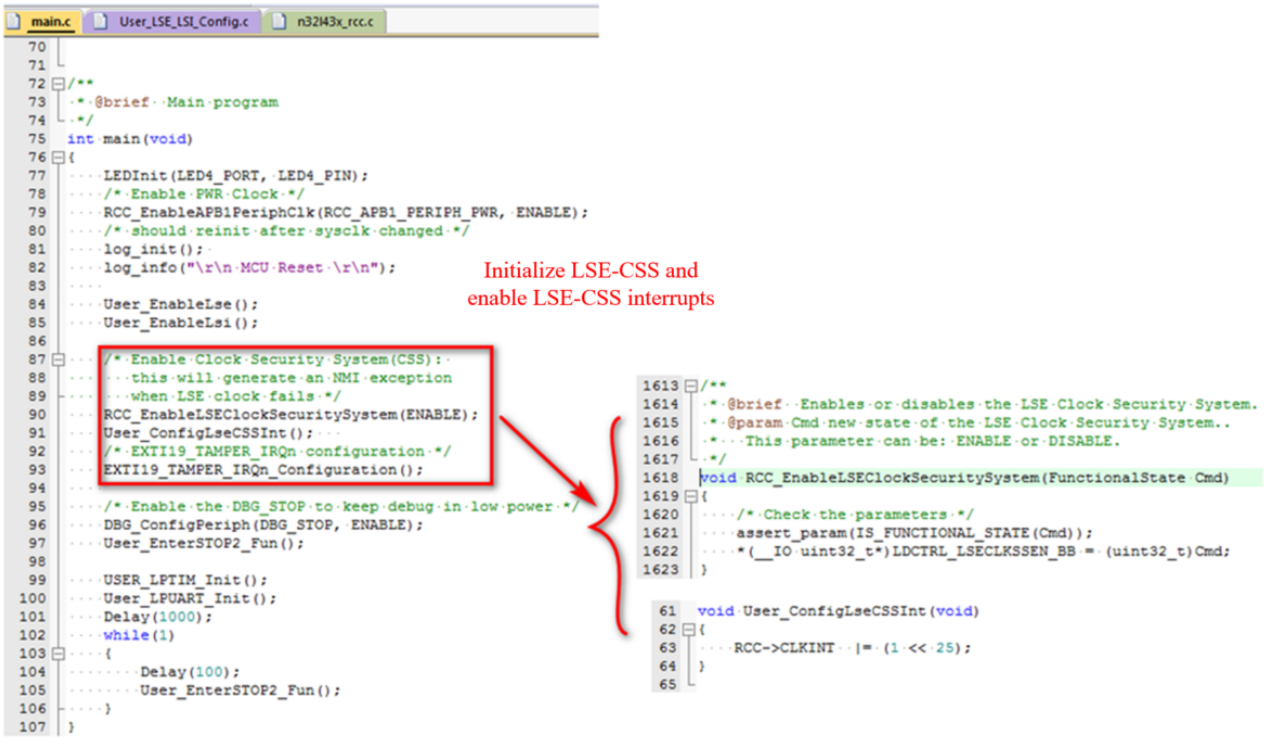
3.2.4 Enable LSE-CSS Monitor

Figure 3–5 RCC_EnableLSEClockSecuritySystem() Function




```c
/**
  * @brief  Main program
  */
int main(void)
{
    LEDInit(LED4_PORT, LED4_PIN);
    /* Enable PWR Clock */
    RCC_EnableAPB1PeriphClk(RCC_APB1_PERIPH_PWR, ENABLE);
    /* should reinit after sysclk changed */
    log_init();
    log_info("\r\n MCU Reset \r\n");

    User_EnableLse();
    User_EnableLsi();

    /* Enable Clock Security System(CSS):
       this will generate an NMI exception
       when LSE clock fails */
    RCC_EnableLSEClockSecuritySystem(ENABLE);
    User_ConfigLseCSSInt();
    /* EXTI19_TAMPER_IRQn configuration */
    EXTI19_TAMPER_IRQn_Configuration();

    /* Enable the DBG_STOP to keep debug in low power */
    DBG_ConfigPeriph(DBG_STOP, ENABLE);
    User_EnterSTOP2_Fun();

    USER_LPTIM_Init();
    User_LPUART_Init();
    Delay(1000);
    while(1)
    {
        Delay(100);
        User_EnterSTOP2_Fun();
    }
}
```

```c
/**
  * @brief  Enables or disables the LSE Clock Security System.
  * @param Cmd new state of the LSE Clock Security System..
  *   This parameter can be: ENABLE or DISABLE.
  */
void RCC_EnableLSEClockSecuritySystem(FunctionalState Cmd)
{
    /* Check the parameters */
    assert_param(IS_FUNCTIONAL_STATE(Cmd));
    *(__IO uint32_t*)LDCTRL_LSECLKSSEN_BB = (uint32_t)Cmd;
}
```

```c
void User_ConfigLseCSSInt(void)
{
    RCC->CLKINT |= (1 << 25);
}
```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3.2.5 Enter STOP2

Figure 3–6 User_EnterSTOP2_Fun() Function

main.c

```
65      /* Request to enter STOP2 mode*/
66      PWR_EnterSTOP2Mode(PWR_STOPENTRY_WFI, PWR_CTRL3_RAM1RET);
67      log_info("\n MCU Wakeup From STOP2 Mode \n");
68  }
69
70
71
72  /**
73    * @brief  Main program
74    */
75  int main(void)
76  {
77      LEDInit(LED4_PORT, LED4_PIN);
78      /* Enable PWR Clock */
79      RCC_EnableAPB1PeriphClk(RCC_APB1_PERIPH_PWR, ENABLE);
80      /* should reinit after sysclk changed */
81      log_init();
82      log_info("\r\n MCU Reset \r\n");
83
84      User_EnableLse();
85      User_EnableLsi();
86
87      /* Enable Clock Security System(CSS):
88         this will generate an NMI exception
89         when LSE clock fails */
90      RCC_EnableLSEClockSecuritySystem(ENABLE);
91      User_ConfigLseCSSInt();
92      /* EXTI19_TAMPER_IRQn configuration */
93      EXTI19_TAMPER_IRQn_Configuration();
94
95      /* Enable the DBG_STOP to keep debug in low power */
96      DBG_ConfigPeriph(DBG_STOP, ENABLE);
97      User_EnterSTOP2_Fun();
98
99      USER_LPTIM_Init();
100     User_LPUART_Init();
101     Delay(1000);
102     while(1)
103     {
104         Delay(100);
105         User_EnterSTOP2_Fun();
106     }
107 }
```

Enter stop2 sleep mode

```
62  void User_EnterSTOP2_Fun(void)
63  {
64      log_info("\r\n MCU Goto STOP2 Mode \n");
65      /* Request to enter STOP2 mode*/
66      PWR_EnterSTOP2Mode(PWR_STOPENTRY_WFI, PWR_CTRL3_RAM1RET);
67      log_info("\n MCU Wakeup From STOP2 Mode \n");
68  }
```


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3.2.6 Initialize LPTIM and LPUART

Figure 3–7 USER_LPTIM_Init() and User_LPUART_Init() Function


```c
/**
  * @brief  Main program
  */
int main(void)
{
    LEDInit(LED4_PORT, LED4_PIN);
    /* Enable PWR Clock */
    RCC_EnableAPB1PeriphClk(RCC_APB1_PERIPH_PWR, ENABLE);
    /* should reinit after sysclk changed */
    log_init();
    log_info("\r\n MCU Reset \r\n");

    User_EnableLse();
    User_EnableLsi();

    /* Enable Clock Security System(CSS):
       this will generate an NMI exception
       when LSE clock fails */
    RCC_EnableLSEClockSecuritySystem(ENABLE);
    User_ConfigLseCSSInt();
    /* EXTI19_TAMPER_IRQn configuration */
    EXTI19_TAMPER_IRQn_Configuration();

    /* Enable the DBG_STOP to keep debug in low power */
    DBG_ConfigPeriph(DBG_STOP, ENABLE);
    User_EnterSTOP2_Fun();

    USER_LPTIM_Init();
    User_LPUART_Init();
    Delay(1000);
    while(1)
    {
        Delay(100);
        User_EnterSTOP2_Fun();
    }
}
```

```c
void User_LPUART_Init(void)
{
    LPUART_InitType LPUART_InitStructure;
    /* Configure the GPIO ports */
    GPIO_Configuration();

    /* System Clocks Configuration */
    RCC_Configuration(RCC_LPUARTCLK_SRC_LSE);

    /* LPUART configuration */
    LPUART_DeInit();
    LPUART_StructInit(&LPUART_InitStructure);
    LPUART_InitStructure.BaudRate            = 9600;
    LPUART_InitStructure.Parity              = LPUART_PE_NO;
    LPUART_InitStructure.RtsThreshold        = LPUART_RTSTH_FIFOFU;
    LPUART_InitStructure.HardwareFlowControl = LPUART_HFCTRL_NONE;
    LPUART_InitStructure.Mode                = LPUART_MODE_RX | LPUART_MODE_TX;
    /* Configure LPUART */
    LPUART_Init(&LPUART_InitStructure);
}
```

```c
void USER_LPTIM_Init(void)
{
    /* Enable interrupt   */
    LPTIMNVIC_Config(ENABLE);
    RCC_ConfigLPTIMClk(RCC_LPTIMCLK_SRC_LSE);
    RCC_EnableRETPeriphClk(RCC_RET_PERIPH_LPTIM,ENABLE);

    LPTIM_SetPrescaler(LPTIM,LPTIM_PRESCALER_DIV4);
    LPTIM_EnableIT_CMPM(LPTIM);
    /* config lptim ARR and compare register */
    LPTIM_Enable(LPTIM);
    LPTIM_SetAutoReload(LPTIM,65000);
    LPTIM_SetCompare(LPTIM,60000);
    LPTIM_StartCounter(LPTIM,LPTIM_OPERATING_MODE_CONTINUOUS);
}
```


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4 User Guide

4.1 Reset MCU

Figure 4–1 Reset MCU

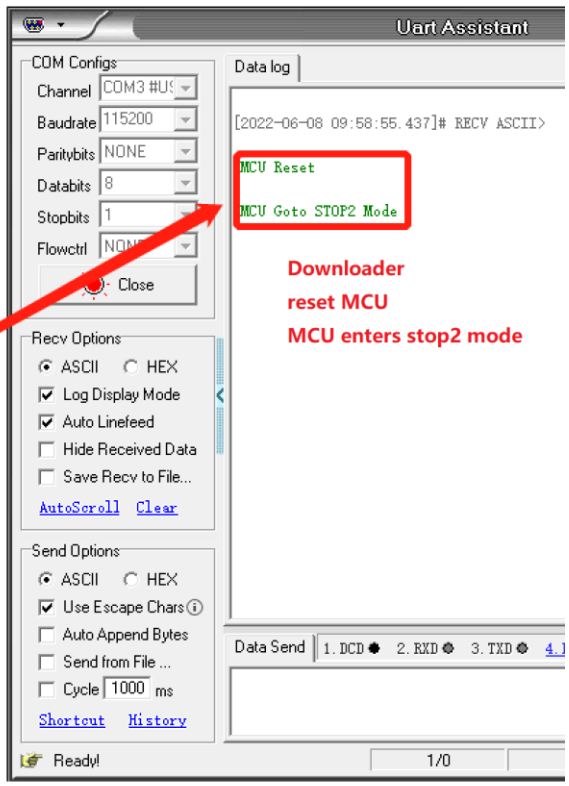
```
/**
  * @brief  Main program
  */
int main(void)
{
    LEDInit(LED4_PORT, LED4_PIN);
    /* Enable PWR Clock */
    RCC_EnableAPB1PeriphClk(RCC_APB1_PERIPH_PWR, ENABLE);
    /* should reinit after sysclk changed */
    log_init();
    log_info("\r\n MCU Reset \r\n");

    User_EnableLse();
    User_EnableLsi();

    /* Enable Clock Security System(CSS):
       this will generate an NMI exception
       when LSE clock fails */
    RCC_EnableLSEClockSecuritySystem(ENABLE);
    User_ConfigLseCSSInt();
    /* EXTI19_TAMPER_IRQn configuration */
    EXTI19_TAMPER_IRQn_Configuration();

    /* Enable the DBG_STOP to keep debug in low power */
    DBG_ConfigPeriph(DBG_STOP, ENABLE);
    User_EnterSTOP2_Fun();

    USER_LPTIM_Init();
    User_LPUART_Init();
    Delay(1000);
    while(1)
    {
        Delay(100);
        User_EnterSTOP2_Fun();
    }
}
```



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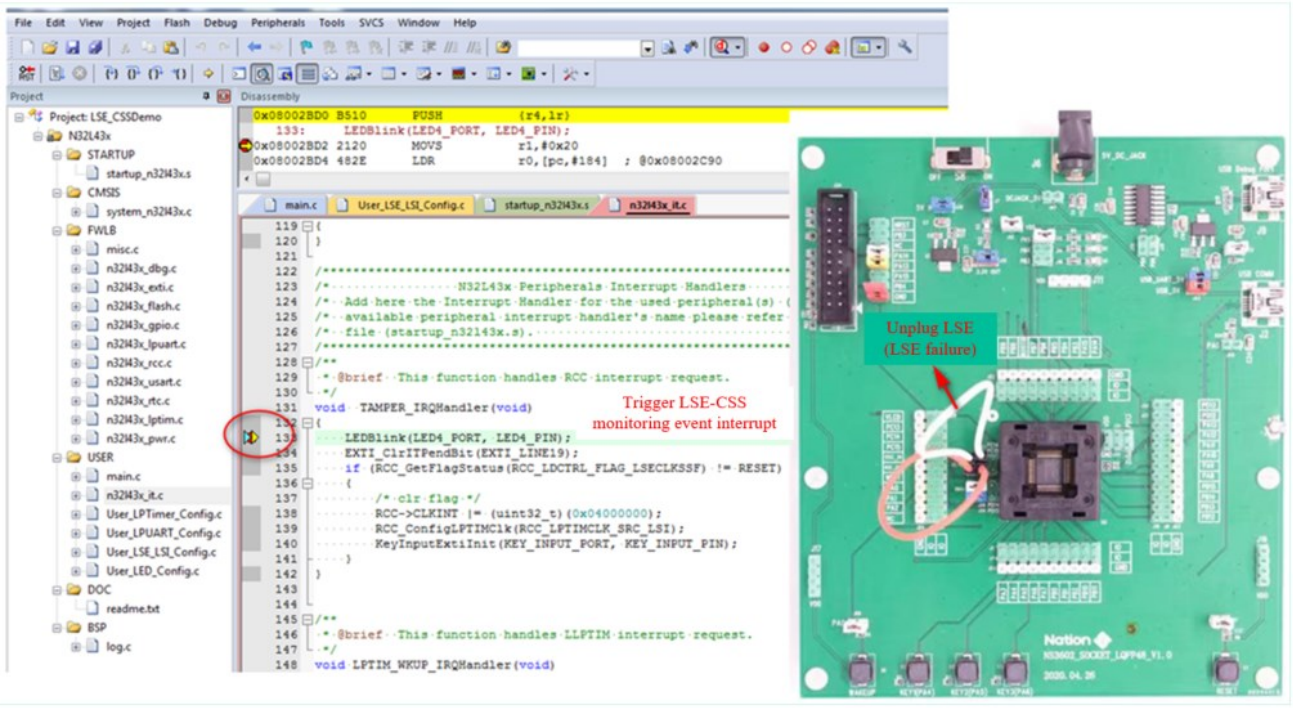
4.2 Generate LSE Fault

Figure 4–2 Generate LSE Fault



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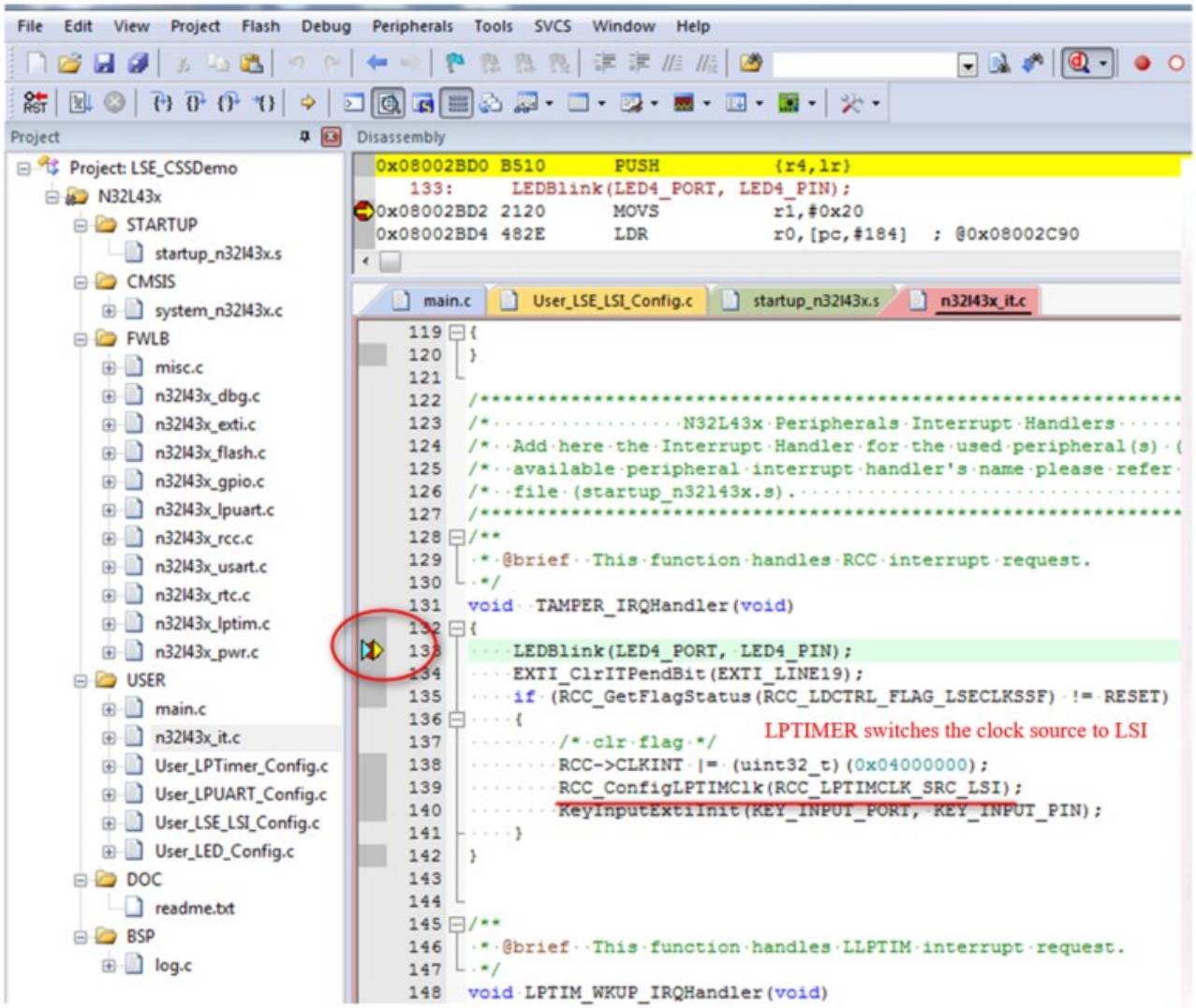
4.3 LPTIMER Switch Clock Source

Figure 4–3 LPTIMER Switch Clock Source



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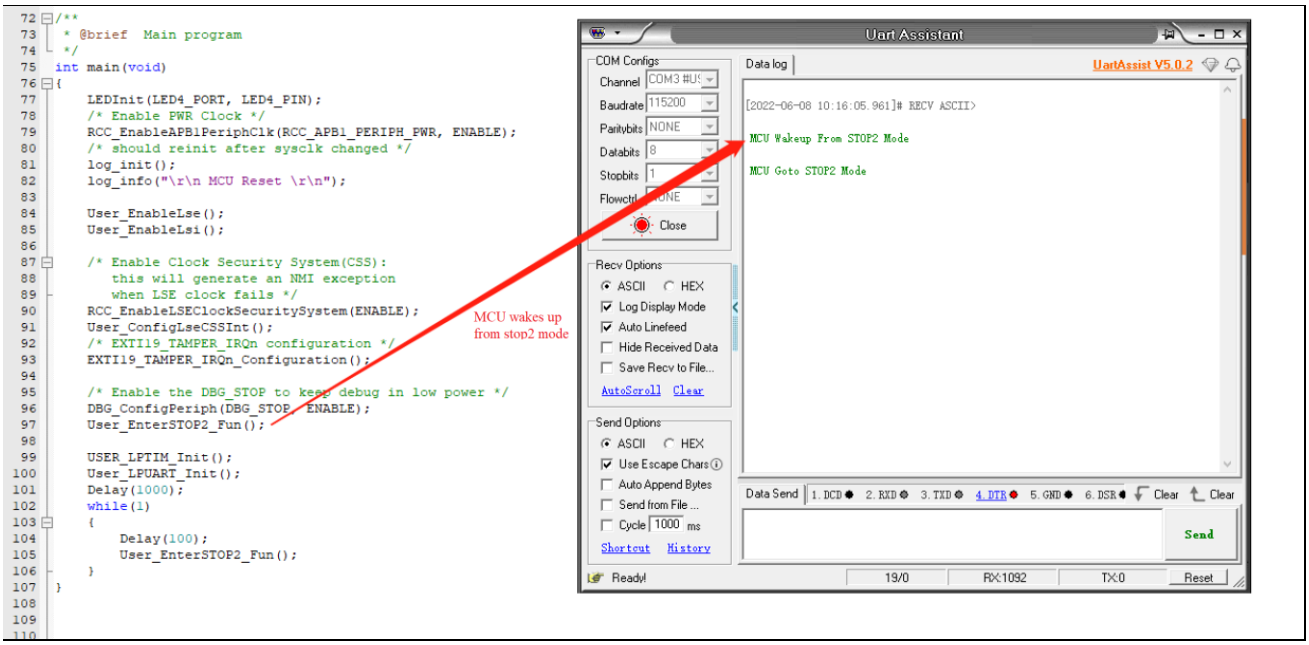
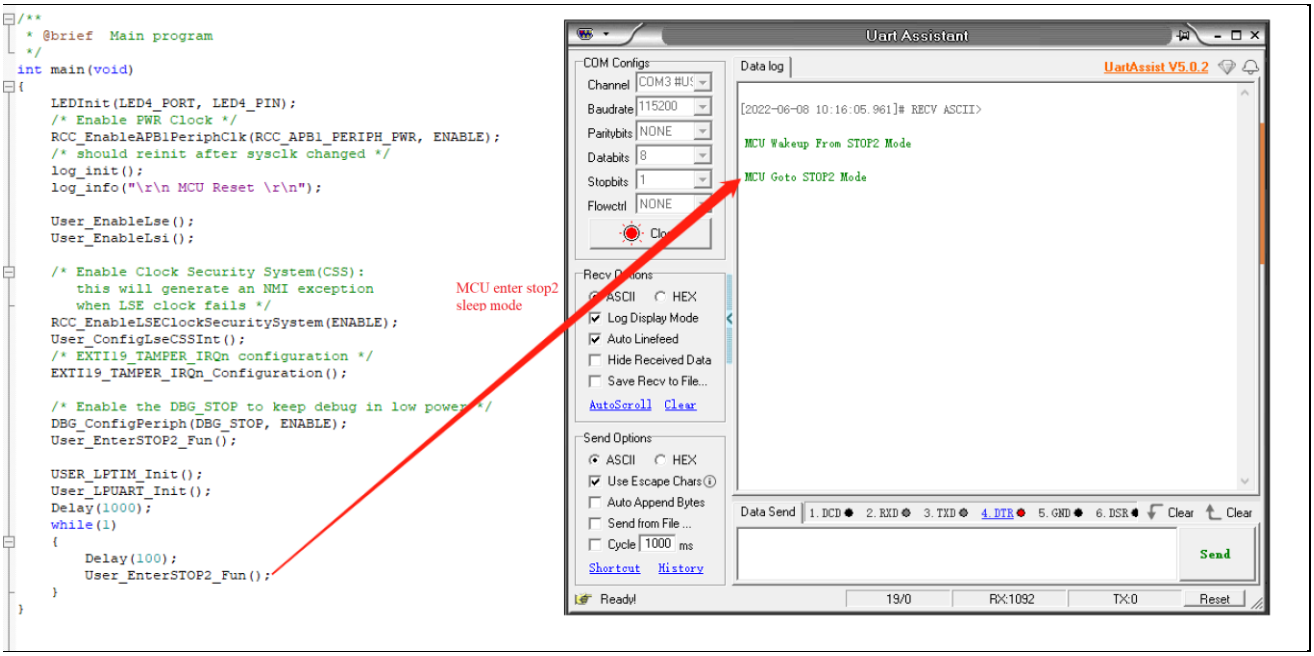
4.4 MCU Wakes Up From STOP2

Figure 4–4 MCU Wake Up from STOP2 Mode



4.5 MCU Enter STOP2 Sleep Mode

Figure 4–5 MCU Enter STOP2 Mode



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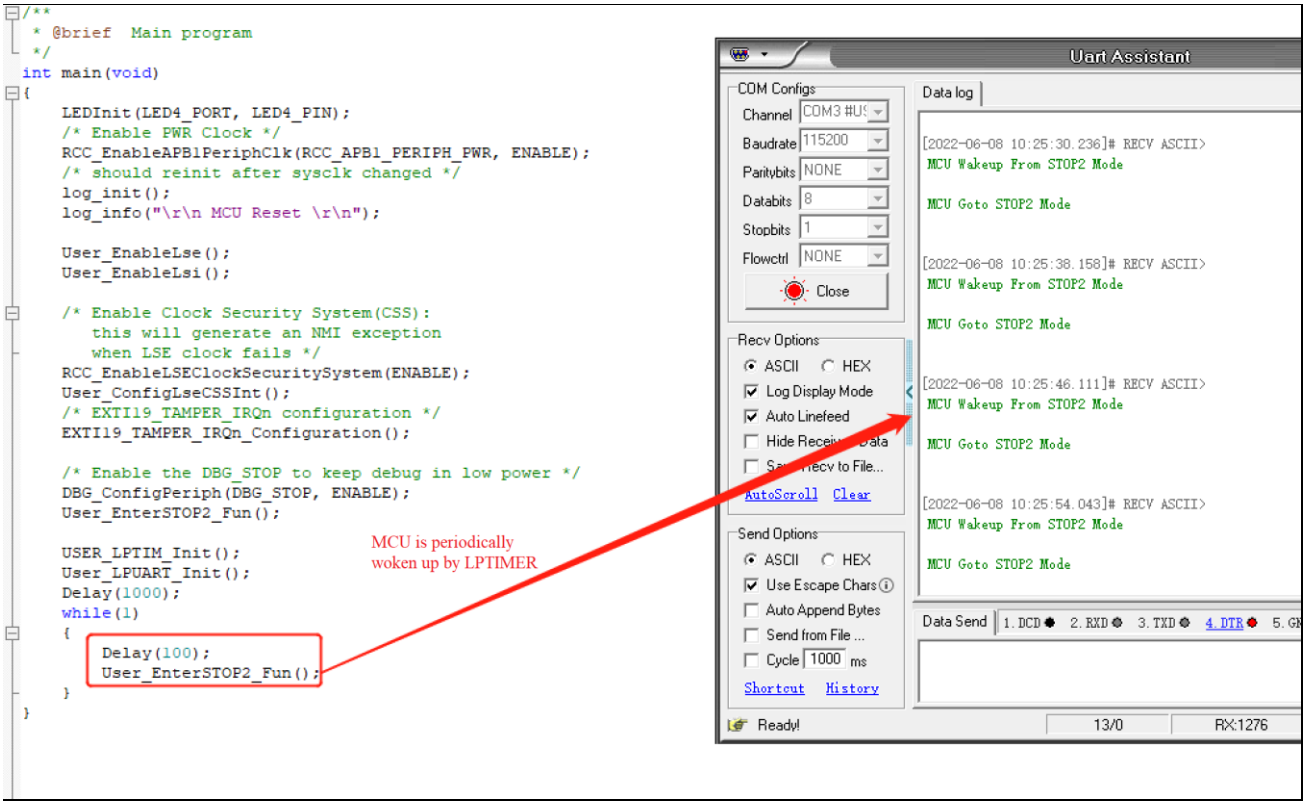
4.6 MCU Periodically Woken Up

Figure 4–6 MCU Periodically Woken Up



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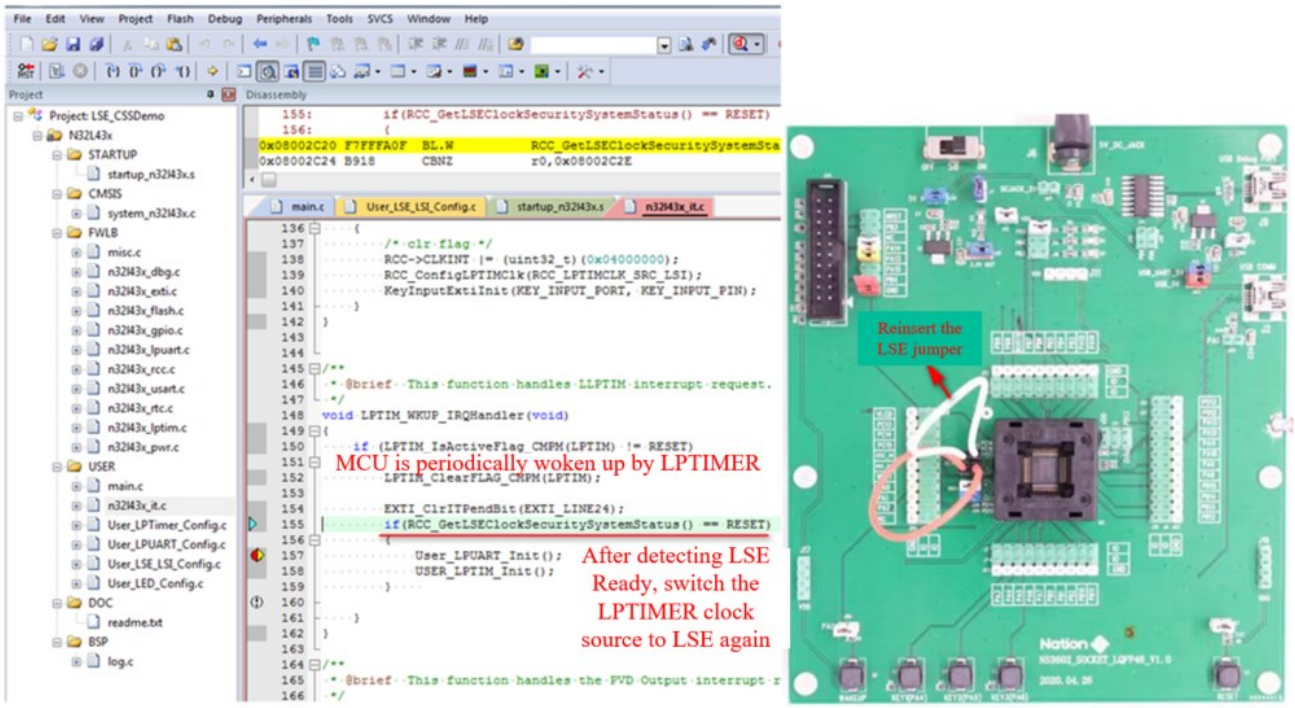
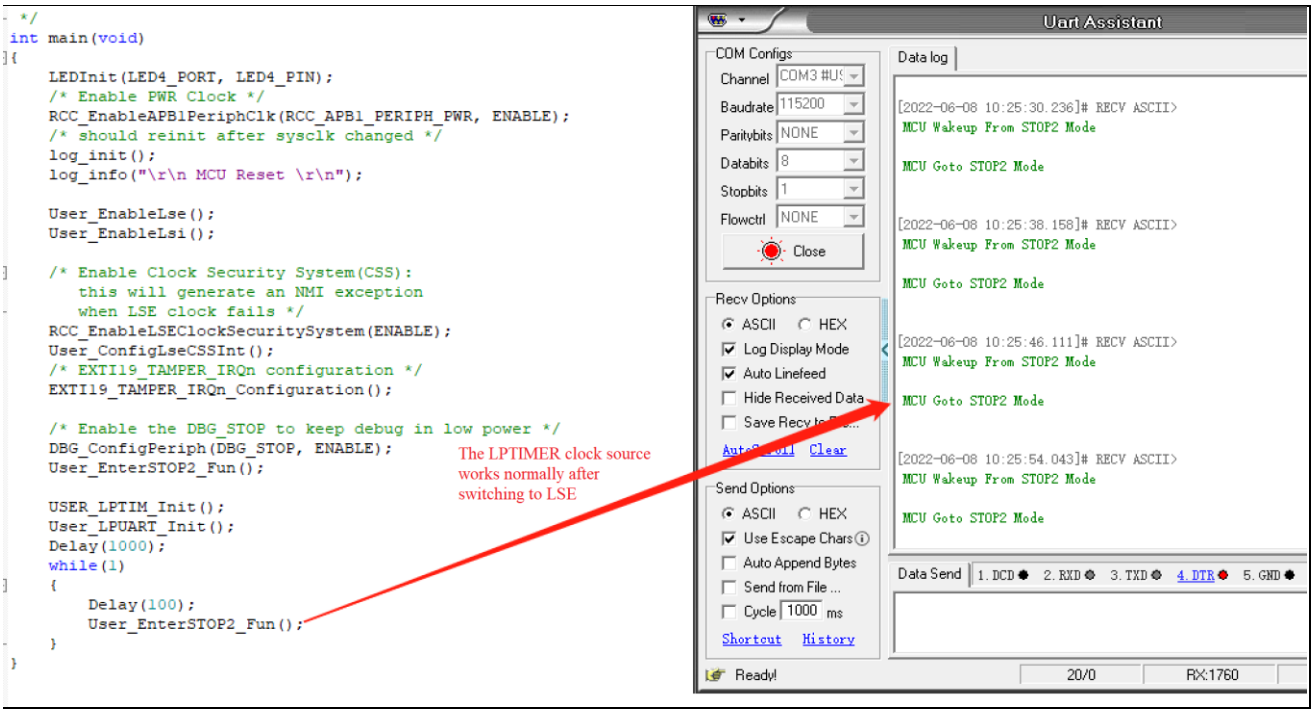
4.7 LSE Recover

Figure 4–7 LSE Recover



4.8 LPTIMER Switches The Clock Source to LSE

Figure 4–8 LPTIMER Switches the Clock Source to LSE



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5 Version History

Version	Date	Changes
V1.0	2020.11.30	Initial release

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