N32L40xx8/xB Product Brief

N32L40x series uses 32-bit ARM Cortex-M4F core, operating frequency up to 64MHz, supporting floating point unit and DSP instructions. The device integrates up to 128KB of encrypted Flash, and up to 24KB of SRAM. The series features rich of high-performance interface, including one Built-in 12bit 4.5Msps ADC, two independent rail-to-rail operational amplifiers, two high-speed comparators, one 1Msps 12bit DAC, multi-channel U(S)ART, I2C, SPI, USB, CAN and other digital communication interfaces, allowing Segment LCD Driver Interface and built-in hardware acceleration engine for cryptographic algorithm

Key Features

- **CPU core**
  - 32-bit ARM Cortex-M4 core with FPU, supporting single-cycle multiplication and hardware divide DSP instructions and MPU.
  - Built-in 2KB instruction Cache supports Flash accelerator unit for zero-wait program execution.
  - Maximum frequency of 64MHz, with 80DMIPS
- **Memories**
  - Up to 128KByte on-chip Flash, supports encrypted storage function, partition management and data protection, supports hardware ECC check, 100,000 erase/write cycles, 10-year data retention.
  - Up to 24KByte of SRAM with hardware parity check, including 16Kbyte SRAM1(Stop2 mode can be configured as retention) and 8 Kbyte SRAM2(both Standby and Stop2 modes can be configured as retention).
- **Low power management**
  - Run mode: 60uA/MHz@64MHz
  - Sleep
  - LP Run mode: PLL off, MSI as the system master clock, MR off, LPR on, USB/CAN/SAC power off, other peripherals are optional
  - LP Sleep
  - Stop2 mode: 3uA, RTC Run, 8KByte SRAM2 retention, CPU register retention, IO retention, fast wake up
  - Standby mode: 1.5uA, all backup registers retention, IO retention, optional RTC Run, 8KByte SRAM2 retention, fast wake up
- **High-performance analog interfaces**
  - 1x 12bit ADC with 4.5Msps,
    - configurable resolution, ,
    - up to 16 external single-ended input channels, supports differential mode
  - 2x rail-to-rail operational amplifiers with built-in 32 times programmable gain amplifier(PGA).
  - 2x high-speed analog comparators with internal 64-level adjustable comparison reference, COMP1 can operate in low-power STOP2 mode
  - 1x 12bit DAC with 1Msps
  - Internal 2.048V reference voltage source
  - Analog voltage operation from 1.8 to 3.6V (VDDA)

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- **Clock**
  - 4MHz~32MHz external high-speed crystal oscillator
  - 32.768KHz external low-speed crystal oscillator
  - Internal high-speed RC(HSI) 16MHz
  - Internal multi-speed RC(MSI) 100K~4MHz
  - Internal low-speed RC(LSI) 40KHz
  - Built-in high-speed PLL
  - Supports 1-channel clock output, configurable as low-speed or high-speed divisional output
- **Reset**
  - Supports power-on, brown-out, and external pin reset
  - Supports watchdog reset, software reset
- **GPIOs.**
  - Up to 64 GPIOs
  - Support multiplexed functions
- **Communication interface**
  - 5x U(S)ART interfaces
    - 3x USART interfaces (support 1xISO7816, 1xIrDA, LIN)
    - 2x UART interfaces
  - 1x LPUART, support waking up MCU from low power stop2 mode.
  - 2x SPI interfaces, the rate is up to 16 Mbps, support I2S communication
  - 2x I2C interfaces, the rate is up to 1 MHz, which can be configured in master/slave mode and support dual address response in slave mode
  - 1x USB2.0 FS Device interface
  - 1x CAN 2.0A/B bus interface
- **Segment LCD driver interface**
  - Supports up to 320 segments (8x40) or 176 segments (4x44) monochrome passive LCD display
  - Flexible LCD refresh rate support (30~102Hz)
  - Supports static, 1/2, 1/3, 1/4, 1/8 duty cycle
  - Supports static, 1/2, 1/3, 1/4 bias
  - Supports normal display in Stop2 mode
- **DMA controller**
  - 1x high-speed DMA controller
  - each controller supports 8 channels
  - channel source and destination addresses can be configured arbitrarily

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- **RTC**
  - supports leap-year perpetual calendar, alarm event, periodic wakeup.
  - supports internal and external clock calibration
- **Timer**
  - 2x 16bit advanced control timers with maximum control precision of 9.25ns,
    - support input capture, complementary output, quadrature encoding input etc.
    - Each timer has 4 independent channels, 3 of which support 6-channel complementary PWM output.
  - 5x 16bit general purpose timers
    - each timer with 4 independent channels
    - support input capture/output comparison /PWM output
  - 2x 16bit basic timers
  - 1x 16bit low power timer, support quadrature encoding and double pulse counting function. it can work in STOP2 mode
  - 1x 24bit SysTick timer
  - 1x 7bit window Watchdog (WWDG)
  - 1x 12bit independent Watchdog (IWDG)
- **Programming method**
  - Supports SWD/JTAG online debugging interface
  - Supports UART and USB Bootloader
- **Security features**
  - Built-in hardware acceleration engine for encryption algorithms
  - Supports AES, DES, TDES, SHA1/224/256, SM1, SM3, SM4, and SM7 algorithms
  - Flash encryption, multi-user partition management (MMU)
  - true random number generator(TRNG)
  - CRC16/32 calculation
  - Supports write protection (WRP), multiple read protection (RDP) levels (L0/L1/L2)
  - Supports secure boot , program encryption download, secure update
  - Supports external clock failure detection, tamper detection
- **96-bit UID and 128-bit UCID**
- **Oprating conditions**
  - Operating voltage range: 1.8V~3.6V
  - Operating temperature range: -40℃ ~ 105℃
  - ESD: ±4KV (HBM model), ±1KV (CDM model)
- **Package**

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- QFN32(4mm x 4mm)
- QFN32(5mm x 5mm)
- QFN48 (6mm x 6mm)
- LQFP48(7mm x 7mm)
- QFN64 (8mm x 8mm)
- LQFP64(10mm x 10mm)
- LQFP80(12mm x 12mm)

- **Order model**

Reference	Part number
N32L402	N32L402C8Q7, N32L402C8L7, N32L402R8L7, N32L402CBQ7, N32L402CBL7, N32L402RBL7
N32L403	N32L403K8Q7, N32L403KBQ7, N32L403KBQ7-1(1)
N32L406	N32L406C8Q7, N32L406R8Q7, N32L406CBL7, N32L406RBL7，N32L406MBL7

Note: (1):The package is QFN32(5mm x 5mm)

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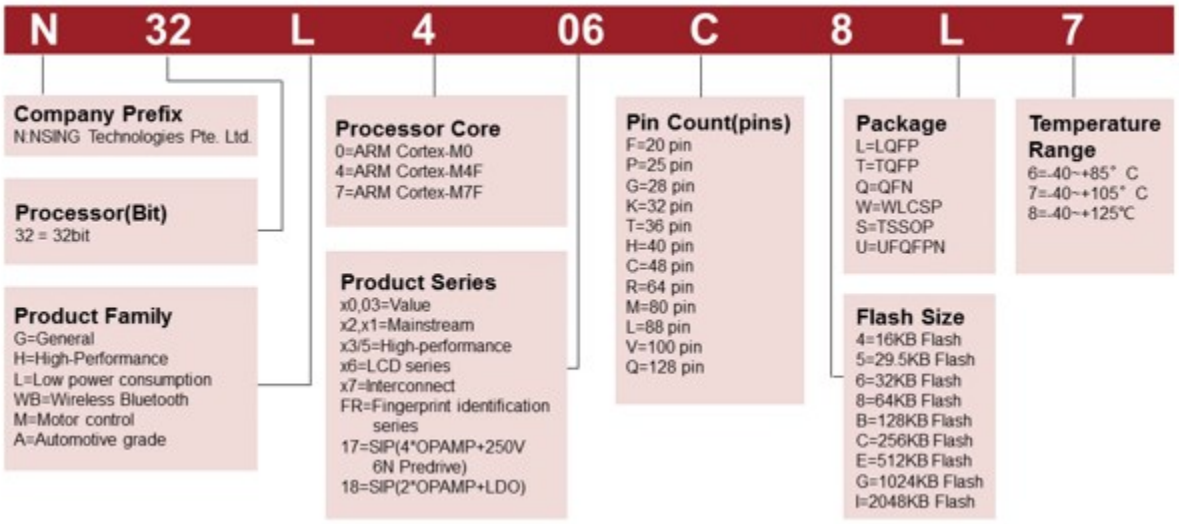
Naming Convention



Product Configurations

Table 2-1 N32L40x series resource configuration

Dvice		N32L402C8/B		N32L402R8/B		N32L403K8/BQ7		N32L403 KBQ7-1[5]	N32L406C8/B		N32L406R8/B		N32L406MB
Flash (KB)		64	128	64	128	64	128	128	64	128	64	128	128
SRAM (KB)		16	16	16	16	16	24	24	16	24	16	24	24
CPU frequency		ARM Cortex-M4F @ 64MHz, 80DMIPS											
Operating Conditions		1.8~3.6V/-40~105℃											
Timer	General	5											
	Advanced	2											
	Basic	2											
	LPTIM	1											
Communication interface	SPI[1]	2		2		2		1	2				
	I2S[1]	2		2		2		1	2				
	I2C	2											
	UART	2											
	USART	3		3		2		2	3				
	LPUART	1											
	USB	1						No[1]	1				
	CAN	No[1]		No[1]		1							
GPIO		38		52		26		29	38		52		64
DMA Number of Channels		1x 8 Channel											
12bit ADC Number of Channels		1x 10Channel		1x 16Channel		1x 10Channel		1x 10Channel	1x 10Channel		1x 16Channel		1x 16Channel
12bit DAC Number of Channels		1x 1 Channel											

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OPAMP/COMP	2/2	2/2	2/2	2/2	2/2	2/2	2/2
Segment LCD	4x20	4x34/8x30(2) (3)	No		4x20	4x34/8x30(2) (3)	4x44/8x40(3)
Algorithm support	DES/TDES, AES, SHA1/SHA224/SHA256, SM1, SM3, SM4, SM7, CRC16/CRC32, TRNG						
Security protection	Read-write protection (RDP/WRP), Storage Encryption, Partition Protection, Secure Boot						
Package	LQFP48/QFN48	LQFP64	QFN32(4)	QFN32(5)	LQFP48/QFN48	LQFP64/QFN64	LQFP80

1. SPI1 and SPI2 interfaces have the flexibility to switch between SPI mode and I2S audio mode.
2. LQFP64/QFN64 package version B chips do not support LCD 1/8 duty cycle mode (8x30).
3. In 1/8 duty cycle mode, B and C chip LCDs do not support 1/4 bias.
4. The package size is QFN32(4mm x 4mm)
5. The package size is QFN32(5mm x 5mm)
6. Note: (1) it is not supported

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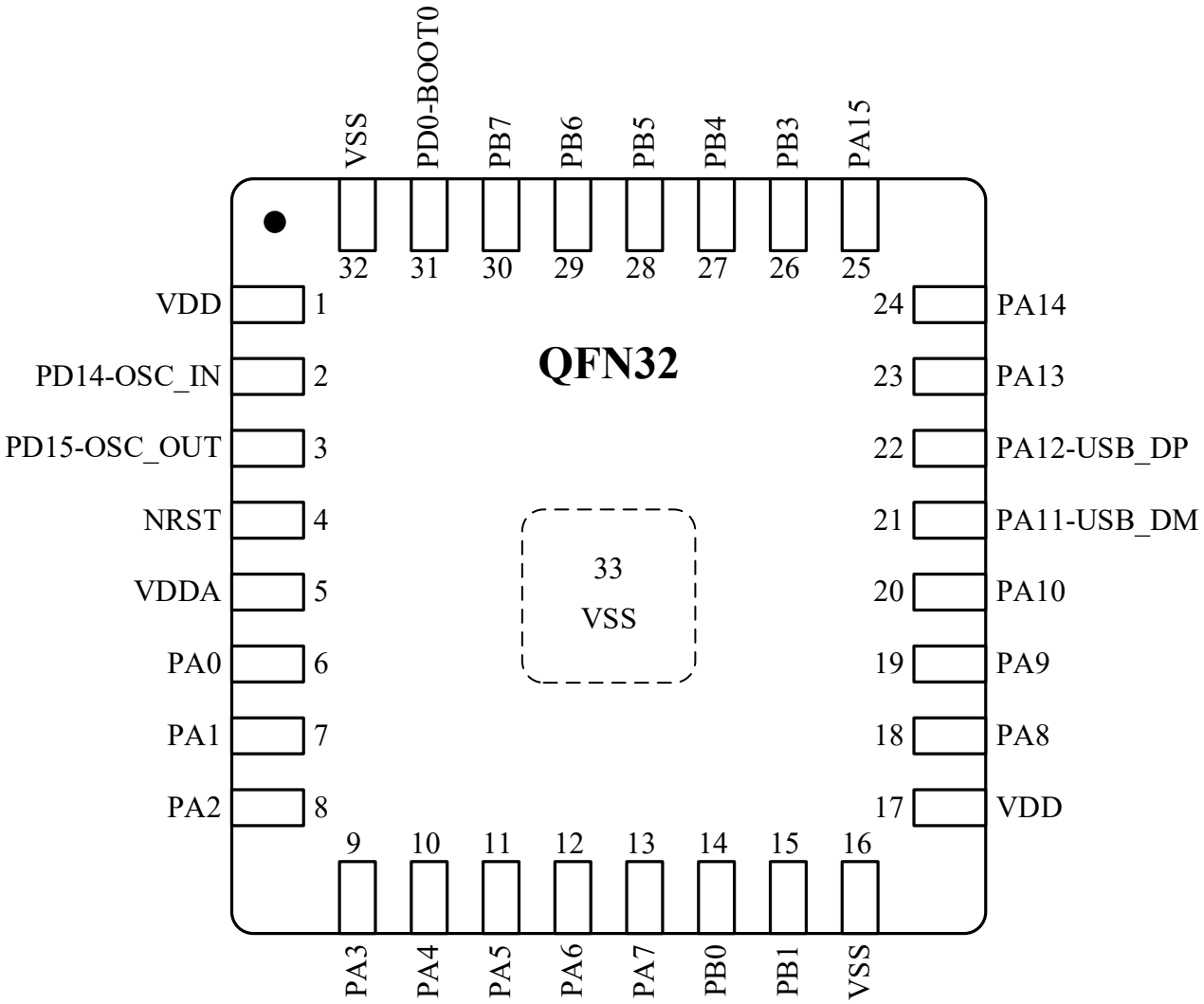
Packages

QFN32 Package

QFN32 (4mm x 4mm) Pinout



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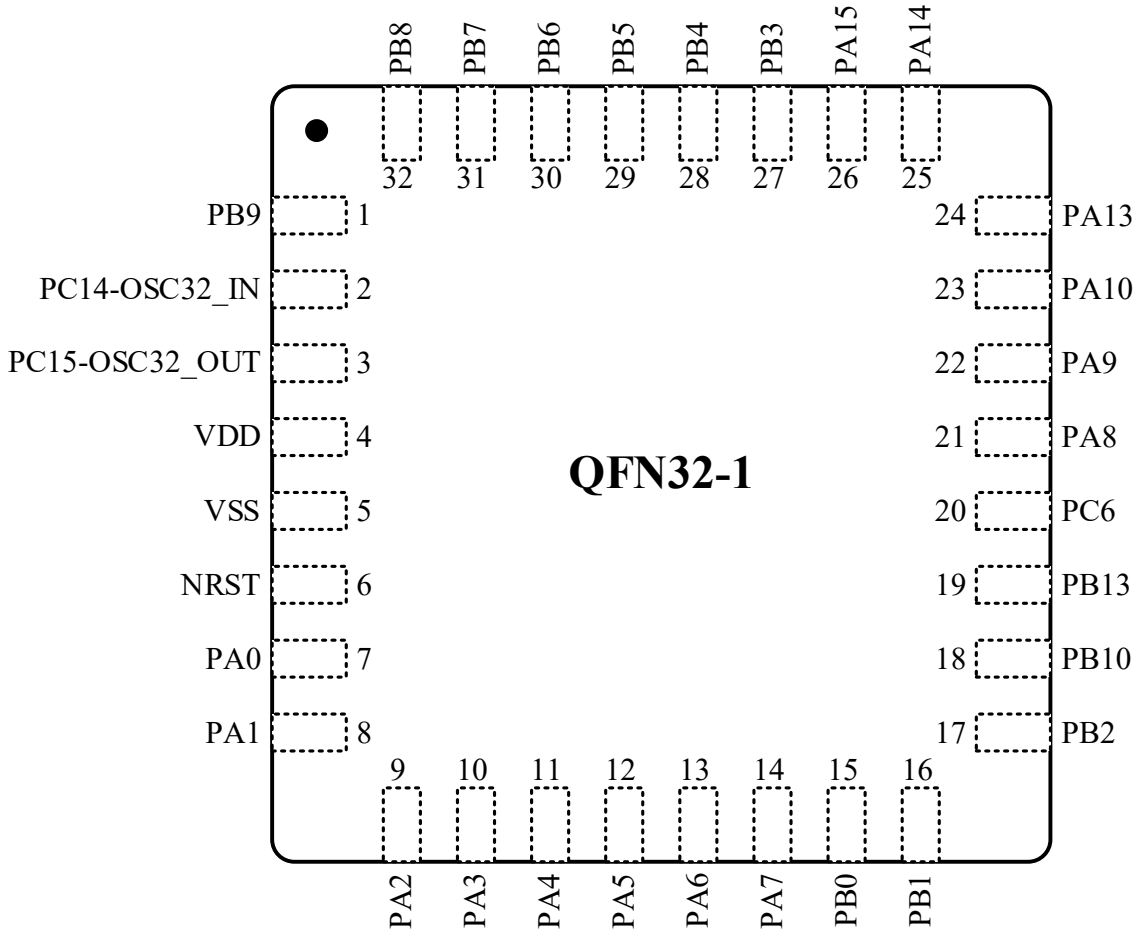
QFN32 (5mm x 5mm) Pinout



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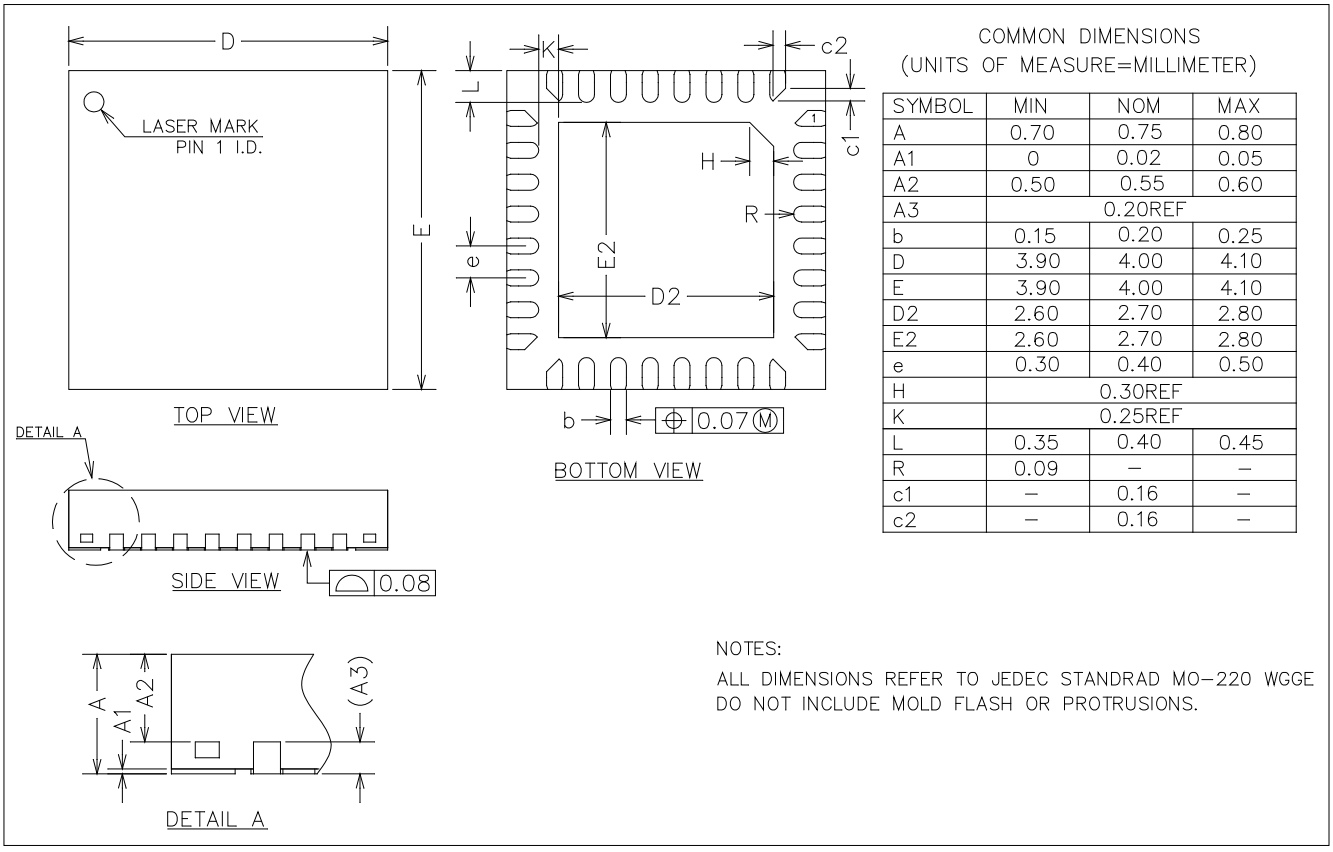
QFN32 (4mm x 4mm) Package Dimensions



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0	0.02	0.05
A2	0.50	0.55	0.60
A3		0.20REF	
b	0.15	0.20	0.25
D	3.90	4.00	4.10
E	3.90	4.00	4.10
D2	2.60	2.70	2.80
E2	2.60	2.70	2.80
e	0.30	0.40	0.50
H		0.30REF	
K		0.25REF	
L	0.35	0.40	0.45
R	0.09	–	–
c1	–	0.16	–
c2	–	0.16	–

NOTES:

ALL DIMENSIONS REFER TO JEDEC STANDRAD MO-220 WGGE
DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.

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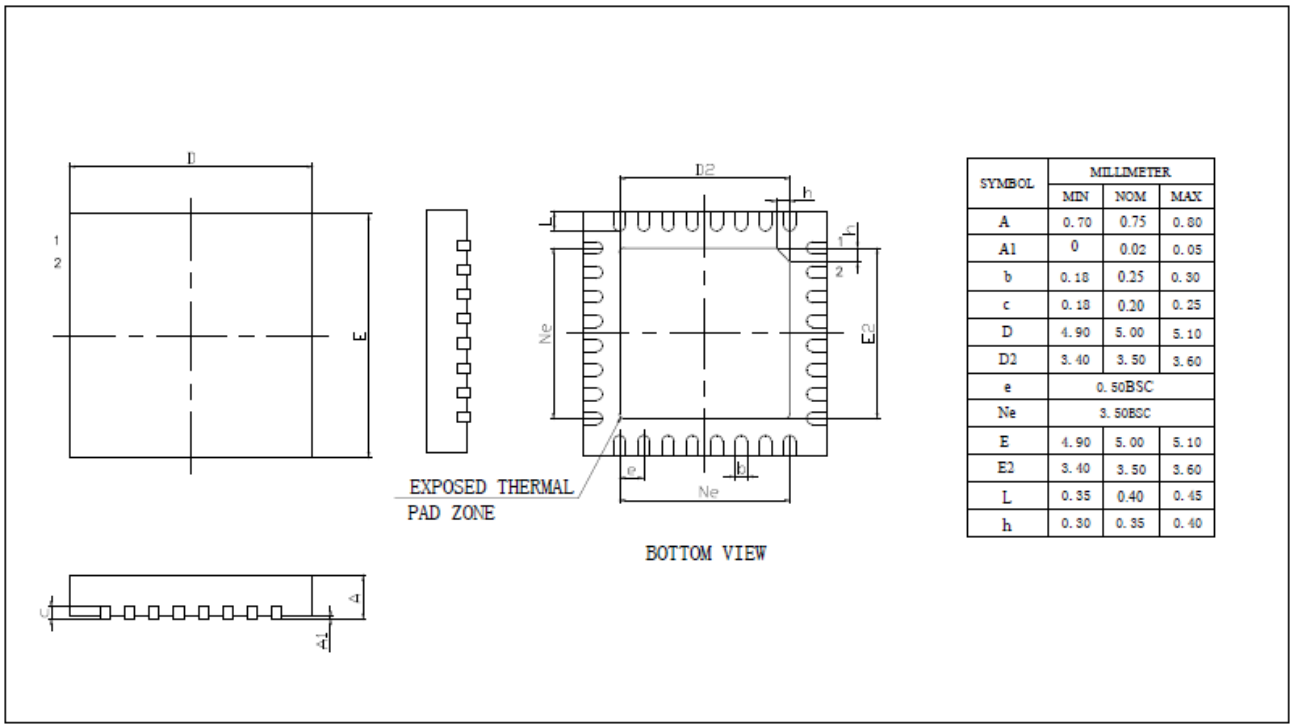
QFN32 (5mm x 5mm) Package Dimensions



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0	0.02	0.05
b	0.18	0.25	0.30
c	0.18	0.20	0.25
D	4.90	5.00	5.10
D2	3.40	3.50	3.60
e	0.50BSC		
Ne	3.50BSC		
E	4.90	5.00	5.10
E2	3.40	3.50	3.60
L	0.35	0.40	0.45
h	0.30	0.35	0.40

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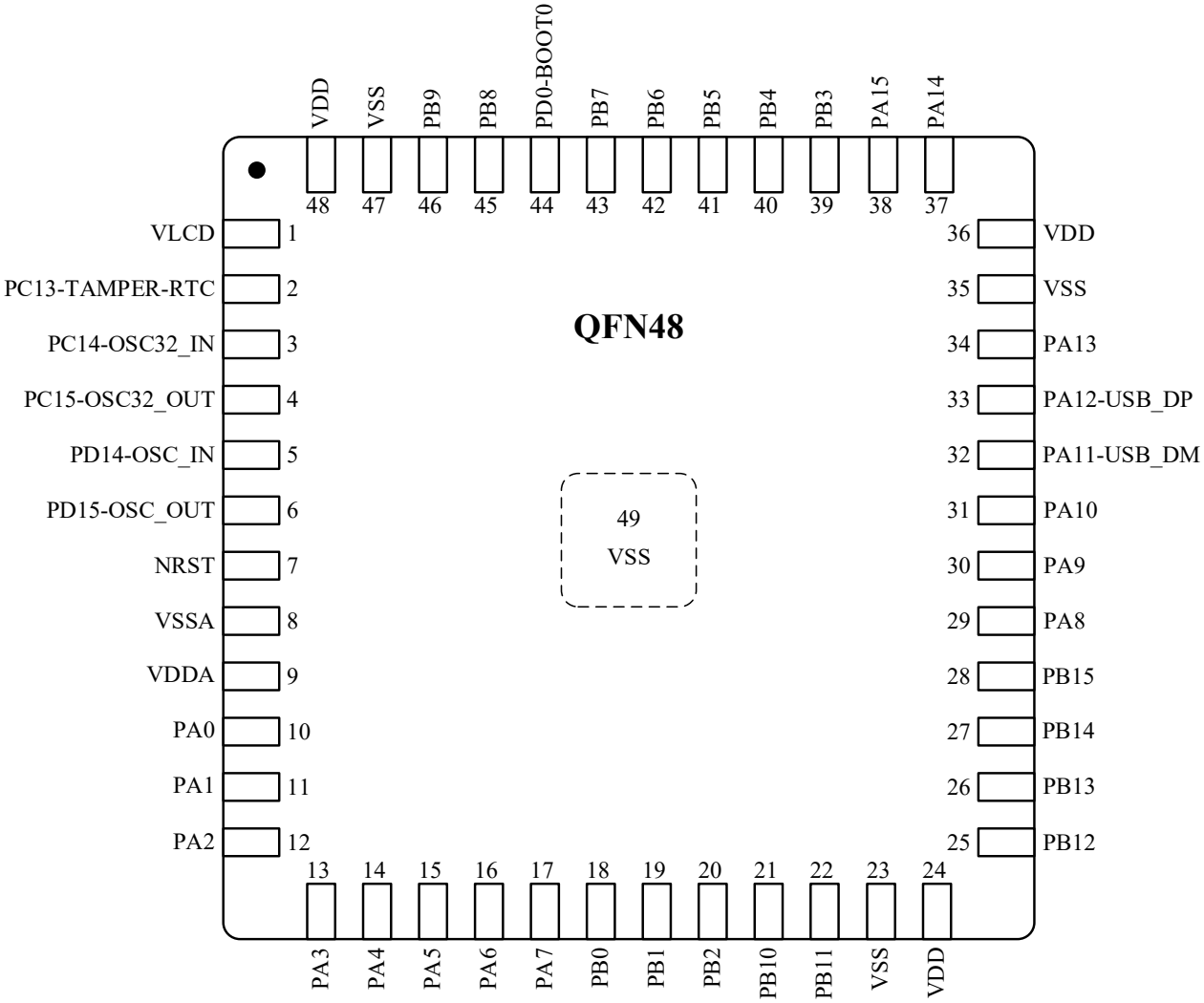
QFN48 Package

QFN48(with LCD) Pinout



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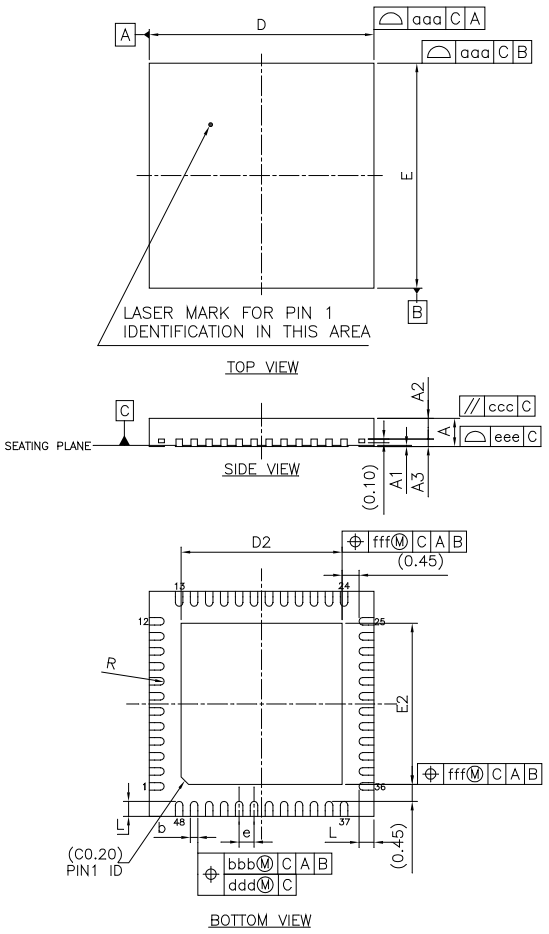
QFN48 (6mm x 6mm) Package



Item		Symbol	MIN.	NOM.	MAX.
total height		A	0.70	0.75	0.80
stand off		A1	0.00	0.02	0.05
mold thickness		A2	0.50	0.55	0.60
leadframe thickness		A3		0.20 REF.	
lead width		b	0.15	0.20	0.25
package size	X	D	5.90	6.00	6.10
	Y	E	5.90	6.00	6.10
E-PAD size	X	D2	4.20	4.30	4.40
	Y	E2	4.20	4.30	4.40
lead length		L	0.30	0.40	0.50
lead pitch		e		0.40 bsc	
lead arc		R	0.075	---	---
Package profile of a surface		aaa		0.10	
Lead position		bbb		0.07	
Paralleliam		ccc		0.10	
Lead position		ddd		0.05	
Lead profile of a surface		eee		0.08	
Epad position		fff		0.10	

NOTES:
ALL DIMENSIONS REFER TO JEDEC STANDARD MO-220 WJJE
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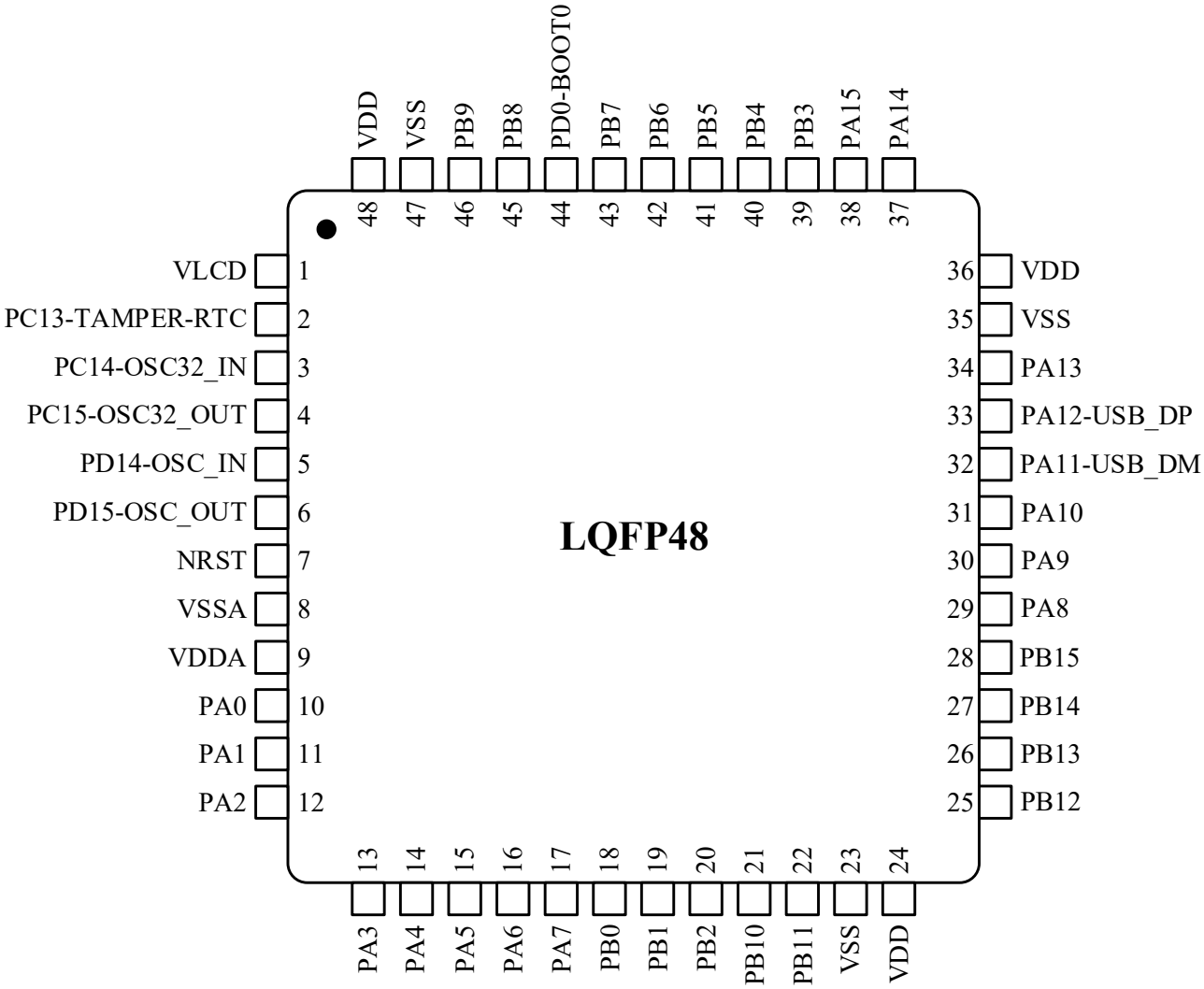
LQFP48 Package

LQFP48 (with LCD) Pinout



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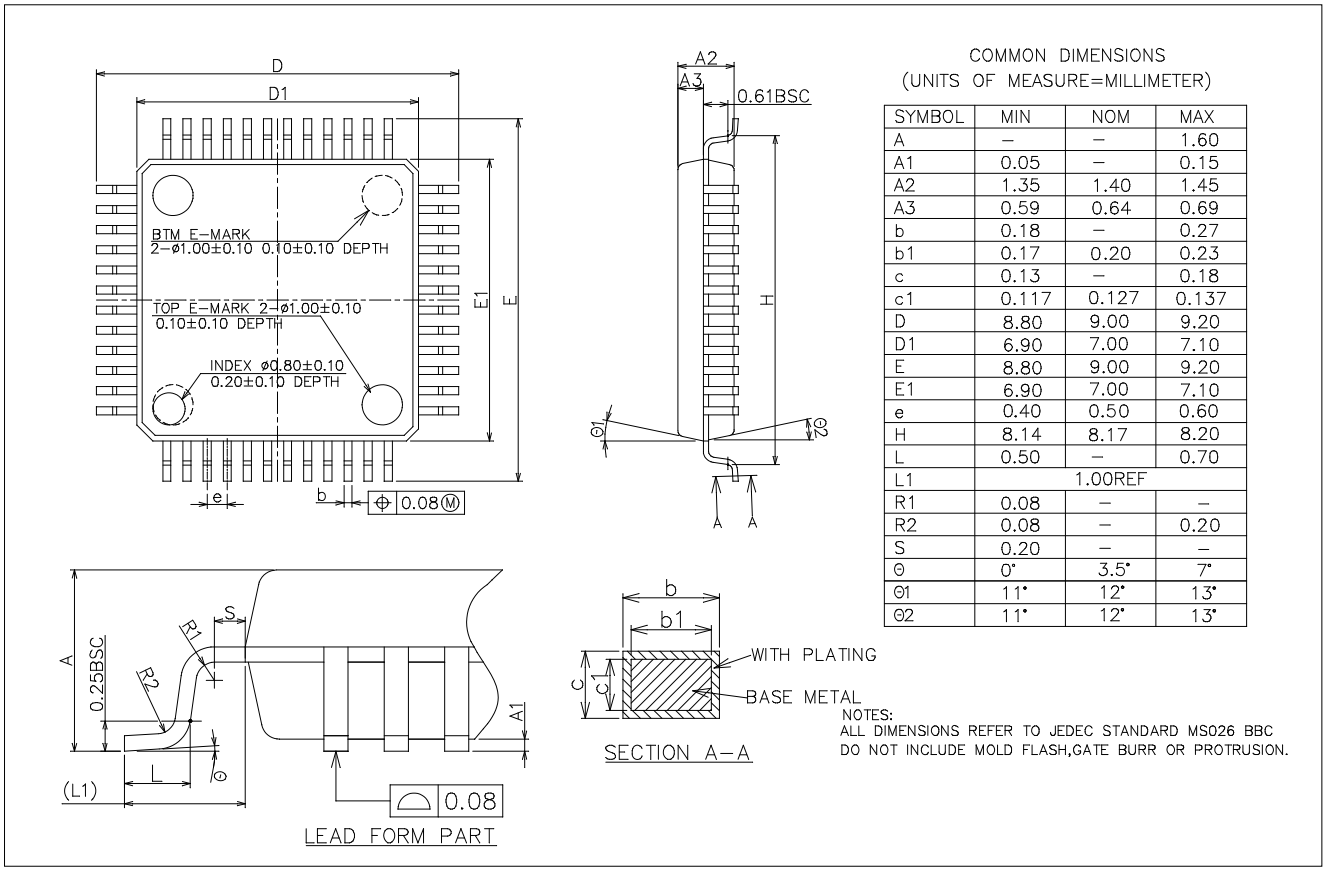
LQFP48 (7mm x 7mm) Package



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	–	–	1.60
A1	0.05	–	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	–	0.27
b1	0.17	0.20	0.23
c	0.13	–	0.18
c1	0.117	0.127	0.137
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
e	0.40	0.50	0.60
H	8.14	8.17	8.20
L	0.50	–	0.70
L1		1.00REF	
R1	0.08	–	–
R2	0.08	–	0.20
S	0.20	–	–
θ	0°	3.5°	7°
θ1	11°	12°	13°
θ2	11°	12°	13°

NOTES:
ALL DIMENSIONS REFER TO JEDEC STANDARD MS026 BBC
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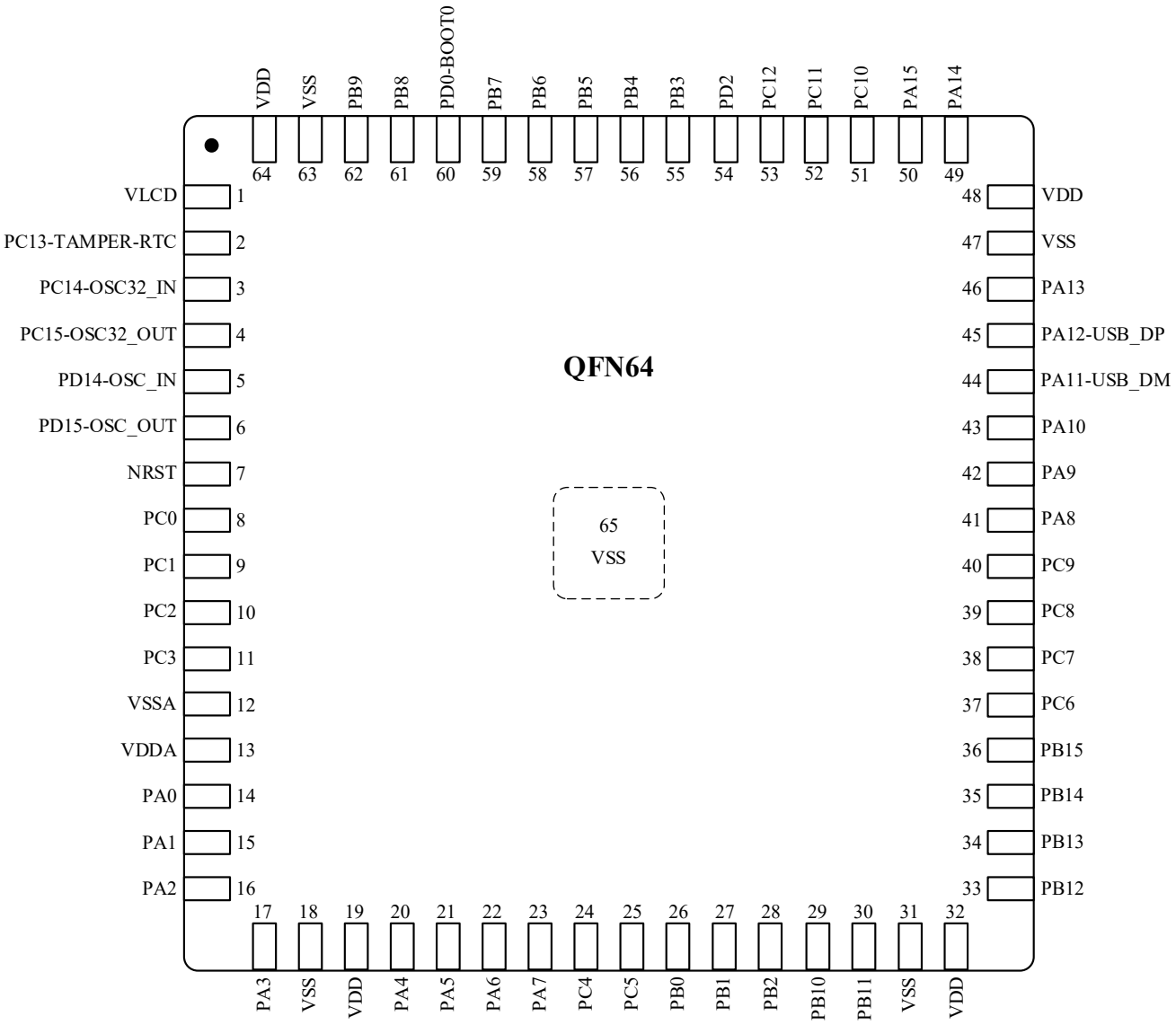
QFN64 Package

QFN64 Pinout



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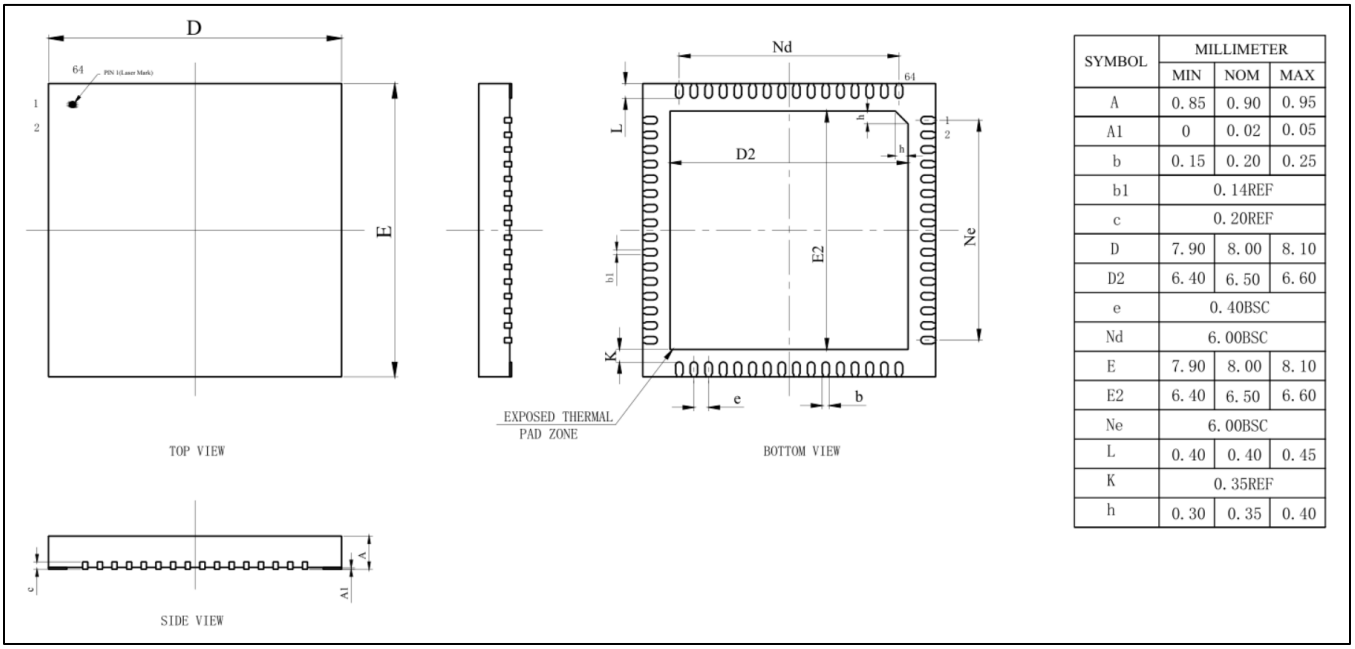
QFN64 (8mm x 8mm) Package



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.85	0.90	0.95
A1	0	0.02	0.05
b	0.15	0.20	0.25
b1		0.14REF	
c		0.20REF	
D	7.90	8.00	8.10
D2	6.40	6.50	6.60
e		0.40BSC	
Nd		6.00BSC	
E	7.90	8.00	8.10
E2	6.40	6.50	6.60
Ne		6.00BSC	
L	0.40	0.40	0.45
K		0.35REF	
h	0.30	0.35	0.40

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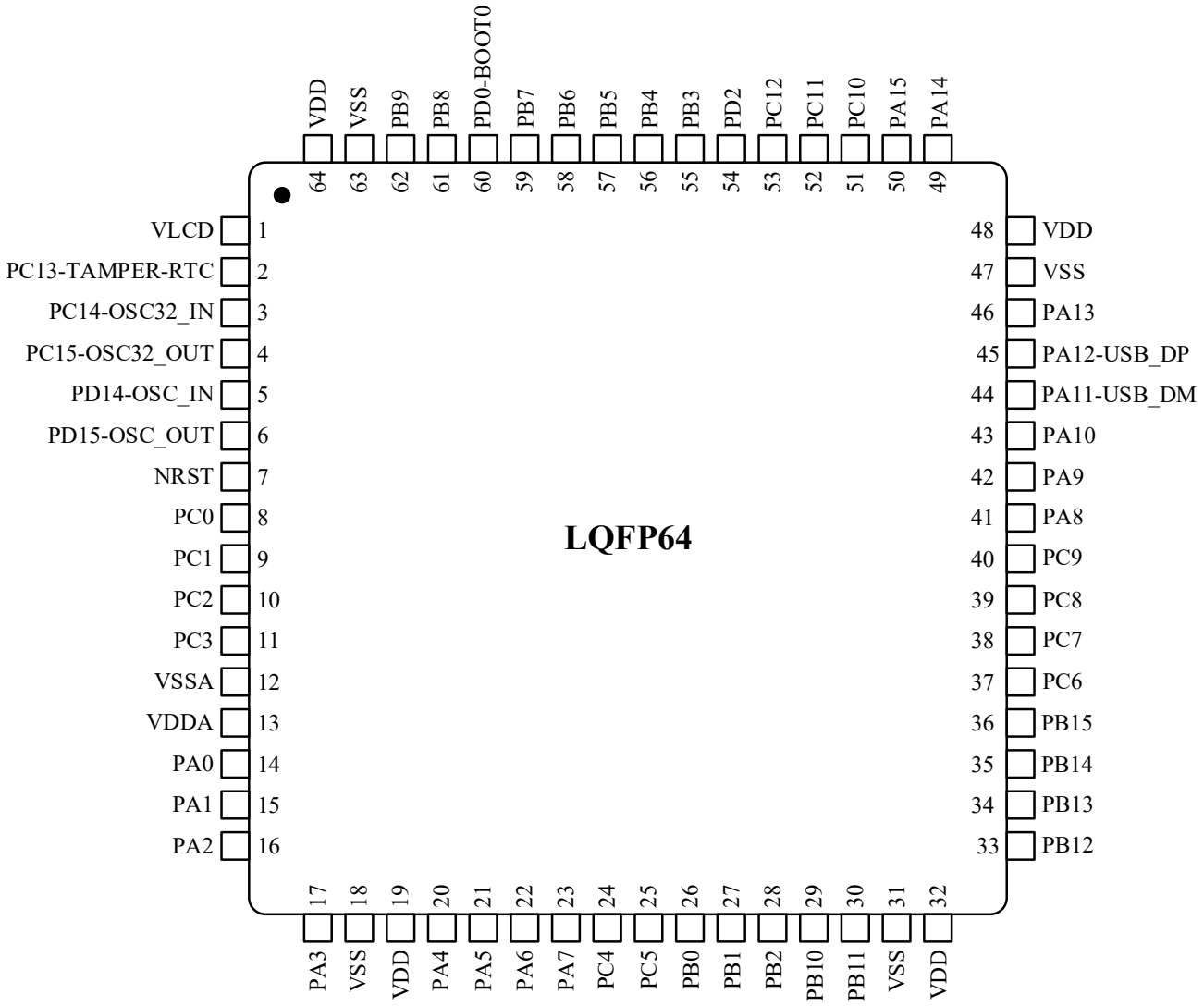
LQFP64 Package

LQFP64 Pinout



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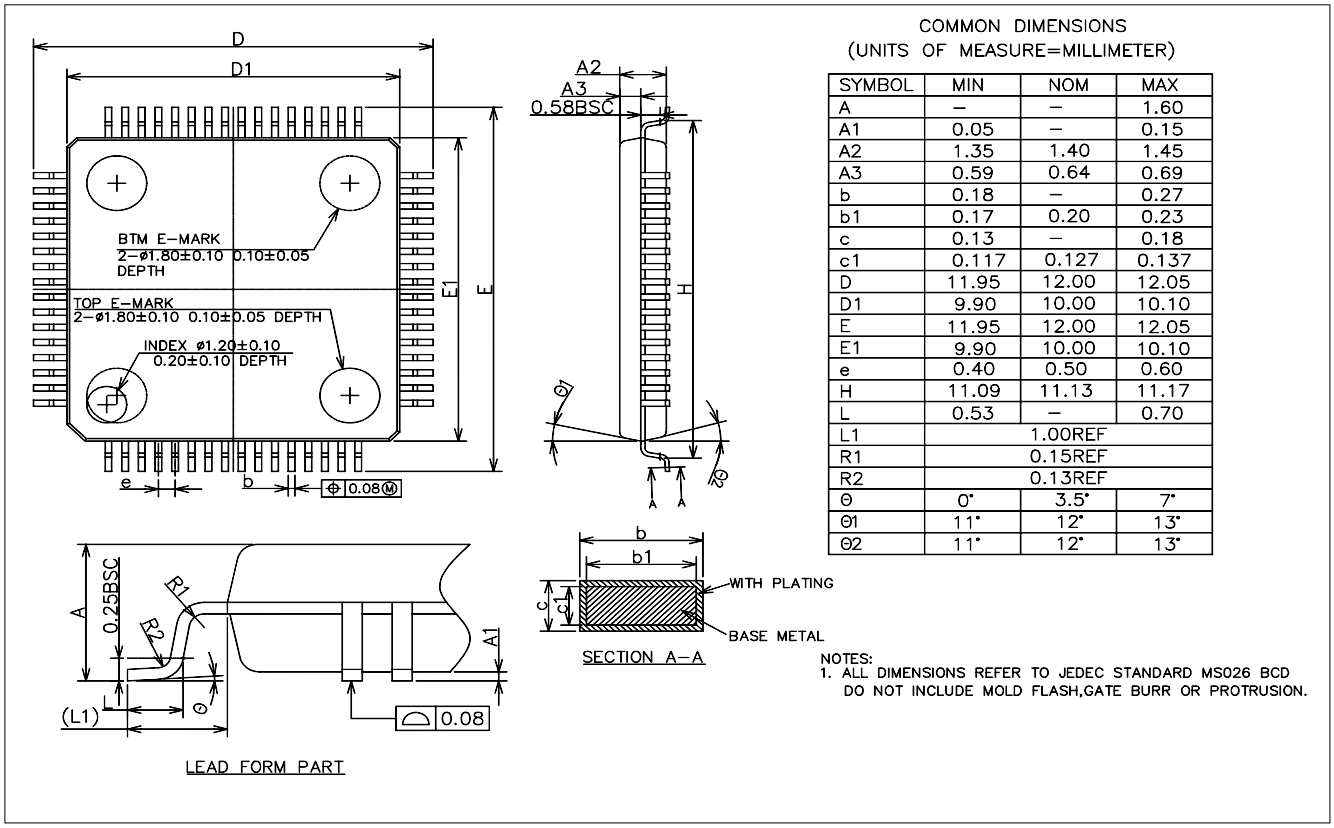
LQFP64 (10mm x 10mm) Package



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	–	–	1.60
A1	0.05	–	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	–	0.27
b1	0.17	0.20	0.23
c	0.13	–	0.18
c1	0.117	0.127	0.137
D	11.95	12.00	12.05
D1	9.90	10.00	10.10
E	11.95	12.00	12.05
E1	9.90	10.00	10.10
e	0.40	0.50	0.60
H	11.09	11.13	11.17
L	0.53	–	0.70
L1	1.00REF		
R1	0.15REF		
R2	0.13REF		
θ	0°	3.5°	7°
θ1	11°	12°	13°
θ2	11°	12°	13°

NOTES:
1. ALL DIMENSIONS REFER TO JEDEC STANDARD MS026 BCD
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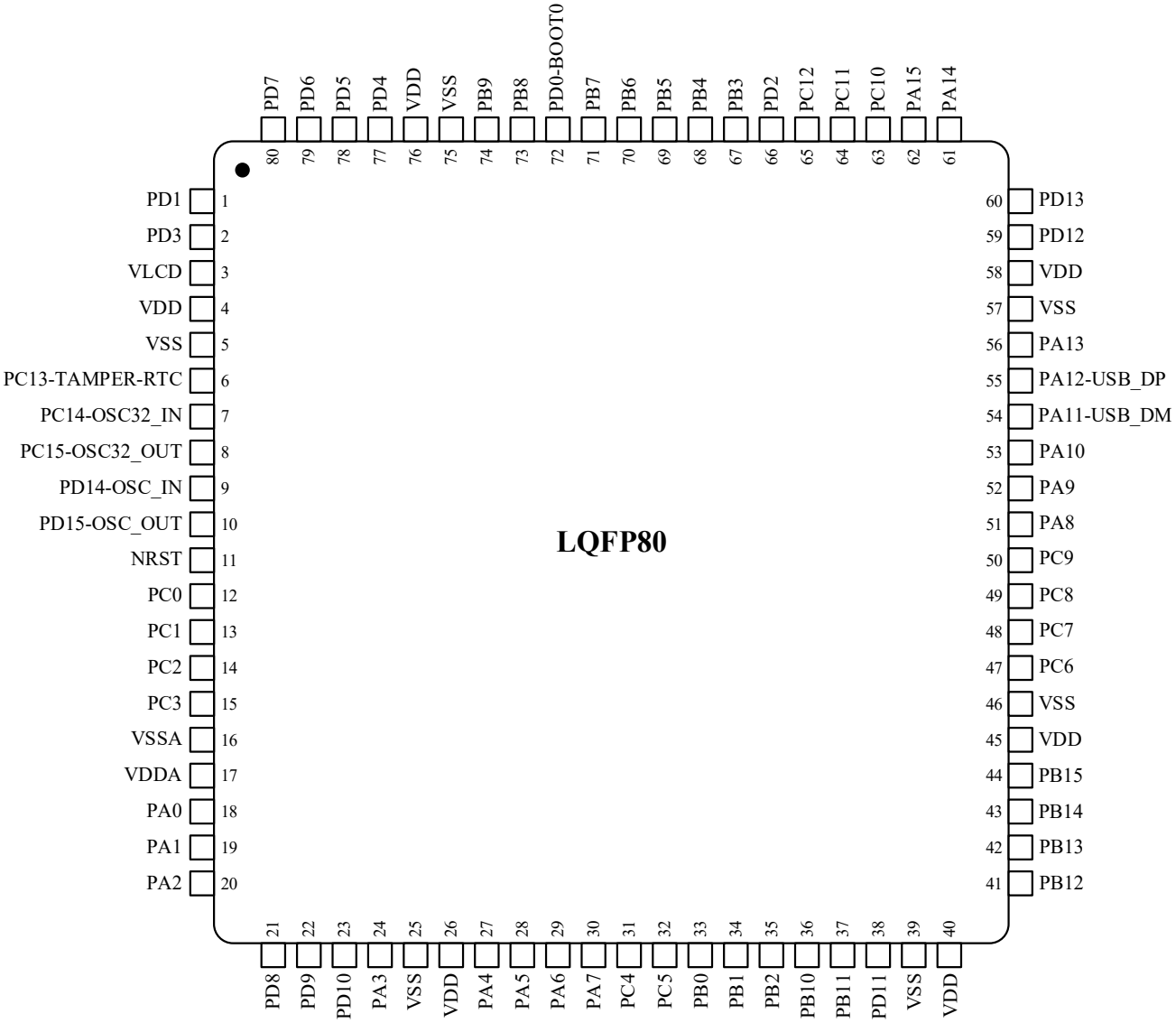
LQFP80 Package

LQFP80 Pinout



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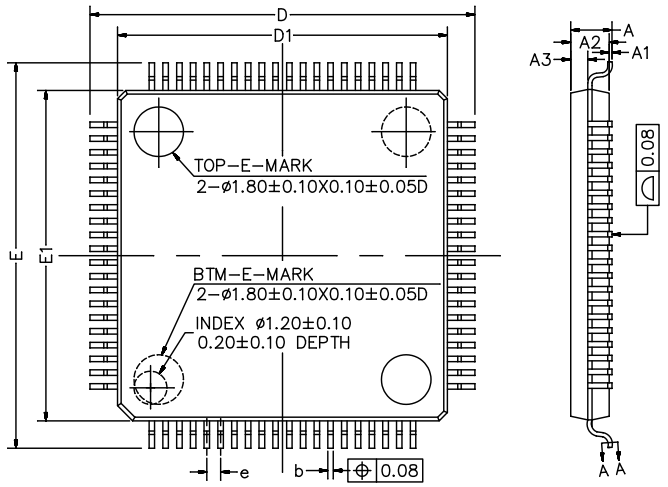
LQFP80 (12mm x 12mm) Package



COMMON DIMENSIONS
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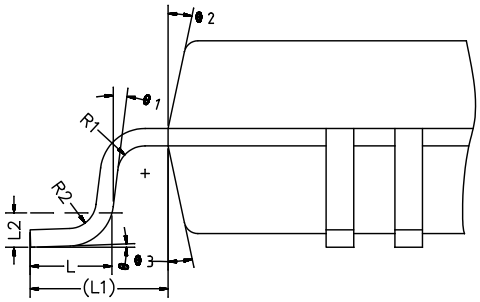
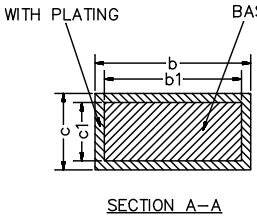
SYMBOL	MIN	NOM	MAX
A	–	–	1.60
A1	0.05	–	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	–	0.27
b1	0.17	0.20	0.23
c	0.13	–	0.18
c1	0.12	0.127	0.134
D	13.80	14.00	14.20
D1	11.90	12.00	12.10
E	13.80	14.00	14.20
E1	11.90	12.00	12.10
e	0.40	0.50	0.60
L	0.45	0.60	0.75
L1	1.00REF		
L2	0.25BSC		
R1	0.08	–	–
R2	0.08	–	0.20
θ	0°	3.5°	7°
θ1	0°	–	–
θ2	11°	12°	13°
θ3	11°	12°	13°





NOTES:
ALL DIMENSIONS REFER TO JEDEC STANDARD MS-026 BDD DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.

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Version History

Version	Date	Changes
V1.0	2020.7.1	Initial release
V1.2	2021.4.14	1. Added N32L401x 2. Updated LCD version difference description, add the precautions for LCD 1/8 duty cycle mode
V1.3	2022.7.6	1. Modify the description of low power 2. Delete N32L401x 3. Modify the description of time counter 4. Modify reset description
V1.4	2022.9.5	1. Add the type N32L403KBQ7-1(1) 2. Modify the number of DAC channels in the resource configuration table 2-1 3. Modify the PB8 pin number of QFN64 pinout 4. Add N32L402 series type 5. Modify LQFP packages size description

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