N32A455 Series Errata Sheet

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2 Power Control (PWR)

2.1 Stop2 Mode Wakeup

Description

When the MCU is in Stop2 mode, wakeup and NRST reset occurs simultaneously, the NRST reset cannot reset MCU.

Wakeup takes precedence, and the MCU will respond to the wakeup event first.

Workaround

To resolve this issue, it is advised to avoid triggering an NRST reset of the MCU simultaneously with the wakeup event. Alternatively, if an NRST reset is necessary in a specific scenario, perform consecutive NRST resets to ensure the MCU is properly reset.

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3 Reset And Clock Control (RCC)

3.1 System Timer (Systick)

Description

The MCU can’t be awakened when external clock source(STCLK) is chosen as clock source.

Workaround

To address this issue, configure the SysTick control register to use the core clock as the clock source instead of the External Reference Clock (STCLK).

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4 GPIO and AFIO

4.1 SPI1 Slave Mode, USART2 Sync Mode

Description

With SPI1 and USART2 clocks already enabled, when pin PA4 is configured as a multiplexed output.SPI1 operating in slave mode with NSS software mode (SSMEN=1, SSEL=0), the USART2 clock in synchronous mode cannot be transmitted .

Workaround

No solution is provided for this issue.

4.2 SPI1 Master Mode, USART2 Sync Mode

Description

With SPI1 and USART2 clocks already enabled, when pin PA4 is configured as a multiplexed output, SPI1 operating in master mode with NSS software mode (SSMEN=1, SSEL=0), the USART2 clock in synchronous mode cannot be transmitted .

Workaround

Enable the SSOEN bit in SPI1 master mode.

4.3 SPI2 Slave Mode, USART3 Sync Mode

Description

With SPI2 and USART3 clocks already enabled, when pin PB12 is configured as a multiplexed output, SPI2 operating in slave mode with NSS software mode (SSMEN=1, SSEL=0), the USART3 clock in synchronous mode cannot be transmitted.

Workaround

No solution is provided for this issue.

4.4 SPI2 Master Mode, USART3 Sync Mode

Description

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With SP2 and USART3 clocks already enabled, when pin PB12 is configured as a multiplexed output, SPI2 operating in master mode with NSS software mode (SSMEN=1, SSEL=0), the USART3 clock in synchronous mode cannot be transmitted.

Workaround

Enable the SSOEN bit in SPI2 master mode.

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5 Analog/Digital Conversion (ADC)

5.1 ADC Data Left Alignment

Description

In the ADC single conversion mode, when using a non-12bit precision with left alignment, and triggering the conversion of regular channels by software, the most significant bit of the invalid bits in the ADC_DAT register is 1.

Workaround

To address this issue, either retain only the valid data bits or switch to right-aligned mode.

5.2 ADC Analog Watchdog

Description

In ADC independent mode, with single conversion, and non-12-bit precision, enabling the analogue watchdog feature, and triggering the conversion of regular/injected channels by software, if the high threshold value of the analogue watchdog has valid bits equal to the value in the ADC data register, with all invalid bits set to 0, it may lead to a false triggering of the analogue watchdog.

Workaround

In this situation, ensure that the most significant bit of the invalid bits in the high threshold value of the analogue watchdog is set to 1 to prevent unintended triggering.

5.3 ADC Injection Channel Triggers Regular Channel Conversion

Description

In continuous conversion mode, with external triggering disabled for regular channels and only software-triggered injection channel conversions, it is possible that the regular channels may be inadvertently triggered, leading to data being generated in the ADC_DAT register, and the corresponding status bit in ADC_STS for regular channel conversions being set.

Workaround

Ignore the flags bits and data generated by regular channel conversions..

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5.4 Slave ADC Conversion Impacted By Master ADC Conversion

Description:

When the ADC operates in dual ADC mode and synchronous injected mode, and only the software triggers the regular channel conversion of the master ADC, the regular channels of the slave ADC are also triggered. Additionally, the lower 16 bits from the ADC_DAT of the slave ADC are merged into the upper 16 bits of the master ADC_DAT.

Workaround:

No solution is provided for this issue.

5.5 Affecting Adjacent ADC Data Registers

Description:

In independent mode, when software triggers the conversion of the ADC4/2 regular channels, the lower 16 bits of the ADC4/2 DAT register content are merged into the upper 16 bits of the ADC3/1 DAT register.

Workaround:

No solution is provided for this issue.

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6 Serial Peripheral Interface (SPI)

6.1 SPI Interface

6.1.1 SPI Baud Rate Setting

Description

CRC validation may fail if SPI master mode, when setting the bitrate control bits (BR[2:0]) to fPLCK/2

Workaround

Avoid setting the bitrate control bits (BR[2:0]) to fPLCK/2 in this scenario.

6.1.2 Checking Slave Mode CRC

Description

In SPI operating in slave mode with CRC verification enabled, even if the NSS pin is at a high level, CRC calculation continues if the SPI receives a clock signal

Workaround

Before using CRC validation , clear the CRC data register to ensure synchronization between the CRC checks of the master and slave devices

The clearing steps are as follows:

1. Reset the SPI enable bit (set to 0)
2. Reset the CRC validation bit (set to 0)
3. Set the CRC validation bit (set to 1)
4. Set the SPI enable bit (set to 1)

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6.2 I2S Interface

6.2.1 PCM Long Frame Mode

Description

When I2S is operating in master mode, PCM long frame mode, and the data format is directly set to 32-bit or is extended from 16-bit to 32-bit, the WS(word select) signal occurs every 16bits instead of every 32bits.

Workaround

If I2S must operate in master mode and use long frame mode, it is recommended to use only the 16-bit data mode to ensure proper WS signal alignment.

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7 I2C Interface

7.1 Handling Software Events Before Current Byte Transferring

Description

In the occurrence of events EV7, EV7_1, EV6_1, EV6, EV2, EV8, and EV3, it is essential to handle the events before the current byte transfer to prevent issues such as reading an extra byte, obtaining duplicate data, or losing data.If the software fails to read the N-1 data before the stop signal generation, the data in the shift register for the Nth byte may become corrupted (shifted left by one bit).

Workaround

1. When transferring more than one byte in I2C, consider using DMA if possible.
2. When using I2C interrupts, set the interrupt priority to the highest priority in the application
3. When the read data reaches the N-1 byte:
   a) Check that BSF(Byte Shift Flag) is set to 1
   b) Configure SCL as a GPIO open-drain output and set it to 0
   c) Set STOPGEN to 1
   d) Read the N-1 byte
   e) Configure SCL back to I2C multiplex open-drain output mode.
   f) Read the last byte

7.2 Notes On Single Read Of One Or Two Bytes

Description

In master read mode, errors in reading data may occur when reading single-byte and double-byte lengths.

Workaround

1. Single byte Read:
   a) Upon receiving ADDRF
   b) Set ACKEN to 0
   c) Clear ADDRF bit (by reading STS1 first and then STS2)
   d) Set STOPGEN to 1

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e) Read one byte of data.

2. Double-byte Read:

a) Upon receiving ADDRF

b) Set ACKPOS to 1

c) Clear ADDRF bit (by reading STS1 first and then STS2)

d) Set ACKEN to 0

e) Check that BSF (Byte Shift Flag) is 1

f) Set STOPGEN to 1

g) Read two consecutive bytes of data

7.3 Using DMA Simultaneously With Other Peripherals

Description

During I2C communication using DMA, it may lead to abnormal I2C communication, if there are other peripherals also use the same DMA controller.

Workaround

1. Use different DMA controllers.
2. Disable DMA for other peripherals during I2C DMA communication.

7.4 The I2C Used As A Slave Device

Description

When I2C is used as a slave device, an abnormal state occurs and cannot be recovered.

Workaround

When I2C is used as a slave device, adding a timeout detection function to reset the I2C module when the timeout occurs.

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8 Universal Synchronous Asynchronous Receiver Transmitter (USART)

8.1 Parity Error Flag

Description

During the reception of a byte of data, if a parity error is detected before receiving the stop bit, the parity error flag is set. During this period, the parity error flag cannot be cleared through software (by reading the status register and then reading data register again).If the parity error interrupt is enabled, it may repeatedly enter the parity error interrupt handling function

Workaround

1. When the read data buffer flag is set and data is received, clear the parity error flag.
2. Disable the parity error interrupt during the first entry into the parity error interrupt, then re-enable it after receiving the data.

8.2 RTS Hardware Flow Control

Description

When the RTS(Request to Send) hardware flow control is enabled, and a USART receives a frame of data, the RTS signal is automatically asserted (pulled high) upon receiving the first byte of data. If this first byte is not promptly read from the data register, upon receiving the next byte of data, the RTS signal is de-asserted (pulled low) again, and the USART waits for the reception of the next frame of data.

Workaround

Read the data from the data register promptly before receiving the next new data.

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9 Debug Interface (DBG)

9.1 The Debug Registers

Description

The DBGMCU_IDCODE debugging register can only be accessed in debug mode (not accessible to user programs). When attempting to read it in user mode, the returned value is 0xFF.

Workaround

Avoid using IDCODE in user applications to prevent issues related to its restricted access in non-debug modes.

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10 Timer (TIM)

10.1 Timer Repetitive Capture Detection

Description

When an input capture occurs, if a new input capture is generated during the reading of TIMx_CCDATx (capture/compare register x) –where the read operation automatically clears the capture flag –the CCxOCF(capture/compare x repeated capture flag) might still remain set.

Workaround

No solution is provided for this issue.

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11 Real Time Clock (RTC)

11.1 RTC Prescaler

Description

The asynchronous prescaler factor and the synchronous prescaler factor in the RTC cannot be set to 0, as it may lead to RTC pre-allocation to failure.

Workaround

Avoid setting the asynchronous prescaler register (TRC_PRE) DIVA[6:0](asynchronous prescaler segment) and DIVS[14:0](synchronous prescaler segment) to 0.

11.2 RTC Calibration

Description

During RTC automatic calibration (when the CP bit in the RTC_CALIB register is set to 1), the automatic calibration may not successful if the asynchronous prescaler factor (DIVA) is not set to 128/64/32/16/8.

Workaround

To ensure successful RTC automatic calibration, choose an asynchronous prescaler (DIVA) factor of 128/64/32/16/8.

11.3 RTC Timing

Description

While the RTC is active, if an NRST (external reset) occurs, the reset period will cause the RTC to stop counting.

Workaround

No solution is provided for this issue.

11.4 RTC Periodic Wakeup

Description

Periodic wake-up from the RTC module does not work to wake up from STANDBY mode.

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Workaround

Use the RTC alarm wake-up feature instead of the periodic wake-up.

11.5 RTC Digital Clock

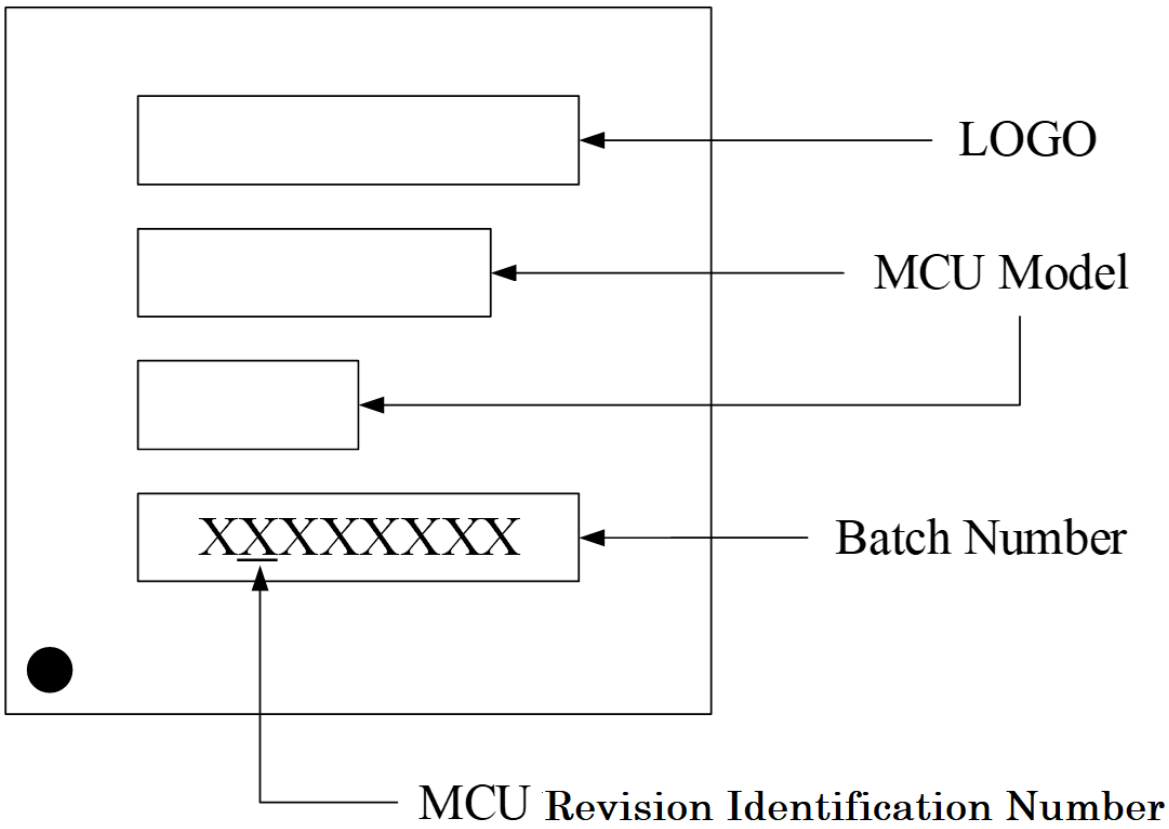
Description

The RTC digital clock precision calibration function is not recommended.

Workaround

No solution is provided for this issue.

12 Chip Marking And Revision Description



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13 Version History

Version	Date	Changes
V1.0.0	2022.06.20	The initial release
V1.1.0	2023.06.28	1.Added RTC wake-up correction item 2.Added I2C used as slave device correction item 3.Added RTC correction item

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