

N32A455xxL7

Datasheet

N32A455xxL7 series adopts a 32-bit ARM Cortex-M4F core, with a maximum operating frequency of 144MHz, support floating-point unit and DSP instructions. It integrates up to 512KB embedded flash, 144KB SRAM, high-performance analog interface such as 4x12bit 4.7Msps ADC, 4xOPAMP, 7xCOMP, 2x1Msps 12bit DAC, multiple communication bus interfaces (U(S)ART, I2C, SPI, QSPI, CAN, SDIO, etc). It also features a built-in hardware acceleration engine for cryptographic algorithm.

Key Features

- **CPU Core**

- 32-bit ARM Cortex-M4F +FPU, single -cycle hardware multiplication and division instructions, support DSP instruction and MPU
- Built-in 8KB instruction Cache supports Flash acceleration unit for zero-wait program execution
- Maximum frequency of 144MHz, 180DMIPS

- **Memories**

- Up to 512KByte of embedded Flash memory with ECC
 - Support encryption multi-user partition and data protection
 - 100,000 erase/write cycles and 10 years data retention
- Up to 144KByte of SRAM, including 16K Byte Retention RAM, the Retention RAM supports hardware parity checking

- **Clock**

- HSE: 4MHz~32MHz high-speed external crystal oscillator
- LSE: 32.768KHz low-speed external crystal oscillator
- HSI: High-speed internal RC 8MHz
- LSI: Low-speed internal RC 40KHz
- Built-in high speed PLL
- MCO: Support 1-channel clock output, which can be configured as SYSCLK, HSE, HSI or PLL clock divisional output

- **Reset**

- Support power-on/power-down/ brown-out/external pin reset
- Support programmable low-voltage detection and reset
- Support watchdog reset, software reset

- **Communication Interfaces**

- 7x U(S)ART interfaces, with maximum rate of 4.5 Mbps.
 - 3x USART interfaces (support ISO7816, IrDA, LIN)
 - 4x UART interfaces
- 3x SPI interfaces with speed up to 36 MHz, two of which support I2S
- 1x QSPI interface with speed up to 144 Mbps
- 4x I2C interfaces(master/slave) with speed up to 1 MHz where slave mode support dual address response

- 2x CAN 2.0A/B bus interfaces
- 1x SDIO interface, supports SD/SDIO/MMC format
- **High Performance Analog Interfaces**
 - 4x 12-bit ADCs with 4.7Msps,
 - Configurable as 12/10/8/6-bit mode
 - Sampling rate up to 8.9Msps in 6-bit mode
 - Up to 38 external single-ended input channels
 - Support differential mode.
 - 4x rail-to-rail operational amplifiers with built-in maximum 32x programmable gain amplifier
 - 7x high-speed analog comparators with built-in 64-level adjustable reference
 - 2x 12-bit DAC with sampling rate of 1Msps
 - Supports external independent reference voltage source
 - Analog voltage operation from 1.8~3.6V .
- **GPIOs**
 - Up to 80 GPIOs.
 - Support multiplexed functions
 - Most GPIOs are 5V tolerant
- **DMA controllers**
 - 2x high-speed DMA controllers
 - Each controller supports 8 channels
 - Channel source address and destination address can be configured arbitrarily
- **Real-time clock (RTC)**
 - Supports leap-year calendar, alarm events, periodic wake-up
 - Supports internal and external clock calibration
- **Timers**
 - 2x 16-bit advanced timers with maximum control precision of 6.9ns
 - Support input capture, complementary output, quadrature encoding input, etc
 - Each timer has 4 independent channels, 3 of which support 6-channel complementary PWM output.
 - 4x 16-bit general-purpose timers
 - Support input capture/output comparison / PWM output
 - Each timer has 4 independent channels
 - 2x 16-bit basic timers
 - 1x 24bit SysTick timer
 - 1x 7bit Window Watchdog (WWDG)
 - 1x 12bit Independent Watchdog (IWDG)
- **Programming Methods**
 - Supports SWD/JTAG debugging interface

- Supports UART Bootloader
- **Security Features**
 - Built-in hardware acceleration engine for cryptographic algorithm
 - Supports DES/3DES, AES, SHA1/SHA224/SHA256, SM1, SM3, SM4, SM7 and MD5 algorithms
 - Flash encryption, multi-user partition management (MMU) True random number generator(TRNG)
 - CRC16/32 operation
 - Support write protection (WRP), multiple read protection (RDP) levels (L0/L1/L2)
 - Support secure boot, program encryption download, secure firmware update.
 - Support external clock failure detection, anti-tamper detection.
- **96-bit UID and 128-bit UCID**
- **Operating Conditions**
 - Operating voltage range: 1.8V~3.6V
 - Operating temperature range: -40°C ~105°C
 - Certified by AEC-Q100-G2
 - ESD: ±4KV (HBM model), ±1KV(CDM model)
- **Packages**
 - LQFP48(7mm x 7mm)
 - LQFP64(10mm x 10mm)
 - LQFP100(14mm x 14mm)
- **Ordered information**

Reference	Part Number
N32A455xxL7	N32A455CEL7,N32A455REL7, N32A455VEL7

Contents

KEY FEATURES	1
1. INTRODUCTION.....	8
1.1 NAMING CONVENTION	9
1.2 PRODUCT CONFIGURATIONS.....	10
2. FUNCTION OVERVIEW.....	11
2.1 PROCESSOR CORE.....	11
2.2 MEMORIES	11
2.2.1 Embedded FLASH Memory	12
2.2.2 Embedded SRAM	12
2.2.3 Nested Vector Interrupt Controller (NVIC).....	12
2.3 EXTENDED INTERRUPT/EVENT CONTROLLER (EXTI).....	12
2.4 CLOCK SYSTEM.....	12
2.5 BOOT MODES	13
2.6 POWER SUPPLY SCHEME	14
2.7 RESET.....	14
2.8 PROGRAMMABLE VOLTAGE DETECTOR	14
2.9 VOLTAGE REGULATOR.....	14
2.10 LOW POWER MODE	14
2.11 DIRECT MEMORY ACCESS (DMA)	15
2.12 REAL TIME CLOCK (RTC).....	15
2.13 TIMERS AND WATCHDOGS	16
2.13.1 Basic Timer (TIM6 and TIM7).....	16
2.13.2 General-Purpose Timer (TIMx).....	16
2.13.3 Advanced Control Timer (TIM1 and TIM8).....	17
2.13.4 SysTick Timer (SysTick)	17
2.13.5 Watchdog (WDG).....	18
2.14 I2C BUS INTERFACE.....	18
2.15 UNIVERSAL SYNCHRONOUS/ASYNCHRONOUS TRANSCEIVER (USART).....	19
2.16 SERIAL PERIPHERAL INTERFACE (SPI)	21
2.17 SERIAL AUDIO INTERFACE (I2S)	22
2.18 QUAD SERIAL PERIPHERAL INTERFACE (QSPI).....	22
2.19 SECURE DIGITAL INPUT OUTPUT INTERFACE (SDIO).....	23
2.20 CONTROLLER AREA NETWORK (CAN)	23
2.21 GENERAL PURPOSE INPUT/OUTPUT INTERFACE (GPIO).....	24
2.22 ANALOG/DIGITAL CONVERTER (ADC)	25
2.23 DIGITAL/ANALOG CONVERTER (DAC)	25
2.24 OPERATIONAL AMPLIFIER (OPAMP).....	26
2.25 ANALOG COMPARATOR (COMP)	26
2.26 TEMPERATURE SENSOR (TS).....	27
2.27 CYCLIC REDUNDANCY CHECK CALCULATION UNIT (CRC).....	27
2.28 CRYPTOGRAPHIC ENGINE (CRYE).....	27
2.29 UNIQUE DEVICE SERIAL NUMBER (UID)	28
2.30 SERIAL SINGLE-WIRE JTAG DEBUG PORT (SWJ-DP).....	28
3. PINOUTS AND PIN DESCRIPTION.....	29
3.1 PINOUTS	29
3.1.1 LQFP48.....	29
3.1.2 LQFP64.....	30
3.1.3 LQFP100.....	31
3.2 PIN DESCRIPTION	32
4. ELECTRICAL CHARACTERISTICS.....	40
4.1 PARAMETER CONDITIONS.....	40
4.1.1 Minimum and Maximum Values	40
4.1.2 Typical Values	40

4.1.3 Typical Curves	40
4.1.4 Loading Capacitors	40
4.1.5 Pin Input Voltage	40
4.1.6 Power Supply Scheme.....	42
4.1.6 Current Consumption Measurement	43
4.2 ABSOLUTE MAXIMUM RATING.....	43
4.3 OPERATING CONDITIONS.....	44
4.3.1 General Operating Conditions.....	44
4.3.2 Operating Conditions at Power-on and Power-off.....	44
4.3.3 Embedded Reset and Power Control Module Features	45
4.3.4 Internal Reference Voltage	45
4.3.5 Power Supply Current Characteristics	46
4.3.6 External Clock Source Characteristics	48
4.3.7 Internal Clock Source Characteristics	51
4.3.7.1 High speed internal (HSI) RC oscillator	51
4.3.7.2 Low speed internal (LSI) RC oscillator	51
4.3.8 Time to Wake Up From Low Power Mode.....	52
4.3.9 PLL Characteristics.....	52
4.3.10 FLASH Memory Characteristics.....	52
4.3.11 Absolute Maximum (Electrical Sensitivity).....	53
4.3.12 I/O Port Characteristics	54
4.3.13 NRST Pin Characteristics	57
4.3.14 Timer and Watchdog Characteristics	58
4.3.15 I2C Interface Characteristics	59
4.3.16 SPI/I2S Interface Characteristics	61
4.3.17 QSPI Characteristics	65
4.3.18 SD/SDIO Master Interface Characteristics	66
4.3.19 Controller Area Network (CAN) Interface Characteristics	67
4.3.20 12-bit Analog-to-Digital Converter (ADC) Electrical Parameters.....	68
4.3.21 12-bit Digital-to-Analog Converter (DAC) Electrical Parameters.....	71
4.3.22 Operational Amplifier (OPAMP) Electrical Parameters.....	73
4.3.23 Comparator (COMP) Electrical Parameters.....	73
4.3.24 Temperature Sensor (TS) Characteristics.....	74
5. PACKAGES	75
5.1 LQFP48(7MM X 7MM).....	75
5.2 LQFP64(10MM X 10MM).....	76
5.3 LQFP100(14MM X 14MM).....	77
5.4 MARKING INFORMATION.....	78
6. VERSION HISTORY	79
7. DISCLAIMER.....	80

List of Table

TABLE 1-1 N32A455xxL7 SERIES RESOURCE CONFIGURATION	10
TABLE 2-1 COMPARISON OF TIMER FUNCTION	16
TABLE 3-1 PIN DESCRIPTION	32
TABLE 4-1 VOLTAGE CHARACTERISTIC	43
TABLE 4-2 CURRENT CHARACTERISTIC.....	43
TABLE 4-3 GENERAL OPERATING CONDITIONS	44
TABLE 4-4 OPERATING CONDITIONS AT POWER-ON AND POWER-OFF.....	44
TABLE 4-5 FEATURES OF EMBEDDED RESET AND POWER CONTROL MODULES	45
TABLE 4-6 EMBEDDED REFERENCE VOLTAGE.....	46
TABLE 4-7 MAXIMUM CURRENT CONSUMPTION IN OPERATING MODE RUNNING FROM EMBEDDED FLASH	46
TABLE 4-8 MAXIMUM CURRENT CONSUMPTION IN SLEEP MODE	46
TABLE 4-9 TYPICAL AND MAXIMUM CURRENT CONSUMPTION IN POWERDOWN MODE AND STANDBY MODE.....	47
TABLE 4-10 TYPICAL CURRENT CONSUMPTION IN OPERATING MODE RUNNING FROM EMBEDDED FLASH	48
TABLE 4-11 TYPICAL CURRENT CONSUMPTION IN SLEEP MODE	48
TABLE 4-12 HIGH SPEED EXTERNAL USER CLOCK FEATURES(BYPASS MODE)	48
TABLE 4-13 FEATURES OF A LOW-SPEED EXTERNAL USER CLOCK (BYPASS MODE).....	49
TABLE 4-14 HSE 4~32MHZ OSCILLATOR CHARACTERISTICS ⁽¹⁾⁽²⁾	50
TABLE 4-15 LSE OSCILLATOR CHARACTERISTICS (F _{LSE} =32.768kHz) ⁽¹⁾	50
TABLE 4-16 HSI OSCILLATOR CHARACTERISTICS ⁽¹⁾⁽²⁾	51
TABLE 4-17 LSI OSCILLATOR CHARACTERISTICS ⁽¹⁾	51
TABLE 4-18 WAKE-UP TIME IN LOW POWER MODE	52
TABLE 4-19 PLL FEATURES	52
TABLE 4-20 FLASH MEMORY CHARACTERISTICS	53
TABLE 4-21 FLASH ENDURANCE AND DATA RETENTION	53
TABLE 4-22 ABSOLUTE MAXIMUM ESD VALUE.....	53
TABLE 4-23 ELECTRICAL SENSITIVITY	54
TABLE 4-24 I/O STATIC CHARACTERISTICS.....	54
TABLE 4-25 IO DRIVING CAPABILITY TABLE	55
TABLE 4-26 OUTPUT VOLTAGE CHARACTERISTIC.....	55
TABLE 4-27 OUTPUT AC CHARACTERISTICS ⁽¹⁾	56
TABLE 4-28 NRST PIN CHARACTERISTICS	57
TABLE 4-29 TIM1/8 CHARACTERISTICS ⁽¹⁾	58
TABLE 4-30 TIM2/3/4/5 CHARACTERISTICS ⁽¹⁾	59
TABLE 4-31 IWDG COUNTING MAXIMUM AND MINIMUM RESET TIME (LSI = 40 KHz).....	59
TABLE 4-32 WWDG COUNTING MAXIMUM AND MINIMUM RESET TIME (APB1 PCLK1 = 36MHz).....	59
TABLE 4-33 I ² C INTERFACE CHARACTERISTICS	60
TABLE 4-34 SPI1 FEATURES ⁽¹⁾	61
TABLE 4-35 SPI2/3 FEATURES ⁽¹⁾	61
TABLE 4-36 I ² S CHARACTERISTICS ⁽¹⁾	64
TABLE 4-37 CHARACTERISTICS OF QSPI IN SDR MODE	65
TABLE 4-38 CHARACTERISTICS OF QSPI IN DDR MODE.....	66
TABLE 4-39 SD/MMC INTERFACE FEATURES	67
TABLE 4-40 ADC CHARACTERISTICS	68
TABLE 4-41 ADC SAMPLING TIME ⁽¹⁾⁽²⁾	68
TABLE 4-42 ADC ACCURACY-LIMITED TEST CONDITIONS ⁽¹⁾⁽²⁾	69
TABLE 4-43 DAC CHARACTERISTICS	72
TABLE 4-44 OPAMP CHARACTERISTICS ⁽¹⁾	73
TABLE 4-45 COMP CHARACTERISTIC	74
TABLE 4-46 TEMPERATURE SENSOR CHARACTERISTICS	74

List of Figures

FIGURE 1-1 BLOCK DIAGRAM OF N32A455XXL7 SERIES	8
FIGURE 1-2 N32A455XXL7 SERIES PART NUMBER INFORMATION	9
FIGURE 2-1 MEMORY MAP	11
FIGURE 2-2 CLOCK TREE.....	13
FIGURE 3-1 N32A455XXL7 SERIES LQFP48 PINOUT	29
FIGURE 3-2 N32A455XXL7 SERIES LQFP64 PINOUT	30
FIGURE 3-3 N32A455XXL7 SERIES LQFP100 PINOUT.....	31
FIGURE 4-1 LOAD CONDITIONS OF PINS	40
FIGURE 4-2 PIN INPUT VOLTAGE	41
FIGURE 4-3 POWER SUPPLY SCHEME.....	42
FIGURE 4-4 CURRENT CONSUMPTION MEASUREMENT SCHEME.....	43
FIGURE 4-5 AC TIMING DIAGRAM OF HIGH-SPEED EXTERNAL CLOCK SOURCE	49
FIGURE 4-6 AC TIMING DIAGRAM OF EXTERNAL LOW-SPEED CLOCK SOURCE	49
FIGURE 4-7 TYPICAL APPLICATION USING 8MHZ CRYSTAL	50
FIGURE 4-8 TYPICAL APPLICATION USING 32.768KHZ CRYSTAL ⁽¹⁾⁽²⁾	51
FIGURE 4-9 INPUT OUTPUT AC CHARACTERISTIC DEFINITION.....	57
FIGURE 4-10 TRANSMISSION DELAY	57
FIGURE 4-11 RECOMMENDED NRST PIN PROTECTION.....	58
FIGURE 4-12 I ² C BUS AC WAVEFORM AND MEASUREMENT CIRCUIT ⁽¹⁾	60
FIGURE 4-13 SPI TIMING DIAGRAM-SLAVE MODE AND CLKPHA=0.....	62
FIGURE 4-14 SPI TIMING DIAGRAM-SLAVE MODE AND CLKPHA=1 ⁽¹⁾	63
FIGURE 4-15 SPI TIMING DIAGRAM-MASTER MODE ⁽¹⁾	63
FIGURE 4-16 I ² S SLAVE MODE TIMING DIAGRAM (PHILIPS PROTOCOL) ⁽¹⁾	65
FIGURE 4-17 I ² S MASTER MODE TIMING DIAGRAM (PHILIPS PROTOCOL) ⁽¹⁾	65
FIGURE 4-18 TIMING OF QSPI IN SDR MODE.....	66
FIGURE 4-19 TIMING OF QSPI IN DDR MODE	66
FIGURE 4-20 SDIO HIGH-SPEED MODE	67
FIGURE 4-21 SD DEFAULT MODE.....	67
FIGURE 4-22 ADC PRECISION CHARACTERISTICS	70
FIGURE 4-23 TYPICAL CONNECTION DIAGRAM USING ADC.....	70
FIGURE 4-24 DECOUPLING CIRCUIT OF POWER SUPPLY AND REFERENCE POWER SUPPLY (V _{REF+} IS NOT CONNECTED TO V _{DDA}).....	71
FIGURE 4-25 DECOUPLING CIRCUIT OF POWER SUPPLY AND REFERENCE POWER SUPPLY (V _{REF+} IS CONNECTED WITH V _{DDA}).....	71
FIGURE 5-1 LQFP48 PACKAGE DIMENSIONS	75
FIGURE 5-2 LQFP64 PACKAGE DIMENSIONS	76
FIGURE 5-3 LQFP100 PACKAGE DIMENSIONS	77
FIGURE 5-4 MARKING INFORMATION	78

1. Introduction

The N32A455xxL7 microcontrollers family features a high-performance 32-bit ARM Cortex™-M4F core with an integrated floating point operation unit (FPU) and digital signal processing (DSP). It supports parallel computing instructions and operates at a maximum frequency of 144MHz. The embedded encrypted memory Flash can hold up to 512KB, supporting multi-user partition permission management. Additionally, it includes up to 144KB of embedded SRAM.

The device is equipped with internal high-speed AHB bus, along with two low-speed peripherals clock buses APB and bus matrix. It offers support up to 80 general I/Os and features a diverse range of high-performance analog interfaces. These include 4x 12-bit 5MSPS ADC with up to 38 external input channels, 2x 12-bit DAC with a 1MSPS sampling rate, 4x independent rail-to-rail operational amplifiers, as well as up to 7 high-speed comparators interfaces.

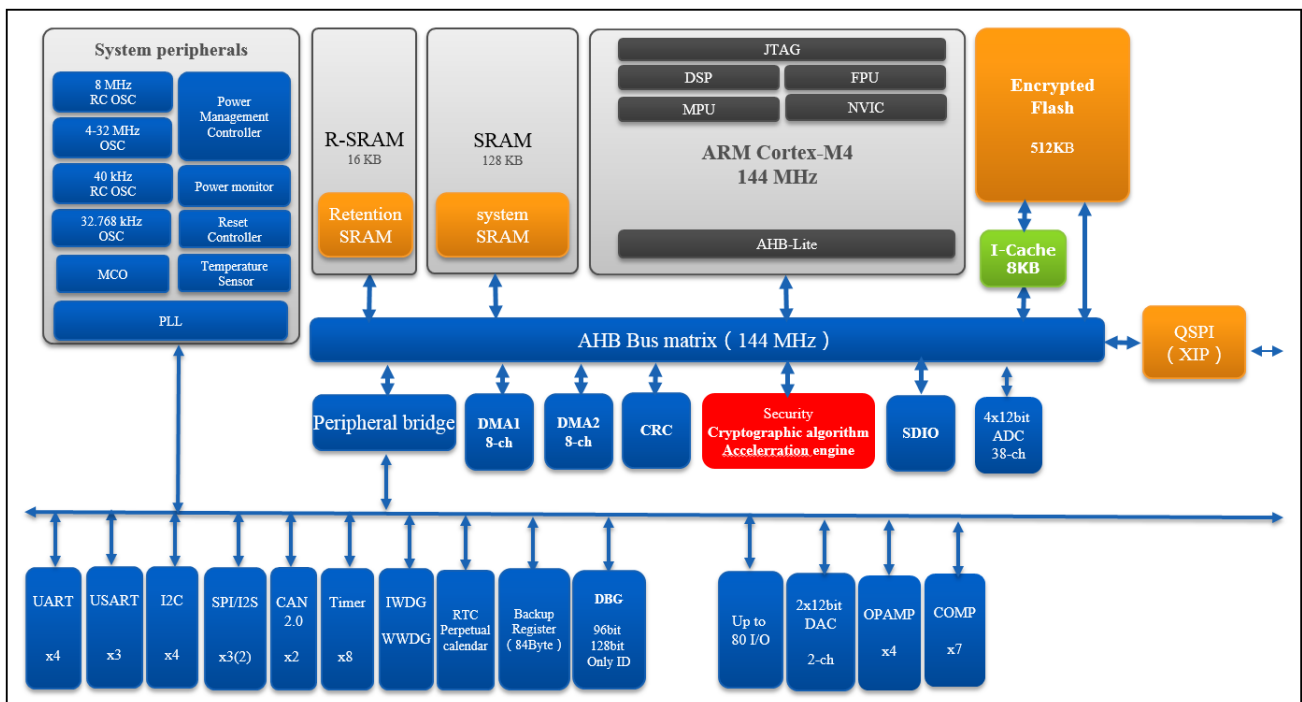
For digital communication, the N32A455xxL7 provides 7x U(S)ART, 4x I2C, 3x SPI, 2x I2S, 1x QSPI, 2x CAN 2.0B, 1x SDIO communication interfaces. It also integrates a hardware acceleration engine, supporting various international encryption algorithms.

The N32A455xxL7 operates reliably in the temperature range of -40°C to +105°C and supply voltage from 1.8V to 3.6V. It offers multiple power modes to cater to low-power applications. Available in 3 different packaging forms from 48 pins to 100 pins, the peripheral configuration varies based on the package type.

These rich peripheral configurations make the N32A455xxL7 series microcontrollers suitable for various application scenarios, including car window controllers (door control; sunroof/sunshade control; electric tailgate control; electric pedal control), light controllers (AFS; ambient light control), air conditioning control systems (HVAC; new energy vehicle PTC; commercial vehicle PTC; commercial vehicle SCR), car motor controllers (electronic water pump; electronic fuel pump; commercial vehicle urea pump) and others (TPMS; receiver; seat control; reverse radar; instrument monitoring MCU; EDR).

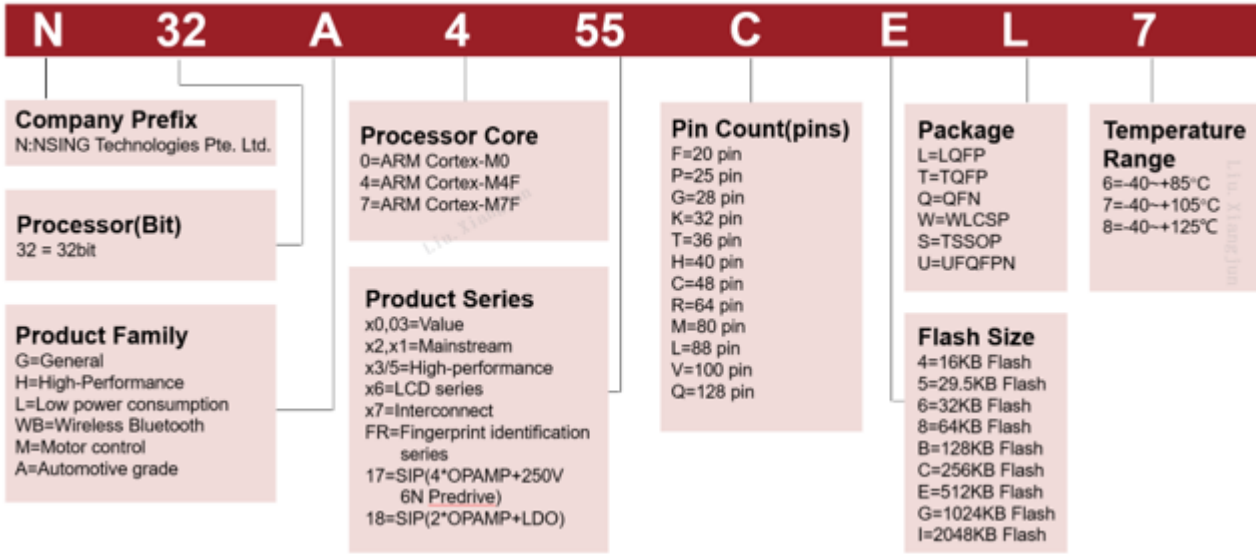
Figure 1-1 the block diagram of this series of products is given.

Figure 1-1 Block Diagram Of N32A455xxL7 Series



1.1 Naming Convention

Figure 1-2 N32A455CEL7 Series Part Number Information



1.2 Product Configurations

Table 1-1 N32A455xxL7 Series Resource Configuration

Device		N32A455CEL7	N32A455REL7	N32A455VEL7
Flash Capacity (KB)		512		
SRAM Capacity (KB)		144		
CPU Frequency		ARM Cortex-M4F @144MHz,180DMIPS		
Operating Environment		1.8~3.6V/-40~105°C		
Timers	General	4		
	Advanced	2		
	Basic	2		
Communication interfaces	SPI ⁽¹⁾	3		
	I2S ⁽¹⁾	2		
	QSPI	Only Single Wire	1	
	I2C	3	4	
	USART	3		
	UART	3	4	
	CAN	2		
	SDIO	No	1	
	GPIO	37	51	80
DMA		2		
DMA Channels		16Channel		
12bit ADC		4	4	4
ADC Channels		16Channel	22Channel	38Channel
12bit DAC		2		
DAC Channels		2Channel		
OPAMP/COMP		4/5	4/7	4/7
Algorithm Support		DES/3DES、AES、SHA1/SHA224/SHA256、SM1、SM3、SM4、SM7、MD5、CRC16/CRC32、TRNG		
Security Protection		Read-write protection (RDP/WRP), Storage encryption, Partition protection, Secure boot		
Package		LQFP48	LQFP64	LQFP100

Note: ⁽¹⁾SPI2 and SPI3 interfaces can flexibly switch between SPI mode and I2S audio mode.

2. Function Overview

2.1 Processor Core

The N32A455xxL7 series integrates the latest generation of embedded ARM Cortex™-M4F processor. It features a floating point processing unit (FPU), DSP and parallel computing instructions, providing excellent performance of 1.25DMIPS/MHz. At the same time, its efficient signal processing capabilities are combined with low power consumption, low cost, and ease of use. It is able to be used in application scenarios that require a blend of control and signal processing capabilities while being user-friendly.

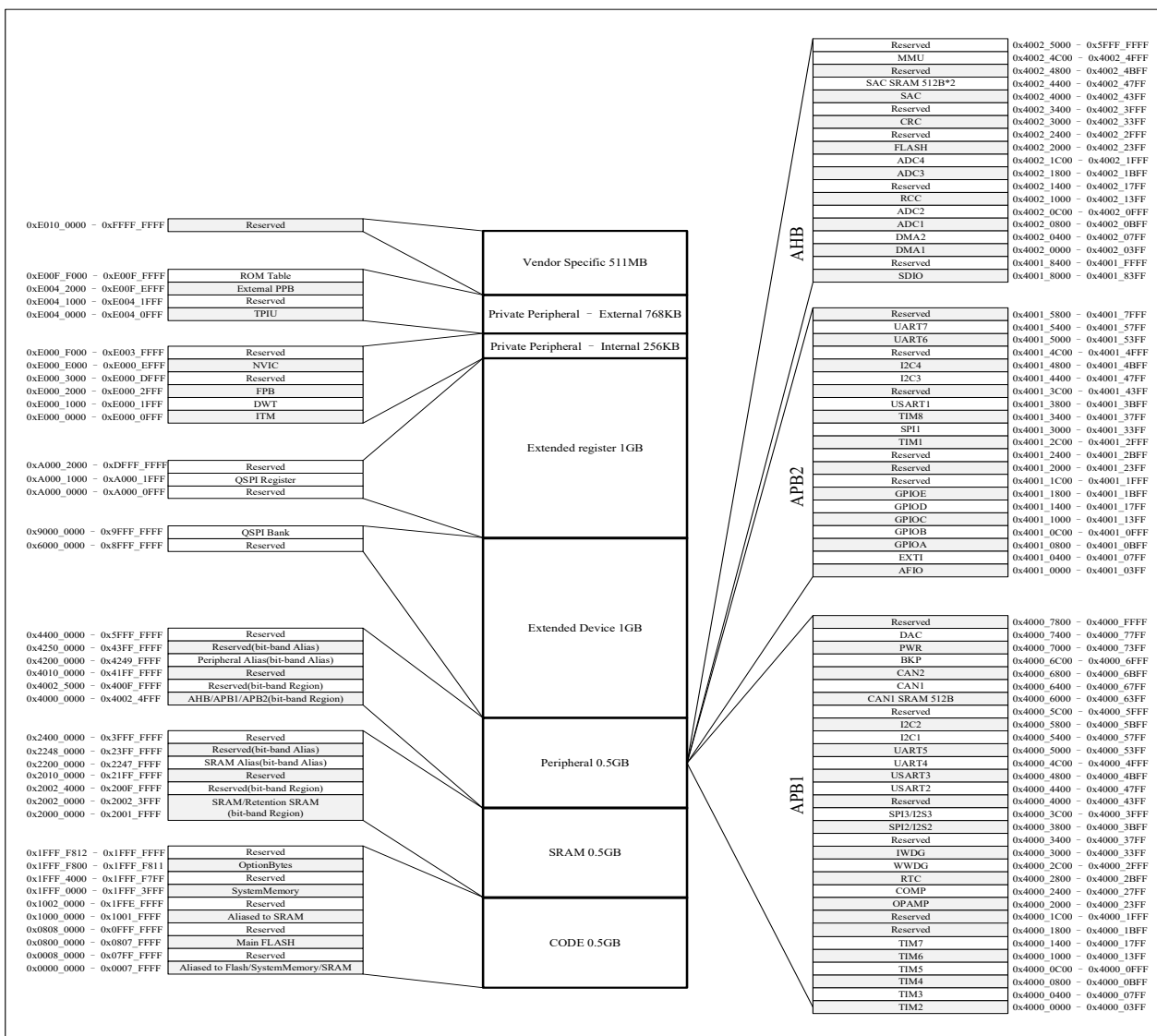
ARM Cortex™-M4F 32-bit reduced instruction set processor offers exceptional code efficiency.

Note: Cortex™-M4F is backward compatible with Cortex-M3 code.

2.2 Memories

The N32A455xxL7 series include embedded encrypted Flash memory and embedded SRAM.

Figure 2-1 Memory Map



2.2.1 Embedded FLASH Memory

The integrated 512K bytes embedded encryption FLASH memory, utilized for storing programs and data. The page size is 2K byte supporting page erasing, word writing, word reading, half-word reading, and byte reading operations.

It supports storage encryption protection, enabling automatic encryption during writing and reading(including program execution operation).

User partition management is supported, allowing for a maximum of two user partitions, different users cannot access each other's data (only executable code can be accessed).

2.2.2 Embedded SRAM

The chip integrates a built-in SRAM of up to 144K bytes, comprising SRAM and Retention SRAM(Ret-SRAM). Ret-SRAM has a size of 16K bytes and can retain data in STOP2 and STANDBY modes. (user-configurable to retain or not retain data);

2.2.3 Nested Vector Interrupt Controller (NVIC)

The built-in Nested Vector Interrupt Controller can handle up to 86 maskable interrupt channels (excluding the 16 Cortex™-M4F interrupts) and 16 priorities.

- The tightly coupled NVIC ensures low-latency interrupt response processing
- Interrupt vector entry address directly access the kernel
- Tightly coupled NVIC interface
- Allows early processing of interrupts
- Processing late arriving higher-priority interrupts
- Support interrupt tail-chaining functionality
- Automatically saves processor state
- Automatically resumes when interrupt returns with no instruction overhead

This module offers flexible interrupt management with minimal interrupt latency.

2.3 Extended Interrupt/Event Controller (EXTI)

The extended interrupt/event controller contains 21 edge detectors for generating interrupt/event requests. Each interrupt line can be independently configured with its trigger event (rising edge, falling edge or both) and can be individually masked. A pending register maintains the state of all interrupt requests. EXTI can detect clock pulse with width smaller than internal APB2. Up to 80 general purpose I/O ports are connected to 16 external interrupt lines.

2.4 Clock System

The device offers various clock options for users to choose from, including:

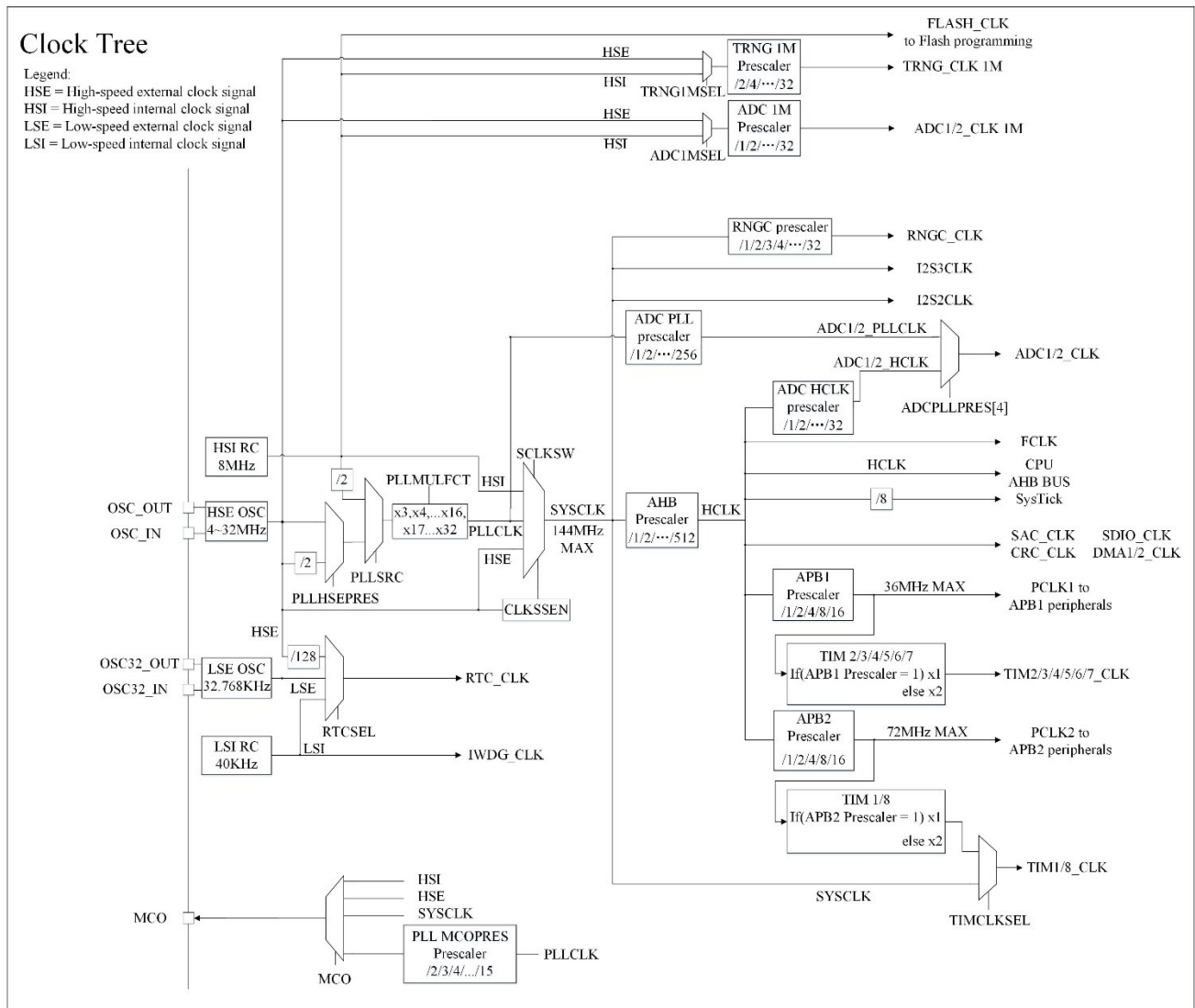
- High speed internal RC oscillator (HSI) at 8MHz.
- Low-speed internal RC oscillator (LSI) at 40KHz
- High speed external crystal oscillator (HSE) ranging from 4MHz~32MHz
- Low speed external crystal oscillator (LSE) at 32.768KHz
- Phase-Locked Loop (PLL).

Upon reset, the internal HSI clock is set as the default CPU clock, user can choose the external HSE clock with failure function. When an external clock failure is detected, it will be isolated, the system will automatically switch to HSI.

If interrupts are enabled, software can receive corresponding interrupt. Similarly, security interrupt management of the PLL clock can be adopted when needed (such as when an indirectly used external oscillator fails).

Multiple prescalers are used to configure the AHB frequency, high-speed APB (APB2) and low-speed APB(APB1) regions. The AHB has a maximum frequency of 144 MHz, APB2 has a maximum frequency of 72 MHz and APB1 has a maximum frequency of 36MHz. Refer to Figure 2-2 Clock tree diagram.

Figure 2-2 Clock Tree



1. When HSI is used as the input of the PLL clock, the highest system clock frequency can only reach 128MHz.

2.5 Boot Modes

During startup, the BOOT mode after reset can be selected through the BOOT0/1 pin.

- Boot from FLASH Memory.
- Boot from System Memory
- Boot from embedded SRAM

The Bootloader is stored in the system memory and can program the flash memory through USART1 interface.

2.6 Power Supply Scheme

- $V_{DD}= 1.8\sim 3.6V$, V_{DD} pin supplies power to the I/O pin and internal voltage regulator.
- $V_{DDA}= 1.8\sim 3.6V$, the V_{DDA} provides power supply for ADC, DAC, OPAMP, COMP.
- V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS} respectively.
- $V_{BAT}= 1.8\sim 3.6V$: When V_{DD} is turned off, it supplies power to RTC, external 32KHz oscillator and backup register.

For more information on how to connect the power supply pins, see Figure 4-3 Power supply scheme.

2.7 Reset

The power-on reset (POR) and power-down reset (PDR) circuits are integrated inside the device. This part of the circuit ensures that the system works stably when the power supply exceeds 1.8V. When V_{DD} falls below a set threshold ($V_{POR/PDR}$), the device goes into reset without using an external reset circuit.

2.8 Programmable Voltage Detector

The device has a built-in programmable voltage detector (PVD), which monitors the power supply of V_{DD}/V_{DDA} and compares it with the threshold V_{PVD} . When V_{DD} is lower or higher than the threshold V_{PVD} , an interrupt will be generated. The interrupt handler can send a warning message, and the PVD function needs to be enabled through the program. See Table 4-5 for values of $V_{POR/PDR}$ and V_{PVD} .

2.9 Voltage Regulator

The voltage regulator operates in the follow modes:

- The MCU operates in RUN, SLEEP modes: Main voltage regulator(MR) operates in normal mode
- The MCU operates in STOP0 modes: Main voltage regulator(MR) can select to operate in normal mode or in low power mode
- MCU operates in STOP2, STANDBY mode: Main voltage regulator(MR) shut down and backup domain voltage regulator(BKR) turn on

After the chip is reset, the main voltage regulator(MR) operates in normal mode by default.

2.10 Low Power Mode

The N32A455xxL7 series supports five low power consumption modes.

- SLEEP mode

In SLEEP mode, only the CPU is stopped, all peripherals remain operational. They can wake up the CPU when an interrupt/event occurs.

- STOP0 mode

In STOP0 mode, the device can achieve lower power consumption while maintaining the contents of SRAM and registers. In this mode, the clocks in the main power domain are turned off, such as PLL, HSI, HSE, and the main voltage regulator can select to operate in normal mode or in low power mode.

Wake-up: The device can be woken up from STOP0 mode by any of the 16 external EXTI signals (I/O related), PVD output, RTC wake-up, RTC alarm, touch wake-up signal..

- STOP2 mode

In STOP2 mode all the core digital logic areas are powered off.

- The Main voltage regulator (MR) is turned off.

- HSE/HSI/PLL is turned off.
- CPU registers are retained.
- LSE/LSI can be configured to operate
- GPIOs are retained
- The peripheral I/O multiplexing functions are not retained
- The 16K-Byte R-SRAM can be retained while the data in other SRAM and registers will be lost.
- The 84-byte backup registers are retained

Wake-up: The device can be woken up from STOP2 mode by any of the 16 external EXTI signals (I/O related), PVD output, RTC periodic wake-up, RTC alarm, RTC tamper, NRST reset, IWDG reset.

- STANDBY mode

In STANDBY mode, the device can achieve a lower current consumption. The internal voltage regulator is turned off, as well as PLL, HSI RC oscillator and HSE crystal oscillator. Upon entering STANDBY mode, the contents of the main domain register will be lost while the contents of the backup register can be retained, R-SRAM can be retained, the STANDBY circuitry continues to function.

External reset signal on NRST, IWDG reset, rising edge on the WKUP pin, RTC wake-up, RTC alarm can wake up the device from STANDBY mode.

- VBAT mode

At any time, whenever VDD is powered down, it will automatically enter VBAT mode. In VBAT mode, except for NRST, PA0-WKUP, PC13_TAMPER, PC14, PC15, most I/O pins are in high impedance state.

Note: RTC, IWDG and corresponding clock will not be stopped when entering STANDBY mode.

2.11 Direct Memory Access (DMA)

The device integrates 2 flexible general-purpose DMA controllers that support 8 DMA channels. It can manage data transfers from memory-to-memory, peripheral-to-memory, and memory-to-peripherals. These 2 DMA controllers support the management of circular buffers, thus avoiding the interrupts when the controller reaches the end of the buffer.

Each channel has dedicated hardware DMA request logic, and each channel can be triggered by software. The transmission length, the source address and the destination address of each channel can be set separately by software.

DMA can be used with major peripherals: SPI, I²C, USART, TIMx(Advanced/General/Basic Timers), DAC, I²S, SDIO, ADC and QSPI.

2.12 Real Time Clock (RTC)

The RTC is a set of continuously running counters integrated with a built-in clock module that provides a perpetual calendar functionality, as well as alarm interrupt and periodic interrupt (with a minimum of 2 clock cycles). The RTC can be powered through V_{DD} or V_{BAT} pin. It is powered by V_{DD} when V_{DD} is valid. Otherwise, it is powered by V_{BAT} pin. The power source is automatically selected and switched by hardware. The RTC will not be reset by system or power reset sources, nor will it be reset when woken up from STANDBY mode.

The RTC can be driven by either a 32.768KHz external crystal oscillator, an internal low-power 40KHz RC oscillator, or a high-speed external clock with 128 prescaler factors.

For application scenarios that requiring very high timing accuracy, it is recommended to use an external 32.768KHz clock as the clock source to compensate for the clock deviation of natural crystals, a 512Hz signal can be output to calibrate the clock of RTC.

The RTC features a 22-bit prescaler for a time-based clock. By default when the clock is set to 32.768kHz, it generates a 1-second time reference. In addition, the RTC can be used to trigger wake-up in low-power mode.

2.13 Timers and Watchdogs

Up to 2 advanced control timers, 4 general-purpose timers and 2 basic timers, as well as 2 watchdog timers and 1 system tick timer.

The following Table compares the functions of advanced control timer, general-purpose timer and basic timer:

Table 2-1 Comparison of Timer Function

Timer	Counter Resolution	Counter Type	Prescaler Factor	Generate DMA Request	Capture/Compare Channels	Complementary Output
TIM1 TIM8	16 bits	Up, Down, Up/Down	Any integer between 1 and 65536	Y	4	Y
TIM2 TIM3 TIM4 TIM5	16 bits	Up, Down, Up/Down	Any integer between 1 and 65536	Y	4	N
TIM6 TIM7	16 bits	Up	Any integer between 1 and 65536	Y	0	N

2.13.1 Basic Timer (TIM6 and TIM7)

Basic timers TIM6 and TIM7 each contain a 16-bit auto-reload counter. These two timers are independent of each other and do not share any resources. The basic timer can provide a time base for general purpose timers. The basic timer is directly connected to the DAC inside the chip and drives the DAC directly through the trigger output.

Main features:

- 16-bit auto-reload up-counting counters
- 16-bit programmable prescaler (The prescaler factor can be configured with any value between 1 and 65536)
- Synchronization circuit for triggering DAC
- Events that generate the interrupt/DMA is as follows:
 - Update event

2.13.2 General-Purpose Timer (TIMx)

The general-purpose timers (TIM2, TIM3, TIM4 and TIM5) are mainly used in the following occasions: counting the input signals, measuring the pulse width of the input signals and generating output waveforms, etc.

Main features:

- 16-bit auto-reload counters. (It can realize up-counting, down-counting, up/down counting)
- 16-bit programmable prescaler. (The prescaler factor can be configured with any value between 1 and 65536)
- TIM2, TIM3, TIM4 and TIM5 up to 4 channels.
- Channel's operating modes: PWM output, output compare, one-pulse mode output, input capture.
- The events that generate the interrupt/DMA are as follows:
 - Update event
 - Trigger event
 - Input capture
 - Output compare
- Timer can be controlled by external signal

- Timers can be linked together internally for timer synchronization or chaining
- Incremental (quadrature) encoder interface: used for tracking motion and resolving rotation direction and position;
- Hall sensor interface: used to do three-phase motor control;
- Supports capture of internal comparator output signals.

2.13.3 Advanced Control Timer (TIM1 and TIM8)

The advanced control timers (TIM1 and TIM8) are mainly used in the following purposes: counting the input signal, measuring the pulse width of the input signal and generating the output waveform, etc.

Advanced timers have complementary output function with dead-time insertion and break function. Suitable for motor control.

Main features:

- 16-bit auto-reload counters. (It can realize up-counting, down-counting, up/down counting).
- 16-bit programmable prescaler. (The prescaler factor can be configured with any value between 1 and 65536)
- Programmable Repetition Counter
- TIM1 and TIM8 up to 6 channels
- 4 capture/compare channels:
 - PWM output
 - Output compare
 - One-pulse mode output
 - Input capture
- The events that generate the interrupt/DMA are as follows:
 - Update event
 - Trigger event
 - Input capture
 - Output compare
 - Break input
- Complementary outputs with programmable dead-time.
 - For TIM1 and TIM8, channel 1,2,3 support this feature
- Timers can be controlled by external signal
- Timers can be linked together internally for timer synchronization or chaining
- TIM1_CC5 and TIM8_CC5 for COMP blanking.
- TIM1_CC6 is used to switch the input channel of OPAMP1 and OPAMP2; TIM8_CC6 is used to switch the input channel of OPAMP3 and OPAMP4;
- Incremental (quadrature) encoder interface: used for tracking motion and resolving rotation direction and position;
- Hall sensor interface: used to do three-phase motor control;

2.13.4 SysTick Timer (Systick)

This timer is dedicated to the real-time operating systems and can also be used as a standard down counter.

Main features :

- 24-bit down counter
- Automatic reloading function
- A maskable system interrupt is generated when the counter is 0
- Programmable clock source

2.13.5 Watchdog (WDG)

Support for two watchdog independent watchdog (IWDG) and window watchdog (WWDG). Two watchdogs provide increased security, time accuracy, and flexibility in use.

Independent Watchdog (IWDG)

The independent watchdog is based on a 12-bit down counter and a 3-bit prescaler. It is driven by a separate low-speed RC oscillator that remains active even if the master clock fails and operates in STOP0, STOP2 and STANDBY modes. Once activated, if the watchdog is not fed (clears the watchdog counter) within the set time, the IWDG generates a reset when the counter counts to 0x000. It can be used to reset the entire system in the event of an application problem, or as a free timer to provide time-out management for applications. It is hardware or software configurable through the option bytes. Reset and low power wake up are available.

Window Watchdog (WWDG)

A window watchdog is usually used to detect software failures caused by an application deviating from the normal running sequence due to external interference or unforeseen logical conditions. Unless the down-counter value is flushed before the T6 bit becomes zero, the watchdog circuit generates an MCU reset when the preset time period is reached. If the 7-bit down-counter value (in the control register) is flushed before the down-counter reaches the window register value, then an MCU reset will also occur. This indicates that the down-counter needs to be refreshed in a finite time window.

Main features:

- The clock of the window watchdog (WWDG) is obtained by dividing APB1 clock
- Programmable free-running decrement counter
- Reset condition:
 - When the down-counter is less than 0x40, a reset occurs (if the watchdog is started)
 - A reset occurs when the down-counter is reloaded outside the window (if the watchdog is started)
 - If the watchdog is enabled and interrupts are allowed, an early wake up interrupt (EWINT) occurs when the down-counter equals 0x40, which can be used to reload the counter to avoid WWDG reset

2.14 I2C Bus Interface

The device integrates up to 4 independent I2C bus interfaces, which provide multi-master function and control all I2C bus-specific timing, protocol, arbitration and timeout. I2C bus interface supports multiple communication rate modes (up to 1MHz), supports DMA operations and is compatible with SMBus 2.0. The I2C module provides multiple functions, including CRC generation and verification, System Management Bus (SMBus), and Power Management Bus(PMBus).

Main features :

- Multi-master function: this module can be used as master device or slave device;
- I2C master device function:
 - Generate a clock;
 - Generate start and stop signals;
- I2C slave device function:

- Programmable address detection;
- The I2C interface supports 7-bit or 10-bit addressing and dual-slave address response capability in 7-bit slave mode.
- Stop bit detection;
- Generate and detect 7-bit / 10-bit addresses and broadcast calls;
- Support different communication speeds;
 - Standard speed (up to 100 kHz);
 - Fast (up to 400 kHz);
 - Fast + (up to 1MHz);
- Status flags:
 - Transmitter/receiver mode flag;
 - Byte transfer complete flag;
 - I2C bus busy flag;
- Error flags:
 - Arbitration loss in Master mode
 - Acknowledge (ACK) error after address/data transfer;
 - Error start or stop condition detected
 - Overrun or underrun when clock extending is disable;
- Two interrupt vectors:
 - 1 interrupt for address/data communication success;
 - 1 interrupt for an error;
- Optional extend clock function
- DMA of single-byte buffers;
- Generation or verification of configurable PEC(Packet error checking)
- In transmit mode, the PEC value can be transmitted as the last byte
- PEC error check for the last received byte
- SMBus 2.0 compatible
 - Timeout delay for 25ms clock low
 - 10ms accumulates low clock extension time of master device
 - 25ms accumulates low clock extension time of slave device
 - PEC generation/verification of hardware with ACK control
 - Support address resolution protocol (ARP)
- Compatible with the PMBus

2.15 Universal Synchronous/Asynchronous Transceiver (USART)

The N32A455xxL7 series products integrate up to 7 serial transceiver interfaces, including 3 universal synchronous/asynchronous transceivers (USART1/USART2/USART3) and 4 universal asynchronous transceivers (UART4/UART5/UART6/UART7). All 7 interfaces provide asynchronous communication, support for IrDA SIR ENDEC

transmission codec, multi-processor communication mode, single-line half-duplex communication mode, and LIN master/slave function.

The communication rate of USART1/USART6/USART7 interface can reach 4.5Mbit/s, and the communication rate of other interfaces can reach 2.25Mbit/s.

The USART1, USART2 and USART3 interfaces have hardware CTS and RTS signal management, ISO7816-compatible Smartcard mode, and similar to SPI communication mode, all of which can use DMA operations.

Main features:

- Full duplex, asynchronous communication
- NRZ standard format
- Fractional baud rate generator system, baud rate programmable, used for sending and receiving, up to 4.5 Mbit/s
- Programmable data word length (8 or 9 bits)
- Configurable stop bit, supporting 1 or 2 stop bits
- LIN master's ability to send synchronous interrupters and LIN slave's ability to detect interrupters. When USART hardware is configured as LIN, it generates 13 bit interrupters and detects 10/11 bit interrupters
- Output clock for synchronous transmission
- IRDA SIR encoder decoder, supports 3/16 bit duration in normal mode
- Smart card simulation function
 - The smart card interface supports the asynchronous smart card protocol defined in ISO7816-3
 - 0.5 and 1.5 stop bits for smart cards
- Single-wire half duplex communication
- Configurable multi-buffer communication using DMA, receiving/sending bytes in SRAM using centralized DMA buffer
- Independent transmitter and receiver enable bits
- Detection flag
 - Receive buffer is full
 - Send buffer empty
 - Transmission complete
- Parity control
 - Send parity bit
 - Check the received data
- Four error detection flags
 - Overflow error
 - Noise error
 - Frame error
 - Parity error
- 10 USART interrupt sources with flags
 - CTS change
 - LIN break detection
 - Send data register is empty

- Send complete
- Received data register is full
- Bus was detected to be idle
- Overflow error
- Frame error
- Noise error
- Parity the error
- Multi-processor communication, if the address does not match, then enter the silent mode;
- Wake up from silent mode (via idle bus detection or address flag detection)
- Mode configuration:

USART Modes	USART1	USART2	USART3	UART4	UART5	UART6	UART7
Asynchronous mode	Y	Y	Y	Y	Y	Y	Y
Hardware flow control	Y	Y	Y	N	N	N	N
Multi buffer communication (DMA)	Y	Y	Y	Y	Y	Y	Y
Multiprocessor communication	Y	Y	Y	Y	Y	Y	Y
Synchronize mode	Y	Y	Y	N	N	N	N
Smartcard mode	Y	Y	Y	N	N	N	N
Half duplex (single wire mode)	Y	Y	Y	Y	Y	Y	Y
IrDA	Y	Y	Y	Y	Y	Y	Y
LIN	Y	Y	Y	Y	Y	Y	Y

2.16 Serial Peripheral Interface (SPI)

The device integrates 3 SPI interfaces, which allow the chip to communicate with peripheral devices in a half/full duplex, synchronous, serial manner. This interface can be configured in master mode and provides a communication clock (SCK) for external slave devices. Interfaces can also work in a multi-master configuration. It can be used for a variety of purposes, including two-line simplex synchronous transmission using a two-way data line, and reliable communication using CRC checks.

Main features:

- 3-wire full-duplex synchronous transmission
- Two-wire simplex synchronous transmission with or without a third bidirectional data line
- 8 or 16 bit transmission frame format selection
- Master or slave operations
- Support multi-master mode
- 8 master mode baud rate prescaler coefficient (Max $f_{PCLK}/2$)
- Slave mode frequency (Max $f_{PCLK}/2$)
- Fast communication between master mode and slave mode
- NSS can be managed by software or hardware in both master and slave modes: dynamic change of master/slave modes
- Programmable clock polarity and phase
- Programmable data order, MSB before or LSB before
- Dedicated send and receive flags that trigger interrupts
- SPI bus busy flag;
- Hardware CRC for reliable communication;

- In send mode, the CRC value can be sent as the last byte;
- In full-duplex mode, CRC is automatically performed on the last byte received.
- Master mode failures, overloads, and CRC error flags that trigger interrupts
- Single-byte send and receive buffer with DMA capability: generates send and receive requests
- Maximum speed: 36Mbps for SPI1 interface and 18Mbps for SPI2/SPI3 interface

2.17 Serial Audio Interface (I2S)

I²S is a 3-pin synchronous serial interface communication protocol. The device integrates 2 standard I2S interfaces (multiplexed with SPI) and can operate in master or slave mode. The 2 interfaces can be configured for 16-bit, 24-bit or 32-bit transmission, or as input or output channels, supporting audio sampling frequencies from 8KHz to 96KHz. It supports four audio standards, including Philips I²S, MSB and LSB alignment, and PCM.

In half duplex communication, it can operate in two modes: master and slave mode. When it acts as a master device, it provides clock signals to external slave devices through an interface.

Main features:

- Simplex communication (send or receive only)
- Master or slave operations
- 8-bit linear programmable prescaler for accurate audio sampling frequencies (8 KHZ to 96KHz)
- The data format can be 16, 24, or 32 bits
- Audio channel fixed packet frame is 16 bit (16 bit data frame) or 32 bit (16, 24 or 32 bit data frame)
- Programmable clock polarity (steady state)
- The overflows flag bit in slave sending mode and the overflows flag bit in master/slave receiving mode
- 16-bit data registers are used for sending and receiving, with one register at each end of the channel
- Supported I²S protocols:
 - I²S Philips standard
 - MSB alignment standard (left aligned)
 - LSB alignment standard (right aligned)
 - PCM standard (16-bit channel frame with long or short frame synchronization or 16-bit data frame extension to 32-bit channel frame)
- The data direction is always MSB first
- Both send and receive have DMA capability
- The master clock can be output to external audio devices at a fixed rate of 256xFs(Fs is the audio sampling frequency)

2.18 Quad Serial Peripheral Interface (QSPI)

The device integrates with 1 channel QSPI in single-master mode, can operate in two modes:

- Memory mapping mode.
- Indirect mode

Main features:

- Can be configured to Single SPI/Dual SPI/Quad SPI mode. In Single mode, it supports standard SPI operation and can operate in half-duplex and full-duplex modes

- The operation mode of QSPI can be configured in indirect mode or memory mapping mode. The command code in the instruction stage can be configured, and the alternate byte or mode byte in the alternate byte stage or mode stage can be configured
- Support 8-bit, 16-bit, 32-bit data access mode
- Data transceiver FIFO
- Support DMA operation
- Support FIFO interrupt, operation completion interrupt, timeout interrupt, data access error interrupt
- Maximum speed:4×36Mbps
- In indirect mode or memory mapping mode, the operation is divided into instruction stage, address stage, alternate byte stage, Dummy stage, and data stage. These stages can be configured to be skipped.

2.19 Secure Digital Input Output Interface (SDIO)

Secure Digital Input and Output (SDIO) provides an operation interface between AHB peripheral bus and Multimedia Card (MMC), SD memory card, SDIO card devices.

Main features:

- Support "MultiMediaCard System Specification Version 4.2", support 1-bit (default), 4-bit and 8-bit data bus
- Compatible with earlier MMC protocol
- Support "SD Memory Card Specifications Version 2.0"
- Support "SD I/O Card Specification Version 2.0", support 1-bit (default) and 4-bit data format
- The clock rate of SDIO is up to 48MHz
- SDIO does not support SPI communication

2.20 Controller Area Network (CAN)

The device integrates 2 CAN bus interfaces compatible with 2.0A and 2.0B (active) specifications, with bit rates up to 1Mbps. It can receive and send standard frames with 11-bit identifiers, as well as extended frames with 29-bit identifiers.

Main features:

- Support CAN protocol 2.0A and 2.0B active mode
- Baud rate up to 1Mbps
- Supports time-triggered communication
- Transmit
 - 3 sending mailboxes
 - The priority of sent packets can be configured by software
 - Records the timestamp of the time when the SOF was sent
- Receive
 - Level 3 depth of 2 receiving FIFO
 - Variable filter group:
 - There are 14 filter groups
 - Identifier list

- The FIFO overflow processing mode is configurable
- Record the time stamp of the receipt for the SOF
- Time-triggered communication mode
 - Disable automatic retransmission mode
 - 16-bit free run timer
 - Timestamp can be sent in the last 2 bytes of data
- Management
 - Interrupt masking
 - The mailbox occupies a separate address space to improve software efficiency

2.21 General Purpose Input/Output Interface (GPIO)

Up to 80 GPIOs, which can be divided into 5 groups (GPIOA/GPIOB/GPIOC/GPIOD/GPIOE). Each group has 16 ports. Each GPIO pin can be configured by software as an output (push pull or open drain), input (with or without pull-up/pull-down), or alternate peripheral function port. Most GPIO pins are shared with digital or analog alternate peripherals, and some I/O pins are multiplexed with clock pins. All GPIO pins have high current passing capability except ports with analog input capability.

Main features:

- Each bit of the GPIO port can be configured separately by the software into multiple modes:
 - Input floating
 - Input pull up (weak pull up)
 - Input pull down (weak pull down)
 - Analog function
 - Open drain output
 - Push-pull output
 - Push-pull alternate function
 - Open drain alternate function
- General I/O (GPIO)
 - During and just after reset, the alternate functions are not enabled, except for BOOT0 /BOOT1(which are placed in input pull-down mode) and NRST pin, the I/O port is configured to analog input mode.
 - During and just after reset, the alternate function is not turned on, the I/O port is configured as analog input mode, and after reset, the JTAG pin is placed in input pull-up or pull-down mode:
 - JTDI in pull-up mode;
 - JTCK in pull-down mode;
 - JTMS in pull-up mode;
 - NJTRST in pull-up mode
 - When configured as output, values written to the output data registers are output to the appropriate I/O pins. It can be output in push-pull mode or open-drain mode
- Separate bit setting or bit clearing functions
- External interrupt/wake up: All ports have external interrupt capability. In order to use external interrupts, ports must be configured in input mode

- Alternate function: port configuration register must be programmed before using default alternate function
- GPIO lock mechanism, which freezes I/O configurations. When a LOCK is performed on a port bit, the configuration of the port bit cannot be changed until the next reset

2.22 Analog/Digital Converter (ADC)

The device supports four 12-bit successive approximation ADCs with a sampling rate of 4.7Msps. It supports both single-ended and differential inputs, capable of measuring 38 external and 7 internal signal sources. ADC1 support 9 external channels, ADC2 supports 12 external channels, ADC3 supports 15 external channels, ADC4 supports 13 external channels.

Main features:

- Support 12/10/8/6-bit resolution configurable
 - The highest sampling rate at 12bit resolution is 4.7MSPS
 - The maximum sampling rate at 10bit resolution is 6.1MSPS
 - The maximum sampling rate at 8bit resolution is 7.3MSPS
 - The maximum sampling rate at 6bit resolution is 8.9MSPS
- ADC clock source is divided into operating clock source, sampling clock source and timing clock source
 - AHB_CLK can be configured as the operating clock source, up to 144MHz
 - PLL can be configured as a sampling clock source, up to 80MHZ, support 1,2,4,6,8,10,12,16,32, 64,128,256 frequency division
 - AHB_CLK can be configured as the sampling clock source, up to 80MHz, and supports frequency 1,2,4,6,8,10,12,16,32
 - The timing clock is used for internal timing functions and the frequency must be configured to 1MHz
- Supports timer trigger ADC sampling
- Interrupts when conversion ends, injection conversion ends, and analog watchdog events occur
- Single and continuous conversion modes
- Automatic scan mode from channel 0 to channel N
- Support for self-calibration
- Data alignment with embedded data consistency
- Sampling intervals can be programmed separately by channel
- Both regular conversions and injection conversions have external triggering options
- Continuous mode
- Dual ADC mode, combine ADC1 with ADC2, combine ADC3 and ADC4
- ADC power supply requirements: 1.8V to 3.6V
- ADC input range: $V_{REF-} \leq V_{IN} \leq V_{REF+}$
- ADC can use DMA operations, and DMA requests are generated during regular channel conversion.
- Analog watchdog function can monitor one, multiple, or all selected channels with great precision. When the monitored signal exceeds the preset threshold, an interruption will occur.

2.23 Digital/Analog Converter (DAC)

The device integrates 2x digital-to-analog converters (DAC), which are 12-bit digital input and voltage output

digital/analog converter. The DAC has 2 output channels, each channel has a separate converter, and the 2 DAC can be used at the same time without affecting each other. The DAC can input the reference voltage(VREF+) through the pin to obtain more accurate conversion results.

Main features:

- 2 DAC converters: each with an output channel
- Configurable 8-bit or 12-bit output
- Configurable left or right data alignment in 12-bit mode
- Update function
- Generation of noise wave
- Generation of triangular wave
- Dual DAC channel, supports independent or synchronous conversion
- DMA support.
- External trigger for conversion
- Input voltage VREF+

2.24 Operational amplifier (OPAMP)

The device integrates up to 4 independent operational amplifiers with multiple operating modes such as external amplification, internal follower, programmable amplifier (PGA) and other operating modes (or both internal amplification and external filtering).

Main features:

- Support rail-to-rail input/output
- Can be configured as an independent OPAMP and programmable gain OPAMP
- Forward and reverse input checkboxes
- The operating mode of OPAMP can be configured as:
 - Independent mode (external gain setting)
 - PGA mode, programmable gain ranging of 2X, 4X, 8X, 16X, 32X
 - Follower mode
- The internally connected ADC channel is used to measure the output signal of operational amplifier

2.25 Analog comparator (COMP)

The device integrates up to 7 comparators. It can be used as a separate device (all ports of the comparator are plugged into the I/O) or in combination with a timer. In the case of motor control, it can be combined with the PWM output from the timer to form periodic current control.

The main functions of comparator are as follows:

- Rail to rail comparators are supported
- The reverse and forward sides of the comparator support the following inputs
 - Optional I/O
 - DAC channel output
 - Internal adjustable voltage input (there are 2 internal adjustable voltages VREF1, VREF2, shared by all 7 comparators), 64-level uniform adjustment based on V_{DDA}

- Programmable hysteresis can be configured as no hysteresis, low hysteresis, medium hysteresis, and high hysteresis
 - The comparator can output to I/O or timer input for triggering
 - Capture events
 - OCREF_CLR events (for periodic current control)
 - Brake events
 - The comparator supports output filtering, including analog and digital filtering
 - COMP1/COMP2, COMP3/COMP4 and COMP5/COMP6 can form a window comparator
 - Support comparator output with blanking, you can choose to disable blanking or choose Timer1_OC5/Timer8_OC5 as blanking input
 - Each comparator can have interrupt wake up capability, support from SLEEP mode wake up

2.26 Temperature Sensor (TS)

The temperature sensor produces a voltage that varies linearly with temperature in range of $1.8V < V_{DDA} < 3.6V$. The temperature sensor is internally connected to the input channel of ADC1_IN16 for converting the output of the sensor to a digital value.

2.27 Cyclic Redundancy Check Calculation Unit (CRC)

The device integrates CRC32 and CRC16 functionalities. The cyclic redundancy check (CRC) calculation unit is based on a fixed generation polynomial to obtain arbitrary CRC calculation results. In many applications, CRC-based techniques are used to verify data transfer or storage consistency. Within the scope of the EN/IEC 60335-1 standard, it provides a means of detecting flash memory errors. The CRC unit can be used to calculate signatures of software in real time and compare them with signatures generated when during the link-time and generating of the software.

The CRC has the following features:

- CRC16: supports polynomials $X^{16} + X^{15} + X^2 + X^0$
- CRC32: supports polynomials $X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$
- CRC16 calculation time: 1 AHB clock cycles (HCLK)
- CRC32 calculation time: 1 AHB clock cycles (HCLK)
- The initial value for cyclic redundancy computing is configurable
- Support DMA mode

2.28 Cryptographic Engine (CRYE)

The device features an embedded algorithm hardware acceleration engine, it supports a variety of international algorithms hash cryptographic algorithm acceleration, which can greatly improve the encryption and decryption speed compared with pure software algorithms.

The hardware supports the following algorithms :

- Supports DES symmetric algorithm
 - DES and 3DES encryption and decryption operations are supported
 - TDES supports 2KEY and 3KEY modes.
 - Support CBC and ECB modes
- Supports the SYMMETRIC AES algorithm

- 128bit/192bit/ 256bit key length is supported
- Supports CBC, ECB and CTR modes
- Supports SHA hash algorithm
 - Supports SHA1/SHA224/SHA256
- Support MD5 summarization algorithm
- Support symmetric SM1, SM4, SM7 algorithm and SM3 hash algorithm.

2.29 Unique Device Serial Number (UID)

The N32A455xxL7 series products have two built-in unique device serial numbers of different lengths, which are 96-bit Unique Device ID (UID) and 128-bit Unique Customer ID (UCID). These two device serial numbers are stored in the system configuration block of Flash memory. The information they contain is written at the time of delivery and is guaranteed to be unique to any of the N32A455xxL7 series microcontrollers under any circumstances and can be read by user applications or external devices through the CPU or JTAG/SWD interface and cannot be modified.

The 96-bit UID is usually used as a serial number or password. When writing Flash memory, this unique identifier is combined with software encryption and decryption algorithm to further improve the security of code in Flash memory.

The UCID is 128-bit, which complies with the definition of Nsing Technologies chip serial number. It contains the information related to chip production and version.

2.30 Serial Single-Wire JTAG Debug Port (SWJ-DP)

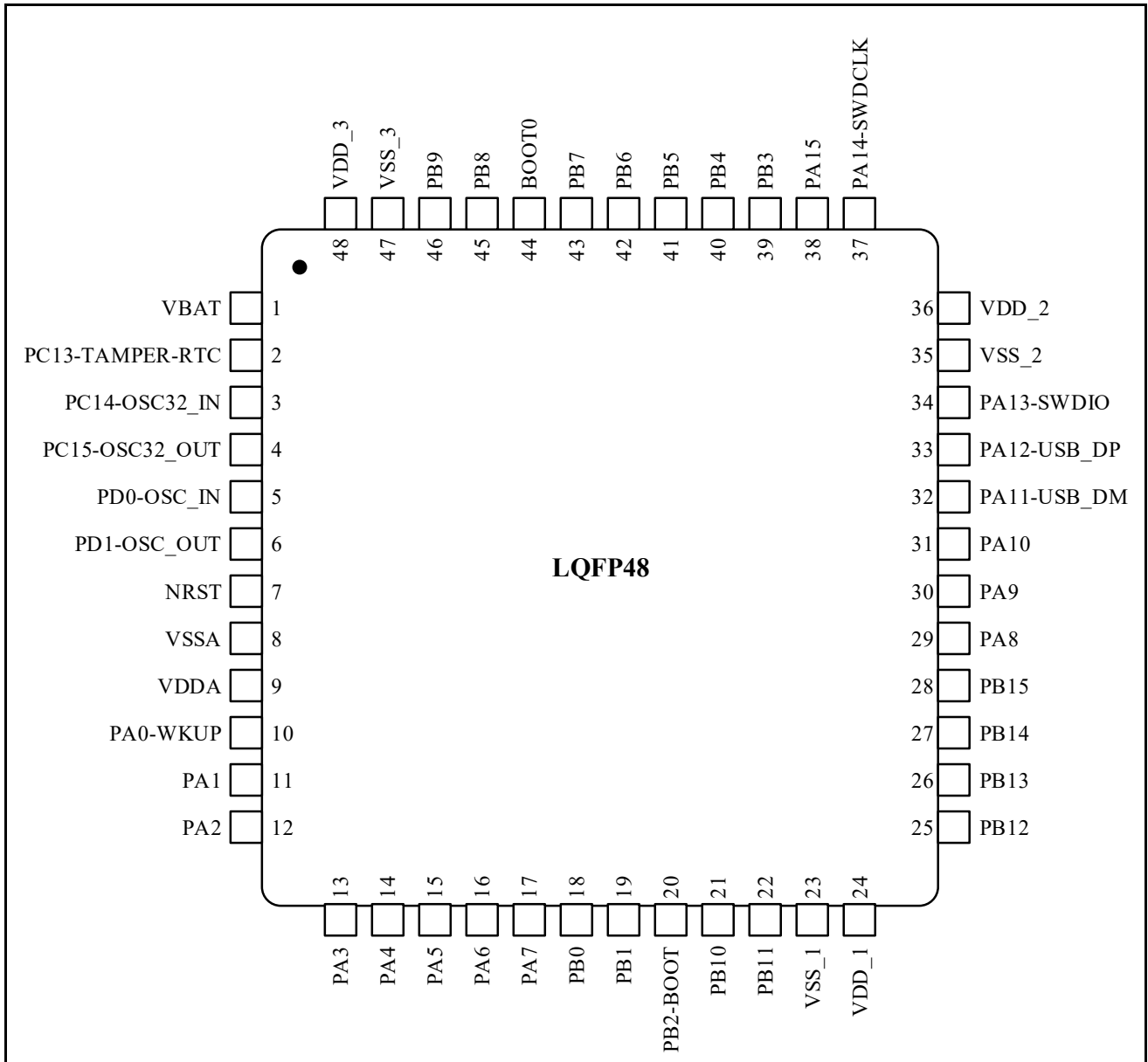
The device has an embedded ARM SWJ-DP interface, which is a combination of JTAG and serial single-line debugging interface, can achieve serial single-line debugging interface or JTAG interface connection. The JTMS and JTCK signals of JTAG share pins with SWDIO and SWCLK respectively, and a special signal sequence on the JTMS pin is used to switch between JTAG-DP and SW-DP.

3. Pinouts and Pin Description

3.1 Pinouts

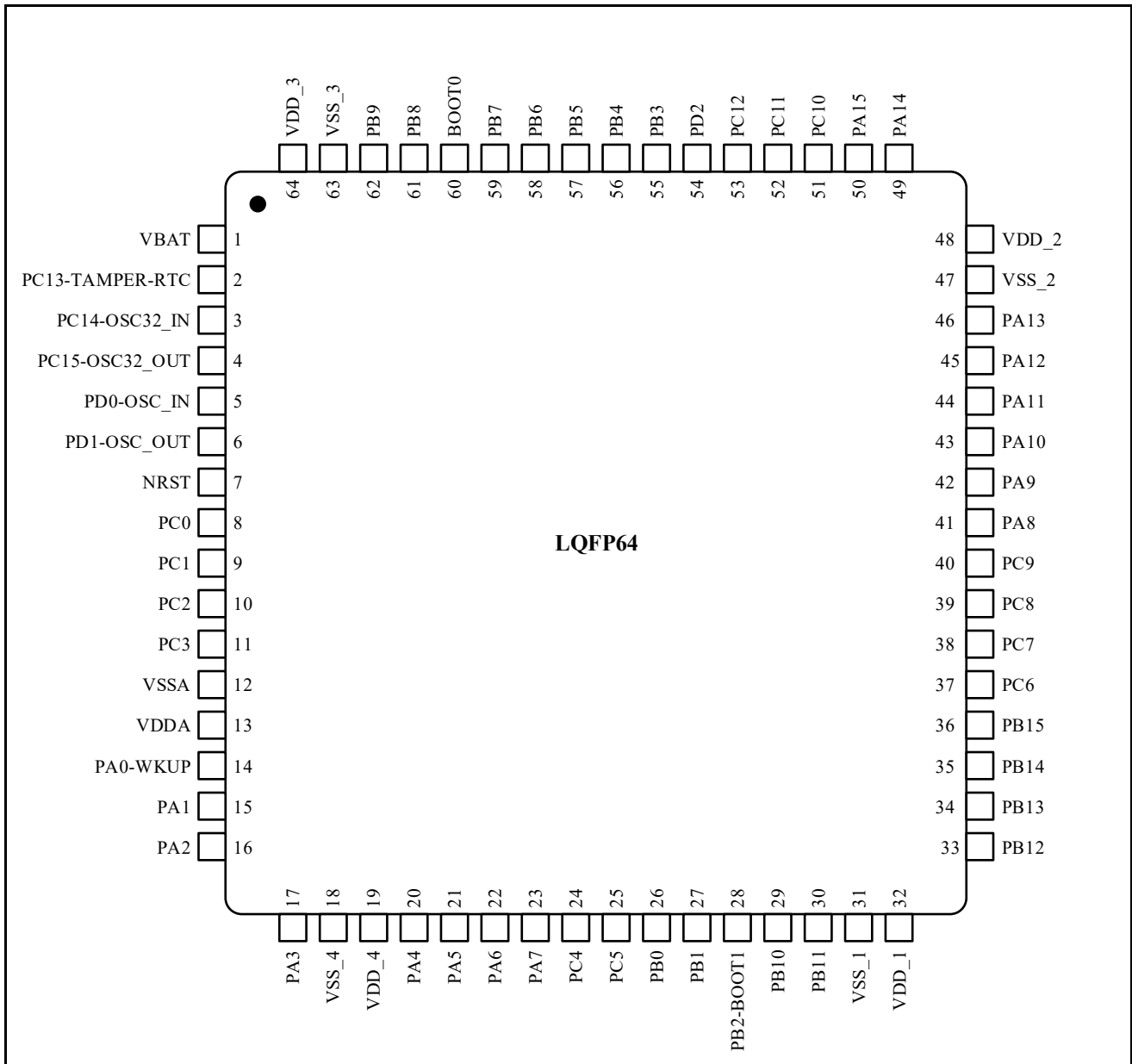
3.1.1 LQFP48

Figure 3-1 N32A455xxL7 Series LQFP48 Pinout



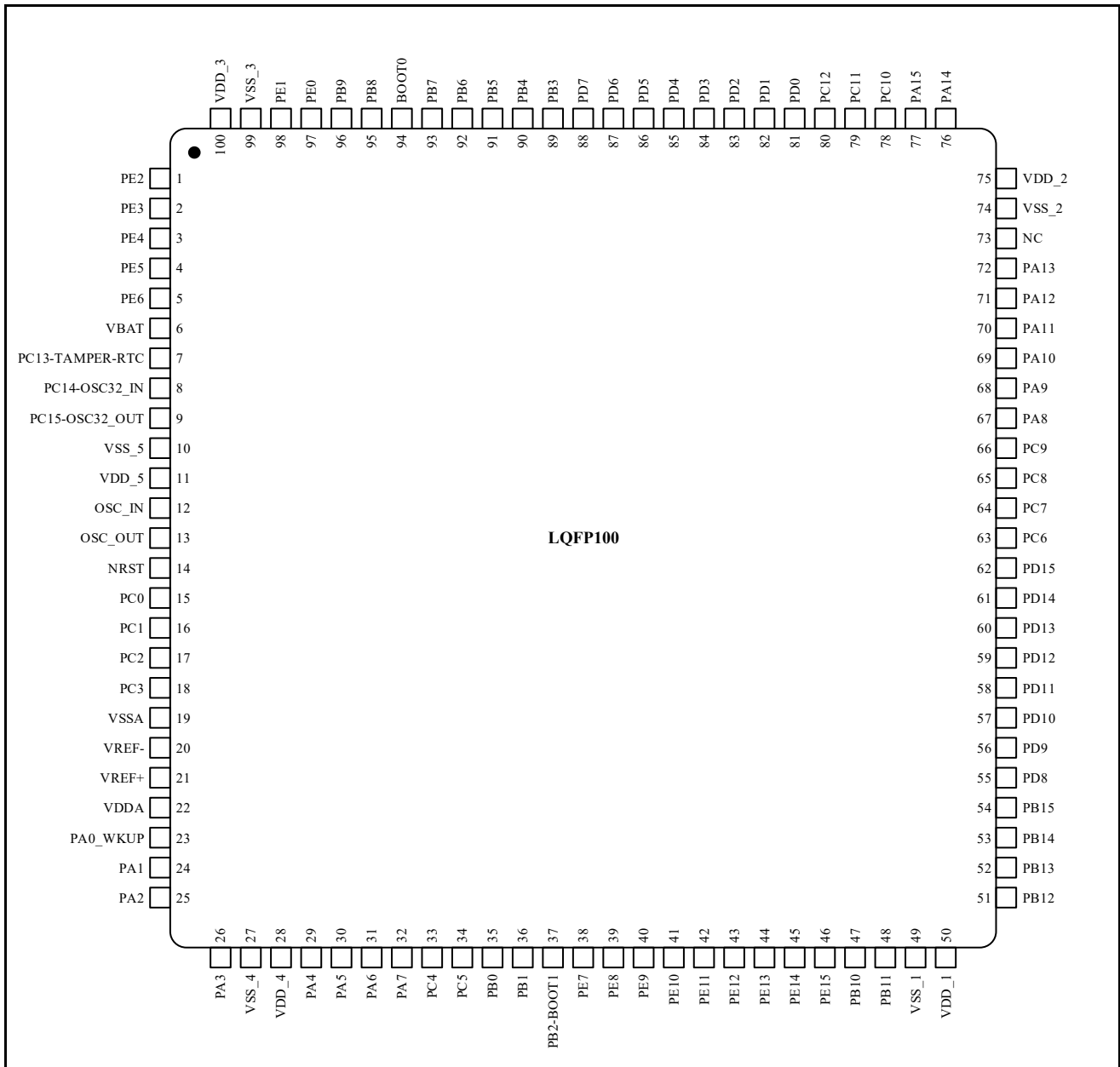
3.1.2 LQFP64

Figure 3-2 N32A455xxL7 Series LQFP64 Pinout



3.1.3 LQFP100

Figure 3-3 N32A455xxL7 Series LQFP100 Pinout



3.2 Pin Description

Table 3-1 Pin Description

Package			Pin name	Type ⁽¹⁾	I/O structure ⁽²⁾	Fail-safe support ⁽⁸⁾	Main Functions ⁽³⁾ (After Reset)	Optional Multiplexing Function ⁽⁶⁾	
LQFP48	LQFP64	LQFP100						Default	Redefine
-	-	1	PE2	I/O	FT	Yes	PE2	UART6_TX	-
-	-	2	PE3	I/O	FT	Yes	PE3	UART6_RX	-
-	-	3	PE4	I/O	FT	Yes	PE4	-	-
-	-	4	PE5	I/O	FT	Yes	PE5	-	-
-	-	5	PE6	I/O	FT	Yes	PE6	-	-
1	1	6	VBAT	S	-	-	VBAT	-	-
2	2	7	PC13-TAMPER- RTC ⁽⁴⁾	I/O	TC	Yes	PC13 ⁽⁵⁾	TAMPER-RTC	-
3	3	8	PC14- OSC32_IN ⁽⁴⁾	I/O	TC	Yes	PC14 ⁽⁵⁾	OSC32_IN	-
4	4	9	PC15- OSC32_OUT ⁽⁴⁾	I/O	TC	Yes	PC15 ⁽⁵⁾	OSC32_OUT	-
-	-	10	VSS_5	S	-	-	VSS_5	-	-
-	-	11	VDD_5	S	-	-	VDD_5	-	-
5	5	12	OSC_IN ⁽⁷⁾	I	TC	Yes	OSC_IN	-	-
6	6	13	OSC_OUT ⁽⁷⁾	O	TC	No	OSC_OUT	-	-
7	7	14	NRST	I/O	-	-	NRST	-	-
-	8	15	PC0	I/OTTa		No	PC0	ADC12_IN6 ⁽¹⁰⁾ I2C3_SCL	COMP7_INM UART6_TX
-	9	16	PC1	I/OTTa		No	PC1	ADC12_IN7 ⁽¹⁰⁾ I2C3_SDA	COMP7_INP UART6_RX
-	10	17	PC2	I/OTTa		No	PC2	ADC12_IN8 ⁽¹⁰⁾ COMP7_OUT	UART7_TX SPI3_NSS I2S3_WS
-	11	18	PC3	I/OTTa		No	PC3	ADC12_IN9 ⁽¹⁰⁾	UART7_RX SPI3_SCK I2S3_CK OPAMP3_VINP OPAMP4_VINP COMP5_INP
8	12	19	VSSA	S	-	-	VSSA	-	-
		20	VREF-	S	-	-	VREF-	-	-
9	13	21	VREF+	S	-	-	VREF+	-	-
		22	VDDA	S	-	-	VDDA	-	-
10	14	23	PA0-WKUP	I/OTTa		No	PA0	WKUP USART2_CTS ADC1_IN1 ⁽⁹⁾ TIM2_CH1_ETR TIM5_CH1 TIM8_ETR COMP1_OUT	COMP1_INM SPI3_MISO

Package			Pin name	Type ⁽¹⁾	I / O structure ⁽²⁾	Fail-safe support ⁽⁸⁾	Main Functions ⁽³⁾ (After Reset)	Optional Multiplexing Function ⁽⁶⁾	
LQFP48	LQFP64	LQFP100						Default	Redefine
11	15	24	PA1	I/OTTa		No	PA1	USART2_RTS ADC1_IN2 ⁽⁹⁾ TIM5_CH2 TIM2_CH2	COMP1_INP OPAMP1_VINP OPAMP3_VINP SPI3_MOSI I2S3_SD
12	16	25	PA2	I/OTTa		No	PA2	USART2_TX TIM5_CH3 ADC12_IN11 ⁽¹⁰⁾ TIM2_CH3 COMP2_OUT	OPAMP1_VINM OPAMP2_VINM
13	17	26	PA3	I/OTTa		No	PA3	USART2_RX TIM5_CH4 ADC1_IN4 ⁽⁹⁾ TIM2_CH4	OPAMP1_VINM OPAMP1_VINP COMP5_INP
-	18	27	VSS_4	S	-	-	VSS_4	-	-
-	19	28	VDD_4	S	-	-	VDD_4	-	-
14	20	29	PA4	I/OTTa		No	PA4	SPI1_NSS USART2_CK DAC_OUT1 ADC2_IN1 ⁽⁹⁾ QSPI_NSS	COMP1_INM COMP2_INM COMP3_INM COMP4_INM COMP5_INM COMP6_INM COMP7_INM OPAMP4_VINP I2C2_SCL
15	21	30	PA5	I/OTTa		No	PA5	SPI1_SCK DAC_OUT2 ADC2_IN2 ⁽⁹⁾ QSPI_SCK	COMP1_INM COMP2_INM COMP3_INM COMP4_INM COMP5_INM COMP6_INM COMP7_INM OPAMP1_VINP OPAMP2_VINM OPAMP3_VINP I2C2_SDA
16	22	31	PA6	I/OTTa		No	PA6	SPI1_MISO TIM8_BKIN ADC1_IN3 ⁽⁹⁾ TIM3_CH1 COMP1_OUT QSPI_IO0	TIM1_BKIN OPAMP1_VOUT COMP2_OUT
17	23	32	PA7	I/OTTa		No	PA7	SPI1_MOSI TIM8_CH1N ADC2_IN4 ⁽⁹⁾ TIM3_CH2 QSPI_IO1 COMP2_OUT	TIM1_CH1N COMP2_INP OPAMP1_VINP OPAMP2_VINP COMP6_INM
-	24	33	PC4	I/OTTa		No	PC4	ADC2_IN5 ⁽⁹⁾ QSPI_IO2 UART7_TX	I2C3_SCL OPAMP3_VINM COMP4_INM COMP5_INP
-	25	34	PC5	I/OTTa		No	PC5	ADC2_IN12 ⁽¹⁰⁾ QSPI_IO3 UART7_RX	I2C3_SDA OPAMP4_VINP COMP4_OUT COMP6_INP

Package			Pin name	Type ⁽¹⁾	I / O structure ⁽²⁾	Fail-safe support ⁽⁸⁾	Main Functions ⁽³⁾ (After Reset)	Optional Multiplexing Function ⁽⁶⁾	
LQFP48	LQFP64	LQFP100						Default	Redefine
18	26	35	PB0	I/OTTa		No	PB0	ADC3_IN12 ⁽¹⁰⁾ TIM3_CH3 TIM8_CH2N	TIM1_CH2N UART6_TX OPAMP2_VINP COMP3_INP COMP5_OUT
19	27	36	PB1	I/OTTa		No	PB1	ADC2_IN3 ⁽⁹⁾ TIM3_CH4 TIM8_CH3N COMP4_OUT	TIM1_CH3N OPAMP2_VOUT UART6_RX COMP2_INM COMP1_OUT
20	28	37	PB2	I/OTTa		No	PB2/BOOT1	ADC2_IN13 ⁽¹⁰⁾	UART4_TX SPI1_NSS
-	-	38	PE7	I/OTTa		No	PE7	ADC3_IN13 ⁽¹⁰⁾	TIM1_ETR UART4_RX SPI1_SCK COMP3_INM
-	-	39	PE8	I/OTTa		No	PE8	ADC34_IN6 ⁽¹⁰⁾	TIM1_CH1N UART5_TX SDIO_DAT0 SPI1_MISO OPAMP2_VINP COMP2_INM
-	-	40	PE9	I/OTTa		No	PE9	ADC3_IN2 ⁽⁹⁾	TIM1_CH1 UART5_RX SDIO_DAT1 SPI1_MOSI
-	-	41	PE10	I/OTTa		No	PE10	ADC3_IN14 ⁽¹⁰⁾	TIM1_CH2N SDIO_DAT2 SPI2_NSS I2S2_WS
-	-	42	PE11	I/OTTa		No	PE11	ADC3_IN15 ⁽¹⁰⁾	TIM1_CH2 SDIO_DAT3 SPI2_SCK I2S2_CK
-	-	43	PE12	I/OTTa		No	PE12	ADC3_IN4 ⁽⁹⁾	TIM1_CH3N SDIO_CLK SPI2_MISO
-	-	44	PE13	I/OTTa		No	PE13	ADC3_IN3 ⁽⁹⁾	TIM1_CH3 SPI2_MOSI I2S2_SD SDIO_CMD
-	-	45	PE14	I/OTTa		No	PE14	ADC4_IN1 ⁽⁹⁾	TIM1_CH4
-	-	46	PE15	I/OTTa		No	PE15	ADC4_IN2 ⁽⁹⁾	TIM1_BKIN
21	29	47	PB10	I/OTTa		Yes	PB10	I2C2_SCL USART3_TX	TIM2_CH3 COMP5_INM OPAMP3_VINM OPAMP4_VINM COMP1_INP COMP3_OUT
22	30	48	PB11	I/OTTa		No	PB11	I2C2_SDA USART3_RX ADC3_IN1 ⁽⁹⁾	TIM2_CH4 OPAMP3_VOUT COMP2_INP COMP5_OUT

Package			Pin name	Type ⁽¹⁾	I / O structure ⁽²⁾	Fail-safe support ⁽⁸⁾	Main Functions ⁽³⁾ (After Reset)	Optional Multiplexing Function ⁽⁶⁾	
LQFP48	LQFP64	LQFP100						Default	Redefine
23	31	49	VSS_1	S	-	-	VSS_1	-	-
24	32	50	VDD_1	S	-	-	VDD_1	-	-
25	33	51	PB12	I/O T T a		No	PB12	SPI2_NSS I2S2_WS I2C2_SMBA USART3_CK TIM1_BKIN CAN2_RX ADC4_IN3 ⁽⁹⁾	COMP3_INM OPAMP4_VOUT COMP4_OUT
26	34	52	PB13	I/O T T a		No	PB13	SPI2_SCK I2S2_CK USART3_CTS TIM1_CH1N CAN2_TX ADC3_IN5 ⁽⁹⁾	UART5_TX COMP4_INM
27	35	53	PB14	I/O T T a		No	PB14	SPI2_MISO TIM1_CH2N USART3_RTS ADC4_IN4 ⁽⁹⁾	COMP3_INP UART5_RX
28	36	54	PB15	I/O T T a		No	PB15	SPI2_MOSI I2S2_SD TIM1_CH3N ADC4_IN5 ⁽⁹⁾	COMP4_INP
-	-	55	PD8	I/O T T a		No	PD8	ADC4_IN12 ⁽¹⁰⁾	USART3_TX OPAMP4_VINM SPI3_NSS I2S3_WS CAN1_RX COMP6_INM
-	-	56	PD9	I/O T T a		No	PD9	ADC4_IN13 ⁽¹⁰⁾	USART3_RX SPI3_SCK I2S3_CK CAN1_TX COMP6_INP
-	-	57	PD10	I/O T T a		No	PD10	ADC34_IN7 ⁽¹⁰⁾	USART3_CK CAN2_RX COMP5_INM
-	-	58	PD11	I/O T T a		No	PD11	ADC34_IN8 ⁽¹⁰⁾	USART3_CTS CAN2_TX SPI3_MISO
-	-	59	PD12	I/O T T a		No	PD12	ADC34_IN9 ⁽¹⁰⁾	TIM4_CH1 USART3_RTS SPI3_MOSI I2S3_SD COMP7_OUT
-	-	60	PD13	I/O T T a		No	PD13	ADC34_IN10 ⁽¹⁰⁾	TIM4_CH2
-	-	61	PD14	I/O T T a		No	PD14	ADC34_IN11 ⁽¹⁰⁾	TIM4_CH3 I2C4_SCL TIM8_CH1
-	-	62	PD15	I/O FT		Yes	PD15	-	TIM4_CH4 I2C4_SDA TIM8_CH2
-	37	63	PC6	I/O TC		Yes	PC6	I2S2_MCK TIM8_CH1 SDIO_DAT6	TIM3_CH1 SPI2_NSS I2S2_WS

Package			Pin name	Type (1)	I / O structure (2)	Fail-safe support (8)	Main Functions (3) (After Reset)	Optional Multiplexing Function (6)			
LQFP48	LQFP64	LQFP100						Default	Redefine		
								I2C4_SCL	USART2_CTS		
-	38	64	PC7	I/O	TC	Yes	PC7	I2S3_MCK TIM8_CH2 SDIO_DAT7 I2C4_SDA	TIM3_CH2 SPI2_SCK I2S2_CK USART2_RTS		
-	39	65	PC8	I/O	TC	Yes	PC8	TIM8_CH3 SDIO_DAT0	TIM3_CH3 SPI2_MISO USART2_TX		
-	40	66	PC9	I/O	Ta	Yes	PC9	TIM8_CH4 SDIO_DAT1	TIM3_CH4 SPI2_MOSI I2S2_SD USART2_RX COMP6_OUT OPAMP3_VINP OPAMP4_VINM COMP4_INP		
29	41	67	PA8	I/O	FT	Yes	PA8	USART1_CK TIM1_CH1 MCO	-		
30	42	68	PA9	I/O	FT	Yes	PA9	USART1_TX TIM1_CH2	I2C4_SCL		
31	43	69	PA10	I/O	FT	Yes	PA10	USART1_RX TIM1_CH3	I2C4_SDA		
32	44	70	PA11	I/O	FT	Yes	PA11	USART1_CTS USBDM CAN1_RX TIM1_CH4 COMP1_OUT	COMP5_OUT		
33	45	71	PA12	I/O	FT	Yes	PA12	USART1_RTS USBDP CAN1_TX TIM1_ETR COMP2_OUT	COMP6_OUT		
34	46	72	PA13	I/O	FT	Yes	JTMS- SWDIO	-	PA13 UART4_TX		
-	-	73	Not Connect								
35	47	74	VSS_2	S	-	-	VSS_2	-	-		
36	48	75	VDD_2	S	-	-	VDD_2	-	-		
37	49	76	PA14	I/O	FT	Yes	JTCK- SWCLK	-	PA14 UART4_RX		
38	50	77	PA15	I/O	FT	Yes	JTDI	SPI3_NSS I2S3_WS	TIM2_CH1_ETR PA15 SPI1_NSS USART2_CTS TIM8_CH1N		

Package			Pin name	Type ⁽¹⁾		Fail-safe support ⁽⁸⁾	Main Functions ⁽³⁾ (After Reset)	Optional Multiplexing Function ⁽⁶⁾	
LQFP48	LQFP64	LQFP100		I/O	Structure ⁽²⁾			Default	Redefine
-	51	78	PC10	I/O	Ta	Yes	PC10	UART4_TX SDIO_DAT2	USART3_TX SPI3_SCK I2S3_CK QSPI_NSS COMP3_OUT
-	52	79	PC11	I/O	Ta	Yes	PC11	UART4_RX SDIO_DAT3	USART3_RX SPI3_MISO QSPI_SCK COMP4_OUT
-	53	80	PC12	I/O	TC	Yes	PC12	UART5_TX SDIO_CLK	USART3_CK SPI3_MOSI I2S3_SD QSPI_IO0 TIM8_CH2N
-	-	81	PD0	I/O	FT	Yes	PD0 ⁽⁷⁾	-	CAN1_RX UART4_TX QSPI_IO1
-	-	82	PD1	I/O	FT	Yes	PD1 ⁽⁷⁾	-	CAN1_TX UART4_RX QSPI_IO2
-	54	83	PD2	I/O	TC	Yes	PD2	TIM3_ETR UART5_RX SDIO_CMD	SPI3_NSS I2S3_WS QSPI_IO3 TIM8_CH3N
-	-	84	PD3	I/O	FT	Yes	PD3	-	USART2_CTS
-	-	85	PD4	I/O	TC	Yes	PD4	-	USART2_RTS
-	-	86	PD5	I/O	TC	Yes	PD5	-	USART2_TX
-	-	87	PD6	I/O	TC	Yes	PD6	-	USART2_RX
-	-	88	PD7	I/O	TC	Yes	PD7	-	USART2_CK
39	55	89	PB3	I/O	FT	Yes	JTDO	SPI3_SCK I2S3_CK	PB3 TRACESWO TIM2_CH2 SPI1_SCK USART2_RTS TIM8_BKIN
40	56	90	PB4	I/O	FT	Yes	NJTRST	SPI3_MISO	PB4 TIM3_CH1 SPI1_MISO USART2_TX TIM8_ETR
41	57	91	PB5	I/O	FT	Yes	PB5	I2C1_SMBA SPI3_MOSI I2S3_SD	TIM3_CH2 SPI1_MOSI CAN2_RX USART2_RX TIM1_BKIN
42	58	92	PB6	I/O	Ta	Yes	PB6	I2C1_SCL TIM4_CH1	USART1_TX CAN2_TX COMP5_OUT

Package			Pin name	Type ⁽¹⁾		Fail-safe support ⁽⁸⁾	Main Functions ⁽³⁾ (After Reset)	Optional Multiplexing Function ⁽⁶⁾	
LQFP48	LQFP64	LQFP100		I/O	structure ⁽²⁾			Default	Redefine
43	59	93	PB7	I/O	TTa	Yes	PB7	I2C1_SDA TIM4_CH2	USART1_RX COMP6_OUT
44	60	94	BOOT0	I	-	-	BOOT0	-	-
45	61	95	PB8	I/O	TTa	Yes	PB8	TIM4_CH3 SDIO_DAT4 COMP1_OUT	I2C1_SCL CAN1_RX UART5_TX
46	62	96	PB9	I/O	TTa	Yes	PB9	TIM4_CH4 SDIO_DAT5 COMP2_OUT	I2C1_SDA CAN1_TX UART5_RX
-	-	97	PE0	I/O	FT	Yes	PE0	TIM4_ETR	-
-	-	98	PE1	I/O	FT	Yes	PE1	-	-
47	63	99	VSS_3	S	-	-	VSS_3	-	-
48	64	100	VDD_3	S	-	-	VDD_3	-	-

1. *I = input, O = output, S = power supply, HiZ = high impedance.*
2. *FT: tolerate 5V; TTa: tolerates 3.3V and supports analog peripherals; TC: ordinary 3.3V I/O*
3. *Some functions are only supported in some models of chips.*
 - *Pin PC13, PC14 and PC15 are powered by the power switch, which can only absorb limited current (3mA). Therefore, when these three pins are used as output pins, they have the following limitations: when they are used as output pins, they can only work in 2MHz mode, the maximum driving load is 30pF, and the total output current for all three pins combined cannot exceed 3mA.*
 - *When the backup area is powered on for the first time, these pins are in the main function state. After that, even if they are reset, the state of these pins is controlled by the backup area registers (these registers will not be reset by the main reset system). For specific information on how to control these IO ports, please refer to the battery backup area of N32A455 user's reference manual and relevant chapters of BKP register.*
 - *Some multiplexing functions can be configured to other pins by software (if the corresponding package model has this pin). For details, please refer to the multiplexing function I/O chapter and debugging setting chapter of N32A455 user reference manual.*
 - *Pin 5 and pin 6 of LQFP48/64 package are configured as OSC_IN and OSC_OUT function pins by default after the chip is reset. Software can reset these two pins to PD0 and PD1 functions. When used as PD0 and PD1, these two pins can only be used as ordinary IO functions. However, for LQFP100 package, because PD0 and PD1 are inherent functional pins, there is no need to remap by software. For more details, please refer to the reuse function I/O chapter and debugging settings chapter of N32A455 user reference manual.*
 - *Fail-safe means that when the chip has no power input, the input high level is added to IO, and there is no phenomenon that the input high level is poured into the chip, which leads to a certain voltage on the power supply and consumes current.*
 - *Corresponding ADC channels are fast channels, support the highest sampling rate 5.14MSPS (12 bit)*
 - *Corresponding ADC channels are slow channels, support the highest sampling rate 4.23MSPS (12 bit)*

Note: ADC12_INx appears in the pin name label in the Table, indicating that this pin can be ADC1_INx or

ADC2_INx. For example, ADC12_IN9 indicates that this pin can be configured as ADC1_IN9 or ADC2_IN9. Similarly, ADC34_INx appears in the pin name annotation in the Table, indicating that this pin can be ADC3_INx or ADC4_INx.

TIM2_CH1_ETR in the multiplexing function corresponding to pin PA0 in the Table indicates that the function can be configured as TIM2_T11 or TIM2_ETR. Similarly, the name of the remapping multiplexing function corresponding to PA15, TIM2_CH1_ETR, has the same meaning.

For the port of FT in the Table, it is necessary to ensure that the difference between IO voltage and power supply voltage is less than 3.6V

4. Electrical Characteristics

4.1 Parameter Conditions

All voltages are based on VSS unless otherwise specified.

4.1.1 Minimum and Maximum Values

Unless otherwise specified, all product are tests at ambient temperatures $T_A=25^{\circ}\text{C}$.where minimums and maximums values apply to the worst ambient temperature, supply voltage and clock frequency specified in the datasheet.

Note at the bottom of each form that data obtained through comprehensive evaluation, design simulation and/or process characteristics will not be tested on the production; Base on comprehensive evaluation, the minimum and maximum values are obtained by taking the average of the samples tested and adding or subtracting three times the standard distribution (mean $\pm 3\sigma$).

4.1.2 Typical Values

Unless otherwise specified, typical data are based on $T_A= 25\text{ C}$ and $V_{DD}=3.3\text{V}$. These data is untested and used only as a design guide for the user.

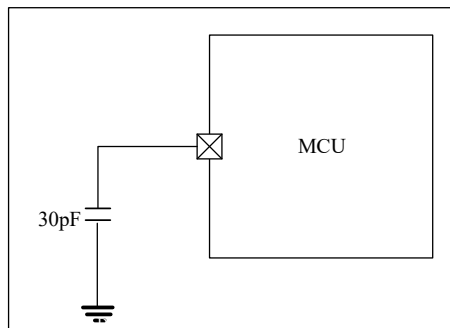
4.1.3 Typical Curves

Unless otherwise specified, these typical curves are untested and used only as a design guide for the user.

4.1.4 Loading Capacitors

The load conditions for measuring pin parameters are shown in Figure 4-1.

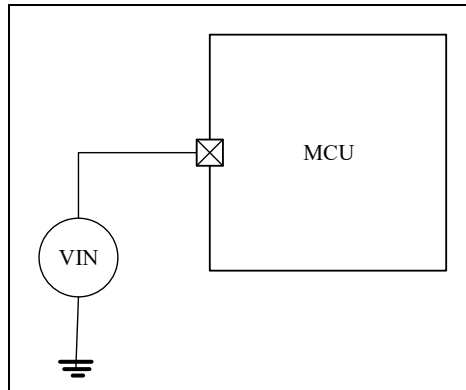
Figure 4-1 Load Conditions of Pins



4.1.5 Pin Input Voltage

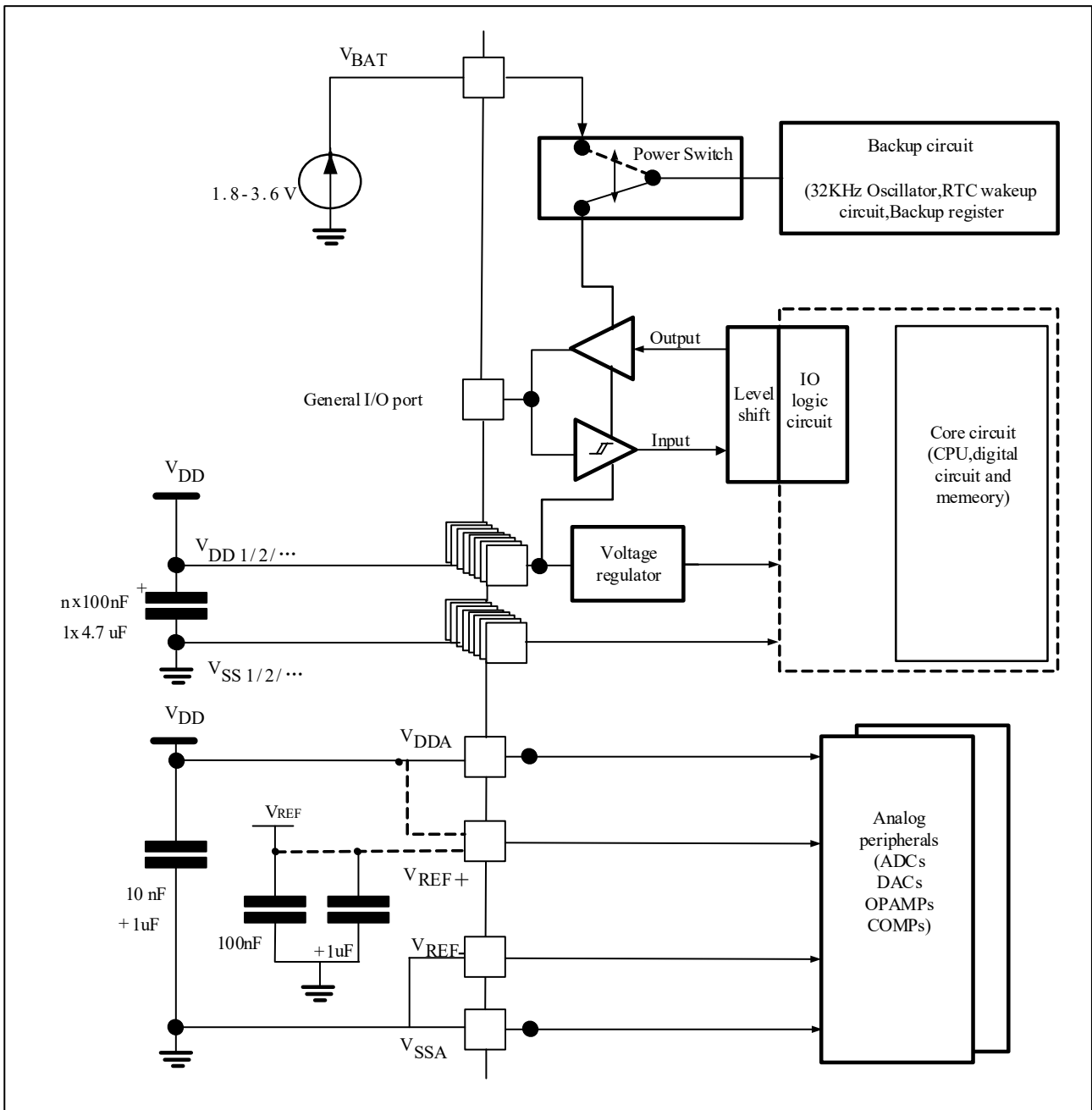
The measurement of the input voltage on pin is shown in Figure 4-2.

Figure 4-2 Pin Input Voltage



4.1.6 Power Supply Scheme

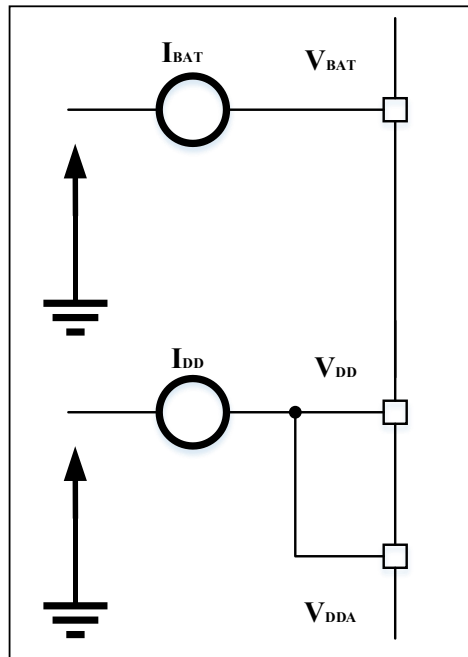
Figure 4-3 Power Supply Scheme



Note:⁽¹⁾ The $4.7\ \mu\text{F}$ capacitor in the above figure must be connected to V_{DD3} .

4.1.6 Current Consumption Measurement

Figure 4-4 Current Consumption Measurement Scheme



4.2 Absolute Maximum Rating

The load applied to the device may permanently damage the device if it exceeds the values given in the Absolute maximum rating list (Table 4-1、 Table 4-2). The maximum load that can be sustained is only given here, and it does not mean that the functional operation of the device under such conditions is correct. The reliability of the device will be affected when the device works for a long time under the maximum condition.

Table 4-1 Voltage Characteristic

Symbol	Describe	Min	Max	Unit
$V_{DD} - V_{SS}$	Main power supply voltage (including V_{DDA} and V_{DD}) ⁽¹⁾	-0.3	4.0	V
V_{IN}	Input voltage on 5V tolerant pin ⁽³⁾	$V_{SS} - 0.3$	5.5	
	Input voltage on other pins ⁽²⁾	$V_{SS} - 0.3$	$V_{DD} + 0.3$	
$ \Delta V_{DDx} $	Voltage difference between different supply pins	-	50	mV
$ V_{SSx} - V_{SS} $	Voltage difference between different grounding pins	-	50	
$V_{ESD(HBM)}$	Electrostatic discharge voltage (Human body mode)	See section 4.3.11		

Note:

- ⁽¹⁾ All power (V_{DD} , V_{DDA}) and ground (V_{SS} , V_{SSA}) pins must always be connected to the external power supply system within permissible limits.
- ⁽²⁾ V_{IN} shall not exceed its maximum value. Refer to Table 4-2 for current characteristics.
- ⁽³⁾ When 5.5V is applied to the 5V tolerant pin, V_{DD} cannot be less than 2.25V.

Table 4-2 Current Characteristic

Symbol	Describe	Max ⁽¹⁾	Unit
I_{VDD}	Total current (supply current) through V_{DD}/V_{DDA} power line ⁽¹⁾⁽⁴⁾	100	mA
I_{VSS}	Total current (outflow current) through V_{SS} ground wire	100	
I_I	Output sink current on any I/O and control pins	12	
	Output current on any I/O and control pins	-12	
$I_{IN(PIN)}^{(2)(3)}$	Injection current of NRST pin	-5/0	
	Injection current of other pins ⁽⁴⁾	+/-5	

Note:

⁽¹⁾All the power supply (V_{DD} , V_{DDA}) and ground (V_{SS} , V_{SSA}) pins of must always be connected to the power supply system within the external allowable range.

⁽²⁾When $V_{IN} > V_{DD}$, there is a forward injection current; when $V_{IN} < V_{SS}$, there is a reverse injection current. $I_{INJ(PIN)}$ should not exceed its maximum value. Voltage characteristics refer to Table 4-1.

⁽³⁾Reverse injection current can interfere with the analog performance of the device. See section 0.

⁽⁴⁾When the maximum current occurs, the maximum allowable voltage drop of V_{DD} is $0.1V_{DD}$.

4.3 Operating Conditions

4.3.1 General Operating Conditions

Table 4-3 General Operating Conditions

Symbol	Parameter	Condition	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency	-	0	144	MHz
f_{PCLK1}	Internal APB1 clock frequency	-	0	36	
f_{PCLK2}	Internal APB2 clock frequency	-	0	72	
V_{DD}	Standard working voltage	-	1.8	3.6	V
V_{DDA}	Analog working voltage	Must be the same as $V_{DD}^{(1)}$	1.8	3.6	V
V_{BAT}	Backup partial working voltage	-	1.8	3.6	V
T_A	Ambient temperature	Maximum power consumption	-40	105	°C
T_J	Junction temperature range	-	-40	125	°C

Note⁽¹⁾It is recommended that the same power supply be used to power the V_{DD} and V_{DDA} . During power-on and normal operation, a maximum of 300mV difference is allowed between the V_{DD} and V_{DDA} .

4.3.2 Operating Conditions at Power-on and Power-off

Table 4-4 Operating Conditions at Power-on and Power-off

Symbol	Parameter	Condition	Min	Max	Unit
t_{VDD}	V_{DD} rising rate	Supply voltage goes from 0 to V_{DD}	20	-	$\mu\text{s/V}$
	V_{DD} falling rate	Supply voltage drops from V_{DD} to 0	80	-	

4.3.3 Embedded Reset and Power Control Module Features

Table 4-5 Features of Embedded Reset and Power Control Modules

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V _{PVD}	Level selection of programmable voltage detector (MSB of PWR_CTRL is 0)	PRS[2:0]=000 (rising edge)	2.09	2.18	2.27	V
		PRS[2:0]=000 (falling edge)	2	2.08	2.16	V
		PRS[2:0]=001 (rising edge)	2.19	2.28	2.37	V
		PRS[2:0]=001 (falling edge)	2.09	2.18	2.27	V
		PRS[2:0]=010 (rising edge)	2.28	2.38	2.48	V
		PRS[2:0]=010 (falling edge)	2.19	2.28	2.37	V
		PRS[2:0]=011 (rising edge)	2.38	2.48	2.58	V
		PRS[2:0]=011 (falling edge)	2.28	2.38	2.48	V
		PRS[2:0]=100 (rising edge)	2.47	2.58	2.69	V
		PRS[2:0]=100 (falling edge)	2.37	2.48	2.59	V
		PRS[2:0]=101 (rising edge)	2.57	2.68	2.79	V
		PRS[2:0]=101 (falling edge)	2.47	2.58	2.69	V
		PRS[2:0]=110 (rising edge)	2.66	2.78	2.9	V
		PRS[2:0]=110 (falling edge)	2.56	2.68	2.8	V
	PRS[2:0]=111 (rising edge)	2.76	2.88	3	V	
	PRS[2:0]=111 (falling edge)	2.66	2.78	2.9	V	
	Level selection of programmable voltage detector (MSB of PWR_CTRL is 1)	PRS[2:0]=000 (rising edge)	1.7	1.78	1.85	V
		PRS[2:0]=000 (falling edge)	1.61	1.68	1.75	V
		PRS[2:0]=001 (rising edge)	1.8	1.88	1.96	V
		PRS[2:0]=001 (falling edge)	1.7	1.78	1.85	V
		PRS[2:0]=010 (rising edge)	1.9	1.98	2.06	V
		PRS[2:0]=010 (falling edge)	1.8	1.88	1.96	V
		PRS[2:0]=011 (rising edge)	2	2.08	2.16	V
		PRS[2:0]=011 (falling edge)	1.9	1.98	2.06	V
		PRS[2:0]=100 (rising edge)	3.15	3.28	3.41	V
		PRS[2:0]=100 (falling edge)	3.05	3.18	3.31	V
PRS[2:0]=101 (rising edge)		3.24	3.38	3.52	V	
PRS[2:0]=101 (falling edge)		3.15	3.28	3.41	V	
PRS[2:0]=110 (rising edge)	3.34	3.48	3.62	V		
PRS[2:0]=110 (falling edge)	3.24	3.38	3.52	V		
PRS[2:0]=111 (rising edge)	3.44	3.58	3.72	V		
PRS[2:0]=111 (falling edge)	3.34	3.48	3.62	V		
V _{PVD hyst} ⁽¹⁾	PVD hysteresis	-	-	100	-	mV
V _{POR}	VDD power-on/power-off reset threshold	-	-	1.64/1.62	-	V
T _{RSTTEMPO} ⁽¹⁾	Reset duration	-	-	0.8	4	ms

Note: ⁽¹⁾ Guaranteed by design, not tested in production.

4.3.4 Internal Reference Voltage

The parameters given in the following table are based on the ambient temperature and VDD supply voltage listed in Table 4-3.

Table 4-6 Embedded Reference Voltage

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{REFINT}	Built-in reference voltage	-40°C < T _A < +85°C	1.16	1.20	1.24	V
		-40°C < T _A < +105°C	1.16	1.20	1.26	V
T _{S_vrefint} ⁽¹⁾	Sampling time of ADC when reading out internal reference voltage	-	-	5.1	17.1 ⁽²⁾	μs

Note:

⁽¹⁾ The shortest sampling time is obtained through multiple cycles in the application.

⁽²⁾ Guaranteed by design, not tested in production.

4.3.5 Power Supply Current Characteristics

Current consumption is a combination of several parameters and factors, including operating voltage, ambient temperature, load of I/O pins, software configuration of the product, operating frequency, I/O pin switching rate, program location in memory, and code executed.

The measurement method of current consumption is described in Figure 4-4.

All of the current consumption measurements given in this section are while executing a reduced set of code.

4.3.2.1 Maximum current consumption

The device is under the following conditions:

- All I/O pins are in input mode and are connected to a static level -- VDD or VSS (no load).
- All peripherals are disabled except otherwise noted.
- The access time of the flash memory is adjusted to the fastest operating frequency (0 waiting periods from 0 to 32MHz, 1 waiting period from 32 to 64MHz, 2 waiting periods from 64MHz to 96MHz, 3 waiting periods from 96MHz to 128MHz, 4 waiting periods from 128MHz to 144MHz).
- Instruction prefetch is enabled (note: this parameter must be set before setting the clock and bus divider).
- When the peripheral is enable: f_{PCLK1} = f_{HCLK}/4, f_{PCLK2} = f_{HCLK}/2.

The parameters given in Table 4-7 and Table 4-8 are based on the test at ambient temperature and V_{DD} supply voltage listed in Table 4-3.

Table 4-7 Maximum Current Consumption in Operating Mode Running From Embedded Flash

Symbol	Parameter	Condition	f _{HCLK}	Typ ⁽¹⁾	Unit
				T _A = 105°C	
I _{DD}	Supply current in operation mode	External clock ⁽²⁾ , Enable all peripherals	144MHz	32	mA
			72MHz	18	
			36MHz	11	
		External clock ⁽²⁾ , Turn off all peripherals.	144MHz	15.8	
			72MHz	9.7	
			36MHz	7	

Note:

⁽¹⁾Based on comprehensive evaluation, not tested in production.

⁽²⁾PLL is enabled when f_{HCLK}>8MHz.

Table 4-8 Maximum Current Consumption In SLEEP Mode

Symbol	Parameter	Condition	f _{HCLK}	Typ ⁽¹⁾	Unit
				T _A = 105°C	
I _{DD}	Supply current in SLEEP mode	External clock ⁽²⁾ , Enable all peripherals	144MHz	27	mA
			72MHz	15.5	
			36MHz	10	
		External clock ⁽²⁾ , Turn off all peripherals.	144MHz	9.4	
			72MHz	6.8	
			36MHz	5.5	

Notes:

⁽¹⁾Based on comprehensive evaluation, not tested in production.

⁽²⁾PLL is enabled when $f_{HCLK} > 8\text{MHz}$.

4.3.2.2 Low power mode current consumption

MCU is under the following conditions:

- All I/O pins are in input mode and are connected to a static level -- VDD or VSS (no load).
- All peripherals are disabled unless otherwise noted.

Table 4-9 Typical and Maximum Current Consumption in Powerdown Mode and Standby Mode

Symbol	Parameter	Condition	Typ ⁽¹⁾		Unit
			T _A =25°C	T _A =105°C	
I _{DD}	Supply current in STOP0 mode	The voltage regulator is in operation mode, low-speed and high-speed internal RC oscillators and high-speed oscillators are off (Independent watchdog is off)	300	4500	μA
		The voltage regulator is in low power consumption mode, and the low-speed and high-speed internal RC oscillators and high-speed oscillators are off (Independent watchdog is off)	150	3500	
	Supply current in STOP2 mode	The external low-speed clock is turned on, RTC is running, R-SRAM is maintained, all I/O states are maintained, and the independent watchdog is off.	10	300	
	Supply current in STANDBY mode	Low-speed RC oscillator and independent watchdog are on.	4	200	
		The internal low-speed RC oscillator is on, and the independent watchdog is off.	3.9	185	
		The internal low-speed RC oscillator and independent watchdog are off, and the low-speed oscillator and RTC is off.	3.7	155	
I _{DD_VBAT}	Supply current of Backup Area (VBAT)	Low speed oscillator and RTC is on.	3	20	

Notes:

⁽¹⁾Typical values are measured at $V_{DD}/V_{BAT} = 3.3\text{V}$

⁽²⁾Based on comprehensive evaluation, not tested in production.

4.3.2.3 Typical current consumption

MCU is under the following conditions:

- All I/O pins are in input mode and are connected to a static level -- VDD or VSS (no load).
- All peripherals are disabled unless otherwise noted.
- The access time of the flash memory is adjusted to the fastest operating frequency (0 waiting periods from 0 to 32MHz, 1 waiting period from 32 to 64MHz, 2 waiting periods from 64MHz to 96MHz, 3 waiting periods from 96MHz to 128MHz, 4 waiting periods from 128MHz to 144MHz).
- Ambient temperature and V_{DD} supply voltage conditions are listed in Table 4-3.
- Instruction prefetch is enabled (note: this parameter must be set before setting the clock and bus divider). When the peripheral is turned on: $f_{PCLK1} = f_{HCLK}/4$, $f_{PCLK2} = f_{HCLK}/2$, $f_{ADCLK} = f_{PCLK2}/4$.

Table 4-10 Typical Current Consumption In Operating Mode Running From Embedded Flash

Symbol	Parameter	Condition	f _{HCLK}	Typ ⁽¹⁾		Unit
				Enable all peripherals ⁽²⁾	Disable all peripherals.	
I _{DD}	Supply current in operation mode	External clock ⁽³⁾	144MHz	30.3	14.2	mA
			72MHz	17	8.1	
			36MHz	9.3	5.3	
		Run in high-speed internal RC oscillator (HSI), use AHB prescaler to reduce frequency.	128MHz	30	12.7	mA
			72MHz	22.5	7.2	
			36MHz	8.8	3.9	

Notes:

⁽¹⁾Typical values are measured at T_A=25°C and V_{DD}= 3.3v.

⁽²⁾Add an additional 0.8mA current consumption to each analog section of the ADC. In an application environment, this current is only increased when the ADC is turned on (setting the ON bit of the ADC_CTRL2 register).

⁽³⁾ According to different packages, VREF+ can be internally connected to VDDA, VREF- can be internally connected to VSSA.

Table 4-11 Typical Current Consumption In SLEEP Mode

Symbol	Parameter	Condition	f _{HCLK}	Typ ⁽¹⁾		Unit
				Enable all peripherals ⁽²⁾	Disable all peripherals	
I _{DD}	Supply current in SLEEP mode	External clock ⁽³⁾	144MHz	25.3	8	mA
			72MHz	13.9	5.3	
			36MHz	8	3.6	
		Run in high-speed internal RC oscillator (HSI), use AHB prescaler to reduce frequency.	128MHz	24.2	6.1	mA
			72MHz	13.9	3.5	
			36MHz	7.2	2.2	

Notes:

⁽¹⁾Typical values are measured at T_A=25°C and V_{DD}= 3.3v.

⁽²⁾Add an additional 0.8mA current consumption to each analog section of the ADC. In an application environment, this current is only increased when the ADC is turned on (setting the ON bit of the ADC_CTRL2 register).

⁽³⁾External clock is 8MHz, PLL is enabled when f_{HCLK}>8MHz.

4.3.6 External Clock Source Characteristics

4.3.2.4 High-speed external clock source (HSE)

The characteristic parameters in the following table are measured using a high-speed external clock source, and the ambient temperature and supply voltage refer to the conditions specified in Table 4-3.

Table 4-12 High Speed External User Clock Features(Bypass Mode)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f _{HSE_ext}	User external clock frequency ⁽¹⁾	-	4	8	32	MHz
V _{HSEH}	OSC_IN input pin high voltage		0.8V _{DD}	-	V _{DD}	V
V _{HSEL}	OSC_IN input pin low voltage		V _{SS}	-	0.3V _{DD}	
t _{w(HSE)}	The time when OSC_IN is high or low ⁽¹⁾		16	-	-	ns
t _{r(HSE)} t _{f(HSE)}	The rising or falling time of OSC_IN ⁽¹⁾		-	-	20	
C _{in(HSE)}	OSC_IN input capacitive reactance ⁽¹⁾		-	-	5	-
DuCy _(HSE)	duty cycle	-	45	-	55	%
I _L	OSC_IN input leakage current	V _{SS} ≤V _{IN} ≤V _{DD}	-	-	±1	μA

Note:⁽¹⁾ Guaranteed by design, not tested in production.

4.3.2.5 Low-speed external clock source (LSE)

The characteristic parameters given in the following table are measured using a low speed external clock source, and

the ambient temperature and supply voltage refer to the conditions specified in Table 4-3.

Table 4-13 Features of A Low-Speed External User clock (Bypass Mode)

Symbol	Parameter	Condition	Min	Typ	Max	Unit	
f_{LSE_ext}	User external clock frequency ⁽¹⁾	-	1	32.768	1000	KHz	
V_{LSEH}	OSC32_IN input pin high voltage		$0.7V_{DD}$	-	V_{DD}	V	
V_{LSEL}	OSC32_IN input pin low voltage		V_{SS}	-	200	mV	
$t_{w(LSE)}$	The time when OSC32_IN is high or low ⁽¹⁾		450	-	-	ns	
$t_{r(LSE)}$ $t_{f(LSE)}$	The rising or falling time of OSC32_IN ⁽¹⁾		-	-	50		
$DuCy_{(LSE)}$	duty cycle		-	30	-	70	%
I_L	OSC32_IN input leakage current		$V_{SS} \leq V_{IN} \leq V_{DD}$	-	-	± 1	μA

Note: ⁽¹⁾Guaranteed by design, not tested in production.

Figure 4-5 AC Timing Diagram Of High-Speed External Clock Source

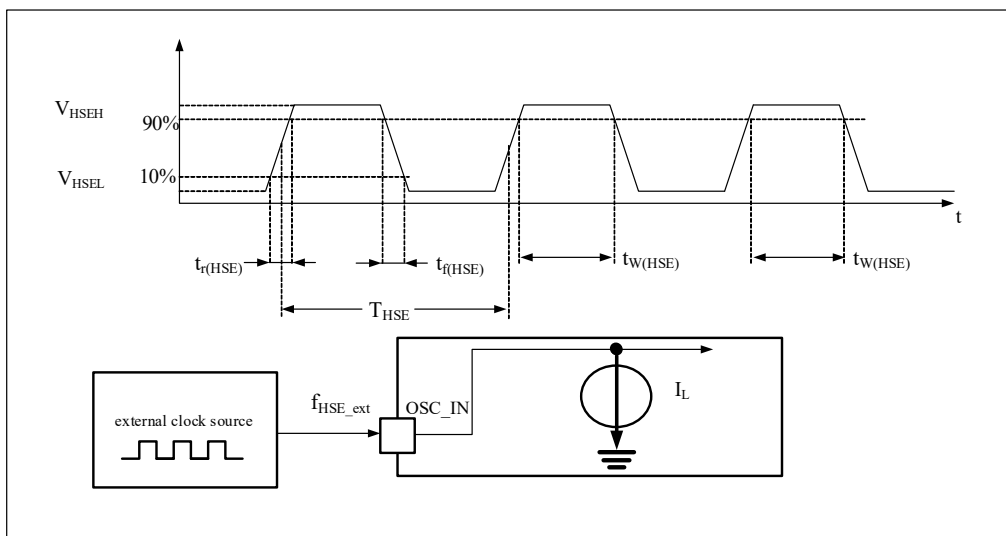
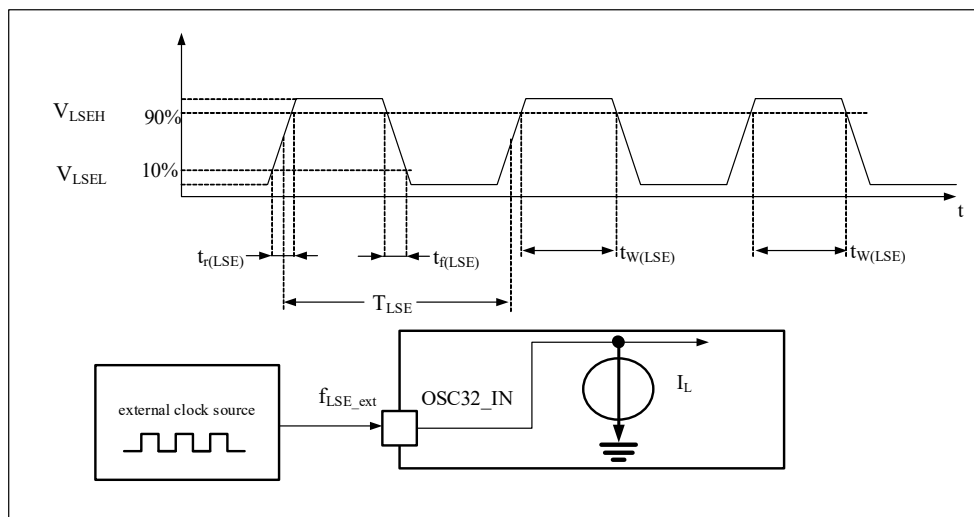


Figure 4-6 AC Timing Diagram Of External low-speed clock source



High-speed external clock generated using a crystal/ceramic resonator

High speed external clocks (HSE) can be generated using an oscillator consisting of a 4~32MHz crystal/ceramic resonator. The information presented in this section is based on a comprehensive feature evaluation using typical external components listed in the table below. In applications, the resonator and load capacitance must be as close to the oscillator pins as possible to reduce output distortion and stabilization time at startup. For detailed crystal

resonator parameters (frequency, package, accuracy, etc.), please consult the appropriate manufacturer. (The crystal resonator mentioned here is usually referred to as passive crystal oscillator).

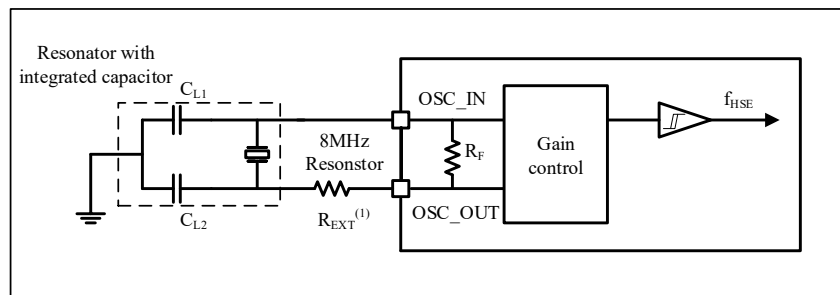
Table 4-14 HSE 4~32MHz Oscillator Characteristics⁽¹⁾⁽²⁾

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{OSC_IN}	Oscillator frequency	-	4	8	32	MHz
R_F	Feedback resistance	-	-	160	-	k Ω
i_2	HSE driving current	$V_{DD}=3.3V, V_{IN}=V_{SS}$ 30pF load	-	1.3	1.6	mA
g_m	Oscillator transconductance	Startup	-	10	-	mA/V
$t_{SU(HSE)}^{(3)}$	Start time(8M crystal)	V_{DD} is stabilized	-	3	5	ms

Note:

- ⁽¹⁾ The characteristic parameters of the resonator are given by the crystal/ceramic resonator manufacturer.
- ⁽²⁾ Guaranteed by design, it is not tested in production.
- ⁽³⁾ $t_{SU(HSE)}$ is the start time, from the time when HSE is enabled by the software to the time when a stable 8MHz oscillation is obtained. This value is measured on a standard crystal resonator and can vary widely depending on the crystal manufacturer.

Figure 4-7 Typical Application Using 8MHz Crystal



Note: ⁽¹⁾The REXT value depends on the properties of the crystal.

Low-speed external clock generated by a crystal/ceramic resonator

The low speed external clock (LSE) can be generated using an oscillator consisting of a 32.768KHz crystal/ceramic resonator. The information presented in this section is based on a comprehensive feature evaluation using typical external components listed in table below. In applications, the resonator and load capacitance must be as close to the oscillator pins as possible to reduce output distortion and stabilization time at startup. For detailed crystal resonator parameters (frequency, package, accuracy, etc.), please consult the appropriate manufacturer. (The crystal resonator mentioned here is usually referred to as passive crystal oscillator)

Note: For C_{L1} and C_{L2} , it is recommended to use high quality ceramic dielectric containers. Usually C_{L1} and C_{L2} have the same parameters. Crystal manufacturers usually give parameters for load capacitance as serial combinations of C_{L1} and C_{L2} .

Load capacitance C_L is calculated by the following formula: $C_L = C_{L1} \times C_{L2} / (C_{L1} + C_{L2}) + C_{stray}$, where C_{stray} is the capacitance of the pin and the PCB or PCB-related capacitance.

For example, if a resonator with a load capacitance of $C_L=6pF$ is selected and $C_{stray}=2pF$, then $C_{L1}=C_{L2}=8pF$.

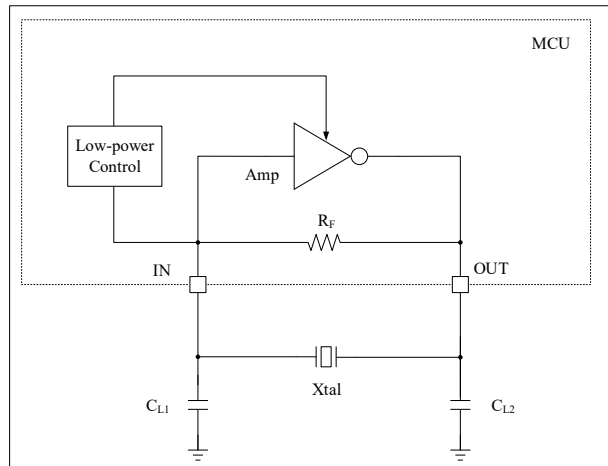
Table 4-15 LSE Oscillator Characteristics ($f_{LSE}=32.768kHz$)⁽¹⁾

Symbol	Parameter	Condition	Min	Typ	Max	Unit
R_F	Feedback resistance	-	-	5	-	M Ω
g_m	Oscillator transconductance	-	5	-	-	$\mu A/V$
$t_{SU(LSE)}^{(2)}$	Startup time	V_{DD} is stabilized	-	2	-	s

Notes:

- ⁽¹⁾ According to the comprehensive evaluation, it is not tested in production.
- ⁽²⁾ $T_{SU(LSE)}$ is the startup time, which is the period from the LSE enabled by the software to the stable 32.768kHz oscillation. This value is measured on a standard crystal resonator and can vary widely depending on the crystal manufacturer.

Figure 4-8 Typical application Using 32.768kHz Crystal^{(1) (2)}



Note:

⁽¹⁾ Please refer to the Crystal Selection Guide.

⁽²⁾ To ensure the working stability of the crystal, do not toggle the adjacent pins when the crystal is working.

4.3.7 Internal Clock Source Characteristics

The characteristic parameters given in the following table were measured using ambient temperature and supply voltage in accordance with Table 4-3.

4.3.7.1 High speed internal (HSI) RC oscillator

Table 4-16 HSI Oscillator Characteristics⁽¹⁾⁽²⁾

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{HSI}	frequency	$V_{DD}=3.3V$, $T_A=25^{\circ}C$, after calibration	7.92 ⁽³⁾	8	8.08 ⁽³⁾	MHz
DuCy _(HSI)	Duty cycle	-	45	-	55	%
ACC _{HSI}	Temperature drift of HSI oscillator ⁽⁴⁾	$V_{DD}=3.3V$, $T_A=0\sim70^{\circ}C$, temperature drift	-1.3	-	2	%
		$V_{DD}=3.3V$, $T_A=-10\sim85^{\circ}C$, temperature drift	-2	-	2.2	%
		$V_{DD}=3.3V$, $T_A=-40\sim105^{\circ}C$, temperature drift	-3	-	3	%
$t_{SU(HSI)}$	HSI oscillator start-up time	-	1	-	3	μs
$I_{DD(HSI)}$	HSI oscillator power consumption	-	-	40	100	μA

Note:

⁽¹⁾ $V_{DD}=3.3V$, $T_A=-40\sim105^{\circ}C$, unless otherwise specified.

⁽²⁾ Guaranteed by design, not tested in production.

⁽³⁾ Production calibration accuracy, excluding welding effects. Welding brings about +1.5% frequency deviation range.

⁽⁴⁾ Frequency deviation includes the effect of welding, data is from sample testing, not tested in production.

4.3.7.2 Low speed internal (LSI) RC oscillator

Table 4-17 LSI Oscillator Characteristics⁽¹⁾

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$f_{LSI}^{(2)}$	Output frequency	25 $^{\circ}C$ calibration, $V_{DD}=3.3V$	38	40	42	KHz
		$V_{DD}=1.8V\sim3.6V$, $T_A=-40\sim105^{\circ}C$	30	48	60	KHz
$t_{SU(LSI)}^{(2)}$	LSI oscillator start-up time	-	-	30	80	μs
$I_{DD(LSI)}^{(2)}$	LSI oscillator power consumption	-	-	0.2	-	μA

Notes:

(1) $V_{DD}= 3.3V$, $T_A=-40 \sim 105^{\circ}C$, unless otherwise specified.

(2) Guaranteed by design, not tested in production.

4.3.8 Time to Wake Up From Low Power Mode

The wake-up time listed in Table 4-18 is measured during the wake-up phase of an 8MHz HSI RC oscillator. The clock source used when waking up depends on the current operating mode:

- STOP0/STOP2/STANDBY mode: Clock source is RC oscillator.
- SLEEP mode: Clock source is the clock used when entering SLEEP mode.

All times were measured using ambient temperature and supply voltage in accordance with Table 4-3.

Table 4-18 Wake-up Time in Low Power Mode

Symbol	Parameter	Typ	Unit
$t_{WUSLEEP}^{(1)}$	Wake up from SLEEP mode	480	ns
$t_{WUSTOP0}^{(1)}$	Wake up from STOP0 (voltage regulator is in running mode)	20	μs
	Wake up from STOP 0 (voltage regulator is in low power mode)	22	
$t_{WUSTOP2}^{(1)}$	Wake up from STOP2	40	
$t_{WUSTDBY}^{(1)}$	Wake up from STANDBY mode	100	

Notes: (1) The wake-up time is measured from the start of the wake-up event to the first instruction read by the user program.

4.3.9 PLL Characteristics

The parameters listed in Table 4-19 are measured when the ambient temperature and power supply voltage refer to the conditions in Table 4-3.

Table 4-19 PLL Features

Symbol	Parameter	Value			Unit
		Min	Typ	Max ⁽¹⁾	
f_{PLL_IN}	PLL input clock ⁽²⁾	4	8.0	32	MHz
	PLL input clock duty cycle	40	-	60	%
f_{PLL_OUT}	PLL frequency doubling output clock	32	-	144	MHz
t_{LOCK}	PLL lock time.	-	-	150	μs
Jitter	Rms cycle-to-cycle jitter @144MHz	-	5	-	ps
I_{pll}	Operating Current of PLL @144MHz VCO frequency.	-	-	850	μA

Note:

(1) Based on comprehensive evaluation, not tested in production.

(2) Care needs to be taken to use the correct frequency doubling factor to input the clock frequency according to PLL so that f_{PLL_OUT} is within the allowable range.

4.3.10 FLASH Memory Characteristics

Unless otherwise specified, all characteristic parameters are obtained at $T_A= -40\sim 105^{\circ}C$.

Table 4-20 Flash Memory Characteristics

Symbol	Parameter	Condition	Min ⁽¹⁾	Typ ⁽¹⁾	Max ⁽¹⁾	Unit
t _{prog}	32-bit programming time	T _A = -40~105°C	-	112	225	μs
t _{ERASE}	Page (2K bytes) erase time	T _A = -40~105°C	-	2	20 ⁽²⁾ 100 ⁽³⁾	ms
t _{ME}	Whole erase time	T _A = -40~105°C;	-	-	100	ms
I _{DD}	Power supply current	Read mode, f _{HCLK} =144MHz,3 waiting cycles, V _{DD} =3.3V	-	-	3.62	mA
		Write mode, f _{HCLK} =144MHz, V _{DD} =3.3V	-	-	6.5	mA
		Erase mode, f _{HCLK} =144MHz, V _{DD} =3.3V	-	-	4.5	mA
		Power-down mode/shutdown, V _{DD} = 3.3 ~ 3.6V.	-	-	0.035	μA
V _{prog}	Programming voltage	-	1.8	3.0	3.6	V

Notes:

⁽¹⁾ Guaranteed by design, not tested in production.

⁽²⁾ Memory space with 10k erase times

⁽³⁾ Memory space with 100k erasing times

Table 4-21 Flash Endurance and Data Retention

Symbol	Parameter	Condition	Min ⁽¹⁾	Unit
N _{END}	Endurance (Note: number of erasures)	T _A =-40 ~ 105°C ; The Flash capacity is 256KB.	10	Thousand times
		T _A =-40 ~ 105°C; The Flash capacity is 512KB, of which the first 256KB of storage space	10	
		T _A =-40 ~ 105°C; The Flash capacity is 512KB, including the last 256KB of storage space.	100	
t _{RET}	Data retention period	T _A = 85°C	20	year

Note: ⁽¹⁾ Based on comprehensive evaluation, not tested in production.

4.3.11 Absolute Maximum (Electrical Sensitivity)

Based on three different tests (ESD, LU), a specific measurement method is used to test the strength of the chip to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharge (a positive pulse followed by a negative pulse one second later) is applied to all pins of all samples.

Table 4-22 Absolute Maximum ESD value

Symbol	Parameter	Condition	Type	Min ⁽¹⁾	Unit
V _{ESD(HBM)}	Electrostatic discharge voltage (Human body model)	T _A = +25 °C, In accordance with MIL-STD-883K Method 3015.9	3A	4000	V
V _{ESD(CDM)}	Electrostatic discharge voltage (Charging device model)	T _A = +25 °C, In accordance with ESDA/JEDEC JS-002-2018	C3	1000	

Note: ⁽¹⁾ Based on comprehensive evaluation, not tested in production.

Static latch-up

In order to evaluate the latch-up performance, two complementary static latching tests need to be performed on 6 samples:

- Supply voltage exceeding limit for each power pin.

- Current is injected into each input, output, and configurable I/O pin.

This test conforms to EIA/JESD78A integrated circuit latch-up standard.

Table 4-23 Electrical Sensitivity

Symbol	Parameter	Condition	Type	Min ⁽¹⁾
LU	Static latch-up type	T _A = +25 °C, in accordance with JESD78A	Class II A	±100mA, 1.5*V _{DDMAX}

Note: ⁽¹⁾ Test at room temperature.

4.3.12 I/O Port Characteristics

General input/output characteristics

Unless otherwise specified, the parameters listed in the following table are measured according to the conditions in Table 4-3. All I/O ports are CMOS and TTL compatible.

Table 4-24 I/O Static Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V _{IL}	Input low level voltage	TTL port	V _{SS}	-	0.8	V
V _{IH}	Input high level voltage		2	-	V _{DD}	
V _{IL}	Input low level voltage	CMOS port	V _{SS}	-	0.35 V _{DD}	
V _{IH}	Input high level voltage		0.65 V _{DD}	-	V _{DD}	
V _{hys}	Schmitt trigger voltage hysteresis ⁽¹⁾	V _{DD} =3.3V	200	-	-	mV
		V _{DD} =2.5V	200	-	-	
		V _{DD} =1.8V	0.1*V _{DD} ⁽²⁾	-	-	
I _{lkg}	Input leakage current ⁽³⁾	V _{DD} =Maximum V _{PAD} =0 or V _{PAD} =V _{DD} ⁽⁵⁾	-1	-	1	μA
R _{PU}	Weak pull-up equivalent resistance ⁽⁴⁾	V _{DD} =3.3V, V _{IN} =V _{SS}	75	-	220	kΩ
		V _{DD} =2.5V, V _{IN} =V _{SS}	95	-	310	
		V _{DD} =1.8V, V _{IN} =V _{SS}	135	-	500	
R _{PD}	Weak pull-down equivalent resistance ⁽⁴⁾	V _{DD} =3.3V, V _{IN} =V _{DD}	75	-	235	kΩ
		V _{DD} =2.5V, V _{IN} =V _{DD}	85	-	315	
		V _{DD} =1.8V, V _{IN} =V _{DD}	120	-	495	
C _{IO}	Capacitance of I/O pin	-	-	5	-	pF

Notes:

⁽¹⁾ Hysteresis voltage of Schmitt trigger switch level. Based on comprehensive evaluation, not tested in production.

⁽²⁾ At least 100mV.

⁽³⁾ If there is reverse current backflow at the adjacent pins, the leakage current may be higher than the maximum value.

⁽⁴⁾ Pull-up and pull-down resistors are implemented with a switchable PMOS/NMOS.

⁽⁵⁾ V_{PAD} refers to the input voltage of the IO pin.

All I/O ports are CMOS and TTL compatible (no software configuration required) and their features take into account most of the strict CMOS process or TTL parameters:

- For V_{IH}:
If V_{DD} is between [1.8V ~ 3.08V]; Uses CMOS features but includes TTL.
If V_{DD} is between [3.08V ~ 3.60V]; Uses TTL feature but includes CMOS.
- For V_{IL}:
If V_{DD} is between [1.8V ~ 2.28V]; Uses TTL feature but includes CMOS.

If V_{DD} is between [2.28V ~ 3.60V]; Uses CMOS features but includes TTL.

Output drive current

GPIO (general purpose input/output port) can absorb or output up to +/-12mA current. In user applications, the number of I/O pins must ensure that the driving current does not exceed the absolute maximum rating given in Section 0:

- The sum of the current drawn from V_{DD} by all I/O ports, plus the maximum operating current drawn by the

MCU on V_{DD} , cannot exceed the absolute maximum rating of I_{VDD} (Table 4-2).

- The sum of the current drawn by all I/O ports and drawn from V_{SS} , plus the maximum operating current drawn by the MCU on V_{SS} , cannot exceed the absolute maximum ratings, I_{VSS} (Table 4-2).

Output voltage

Unless otherwise specified, the parameters listed in Table 4-26 were measured using ambient temperature and VDD supply voltage in accordance with Table 4-3. All I/O ports are CMOS and TTL compatible.

Table 4-25 IO Driving Capability Table

Driving grade	Condition	$I_{OH}^{(1)}$, VDD=3.3V	$I_{OL}^{(1)}$, VDD=3.3V	$I_{OH}^{(1)}$, VDD=2.5V	$I_{OL}^{(1)}$, VDD=2.5V	$I_{OH}^{(1)}$, VDD=1.8V	$I_{OL}^{(1)}$, VDD=1.8V	Unit
2	105° C	-2	2	-1.5	1.5	-1.2	1.2	mA
4	105° C	-4	4	-3	3	-2.5	2.5	
8	105° C	-8	8	-7	7	-5	5	
12	105° C	-12	12	-11	11	-7.5	7.5	

Note: ⁽¹⁾Guaranteed by design, not tested in production.

Table 4-26 Output Voltage Characteristic

Symbol	Parameter	Condition	Min	Max	Unit
$V_{OL}^{(1)}$	Output low level	$V_{DD} = 3.3$ V, drive level ⁽⁴⁾ 2/4/8/12	V_{SS}	0.55	V
		$V_{DD} = 2.5$ V, drive level ⁽⁴⁾ 2/4/8/12	V_{SS}	0.45	
		$V_{DD} = 1.8$ V, drive level ⁽⁴⁾ 2/4/8/12	V_{SS}	0.684	
$V_{OH}^{(2)}$	Output high level	$V_{DD} = 3.3$ V, drive level ⁽⁴⁾ 2/4/8/12	2.4 ⁽³⁾	V_{DD}	
		$V_{DD} = 2.5$ V, drive level ⁽⁴⁾ 2/4/8/12	1.8 ⁽³⁾	V_{DD}	
		$V_{DD} = 1.8$ V, drive level ⁽⁴⁾ 2/4/8/12	0.8* V_{DD}	V_{DD}	

Note:

⁽¹⁾ The current I_{IO} absorbed by the chip must always follow the absolute maximum rating given in Table 4-2, and the sum of I_{IO} (all I/O pins and control pins) must not exceed I_{VSS} .

⁽²⁾ The current I_{IO} output from the chip must always follow the absolute maximum rating given in Table 4-2, and the sum of I_{IO} (all I/O pins and control pins) must not exceed I_{VDD} .

⁽³⁾ PC13, PC14 and PC15 are not in this range. ⁽⁴⁾ See Table 4-25 for actual driving capacity.

Input-output AC characteristics

The values measured under ambient temperature and supply voltage conditions in accordance with Figure 4-9 and Table 4-27.

Unless otherwise specified, the parameters listed in Table 4-27 were measured under ambient temperature and supply voltage in accordance with Table 4-3.

Table 4-27 Output AC Characteristics⁽¹⁾

DS_CFGy Configuration	PMODEy[1:0] Configuration	Symbol	Parameter	Condition	Min	Max	Unit
0	xx (2mA)	f _{max(IO)out}	Maximum frequency ⁽²⁾	C _L =5pF, V _{DD} =3.3V	-	75	MHz
				C _L =5pF, V _{DD} =2.5V	-	50	
				C _L =5pF, V _{DD} =1.8V	-	30	
		t _{(IO)out}	Output delay	C _L =5pF, V _{DD} =3.3V	-	3.66	ns
				C _L =5pF, V _{DD} =2.5V	-	4.72	
				C _L =5pF, V _{DD} =1.8V	-	7.12	
t _{(IO)in}	Input delay	C _L =50fF, V _{DD} =2.97V, V _{DDD} =0.81V input characteristics at 1.8V and 2.5V are derated	-	2	ns		
1	00/01 (4mA)	f _{max(IO)out}	Maximum frequency ⁽²⁾	C _L = 10pF, V _{DD} = 3.3V	-	90	MHz
				C _L =10pF, V _{DD} =2.5V	-	60	
				C _L =10pF, V _{DD} =1.8V	-	40	
		t _{(IO)out}	Output delay	C _L = 10pF, V _{DD} = 3.3V	-	3.5	ns
				C _L =10pF, V _{DD} =2.5V	-	4.5	
				C _L =10pF, V _{DD} =1.8V	-	6.74	
t _{(IO)in}	Input delay	C _L =50fF, V _{DD} =2.97V, V _{DDD} =0.81V input characteristics at 1.8V and 2.5V are derated	-	2	ns		
1	10 (8mA)	f _{max(IO)out}	Maximum frequency ⁽²⁾	C _L = 20pF, V _{DD} = 3.3V	-	100	MHz
				C _L =20pF, V _{DD} =2.5V	-	75	
				C _L =20pF, V _{DD} =1.8V	-	50	
		t _{(IO)out}	Output delay	C _L = 20pF, V _{DD} = 3.3V	-	3.42	ns
				C _L =20pF, V _{DD} =2.5V	-	4.73	
				C _L =20pF, V _{DD} =1.8V	-	6.53	
t _{(IO)in}	Input delay	C _L =50fF, V _{DD} =2.97V, V _{DDD} =0.81V input characteristics at 1.8V and 2.5V are derated	-	2	ns		
1	11 (12mA)	f _{max(IO)out}	Maximum frequency ⁽²⁾	C _L = 30pF, V _{DD} = 3.3V	-	120	MHz
				C _L =30pF, V _{DD} =2.5V	-	90	
				C _L =30pF, V _{DD} =1.8V	-	60	
		t _{(IO)out}	Output delay	C _L = 30pF, V _{DD} = 3.3V	-	3.34	ns
				C _L =3pF, V _{DD} =2.5V	-	4.26	
				C _L =3pF, V _{DD} =1.8V	-	6.34	
t _{(IO)in}	Input delay	C _L =50fF, V _{DD} =2.97V, V _{DDD} =0.81V input characteristics at 1.8V and 2.5V are derated	-	2	ns		

Notes:

⁽¹⁾I/O port speed can be configured by DS_CFGy and PMODEy[1:0]. See N32A455 Series User Manual for the description of GPIO port configuration register.

⁽²⁾The maximum frequency is Figure 4-9 Define.

Figure 4-9 Input Output AC Characteristic Definition

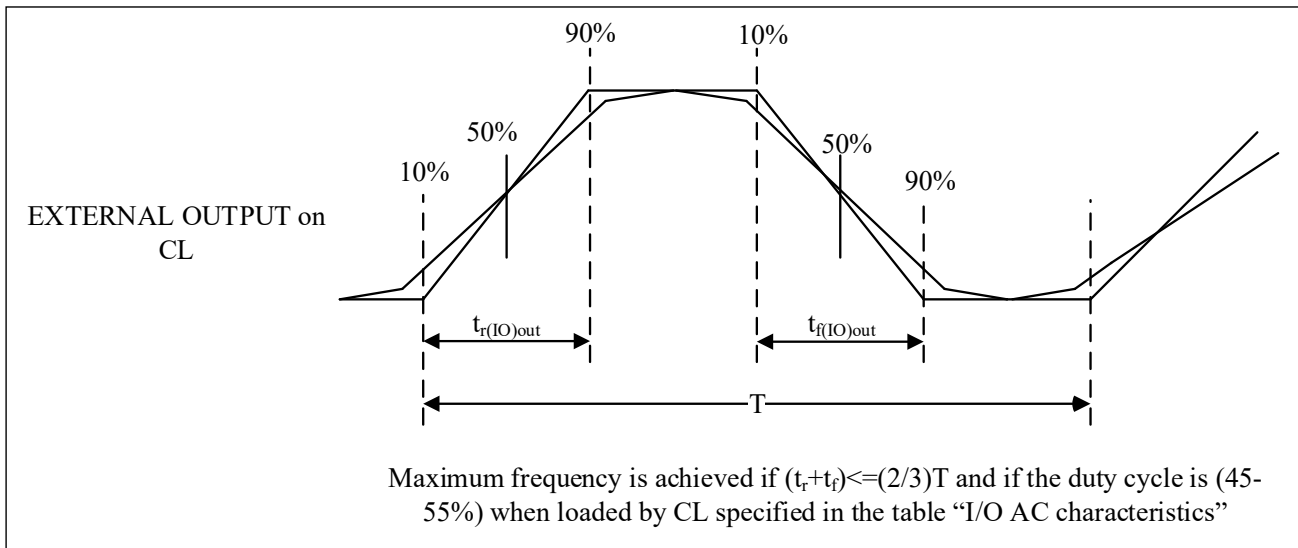
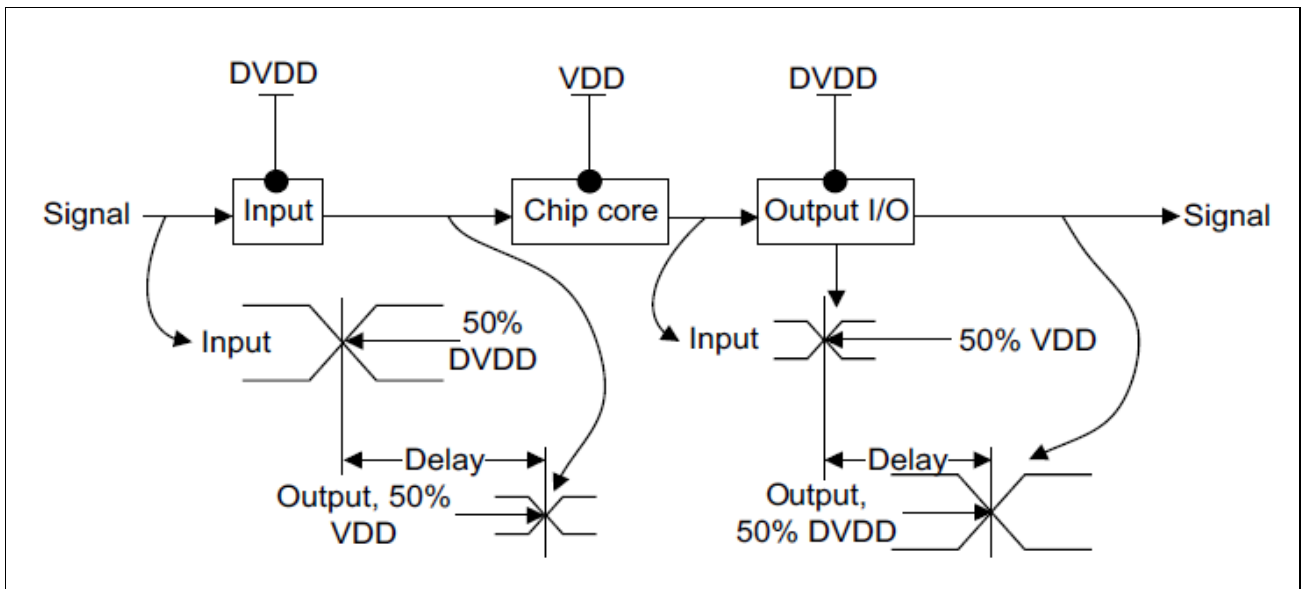


Figure 4-10 Transmission Delay



4.3.13 NRST Pin Characteristics

The NRST pin input driver uses CMOS technology and integrates a pull-up resistor that cannot be disconnected, R_{PU} (see Table 4-28). Unless otherwise specified, the parameters listed in Table 4-28 are measured under the ambient temperature and supply voltage in accordance with the conditions in Table 4-3.

Table 4-28 NRST Pin Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$V_{IL(NRST)}^{(1)}$	NRST input low voltage	$V_{DD} = 3.3 \text{ V}$	V_{SS}	-	0.8	V
		$V_{DD} = 1.8 \text{ V}$	V_{SS}	-	$0.3 * V_{DD}$	
$V_{IH(NRST)}^{(1)}$	NRST input high voltage	$V_{DD} = 3.3 \text{ V}$	2	-	V_{DD}	V
		$V_{DD} = 1.8 \text{ V}$	$0.7 * V_{DD}$	-	V_{DD}	
$V_{hys(NRST)}$	NRST Schmitt trigger voltage hysteresis	$V_{DD} = 3.3 \text{ V}$	200	-	-	mV
		$V_{DD} = 1.8 \text{ V}$	$0.1 * V_{DD}$	-	-	V
R_{PU}	Weak pull-up equivalent resistance ⁽²⁾	$V_{DD} = 3.3 \text{ V}$	30	50	70	K Ω
$V_{F(NRST)}^{(1)}$	NRST input filtered pulse	-	-	-	100	ns

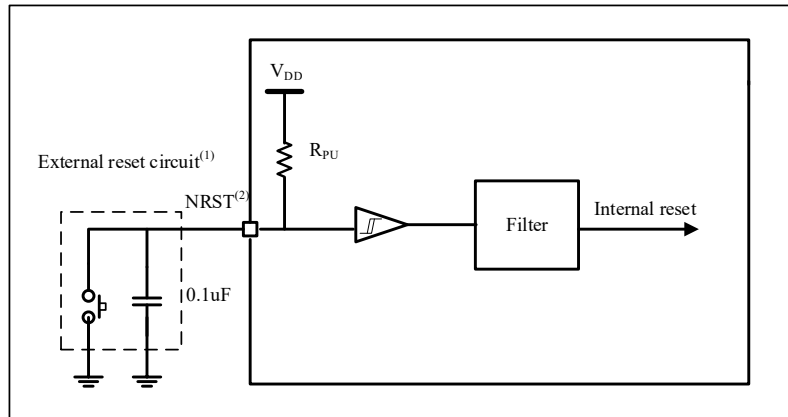
Symbol	Parameter	Condition	Min	Typ	Max	Unit
$V_{NF(NRST)}^{(1)}$	NRST input unfiltered pulse	-	300	-	-	ns

Notes:

⁽¹⁾Guaranteed by design, not tested in production.

⁽²⁾The pull-up resistor is designed as a real resistor in series with a switchable PMOS. The resistance of this PMON/NMOS switch is very small (about 10%).

Figure 4-11 Recommended NRST Pin Protection



Notes:

⁽¹⁾ Filter circuit to protect the device against parasitic resets.

⁽²⁾ The user must ensure that the NRST pin potential is below the maximum $V_{IL(NRST)}$ listed in Table 4-28, otherwise the MCU cannot be reset.

4.3.14 Timer and Watchdog Characteristics

4.3.12 I/O Port Characteristics for details on the features of the I/O reuse function pins (output comparison, input capture, external clock, PWM output), See section 0

Table 4-29 TIM1/8 Characteristics⁽¹⁾

Symbol	Parameter	Condition	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time	-	1	-	$t_{TIMxCLK}$
		$f_{TIMxCLK} = 144MHz$	6.95	-	ns
f_{EXT}	Timer CH1 to CH4 external clock frequency	-	0	$f_{TIMxCLK}/2$	MHz
		$f_{TIMxCLK} = 144MHz$	0	72	MHz
RESTIM	Timer resolution	-	-	16	bit
$t_{COUNTER}$	16-bit counter clock cycle when internal clock is selected	-	1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK} = 144MHz$	0.00695	455	μs
t_{MAX_COUNT}	Maximum count	-	-	65536×65536	$t_{TIMxCLK}$
		$f_{TIMxCLK} = 144MHz$	-	29.8	s

Note: ⁽¹⁾Guaranteed by design, not tested in production.

Table 4-30 TIM2/3/4/5 Characteristics⁽¹⁾

Symbol	Parameter	Condition	Min	Max	Unit
t _{res(TIM)}	Timer resolution time	-	1	-	t _{TIMxCLK}
		f _{TIMxCLK} = 72MHz	13.9	-	ns
f _{EXT}	Timer CH1 to CH4 external clock frequency	-	0	f _{TIMxCLK} /2	MHz
		f _{TIMxCLK} = 72MHz	0	36	MHz
RE _{TIM}	Timer resolution	-	-	16	bit
t _{COUNTER}	16-bit counter clock cycle when internal clock is selected	-	1	65536	t _{TIMxCLK}
		f _{TIMxCLK} = 72MHz	0.0139	910	μs
t _{MAX_COUNT}	Maximum count	-	-	65536 x 65536	t _{TIMxCLK}
		f _{TIMxCLK} = 72MHz	-	59.6	s

Note: ⁽¹⁾ Guaranteed by design, not tested in production.

Table 4-31 IWDG Counting Maximum and Minimum Reset Time (LSI = 40 KHz)

Prescaler	IWDG_PREDIV.PD[2:0]	Min ⁽¹⁾ IWDG_RELV.REL[11:0]=0	Max ⁽¹⁾ IWDG_RELV.REL[11:0]=0xFFF	Unit
/4	000	0.1	409.6	ms
/8	001	0.2	819.2	
/16	010	0.4	1638.4	
/32	011	0.8	3276.8	
/64	100	1.6	6553.6	
/128	101	3.2	13107.2	
/256	11x	6.4	26214.4	

Note: ⁽¹⁾ Guaranteed by design, not tested in production.

Table 4-32 WWDG Counting Maximum and Minimum Reset Time (APB1 PCLK1 = 36MHz)

Prescaler	WWDG_CFG.TIMERB[1:0]	Min ⁽¹⁾ WWDG_CFG.W[6:0]=0x3F	Max ⁽¹⁾ WWDG_CFG.W[6:0]=0x7F	Unit
/1	00	0.113	7.28	ms
/2	01	0.227	14.56	
/3	10	0.455	29.12	
/4	11	0.910	58.25	

Note: ⁽¹⁾ Guaranteed by design, not tested in production.

4.3.15 I2C Interface Characteristics

Unless otherwise specified, the parameters listed in Table 4-33 were measured using ambient temperature, f_{PCLK1} frequency, and V_{DD} supply voltage in accordance with Table 4-3.

The I2C interface of the N32A455xxL7 product conforms to the standard I2C communication protocol, but has the following limitations: SDA and SCL are not "true" open leak pins, and when configured for open leak output, the PMOS tube between the pin and VDD is closed, but still exists.

I2C interface features are listed in Table 4-33. See Section 0 for details about the features of the input/output multiplexing function pins (SDA and SCL).

Table 4-33 I²C Interface Characteristics

Symbol	Parameter	Standard Mode ⁽¹⁾⁽²⁾		Fast Mode ⁽¹⁾⁽²⁾		Fast+ Mode ⁽¹⁾⁽²⁾		Unit
		Min	Max	Min	Max	Min	Max	
f _{SCL}	I2C interface frequency	0.0	100	0	400	0	1000	KHz
t _{h(STA)}	Start condition holding time	4.0	-	0.6	-	0.26	-	μs
t _{w(SCKL)}	SCL clock low time	4.7	-	1.3	-	0.5	-	μs
t _{w(SCKH)}	SCL clock high time	4.0	-	0.6	-	0.26	-	μs
t _{su(STA)}	Repeated start condition set up time	4.7	-	0.6	-	0.26	-	μs
t _{h(SDA)}	SDA data hold time	-	3.4	-	0.9	-	0.4	μs
t _{su(SDA)}	SDA setup time	250.0	-	100	-	50	-	ns
t _{r(SDA)} t _{r(SCL)}	SDA and SCL rising time	-	1000	20+0.1Cb	300	-	120	ns
t _{f(SDA)} t _{f(SCL)}	SDA and SCL falling time	-	300	20+0.1Cb	300	-	120	ns
t _{su(STO)}	Stop condition set up time	4.0	-	0.6	-	0.26	-	μs
t _{w(STO:STA)}	Time from stop condition to start condition (bus idle)	4.7	-	1.3	-	0.5	-	μs
C _b	Capacitive load per bus	-	400	-	400	-	100	pF
t _{v(SDA)}	Data valid time	-	3.45	-	0.9	-	0.45	μs
t _{v(ACK)}	Response effective time	-	3.45	-	0.9	-	0.45	μs

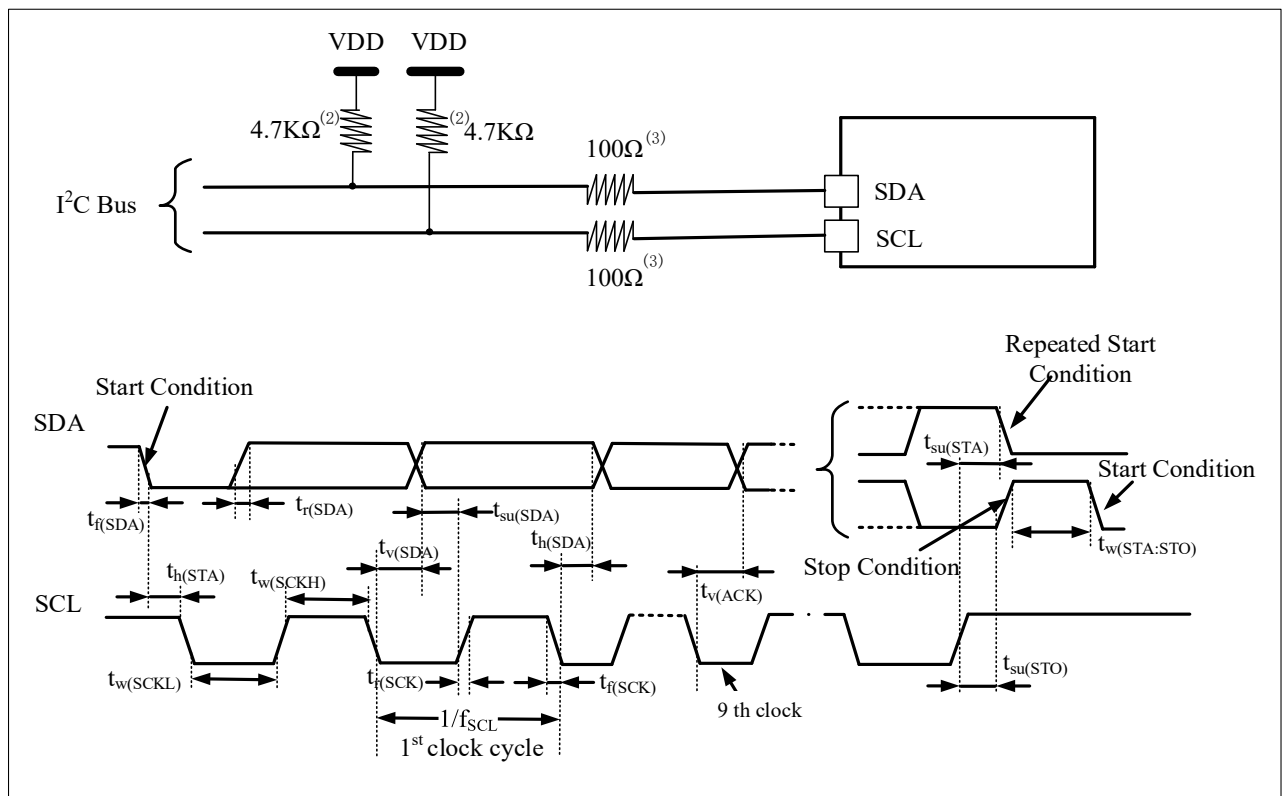
Note:

⁽¹⁾Guaranteed by design, not tested in production.

⁽²⁾To achieve the maximum frequency of standard mode I²C, f_{CLK1} must be greater than 2MHz. To achieve the maximum frequency of fast mode I²C, f_{CLK1} must be greater than 4MHz.

⁽³⁾Above parameter conditions -40~105°C

Figure 4-12 I²C Bus AC Waveform and Measurement Circuit⁽¹⁾



Note:

⁽¹⁾The measuring points are set at CMOS level: 0.3V_{DD} and 0.7V_{DD}.

⁽²⁾The pull-up resistor depends on the I2C interface speed.

⁽³⁾The resistance value depends on the actual electrical characteristics. The signal line can be directly connected without serial resistance.

4.3.16 SPI/I2S Interface Characteristics

Unless otherwise specified, the SPI parameters listed in Table 4-34 / Table 4-35 and the I²S parameters listed in Table 4-36 are measured using ambient temperature, f_{PCLKx} frequency, and V_{DD} supply voltage in accordance with Table 4-3.

See section 0 for details on the characteristics of the I/O multiplexed pins (NSS, SCLK, MOSI, MISO for SPI, WS, CLK, SD for I²S).

Table 4-34 SPI1 Features⁽¹⁾

Symbol	Parameter	Condition	Min	Max(105 °C)	Unit
f _{SCLK} 1/t _c (SCLK)	SPI clock frequency	Master mode	-	36	MHz
		Slave mode	-	36	
t _r (SCLK)t _f (SCLK)	SPI clock rise and fall time	Capacitance: C = 30pF	-	6	ns
DuCy(SCK)	SPI slave input clock duty cycle	SPI slave mode	45	55	%
t _{su} (NSS) ⁽¹⁾	NSS setup time	Slave mode	4t _{PCLK}	-	ns
t _h (NSS) ⁽¹⁾	NSS hold time	Slave mode	2t _{PCLK}	-	
t _w (SCLKH) ⁽¹⁾ t _w (SCLKL) ⁽¹⁾	SCLK high and low time	Master mode	t _{PCLK} - 2	t _{PCLK} + 2	
t _{su} (MI) ⁽¹⁾	Enter the data setup time.	Master mode	3.5	-	
t _{su} (SI) ⁽¹⁾		Slave mode	3	-	
t _h (MI) ⁽¹⁾	Enter the data retention time	Master mode	3	-	
t _h (SI) ⁽¹⁾		Slave mode	3	-	
t _a (SO) ⁽¹⁾⁽²⁾	Data output access time	Slave mode, f _{PCLK} = 20MHz	0	3t _{PCLK}	
t _{dis} (SO) ⁽¹⁾⁽³⁾	Data output prohibition time	Slave mode	2	10	
t _v (SO) ⁽¹⁾	Data output effective time	Slave mode (after enabling edge)	-	12.5	
t _v (MO) ⁽¹⁾		Master mode (after enable edge)	-	6.5	
t _h (SO) ⁽¹⁾	Data output holding time	Slave mode (after enabling edge)	5	-	
t _h (MO) ⁽¹⁾		Master mode (after enable edge)	-0.5	-	

Table 4-35 SPI2/3 Features⁽¹⁾

Symbol	Parameter	Condition	Min	Max(105 °C)	Unit	
f _{SCLK} 1/t _c (SCLK)	SPI clock frequency	Master mode	-	18	MHz	
		Slave mode	-	18		
t _r (SCLK)t _f (SCLK)	SPI clock rise and fall time	Capacitance: C = 30pF	-	8	ns	
DuCy(SCK)	SPI slave input clock duty cycle	SPI slave mode	45	55	%	
t _{su} (NSS) ⁽¹⁾	NSS setup time	Slave mode	4t _{PCLK}	-	ns	
t _h (NSS) ⁽¹⁾	NSS hold time	Slave mode	2t _{PCLK}	-		
t _w (SCLKH) ⁽¹⁾ t _w (SCLKL) ⁽¹⁾	SCLK high and low time	Master mode	t _{PCLK} - 2	t _{PCLK} + 2		
t _{su} (MI) ⁽¹⁾	Enter the data setup time.	Master mode	SPI2	4		-
			SPI3	5		-

$t_{su(SI)}^{(1)}$		Slave mode	SPI2	4	-
			SPI3	5	-
$t_{h(MI)}^{(1)}$	Enter the data retention time	Master mode	SPI2	2	-
			SPI3	2.5	-
$t_{h(SI)}^{(1)}$		Slave mode	SPI2	2	-
			SPI3	2	-
$t_{a(SO)}^{(1)(2)}$	Data output access time	Slave mode, $f_{PCLK} = 20\text{MHz}$		0	$3t_{PCLK}$
$t_{dis(SO)}^{(1)(3)}$	Data output prohibition time	Slave mode		2	10
$t_{v(SO)}^{(1)}$	Data output effective time	Slave mode (after enabling edge)	SPI2	-	13.5
			SPI3	-	17.5
$t_{v(MO)}^{(1)}$		Master mode (after enable edge)	SPI2	-	6.5
			SPI3	-	9
$t_{h(SO)}^{(1)}$	Data output holding time	Slave mode (after enabling edge)	SPI2	4	-
			SPI3		
$t_{h(MO)}^{(1)}$		Master mode (after enable edge)	SPI2	1	-
			SPI3		

Notes:

⁽¹⁾Guaranteed by design, not tested in production.

⁽²⁾The minimum value represents the minimum time to drive the output, and the maximum value represents the maximum time to get the data correctly.

⁽³⁾The minimum value represents the minimum time for turning off the output and the maximum value represents the maximum time for placing the data line in a high resistance state.

Figure 4-13 SPI Timing Diagram-Slave Mode and CLKPHA=0

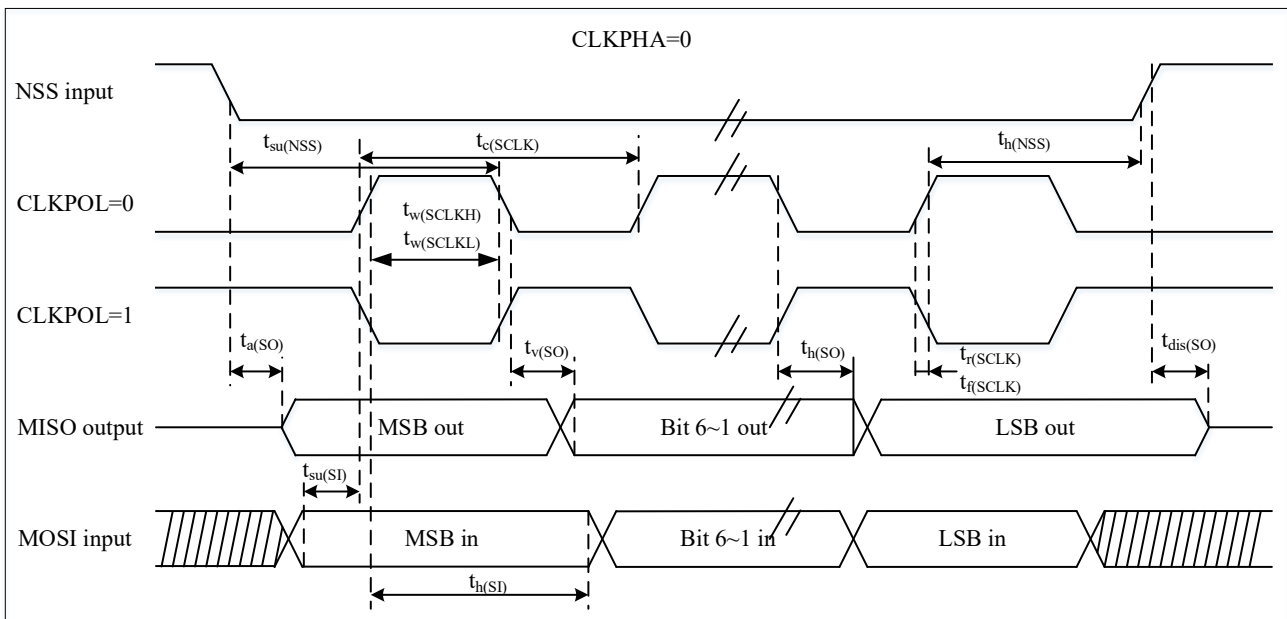
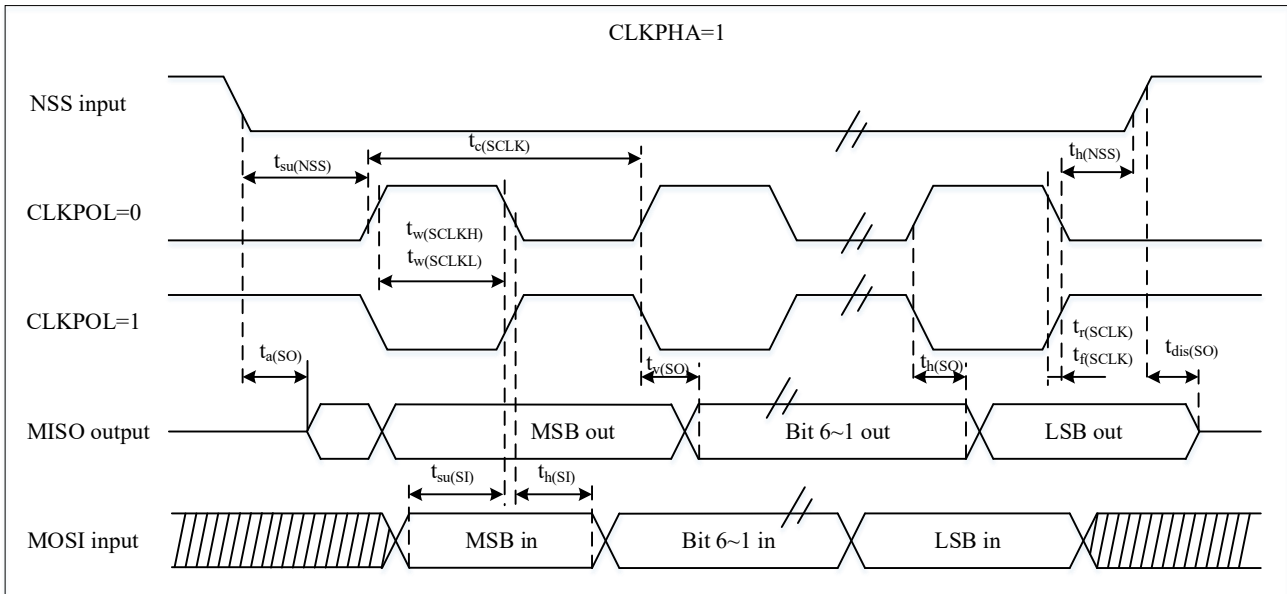
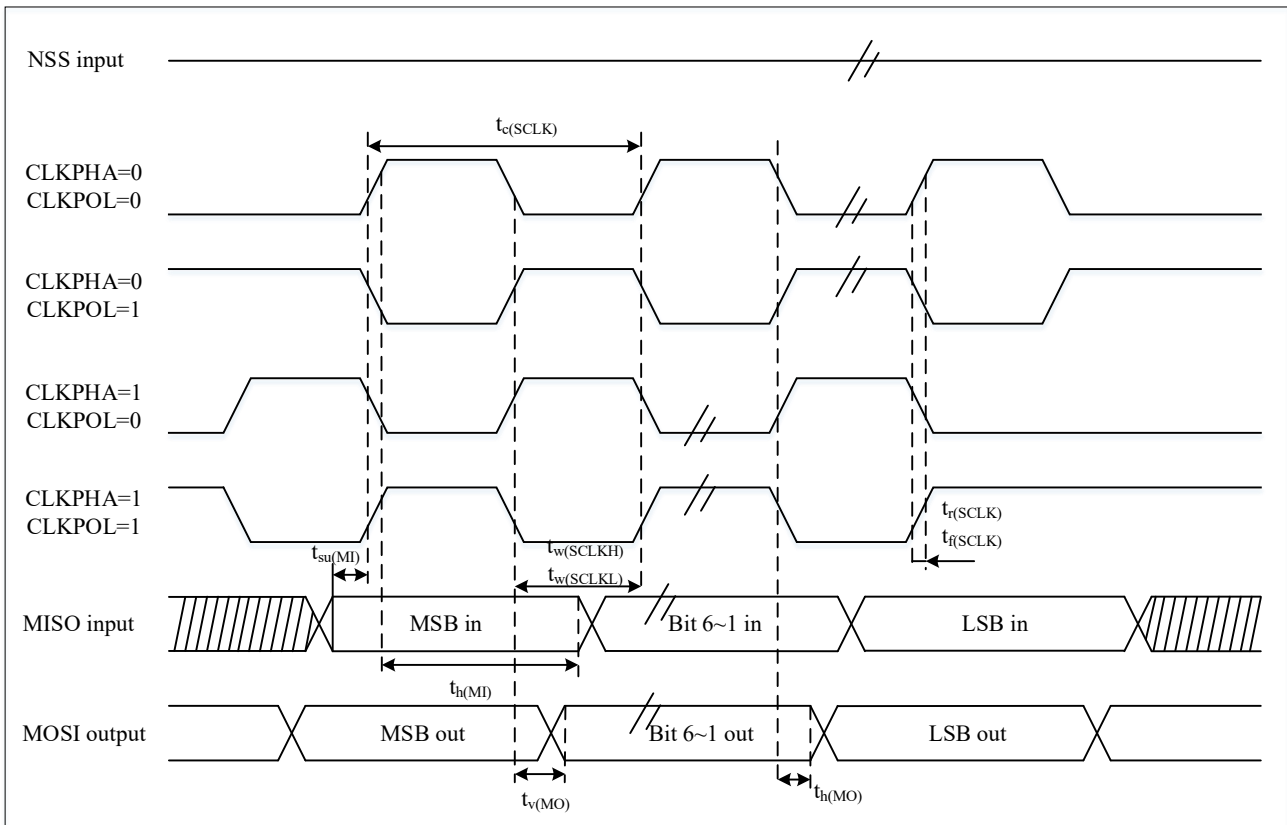


Figure 4-14 SPI Timing Diagram-Slave Mode and CLKPHA=1⁽¹⁾



Note: ⁽¹⁾ The measuring points is set at 0.3V_{DD} and 0.7V_{DD}.

Figure 4-15 SPI Timing Diagram-Master Mode⁽¹⁾



Note: ⁽¹⁾ The measuring points is set at 0.3V_{DD} and 0.7V_{DD}.

Table 4-36 I²S Characteristics⁽¹⁾

Symbol	Parameter	Condition	Min	Max(105 °C)	Unit	
DuCy(SCK)	I ² S slave input clock duty cycle	I2S slave mode	30	70	%	
f _{MCLK}	I ² S master clock	Master mode	-	256Fs ⁽³⁾	MHz	
f _{CLK} 1/t _{c(CLK)}	I ² S clock frequency	Master mode (32bit)	-	64*Fs ⁽³⁾		
		Slave mode (32bit)	-	64*Fs ⁽³⁾		
t _{r(CLK)} t _{f(CLK)}	I ² S clock rise and fall time	Capacitance: CL = 50pF	-	8	ns	
t _{v(WS)} ⁽¹⁾	WS valid time	Master mode	I2S2	4.5		-
			I2S3	6.5		-
t _{h(WS)} ⁽¹⁾	WS holding time	Master mode	I2S2	4.5		-
			I2S3	0.5		-
t _{su(WS)} ⁽¹⁾	WS setup time	Slave mode	I2S2	5.5		-
			I2S3	7		-
t _{h(WS)} ⁽¹⁾	WS holding time	Slave mode	I2S2	1.5		-
			I2S3	2.5		-
t _{w(CLKH)} ⁽¹⁾	CLK high and low time	Master mode, f _{PCLK} = 16MHz, audio frequency 48kHz		312.5		-
t _{w(CLKL)} ⁽¹⁾				345		-
t _{su(SD_MR)} ⁽¹⁾	Enter the data setup time.	Master receiver	I2S2	4		-
			I2S3	5		-
t _{su(SD_SR)} ⁽¹⁾		Slave receiver	I2S2	4		-
			I2S3	4.5		-
t _{h(SD_MR)} ⁽¹⁾⁽²⁾	Enter the data retention time	Master receiver	I2S2	1.5		-
			I2S3	1.5		-
t _{h(SD_SR)} ⁽¹⁾⁽²⁾		Slave receiver	I2S2	1.5		-
			I2S3	1.5		-
t _{v(SD_ST)} ⁽¹⁾⁽²⁾	Data output effective time	Slave transmitter (after enable edge)	I2S2	-		14
			I2S3	-	16.5	
t _{h(SD_ST)} ⁽¹⁾	Data output holding time	Slave generator (after enable edge)	I2S2	3.5	-	
			I2S3	4.5	-	
t _{v(SD_MT)} ⁽¹⁾⁽²⁾	Data output effective time	Master generator (after enable edge)	I2S2	-	6.5	
			I2S3	-	6	
t _{h(SD_MT)} ⁽¹⁾	Data output holding time	Master generator (after enable edge)	I2S2	-0.5	-	
			I2S3	-0.5	-	

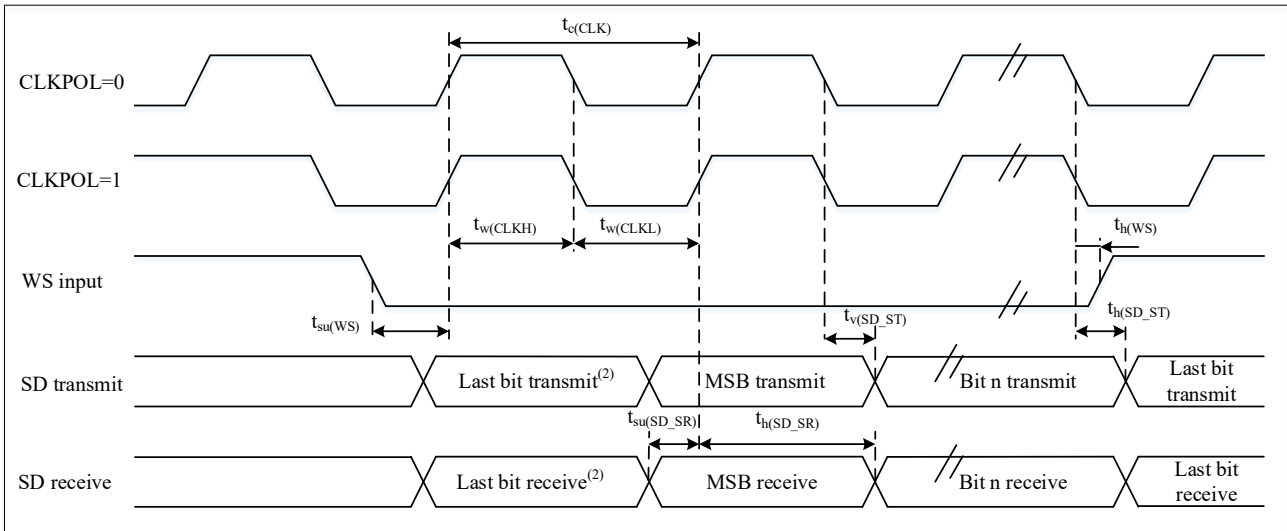
Notes:

⁽¹⁾Guaranteed by design, not tested in production.

⁽²⁾Depends on f_{PCLK}. For example, if f_{PCLK}=8MHz, then T_{PCLK}=1/f_{PCLK} =125ns.

⁽³⁾Audio signal sampling frequency.

Figure 4-16 I²S Slave Mode Timing Diagram (Philips Protocol)⁽¹⁾

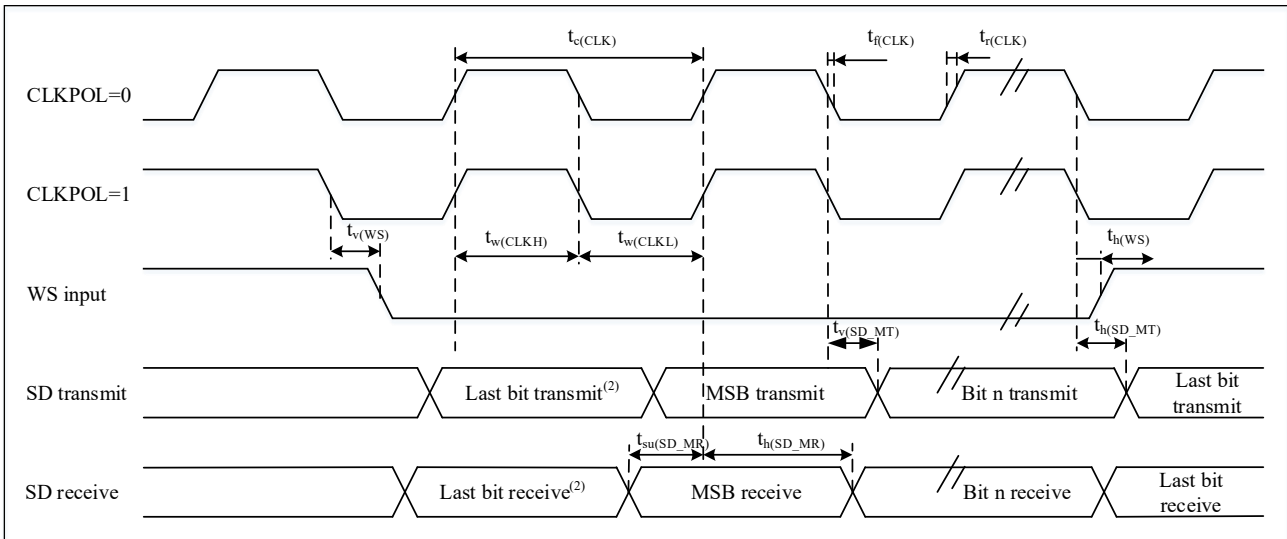


Notes:

⁽¹⁾The measuring points is set at 0.3V_{DD} and 0.7V_{DD}.

⁽²⁾Transmit/receive of the last byte. There is no transmit/receive of this least significant bit before the first byte.

Figure 4-17 I²S Master Mode Timing Diagram (Philips Protocol)⁽¹⁾



Notes:

⁽¹⁾The measuring points is set at 0.3V_{DD} and 0.7V_{DD}.

⁽²⁾Transmit/receive of the last byte. There is no transmit/receive of this last bit before the first byte.

4.3.17 QSPI Characteristics

Table 4-37 Characteristics Of QSPI In SDR Mode

Symbol	Parameter	Min	Max(105 °C)	Unit
f _{CK} 1/t _(CK)	QSPI clock frequency	-	36	MHz
t _w (CKH)	SCK high and low time	t _(CK) /2-2	t _(CK) /2	ns
t _w (CKL)		t _(CK) /2	t _(CK) /2+2	ns
t _s (IN)	Enter data setup time.	4.5	-	ns
t _h (IN)	Enter the data retention time	4	-	ns
t _v (OUT)	Effective time of output data	-	5.5	ns
t _h (OUT)	Output data retention time	-0.15	-	ns

Figure 4-18 Timing Of QSPI In SDR Mode

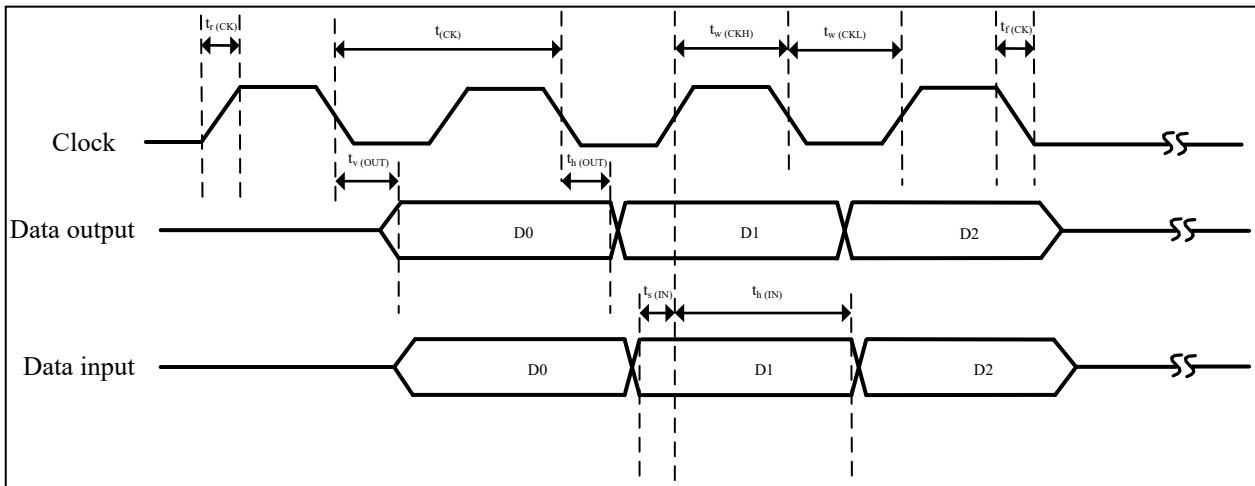
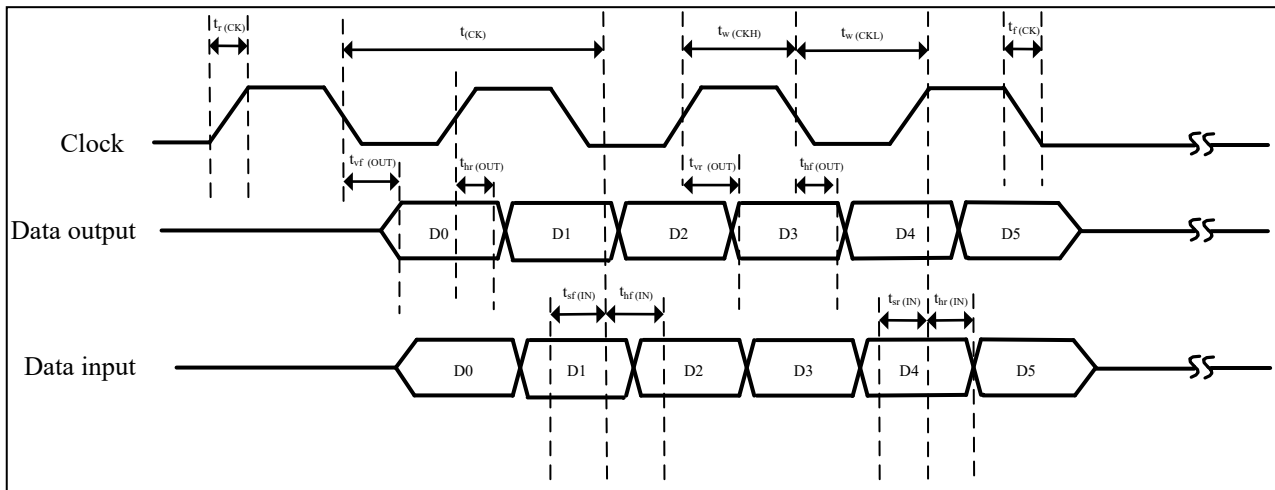


Table 4-38 Characteristics Of QSPI In DDR Mode

Symbol	Parameter	Min	Max(105 °C)	Unit
f_{CK} $1/t_{(CK)}$	QSPI clock frequency	-	36	MHz
$t_{w(CKH)}$	SCK high and low time	$t_{(CK)}/2-2$	$t_{(CK)}/2$	ns
$t_{w(CKL)}$		$t_{(CK)}/2$	$t_{(CK)}/2+2$	ns
$t_{sf(IN)}$; $t_{sr(IN)}$	Enter data setup time.	4.5	-	ns
$t_{hf(IN)}$; $t_{hr(IN)}$	Enter the data retention time	4.5	-	ns
$t_{vf(OUT)}$; $t_{vr(OUT)}$	Effective time of output data	-	12	ns
$t_{hf(OUT)}$; $t_{hr(OUT)}$	Output data retention time	6	-	ns

Figure 4-19 Timing Of QSPI In DDR Mode



4.3.18 SD/SDIO Master Interface Characteristics

Unless otherwise specified, the parameters listed in Table 4-39 are measured using ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage in accordance with the conditions in Table 4-3.

For details on the characteristics of the I/O alternate function pins (D[7:0], CMD, CK), see Section 0.

Figure 4-20 SDIO High-Speed Mode

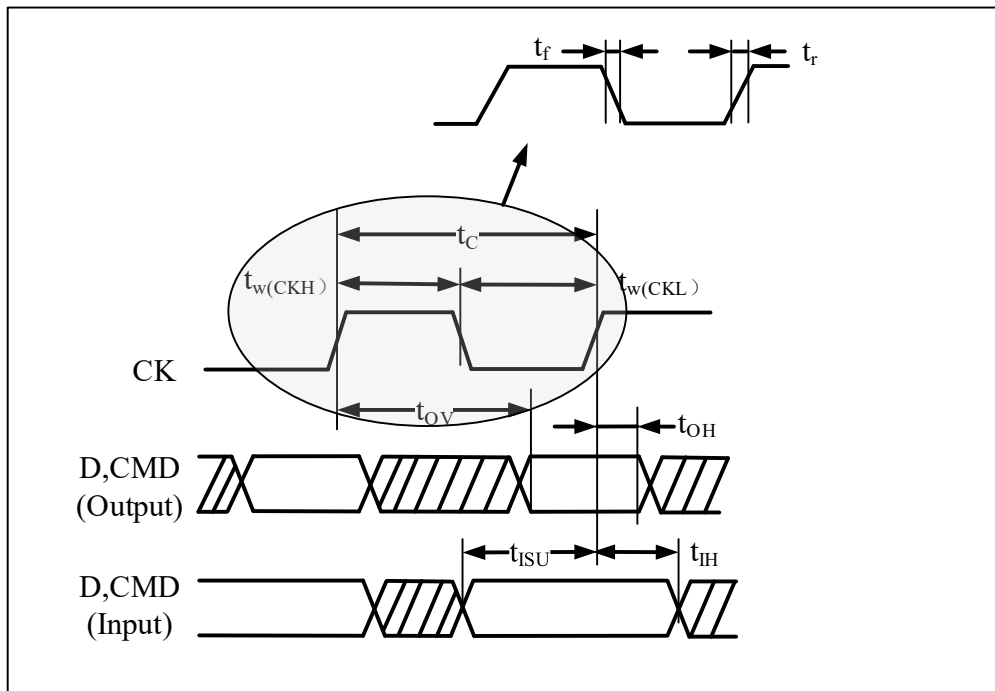


Figure 4-21 SD Default Mode

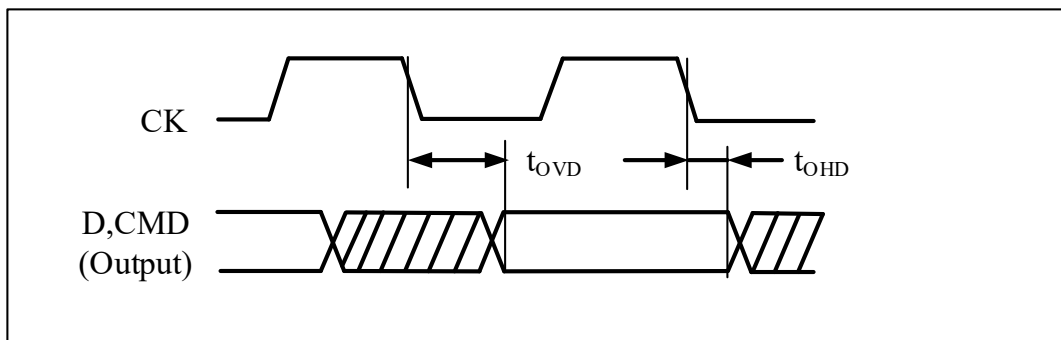


Table 4-39 SD/MMC Interface Features

Symbol	Parameter	Condition	Min	Max(105 °C)	Unit
f_{PP}	Clock frequency in data transmission mode	$CL \leq 30pF$	0	48	MHz
$t_{w(CKL)}$	Clock low time, $f_{PP} = 16$ MHz	$CL \leq 30pF$	32	-	ns
$t_{w(CKH)}$	Clock high time	$CL \leq 30pF$	30	-	
t_r	Clock rising time	$CL \leq 30pF$	-	6	
t_f	Clock falling time	$CL \leq 30pF$	-	6	
CMD, D input (refer to CK)					
t_{ISU}	Input set up time.	$CL \leq 30pF$	1	-	ns
t_{IH}	Input holding time	$CL \leq 30pF$	1	-	
CMD, D output in MMC and SD high-speed mode (refer to CK)					
t_{OV}	Output valid time	$CL \leq 30pF$	-	6	ns
t_{OH}	Output holding time	$CL \leq 30pF$	0	-	
CMD, D output in SD default mode (refer to CK)					
t_{OVD}	Output valid default time	$CL \leq 30pF$	-	8	ns
t_{OHD}	Output hold default time.	$CL \leq 30pF$	-1	-	

4.3.19 Controller Area Network (CAN) Interface Characteristics

See Section 0 for details on the features of the input/output multiplexing function pins (CAN_TX and CAN_RX).

4.3.20 12-bit Analog-to-Digital Converter (ADC) Electrical Parameters

Unless otherwise specified, the parameters in Table 4-40 are measured using ambient temperature, f_{HCLK} frequency, and V_{DDA} supply voltage in accordance with the conditions in Table 4-3.

Note : It is recommended to perform a calibration at each power up.

Table 4-40 ADC Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{DDA}	supply voltage	-	1.8	-	3.6	V
V_{REF+}	Positive reference voltage	-	1.8	-	V_{DDA}	
f_{ADC}	ADC clock frequency	-	-	-	80	MHz
$f_s^{(2)}$	sampling rate	$1.8V \leq V_{DD} \leq 3.6V$, Resolution 12bit	0.01 ⁽²⁾	-	4.7 ⁽¹⁾	MHz
		$1.8V \leq V_{DD} \leq 3.6V$, Resolution 10bit	0.012 ⁽²⁾	-	6.1 ⁽¹⁾	MHz
		$1.8V \leq V_{DD} \leq 3.6V$, Resolution 8bit	0.014 ⁽²⁾	-	7.3 ⁽¹⁾	MHz
		$1.8V \leq V_{DD} \leq 3.6V$, Resolution 6bit	0.0175 ⁽²⁾	-	8.9 ⁽¹⁾	MHz
V_{AIN}	Conversion voltage range ⁽³⁾	-	0(V_{SSA} or V_{REF-} Connect to ground)	-	V_{REF+}	V
$R_{ADC}^{(2)}$	Sampling switch resistance	Fast channel, Under the condition of 3.6V voltage	-	-	137.6	Ω
		Slow channel, Under the condition of 3.6V voltage	-	-	147	Ω
$C_{ADC}^{(2)}$	Internal sample and hold capacitor	-	-	5	-	pF
SNDR	Signal noise distortion ration	-	-	65	-	dBFS
T_{cal}	Calibration time	-	82			$1/f_{ADC}$
$T_s^{(2)}$	Sampling cycles	Resolution 6/8/10/12-bit	1.5	-	601.5	$1/f_{ADC}$
$t_{STAB}^{(2)}$	Power-up time	-	6	10	20	μs
$t_{CONV}^{(2)}$	Total conversion time of (including sampling time)	-	8~614 (sampling t_s + gradually approaching 6.5/8.5/10.5/12.5)			$1/f_{ADC}$

Notes:

⁽¹⁾ Only fast channel support, $f_{ADC} = 80$ MHz.

⁽²⁾ Guaranteed by design, not tested in production.

⁽³⁾ According to different packages, V_{REF+} can be internally connected to V_{IN} and V_{REF-} can be internally connected to V_{IN} .

Formula 1: maximum R_{AIN} formula

$$R_{AIN} < \frac{T_s}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$$

The above formula (Formula 1) is used to determine the maximum external impedance so that the error can be less than 1/4 LSB. Where N=12 (representing 12-bit resolution).

Table 4-41 ADC Sampling Time^{(1) (2)}

Input	Resolution	Rin(k Ω)	Typical value of minimum sampling time (ns)	Input	Resolution	Rin(k Ω)	Typical value of minimum sampling time (ns)
Fast channel	12-bit	0.06	37	Slow channel	12-bit	0.05	53

Input	Resolution	Rin(kΩ)	Typical value of minimum sampling time (ns)	Input	Resolution	Rin(kΩ)	Typical value of minimum sampling time (ns)
		0.36	45			0.35	73
		0.86	79			0.85	103
		4.86	300			4.85	345
		9.86	576			9.85	651
		19.86	1131			19.85	1257
		49.86	2776			49.85	3051
		99.86	5475			99.85	5982
Fast channel	10-bit	0.06	25	Slow channel	10-bit	0.05	46
		0.36	39			0.35	61
		0.86	64			0.85	88
		4.86	250			4.85	357
		9.86	478			9.85	540
		19.86	935			19.85	1040
		49.86	2294			49.85	2526
99.86	4532	99.85	4963				
Fast channel	8-bit	0.06	22	Slow channel	8-bit	0.05	39
		0.36	33			0.35	50
		0.86	52			0.85	71
		4.86	202			4.85	234
		9.86	391			9.85	457
		19.86	800			19.85	1012
		49.86	1838			49.85	2027
99.86	3632	99.85	3984				
Fast channel	6-bit	0.06	19	Slow channel	6-bit	0.05	32
		0.36	27			0.35	40
		0.86	41			0.85	56
		4.86	153			4.85	177
		9.86	292			9.85	330
		19.86	569			19.85	642
		49.86	1435			49.85	1666
99.86	3001	99.85	3919				

Notes:

⁽¹⁾Guaranteed by design, not tested in production.

⁽²⁾Typical values are measured at T_A=25°C and V_{DD}= 3.3V.

Table 4-42 ADC Accuracy-Limited Test Conditions⁽¹⁾⁽²⁾

Symbol	Parameter	Test condition	Typ	Max	Unit
ET	composite error	f _{HCLK} = 72 MHz, f _{ADC} = 72 MHz, sample rate=1.75Msps, V _D = 3.3V, T _A = 25 °C The measurement is performed after ADC calibration. V _{REF±} = V _D	±1.3	±5	LSB
EO	offset error		±1	±2	
ED	Differential linear error		±0.7	±1	
EL	Integral linear error		±0.8	±2	

Notes:

- (1) The DC accuracy values of the ADC are measured after internal calibration.
- (2) ADC Accuracy vs. Reverse Injection Current: Injecting reverse current on any standard analog input pin needs to be avoided, as this will significantly degrade the accuracy of an ongoing conversion on another analog input pin. It is recommended to add a Schottky diode (between the pin and ground) to standard analog pins where reverse injection current may occur.
- (3) Guaranteed by comprehensive evaluation, not tested in production.

Figure 4-22 ADC Precision Characteristics

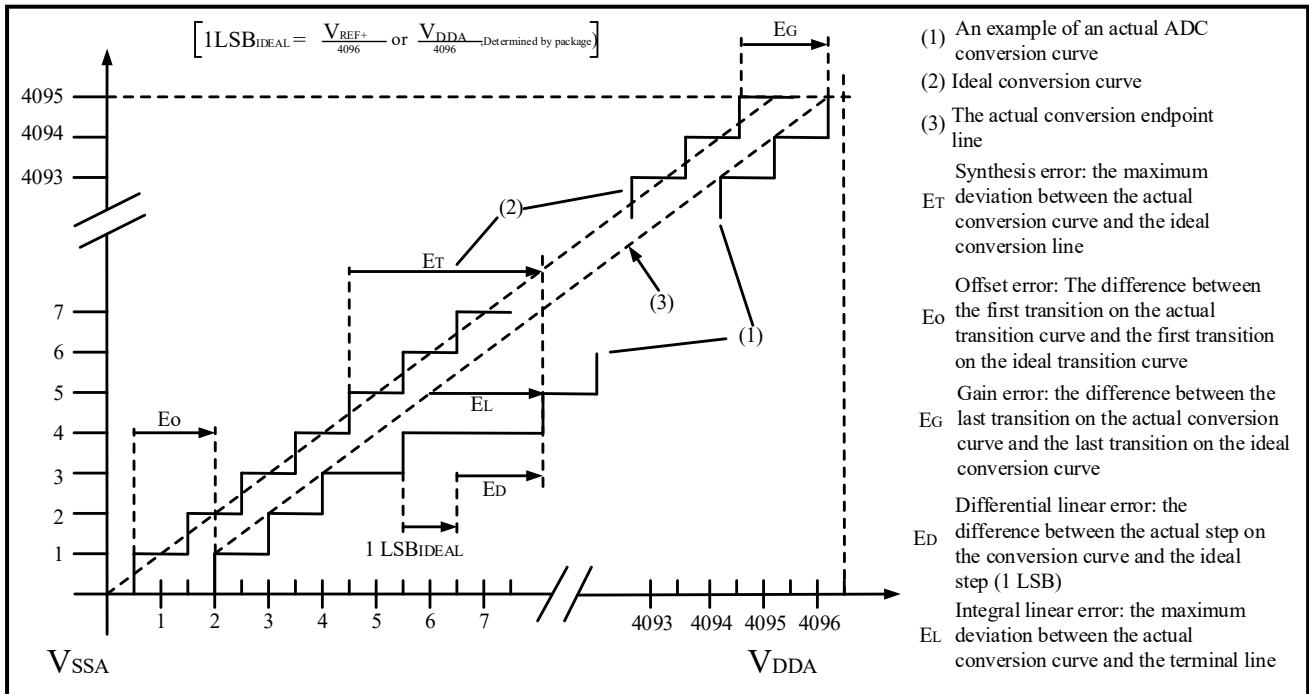
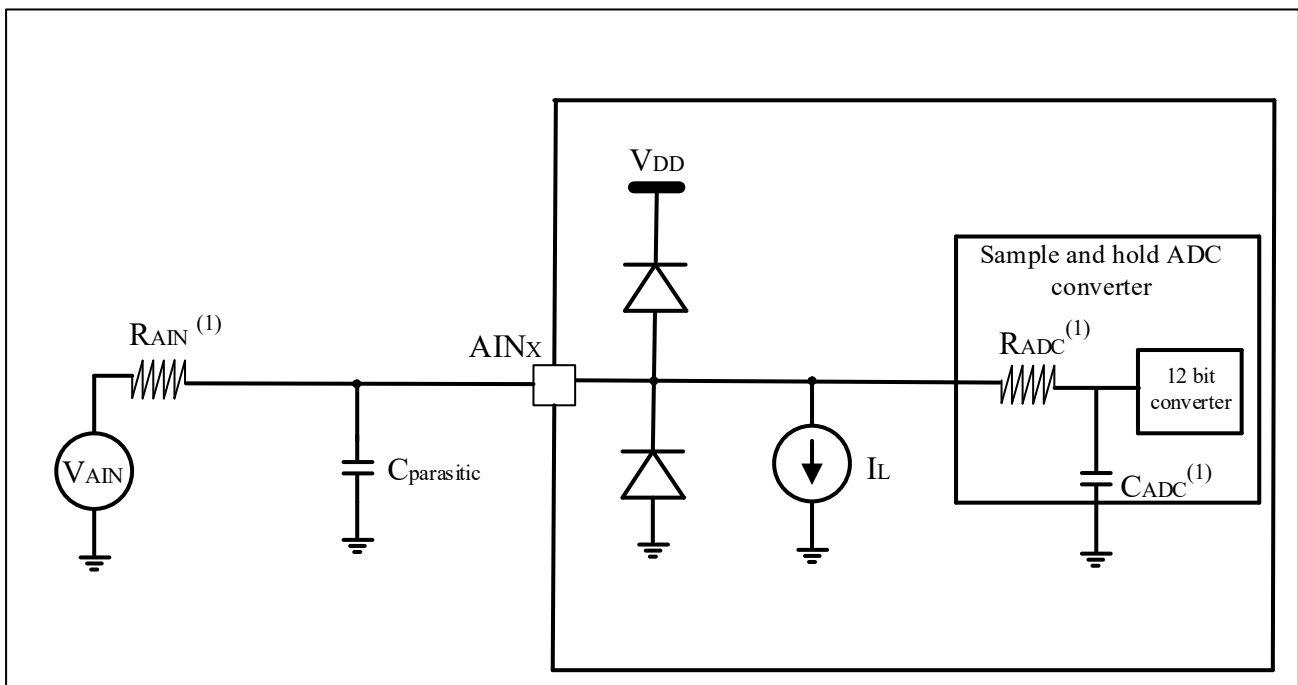


Figure 4-23 Typical Connection Diagram Using ADC



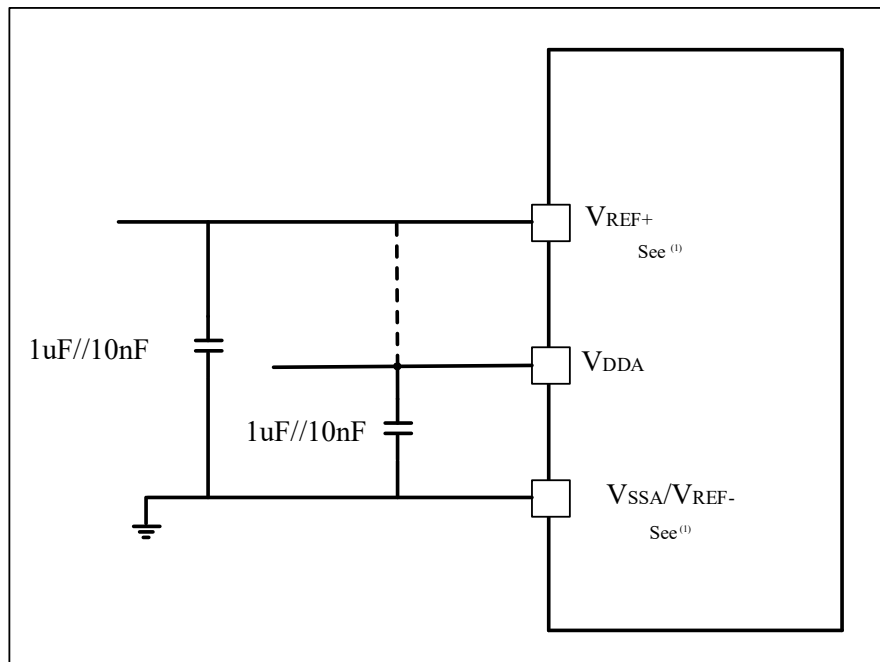
Note: (1)On the numerical values of R_{AIN} , R_{ADC} and C_{ADC} , see Table 4-40.

Caution: $C_{parasitic}$ represents parasitic capacitance on PCB (related to soldering and PCB layout quality) and pads (approximately 7pF). A larger $C_{parasitic}$ value would reduce the accuracy of conversion, and the solution was to reduce f_{ADC} .

PCB design suggestions

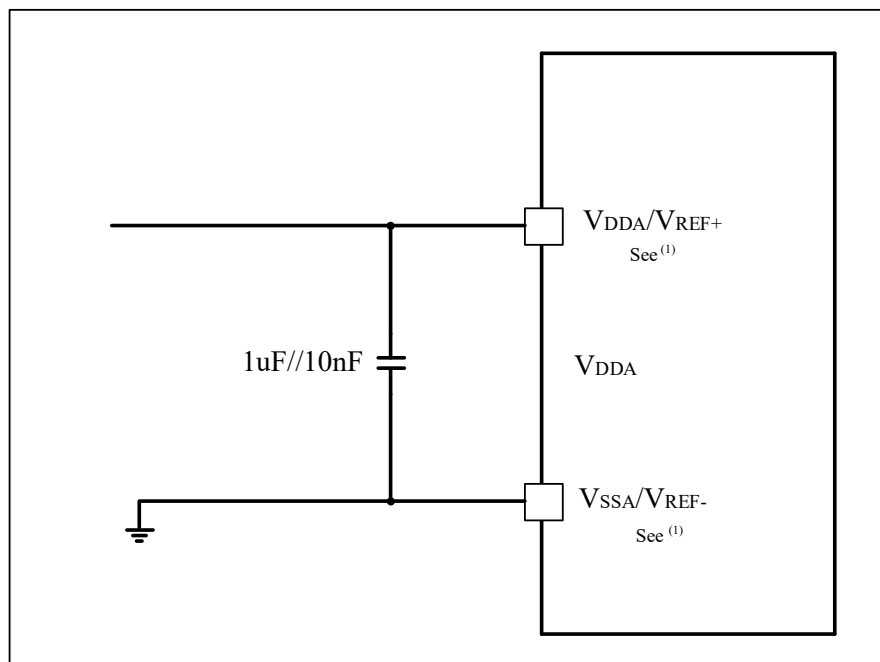
Depending on whether V_{REF+} is connected to V_{DDA} , the decoupling of the power supply must be connected as shown in Figure 4-24 or Figure 4-25. The 10nF capacitors in the picture must be ceramic capacitors (good quality), and they should be as close to the MCU chip as possible.

Figure 4-24 Decoupling Circuit of Power Supply and Reference Power Supply (V_{REF+} Is Not Connected To V_{DDA})



Notes: (1) V_{REF+} and V_{REF-} inputs only products with more than 100 pins.

Figure 4-25 Decoupling Circuit of Power Supply and Reference Power Supply (V_{REF+} Is Connected With V_{DDA})



Note: (1) V_{REF+} and V_{REF-} inputs only products with 100 pins.

4.3.21 12-bit Digital-to-Analog Converter (DAC) Electrical Parameters

Unless otherwise specified, the parameters in Table 4-43 are measured using ambient temperature, f_{HCLK} frequency, and V_{DDA} supply voltage in accordance with the conditions in Table 4-3.

Table 4-43 DAC Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Annotate
V _{DDA}	Analog supply voltage	2.4	-	3.6	V	-
V _{DDD}	Digital supply voltage	1.0	1.1	1.2	V	-
V _{REF+}	Reference voltage	2.4	-	3.6	V	V _{REF+} must always be lower than V _{DDA}
V _{SSA}	Ground wire	0	-	0	V	-
R _L	Load resistance when buffer is open	5	-	-	KΩ	The minimum load resistance between DAC_OUT and V _{SSA}
C _L	Load Capacitance	-	-	50	pF	Maximum capacitance on DAC_OUT pin
DAC_OUT _{minimum}	DAC_OUT voltage when buffer is open	0.2	-	-	V	The maximum DAC output span is given. When V _{REF+} =3.6V corresponds to a 12-bit input value 0x0E0~0xF1C, When V _{REF+} =2.4V corresponds to a 12-bit input value 0x155~0xEAB.
DAC_OUT _{maximum}	DAC_OUT voltage when buffer is open	-	-	V _{REF+} - 0.2	V	
I _{DD}	In static mode (STANDBY mode), DAC DC consumption (V _{DDD} +V _{DDA} +V _{REF+})	-	425	600	μA	No load, enter the median 0x800
		-	500	700		No load, enter the maximum value when V _{REF+} = 3.6V.
I _{DDQ}	DC consumption of DAC in power-down mode (V _{DDD} +V _{DDA} +V _{REF+})	-	5	350	nA	non-loaded
	DC consumption of DAC in power-down mode (V _{DDA} +V _{REF+})	-	5	200		
DNL	Nonlinear distortion (deviation between two consecutive codes)	-	±0.5	-	LSB	DAC is configured with 10 bits (B1=B0=0 at all times)
		-	±2	-	LSB	DAC is configured with 12 bits
INL	Non-linearity accumulation (deviation between the measured value at code I and the line between code 0 and code 4095)	-	±6	-	LSB	DAC is configured as 12-bit
offset	Offset error (the deviation between the measured value of code 0x800 and the ideal value V _{REF+} /2)	-	±10	-	mV	DAC is configured as 12-bit
		-	±12	-	LSB	With V _{REF+} =3.6V, the DAC is configured with 12 bits.
Gain error	Gain error	-	±0.5	-	%	DAC is configured as 12-bit
Amplifier gain	Gain of open-loop amplifier	80	85	-	dB	The load of 5k (maximum load) , input medium value is 0x800
t _{SETTLING}	Setting time (full range: 10-bit input code changes from minimum value to maximum value, and DAC_OUT reaches ±1 LSB of its final value)	-	5	7	μs	C _{LOAD} ≤ 50pF R _{LOAD} ≥ 5kΩ
Update rate	When the input code changes slightly (from the value i to i+1LSB), the maximum frequency of the correct DAC_OUT is obtained.	-	-	1	MS/s	C _{LOAD} ≤ 50pF R _{LOAD} ≥ 5kΩ
t _{WAKEUP}	Time to wake up from off state (setting the CHxEN bit in DAC control register)	-	6.5	10	μs	C _{LOAD} ≤ 50pF, R _{LOAD} ≥ 5kΩ The input code is between the minimum and maximum possible values.
PSRR+	Power supply rejection ratio (relative to V _{DD33A}) (static DC measurement)	-	-67	-40	dB	Without R _{LOAD} , C _{LOAD} ≤ 50pF

4.3.22 Operational Amplifier (OPAMP) Electrical Parameters

Unless otherwise specified, the parameters in Table 4-44 are measured using ambient temperature, f_{HCLK} frequency, and V_{DDA} supply voltage in accordance with the conditions in Table 4-3.

Table 4-44 OPAMP Characteristics⁽¹⁾

Symbol	Parameter	Condition	Min	Typ	Max(105 °C)	Unit
V_{DDA}	Analog supply voltage	-	1.8	-	3.6	V
CMIR	Common-mode voltage input range	-	0	-	V_{DDA}	V
$V_{IOFFSET}$	Input offset voltage	-	-3.5	+/-1	3.5	mV
$\Delta V_{IOFFSET}$	Input offset voltage temperature drift	-	-	10	-	$\mu V/^{\circ}C$
I_{LOAD}	drive current	-	-	0.5	-	mA
I_{DDA}	Operational amplifier current consumption	No load, quiescent mode	-	-	1.5	mA
TS_OPAMP_VOUT	ADC sampling time as output of operational amplifier	-	400	-	-	ns
CMMR	common mode rejection ratio	-	-	84	-	dB
PSRR	Power supply rejection ratio	-	-	100	-	dB
GBW	Gain bandwidth	-	-	4	-	MHz
SR	Slew rate	-	-	1.5	-	V/ μs
RLOAD	Minimum impedance load	-	4	-	-	K Ω
CLOAD	Maximum capacitive reactance load	-	-	-	50	pF
TSTARTUP	Setup time	CLOAD \leq 50 pF, RLOAD \geq 4 k Ω , Follower configuration	-	3	-	μs
PGA Gain error	Programmable gain error	Input signal amplitude > 10	-	± 2.5	-	%
PGA BW	PGA bandwidth for different non inverting gain	PGA Gain = 2, Cload = 50pF, Rload = 4 K Ω	-	2	-	MHz
		PGA Gain = 4, Cload = 50pF, Rload = 5 K Ω	-	1	-	
		PGA Gain = 16, Cload = 50pF, Rload = 6 K Ω	-	0.25	-	
		PGA Gain = 32, Cload = 50pF, Rload = 7 K Ω	-	0.125	-	
en	Voltage noise density	@ 1KHz, Output loaded with 4 K Ω	-	111	-	nV/ \sqrt{Hz}
		@ 10KHz, Output loaded with 4 K Ω	-	43.9	-	

Note: ⁽¹⁾Guaranteed by design, not tested in production.

4.3.23 Comparator (COMP) Electrical Parameters

Unless otherwise specified, the parameters in Table 4-45 are measured using ambient temperature, f_{HCLK} frequency, and V_{DDA} supply voltage in accordance with the conditions in Table 4-3.

Table 4-45 COMP Characteristic

Symbol	Parameter	Condition	Min	Typ	Max(105 °C)	Unit	
V _{DDA}	Analog supply voltage	-	1.8	-	3.6	V	
V _{IN}	Input voltage range	-	0	-	V _{DDA}		
t _{START} ⁽¹⁾	Comparator startup setup time	-	-	10	-	μs	
t _D	Propagation delay for 200 mV step with 100 mV overdrive	-	-	70	-	ns	
V _{OFFSET}	Comparator input offset error	Full common mode range	-	±10	-	mV	
V _{hys}	Compare hysteresis voltage	No hysteresis	-	0	-	mV	
		Low hysteresis	-	20	-		
		Medium hysteresis	-	30	-		
		High hysteresis	-	40	-		
I _{DDA}	Comparator current consumption	High speed mode	Static	-	50	-	μA
			With 50 kHz ±100 mV overdrive square signal	-	60	-	

Note: ⁽¹⁾Guaranteed by design, not tested in production.

4.3.24 Temperature Sensor (TS) Characteristics

Unless otherwise specified, the parameters in Table 4-46 are measured using ambient temperature, f_{HCLK} frequency, and V_{DDA} supply voltage in accordance with the conditions in Table 4-3.

Table 4-46 Temperature Sensor Characteristics

Symbol	Parameter	Min	Typ	Max(105 °C)	Unit
T _L ⁽¹⁾	Linearity of V _{SENSE} with respect to temperature	-	±1	±4	°C
Avg_Slope ⁽¹⁾	Average slope	-	-4.1	-	mV/°C
V ₃₀ ⁽¹⁾	Voltage at 30°C	-	1.32	-	V
t _{START} ⁽¹⁾	setting time	-	10	-	μs
T _{S_temp} ⁽²⁾⁽³⁾	When reading temperature, ADC sampling time	8.3	-	-	μs

Notes:

⁽¹⁾Guaranteed by comprehensive evaluation, not tested in production.

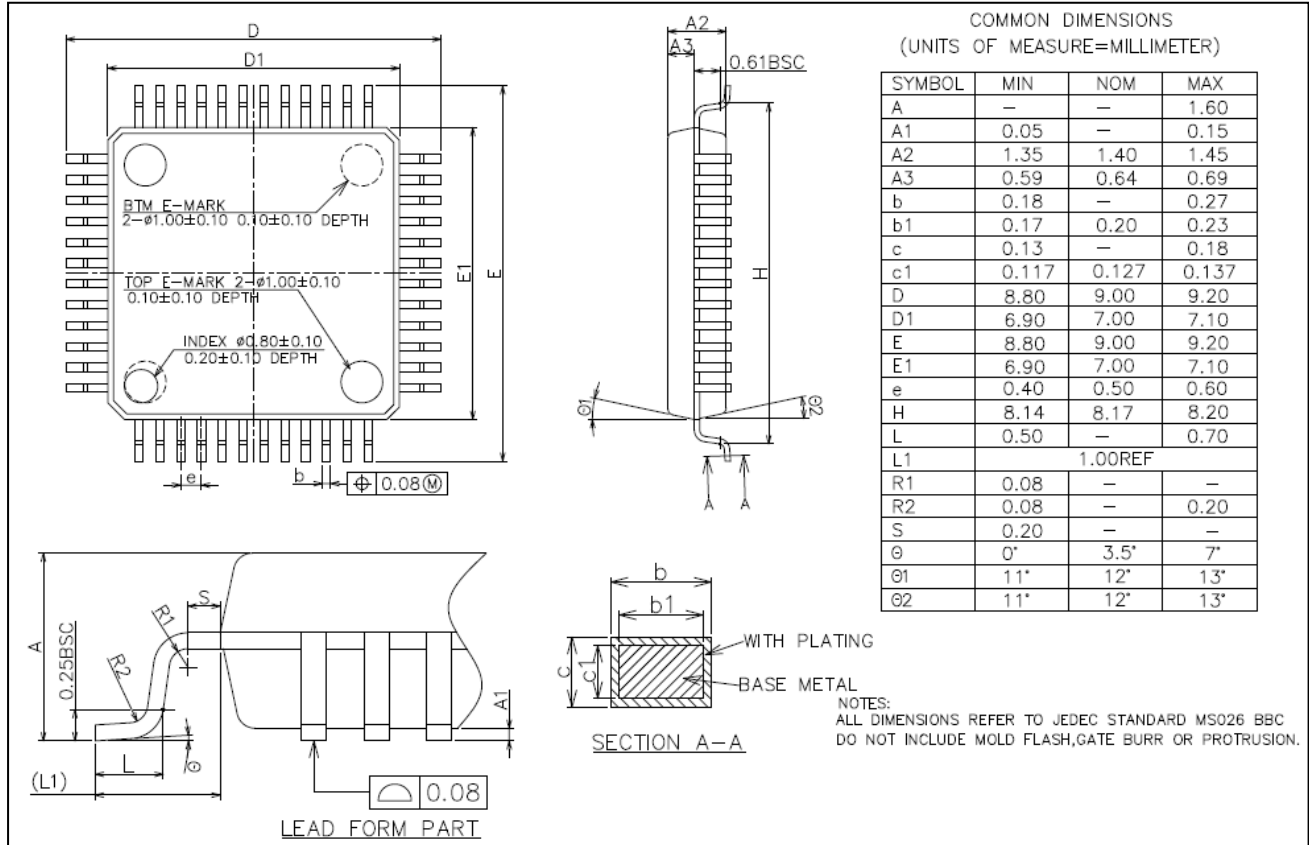
⁽²⁾Guaranteed by design, not tested in production.

⁽³⁾The shortest sampling time of can be determined by the application through multiple cycles.

5. Packages

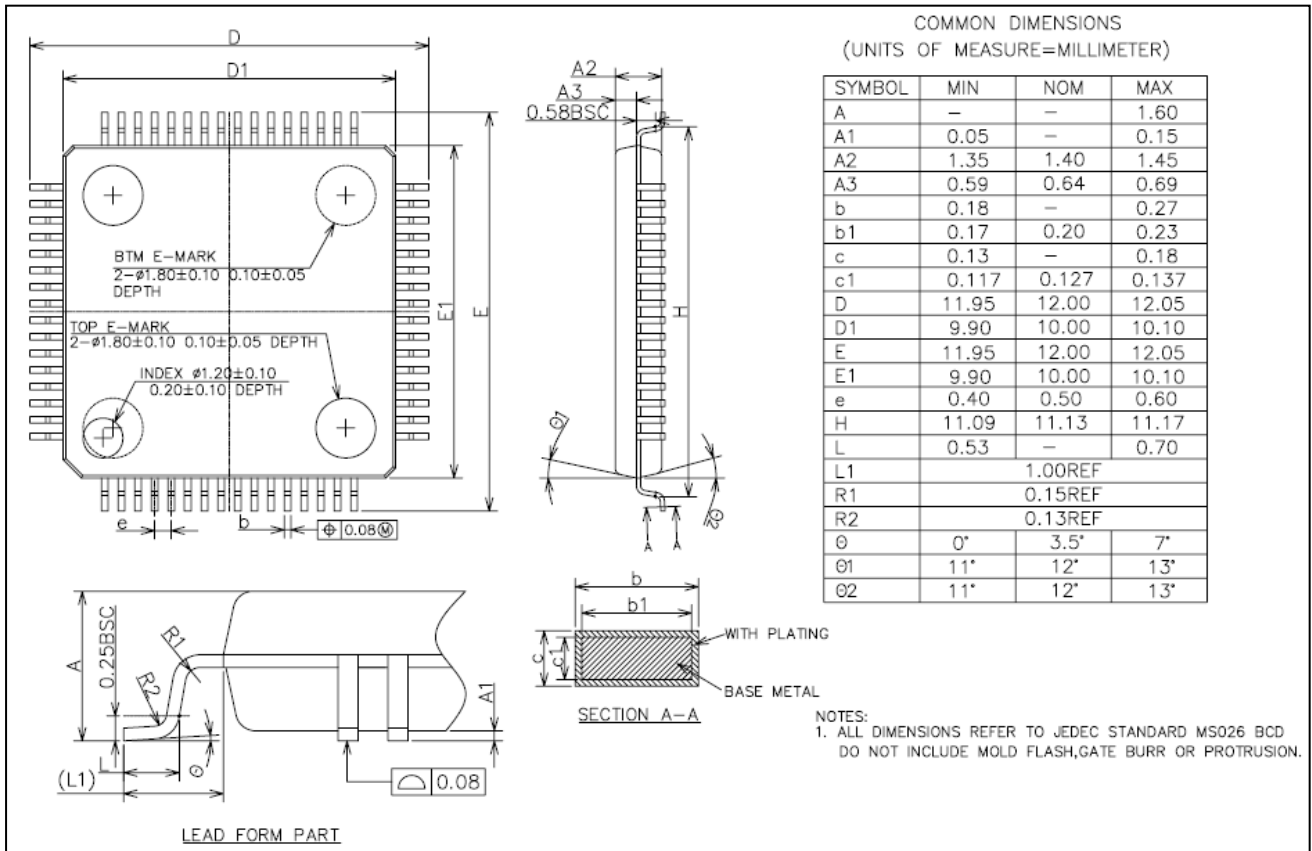
5.1 LQFP48(7mm x 7mm)

Figure 5-1 LQFP48 Package Dimensions



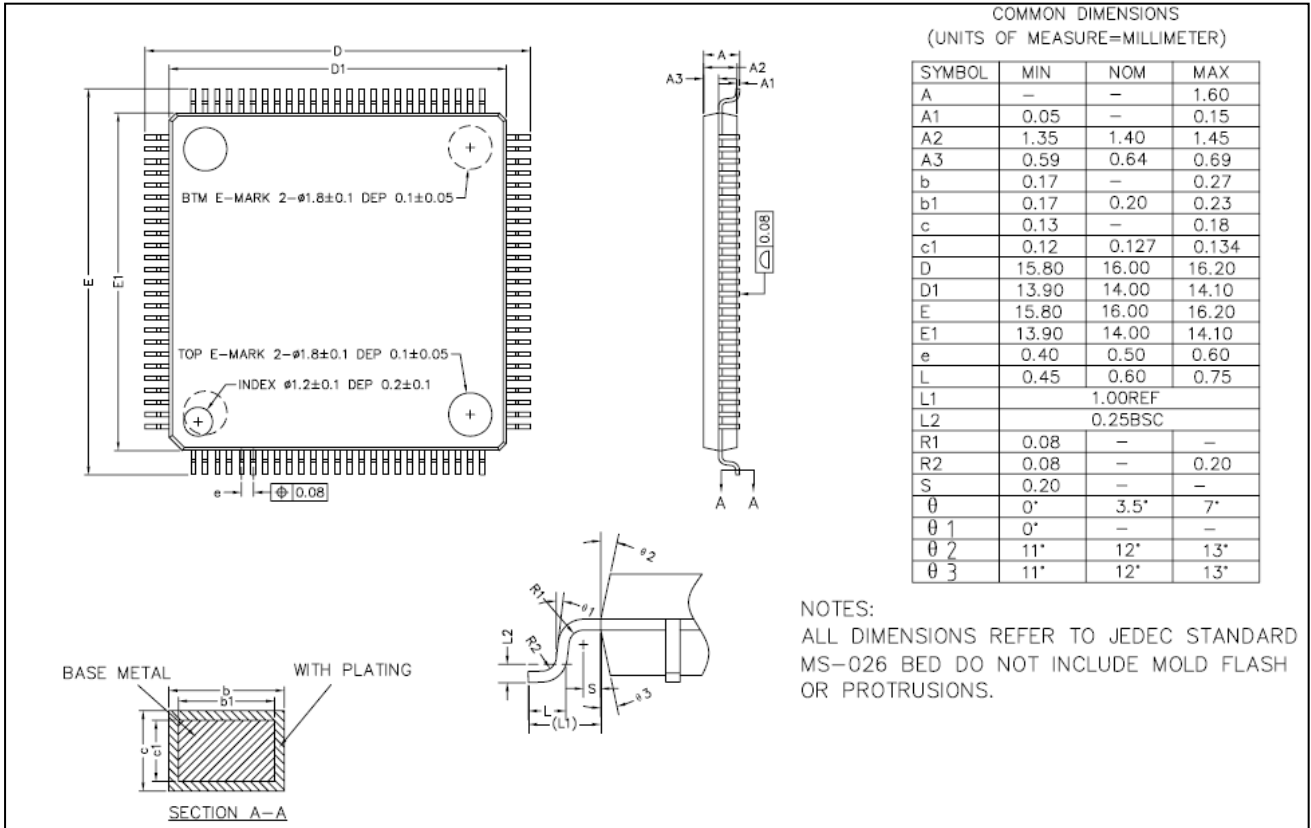
5.2 LQFP64(10mm x 10mm)

Figure 5-2 LQFP64 Package Dimensions



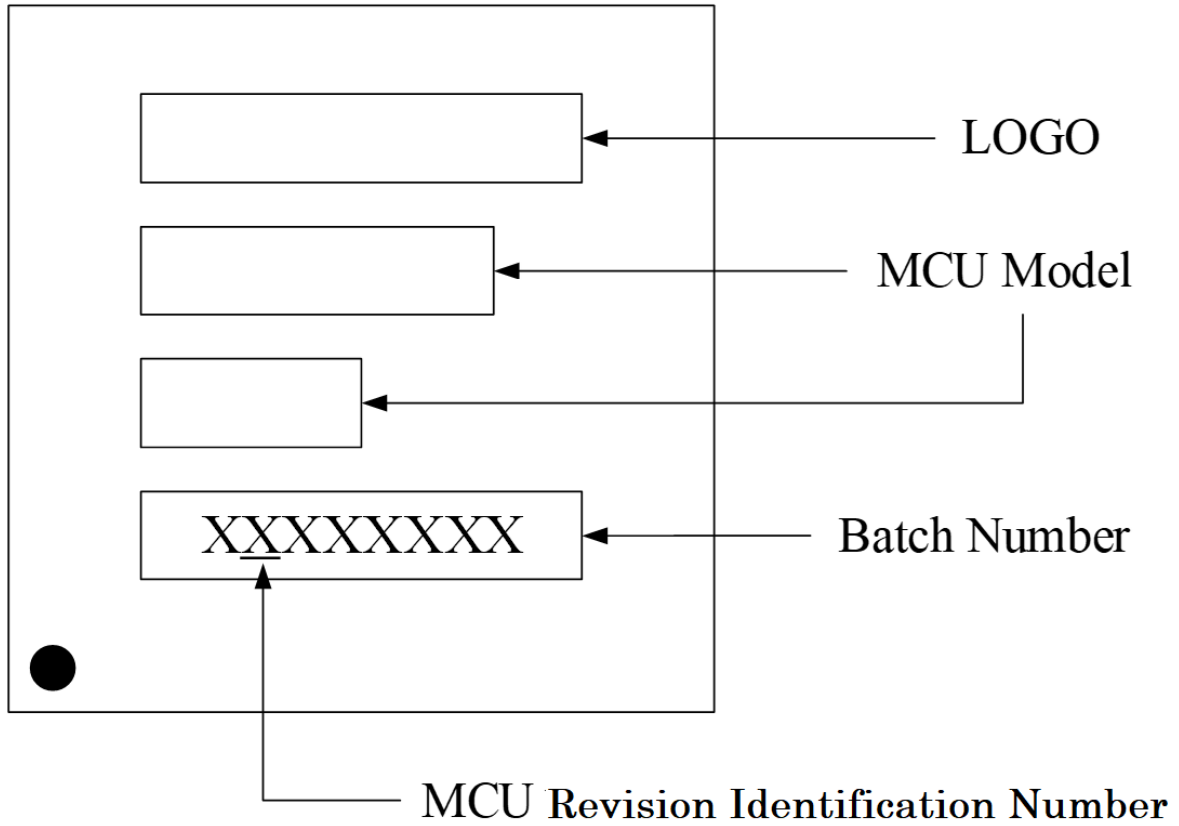
5.3 LQFP100(14mm x 14mm)

Figure 5-3 LQFP100 Package Dimensions



5.4 Marking Information

Figure 5-4 Marking Information



6. Version History

Version	Date	Changes
V1.0.0	2023.09.18	Initial version

7. Disclaimer

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