N32A455xxL7 series Product Brief

N32A455xxL7 series uses 32-bit ARM Cortex-M4F core, operating frequency up to 144MHz, supporting floating-point unit and DSP instructions. The devices integrates up to 512KB of embedded flash and 144KB of SRAM. The series features rich of high-performance interfaces, including four built-in 12bit 4.7Msps ADCs, four independent rail-to-rail operational amplifiers, seven high-speed comparators, two 1Msps 12-bit DACs, multi-channel U(S)ART, I2C, SPI, QSPI, CAN, SDIO and other communication interfaces, allowing a built-in hardware acceleration engine for cryptographic algorithms.

Key features

- **CPU Core**
  - 32-bit ARM Cortex-M4F core with FPU, supporting single-cycle multiplication and hardware division, DSP instructions and MPU
  - Built-in 8KB instruction Cache, supporting 0-wait-state execution from Flash memory
  - Frequency up to 144MHz with 180DMIPS
- **Memories**
  - Up to 512KByte of embedded Flash with ECC
    - Supports encryption, multi-user partition and data protection
    - 100,000 erase/write cycles, and 10 years data retention
  - Up to 144KByte of SRAM(including 16KByte Retention RAM) with hardware parity check
- **High-Performance Analog Interfaces**
  - 4x 12bit 5Msps ADCs
    - Multiple precision configuration
    - Up to 38 external single-ended input channels
    - Sampling rate up to 8.9Msps in 6-bit mode
    - Supports differential mode
  - 4x rail-to-rail operational amplifiers with built-in up to 32 times programmable gain amplifier(PGA)
  - 7x high-speed analog comparators with internal 64-level adjustable comparison reference
  - 2x 12-bit 1Msps DACs
  - External independent reference voltage source
  - Analog voltage operation from 1.8~3.6V
- **Clock**
  - 4MHz~32MHz high speed external crystal oscillator
  - 32.768KHz low speed external crystal oscillator

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- High-speed internal RC (HSI) 8MHz
- Low-speed internal RC(LSI) 40KHz
- Built-in high Speed PLL
- Support one clock output, which can be configured as system clock, HSE, HSI or PLL division output

- **Reset**
  - Supports power-on/power-down/external pin reset
  - Supports programmable low voltage detection and reset
  - Support watchdog reset
- **GPIOs**
  - Up to 80 GPIOs.
  - Support multiplexed functions
  - Maximum toggle speed of 50MHz
- **Communication Interfaces**
  - 7x U(S)ART interfaces, with a maximum speed of 4.5 Mbps.
    - 3x USART interfaces (support 1xISO7816, 1xIrDA, LIN).
    - 4x UART interfaces
  - 3x SPI interfaces, the rate is up to 36 MHz, 2 of which support I2S communication
  - 1x QSPI interface with speed up to 144 Mbps
  - 4x I2C interfaces, the rate is up to 1 MHz, which can be configured in master/slave mode and support dual address response in slave mode
  - 2x CAN 2.0A/B bus interfaces
  - 1x SDIO interface, supports SD/SDIO/MMC format
- **DMA Controllers**
  - 2x high-speed DMA controllers
  - Each controller supports 8 channels
  - Channel source address and destination address can be configured arbitrarily
- **Real-Time Clock(RTC)**
  - Supports leap year calendar, alarm events, periodic wake-up
  - Supports internal and external clock calibration
- **Timers**
  - －2x 16bit advanced control timers with maximum control precision of 6.9ns
    - Support input capture, complementary output, quadrature encoding input
    - Each timer has 4 independent channels, with 3 channels support 6 complementary PWM output.

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- 4x 16bit general-purpose timers
  - Support input capture/output comparison/ PWM output
  - Each timer has 4 independent channels
- 2x 16bit basic timers
- 1x 24bit SysTick timer
- 1x 7bit Window Watchdog (WWDG)
- 1x 12bit Independent Watchdog (IWDG)

- **Programming Methods**
  - Supports SWD/JTAG debugging interface
  - Supports UART Bootloader
- **Security Features**
  - Built-in hardware acceleration engine for cryptographic algorithms
  - Supports DES/3DES, AES, SHA1/SHA224/SHA256, SM1, SM3, SM4, SM7 and MD5 algorithms
  - Flash storage encryption, multi-user partition management (MMU)
  - True random number generator(TRNG)
  - CRC16/32 calculation
  - Supports write protection (WRP), multiple read protection (RDP) levels (L0/L1/L2)
  - Supports program encryption download
  - Supports clock failure detection, tamper detection
- **96-bit UID and 128-bit UCID**
- **Operating Conditions**
  - Operating voltage range: 1.8V~3.6V
  - Operating temperature range: -40℃~105℃
  - Certified by AEC-Q100-G2
  - ESD: ±4KV (HBM model), ±1KV (CDM model)
- **Packages**
  - LQFP48(7mm x 7mm)
  - LQFP64(10mm x 10mm)
  - LQFP100(14mm x 14mm)
- **Ordering information**

Reference	Part Number
N32A455xxL7	N32A455CEL7,N32A455REL7, N32A455VEL7

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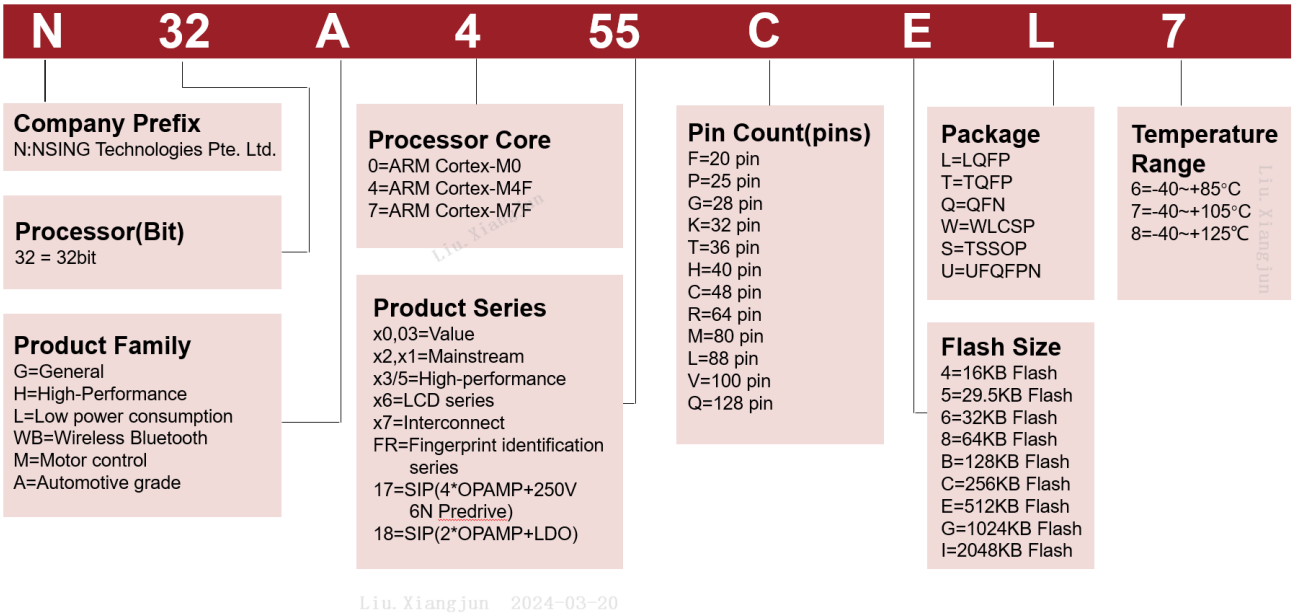
Naming Convention

MCU Part Number Suffixes



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Product Configurations

Device		N32A455CEL7	N32A455REL7	N32A455VEL7
Flash Capacity (KB)		512		
SRAM Capacity (KB)		144		
CPU Frequency		ARM Cortex-M4 @144MHz,180DMIPS		
Operating Conditions		1.8~3.6V/-40~105℃		
Timers	General	4		
	Advanced	2		
	Basic	2		
Communication interface	SPI	3		
	I2S	2		
	QSPI	Only Single Wire	1	
	I2C	3	4	
	USART	3		
	UART	3	4	
	CAN	2		
	SDIO	No	1	
GPIO		37	51	80
DMA		2		
DMA Channels		16Channel		
12bit ADC		4	4	4
ADC channels		16Channel	22Channel	38Channel
12bit DAC		2		
DAC channels		2Channel		
OPA/COMP		4/5	4/7	4/7
Algorithm support		DES/3DES、AES、 SHA1/SHA224/SHA256、SM1、SM3、SM4、SM7、MD5、CRC16/CRC32、TRNG		
Security protection		Read-Write Protection (RDP/WRP), Storage Encryption, Partition Protection, Secure Boot		
Package		LQFP48	LQFP64	LQFP100

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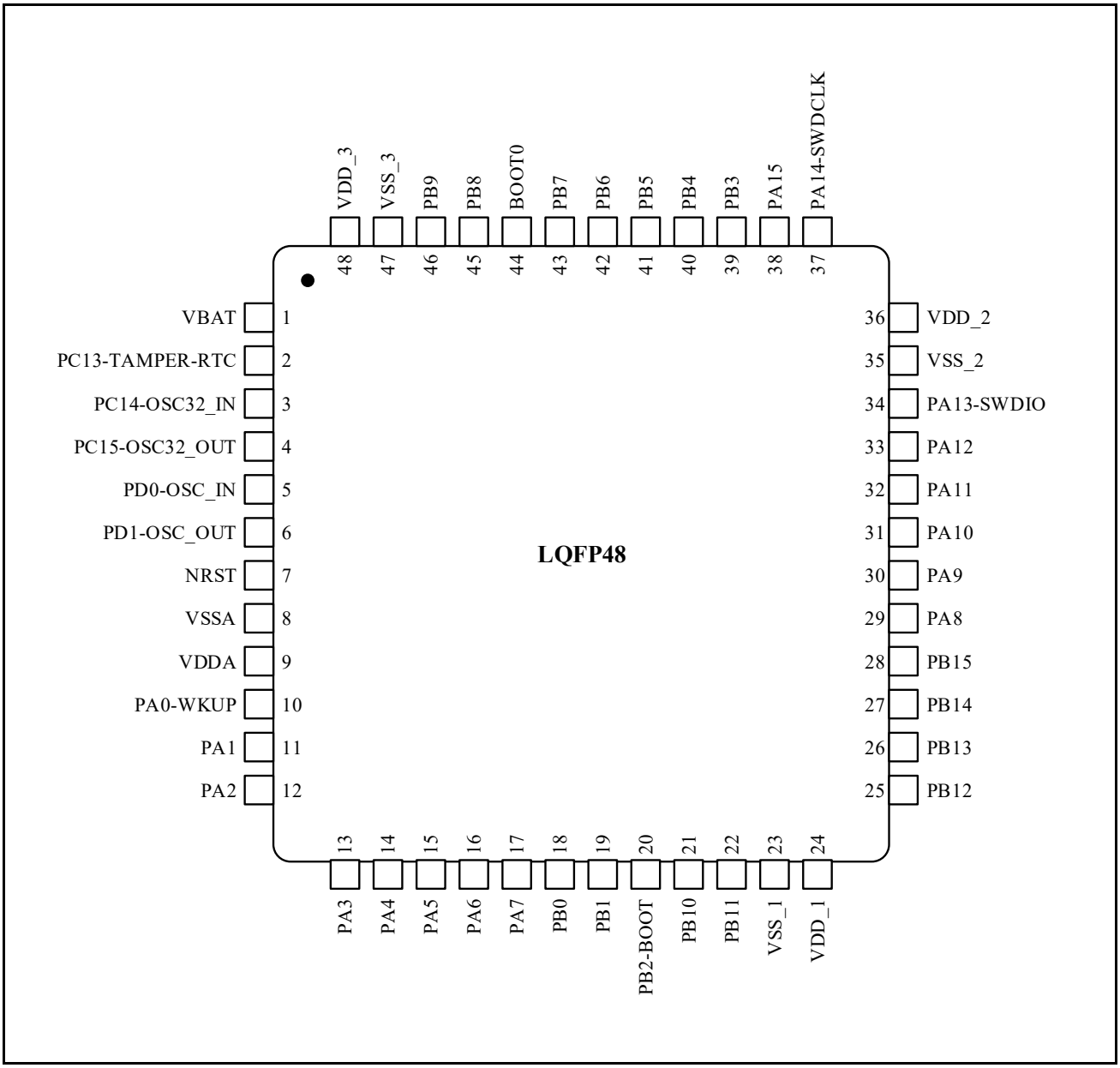
Packages

1.1 LQFP48 Package

1.1.1 LQFP48 Pin Assignment



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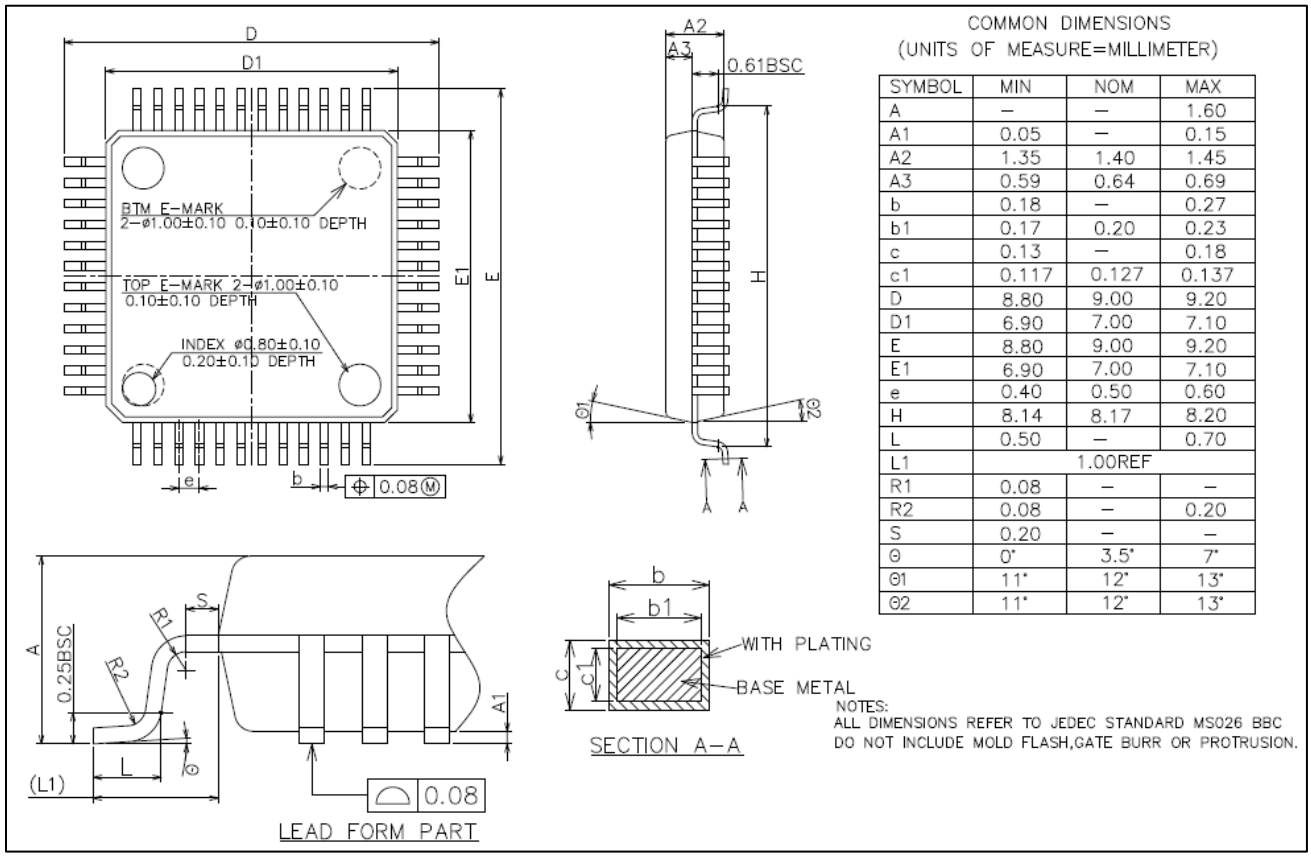
1.1.2 LQFP48(7mm x 7mm) Package Dimensions



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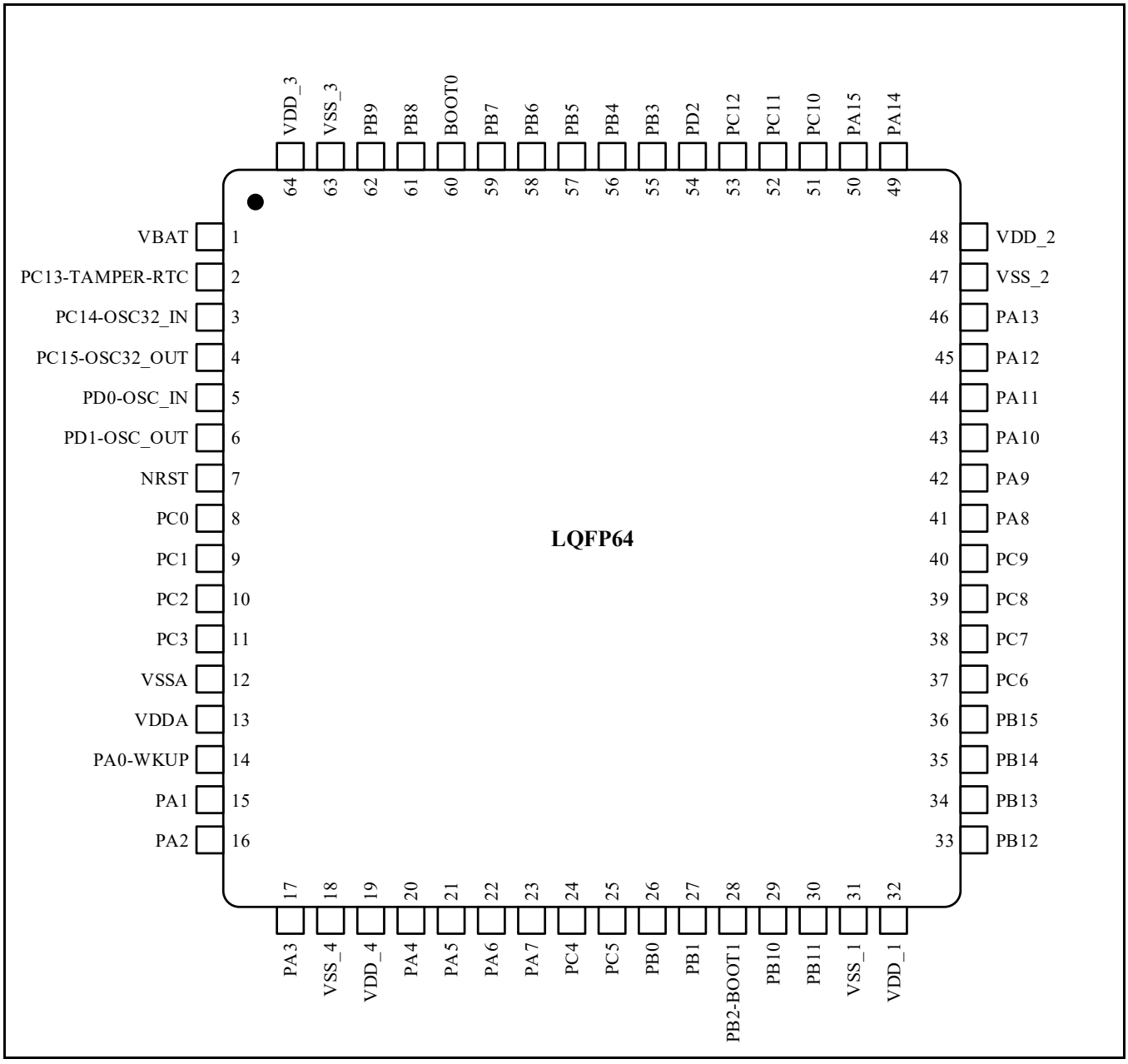
1.2 LQFP64 Package

1.2.1 LQFP64 Pin Assignment



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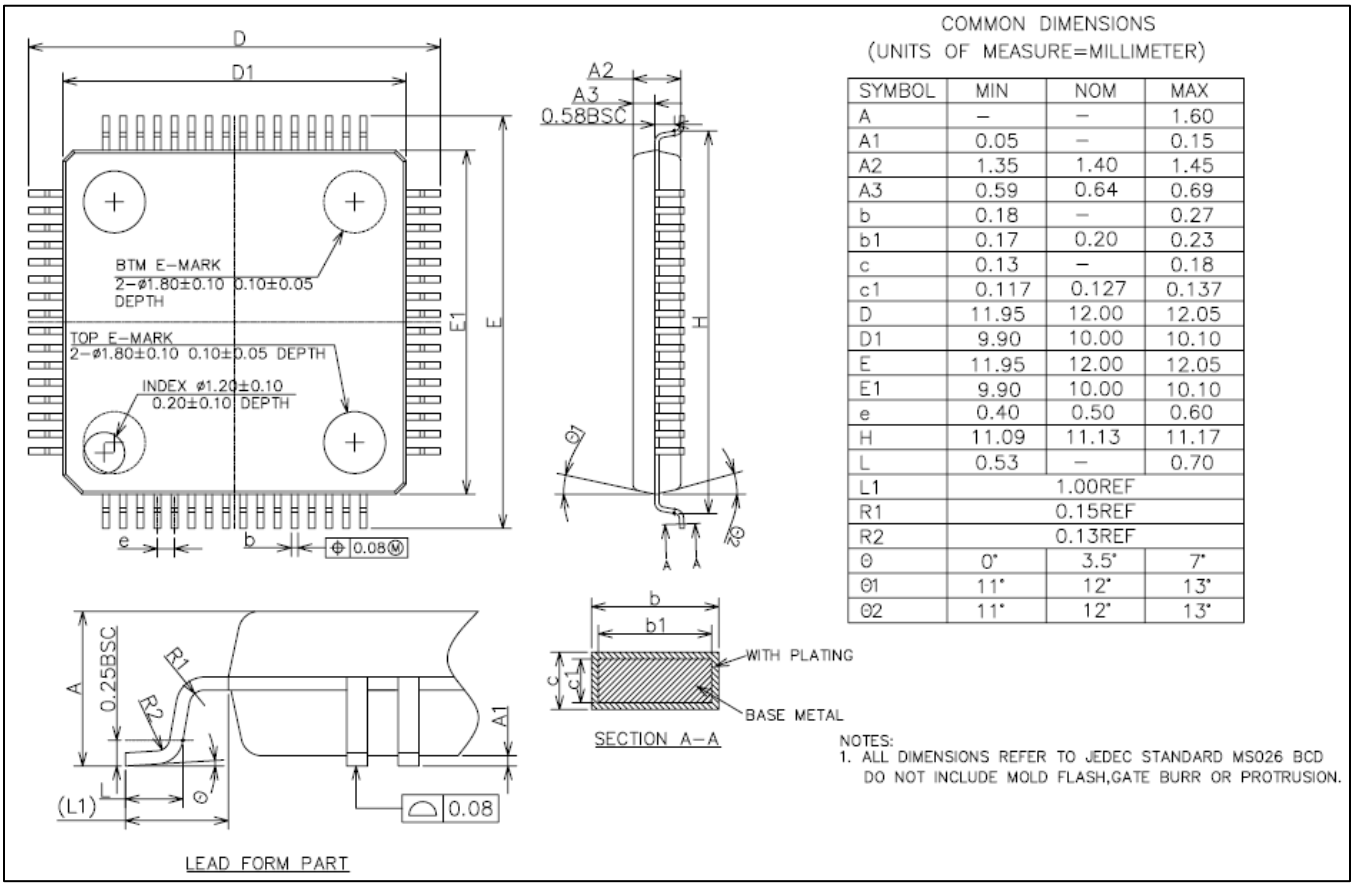
1.2.2 LQFP64(10mm x 10mm) Package Dimensions



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	–	–	1.60
A1	0.05	–	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	–	0.27
b1	0.17	0.20	0.23
c	0.13	–	0.18
c1	0.117	0.127	0.137
D	11.95	12.00	12.05
D1	9.90	10.00	10.10
E	11.95	12.00	12.05
E1	9.90	10.00	10.10
e	0.40	0.50	0.60
H	11.09	11.13	11.17
L	0.53	–	0.70
L1	1.00REF		
R1	0.15REF		
R2	0.13REF		
θ	0°	3.5°	7°
θ1	11°	12°	13°
θ2	11°	12°	13°

NOTES:
1. ALL DIMENSIONS REFER TO JEDEC STANDARD MS026 BCD
DO NOT INCLUDE MOLD FLASH,GATE BURR OR PROTRUSION.

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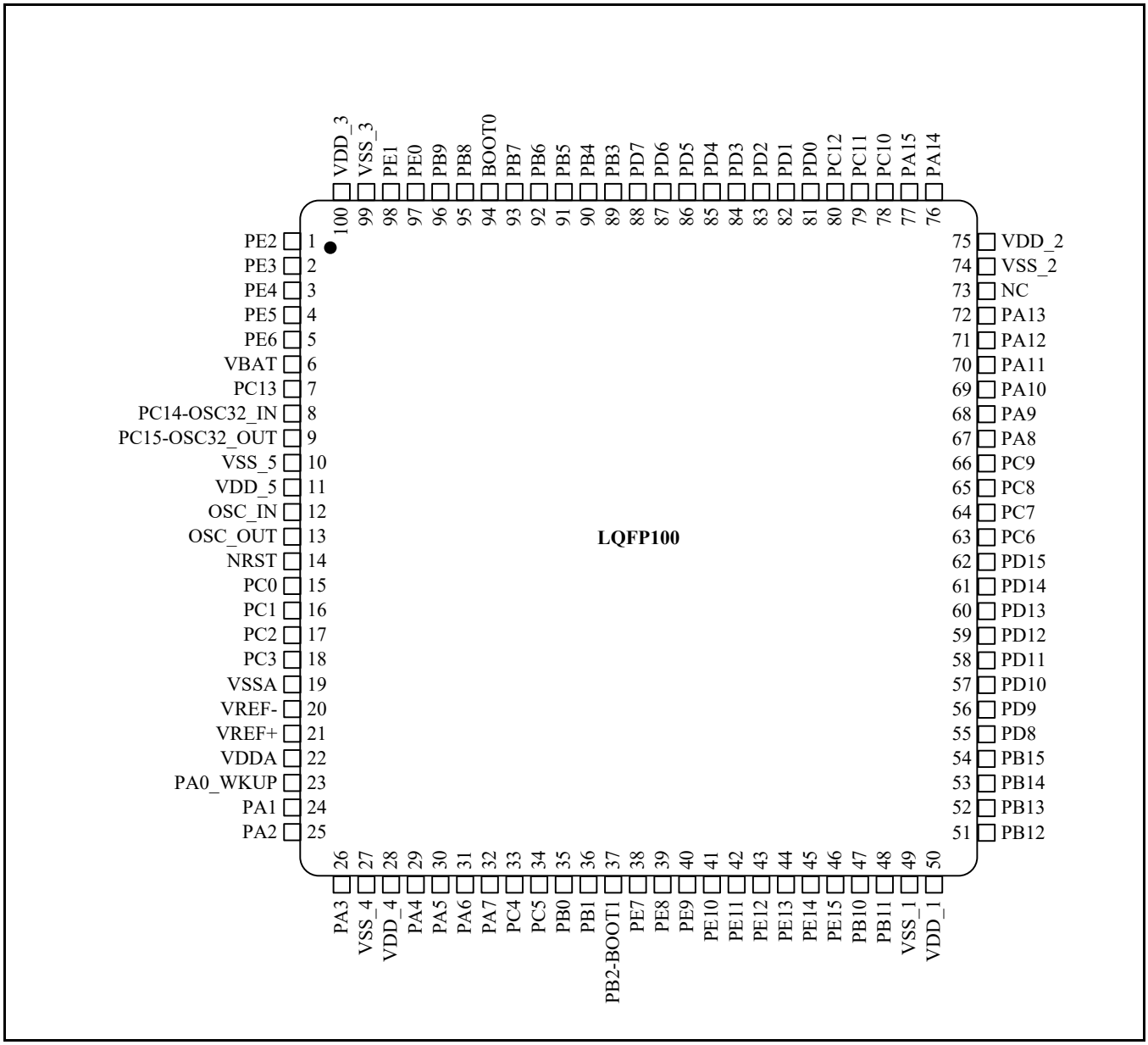
1.3 LQFP100 Package

1.3.1 LQFP100 Pin Assignment



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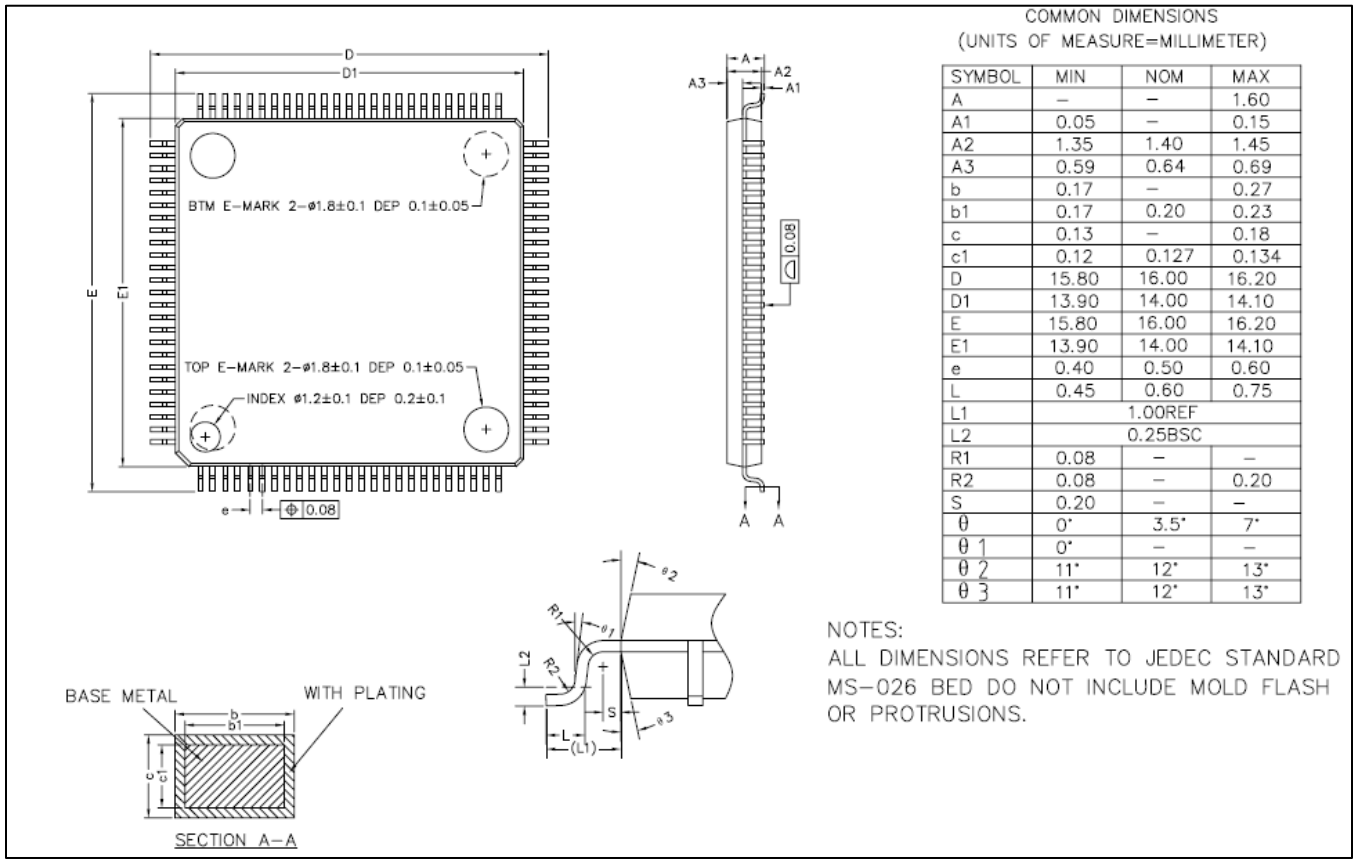
1.3.2 LQFP100(14mm x 14mm) Package Dimensions



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	–	–	1.60
A1	0.05	–	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.17	–	0.27
b1	0.17	0.20	0.23
c	0.13	–	0.18
c1	0.12	0.127	0.134
D	15.80	16.00	16.20
D1	13.90	14.00	14.10
E	15.80	16.00	16.20
E1	13.90	14.00	14.10
e	0.40	0.50	0.60
L	0.45	0.60	0.75
L1		1.00REF	
L2		0.25BSC	
R1	0.08	–	–
R2	0.08	–	0.20
S	0.20	–	–
θ	0°	3.5°	7°
θ1	0°	–	–
θ2	11°	12°	13°
θ3	11°	12°	13°

NOTES:
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Version History

Version	Date	Changes
V1.0	2023.09.21	Initial version

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