N32A455xxL7 series Product Brief

N32A455xxL7 series based on 32-bit ARM Cortex-M4F kernel, run up to 144MHz, support floating-point unit and DSP instructions, integrates up to 512KB embedded flash, 144KB SRAM, integrates rich high-performance analog devices, built-in 4x 12bit 4.7Msps ADCs, 4x independent rail-to-rail operational amplifiers, 7x high-speed comparators, 2x 1Msps 12bit DACs, integrates multi-channel U(S)ART, I2C, SPI, QSPI, CAN, SDIO communication interfaces, built-in cryptographic algorithm hardware acceleration engine

Key features

- **CPU core**
  - 32-bit ARM Cortex-M4 core + FPU, single-cycle hardware multiply instructions, DSP instruction and MPU support
  - Built-in 8KB instruction Cache, support Flash acceleration unit execution program 0 wait
  - Maximum main frequency 144MHz, 180DMIPS
- **Memory**
  - Up to 512KByte on-chip Flash with encrypted storage, partition management and data protection, hardware ECC checksum, 100,000 erasures, 10-year data retention
  - Up to 144KByte on-chip SRAM (including 16KByte Retention RAM) with hardware parity support
- **High-performance analog interface**
  - 4x 12bit 5Msps high-speed ADCs, configurable in 12/10/8/6-bit mode, with sampling rates up to 8.9Msps in 6bit mode, up to 38 external single-ended input channels, supporting differential mode
  - 4x rail-to-rail operational amplifiers with built-in programmable gain amplification up to 32x
  - Up to 7 high-speed analog comparators with built-in 64-level adjustable comparison reference
  - 2x 12-bit DACs with 1Msps sampling rate
  - Support external input independent reference voltage source
  - All analog interfaces support 1.8~3.6V full voltage operation
- **Clock**
  - 4MHz~32MHz External High Speed Crystal
  - 32.768KHz External Low Speed Crystal
  - Internal High Speed RC 8MHz
  - Internal low-speed RC 40KHz
  - Internal high speed PLL
  - Support 1 channel clock output, configurable system clock, HSE, HSI or PLL post-division output
- **Reset**
  - Support power-up/power-down/external pin reset
  - Support programmable low voltage detection and reset
  - Support watchdog reset

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- **Support up to 80 GPIOs with multiplexing function and a maximum flip speed of 50MHz**
- **Communication interface**
  - 7x U(S)ART interfaces, up to 4.5 Mbps, including 3 USART interfaces (1xISO7816, 1xIrDA, LIN supported) and 4 UART interfaces
  - 3x SPI interfaces with speeds up to 36 MHz, 2 of which support I2S
  - 1x QSPI interface with speeds up to 144 Mbps
  - 4x I2C interfaces at up to 1 MHz, master-slave mode configurable, dual address response support in slave mode
  - 2x CAN 2.0A/B bus interfaces
  - 1x SDIO interface, supporting SD/SDIO/MMC format
- **2x high-speed DMA controllers, each controller supports 8 channels, channel source and destination**
- **RTC real time clock, support leap year perpetual calendar, alarm events, periodic wake-up, support internal and external clock calibration**
- **Timer counter**
  - 2x 16-bit advanced timer counters, support input capture, complementary output, quadrature encoding input, etc., with maximum control accuracy of 6.9ns; each timer has 4 independent channels, 3 of which support 6 complementary PWM outputs
  - 4x 16bit general-purpose timers, each timer has 4 independent channels, support input capture/output comparison/PWM output
  - 2x 16bit base timer counters
  - 1x 24bit SysTick
  - 1x 7bit Window Watchdog (WWDG)
  - 1x 12bit Independent Watchdog (IWDG)
- **Programming mode**
  - Support SWD/JTAG online debugging interface
  - Support UART bootloader
- **Safety features**
  - Built-in hardware acceleration engine for cryptographic algorithms
  - Support DES/3DES、AES、SHA1/SHA224/SHA256、SM1、SM3、SM4、SM7、MD5 algorithms
  - Flash storage encryption, multi-user partition management (MMU)
  - TRNG true random number generator
  - CRC16/32 operation
  - Support write protection (WRP), multiple read protection (RDP) levels (L0/L1/L2)
  - Support program encryption download
  - Support clock failure detection, tamper-proof detection
- **96-bit UID and 128-bit UCID**
- **Working Conditions**

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- Working voltage range: 1.8V~3.6V
- Working temperature range: -40℃~105℃
- Certified by AEC-Q100-G2
- ESD: ±4KV (HBM model), ±1KV (CDM model)

- **Package**
  - LQFP48(7mm x 7mm)
  - LQFP64(10mm x 10mm)
  - LQFP100(14mm x 14mm)

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1 Ordering information

Figure 1-1 N32A455 Series Part Number Information

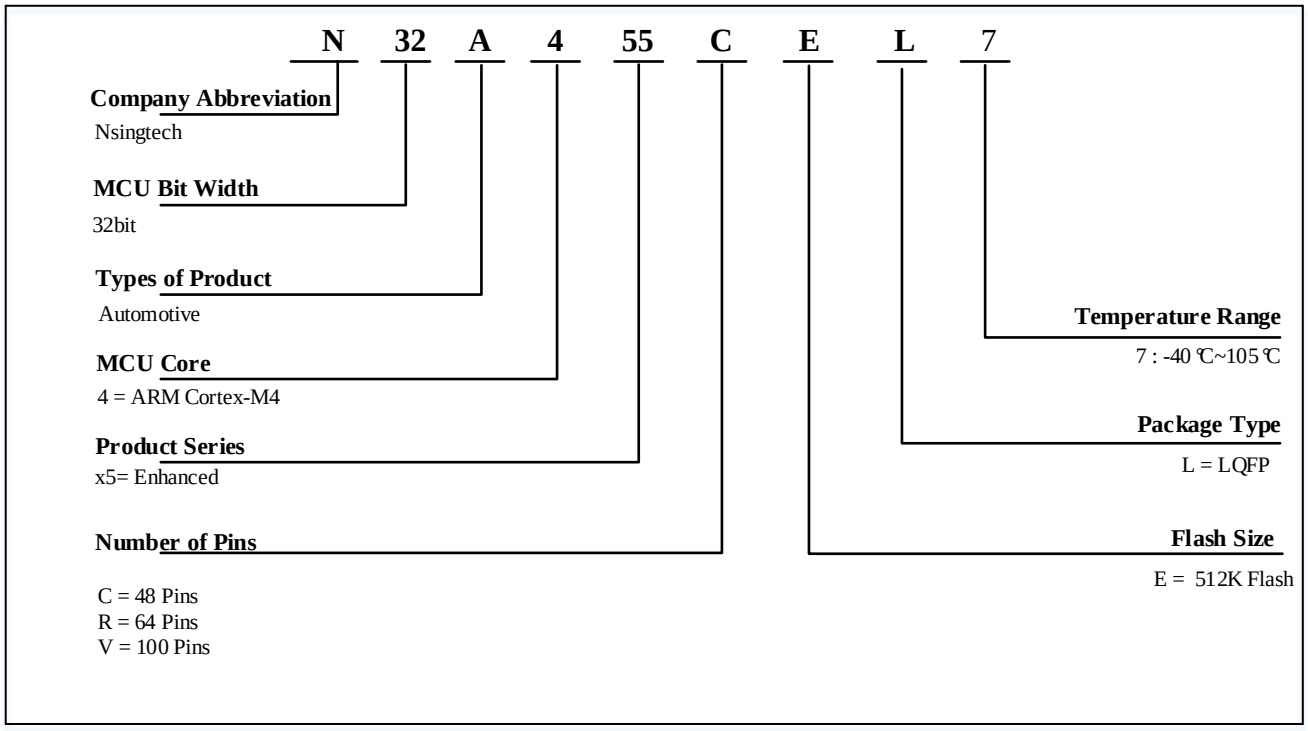

Table 1-1 N32A455 Series Ordering Code

Ordering code (1)	Package	Package size	Packaging (2)	SPQ(3)	Temperature range
N32A455CEL7	LQFP48	7mm*7mm	Tray	250	-40℃ ~ 105℃
N32A455REL7	LQFP64	10mm*10mm	Tray	160	-40℃ ~ 105℃
N32A455VEL7	LQFP100	14mm*14mm	Tray	90	-40℃ ~ 105℃

1. For the latest detailed ordering information, please refer to the Selection Guide.
2. The packaging provided is the basic packaging. If user has any other requirements, please contact NSING.
3. Minimum packaging quantity.

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2 List of devices

Part number		N32A455CEL7	N32A455REL7	N32A455VEL7
Flash capacity (KB)		512		
SRAM capacity (KB)		144		
CPU frequency		ARM Cortex-M4 @144MHz,180DMIPS		
Working environment		1.8~3.6V/-40~105℃		
Timer	General	4		
	Advanced	2		
	Basic	2		
Communication interface	SPI	3		
	I2S	2		
	QSPI	Only Single Wire	1	
	I2C	3	4	
	USART	3		
	UART	3	4	
	CAN	2		
	SDIO	No	1	
GPIO		37	51	80
DMA		2		
Number of Channels		16Channel		
12bit ADC		4	4	4
Number of channels		16Channel	22Channel	38Channel
12bit DAC		2		
Number of channels		2Channel		
OPA/COMP		4/5	4/7	4/7
Algorithm support		DES/3DES、AES、 SHA1/SHA224/SHA256、SM1、SM3、SM4、SM7、MD5、CRC16/CRC32、TRNG		
Security protection		Read-write protection (RDP/WRP), Storage encryption, Partition protection, Secure startup		
Package		LQFP48	LQFP64	LQFP100

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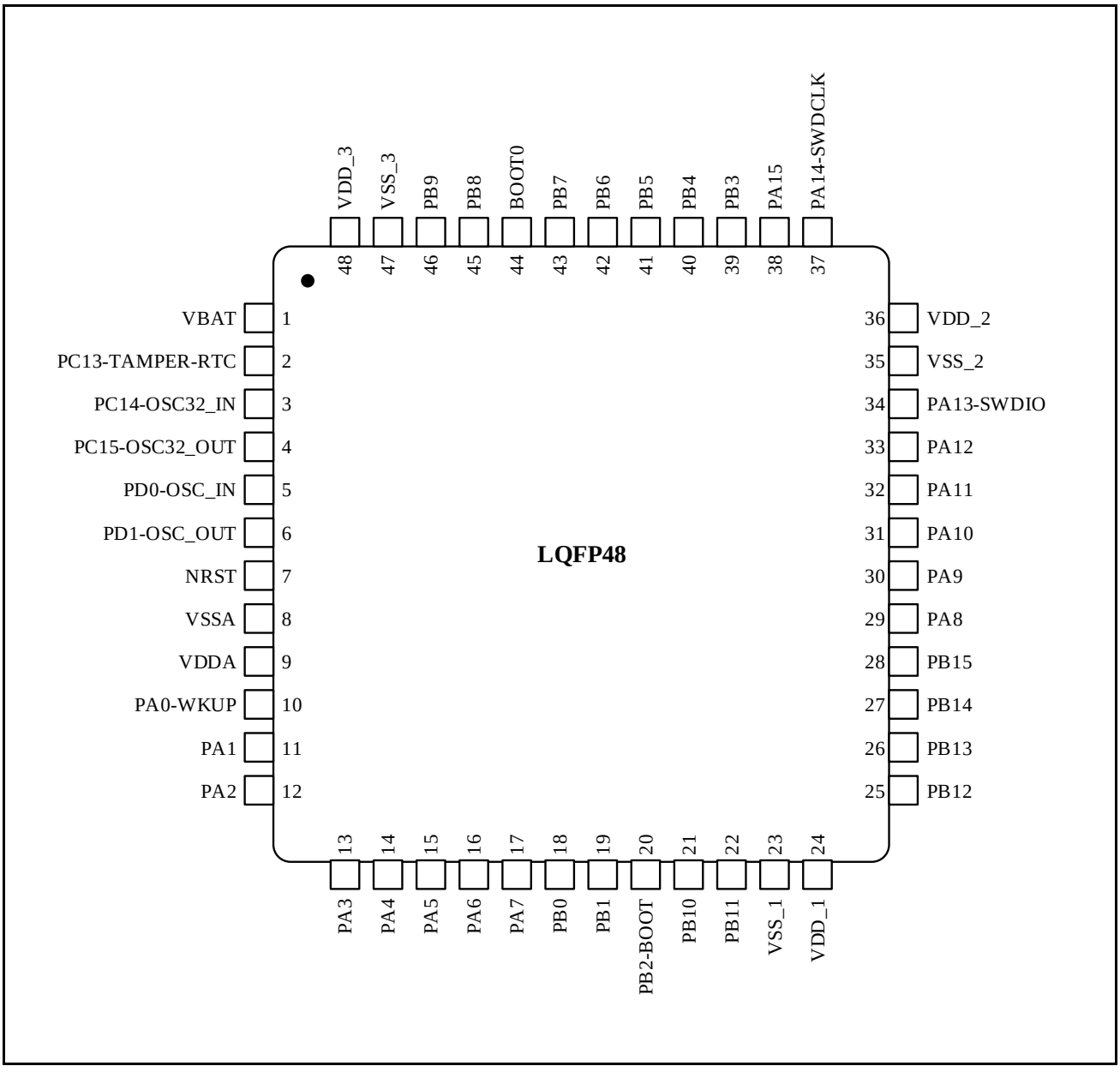
3 Package Information

3.1 LQFP48 package

3.1.1 LQFP48 pinouts



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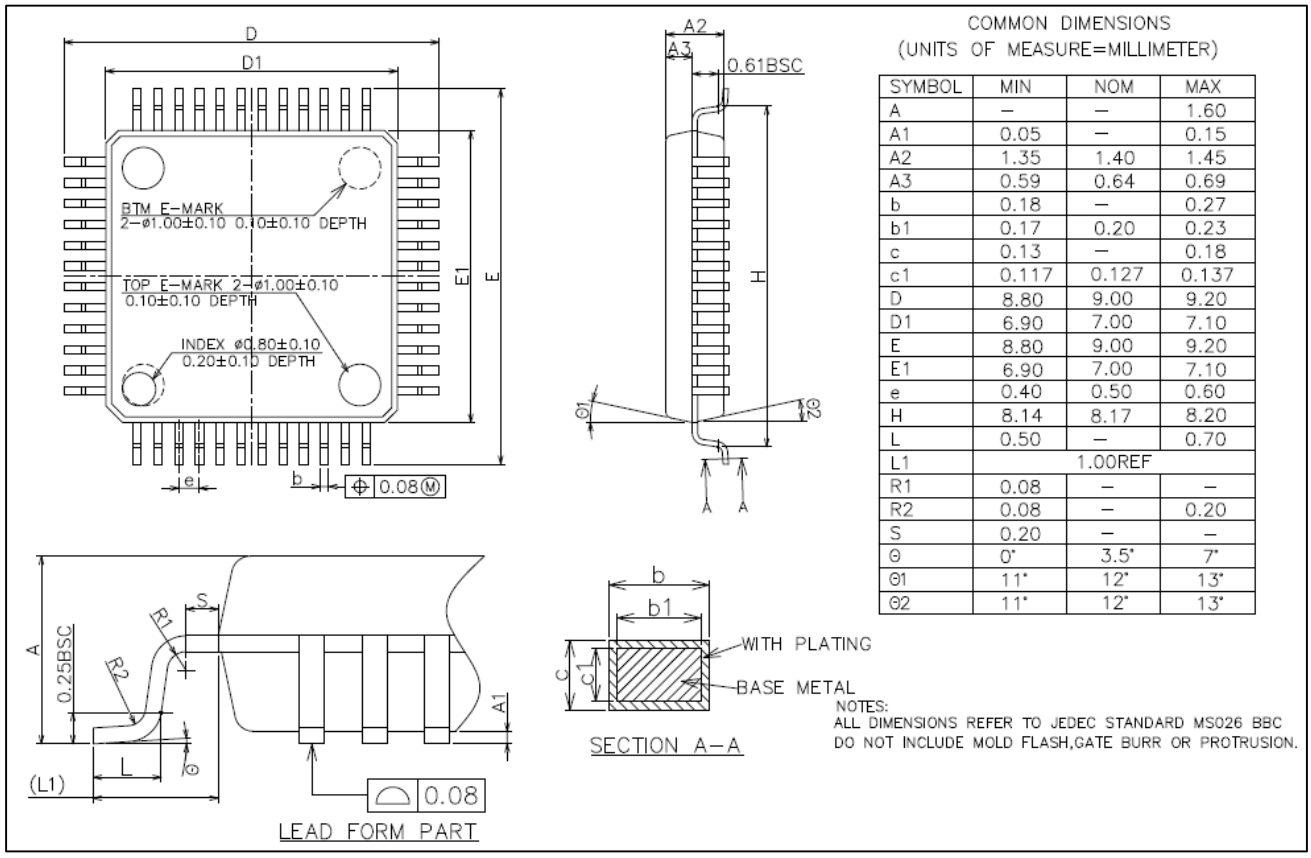
3.1.2 LQFP48 package outline



SYMBOL	MIN	NOM	MAX
A	–	–	1.60
A1	0.05	–	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	–	0.27
b1	0.17	0.20	0.23
c	0.13	–	0.18
c1	0.117	0.127	0.137
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
e	0.40	0.50	0.60
H	8.14	8.17	8.20
L	0.50	–	0.70
L1		1.00REF	
R1	0.08	–	–
R2	0.08	–	0.20
S	0.20	–	–
θ	0°	3.5°	7°
θ1	11°	12°	13°
θ2	11°	12°	13°

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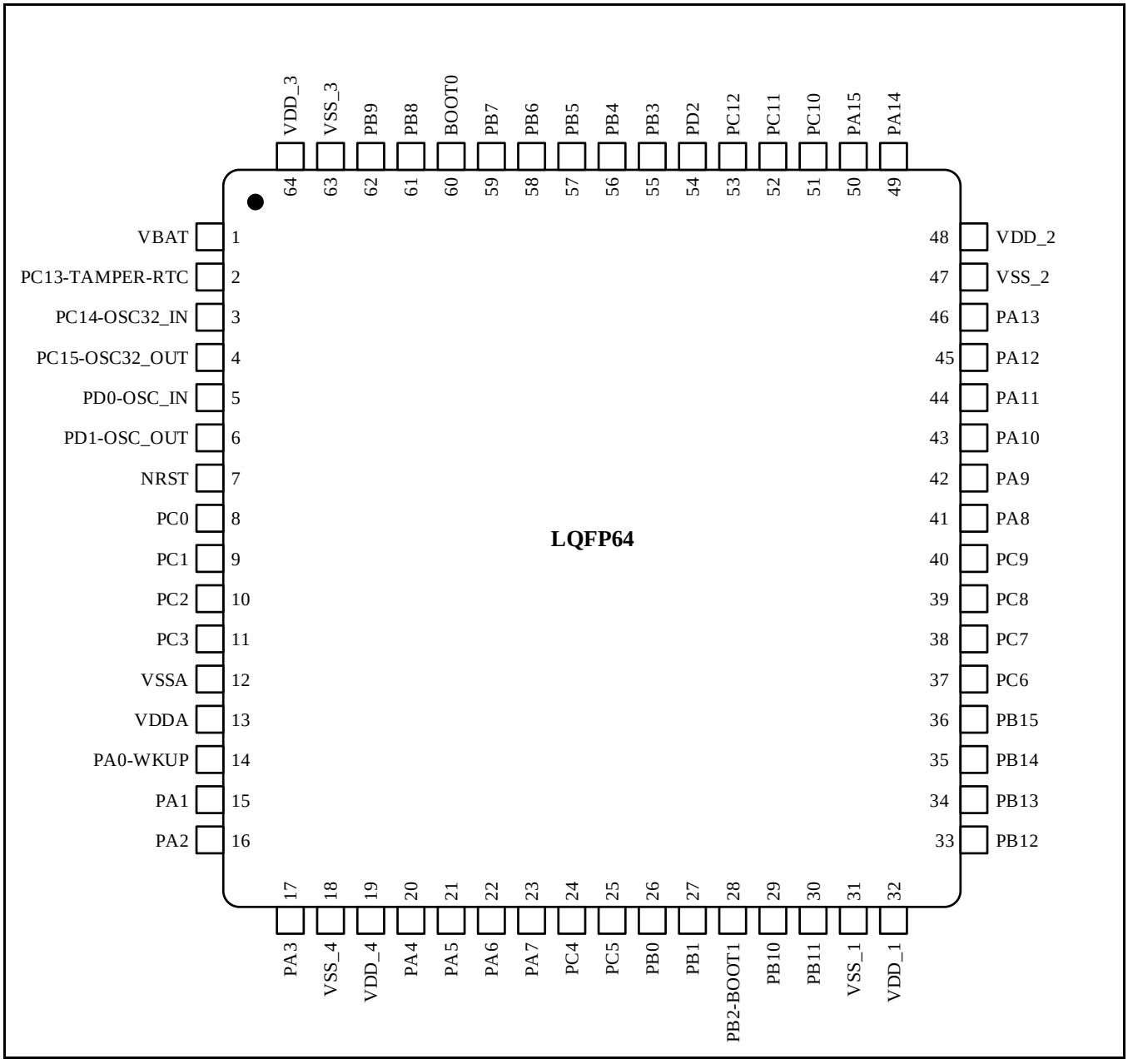
3.2 LQFP64 package

3.2.1 LQFP64 pinouts



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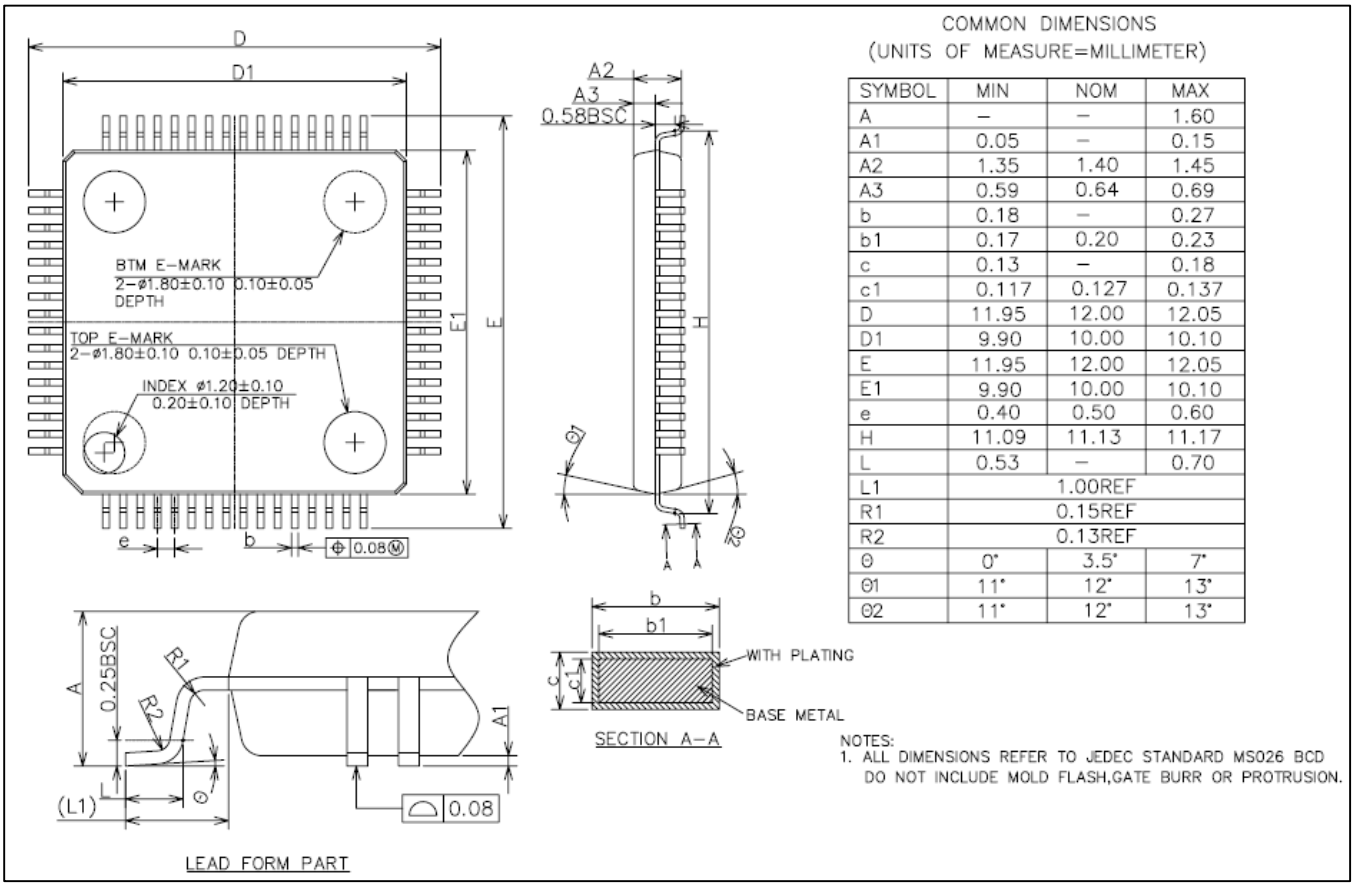
3.2.2 LQFP64 package outline



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	–	–	1.60
A1	0.05	–	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	–	0.27
b1	0.17	0.20	0.23
c	0.13	–	0.18
c1	0.117	0.127	0.137
D	11.95	12.00	12.05
D1	9.90	10.00	10.10
E	11.95	12.00	12.05
E1	9.90	10.00	10.10
e	0.40	0.50	0.60
H	11.09	11.13	11.17
L	0.53	–	0.70
L1	1.00REF		
R1	0.15REF		
R2	0.13REF		
θ	0°	3.5°	7°
01	11°	12°	13°
02	11°	12°	13°

NOTES:
1. ALL DIMENSIONS REFER TO JEDEC STANDARD MS026 BCD
DO NOT INCLUDE MOLD FLASH,GATE BURR OR PROTRUSION.

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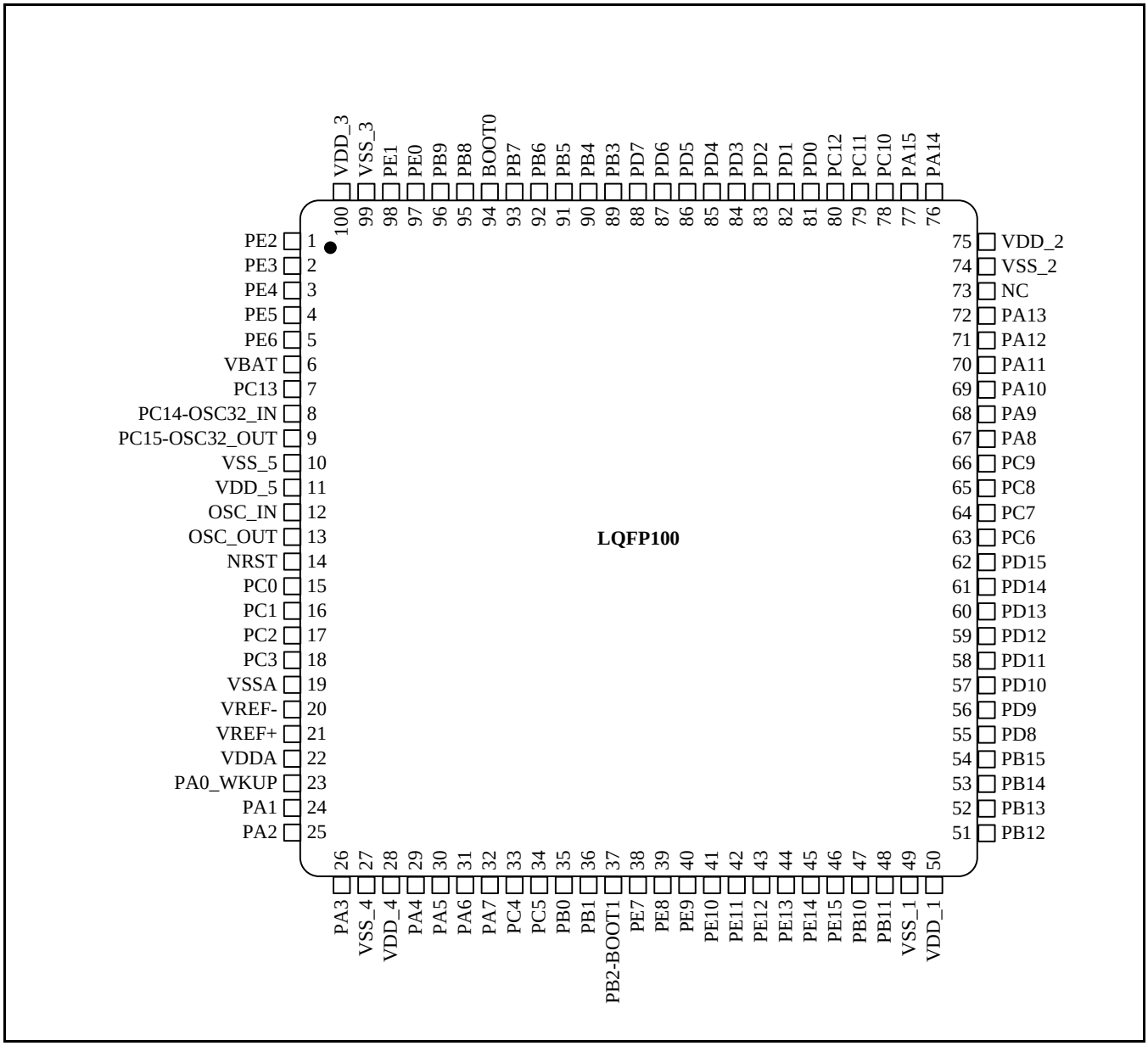
3.3 LQFP100 package

3.3.1 LQFP100 pinouts



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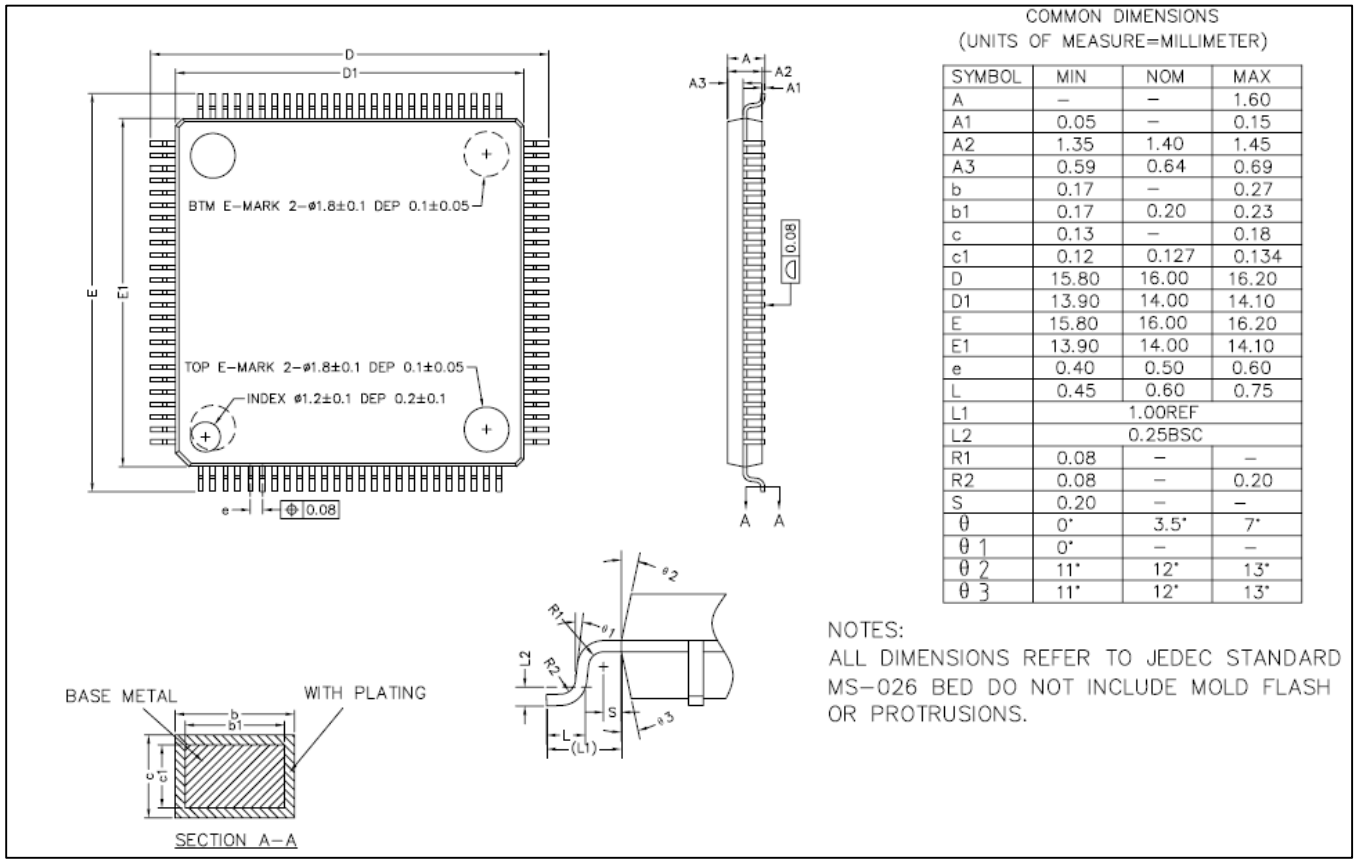
3.3.2 LQFP100 package outline



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	–	–	1.60
A1	0.05	–	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.17	–	0.27
b1	0.17	0.20	0.23
c	0.13	–	0.18
c1	0.12	0.127	0.134
D	15.80	16.00	16.20
D1	13.90	14.00	14.10
E	15.80	16.00	16.20
E1	13.90	14.00	14.10
e	0.40	0.50	0.60
L	0.45	0.60	0.75
L1		1.00REF	
L2		0.25BSC	
R1	0.08	–	–
R2	0.08	–	0.20
S	0.20	–	–
θ	0°	3.5°	7°
θ1	0°	–	–
θ2	11°	12°	13°
θ3	11°	12°	13°

NOTES:
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4 Version History

Date	Version	Remarks
2023.09.21	V1.0.0	Initial version
2024.11.20	V1.1.0	1. Modify Part number information to ordering information, modify ordering information table
2026.03.17	V1.2.0	1. Modify the description in the main features section to “single-cycle hardware multiply instruction”

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