N32G401 Series Errata Sheet

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2 Power Control (PWR)

2.1 Cannot Reset The Chip By Pressing NRST Button In DEBUG STOP2 Mode

Description

When the DBG_CTRL.STOP bit is set to 1 and the chip enters the STOP2 mode, the chip cannot be reset by pressing the NRST button.

Workaround

Clear the DBG_CTRL.STOP bit before the chip enters STOP2 mode.

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3 Timer (TIM)

3.1 TIM1/2/3/4/5/8 Cannot Generate Compare Events Under Specific Conditions

Description

In edge-aligned mode, and up-counting PWM1 mode, when CCDATx shadow register value is greater than or equal to AR value in current PWM cycle, if the CCDATx shadow register value is 0 in the next PWM cycle, the compare event will not be generated at the moment although the value of PWM cycle counter is equal to the value of CCDATx shadow register, which is 0.

Workaround

If it is not required that "the compare event is generated at the time when the count value = the shadow register of the compare value =0", the compare event can be generated through another channel.

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4 Serial Peripheral Interface (SPI)

4.1 I2S Interface

4.1.1 PCM Long Frame Mode

Description

When I2S is operating in master mode, PCM long frame mode, and the data format is set to "32bit" or "16bit extended to 32bit", the WS signal is generated every 16bits per cycle instead of 32bit.

Workaround

If I2S must operate in master mode and use long frame mode, it is recommended to use only the 16-bit data mode to ensure proper WS signal alignment.

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5 Real Time Clock (RTC)

5.1 The First Automatic Wake-up Time Of The RTC is Abnormal

Description

After setting up the RTC calendar and configuring the automatic wake-up function, the time from enabling automatic wake-up to the first wake-up is smaller than the time represented by the wake-up automatic reload value. But the subsequent automatic wake-up time is normal.

Workaround

Ignore the first wakeup.

5.2 The RTC Wakeup Event occurs Before the Chip Enters STANDBY Mode Resulting In the Chip Being Unable to Wake Up

Description

Before the chip enters STANDBY mode, if an RTC wakeup event occurs, the chip will not wake up after entering STANDBY mode.

Workaround

None.

5.3 The RTC Calendar Function Prohibits Multiple Initializations Within 1 Second

Description

Multiple initializations of the RTC calendar function within 1 second will result in the inability to generate RTC alarm interrupts..

Workaround

The interval between two initializations of the RTC calendar function should be more than 1 second.

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5.4 The RTC Incorrectly Triggers the TISOVF Flag

Description

When the system wakes up from STANDBY mode or reset by IWDG timeout, the TISOVF flag in RTC may be set incorrectly.

Workaround

Before entering STANDBY mode or when the system is reset by IWDG time out, when the SHOPF flag is 0, configure RTC_SCTRL.SUBF [14:0] register once, and SHOPF flag will set to 1. When SHOPF flag become 0 again, configure RTC_SCTRL.SUBF [14:0] register for the second time. This will solve the issue.

Note: NRST cannot be triggered during above process.

5.5 The Shift Operation of The RTC on The Sub-seconds Causes Inaccurate Current Wake-Up Time

Description

When the RTC is configured as periodic wake up, performing the shift operation on sub-seconds before triggering the periodic wake-up will cause the current wake-up time to be inaccurate, and the subsequent wake-up time will be normal.

Workaround

No solution is provided for this issue.

5.6 RTC_DATE Register Being Locked

Description

1. Before the system software reset, if the RTC_DATE register is not read after reading the RTC_SUBS or RTC_TSH shadow register, and after the system software reset, if the RTC is initialized without configuring or reading the RTC_DATE register, the RTC_DATE register will revert to its default value;
2. When reading the calendar, after reading the RTC_SUBS or RTC_TSH shadow register, the value of the RTC_DATE register remains unchanged;

Workaround

1. Read the RTC_DATE register before initializing the RTC;
2. After reading the RTC_SUBS or RTC_TSH shadow register, read the RTC_DATE register;

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6 GPIO And AFIO

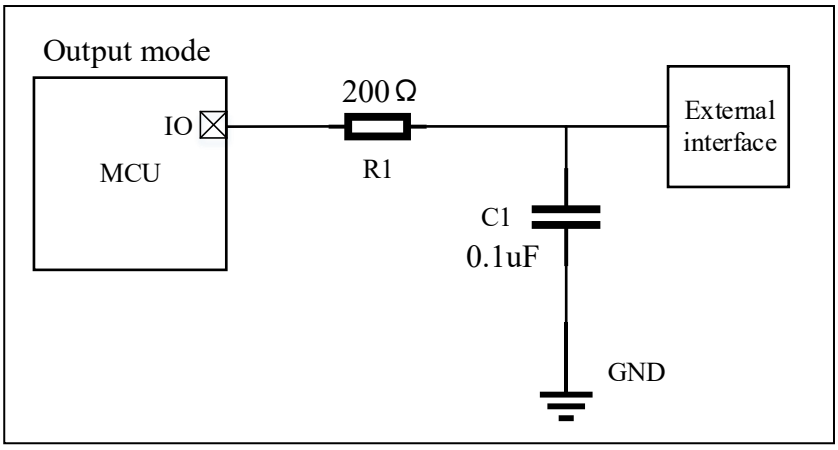
6.1 Glitches Occur on The IO Appeared During Chip Power-On

Description

When the MCU is powered on, some IOs will have glitches appeared.

Workaround

When an IO is used as an input, the glitches have no effect on MCU; When an IO is used as an output, an external 200Ohm resistor and a 0.1uF capacitor are applied for filtering to solve the issue.



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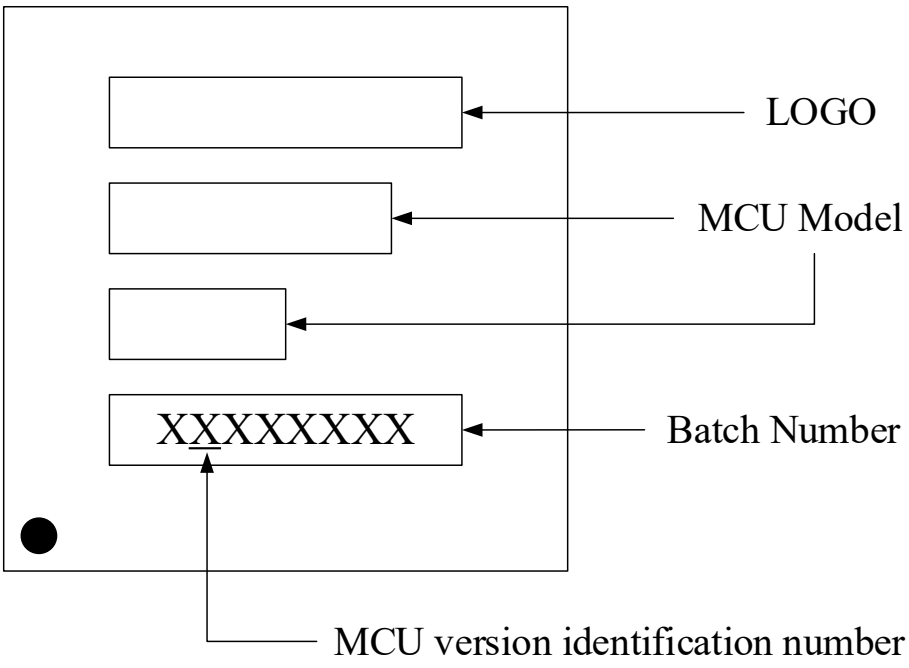
7 Chip Marking And Revision Description



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8 Version History

Version	Date	Changes
V1.0.0	2023.5.16	Initial release

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