

## N32G401x6/x8

## **Product Brief**

N32G401 series uses 32-bit ARM Cortex-M4F core, operating frequency up to 72MHz, supporting floating-point unit and DSP instructions. The devices integrate up to 64KB of encrypted flash, and 8KB of SRAM. The series features rich of high-performance interfaces, including 1 built-in 12bit 4.2Msps ADC, 3 high-speed comparators, multi-channel U(S)ART, I2C, SPI and other communication interfaces.

## **Key Features**

- CPU Core
  - 32-bit ARM Cortex-M4F with FPU, supports DSP instructions
  - Built-in 1KB instruction Cache, supports Flash accelerator unit for zero-wait program execution
  - Maximum frequency of 72MHz, 90DMIPS

#### • Memories

- Up to 64KByte of embedded Flash memory
  - Supporting encrypted memory function, partition management and data protection
  - o 10,000 erase/write cycles and 10 years data retention
- Up to 8KByte on-chip SRAM, retained in Stop2 mode, can be configured to retention in Standby mode

#### Low Power Management

- Sleep mode: The CPU is stopped; all peripherals are active and can wake up the CPU
- Stop0 mode: PLL, HSI and HSE are disabled, LSE/LSI can keep running, RTC can keep running, SRAM and all register contents retained, all IOs retained.
- Stop2 mode: PLL, HSI and HSE are disabled, LSE/LSI can keep running, RTC can keep running, SRAM and all register contents retained, all IOs retained, CPU register and backup register contents retained.
- Standby mode: Internal voltage regulator is turned off, PLL, HSI and HSE are disabled, LSE/LSI can keep running, RTC and IWDG can keep running, SRAM can be configured to retention, all IOs retained.

#### High-performance Analog Interfaces

- 1x 12bit ADC with 4.2Msps
  - $\circ$  Configurable as 12/10/8/6 bits mode
  - o Up to 16 external single-ended input channels, 3 internal single-ended input channels
  - Support differential mode
- 3x COMPs with internal 64-level adjustable comparison reference

#### Clock

- HSE: 4MHz~32MHz high-speed external crystal oscillator
- LSE: 32.768KHz low-speed external crystal oscillator
- HSI: High-speed internal RC 8MHz
- LSI: Low speed internal RC 40KHz
- Built-in high-speed PLL



 MCO: Support 2-channals clock output, configurable as SYSCLK, HSI, HSE, LSI, LSE, and PLL divisional output

• Reset

- Supports power-on/power-down/external pin reset.
- Supports watchdog reset, software reset.
- Supports programmable voltage detection.
- GPIO
  - Up to 39+1 GPIOs
- Communication Interfaces
  - 4x U(S)ART interfaces
    - 2x USART interfaces (support ISO7816, IrDA, LIN)
    - 2x UART interfaces
  - 2x SPI interfaces
    - Speed up to 28Mbps (without CRC) and 20Mbps (with CRC) in master mode.
    - Speed up to 32Mbps in slave mode.
    - Supports I2S
  - 2x I2C interfaces (Master/Slave) with speed up to 1 MHz, support dual address responses in slave mode
- DMA controller
  - 1 x high-speed DMA controller supports 8 channels, with arbitrarily configurable channel sources and destination addresses
- RTC real-time clock
  - Supports leap year calendar, alarm event, periodic wake up
  - Supports internal and external clock calibration
- Beeper
  - Supports complementary output, 12mA output driving capability
- Timer
  - 2x 16-bit advanced timers with maximum control precision of 7.8ns
    - o Supports input capture, complementary output, quadrature encoder input, etc.
    - Each timer has four independent channels, of which Timer1 supports 8 channels complementary PWM output, Timer8 supports 6 channels complementary PWM output
  - 4x 16-bit general purpose timers
    - Each timer has 4 independent channels.
    - Supports input capture/output comparison /PWM output.
  - 1x 16-bit basic timer
  - 1x 16-bit low power timer



- Supports single pulse and double pulse counting function.
- Supports operating in STOP2 mode.
- 1x 24-bit SysTick timer
- 1x 14-bit Window Watchdog (WWDG)
- 1x 12-bit Independent Watchdog (IWDG)
- Programming Methods
  - Supports SWD/JTAG debugging interface.
  - Supports UART Bootloader
- Security Features
  - Flash storage encryption, Multi-user partition Management Unit (MMU)
  - CRC16/32 computation
  - Supports write protection (WRP), multiple level (L0/L1/L2) of read protection (RDP)
  - Supports secure boot, encrypted program download, secure firmware updates.
  - Supports external clock failure detection, anti-tamper detection.
- 96-bit UID and 128-bit UCID
- Operating Conditions
  - Operating voltage range: 2.4V~3.6V
  - Operating temperature range:  $-40^{\circ}$ C ~  $105^{\circ}$ C
  - ESD: ±4KV (HBM model), ±2KV (CDM model)
- Packages
  - LQFP32(7mm x 7mm)
  - LQFP48(7mm x 7mm)
  - QFN20(3mm x 3mm)
  - QFN28(4mm x 4mm)
  - QFN32(4mm x 4mm)
  - QFN48(6mm x 6mm)
  - TSSOP20(6.5mm x 4.4mm)
- Ordering Information

Reference	Part Number					
	N32G401C6L7, N32G401K6L7					
N32G401x6	N32G401C6Q7, N32G401K6Q7, N32G401G6Q7, N32G401F6Q7,					
	N32G401F6S7-1					
	N32G401C8L7, N32G401K8L7					
N32G401x8	N32G401C8Q7, N32G401K8Q7, N32G401G8Q7, N32G401F8Q7,					
	N32G401F8S7-1					



# **1** Naming Convention

N 32	G 4 0'		8 L	7
Company Prefix N:NSING Technologies Pte. Ltd.	Processor Core 0=ARM Cortex-M0	Pin Count(pins) F=20 pin P=25 pin	Package L=LQFP T=TQFP	Temperature Range
Processor(Bit) 32 = 32bit	4=ARM Cortex-M4F 7=ARM Cortex-M7F	G=28 pin K=32 pin T=36 pin H=40 pin	Q=QFN W=WLCSP S=TSSOP U=UFQFPN	6=-40~+85° C 7=-40~+105° C 8=-40~+125℃
Product Family G=General H=High-Performance L=Low power consumption WB=Wireless Bluetooth M=Motor control A=Automotive grade	Product Series x0,03=Value x2,x1=Mainstream x3/5=High-performance x6=LCD series x7=Interconnect FR=Fingerprint identification series 17=SIP(4*OPAMP+250V 6N Predrive)	C=48 pin R=64 pin M=80 pin L=88 pin V=100 pin Q=128 pin	Flash Size 4=16KB Flash 5=29.5KB Flash 6=32KB Flash 8=64KB Flash B=128KB Flash C=256KB Flash E=512KB Flash G=1024KB Flash	

#### Figure 1-1 N32G401 Series Part Naming Conversion



# 2 Product Configurations

D	evice	N32G401F687-1	N32G401F8S7-1	N32G401F6Q7	N32G401F8Q7	N32G401G6Q7	N32G401G8Q7		
Flash ca	pacity (KB)	32	64	32	64	32	64		
	apacity (KB)	8	8	8	8	8	8		
CPU f	requency		ARM	I Cortex-M4F @	72MHz, 90DM	MIPS			
Operating	g Conditions		2.4~3.6V/-40~105℃						
	General		4						
Timers	Advanced			2	(1)				
Tin	Basic			1	l				
Ľ	LPTIM		1						
uo	SPI	2							
cati ces	I2S	2							
I2S2I2C2UART1									
UART			1			2			
SPI2I2S2I2C2UART1USART2									
BE	EPER			]	1				
GPIO		15+1				23	+1		
DMA Number of Channels			1 8 Channel						
12bit ADC		1	l	1 1		l			
Number of Channels		9Cha	9Channel 7Channel 10Ch			annel			
COMP		0 3							
Security	Protection	Read and Write	Protection (RD)	P/WRP), Memor	ry Encryption, P	artition Protection	on, Secure Boo		
Pa	ckage	TSS	OP20	QFI	N20	QF	N28		

#### Table 2-1 N32G401 Series Resource Configuration (1)

Note: <sup>(1)</sup> Timer1 supports 4 channels and 8 complementary output, Timer8 supports 3 channels and 6 complementary output.



evice	N32G401K6L7 N32G401K6O7	N32G401K8L7 N32G401K8O7	N32G401C6L7	N32G401C8L7 N32G401C8Q7			
nacity (KB)		_	_	64			
				8			
• • • •		_	-	-			
		Č					
Basic			1				
LPTIM		]	1				
SPI		2					
I2S	2						
I2C	2						
UART	2						
USART	2						
EPER	1						
GPIO	25+1 39+1			+1			
DMA		1	1				
of Channels	8 Channel						
it ADC	1	l	1				
of Channels	10Channel 16Channel			annel			
OMP	3						
Protection	Read and Write Protection (RDP/WRP), Memory Encryption, Partition Protection, Secure Boot						
ckage	•	FP32	LQFP48 QFN48				
	pacity (KB) apacity (KB) frequency g Conditions General Advanced Basic LPTIM SPI I2S I2C UART USART EPER BPIO DMA of Channels it ADC of Channels OMP	eviceN32G401K6Q7pacity (KB)32apacity (KB)8TrequencyAg Conditions9GeneralAAdvanced9Basic10LPTIM10SPI12I2S12UART10USART25DMA10of Channels10it ADC10of Channels10of Channels10ADC10OMP10Approtection10Channels </td <td>eviceN32G401K6Q7N32G401K8Q7pacity (KB)3264apacity (KB)88FrequencyARM Cortex-M4F @g Conditions2.4~3.6V/g Conditions2.4~3.6V/General2Advanced2Basic2LPTIM2I2S2I2C2UART2EPER2PIO25+1DMA10Channelof Channels10ChannelOMP2ProtectionRead and Write Protection (RDP/W Protection, Protection, IOFP32</td> <td>eviceN32G401K6Q7N32G401K8Q7N32G401C6Q7pacity (KB)<math>32</math><math>64</math><math>32</math>apacity (KB)<math>8</math><math>8</math><math>8</math>SrequencyARM Cortex-M4F @.72MHz, 90DMIFg Conditions<math>2.4 \sim 3.6 V/-40 \sim 105 °C</math>General<math>4</math>Advanced<math>2^{(1)}</math>Basic<math>1</math>LPTIM<math>1</math>SPI<math>2</math>I2S<math>2</math>UART<math>2</math>USART<math>2</math>EPER<math>1</math>of Channels<math>8</math> Channelit ADC<math>1</math>of Channels<math>10</math>Channel10Channels<math>10</math>Channel0MP<math>3</math><math>4</math> ProtectionRead and Write Protection (RDP/WRP), Memory Encr Protection, Secure BootLQFP32LQFP32</td>	eviceN32G401K6Q7N32G401K8Q7pacity (KB)3264apacity (KB)88FrequencyARM Cortex-M4F @g Conditions2.4~3.6V/g Conditions2.4~3.6V/General2Advanced2Basic2LPTIM2I2S2I2C2UART2EPER2PIO25+1DMA10Channelof Channels10ChannelOMP2ProtectionRead and Write Protection (RDP/W Protection, Protection, IOFP32	eviceN32G401K6Q7N32G401K8Q7N32G401C6Q7pacity (KB) $32$ $64$ $32$ apacity (KB) $8$ $8$ $8$ SrequencyARM Cortex-M4F @.72MHz, 90DMIFg Conditions $2.4 \sim 3.6 V/-40 \sim 105 °C$ General $4$ Advanced $2^{(1)}$ Basic $1$ LPTIM $1$ SPI $2$ I2S $2$ UART $2$ USART $2$ EPER $1$ of Channels $8$ Channelit ADC $1$ of Channels $10$ Channel10Channels $10$ Channel0MP $3$ $4$ ProtectionRead and Write Protection (RDP/WRP), Memory Encr Protection, Secure BootLQFP32LQFP32			

Table 2-2 N32G40	Series Resource	<b>Configuration (2)</b>
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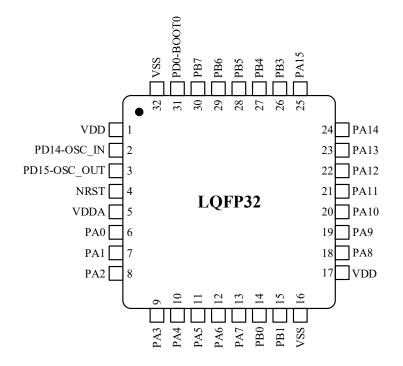
Note: (1) Timer1 supports 4 channels and 8 complementary output, Timer8 supports 3 channels and 6 complementary output



## **3** Packages

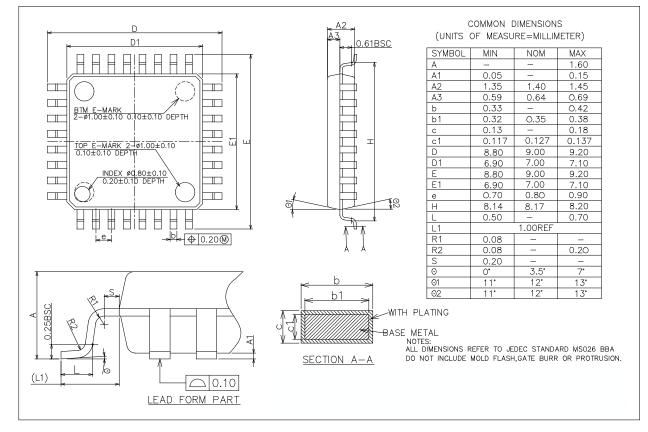
## 3.1 LQFP32(7mm x 7mm) Package

### 3.1.1 LQFP32 Pin Assignment



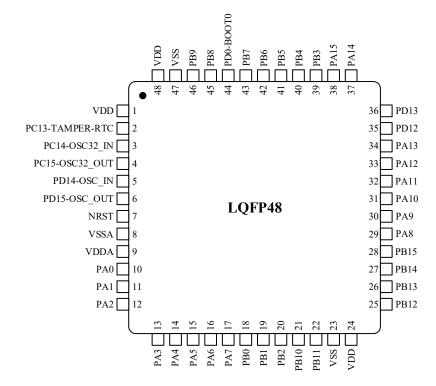


#### 3.1.2 LQFP32 Package Dimensions



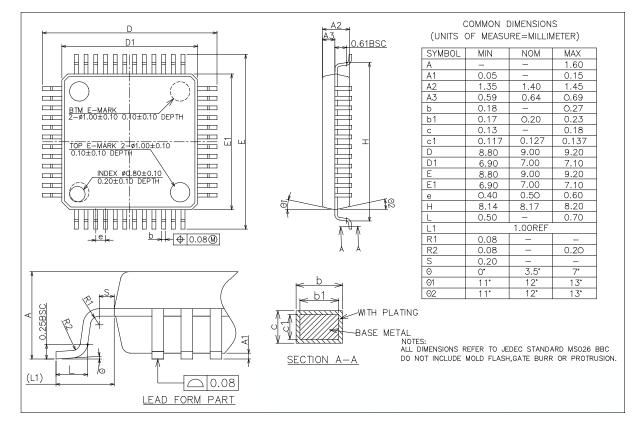
### 3.2 LQFP48(7mm x 7mm) Package

### 3.2.1 LQFP48 Pin Assignment





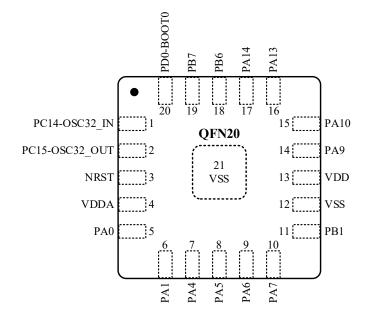
#### 3.2.2 LQFP48 Package Dimensions





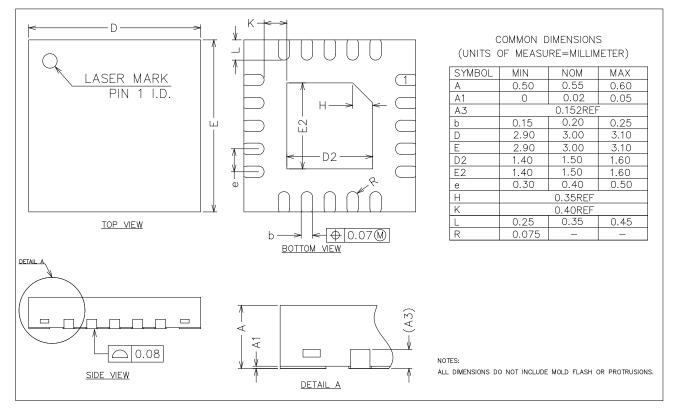
### 3.3 QFN20(3mm x 3mm) Package

### 3.3.1 QFN20 Pin Assignment



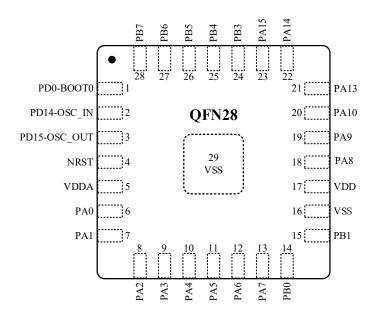


#### 3.3.2 QFN20 Package Dimensions



### 3.4 QFN28(4mm x 4mm) Package

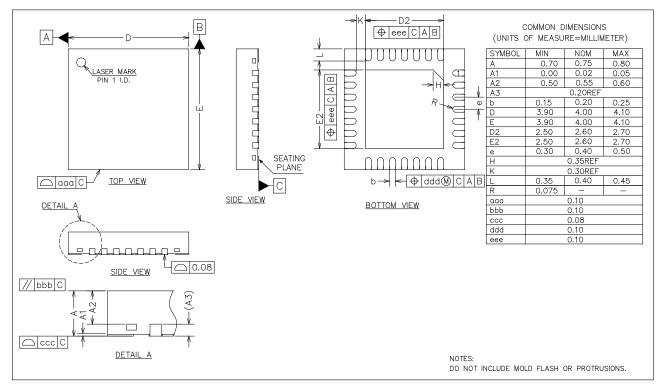
#### 3.4.1 QFN28 Pin Assignment



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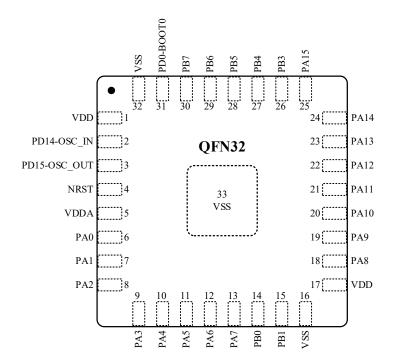


#### 3.4.2 QFN28 Package Dimensions



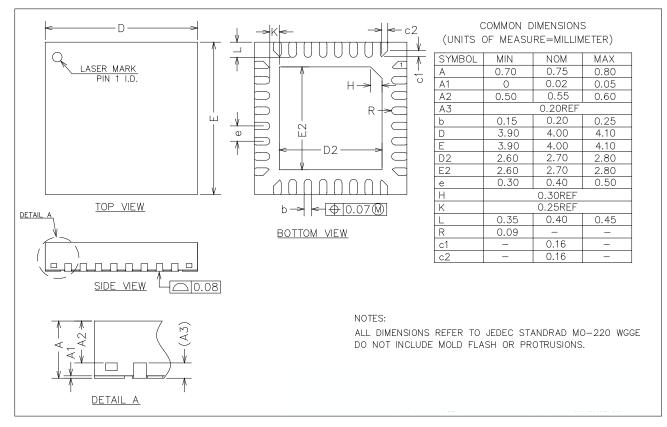
### 3.5 QFN32(4mm x 4mm) Package

### 3.5.1 QFN32 Pin Assignment



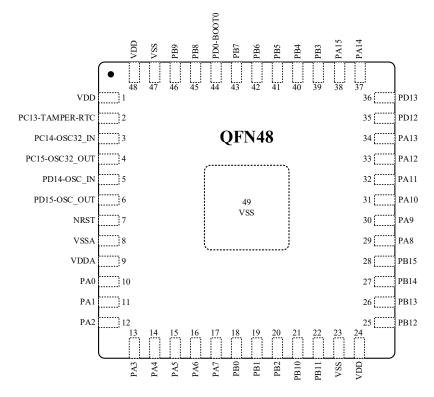


### 3.5.2 QFN32 Package Dimensions



### 3.6 QFN48(6mm x 6mm) Package

#### 3.6.1 QFN48 Pin Assignment

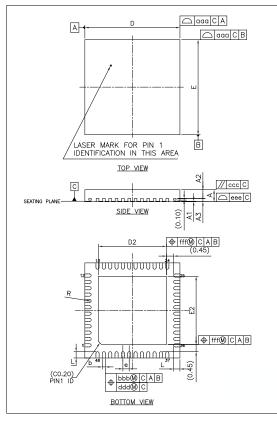


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#### 3.6.2 **QFN48** Package Dimensions



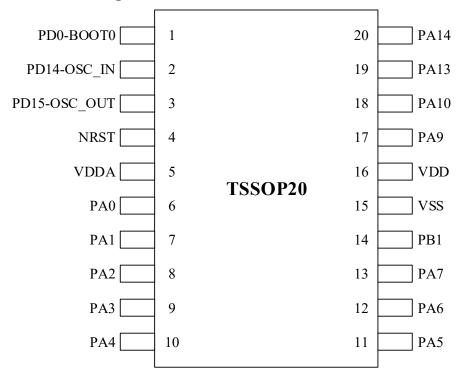
Item		Symbol	MIN.	NOM.	MAX.
total height		A	0.70	0.75	0.80
stand off		A1	0.00	0.02	0.05
mold thickness		A2	0.50	0.55	0.60
leadframe thickness		A3	0.20 REF.		
lead width		ь	0.15	0.20	0.25
	х	D	5.90	6.00	6.10
package size	Y	Е	5.90	6.00	6.10
E-PAD size	х	D2	4.20	4.30	4.40
E-PAD size	Y	E2	4.20	4.30	4.40
lead length	L	0.30	0.40	0.50	
lead pitch	e	0.40 bsc			
lead arc	R	0.075			
Package profile of a sur	aaa	0.10			
Lead position	bbb	0.07			
Paralleliam	ccc	0.10			
Lead position		ddd	0.05		
Lead profile of a surface	eee	0.08			
Epad position	fff	0.10			

#### NOTES:

ALL DIMENSIONS REFER TO JEDEC STANDARD MO-220 WJJE DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.

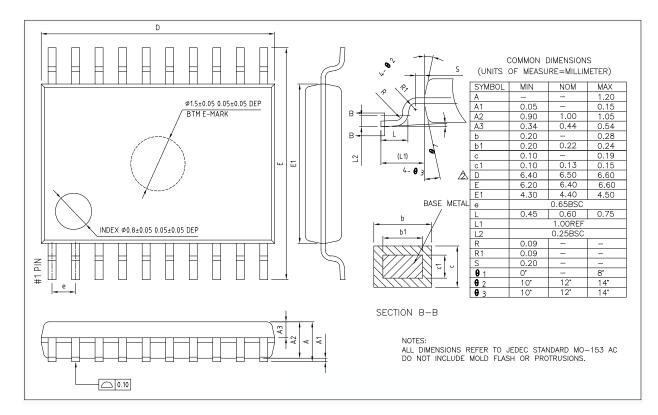
## 3.7 TSSOP20(6.5mm x 4.4mm) Package

#### 3.7.1 **TSSOP20** Pin Assignment





### 3.7.2 TSSOP20 Package Dimensions





# 4 Version History

Version	Date	Changes
V1.0.0	2023.06.06	Initial release



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## 5 Disclaimer

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