

N32G401x6/x8

Product Brief

N32G401 series uses 32-bit ARM Cortex-M4F core, operating frequency up to 72MHz, supporting floating-point unit and DSP instructions. The devices integrate up to 64KB of encrypted flash, and 8KB of SRAM. The series features rich of high-performance interfaces, including 1 built-in 12bit 4.2Msps ADC, 3 high-speed comparators, multi-channel U(S)ART, I2C, SPI and other communication interfaces.

Key Features

- **CPU Core**
 - 32-bit ARM Cortex-M4F with FPU, supports DSP instructions
 - Built-in 1KB instruction Cache, supports Flash accelerator unit for zero-wait program execution
 - Maximum frequency of 72MHz, 90DMIPS
- **Memories**
 - Up to 64KByte of embedded Flash memory
 - Supporting encrypted memory function, partition management and data protection
 - 10,000 erase/write cycles and 10 years data retention
 - Up to 8KByte on-chip SRAM, retained in Stop2 mode, can be configured to retention in Standby mode
- **Low Power Management**
 - Sleep mode: The CPU is stopped; all peripherals are active and can wake up the CPU
 - Stop0 mode: PLL, HSI and HSE are disabled, LSE/LSI can keep running, RTC can keep running, SRAM and all register contents retained, all IOs retained.
 - Stop2 mode: PLL, HSI and HSE are disabled, LSE/LSI can keep running, RTC can keep running, SRAM and all register contents retained, all IOs retained, CPU register and backup register contents retained.
 - Standby mode: Internal voltage regulator is turned off, PLL, HSI and HSE are disabled, LSE/LSI can keep running, RTC and IWDG can keep running, SRAM can be configured to retention, all IOs retained.
- **High-performance Analog Interfaces**
 - 1x 12bit ADC with 4.2Msps
 - Configurable as 12/10/8/6 bits mode
 - Up to 16 external single-ended input channels, 3 internal single-ended input channels
 - Support differential mode
 - 3x COMPs with internal 64-level adjustable comparison reference
- **Clock**
 - HSE: 4MHz~32MHz high-speed external crystal oscillator
 - LSE: 32.768KHz low-speed external crystal oscillator
 - HSI: High-speed internal RC 8MHz
 - LSI: Low speed internal RC 40KHz
 - Built-in high-speed PLL

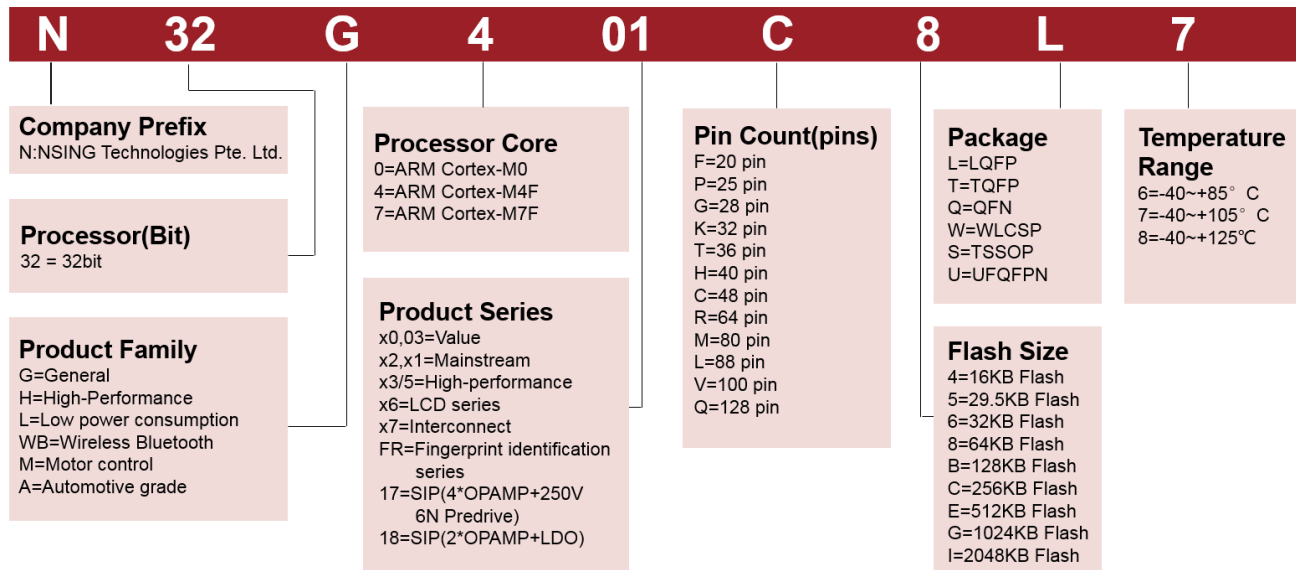
- MCO: Support 2-channels clock output, configurable as SYSCLK, HSI, HSE, LSI, LSE, and PLL divisional output
- **Reset**
 - Supports power-on/power-down/external pin reset.
 - Supports watchdog reset, software reset.
 - Supports programmable voltage detection.
- **GPIO**
 - Up to 39+1 GPIOs
- **Communication Interfaces**
 - 4x U(S)ART interfaces
 - 2x USART interfaces (support ISO7816, IrDA, LIN)
 - 2x UART interfaces
 - 2x SPI interfaces
 - Speed up to 28Mbps (without CRC) and 20Mbps (with CRC) in master mode.
 - Speed up to 32Mbps in slave mode.
 - Supports I2S
 - 2x I2C interfaces (Master/Slave) with speed up to 1 MHz, support dual address responses in slave mode
- **DMA controller**
 - 1 x high-speed DMA controller supports 8 channels, with arbitrarily configurable channel sources and destination addresses
- **RTC real-time clock**
 - Supports leap year calendar, alarm event, periodic wake up
 - Supports internal and external clock calibration
- **Beeper**
 - Supports complementary output, 12mA output driving capability
- **Timer**
 - 2x 16-bit advanced timers with maximum control precision of 7.8ns
 - Supports input capture, complementary output, quadrature encoder input, etc.
 - Each timer has four independent channels, of which Timer1 supports 8 channels complementary PWM output, Timer8 supports 6 channels complementary PWM output
 - 4x 16-bit general purpose timers
 - Each timer has 4 independent channels.
 - Supports input capture/output comparison /PWM output.
 - 1x 16-bit basic timer
 - 1x 16-bit low power timer

- Supports single pulse and double pulse counting function.
- Supports operating in STOP2 mode.
- 1x 24-bit SysTick timer
- 1x 14-bit Window Watchdog (WWDG)
- 1x 12-bit Independent Watchdog (IWDG)
- **Programming Methods**
 - Supports SWD/JTAG debugging interface.
 - Supports UART Bootloader
- **Security Features**
 - Flash storage encryption, Multi-user partition Management Unit (MMU)
 - CRC16/32 computation
 - Supports write protection (WRP), multiple level (L0/L1/L2) of read protection (RDP)
 - Supports secure boot, encrypted program download, secure firmware updates.
 - Supports external clock failure detection, anti-tamper detection.
- **96-bit UID and 128-bit UCID**
- **Operating Conditions**
 - Operating voltage range: 2.4V~3.6V
 - Operating temperature range: -40°C ~ 105°C
 - ESD: ±4KV (HBM model), ±2KV (CDM model)
- **Packages**
 - LQFP32(7mm x 7mm)
 - LQFP48(7mm x 7mm)
 - QFN20(3mm x 3mm)
 - QFN28(4mm x 4mm)
 - QFN32(4mm x 4mm)
 - QFN48(6mm x 6mm)
 - TSSOP20(6.5mm x 4.4mm)
- **Ordering Information**

Reference	Part Number
N32G401x6	N32G401C6L7, N32G401K6L7 N32G401C6Q7, N32G401K6Q7, N32G401G6Q7, N32G401F6Q7, N32G401F6S7-1
N32G401x8	N32G401C8L7, N32G401K8L7 N32G401C8Q7, N32G401K8Q7, N32G401G8Q7, N32G401F8Q7, N32G401F8S7-1

1 Naming Convention

Figure 1-1 N32G401 Series Part Naming Conversion



2 Product Configurations

Table 2-1 N32G401 Series Resource Configuration (1)

Device		N32G401F6S7-1	N32G401F8S7-1	N32G401F6Q7	N32G401F8Q7	N32G401G6Q7	N32G401G8Q7
Flash capacity (KB)		32	64	32	64	32	64
SRAM capacity (KB)		8	8	8	8	8	8
CPU frequency		ARM Cortex-M4F @72MHz, 90DMIPS					
Operating Conditions		2.4~3.6V/-40~105℃					
Timers	General	4					
	Advanced	2 ⁽¹⁾					
	Basic	1					
	LPTIM	1					
Communication Interfaces	SPI	2					
	I2S	2					
	I2C	2					
	UART	1				2	
	USART	2					
BEEPER		1					
GPIO		15+1				23+1	
DMA		1					
Number of Channels		8 Channel					
12bit ADC		1		1		1	
Number of Channels		9Channel		7Channel		10Channel	
COMP		0		3			
Security Protection		Read and Write Protection (RDP/WRP), Memory Encryption, Partition Protection, Secure Boot					
Package		TSSOP20		QFN20		QFN28	

Note: ⁽¹⁾ Timer1 supports 4 channels and 8 complementary output, Timer8 supports 3 channels and 6 complementary output.

Table 2-2 N32G401 Series Resource Configuration (2)

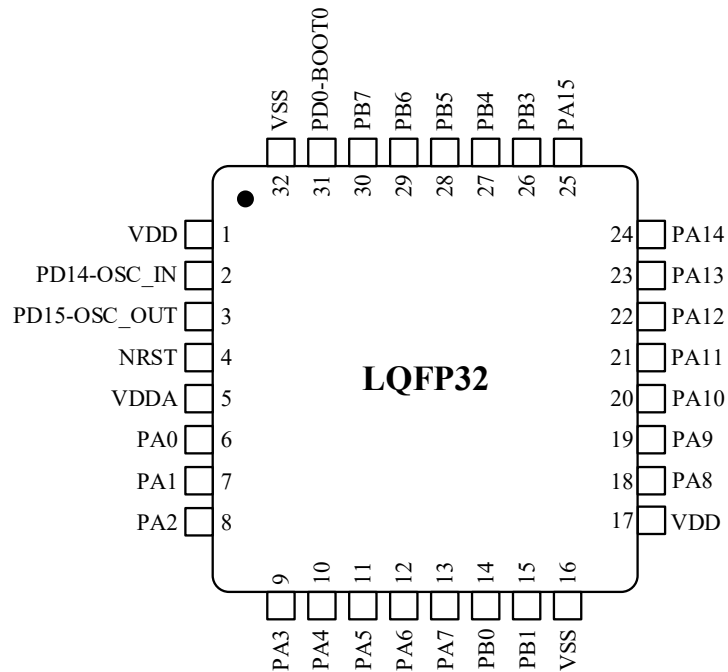
Device		N32G401K6L7 N32G401K6Q7	N32G401K8L7 N32G401K8Q7	N32G401C6L7 N32G401C6Q7	N32G401C8L7 N32G401C8Q7
Flash capacity (KB)		32	64	32	64
SRAM capacity (KB)		8	8	8	8
CPU frequency		ARM Cortex-M4F @72MHz, 90DMIPS			
Operating Conditions		2.4~3.6V/-40~105℃			
Timers	General	4			
	Advanced	2 ⁽¹⁾			
	Basic	1			
	LPTIM	1			
Communication Interfaces	SPI	2			
	I2S	2			
	I2C	2			
	UART	2			
	USART	2			
BEEPER		1			
GPIO		25+1		39+1	
DMA		1			
Number of Channels		8 Channel			
12bit ADC		1		1	
Number of Channels		10Channel		16Channel	
COMP		3			
Security Protection		Read and Write Protection (RDP/WRP), Memory Encryption, Partition Protection, Secure Boot			
Package		LQFP32 QFN32		LQFP48 QFN48	

Note: ⁽¹⁾ Timer1 supports 4 channels and 8 complementary output, Timer8 supports 3 channels and 6 complementary output

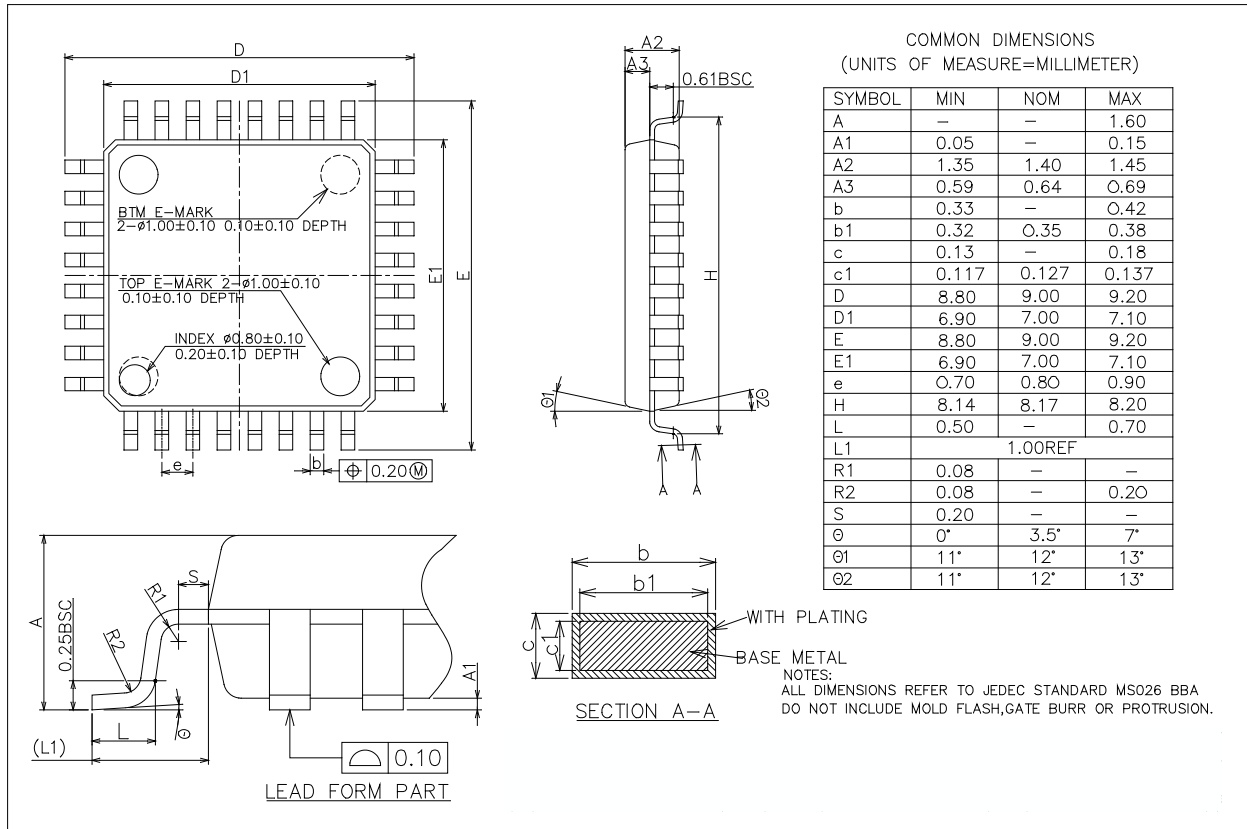
3 Packages

3.1 LQFP32(7mm x 7mm) Package

3.1.1 LQFP32 Pin Assignment

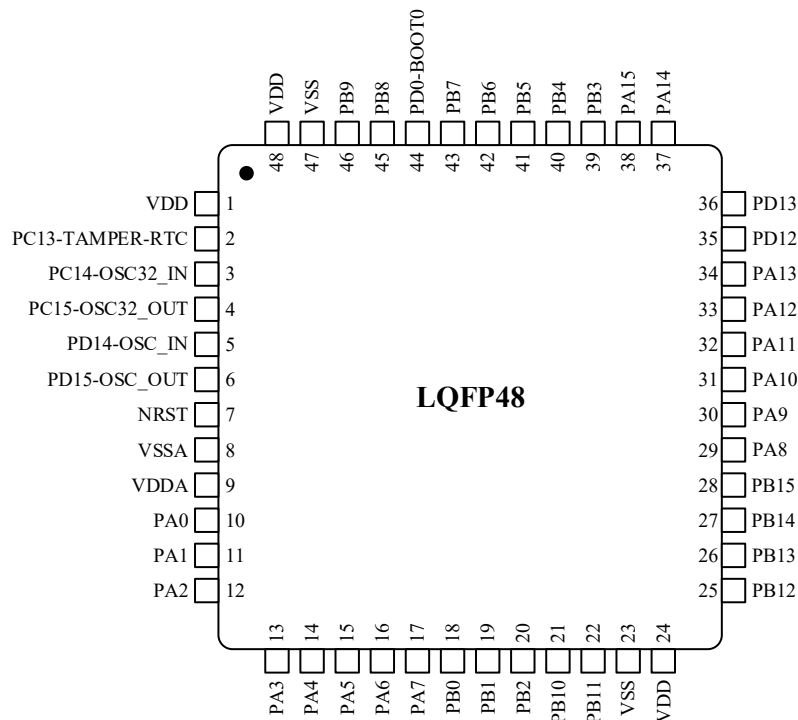


3.1.2 LQFP32 Package Dimensions

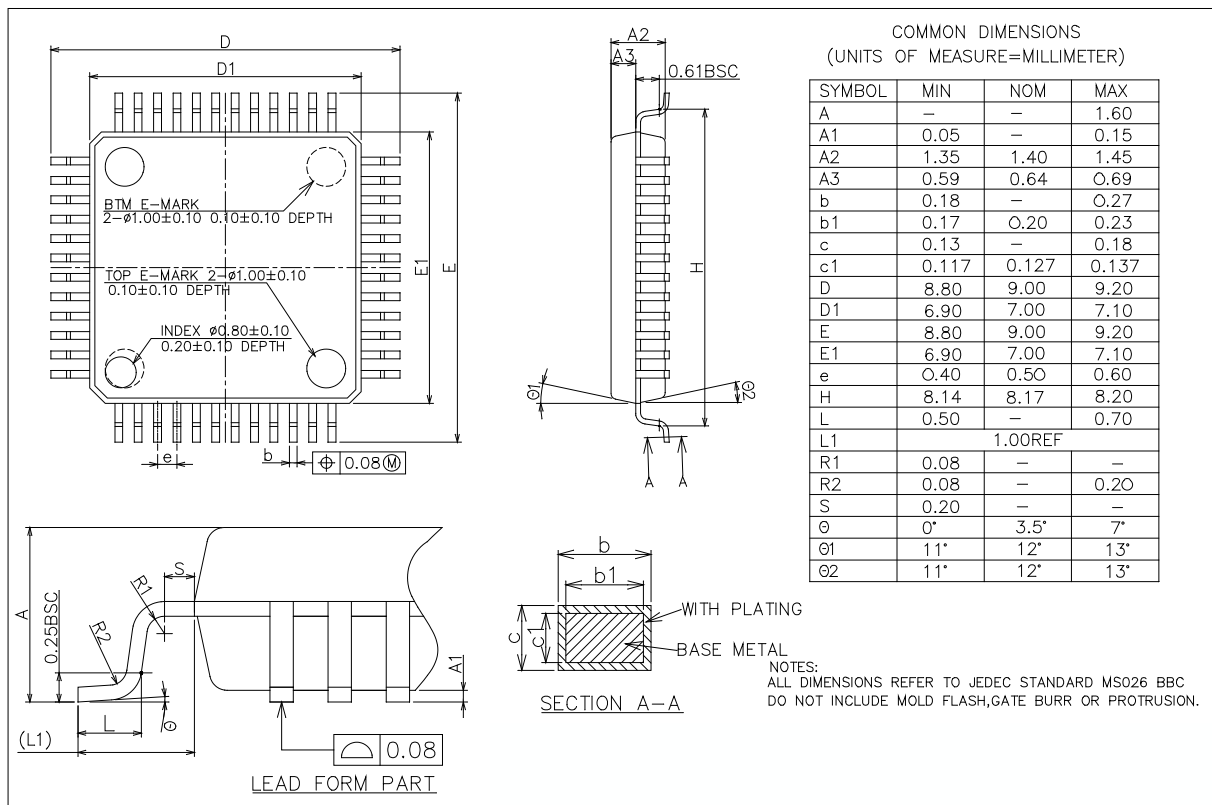


3.2 LQFP48(7mm x 7mm) Package

3.2.1 LQFP48 Pin Assignment

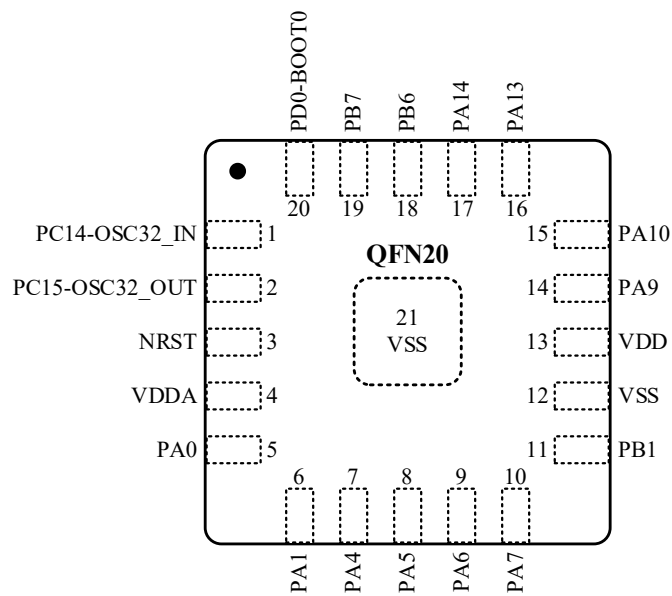


3.2.2 LQFP48 Package Dimensions

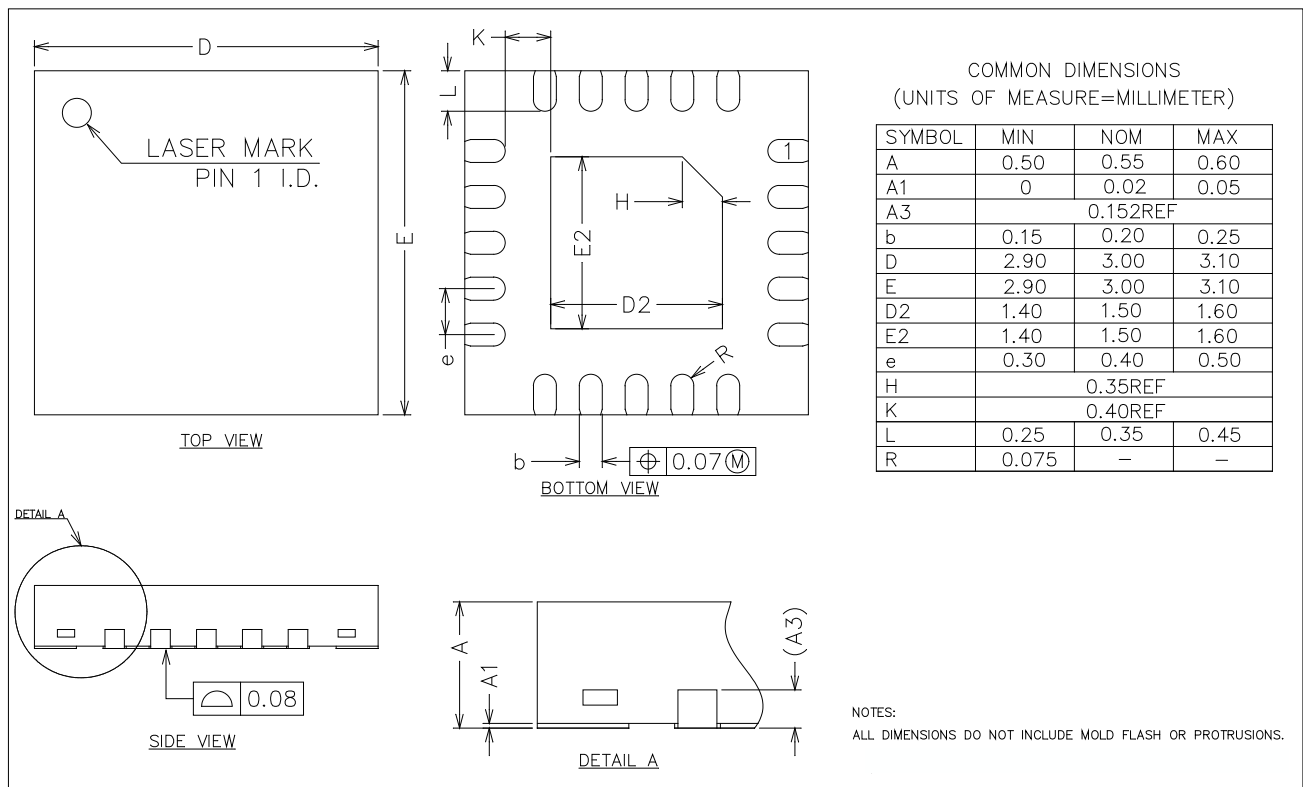


3.3 QFN20(3mm x 3mm) Package

3.3.1 QFN20 Pin Assignment

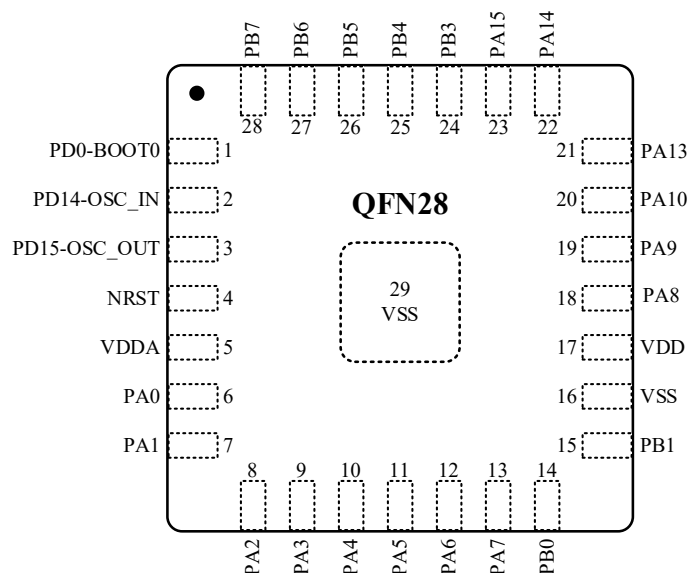


3.3.2 QFN20 Package Dimensions

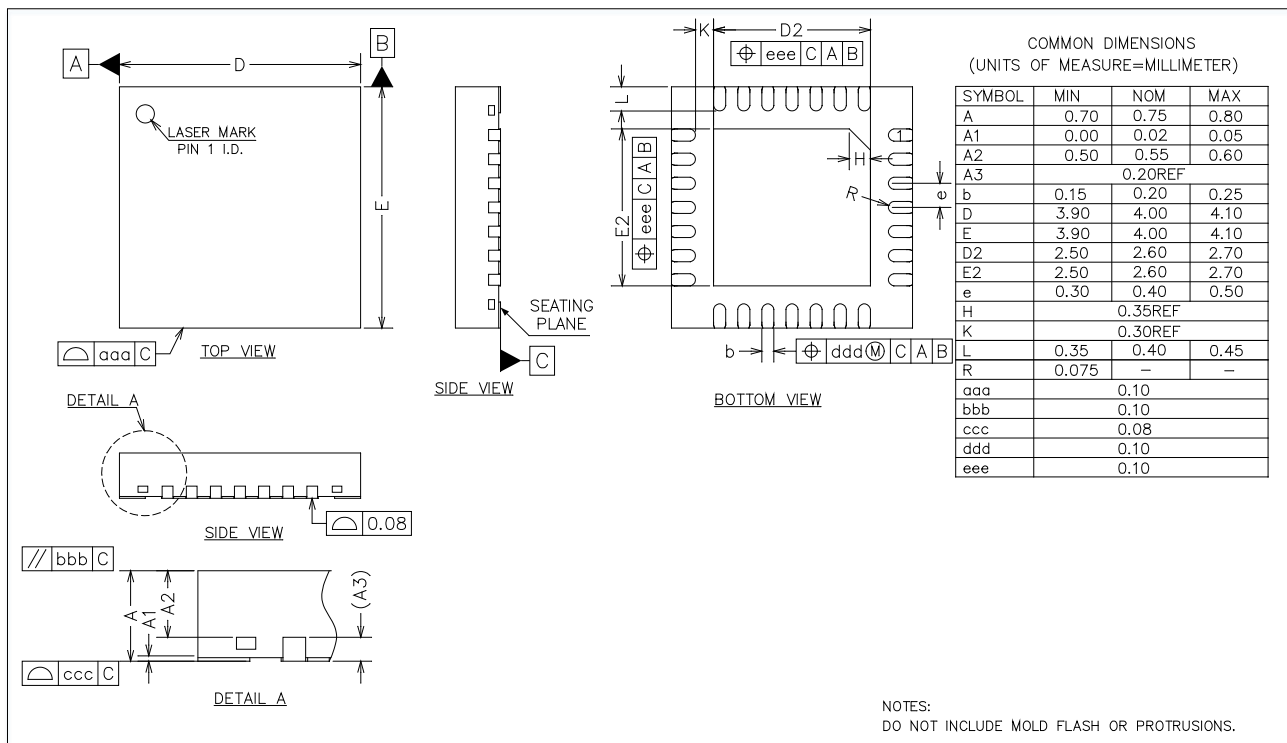


3.4 QFN28(4mm x 4mm) Package

3.4.1 QFN28 Pin Assignment

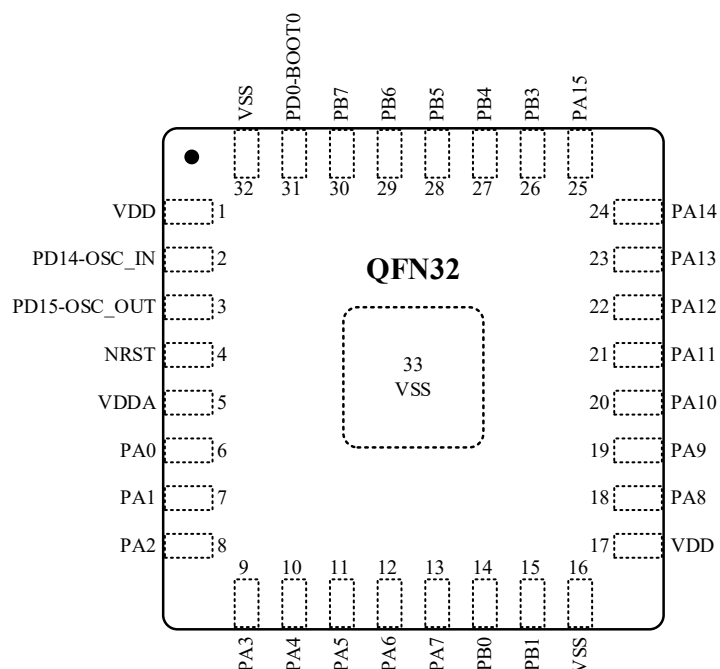


3.4.2 QFN28 Package Dimensions

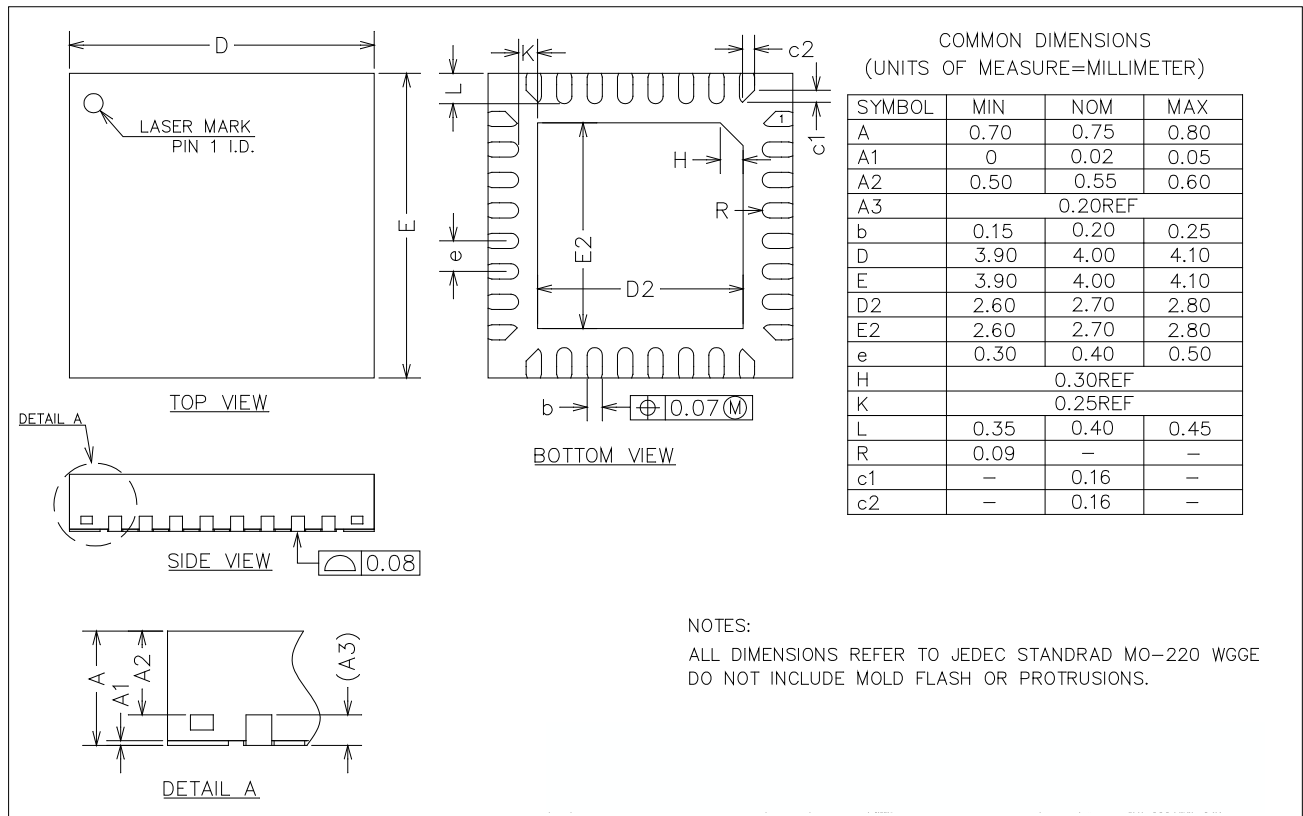


3.5 QFN32(4mm x 4mm) Package

3.5.1 QFN32 Pin Assignment

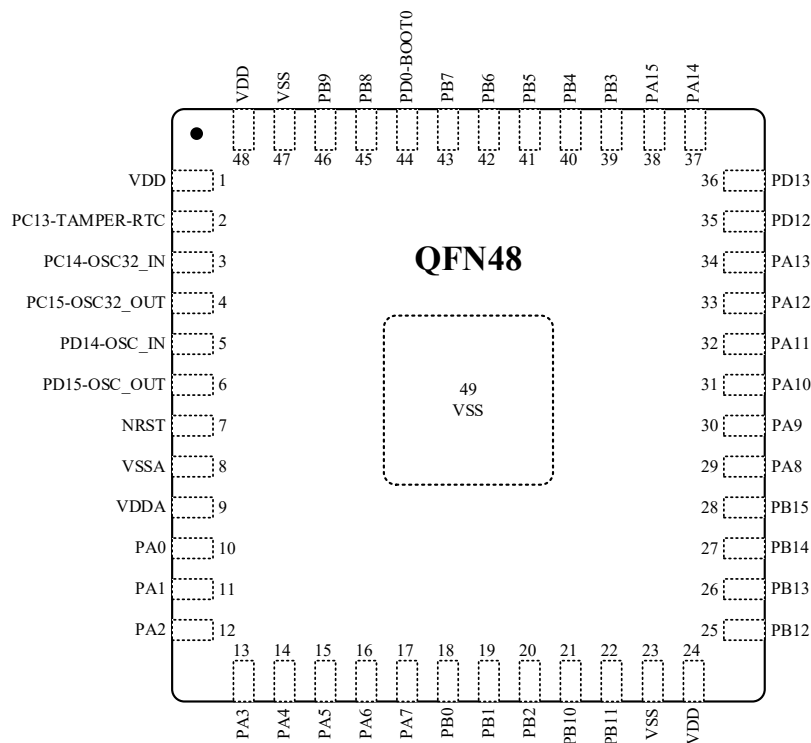


3.5.2 QFN32 Package Dimensions

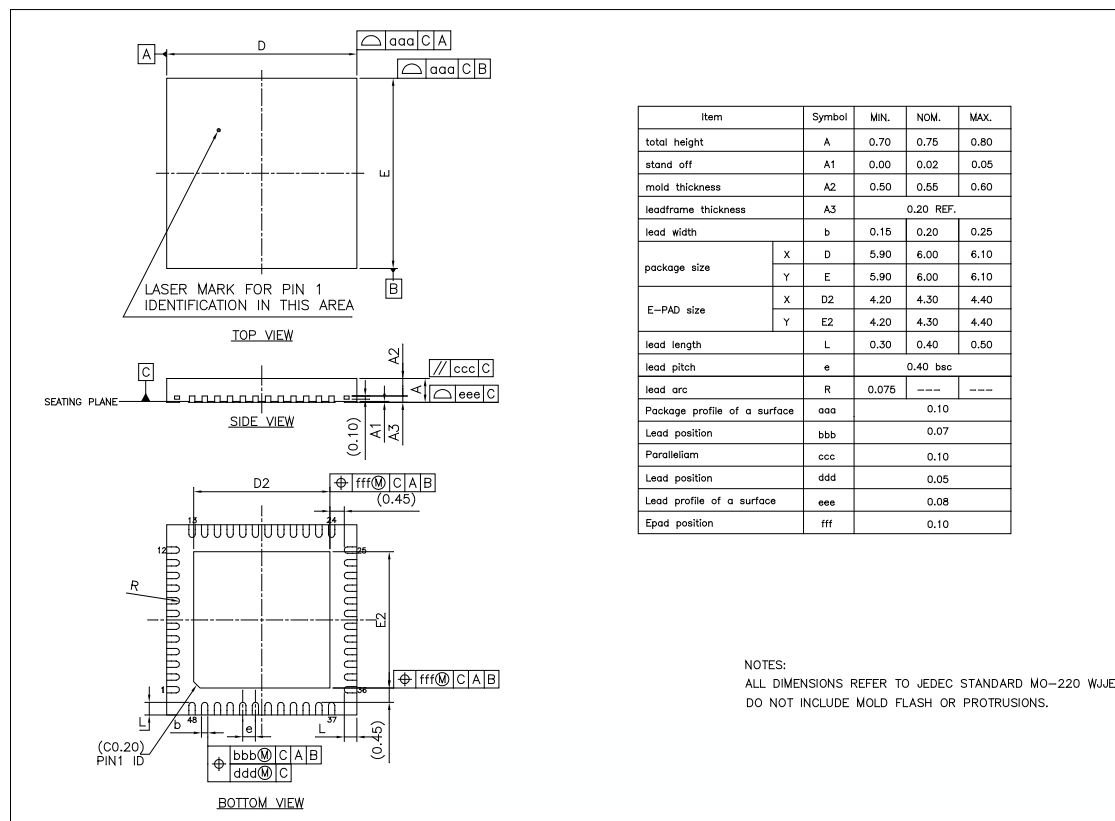


3.6 QFN48(6mm x 6mm) Package

3.6.1 QFN48 Pin Assignment

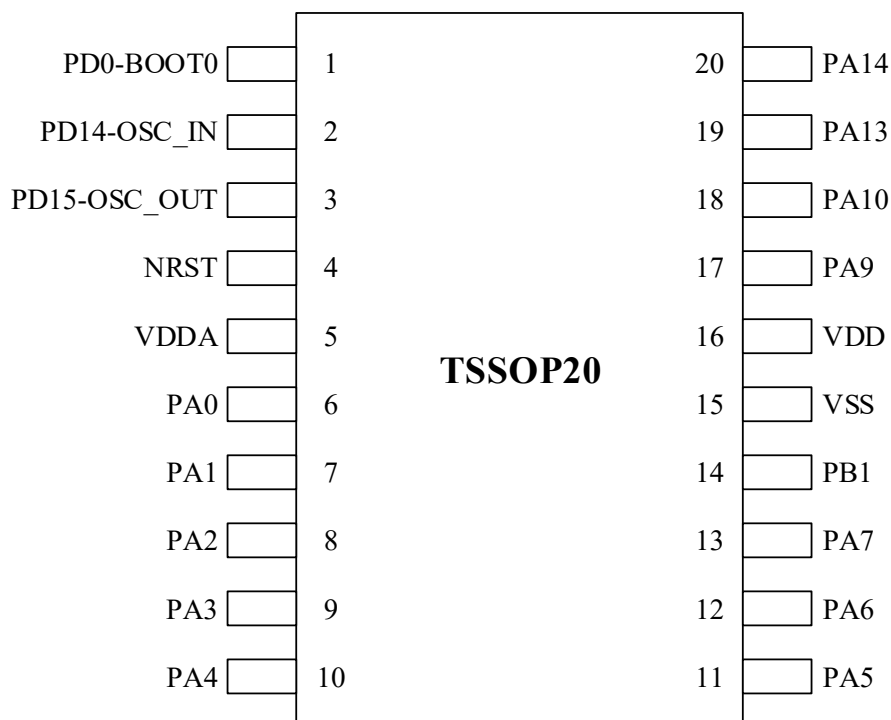


3.6.2 QFN48 Package Dimensions

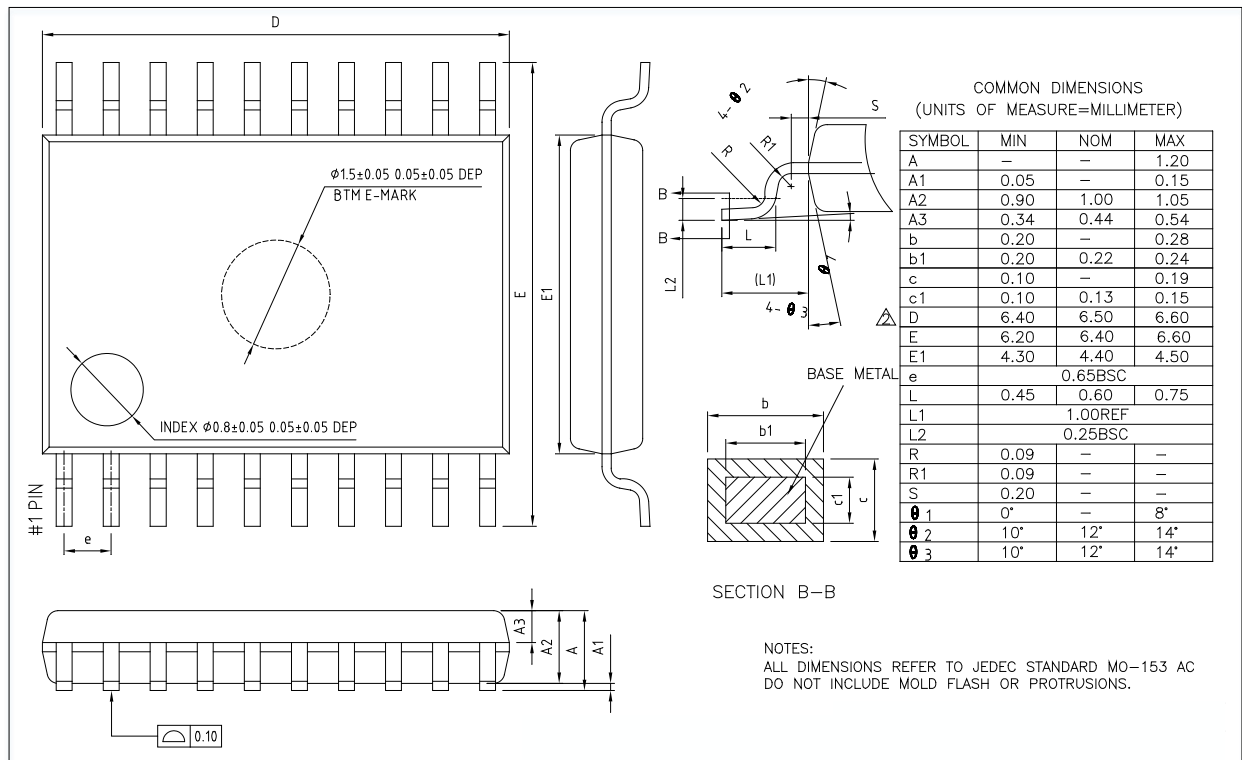


3.7 TSSOP20(6.5mm x 4.4mm) Package

3.7.1 TSSOP20 Pin Assignment



3.7.2 TSSOP20 Package Dimensions



4 Version History

Version	Date	Changes
V1.0.0	2023.06.06	Initial release

5 Disclaimer

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