N32G430 Series

Errata Sheet

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Contents

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1 Errata List

Table 1-1 Overview of Errata

Errata Link		Chip Revision	
		C	D
Ch 2: **Error! Reference source not found.**	2.1: **Error! Reference source not found.**	●	-
Ch 3: **Error! Reference source not found.**	3.1: **Error! Reference source not found.** specific conditions	●	●
Ch 4: **Error! Reference source not found.**	4.1: **Error! Reference source not found.** 4.1.1: **Error! Reference source not found.**	●	●
Ch 5: **Error! Reference source not found.**	5.1: RTC automatic wake up	●	●
	5.2: The RTC wakeup event is generated before the chip enters STANDBY and cannot wake up	●	-
	5.3: The RTC calendar function cannot be initialized multiple times within 1 second	●	-
	5.4: **Error! Reference source not found.**	●	-
	5.5: The shift operation of the RTC on the subsecond causes the current wakeup time is inaccurate	●	●
	5.6: The **Error! Reference source not found.**ed	●	●
Ch 6: GPIO and AFIO	6.1: IO appeared burr during power-on	●	-
Ch 7: Controller area network(CAN)	7.1: CAN active error	●	-

Notes:

（1） ●: problem present

（2） -: fixed

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2 Power Control (PWR)

2.1 Cannot Reset the Chip by Pressing NRST Button in DEBUG STOP2 Mode

Description

When the DBG_CTRL.STOP bit is set to 1 and the chip enters the STOP2 mode, the chip cannot be reset by pressing the NRST button.

Workaround

Clear the DBG_CTRL.STOP bit before the chip enters STOP2 mode.

3 Timer (TIM)

3.1 TIM1/2/3/4/5/8 Cannot Generate Compare Events under Specific Conditions

Description

In edge-aligned mode, and up-counting PWM1 mode, when CCDATx shadow register value is greater than or equal to AR value in current PWM cycle, and if the CCDATx shadow register value is equal to 0 in the next PWM cycle. Then compare event will not be generated when the count value of counter is equal to the value of the CCDATx shadow register is 0.

Workaround

If it is not required that "the compare event is generated at the time when the count value = the shadow register of the compare value =0", the compare event can be generated through another channel.

4 Serial Peripheral Interface (SPI)

4.1 I2S Interface

4.1.1 PCM Long Frame Mode

Description

When I2S is operating in master mode, PCM long frame mode, and the data format is directly set to "32bit" or is extended from "16bit to 32bit", the WS (word select) signal occurs every 16bits instead of every 32bits.

Workaround

If I2S must operate in master mode and use long frame mode, it is recommended to use only the 16-bit data mode to ensure proper WS signal alignment.

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5 Real Time Clock (RTC)

5.1 The First Automatic Wakeup Time of the RTC Is Abnormal

Description

After setting up the RTC calendar and configuring the automatic wakeup function, the time from enabling automatic wake-up to the first wakeup is smaller than the time represented by the wakeup automatic reload value. But the subsequent automatic wakeup time is normal.

Workaround

Ignore the first wakeup.

5.2 The Chip Cannot Wakeup if the RTC Wakeup Event Occurs before Entering STANDBY Mode

Description

Before the chip enters STANDBY mode, if an RTC wakeup event occurs, the chip will not be able to be waken up after entering STANDBY mode.

Workaround

None.

5.3 The RTC Calendar Function Prohibits Multiple Initializations within 1 Second

Description

Multiple initializations of the RTC calendar function within 1 second will result in the inability to generate RTC alarm interrupts.

Workaround

The interval between two initializations of the RTC calendar function should be more than 1 second.

5.4 The RTC Incorrectly Triggers the TISOVF Flag

Description

When the system wakes up from STANDBY mode or reset by IWDG timeout, TISOVF flag in RTC may be set incorrectly.

Workaround

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Before entering STANDBY mode or when the system is reset by IWDG timeout, when the SHOPF flag is 0, configure RTC_SCTRL.SUBF[14:0] register once, and the SHOPF flag will be set to 1. When the SHOPF flag is 0 again, it should configure RTC_SCTRL.SUBF[14:0] register for the second time. This will solve the issue.

Note: that NRST cannot be triggered during above process.

5.5 The Shift Operation of the RTC on the Sub-Seconds Causes Inaccurate Wake-up Time

Description

When the RTC is configured as periodic wake up, performing the shift operationon sub-seconds before triggering the periodic wakeup will cause the current wakeup time to be inaccurate. And the subsequent wakeup time will be normal.

Workaround

No solution is provided for this issue.

5.6 RTC_DATE Register Locked

Description

- Before the system software reset, if the RTC_DATE register is not read after reading the RTC_SUBS or RTC_TSH shadow register, and after the system software reset, if the RTC is initialized without configuring or reading the RTC_DATE register, then the RTC_DATE register will revert to its default value.
- When reading the calendar, after reading the RTC_SUBS or RTC_TSH shadow register, the value of the RTC_DATE register remains unchanged.

Workaround

- Read the RTC_DATE register before initializing the RTC.
- After reading the RTC_SUBS or RTC_TSH shadow register, read the RTC_DATE register.

6 GPIO and AFIO

6.1 Glitchs Occur on the IO during Chip Power-on

Description

When the MCU is powered on, some IOs will have glitches appeared.

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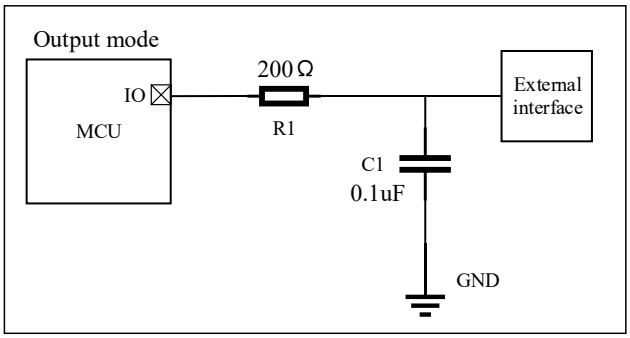
Workaround

When IO is used as an input, glitches have no effect on the MCU; When IO is used as an output, an external 200Ohm resistor and a 0.1uF capacitor are applied for filtering to solve the issue.



7 Controller Area Network (CAN)

7.1 CAN Active Error

Description

When the CAN is operating in normal mode, and the CAN bit is hard synchronized, if the baud rate deviation of other nodes on the bus is too large (approaching or exceeding the synchronization segment) compared to the CAN module, the CAN module is prone to generate the active error.

Workaround

None.

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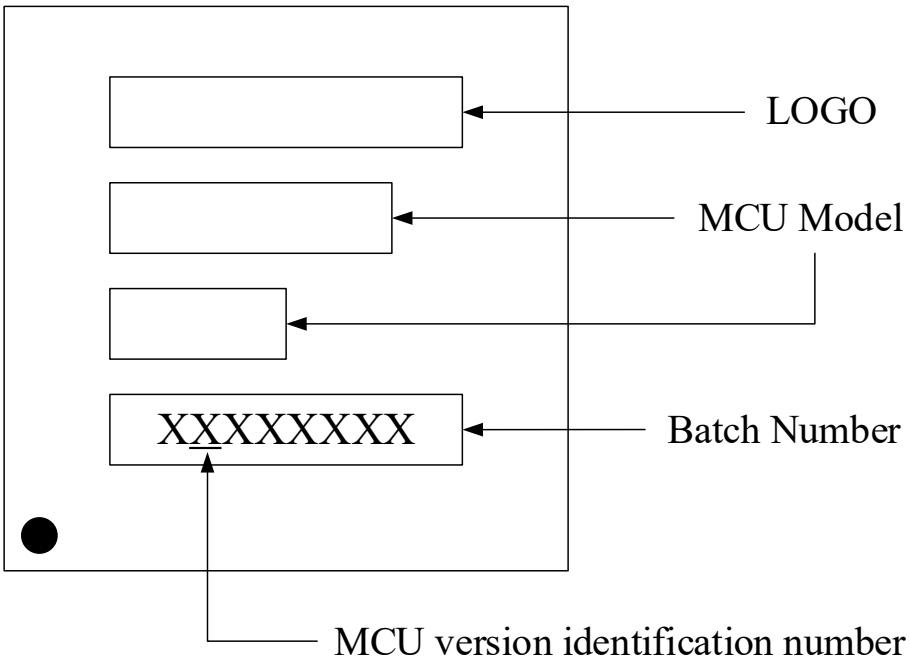
8 Chip Marking and Revision Description



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9 Version History

Version	Date	Changes
V1.0.0	2022.5.12	Initial release
V1.1.0	2022.7.19	Added Ch 6
V1.2.0	2023.3.21	1) Added Ch 7, CAN active error 2) Modified Ch 5.2, wakeup event instead of tamper event 3) Added Ch 5.4, the RTC set the TISOVF flag by mistake 4) Added Ch 5.5, the shift operation of the RTC on the sub-second causes inaccurate wake-up time
V1.3.0	2023.5.9	Added Ch 5.6

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