

N32G430x6/x8

Product Brief

The N32G430 series adopts a 32-bit ARM Cortex-M4F core with a maximum operating frequency of 128MHz. It supports floating-point calculations and DSP instructions. It integrates up to 64KB embedded encrypted Flash, 16KB SRAM, and a rich set of high-performance analog devices, including a built-in 12bit 4.7MSPS ADC and 3 high-speed comparators. It also integrates multiple digital communication interfaces such as U(S)ART, I2C, SPI, and CAN.

Key Features

- **CPU core**
 - 32-bit ARM Cortex-M4 + FPU, supporting DSP instructions
 - Built-in 1KB instruction Cache supports Flash acceleration unit for zero-wait program execution.
 - Maximum frequency of 128MHz, 160DMIPS
- **Memories**
 - Up to 64KByte of embedded Flash memory, supports encrypted storage function, Multi-user partition management and data protection, 100,000 erase/write cycles, 10 years data retention.
 - Up to 16KByte of on-chip SRAM, retained in Stop2 mode, configurable to be retained in Standby mode.
- **Power Consumption Mode**
 - Supports Run, Sleep, Stop0, Stop2, Standby mode.
- **High-Performance Analog Interface**
 - 1x 12bit 4.7MSPS ADC, configurable to 12/10/8/6 bits, up to 16 external single-ended input channels, 3 internal single-ended input channels, supporting differential mode.
 - 3x high-speed comparators with built-in 64-level adjustable reference.
- **Clock**
 - HSE: 4MHz~32MHz High-speed external crystal
 - LSE: 32.768KHz Low-speed external crystal
 - HSI: Internal high-speed RC 8MHz
 - LSI: Internal low speed RC 40KHz
 - Built-in high speed PLL
 - MCO: Support 2-channel clock output, configurable to output SYSCLK, HSI, HSE, LSI, LSE, and PLL clock with prescaler.
- **Reset**
 - Supports power-on/power-down/external pin reset.
 - Support watchdog reset and software reset.
 - Support programmable voltage detection.
- **Maximum of 39+1 GPIOs.**
- **Communication interface**

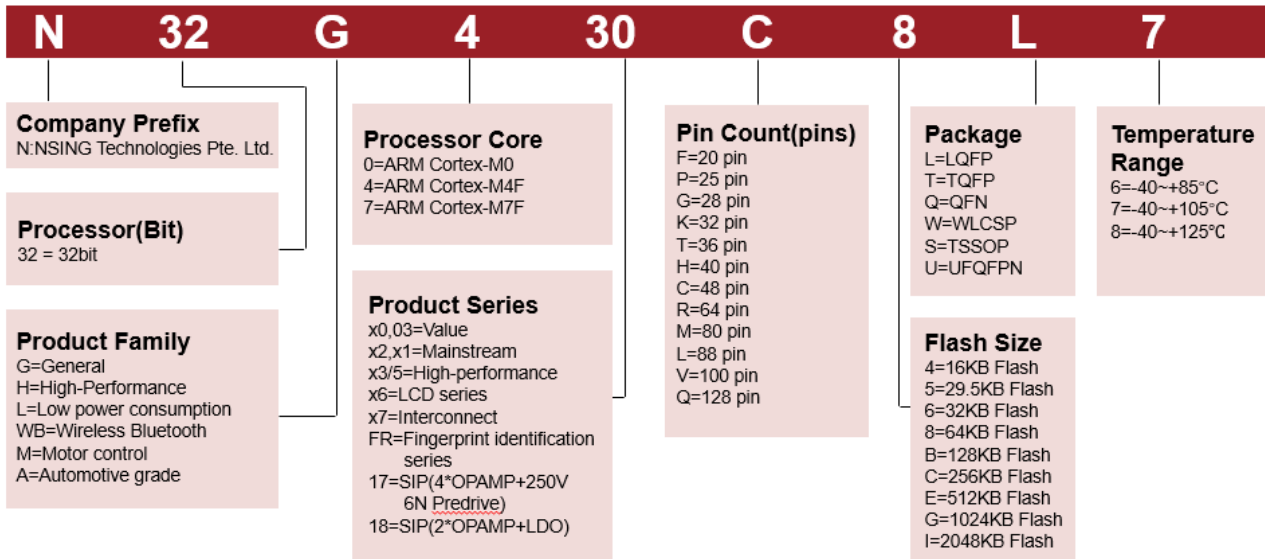
- 4x U(S)ART interfaces, including 2x USART interfaces (supporting ISO7816, IrDA, LIN) and 2x UART interfaces.
- 2x SPI interfaces, maximum master mode rate up to 28Mbps (non-CRC mode), 20Mbps (CRC mode), maximum slave mode rate up to 32Mbps, support I2S communication.
- 2x I2C interfaces, maximum rate up to 1 MHz, configurable master/slave mode, supporting dual-address response in slave mode.
- 1x CAN 2.0A/B bus interface, maximum rate up to 1Mbps
- **1x high-speed DMA controller, supporting 8 channels with arbitrary source and destination addresses.**
- **RTC real-time clock, supporting leap year, perpetual calendar, alarm clock event, periodic wake up, support internal and external clock calibration.**
- **1x Beeper, support complementary output, 12mA output drive capability.**
- **Timing counter**
 - 2x 16-bit advanced timer counters, support input capture, complementary output, orthogonal encoding input, maximum control precision 7.8ns; Each timer has four independent channels, Timer1 supports 4 channels and 8 complementary PWM output, Timer8 supports 3 channels and 6 complementary PWM output.
 - 4x 16-bit general-purpose timer, each with 4 independent channels, supporting input capture/output comparison /PWM output.
 - 1x 16-bit basic timer counter
 - 1x 16-bit low power timer counter, supporting dual-pulse counting function, can work in STOP2 mode.
 - 1x 24-bit SysTick
 - 1x 14-bit Window Watchdog (WWDG)
 - 1x 12-bit Independent Watchdog (IWDG)
- **Programming mode**
 - Support SWD/JTAG debugging interface.
 - Supports UART Bootloader
- **Security features**
 - Flash Storage encryption, Multi-user partition Management Unit (MMU)
 - CRC16/32 operation
 - Support write protection (WRP), multiple read protection (RDP) levels (L0/L1/L2)
 - Support safe start, program encryption download, security updates
 - Support external clock failure detection, tamper detection
- **96-bit UID and 128-bit UCID**
- **Operating conditions**
 - Operating voltage range: 2.4V~3.6V
 - Operating temperature range: -40°C ~ 105°C
 - ESD: ±4KV (HBM model), ±2KV (CDM model)
- **Packages**
 - LQFP32(7mm x 7mm)
 - LQFP48(7mm x 7mm)

- QFN20(3mm x 3mm)
- QFN28(4mm x 4mm)
- QFN32(4mm x 4mm)
- QFN48(6mm x 6mm)
- TSSOP20(6.5mm x 4.4mm)

● **Ordering information**

Reference	Part Number
N32G430x6	N32G430C6L7, N32G430K6L7 N32G430C6Q7, N32G430K6Q7, N32G430G6Q7, N32G430F6Q7, N32G430F6S7, N32G430F6S7-1
N32G430x8	N32G430C8L7, N32G430K8L7 N32G430C8Q7, N32G430K8Q7, N32G430G8Q7, N32G430F8Q7, N32G430F8S7, N32G430F8S7-1

1 Naming Convention



2 Product Configurations

Table 2-1 N32G430 Series Resource Configuration

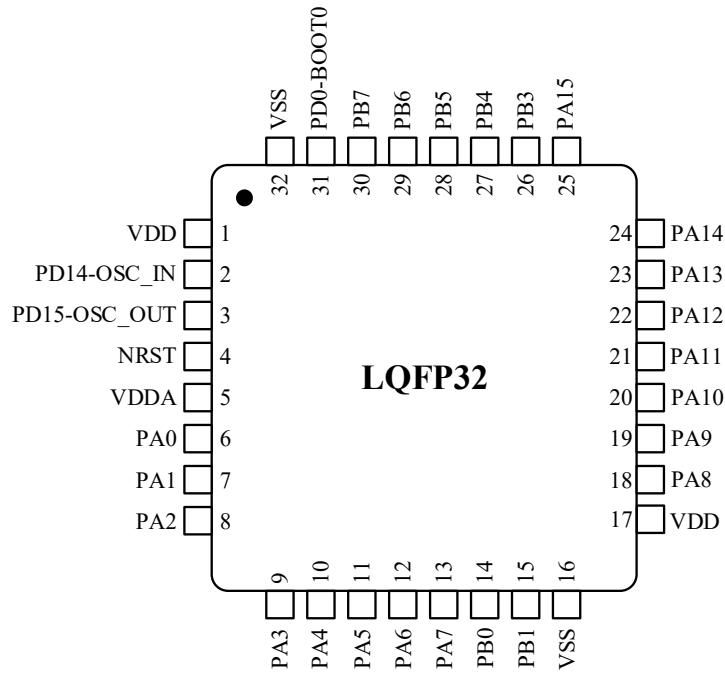
Part Number	N32G430F6S7 N32G430F6S7-1 ⁽¹⁾	N32G430F8S7 N32G430F8S7-1 ⁽¹⁾	N32G430F 6Q7	N32G430F8 Q7	N32G430G 6Q7	N32G430G 8Q7	N32G430K6L7 N32G430K6Q7	N32G430K8L7 N32G430K8Q7	N32G430C6L7 N32G430C6Q7	N32G430C8L7 N32G430C8Q7	
Flash capacity (KB)	32	64	32	64	32	64	32	64	32	64	
SRAM capacity (KB)	16	16	16	16	16	16	16	16	16	16	
CPU frequency	ARM Cortex-M4F @128MHz, 160DMIPS										
working environment	2.4~3.6V/-40~105°C										
Timer	General	4									
	Advanced	2 (Timer1 supports 4 channels and 8 complementary outputs, Timer8 supports 3 channels and 6 complementary output)									
	Basic	1									
	LPTIM	1									
Communication interface	SPI	2									
	I2S	2									
	I2C	2									
	UART	1				2					
	USART	2									
	CAN	1									
BEEPER	1										
GPIO	15+1				23+1		25+1		39+1		
DMA Number of Channels	1 8 Channel										
12bit ADC Number of channels	1 9Channel		1 7Channel		1 10Channel			1 16Channel			
COMP	3										
security protection	Read and write protection (RDP/WRP), storage encryption, partition protection, secure boot										
Package	TSSOP20		QFN20		QFN28		LQFP32 QFN32		LQFP48 QFN48		

Note: ⁽¹⁾ PIN2/PIN3 of N32G430F6S7 and N32G430F8S7 are OSC_IN/OSC_OUT, PIN2/PIN3 of N32G430F6S7-1 and N32G430F8S7-1 are OSC32_IN/OSC32_OUT.

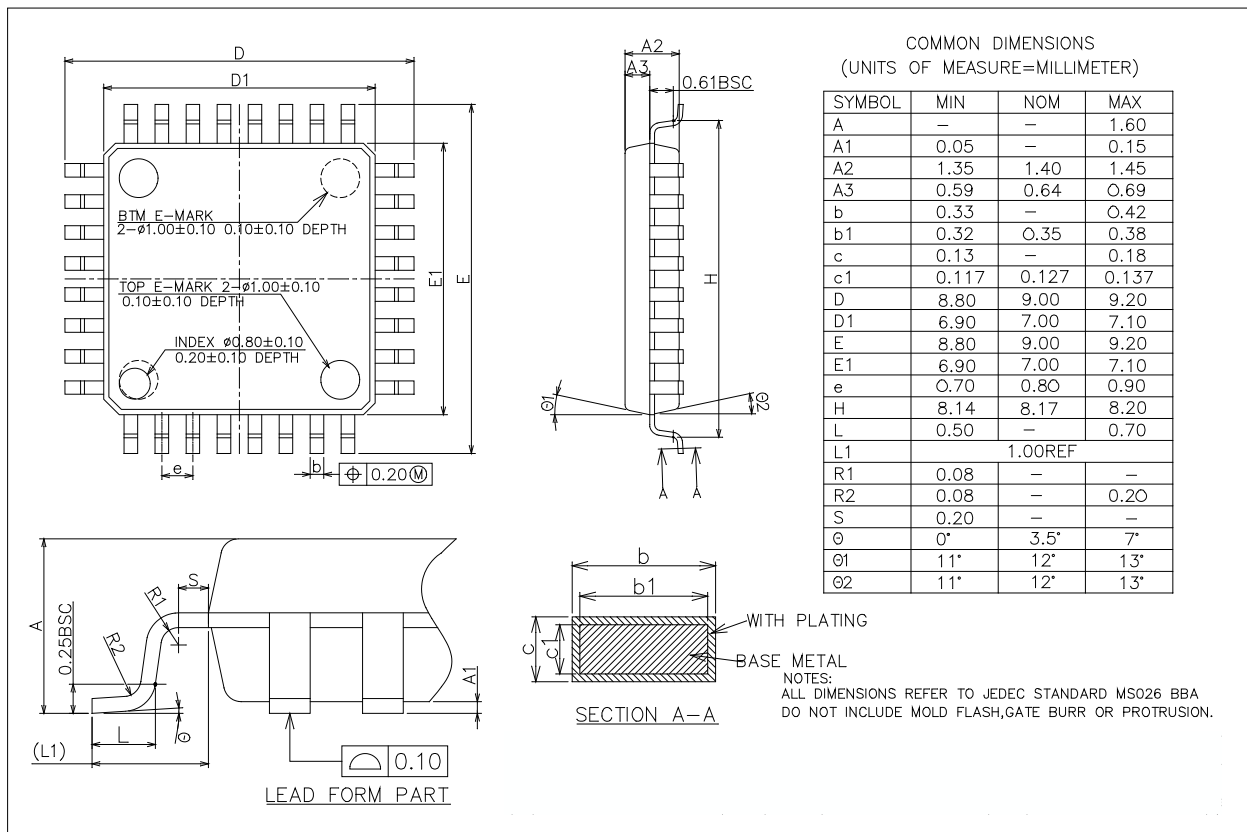
3 Package Information

3.1 LQFP32

3.1.1 LQFP32 Pinout

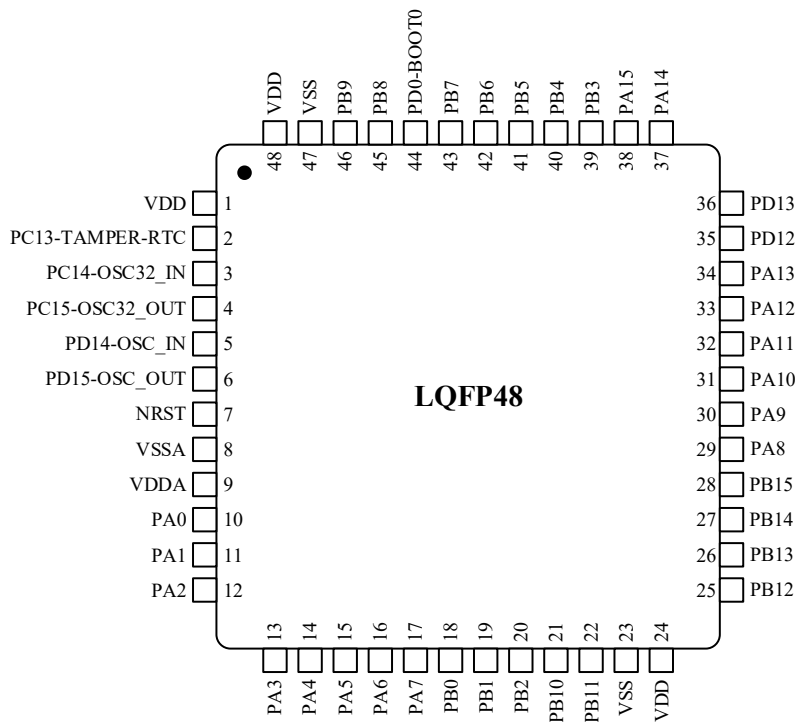


3.1.2 LQFP32 Package

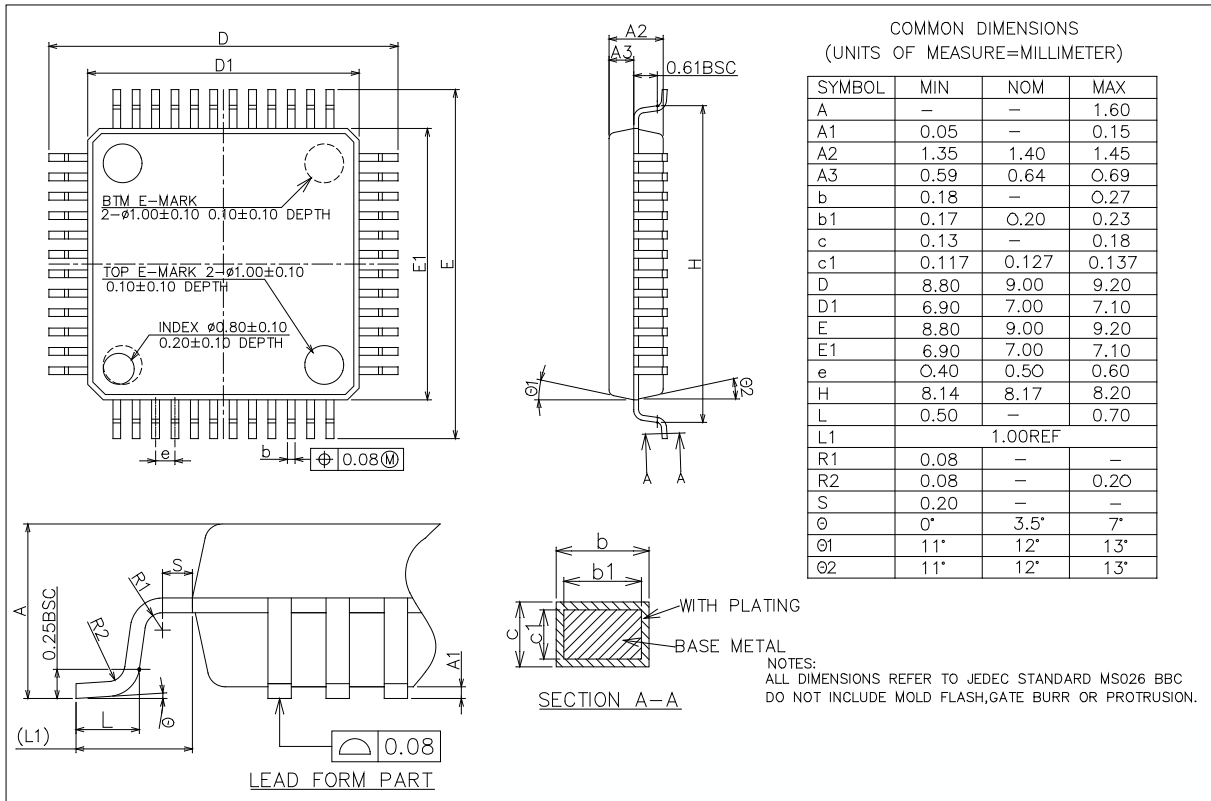


3.2 LQFP48

3.2.1 LQFP48 Pinout

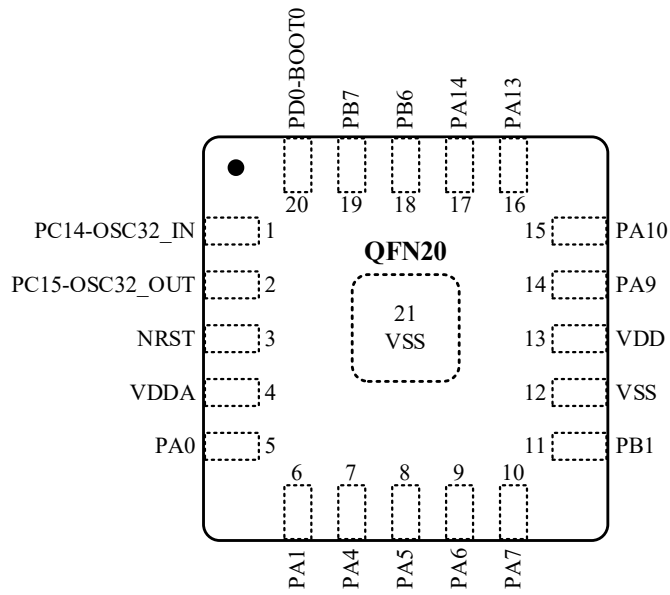


3.2.2 LQFP48 Package

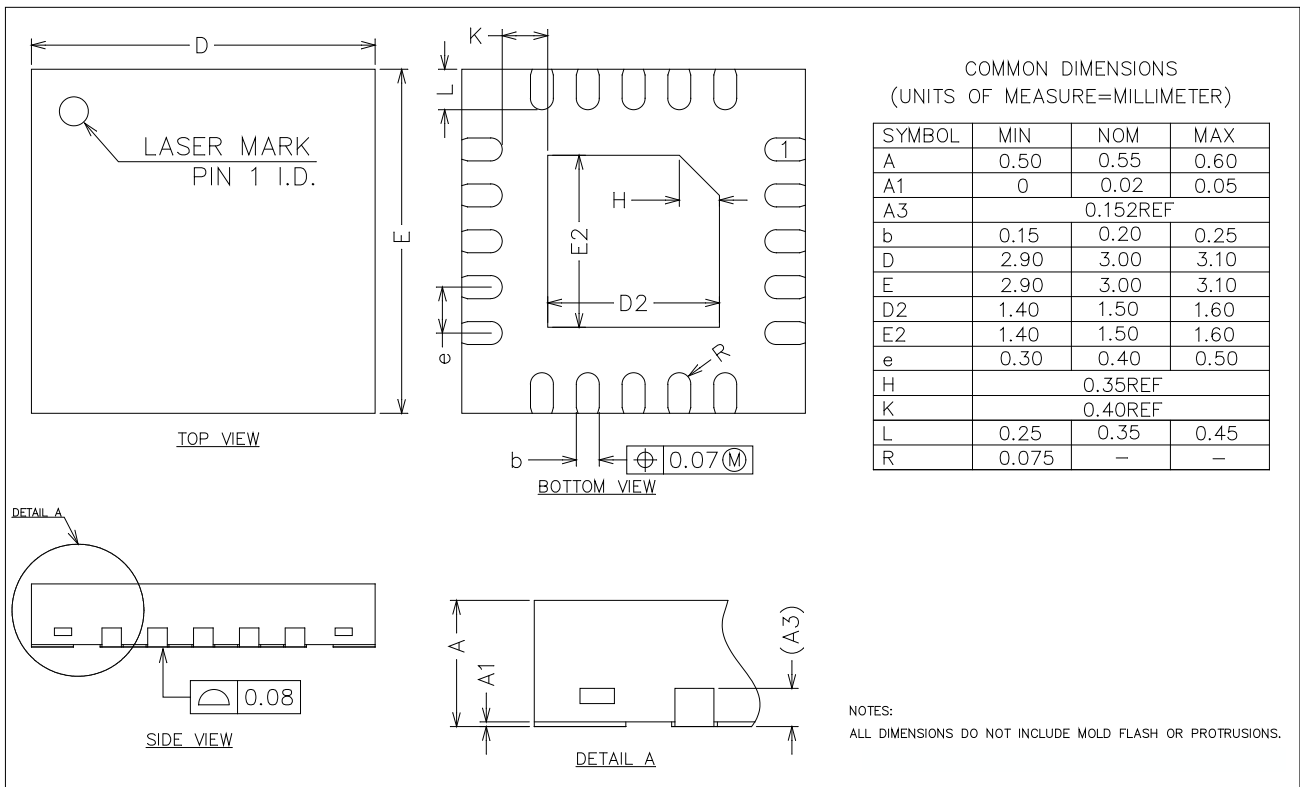


3.3 QFN20

3.3.1 QFN20 Pinout

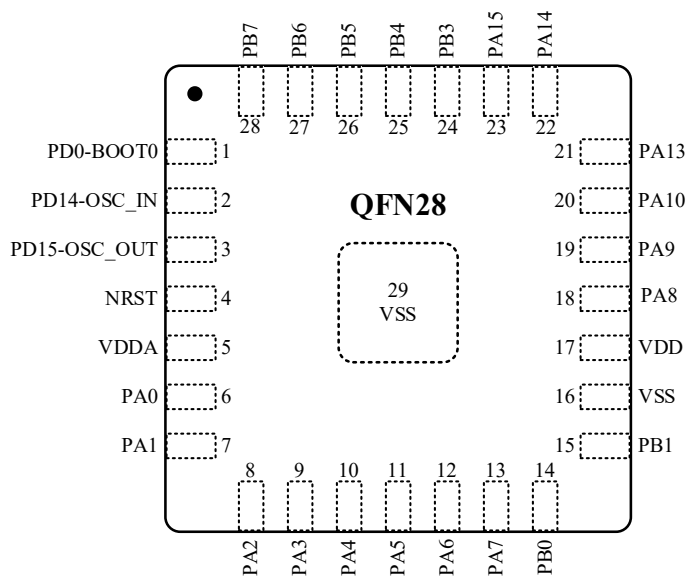


3.3.2 QFN20 Package

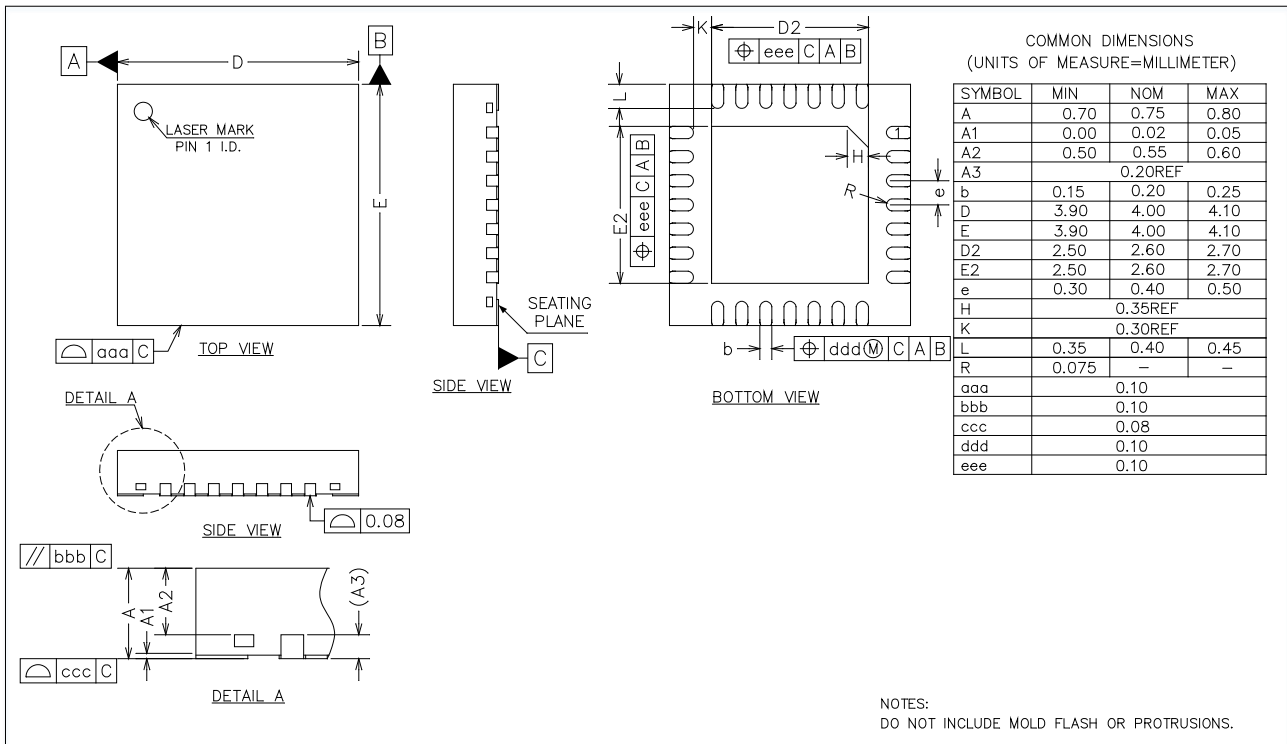


3.4 QFN28

3.4.1 QFN28 Pinout

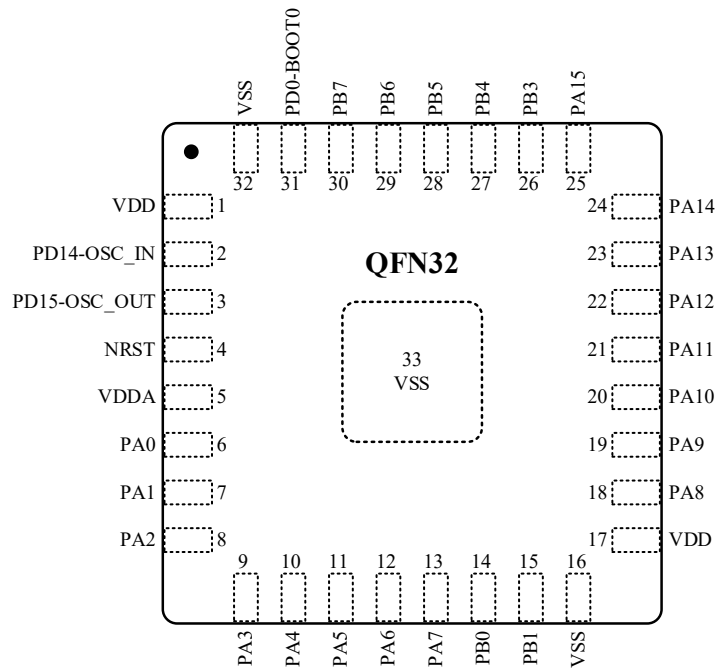


3.4.2 QFN28 Package

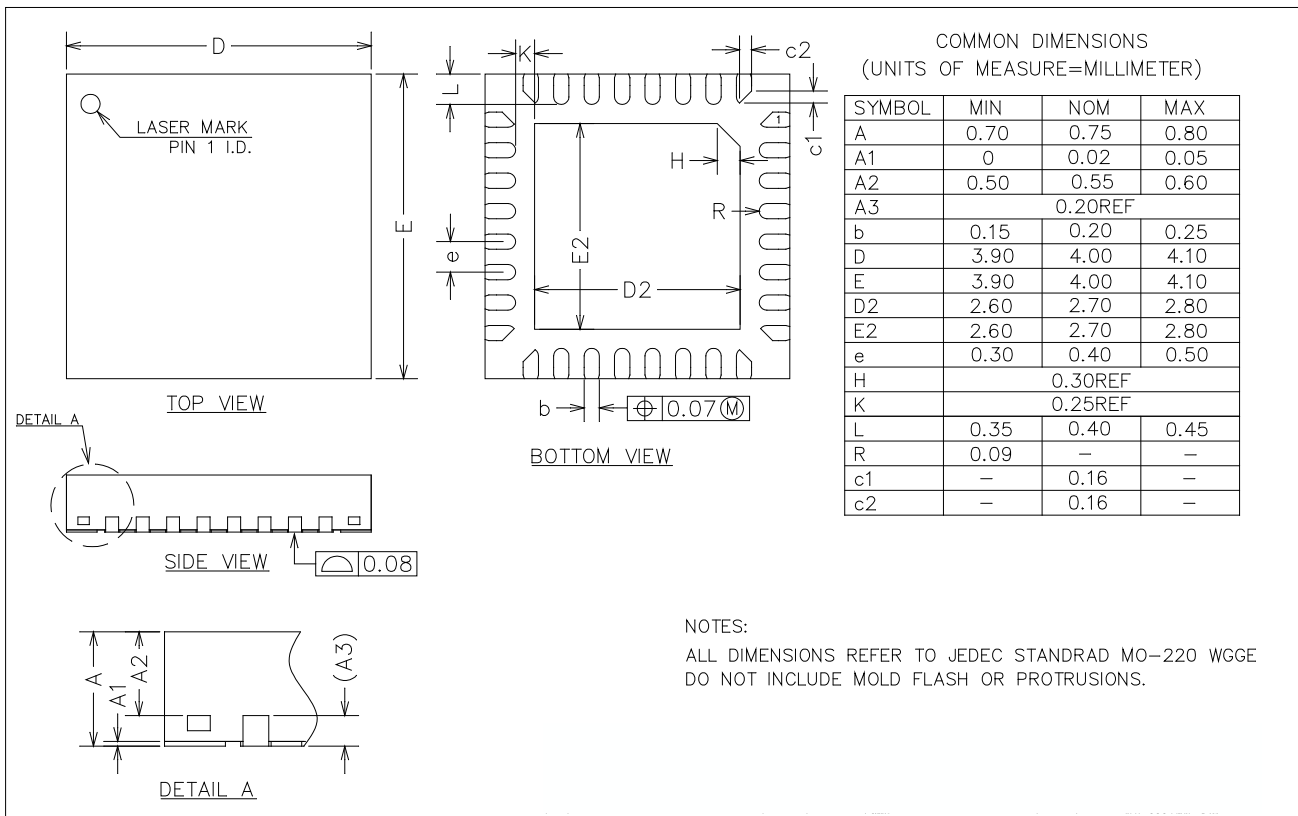


3.5 QFN32

3.5.1 QFN32 Pinout

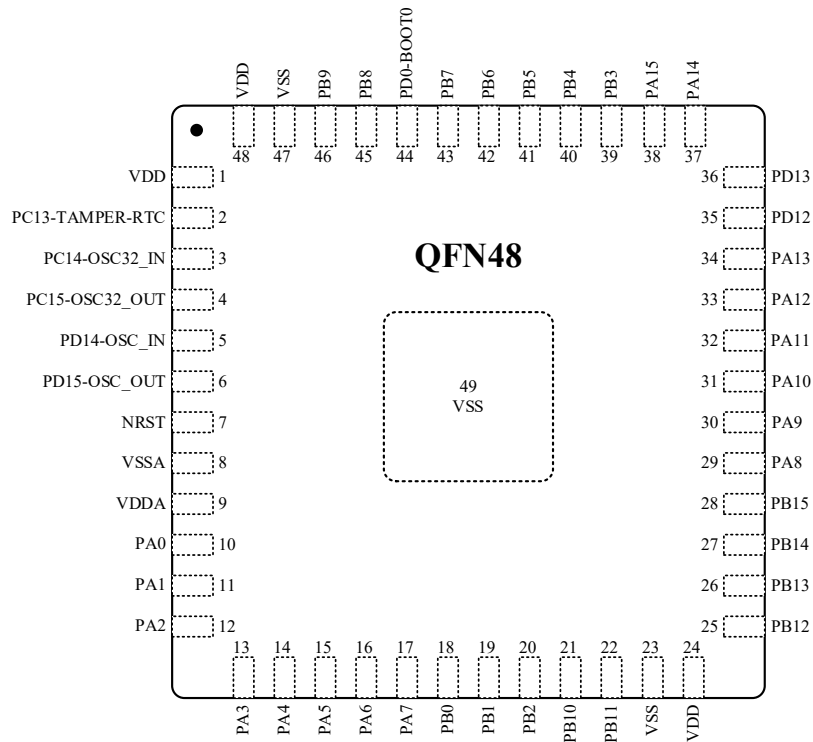


3.5.2 QFN32 Package

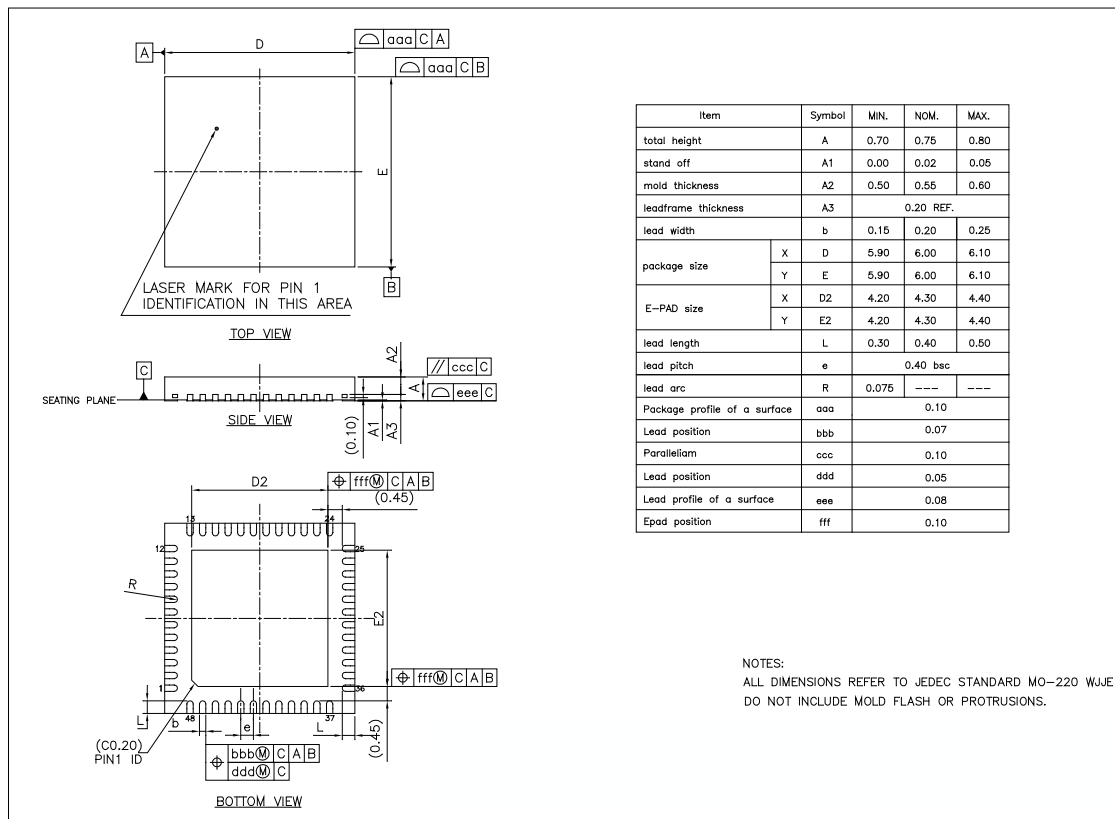


3.6 QFN48

3.6.1 QFN48 Pinout

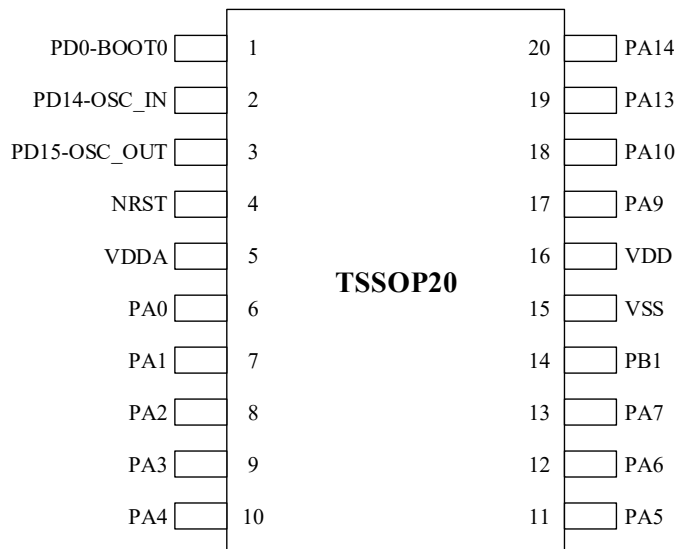


3.6.2 QFN48 Package

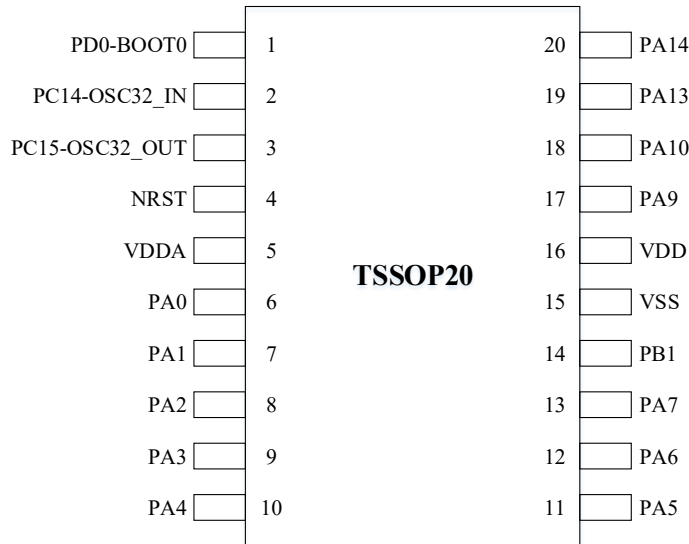


3.7 TSSOP20

3.7.1 TSSOP20 Pinout

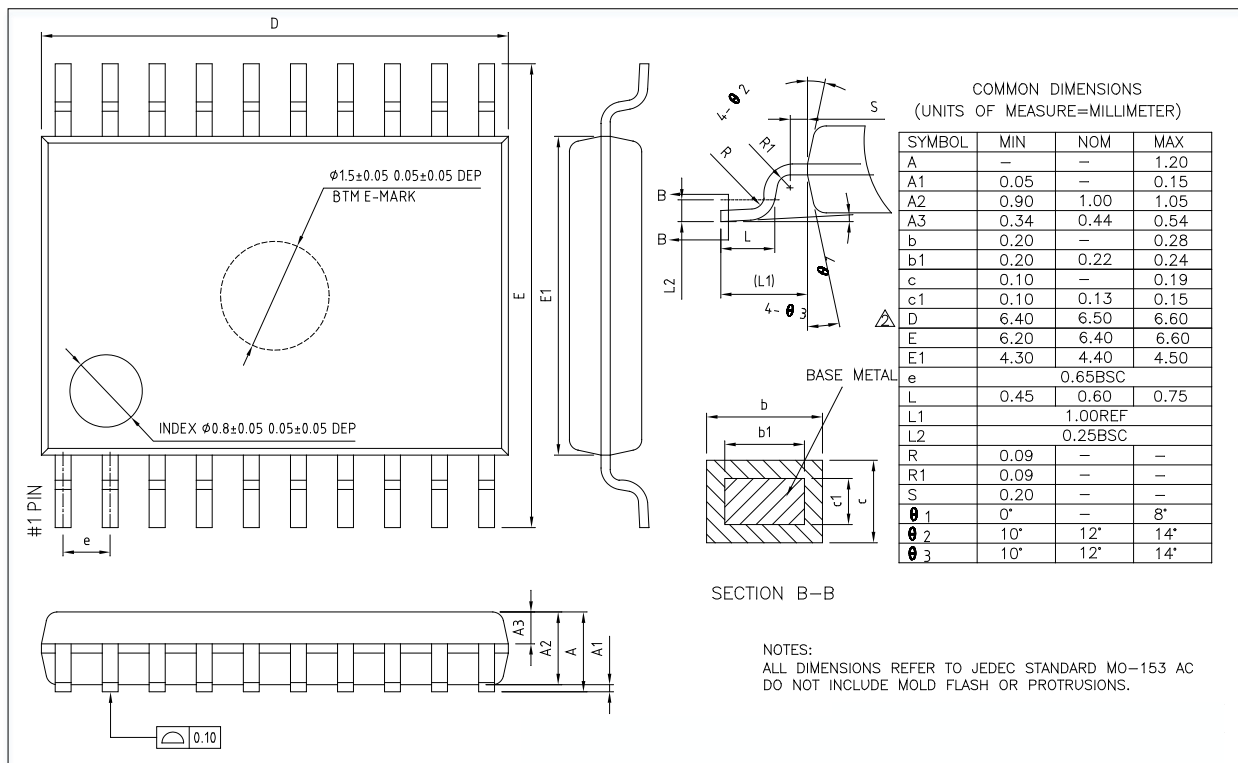


This pinout is for N32G430F6S7 and N32G430F8S7.



This pinout is for N32G430F6S7-1 and N32G430F8S7-1.

3.7.2 TSSOP20 Package



4 Version History

Version	Date	Changes
V1.0	2022.4.21	Initial release
V1.1	2022.8.22	1. Delete MPU support
V1.2.0	2023.3.17	1. Modify SPI master mode speed description

5 Disclaimer

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