Application Note

AN_N32G43x_N32L43x_N32L40x_USB_Xtal_Less_Application_Note

Introduction

In embedded product development, the USB device is often used, because the USB clock accuracy requirement, and in most cases will use external high speed crystal as the clock source to ensure accuracy, of course, in some applications, there is no external high-speed crystal, at this point you can use the USB xtal_less mode to ensure USB clock precision and the normal transmission of USB data.

This document mainly introduces the USB xtal_less mode, MCU does not need to connect to high-speed external crystal, this document is only applicable to nations MCU products, currently supported product series are N32G43x, N32L40x and N32L43x series.

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1. Overview

The USB2.0 full-speed protocol has a transmission rate of 12Mbps (12Mbps ± 0.025%(2500ppm)), and the system clock of USB is four times as long as the transmission rate, is 48MHz. In order to obtain an accurate 48MHz clock, there are two ways to achieve it in N32G43x series, N32L40x series and N32L43x series. One is to use external HSE crystal to obtain an accurate 48MHz clock by frequency doubling and frequency division. The other is to use the UCDR module inside the chip to get an accurate 48MHz clock.

This document describes how to obtain an accurate 48MHz clock by using the UCDR module inside the chip.

The following uses the N32L40x series as an example.

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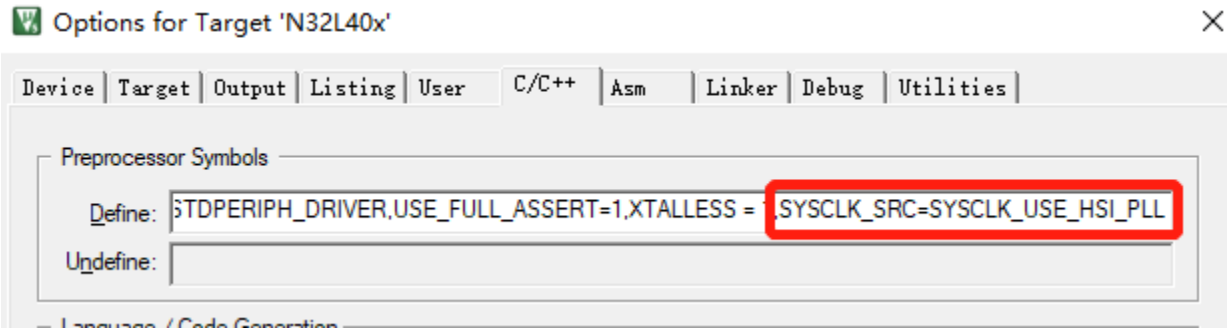
2. Configure the System Clock and UCDR Module

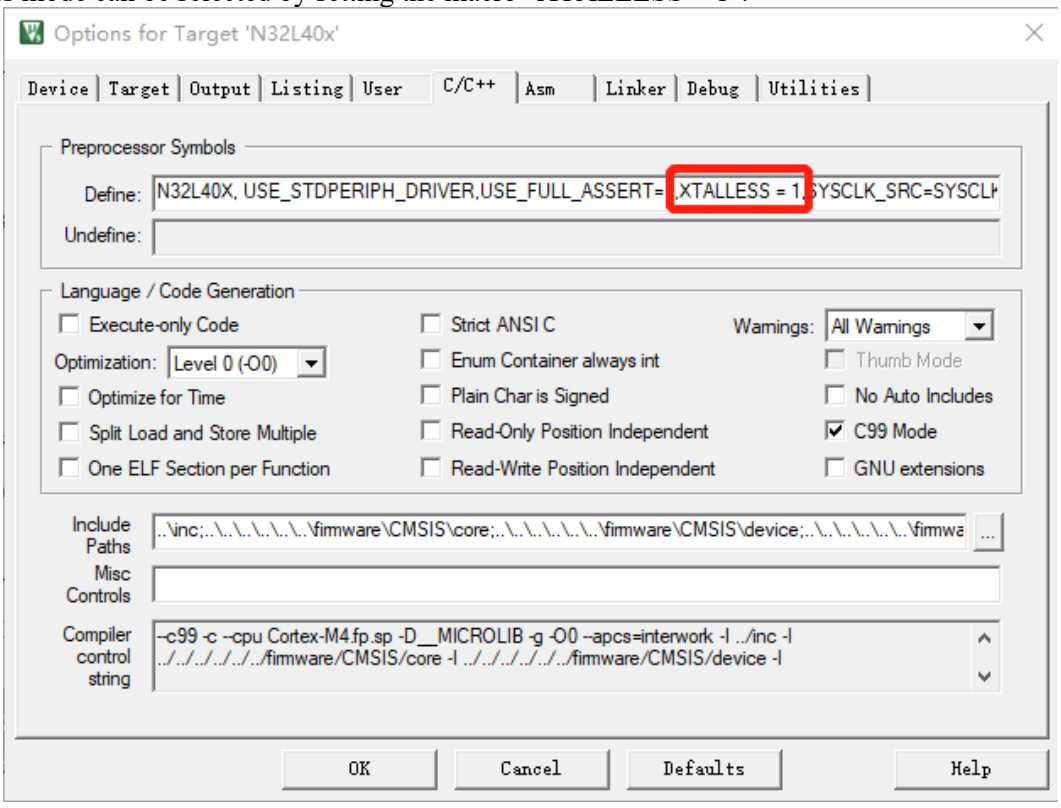
2.1 Modify System Clock

SYSCLK_USE_HSI_PLL is selected for the system clock for there id no external high-speed crystal.



2.2 Select Xtal_Less Mode

The xtal_less mode can be selected by setting the macro "XTALLESS = 1".



2.3 Configure UCDR Module

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```
/**
  * @brief  SB_XtallessIni.
  * @param  RCC_UCDR300MSource: ucdr source
  * @return USBClock set Status.
  */
void USB_XtallessIni(uint32_t RCC_UCDR300MSource)
{
    uint32_t time;

    /* Check the parameters */
    assert_param(IS_RCC_UCDR300M_SRC(RCC_UCDR300MSource));

    RCC->APB1PCLKEN |= RCC_APB1PCLKEN_AFECEN;
    /* Clear UCDR300MSEL bits */
    RCC->CFG3 &= RCC_UCDR300MSource_MASK; //RCC_UCDR300M_SRC_MASK;
    /* Set UCDR300MSEL bits */
    RCC->CFG3 |= RCC_UCDR300MSource;
    /* Select the USB Crystal Mode */
    RCC->CFG3 |= RCC_USBXTALESS_LESSMODE;

    /* Enable LDO for OSC UCDR */
    _EnOsc300Ldo();
    time = 0x4000;
    while(time--);
    /* Enable iBias for OSC UCDR */
    _EnOsc300Ibias();
    time = 0x4000;
    while(time--);
    /* Enable Core for OSC UCDR */
    _EnOsc300Core();
    time = 0x4000;
    while(time--);

    /* Enable UDCR */
    RCC->CFG3 |= RCC_UCDR_ENABLE;
    time = 0x4000;
    while(time--);

    return;
}
```

After the UCDR configuration is completed, the bus signal input by USB host will be detected to obtain the accurate USB data bit width, and then through OSC300MHz frequency division to obtain the accurate USB communication clock. The USB initialization process is the same as in xtal mode.

After the UCDR configuration is complete, don't enable ESOF interrupt, and then enable ESOF interrupt after receiving SOF frame, see Figure 2-1.

To ensure the quality of USB communication, reset the UCDR module in the following cases:

1. When the USB device is just inserted, the UCDR module is reset when the first SOF frame is received after each enumeration because the signal is unstable, see Figure 2-1;

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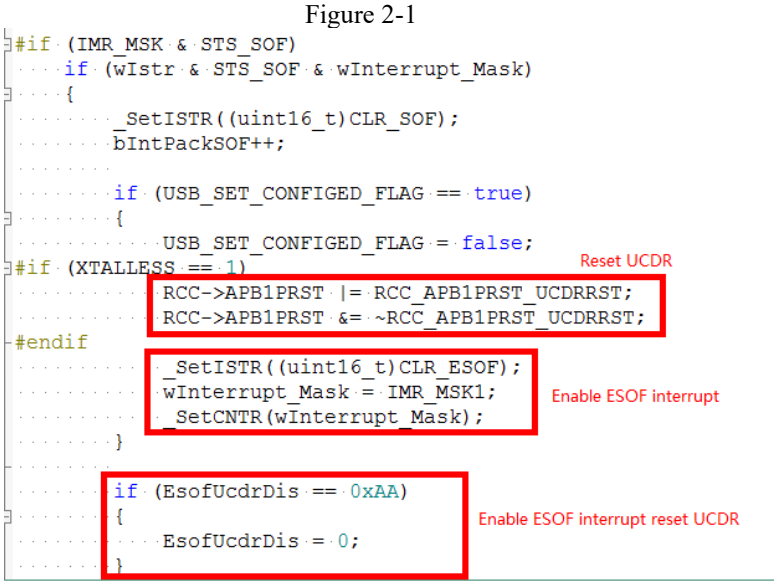
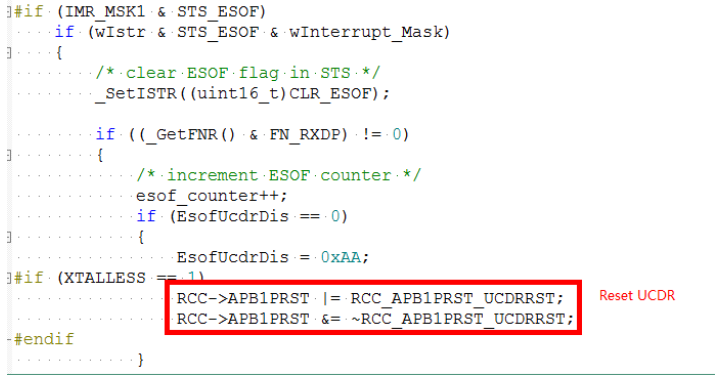
Figure 2-1



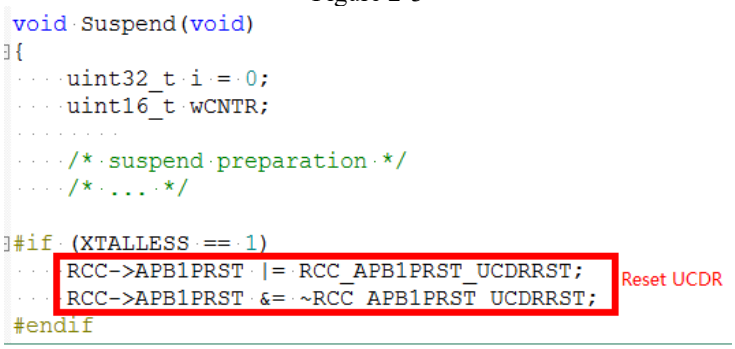
2. Reset the UCDR module after receiving an ESOF interrupt. To prevent repeated resetting of the UCDR module, after completing the UCDR reset during an ESOF interrupt, restart the UCDR module after receiving the SOF frame during an ESOF interrupt, see Figure 2-1 and Figure 2-2.

Figure 2-2



3. After the USB is suspend, reset the UCDR module, see Figure 2-3.

Figure 2-3



For more details, see DEMO in Application Notes please.

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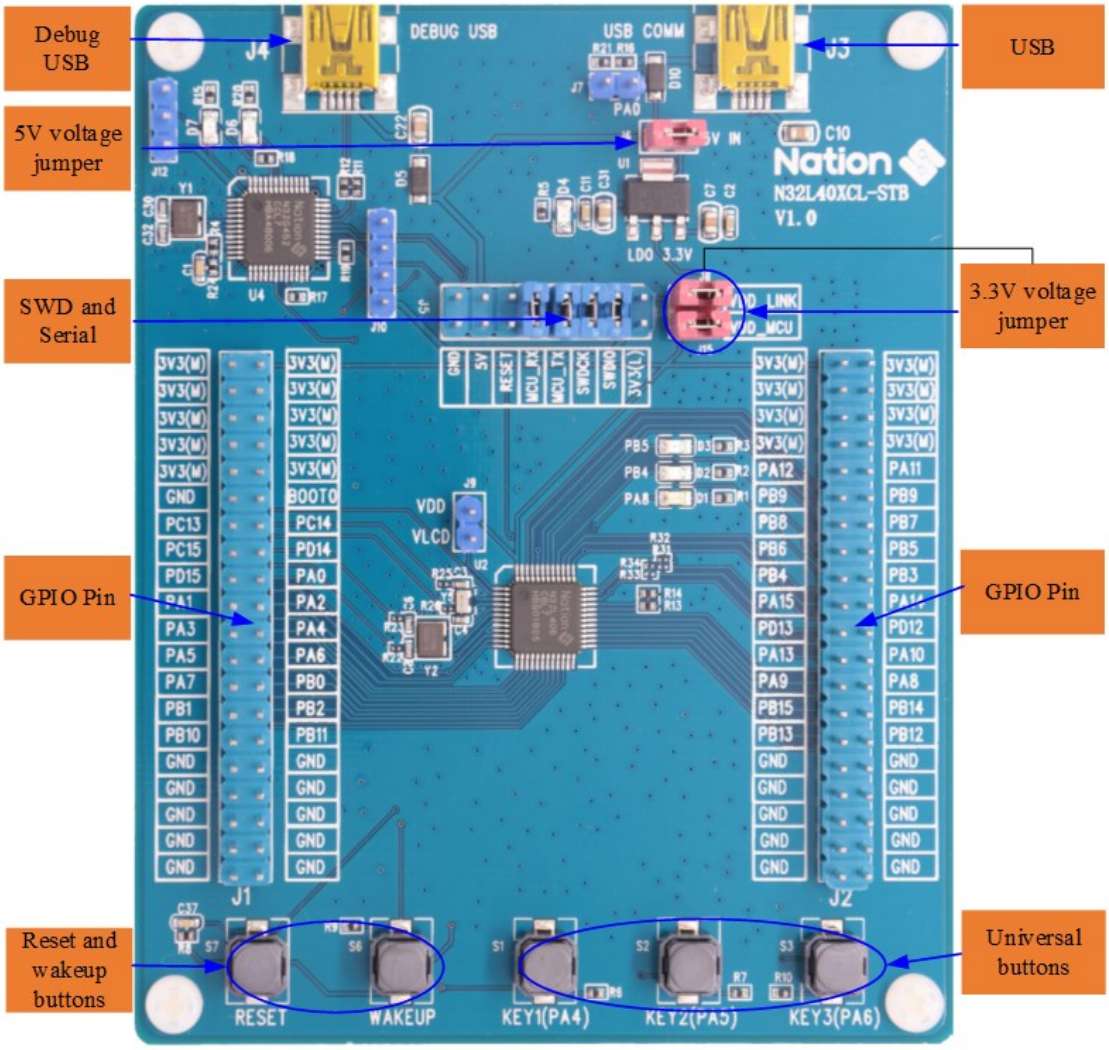
3. Demo Presentation

Select N32L40x series minimum system development board N32L40XCL-STB V1.0. Figure 3-1 shows N32L40XCL-STB V1.0 minimum system development board. Please refer to "UG_N32L40XCL-STB Development Board Hardware Usage Guide" for the use of development board.

Figure 3-1 Development board layout



J4 on the development board is the USB download and debugging interface, and J3 is the USB device interface. After the code is compiled and downloaded to the board through J4, reset and run, and then connect J3 port to the computer, it can be seen that the computer recognizes the keyboard device, press KEY1(PA4) button, and the computer enters "a".

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4. Version History

Date	Version	Remark
2022/07/26	V1.0	New document

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