N32G435 Series

Errata Sheet

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Contents

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1 Errata List

Table 1-1 Overview of Errata

	Errata link	Chip version					
		Version B	Version C	Version D	Version E	Version G	Version H
Ch 2: Power control (PWR)	2.1: System clock switchover	●					
	2.2: Switch to Stop2 mode from LPRUN mode	●	●	●	●	●	●
	2.3: Power on again after power down	●	●				
Ch 3: Reset and clock control (RCC)	3.1: Enter Stop2 mode from run mode	●	●	●	●	●	●
	3.2: LSE-CSS fault detection	●	●	●	●	●	●
Ch 4: GPIO and AFIO	4.1: GPIO analog function	●	●				
Ch 5: Analog/Digital conversion (ADC)	5.1: ADC data left-align	●	●	●	●	●	●
	5.2: ADC injection channels trigger regular channel conversions	●	●	●	●	●	●
	5.3: ADC analog watchdog	●	●	●	●	●	●
	5.4: DMA moves ADC data	●	●	●	●	●	●
Ch 6: Serial peripheral interface (SPI)	6.1: SPI interface — 6.1.1: SPI baud rate setting	●	●	●	●	●	●
	6.1: SPI interface — 6.1.2: CRC check slave mode	●	●	●	●	●	●
	6.1: SPI interface — 6.1.3: SPI CLK GPIO configuration	●	●	●	●	●	●
	6.2: I2S interface — 6.2.1: PCM long frame mode	●	●	●	●	●	●
Ch 7: I²C interface	7.1: Software events that must be managed before the current byte transfer	●	●	●	●	●	●
	7.2: Considerations when reading single or double bytes at a time	●	●	●	●	●	●
	7.3: Use DMA in conjunction with other peripherals	●	●	●	●	●	●
	7.4: Abnormal signal interference	●	●	●	●	●	●
Ch 8: Universal synchronous asynchronous receiver (USART)	8.1: Check error flag	●	●	●	●	●	●
	8.2: RTS hardware flow control	●	●	●	●	●	●
Ch 9: Debug interface (DBG)	9.1: Debug register	●	●	●	●	●	●
Ch 10: Timer (TIM)	10.1: Timer repeat capture detection	●	●	●	●	●	●
Ch 11: Comparator (COMP)	11.1: Comparator INP input		●	●	●	●	●
Ch 12: Real time clock (RTC)	12.1: RTC prescale	●	●	●	●	●	●
	12.2: RTC subpicosecond interrupt	●	●	●	●	●	●
	12.3: RTC interrupt	●	●	●	●	●	●
	12.4: RTC auto wakeup	●	●	●	●	●	●
	12.5: RTC mistakenly triggers TISOVF flag bit	●	●	●	●	●	●
Ch 13: Low power timer (LPTIM)	13.1: LPTIM maximum count value	●	●	●	●	●	●
Ch 14: Controller area network (CAN)	14.1: CAN active error	●	●	●	●	●	

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2 Power Control (PWR)

2.1 System Clock Switching

Description

During the process of switching from the system clock using HSI/HSE to MSI, if a system reset occurs, it may lead to chip crash.

Workaround

To avoid using HSI/HSE directly as the system clock, it is recommended to choose PLL as the system clock.

2.2 Switch to Stop2 Mode from LPRUN Mode

Description

When the MCU switches from LPRUN mode to Stop2 mode, a reset may occur after wakeup.

Workaround

To solve this problem, ensure that PVDBOR is always enabled on in Stop2 mode (clear the PBDTLPR bit of PWR_CTRL3 to 0) before entering Stop2 mode.

2.3 Power On Again after Power Down

Description

If the power supply is powered off and drops to the range of 600 mv to 100mV, and then power on again, the power on may be unsuccessful.

Workaround

When the MCU is powered off, it is necessary to ensure that the chip's VDD voltage drops below 100mV before powering up the MCU.

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3 Reset and Clock Control (RCC)

3.1 Enter Stop2 Mode from Run Mode

Description

Dividing AHB CLK and APB CLK by certain frequency divisors may result in an extremely low probability of the chip not entering Stop2 mode in Run mode. The higher the frequency divisor, the more likely this phenomenon may occur.

Workaround

Back up AHB CLK frequency division factor and configure the AHB CLK to be undivided before entering STOP2 mode. Besides, restore the frequency division backed up after exit from STOP2 mode.

3.2 LSE-CSS Fault Detection

Description

After the LSE-CSS detects that the LSE is stopped, it cannot switch to the LSI through software.

Workaround

Power on again.

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4 GPIO and AFIO

4.1 GPIO Analog Function

Description

When the four GPIO PA1/PA2/PA3/PA4 output high and are switched to analog function, it will cause 30mV voltage drop in the switching process.

Workaround

Avoid the above methods.

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5 Analog/Digital Conversion (ADC)

5.1 ADC Data Left-Align

Description

In ADC single conversion mode, with non-12-bit precision and left alignment, when a software-triggered conversion of the regular channel is initiated, the highest bit of the invalid bits in the ADC_DAT register is set to 1.

Workaround

Retain only valid data bits or use right-aligned mode.

5.2 ADC Injection Channels Trigger Regular Channel Conversions

Description

In ADC continuous conversion mode, if external trigger for regular channel is disabled and only software trigger is used for injected channel conversion, it is possible that the regular channel may be triggered to convert As a result, data is generated in ADC_DAT, and the corresponding status bit of ADC_STS regular channel conversion will be set.

Workaround

Ignore the flag bits and data generated by regular channels.

5.3 ADC Analog Watchdog

Description

In ADC independent mode with single conversion and non-12-bit precision, enabling the analog watchdog feature, and triggering the conversion of regular/injected channels by software, if the high threshold value of the analog watchdog is set equal to the value in the ADC data register with all invalid bits set to 0, it may inadvertently trigger the analog watchdog.

Workaround

In this case, the highest position 1 of the invalid bit of the simulated watchdog high threshold is not triggered.

5.4 DMA Moves ADC Data

Description

In ADC independent mode with continuous conversion and DMA transfer of ADC data, when the configured number of transfers is completed, disabling DMA first and then disabling ADC, and then re-enabling DMA, if DMA is enabled before ADC is enabled, the first data transferred by DMA may be the residual ADC conversion data from before DMA was disabled.

Workaround

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In this case, if DMA is re-enabled after being disabled in a loop, an additional data transfer is added to the base transfer count N. After the first disable, the data from the first to the Nth transfer is read. Subsequent disables will read the data from the second to the N+1th transfer.

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6 Serial Peripheral Interface (SPI)

6.1 SPI Interface

6.1.1 SPI Baud Rate Setting

Description

When the baud rate control bit (BR[2:0]) is set to $f_{PLCK}/2$ in SPI master mode, the CRC check will fail.

Workaround

In this case, avoid setting baud rate control bit (BR[2:0]) to $f_{PLCK}/2$.

6.1.2 CRC Check Slave Mode

Description

When the SPI is operating in slave mode with CRC enabled, even if the NSS pin is at a high level, as long as the SPI receives clock signals, it will still perform CRC calculation.

Workaround

Before using CRC check, clear the CRC data register to synchronize the CRC check between the master and slave devices

The clearing steps are as follows:

1. Reset the SPI enable bit (set to 0)
2. Reset the CRC check bit (set to 0)
3. Set the CRC check bit (set to 1)
4. Set the SPI enable bit (set to 1)

6.1.3 SPI CLK GPIO Configuration

Description

When the SPI clock polarity is configured as high, after enabling the SPI, the clock of GPIO will be pulled high before outputting the clock signal. The slave may mistakenly interpret this edge as a clock signal, causing the received data to shift.

Workaround

Configure the clock of GPIO based on the clock polarity (pull up the clock of GPIO if the clock polarity is high, and pull down the clock of GPIO if the clock polarity is low) before enabling the SPI.

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6.2 I²S Interface

6.2.1 PCM Long Frame Mode

Description

When the I²S is operating in master mode, PCM long frame mode, and the data format is extended from 16bit to 24bit or 32bit, the WS signal is cycles every 16bit instead of 24bit or 32bit.

Workaround

When I²S is in master mode and long frame mode must be used, 16bit data mode should be used.

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7 I²C Interface

7.1 Handling Software Events before Current Byte Transferring

Description

In the occurrence of events EV7, EV7_1, EV6_1, EV6, EV2, EV8, and EV3, it is essential to handle the events before the current byte transfer to prevent issues such as reading an extra byte, obtaining duplicate data, or losing data. If the software fails to read the N-1 data before the stop signal generation, the data in the shift register for the Nth byte may become corrupted (shifted left by one bit).

Workaround

1. When transferring more than one byte using I²C, it is recommended to use DMA
2. When using I²C interrupts, the interrupt priority is set to the highest priority of the application
3. When the read data reaches the N-1 byte:
    1) Check BSF is 1
    2) Set SCL to GPIO open miss output and set it to 0
    3) Set STOPGEN to 1
    4) Read the N-1 byte
    5) Set SCL to open/miss output mode for I²C multiplexing
    6) Read the last byte

7.2 Notes on Single Read of One or Two Bytes

Description

In master read mode, errors in reading data may occur when reading byte lengths of single byte and double byte.

Workaround

1. Single byte read:
    1) Upon receipt of ADDRF
    2) Set the ACKEN bit to 0
    3) Clear the ADDRF bit (by reading STS1 and then STS2)
    4) Set STOPGEN to 1
    5) Read one byte of data
2. Double-byte read:
    1) Upon receipt of ADDRF

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2) Set the ACKPOS bit to 1

3) Clear the ADDRF bit (by reading STS1 and then STS2)

4) Set the ACKEN bit to 0

5) The BSF level was 1

6) Set STOPGEN to 1

7) Read two bytes of data in a row

7.3 Use DMA Simultaneously with Other Peripherals

Description

If other peripherals are using DMA during the I^2C communication, the I^2C communication will be abnormal.

Workaround

During I^2C communication using DMA, disable DMA for other peripherals.

7.4 Abnormal Signal Interference

Description

During operation, I^2C may experience communication anomalies due to glitches on SCL and SDA lines.

Workaround

1. Master and slave automatic recovery:

   1) Soft reset of I^2C by I^2C CTRL1[15](SWRST) bit

   2) Restore the IIC module by controlling the RCC_APB1RSTR[21](I2CxRST) bit in the RCC module to complete the recovery

   3) Restore the IIC module by calling the global soft reset NVIC_SystemReset() function for global reset

2. Master recovery slave machine:

   1) Restore the slave machine by controlling the hardware reset pin reset the slave machine

   2) Use the power management mechanism to power on the slave machine for restoration

   3) Set the communication port of the IIC master to GPIO mode, and send 9 clocks on the SCL CLOCK line to recover the slave machine

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8 Universal Synchronous Asynchronous Receiver (USART)

8.1 Check Error Flag

Description

During the receipt of a byte of data, if a checksum error is detected before the stop bit is received, and the checksum error flag bit is set. During this period, the checksum error flag bit cannot be cleared by software (read status register, and then read data register). If checksum interrupt is enabled, the checksum interrupt handler will be entered several times.

Workaround

The read buffer flag bit is set, and the error flag bit operation is performed after the data is received.

If checksum error interrupt is enabled, to avoid entering the interrupt processing function for multiple times, the checksum error interrupt is disabled when entering the checksum error interrupt for the first time. After receiving data, the checksum error interrupt is enabled again.

8.2 RTS Hardware Flow Control

Description

When the RTS hardware flow control is enabled, the USART receives a frame of data. When the first byte of data is received, the RTS signal is automatically pulled up. If the first byte of data is not read out of the data register in time, the RTS signal is pulled down again after the next byte of data is received, and the USART waits for the next frame of data to be received.

Workaround

Read the data from the data register in time before receiving the next new data.

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9 Debug Interface (DBG)

9.1 Debug Register

Description

The DBGMCU_IDCODE debug register can only be accessed in debug mode (not by user programs), and the value returned by reading in user mode is 0xFF.

Workaround

Avoid using IDCODE in user applications.

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10 Timer (TIM)

10.1 Timer Repeat Capture Detection

Description

When an input capture event occurs, while reading TIMx_CCDATx (capture/compare register x) (the read operation automatically clears the capture flag), the CCxOCF (capture/compare x overcapture flag) may still be set.

Workaround

None.

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11 Comparator (COMP)

11.1 Comparator INP Input

Description

When PA0/PA1/PA3 are configured as a digital function pin and are at a high level, it will affect the INP input of COMP1.

Workaround

When using COMP1, do not use PA0/PA1/PA3 as digital function pins.

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12 Real Time Clock (RTC)

12.1 RTC Prescale

Description

The asynchronous prescaler factor and the synchronous prescaler factor in the RTC cannot be set to 0, as it may lead to easily RTC pre-allocation to failure.

Workaround

Avoid setting the asynchronous prescaler register (TRC_PRE) DIVA[6:0] (asynchronous prescaler segment) and DIVS[14:0](synchronous prescaler segment) to 0.

12.2 RTC Subpicosecond Interrupt

Description

The first RTC subpicosecond interrupt will not be generated.

Workaround

The application waits for the second and subsequent subpicosecond interrupt.

12.3 RTC Interrupt

Description

If the interval between two RTC initialization is less than 1S, the RTC alarm and auto wake-up interrupt can’t be generated.

Workaround

The time interval for RTC initialization should be more than 1S.

12.4 RTC Periodic WakeUp

Description

Periodic wakeup from the RTC module does not work to wake up from STANDBY mode.

Workaround

Use the RTC alarm wake-up feature instead of the periodic wakeup.

12.5 RTC Mistakenly Triggers TISOVF Flag Bit

Description

When the system wakes up from STANDBY mode or reset by IWDG timeout, TISOVF flag in RTC may be set incorrectly.

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Workaround

Before entering STANDBY mode or when the system is reset by IWDG timeout, when the SHOPF flag is 0, configure RTC_SCTRL.SUBF[14:0] register once, and SHOPF flag will set to 1. When SHOPF flag is 0 again, it should configure RTC_SCTRL.SUBF[14:0] register for the second time. This will solve the issue.

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13 Low Power Timer (LPTIM)

13.1 LPTIM Maximum Count Value

Description

When selecting the internal clock source for LPTIM (CKSLE bit in the LPTIM_CFG register is 0), and the counter is configured to increment for each valid clock pulse on Input1 (the CNTMEN bit in the LPTIM_CFG register is 1), the maximum count value of the counter is ARRVAL (automatic reload counter) -1.

Workaround

When the LPTIM_CFG register CKSLE bit is 0 and the LPTIM_CFG register CNTMEN bit is 1, the calculated target value of ARRVAL needs to be incremented by 1 for configuration.

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14 Controller Area Network (CAN)

14.1 CAN Active Error

Description

In normal mode, if the CAN bit is hard synchronized and the bus rate deviation of other nodes on the bus is too large (approaching or exceeding the synchronization segment), the CAN module is prone to report active errors.

Workaround

None.

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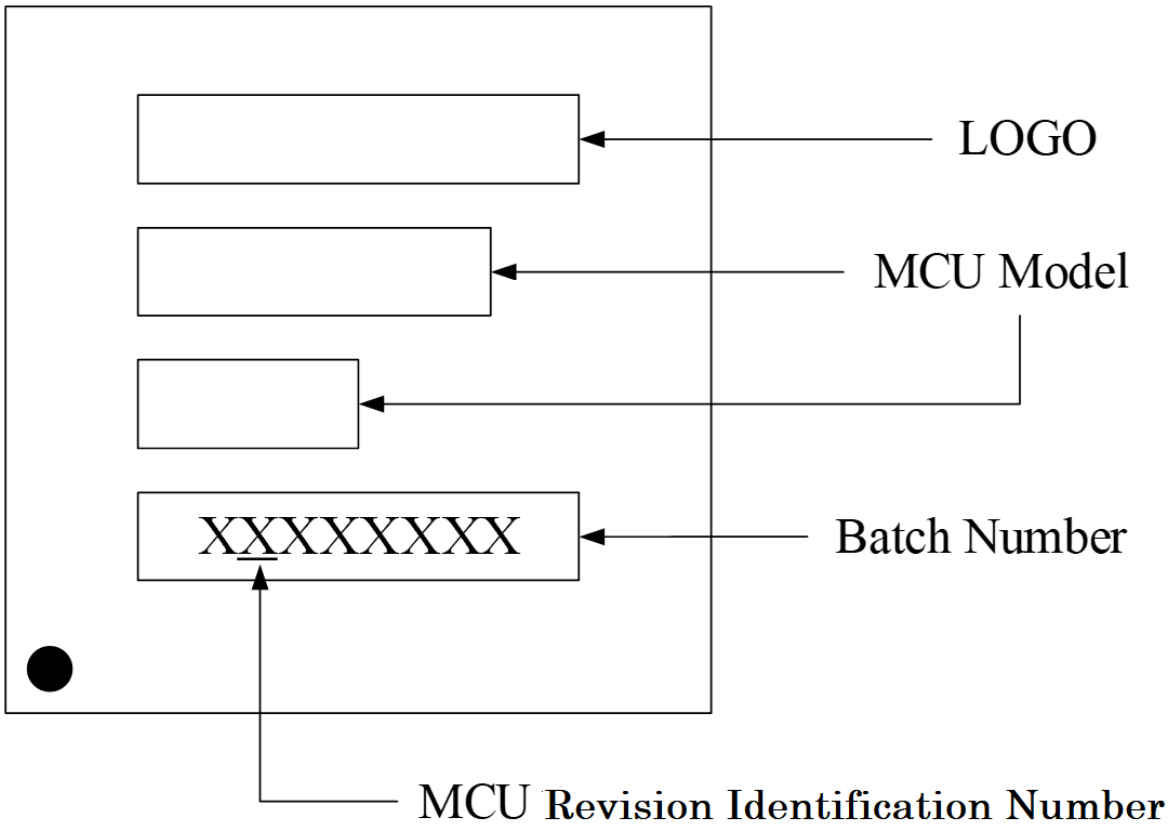
15 Chip Screen Printing and Version Description



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16 Version History

Version	Date	Changes
V1.0.0	2021.09.15	Initial release
V1.0.1	2021.11.30	1) Added 5.3 ADC analog watchdog 2) Added 5.4 DMA moving ADC data 3) Added 7.4 Abnormal signal interference 4) Added 11.2 RTC subsecond interrupt
V1.1.0	2022.02.22	Added SPI CLK GPIO Configuration
V1.2.0	2022.04.06	1) Modified Table 1-1 Errata Description Added version E 2) Modified 11.2 Ch to change RTC sub-pico-second to RTC subsecond 3) Added 12 Ch on Low Power Timer (LPTIM) 4) Added 3.2 LSE-CSS Fault Detection 5) Modified 7.3 Ch to add I^2C DMA usage restrictions
V1.2.1	2022.09.05	1. Added 14 Chs Controller Area Network(CAN) 2. Added 12.3 RTC interrupt Ch 3. Added 12.4 RTC Auto Wakeup Ch
V1.3.0	2023.02.14	Added 12.5 Ch RTC mistakenly triggers TISOVF flag bit

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