User Guide

ADC User Guide

Introduction

The MCU features four embedded advanced 12-bit ADC with calibration function, used to improve ADC accuracy under changing environmental conditions. This document aims to help users correctly use the ADC, reduce errors, and improve the stability of ADC operation. The main contents include:

- Correct configuration of three ADC clocks
- ADC calibration
- Multiple switching applications
- Core power configuration
- ADC interference and errors
- ADC impedance and small signal acquisition
- Differential calculation formula

This document is only applicable to NSING MCU products, currently supported product series are N32G4xx, and N32L4xx.

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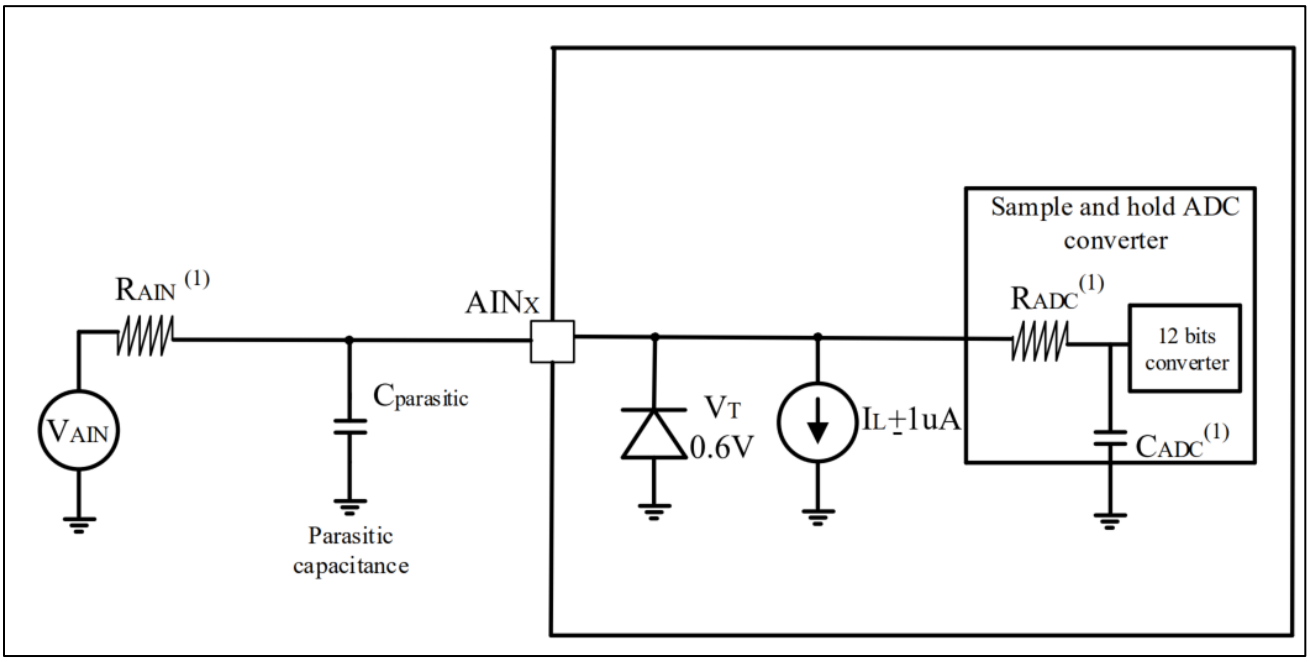
1. Overview

1.1 SAR ADC

The serie's ADCs are all 12-bit successive approximation analog-to-digital converters, supporting various operating modes to meet the needs of most analog-to-digital conversion applications. The ADC has three clocks: the operation clock, the sampling clock, and the timing clock, to ensure the ADC sampling rate and accuracy.

The process of external input signal acquisition is as follows: first, the channel and chip pins are connected via MUX to charge the sampling capacitor inside the chip, then the MUX disconnects the channel connection after the sampling is completed, keeping the input signal on the sampling capacitor. Finally, the converter sequentially compares and calculates the code value and transfers it to the data register.

Figure 1-1 Typical ADC Connections



The parameters marked in the figure are as follows:

VAIN: input signal.

RAIN: external input impedance.

C-parasitic: parasitic capacitance on PCB and pads.

AINX: signal input port.

RADC: sampling switch resistance.

CADC: internal sampling and hold capacitor.

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1.2 Basic Operating Principle

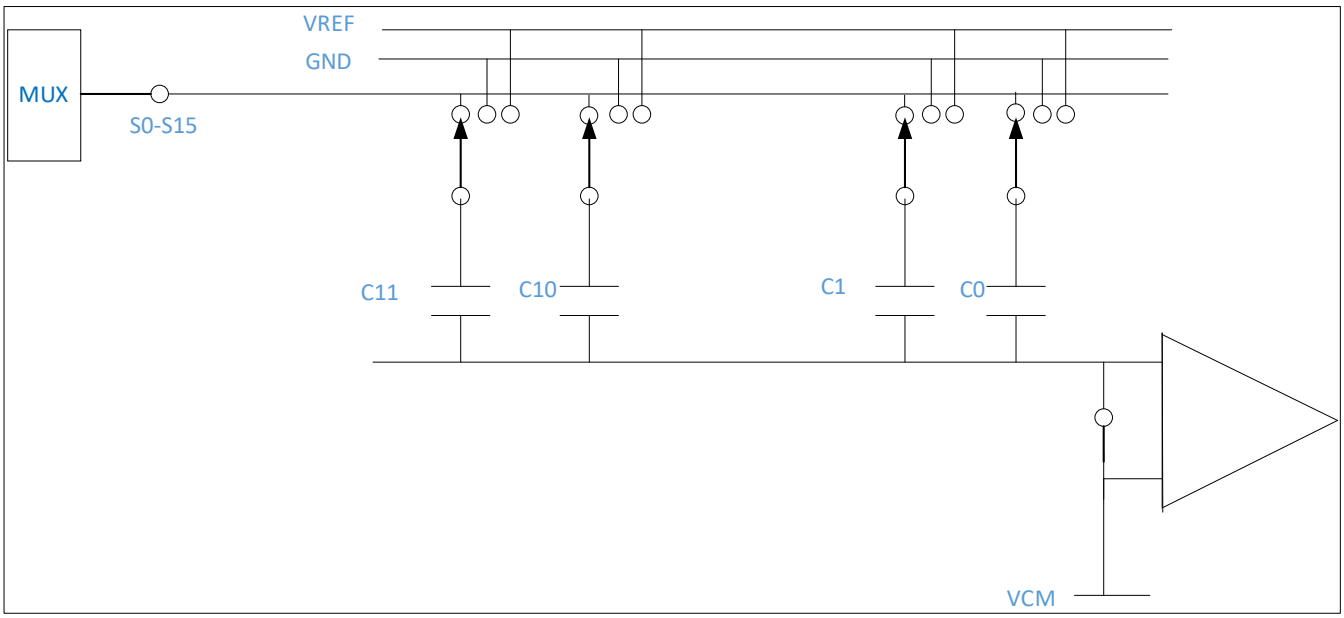
The basic operating principle of an ADC consists of three processes: sampling, holding, and quantization. Sampling is the process of converting a continuously changing analog signal in time into a discrete analog signal, holding is the process of storing the signal for the next sampling, and quantization is the process of converting the held analog signal into a digital signal.

If the internal sampling and conversion circuit of the ADC is simplified, it can be equivalent to three working stages:

- Sampling stage

  S0~S15 are connected to chip pins (input signal sources) based on the configured channel selection. The sampling capacitors are C0 to C11, with the lower board of the capacitor connected to the signal source and the upper plate (COMP end) connected to VCM for input signal sampling.

Figure 1-2 Equivalent Circuit of Sampling Stage



- Hold stage

  Disconnect S0~S15 from the input signal, with the upper plate of the capacitor (COMP end) floating and the lower plate connected to ground.

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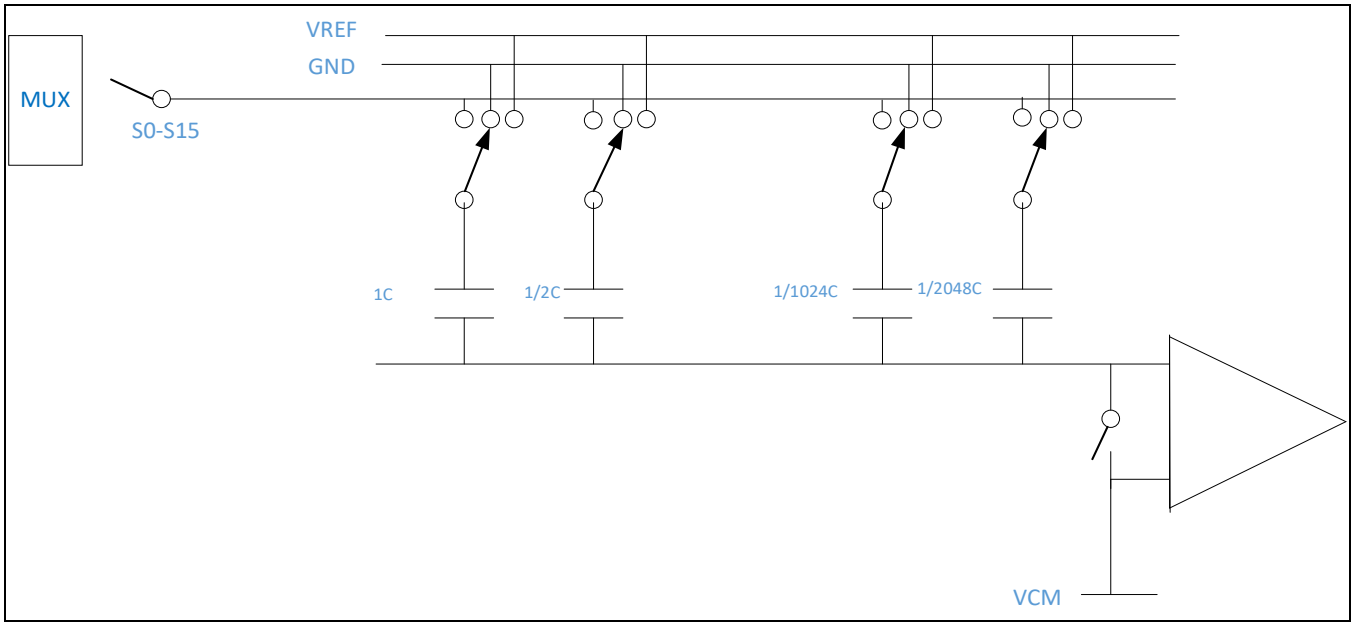
Figure 1-3 Equivalent Circuit of Hold Stage



- Sequential comparison stage

  In the initial stage, the lower plate of the capacitor is connected from high to low to VREF, GND... GND, and from C11 to C0, the capacitor switch is decided based on the comparator output result:

  - MSB: C11 is connected to VREF for comparison. If the comparator output is high, it remains connected to VREF; otherwise, it is changed to connect to GND.
  - (M-1)SB: C10 is connected to VREF for comparison. If the comparator output is high, it remains in that state; otherwise, it is changed to connect to GND.
  - Repeat the comparison process described above.
  - LSB: C0 is connected to VREF for comparison. If the comparator output is high, it remains in that state; otherwise, it is changed to connect to GND.
  - After the conversion is complete, move the quantized value to the data register.

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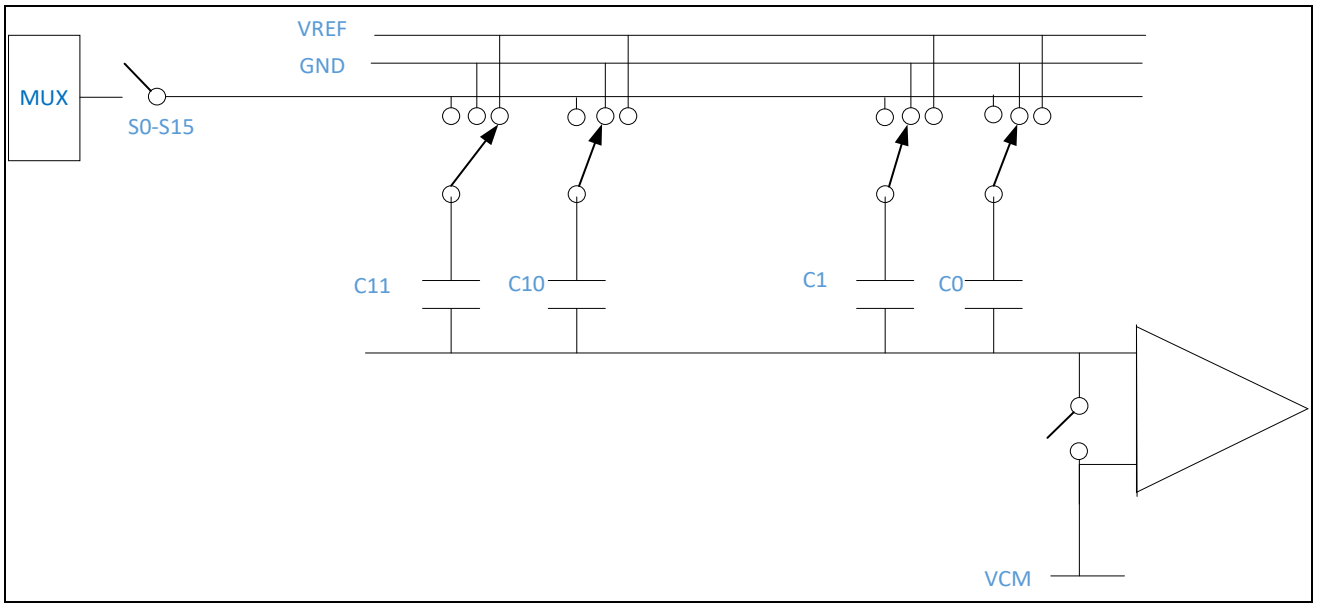
Figure 1-4 Equivalent Circuit of Sequential Comparison Stage



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2. ADC Application Considerations

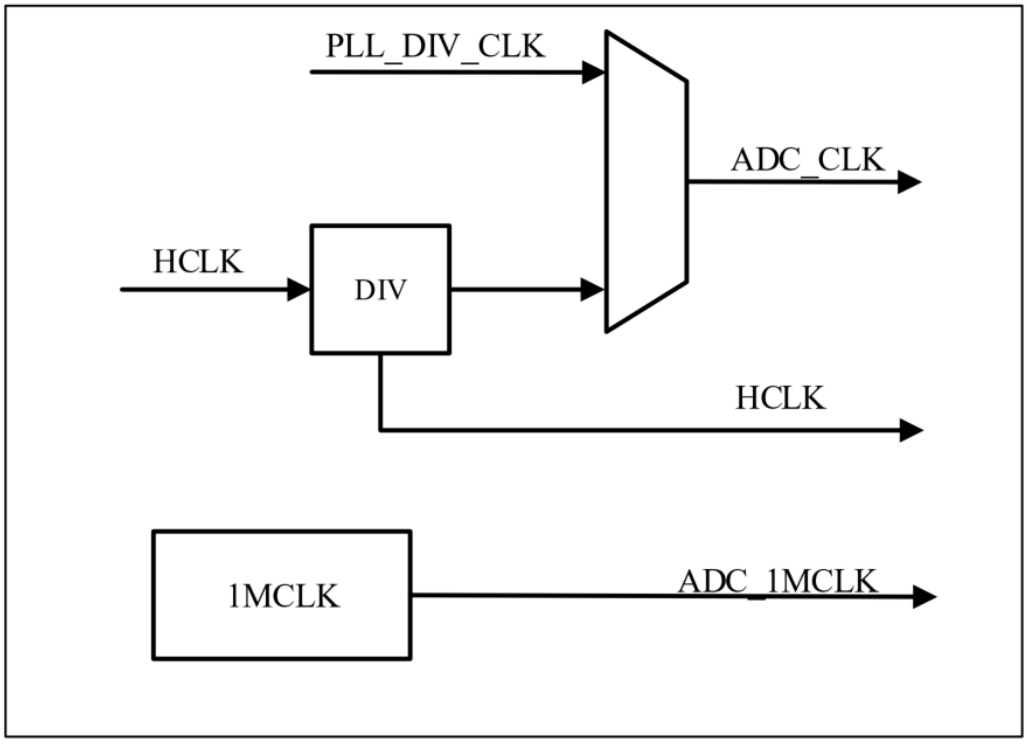
In many applications, it is necessary to collect analog signals and perform calculations to achieve a series of functions. Therefore, the ADC is an important peripheral in the chip. High-precision ADC can ensure that the converted values of input signals are closer to the original signal source. However, errors become an unavoidable topic for ADCs. In order to reduce sampling signal errors, it is necessary not only to filter the noise in the input signal but also to correctly configure and use the ADC.

Below will be a detailed introduction to the application considerations of the ADC, aiming to reduce errors in data acquisition, obtain high-precision sampled data, and leverage the powerful performance of the ADC.

2.1 ADC Clock Config

Below will be a detailed introduction to the application considerations of the ADC, aiming to reduce errors in data acquisition, obtain high-precision sampled data, and leverage the powerful performance of the ADC.

Figure 2-1 ADC Clock



- ADC operating clock

  The operating clock used for accessing registers is HCLK;

  Example of configuring the ADC operating clock in various series of library functions:

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Figure 2-2 Clock Function

N32G45x：

RCC_EnableAHBPeriphClk(RCC_AHB_PERIPH_ADC1 | RCC_AHB_PERIPH_ADC2 | RCC_AHB_PERIPH_ADC3 | RCC_AHB_PERIPH_ADC4, ENABLE);

N32G43x/N32L40x/N32L43x：

RCC_EnableAHBPeriphClk(RCC_AHB_PERIPH_ADC, ENABLE);

- ADC sampling clock

  The sampling clock ADC_CLK has two sources (HCLK division or PLL division). The HCLK division is a synchronous clock with the system, while the PLL division is an asynchronous clock with the system. The advantage of using a synchronous clock is that there is no uncertainty when triggering the ADC response. The advantage of using the PLL division clock is that it can independently handle the ADC's operating clock without affecting other modules hanging on HCLK.

  Examples of configuring ADC sampling clocks in various series library functions:

  - The N32G45x: The maximum operating frequency of this series is 144MHz, and PLL can be configured as the sampling clock source, with a maximum frequency of 72MHz, supporting divisors of 1, 2, 4, 6, 8, 10, 12, 16, 32, 64, 128, 256. AHB_CLK can be configured as the sampling clock source, with a maximum frequency of 72MHz, supporting divisors of 1, 2, 4, 6, 8, 10, 12, 16, 32.

Figure 2-3 N32G45x Sampling Clock Function

When the system frequency is greater than 72MHz, the ADC_CLK must be divided by at least 2.

AHB_CLK as the sampling clock source:

ADC_ConfigClk(ADC_CTRL3_CKMOD_AHB,RCC_ADCHCLK_DIV2);

PLL as the sampling clock source: ADC_ConfigClk(ADC_CTRL3_CKMOD_PLL,RCC_ADCPLLCLK_DIV2);

  - The N32G43x/ N32L43x: The maximum operating frequency of this series is 108MHz, and PLL can be configured as the sampling clock source, with a maximum frequency of 72MHz, supporting divisors of 1, 2, 4, 6, 8, 10, 12, 16, 32, 64, 128, 256. AHB_CLK can be configured as the sampling clock source, with a maximum frequency of 72MHz, supporting divisors of 1, 2, 4, 6, 8, 10, 12, 16, 32.

Figure 2-4 N32G43x/ N32L43x Sampling Clock Function

When the system frequency is greater than 72MHz, the ADC_CLK must be divided by at least 2.

AHB_CLK as the sampling clock source:

ADC_ConfigClk(ADC_CTRL3_CKMOD_AHB,RCC_ADCHCLK_DIV2);

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PLL as the sampling clock source: ADC_ConfigClk(ADC_CTRL3_CKMOD_PLL,RCC_ADCPLLCLK_DIV2);

- The N32L40x: The maximum operating frequency of this series is 64MHz, and PLL can be configured as the sampling clock source, with a maximum frequency of 64MHz, supporting divisors of 1, 2, 4, 6, 8, 10, 12, 16, 32, 64, 128, 256. AHB_CLK can be configured as the sampling clock source, with a maximum frequency of 64MHz, supporting divisors of 1, 2, 4, 6, 8, 10, 12, 16, 32.

Figure 2-5 N32G43x/ N32L43x Sampling Clock Function

The maximum system clock frequency of this series is 64MHz. When the system clock is 64MHz, the ADC_CLK can be divided by 1.

AHB_CLK as the sampling clock source:
ADC_ConfigClk(ADC_CTRL3_CKMOD_AHB,RCC_ADCHCLK_DIV2);

PLL as the sampling clock source: ADC_ConfigClk(ADC_CTRL3_CKMOD_PLL,RCC_ADCPLLCLK_DIV2);

- ADC timing clock

  The timing clock can be HSI and HSE, mainly used for internal timing, and the frequency must be configured as 1MHz. Examples of configuring ADC timing clocks in various series library functions:

  - For the N32G45x series, configuring the ADC timing clock, the clock source can be internal HSI and HSE. HSI is 8MHz, and HSE supports 4~32MHz.

Figure 2-6 N32G45x Timing Clock Function

HIS is 8MHZ: RCC_ConfigAdc1mClk(RCC_ADC1MCLK_SRC_HSI, RCC_ADC1MCLK_DIV8);

HSE is 8MHZ: RCC_ConfigAdc1mClk(RCC_ADC1MCLK_SRC_HSE, RCC_ADC1MCLK_DIV8);

  - For the N32G43x/N32L43x/N32L40x series, configuring the ADC timing clock, the clock source can be internal HSI and HSE. HSI is 16MHz, and HSE supports 4~32MHz.

Figure 2-7 N32G43x/N32L43x/N32L40x Timing Clock Function

HIS is 8MHZ: RCC_ConfigAdc1mClk(RCC_ADC1MCLK_SRC_HSI, RCC_ADC1MCLK_DIV8);

HSE is 8MHZ: RCC_ConfigAdc1mClk(RCC_ADC1MCLK_SRC_HSE, RCC_ADC1MCLK_DIV8);

2.2 ADC Calibration

Calibration can increase sampling accuracy. Calibration is required when the ADC is powered up for the first time and when the ADC wakes up from deep sleep to ensure the sampling accuracy of the ADC.

The ADC digital calibration module is used to measure and correct the offset voltage of the ADC. The calibration process samples the ideal "0" voltage through internal connections, calculates the offset, and removes the offset voltage during normal operation.

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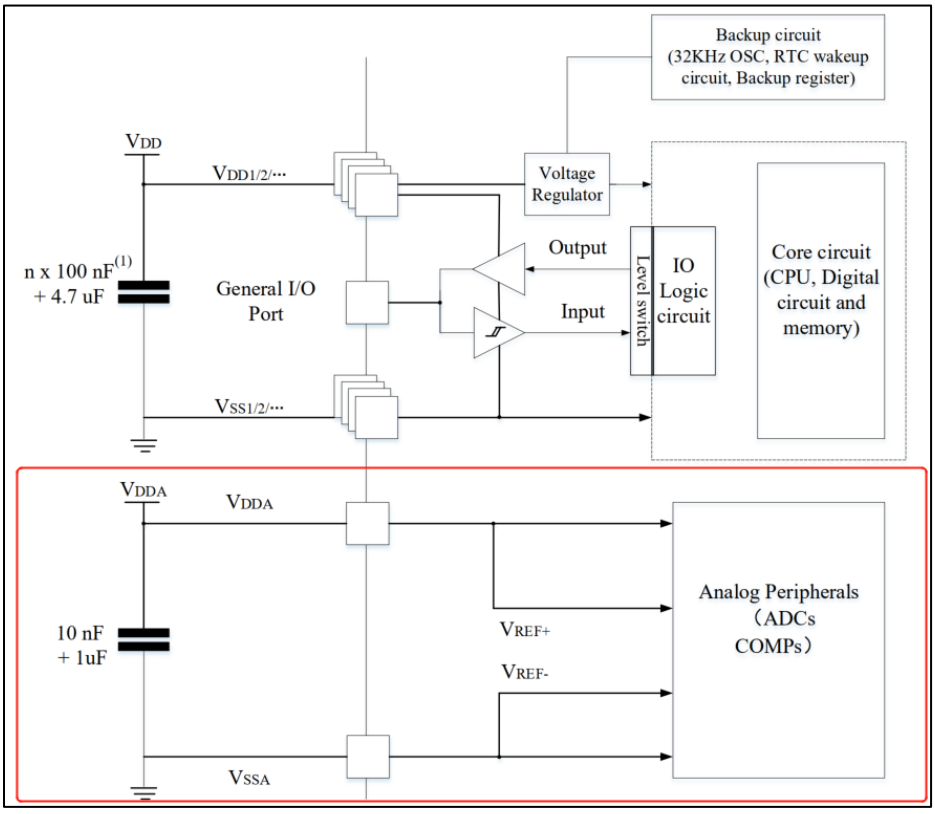
Figure 2-8 ADC ADC Calibration Function

```
N32G45x series, ADC calibration operation:
/* Start ADC1 calibration */
ADC_StartCalibration(ADC1);
/* Check the end of ADC1 calibration */
while (ADC_GetCalibrationStatus(ADC1))
N32G43x/N32L40x/N32L43x series, ADC calibration operation:
/* Start ADC calibration */
ADC_StartCalibration(ADC);
/* Check the end of ADC calibration */
while (ADC_GetCalibrationStatus(ADC));
```

2.3 ADC Power Supply

The chip power supply system consists of digital power supply and analog power supply. VDD mainly provides power to digital modules such as CPU, USART, GPIO, etc. VDDA mainly provides power to analog modules such as ADC, COMP, etc. It is recommended to use the same power supply for VDD and VDDA. During power-up and normal operation, a maximum difference of 300mV is allowed between VDD and VDDA.

Figure 2-9 Power System



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The ADC module is powered by an internal LDO by default, with the LDO reference source initially set to VDDA. Fluctuations in the VDDA voltage can affect the ADC sampling accuracy and operation. In harsh working environments, there is a probability of abnormal ADC operation, manifested as abnormal or halted data acquisition. When using DMA for data transfer in multi-channel acquisition, there may also be a probability of channel shifting during data transfer.

When encountering similar phenomena in ADC applications, adjusting the MR voltage and switching the ADC power supply to the digital system instead of using the internal LDO power supply method can effectively improve the stability of ADC operation.

- N42G45x MR voltage adjustment

Figure 2-10 N42G45x MR Voltage Adjustment

1. Define the MR operation register: ADCIP_CTRL (*(UINT32_T*)(0x40020800+0x60));
2. Before initializing the ADC registers, switch the ADC module to digital power supply: ADCIP_CTRL = 0x28;
3. Normal initialization of ADC register parameters

- N32G43x/N32L40x/N32L43x MR voltage adjustment

Figure 2-11 N32G43x/N32L40x/N32L43x MR Voltage Adjustment

1. Define the MR operation register: ADCIP_CTRL (*(UINT32_T*)(0x40020800+0x60));
2. Before initializing the ADC registers, switch the ADC module to digital power supply: ADCIP_CTRL = 0x28;
3. Normal initialization of ADC register parameters

2.4 ADC State Switching

In some application scenarios where the ADC working state needs to be switched multiple times, the ADC is repeatedly turned on and off. It is not enough to only operate the ON bit to enable or disable. It is also necessary to confirm the ADC status and determine whether the ADC state switch is completed before proceeding to the next step.

- ADC power-up

When the ADC is powered up for the first time, it is necessary to wait for the PowerUp process to complete. This can be confirmed by checking the RDY bit in ADC_CTRL3 to see if the power-up is complete, and then proceed with the ADC calibration.

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Figure 2-12 ADC Power-up

```
N32G45x: power-on operation for ADC, using ADC1 as an example：

/* Enable ADC1 */

ADC_Enable(ADC1, ENABLE);

/*Check ADC Ready*/

while(ADC_GetFlagStatusNew(ADC1,ADC_FLAG_RDY) == RESET);


N32G43x/N32L4xx: power-on operation for ADC：

/* Enable ADC */

ADC_Enable(ADC, ENABLE);

/*Check ADC Ready*/

while(ADC_GetFlagStatusNew(ADC,ADC_FLAG_RDY) == RESET);


N32G03x: power-on operation for ADC：

/* Enable ADC */

ADC_Enable(ADC, ENABLE);

/*wait ADC is ready to use*/
while(!ADC_GetFlagStatusNew(ADC, ADC_FLAG_RDY));
```

- ADC power-down

By clearing the ON bit, conversions can be stopped, and the ADC can be placed in power-down mode, where the ADC consumes very little power (only a few uA). When powering down the ADC, users should check the PDRDY bit in ADC_CTRL3 to confirm if the power-down is complete before proceeding to the next step.

When the ADC is disabled, it defaults to the power-down mode, where as long as it is not powered down, recalibration is not required as the calibration value is automatically retained by the ADC. To further reduce power consumption, the ADC has a deep sleep mode. When entering deep sleep mode after ADC DISABLE, the internal calibration value of the ADC is lost and recalibration is required.

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Figure 2-13 ADC Power-down

```
N32G45x: ADC power-down operation:

/* Disable ADC ADC1 */

ADC_Enable(ADC1, DISABLE);

/*Check ADC Power Down  Ready*/

while(ADC_GetFlagStatusNew(ADC1, ADC_FLAG_PD_RDY) == RESET);


N32G43x/N32L43x/N32L40x: ADC power-down operation:

/* Disable ADC ADC */

ADC_Enable(ADC, DISABLE);

/* Check ADC Power Down  Ready */

while(ADC_GetFlagStatusNew(ADC, ADC_FLAG_PD_RDY) == RESET);
```

- Wake-up in low power mode

  When the chip wakes up from low power mode, it is necessary to reset the ADC module clock and then perform the initialization configuration, otherwise it will affect the sampling accuracy of the ADC.

Figure 2-14 ADC Wake-up in Low Power Mode

After waking up in low power mode, re-initialize the ADC configuration, taking ADC1 as an example:

1. De-initialize ADC clock: ADC_DeInit(ADC1);
2. ADC initialization configuration;
3. Enable ADC calibration

2.5 ADC Error

In theory, the accuracy of an ADC is the smallest scale of the conversion code. However, in practical signal acquisition, various errors are superimposed. The actual accuracy of the ADC, after being affected by error interference, is $V_{ref}/4096 + V_{error}$.

The main factors affecting ADC errors are:

- Internal ADC errors, including offset error, gain error, differential nonlinearity error, integral nonlinearity error, etc.
- Reference voltage noise, in analog signal voltage acquisition, the reference voltage serves as the

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basis. Any noise on the reference voltage will cause the converted digital value to change.

- Analog input signal noise, electrical equipment can generate noise on the analog signal, causing fluctuations in the acquired values.
- I/O pin crosstalk, adjacent digital ports with high-frequency switching signals can introduce noise into the analog input signal of the ADC.
- Exceeding the chip specifications for analog signal voltage, if the analog I/O port input voltage is below -0.2V or above the VDD voltage, it will pull down or pull up the acquisition value.
- External signal impedance can affect sampling accuracy.
- Improper clock configuration, the ADC requires three clocks to be enabled, and any one of the clocks not configured correctly will affect the ADC accuracy.

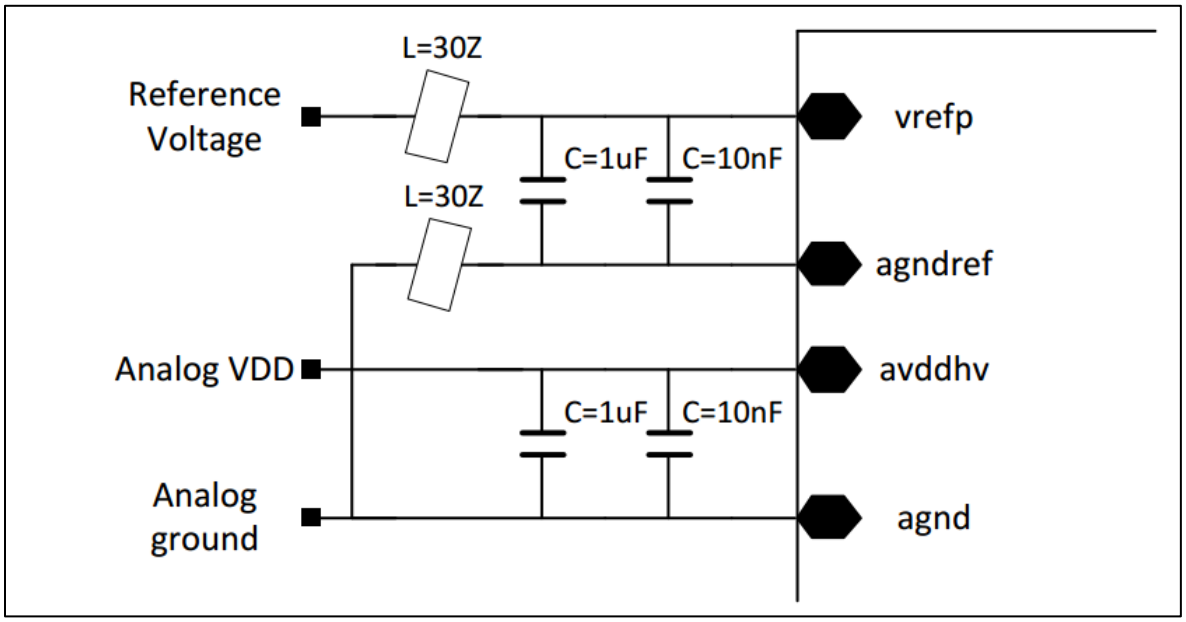
To achieve the best sampling accuracy for the ADC, we can take the following measures:

- Reduce power supply noise in PCB design

  Power supply side: small capacitors filter high-frequency noise, while large capacitors filter low-frequency noise. It is recommended to place ceramic capacitors near the analog power (VDDA and VSSA) pins. These capacitors can filter noise introduced by PCB traces. Capacitors with small values can respond to rapid changes in current and quickly discharge to adapt to fast current changes.

  Near the chip side: 10nF ceramic capacitor and 1uF tantalum capacitor/ceramic capacitor.

Figure 2-15 Power System Design



- Process signal sources
  - Average the sampled input signal values.

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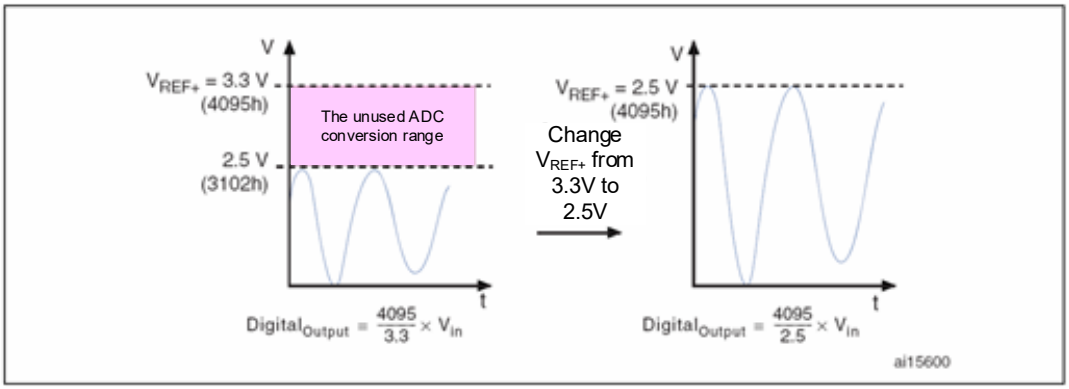
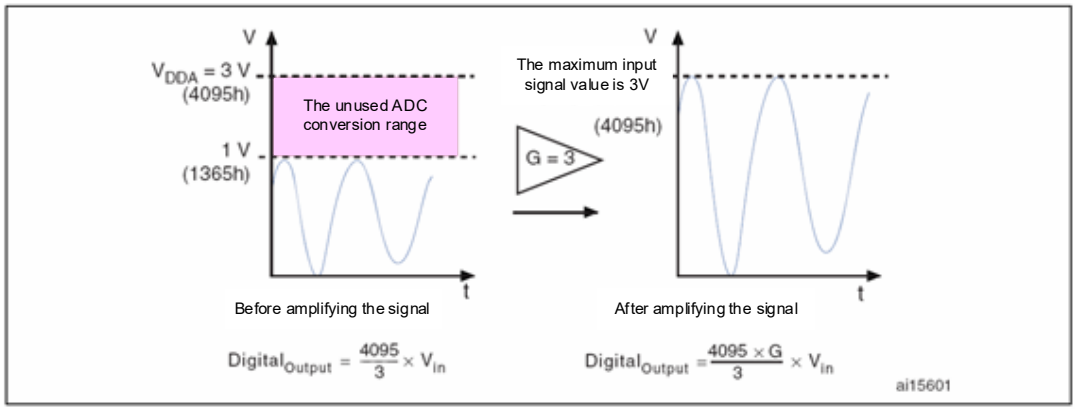
- Use a VREF that better matches the input range.

Figure 2-16 V_{ref} Range



- Add an external filter to the input signal.
- Increase the signal amplitude to better match the ADC range.

Figure 2-17 ADC Value Range



- The input signal voltage meets the chip specifications

  When using a certain ADC channel, negative voltage (such as -0.2V) should not be applied to other unused ADC sampling channels. Applying negative voltage to unused channels can lower the voltage of the normally sampled ADC channel, resulting in inaccurate data sampling. Similarly, when using a specific ADC channel, high voltage (greater than VDD voltage) should not be applied to other unused ADC sampling channels. Applying high voltage to unused channels can raise the voltage of the normally sampled ADC channel, leading to inaccurate data readings.

- Choose an appropriate sampling period

  During the sampling process of the ADC, it can actually be equivalent to sampling the external signal source through capacitance. In actual circuits, the switches themselves have impedance, and the I/O channel routing also has impedance.

  The setting of the sampling period needs to be calculated based on the external input impedance, which can be referenced by the following formula:

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$$R_{AIN} < \frac{T_s}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$$

Taking the N32G45x series as an example, with an ADC sampling clock of 72MHz and an external analog signal input impedance of 1000Ω, to match the appropriate sampling period, calculate:

$$1000 < \frac{T_s}{72000000 \times 5 \times 10^{-12} \times \ln(2^{12+2})} - 70$$

It is calculated that TS > 3.7, indicating that the software-configured sampling period needs to be greater than 3.7. (The parameters for the formula can be obtained from the chip's datasheet).

Taking the N32G430 series as an example: When using a 12-bit ADC with a sampling clock of 80MHz and an external analog signal input impedance of 10kΩ, to match the appropriate sampling period, it can be determined from the table that the minimum time is 815.9ns. The corresponding sampling time must be greater than 52.7 cycles (corresponding to the configuration value of ADC_SAMPT.SAMPx).

- Correctly configure the ADC clock

  The ADC requires three clocks: the operating clock, the sampling clock, and the counting clock. During ADC initialization, all three clocks need to be correctly configured, as improper configuration can affect the digital values of the signal acquisition conversion.

2.6 Small Signal / High Impedance Signal Measurement

- Small signal measurement

  When it is necessary to collect mV-level input signals, the following methods can be used:

  - Use an external amplification circuit to amplify the small input signal before outputting it to the ADC for acquisition.
  - Select the ADC fast channel and increase the ADC sampling period.
  - Add a capacitor with appropriate parameters to the input channel.
  - Use software oversampling and software filtering to extract the desired values that meet your requirements.

- High impedance signal measurement

  When it is necessary to collect high-impedance signals, capacitors can be added on the channel in hardware, and the sampling period can be increased in software.

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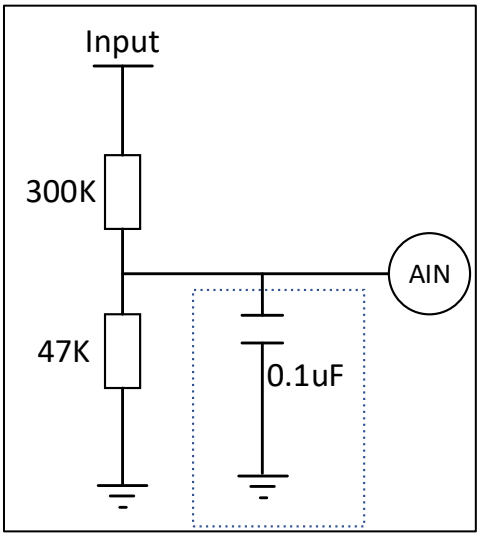
Figure 2-18 High Impedance Signal Measurement



By increasing the sampling rate and adding external capacitors, the ADC sampling accuracy can be significantly improved when collecting the input signal shown in the figure. Taking N32G03x as an example:

Table 2-1 Measurement

Sampling Period	240	72	42	6
Connect a 0.1uf Capacitor	0.16%	0.74%	-1.69%	0.78%
Do Not Connect a 0.1uf Capacitor	0.08	0.47	-6.88%	-42.23&

2.7 Differential Calculation Formula

Some series of ADCs support differential inputs, where the positive and negative terminals of the differential input need to be adjacent ADC channels (see Figure 2-14 ADC Channel and PIN Relationship). This can be configured in the ADC_DIFSEL register for differential mode.

The differential signal input range is between 0 and V_{REF}, the output range is $-V_{REF}$ to $+V_{REF}$, and the common-mode voltage range is $\frac{VDD}{2}$-0.18~$\frac{VDD}{2}$+0.18.The conversion value can be calculated as follows: ADC_DAT = 4095 * $(\frac{1}{2}*\frac{Vin}{vref}+\frac{1}{2})$. Example:

Table 2-2 Voltage Range

ADC_DAT	**VINP**	**VINN**	**VIN**	**VREF**
0	0V	3.3V	-3.3V	3.3V

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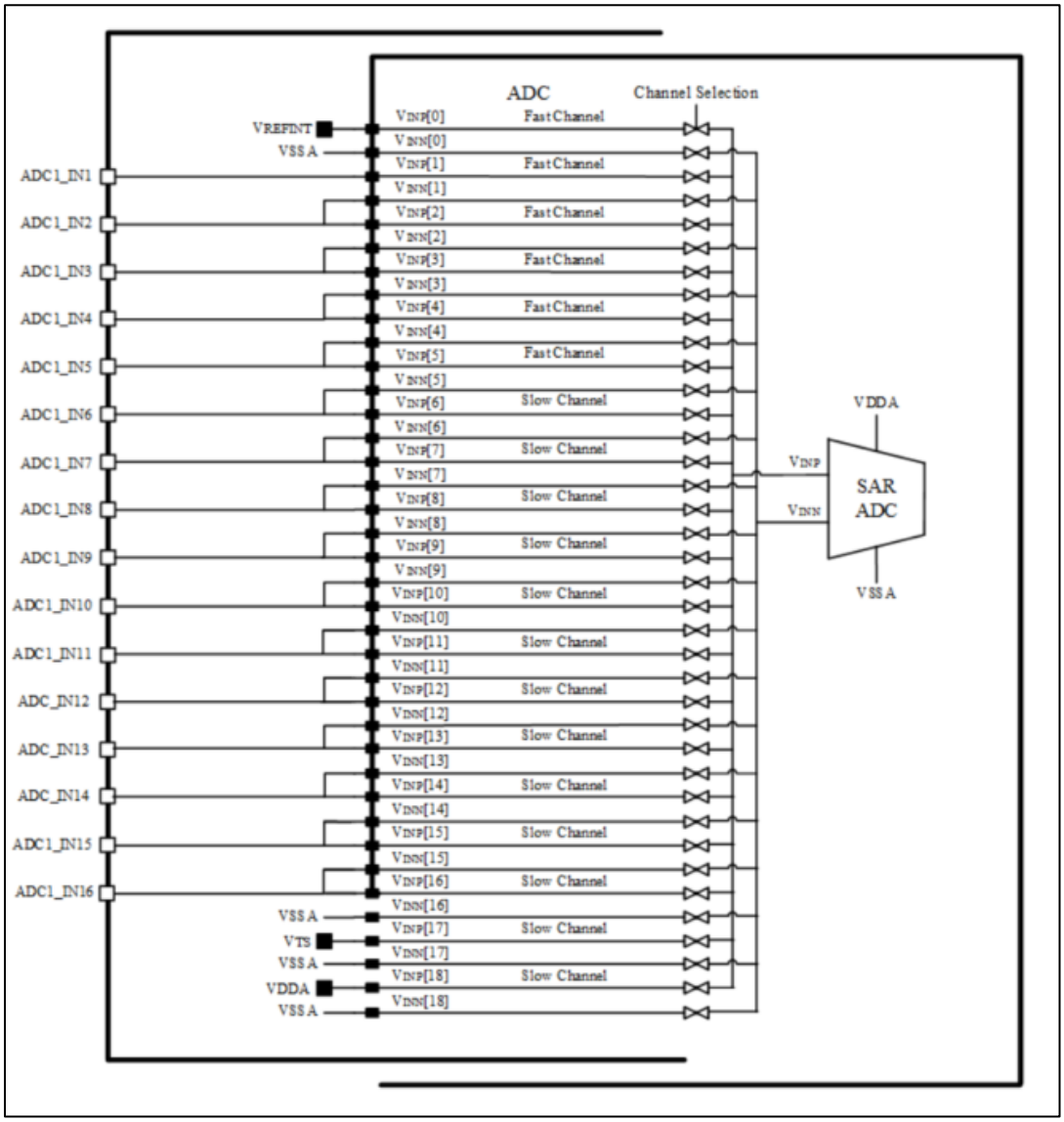
2048	1.65V	1.65V	0V	3.3V
4095	3.3V	0V	3.3V	3.3V

Figure 2-19 ADC Channel and PIN Relationship



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3. Conclusion

This application note mainly introduces the ADC module, helping users quickly familiarize themselves with the application and configuration of the ADC.

If there are any questions regarding the parameters mentioned in this document, please refer to the product datasheet for accurate information.

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4. Version History

Version	Date	Changes
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