N32G4FRxC/xE Datasheet

N32G4FR series uses a 32-bit ARM® Cortex®-M4F core, operating frequency up to 144MHz, supporting floating-point unit and DSP instructions. The devices integrates up to 512KB of embedded flash and 144KB of SRAM, suitable for secure storage of fingerprint information. The series features rich of high-performance interfaces, including 2x12bit 4.7Msps ADC, 2x1Msps 12bit DAC, multi-channel communication interfaces(U(S)ART, I2C, SPI, QSPI, USB, CAN, etc), 1x SDIO interface, digital video (DVP) interface, supporting mainstream semiconductor fingerprint and optical fingerprint sensor. It also features a built-in hardware acceleration engine for cryptographic algorithm.

Key Features

- **CPU Core**
  - 32-bit ARM® Cortex®-M4 +FPU, single-cycle hardware multiplication and divide instructions, support DSP instruction and MPU
  - Built-in 8KB instruction Cache supports Flash acceleration unit for zero-wait program execution
  - Maximum frequency of 144MHz, 180DMIPS
- **Memories**
  - Up to 512KBytes of embedded Flash memory with ECC
    - Support encryption multi-user partition management and data protection
    - 100,000 erase/write cycles and 10 years data retention
  - Up to 144KBytes of SRAM (including 16K Byte Retention RAM). The Retention RAM supports hardware parity check
- **Clock**
  - HSE: 4MHz~32MHz high-speed external crystal oscillator
  - LSE: 32.768KHz low-speed external crystal oscillator
  - HSI: high-speed internal RC 8MHz
  - LSI: low-speed internal RC 40KHz
  - Built-in high speed PLL
  - MCO: Support 1-channel clock output, which can be configured as SYSCLK, HSE, HSI or PLL divisional output
- **Reset**
  - Support power-on/power-down/brown-out/external pin reset
  - Support watchdog reset, software reset
- **Communication Interface**
  - 7x U(S)ART interfaces with maximum rate up to 4.5 Mbps
    - 3x USART interfaces (supporting ISO7816, IrDA, LIN)
    - 4x UART interfaces

- 3x SPI interfaces with speed up to 36 MHz, 2 of which support I2S communication
- 1x QSPI interface up to 144 Mbps
- 4x I2C interfaces (Master/Slave) with speed up to 1 MHz where slave mode support dual address response
- 1x USB2.0 Full Speed Device interface
- 2x CAN 2.0B bus interfaces
- 1x SDIO interface, supports SD/SDIO/MMC format
- 1x DVP (Digital Video Port) interface

- **High Performance Analog Interface**
  - 2 x 12-bit ADCs with 4.7Msps,
    - Configurable as12/10/8/6bit mode
    - Sampling rate up to 8.9Msps in 6bit mode
    - Up to 16 external single-ended input channels, support differential mode
  - 2x 12-bit DAC with sampling rate of 1Msps
  - Supports external reference voltage source
  - Analog voltage operation from 1.8~3.6V
- **GPIO**
  - Up to 65 GPIOs
  - Support multiplexed functions
  - Most GPIOs are 5V tolerant
- **DMA Controllers**
  - 2x high-speed DMA controllers
  - Each controller support 8 channels
  - Channel source address and destination address can be configured arbitrarily
- **Real-time clock (RTC)**
  - Support leap-year calendar, alarm events, periodic wake-up
  - Support internal and external clock calibration
- **Timers**
  - 2x 16-bit advanced timers with maximum control precision of 6.9ns
    - Support input capture, complementary output, quadrature encoding input, etc
    - Each timer has 4 independent channels, 3 of which support 6-channel complementary PWM output
  - 4x 16-bit general-purpose timers
    - Support input capture/output comparison /PWM output/One-pulse output
    - Each with 4 independent channels
  - 2x 16-bit basic timers
  - 1x 24bit SysTick timer

  - 1x 7bit Window Watchdog (WWDG)
  - 1x 12bit Independent Watchdog (IWDG)
- **Programming mode**
  - Support SWD/JTAG debugging interface
  - Support UART, USB Bootloader
- **Security Features**
  - Built-in hardware acceleration engine for cryptographic algorithm
  - Support AES, DES, SHA and MD5 algorithms
  - Flash storage encryption, Multi-user partition management (MMU)
  - True random number generator (TRNG)
  - CRC16/32 operation
  - Support write protection (WRP), multiple read protection (RDP) levels (L0/L1/L2)
  - Support secure boot, encrypted download of programs, and secure update
  - Support external clock failure detection, anti-tamper detection
- **96-bit UID and 128-bit UCID**
- **Operating Conditions**
  - Operating voltage range: 1.8V~3.6V
  - Operating temperature range: -40°C ~105°C
  - ESD: ±4KV (HBM model), ±1KV(CDM model)
- **Packages**
  - QFN32(4mm x 4mm)
  - QFN40(5mm x 5mm)
  - LQFP64(10mm x 10mm)
  - LQFP80(12mm x 12mm)
- **Ordered Information**

Reference	Part Number
N32G4FRxC	N32G4FRKCQ7 N32G4FRHCQ7
N32G4FRxE	N32G4FRKEQ7 N32G4FRHEQ7 N32G4FRREL7 N32G4FRMEL7

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1 Introduction

The N32G4FR microcontrollers series features a high-performance 32-bit ARM® Cortex®-M4F core with an integrated floating point operation unit (FPU) and digital signal processing (DSP). It supports parallel computing instructions and operates at a maximum frequency of 144MHz. The embedded encrypted memory Flash can hold up to 512KB, supporting multi-user partition permission management. Additionally, it includes up to 144KB of embedded SRAM.

The device is equipped with internal high-speed AHB bus, along with two low-speed peripherals clock bus APB and bus matrix. It offers support up to 65 general I/Os and features a diverse range of high-performance analog interfaces. These include 2 12-bit 5Msps ADC with up to 16 external input channels, 2 12-bit DAC with a 1Msps sampling rate.

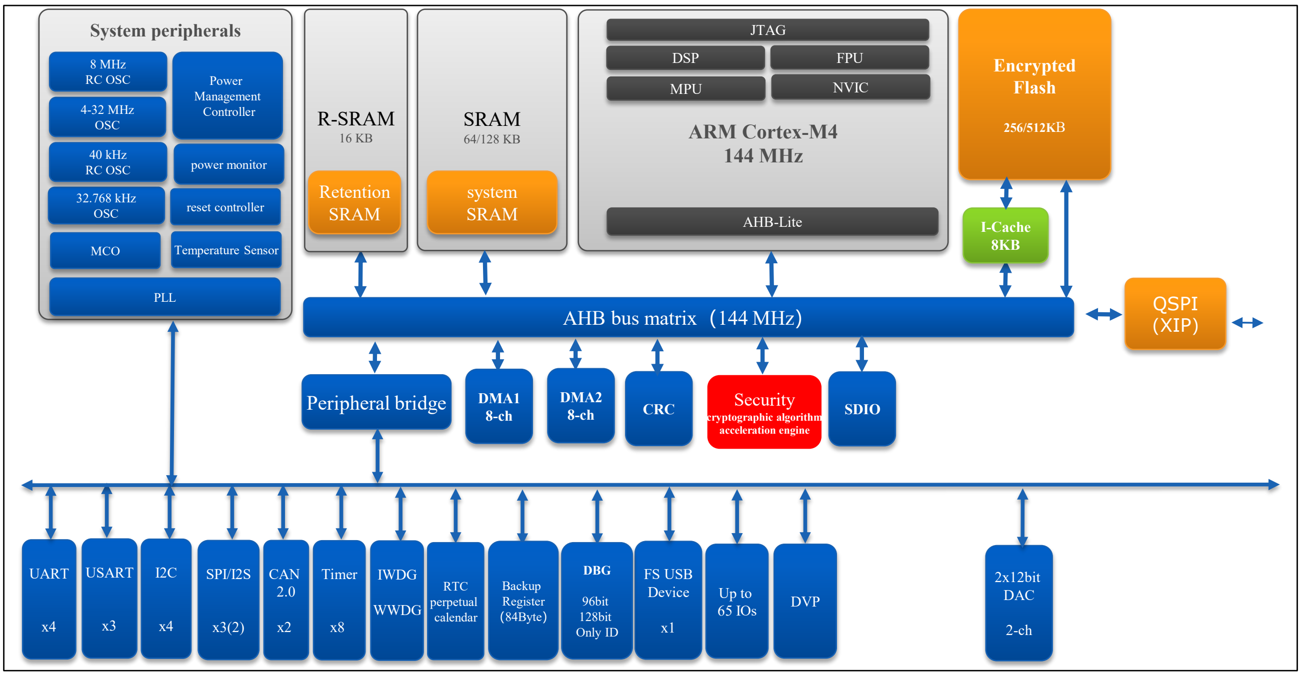
For digital communication , the N32G4FR provides 7x U(S)ART, 4x I2C, 3x SPI, 2x I2S, 1x QSPI, 1x USB 2.0 device, 2x CAN 2.0B, 1x SDIO communication interface, 1x Digital Camera Interface (DVP). It also integrates a hardware acceleration engine, supporting various international encryption algorithms.

The N32G4FR operates reliably in the temperature range of -40°C to +105°C and supply voltage from 1.8V to 3.6V. It offers multiple power modes to cater to low-power applications. Available in 4 different packaging forms (QFN32/QFN40/LQFP64/LQFP80), the peripheral configuration varies based on the package type.

These rich peripheral configurations, high-performance processors and low power consumption make the N32G4FR series microcontrollers suitable for various application scenarios, including fingerprint modules, fingerprint locks, fingerprint access control, fingerprint attendance machines and other biometric fingerprint identification applications.

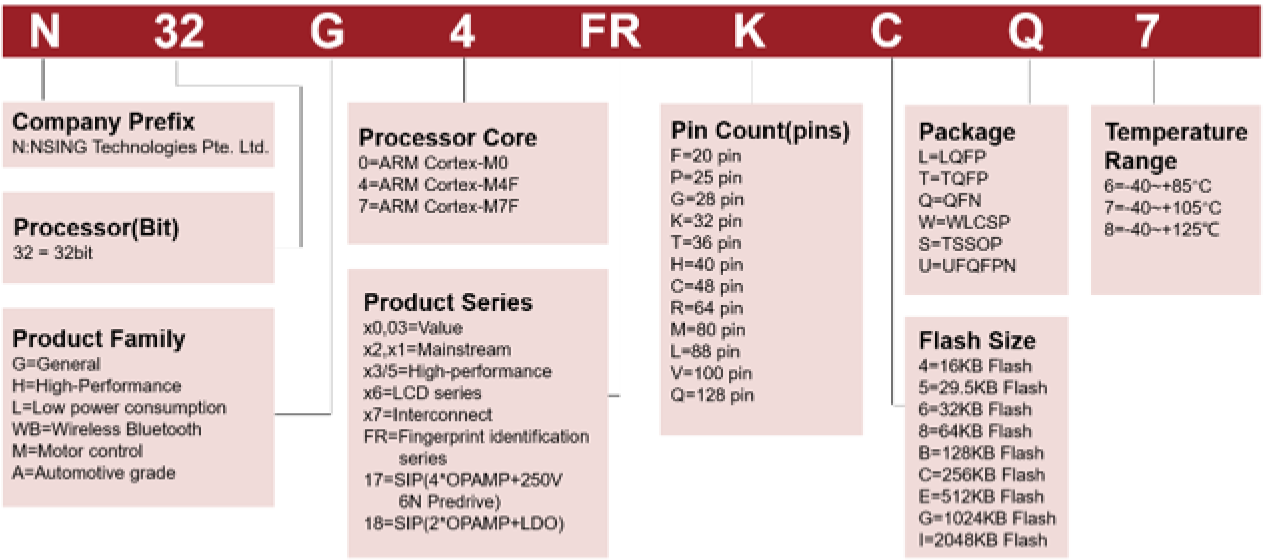
Figure 1-1 the block diagram of this series of products is given.

Figure 1-1 Block Diagram of N32G4FR Series



1.1 Naming Convention

Figure 1-2 N32G4FR Series Naming Convention



Company Prefix
N:NSING Technologies Pte. Ltd.

Processor(Bit)
32 = 32bit

Product Family
G=General
H=High-Performance
L=Low power consumption
WB=Wireless Bluetooth
M=Motor control
A=Automotive grade

Processor Core
0=ARM Cortex-M0
4=ARM Cortex-M4F
7=ARM Cortex-M7F

Product Series
x0,03=Value
x2,x1=Mainstream
x3/5=High-performance
x6=LCD series
x7=Interconnect
FR=Fingerprint identification series
17=SIP(4*OPAMP+250V 6N Predrive)
18=SIP(2*OPAMP+LDO)

Pin Count(pins)
F=20 pin
P=25 pin
G=28 pin
K=32 pin
T=36 pin
H=40 pin
C=48 pin
R=64 pin
M=80 pin
L=88 pin
V=100 pin
Q=128 pin

Package
L=LQFP
T=TQFP
Q=QFN
W=WLCSP
S=TSSOP
U=UFQFPN

Flash Size
4=16KB Flash
5=29.5KB Flash
6=32KB Flash
8=64KB Flash
B=128KB Flash
C=256KB Flash
E=512KB Flash
G=1024KB Flash
I=2048KB Flash

Temperature Range
6=-40~+85°C
7=-40~+105°C
8=-40~+125℃

1.2 Product Configurations

Table 1-1 N32G4FR Series Product Configuration

<table>
<tr><th colspan="2">Device</th><th colspan="2">N32G4FRKC/E</th><th colspan="2">N32G4FRHC/E</th><th>N32G4FRRE</th><th>N32G4FRME</th></tr>
<tr><td colspan="2">Flash Capacity (KB)</td><td>256</td><td>512</td><td>256</td><td>512</td><td>512</td><td>512</td></tr>
<tr><td colspan="2">SRAM Capacity (KB)</td><td>144</td><td>144</td><td>144</td><td>144</td><td>144</td><td>144</td></tr>
<tr><td colspan="2">CPU Frequency</td><td colspan="6">ARM® Cortex®-M4F @144MHz,180DMIPS</td></tr>
<tr><td colspan="2">Operating Condition</td><td colspan="6">1.8~3.6V/-40~105℃</td></tr>
<tr><td rowspan="3">Timers</td><td>General</td><td colspan="6">4</td></tr>
<tr><td>Advanced</td><td colspan="6">2</td></tr>
<tr><td>Basic</td><td colspan="6">2</td></tr>
<tr><td rowspan="10">Communication interface</td><td>SPI(1)</td><td colspan="2">2</td><td colspan="4">3</td></tr>
<tr><td>I2S(1)</td><td colspan="2">1</td><td colspan="4">2</td></tr>
<tr><td>QSPI</td><td colspan="6">1</td></tr>
<tr><td>I2C</td><td colspan="4">3</td><td colspan="2">4</td></tr>
<tr><td>USART</td><td colspan="2">1</td><td colspan="2">2</td><td colspan="2">3</td></tr>
<tr><td>UART</td><td colspan="2">3</td><td colspan="4">4</td></tr>
<tr><td>USB</td><td colspan="6">1</td></tr>
<tr><td>CAN</td><td colspan="2">1</td><td colspan="4">2</td></tr>
<tr><td>SDIO</td><td colspan="4">No(2)</td><td colspan="2">1</td></tr>
<tr><td>DVP</td><td colspan="2">No(2)</td><td colspan="4">1</td></tr>
<tr><td colspan="2">GPIO</td><td colspan="2">24</td><td colspan="2">32</td><td>51</td><td>65</td></tr>
<tr><td colspan="2">DMA</td><td colspan="6">2</td></tr>
<tr><td colspan="2">DMA Channels</td><td colspan="6">16Channel</td></tr>
<tr><td colspan="2">12bit ADC</td><td colspan="2">2</td><td colspan="2">2</td><td>2</td><td>2</td></tr>
<tr><td colspan="2">ADC Channels</td><td colspan="2">7Channel</td><td colspan="2">11Channel</td><td>16Channel</td><td>16Channel</td></tr>
<tr><td colspan="2">12bit DAC</td><td colspan="6">2</td></tr>
<tr><td colspan="2">DAC Channels</td><td colspan="6">2Channel</td></tr>
<tr><td colspan="2">Algorithm Support</td><td colspan="6">DES/3DES, AES, SHA1/SHA224/SHA256, MD5, CRC16/CRC32, TRNG</td></tr>
<tr><td colspan="2">Security Protection</td><td colspan="6">Read-write protection (RDP/WRP), Storage encryption, Partition protection, Secure boot</td></tr>
<tr><td colspan="2">Package</td><td colspan="2">QFN32</td><td colspan="2">QFN40</td><td>LQFP64</td><td>LQFP80</td></tr>
</table>

Notes:

(1) SPI2 and SPI3 interfaces can flexibly switch between SPI mode and I2S audio mode.

(2) Not supported

2 Function Overview

2.1 Processor Core

The N32G4FR series integrates the latest generation of embedded ARM® Cortex®-M4F processor. It features a floating point processing unit (FPU), DSP and parallel computing instructions, providing excellent performance of 1.25DMIPS/MHz. At the same time, its efficient signal processing capabilities are combined with low power consumption, low cost, and ease of use. It is able to be used in application scenarios that require a blend of control and signal processing capabilities while being user-family.

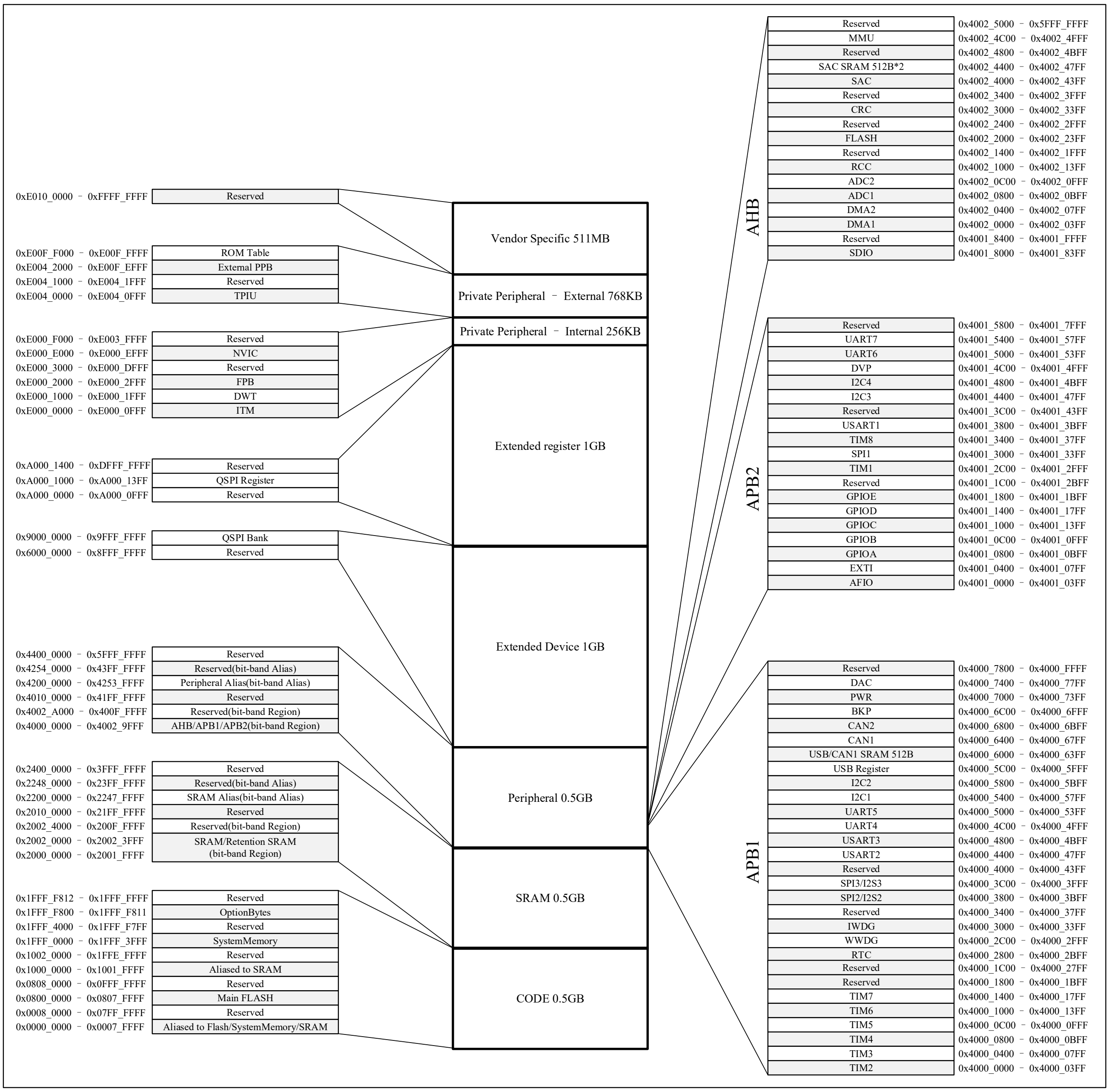
ARM® Cortex®-M4F 32-bit reduced instruction set processor offers exceptional code efficiency.

Note: Cortex®-M4F is backward compatible with Cortex®-M3 code.

2.2 Memories

The N32G4FR series include embedded encrypted Flash memory and embedded SRAM.

Figure 2-1 Memory Map



2.2.1 Embedded FLASH Memory

The integrated encrypted Flash memory ranges from 256K to 512K bytes, utilized for storing programs and data. The page size is 2K byte supporting page erasing, word writing, word reading, half-word reading, and byte reading operations.

It supports storage encryption protection, enabling automatic encryption during writing and decryption during reading (including program execution operation).

User partition management is supported, allowing for a maximum of 2 user partitions, different users cannot access each other's data (only executable code can be accessed).

2.2.2 Embedded SRAM

The chip integrates a built-in SRAM of up to 144K bytes, comprising SRAM and Retention SRAM(RET-SRAM). RET-SRAM has a size of 16K bytes and can retain data in VBAT and STANDBY modes (user-configurable to retain or not retain data). RET-SRAM can retain data by default in other operation modes (RUN/SLEEP/STOP0/STOP2), and PWR is required to control and manage its Retention.

2.2.3 Nested Vector Interrupt Controller (NVIC)

The built-in Nested Vector Interrupt Controller can handle up to 86 maskable interrupt channels (excluding the 16 Cortex®-M4F interrupts) and 16 priorities.

- The tightly coupled NVIC ensures low-latency interrupt response processing
- Interrupt vector entry address directly access the kernel
- Tightly coupled NVIC interface
- Allows early processing of interrupts
- Processing late arriving higher-priority interrupts
- Support interrupt tail-chaining functionality
- Automatically saves processor state
- Automatically resumes when interrupt returns with no instruction overhead

This module provides flexible interrupt management with minimal interrupt latency.

2.3 External Interrupt/Event Controller (EXTI)

The extended interrupt/event controller contains 21 edge detectors used for generating interrupt/event requests. Each interrupt line can be independently configured with its trigger event (rising edge, falling edge or both) and can be individually masked. A pending register that maintains the state of all interrupt requests. EXTI can detect clock pulse with widths smaller than internal APB2 clock cycle. Up to 65 general-purpose I/O ports are connected to 16 external interrupt lines.

2.4 Clock System

The device offers various clock options for users to choose from, including:

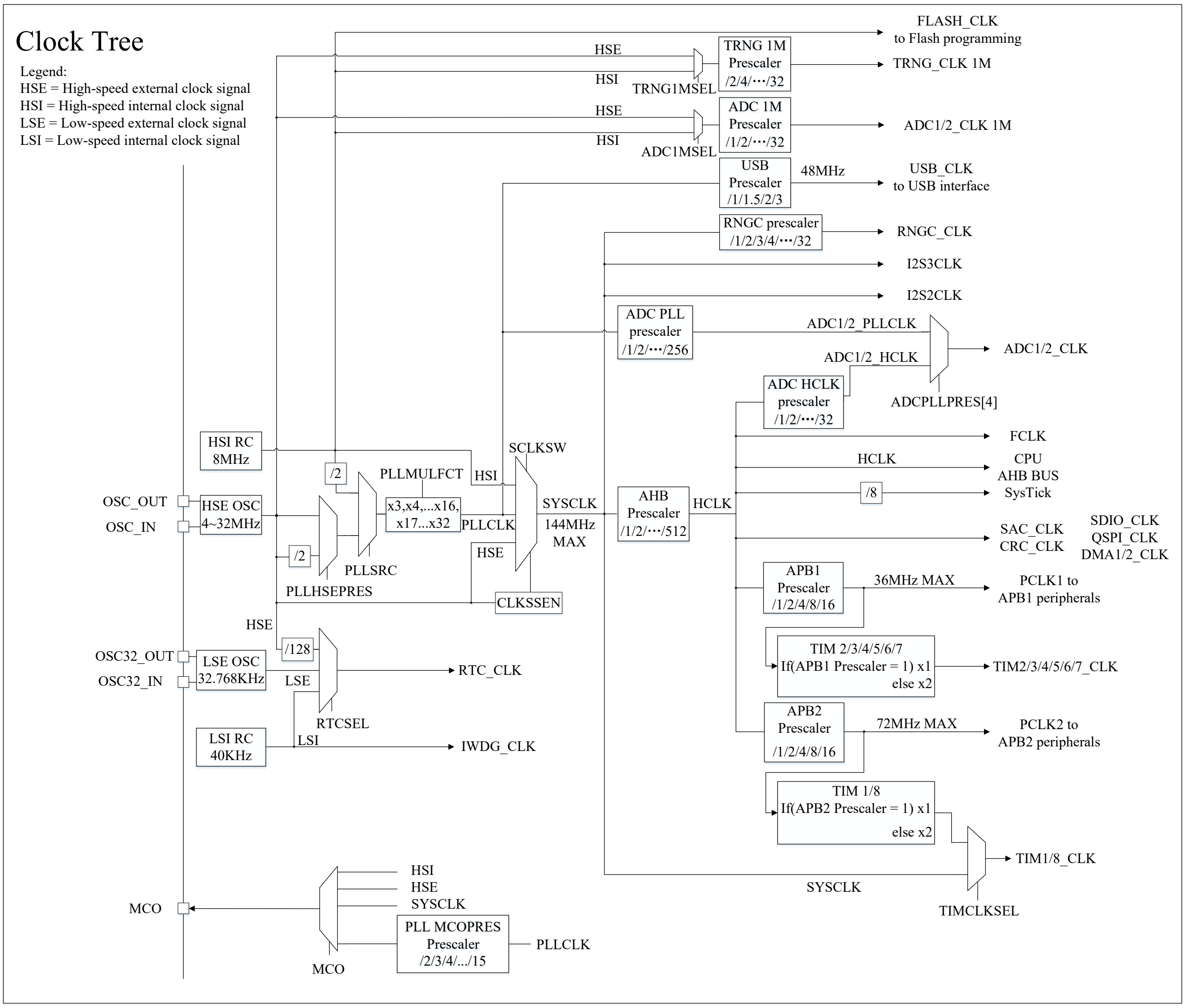
- High speed internal RC oscillator (HSI) at 8MHz
- Low speed internal RC oscillator (LSI) at 40KHz
- High speed external crystal oscillator (HSE) range from 4MHz to 32MHz
- Low speed external crystal oscillator (LSE) at 32.768 KHz
- Phase-Locked Loop (PLL)

Upon reset, the internal HSI clock is set as the default CPU clock, user can choose the external HSE clock with fail function. When an external clock failure is detected, it will be isolated, the system will automatically switch to HSI.

If interrupts are enabled, software can receive corresponding interrupts. Similarly the system will automatically switch to HSI when the PLL clock was adopted and external oscillator fails.

Multiple prescalers are used to configure the AHB frequency, high speed APB (APB2) and low-speed APB (APB1) regions. The AHB has a maximum frequency of 144 MHz, APB2 has a maximum frequency of 72 MHz and APB1 has a maximum frequency of 36MHz. Refer to Figure 2-2 Clock tree diagram.

Figure 2-2 Clock Tree



When HSI is used as the input clock for PLL, the maximum system clock frequency is limited to 128MHz.

When using the USB function, both HSE and PLL must be used and the CPU frequency must be 48MHz, 72MHz, 96MHz or 144MHz.

2.5 Boot Modes

During startup, the BOOT mode after reset can be selected through the BOOT0/1 pin.

- BOOT from FLASH Memory.
- BOOT from System Memory
- BOOT from embedded SRAM

The Bootloader is stored in the system memory and can program the flash memory through USART1 and USB interface.

2.6 Power Supply Scheme

- V_{DD}= 1.8~3.6V: The V_{DD} pin supplies power to the I/O pin and internal voltage regulator.
- V_{DDA}= 1.8~3.6V:The V_{DDA} provides power supply for ADC and DAC.
- V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS} respectively.
- V_{BAT}= 1.8~3.6V: When V_{DD} is turned off, it supplies power to RTC, external 32KHz oscillator and backup register.

For more information on how to connect the power supply pins, see Figure 4-3 Power supply scheme。

2.7 Reset

The power-on reset (POR) and power-down reset (PDR) circuits are integrated inside. This part of the circuit ensure that the system works stably when the power supply exceeds 1.8V. When V_{DD} falls below a set threshold ($V_{POR/PDR}$) , the device goes into reset state without using an external reset circuit.

2.8 Programmable Voltage Detector

The device has a built-in programmable voltage detector (PVD), which monitors the power supply of V_{DD}/V_{DDA} and compares it with the threshold V_{PVD}. When V_{DD} is lower or higher than the threshold V_{PVD}, an interrupt will be generated. The interrupt handler can send a warning message, and the PVD function needs to be enabled through the program. See Table 4-6 for values of $V_{POR/PDR}$ and V_{PVD}.

2.9 Voltage Regulator

The voltage regulator operates in the follow modes:

- The MCU operates in RUN, SLEEP modes: Main voltage regulator(MR) operates in normal mode
- The MCU operates in STOP0 modes: Main voltage regulator(MR) can select to operate in normal mode or low power mode
- The MCU operates in STOP2, STANDBY mode: Main voltage regulator(MR) shut down and backup domain voltage regulator(BKR) turn on

After the chip is reset, the main voltage regulator(MR) operates in normal mode by default.

2.10 Low Power Mode

The N32G4FR series supports five low-power modes.

- SLEEP mode

In SLEEP mode, only the CPU is stopped, all peripherals remain operational. They can wake up the CPU when an interrupt/event occurs.

- STOP0 mode

In STOP0 mode, the device can achieve lower power consumption while maintaining the contents of the SRAM and registers. In this mode, the clocks in the main power domain are turned off, such as PLL, HSI, HSE, and the main voltage regulator can select to operate in normal mode or in low power mode.

Wake-up: The device can be woken up from STOP0 mode by any of the 16 external EXTI signals (I/O related), PVD output, RTC wake-up, RTC alarm or wake-up signal from USB.

- STOP2 mode

In STOP2 mode, all the core digital logic areas are powered off.

  - The main voltage regulator(MR) is turned off
  - HSE/HSI/PLL is turned off

- CPU registers are retained
- LSE/LSI can be configured to operate
- All GPIOs are retained
- The peripheral I/O multiplexing functions are not retained
- 16K bytes RET-SRAM can be retained, while the data in other SRAM and registers will be lost
- The 84-byte backup register are retained

Wake-up: The device can be woken up from STOP2 mode by any of the 16 external EXTI signals (I/O related), PVD output, RTC periodic wake up, RTC alarm, RTC tamper, NRST reset, IWDG reset.

- STANDBY mode

In STANDBY mode, the device can achieve a lower current consumption. The internal voltage regulator is turned off, as well as PLL, HSI RC oscillator and HSE crystal oscillator. Upon entering STANDBY mode, the contents of the main registers will be lost while the contents of the backup registers can be retained, RET-SRAM can be retained, the Standby circuitry continues to function.

External reset signal on NRST, IWDG reset, rising edge on the WKUP pin, RTC wake-up and RTC alarm can wake up the device from STANDBY mode.

- VBAT mode

At any time, whenever VDD is powered down, it will automatically enter VBAT mode. In VBAT mode, except for NRST, PA0-WKUP, PC13_TAMPER, PC14, PC15, most I/O pins are in high impedance state.

Note: RTC, IWDG and corresponding clock will not be stopped when entering STANDBY mode.

2.11 Direct Memory Access (DMA)

The device integrates 2 flexible general-purpose DMA controllers that supports 8 DMA channels. It can manage data transfers from memory to memory, peripherals to memory, and memory to peripherals. These 2 DMA controllers support the management of circuit buffers, thus avoiding the interrupts when the controller reaches the end of the buffer.

Each channel has dedicated hardware DMA request logic and each channel can be triggered by software. The transmission length, the source address and destination address of each channel can be set separated by software.

DMA can be used with major peripherals: SPI, I2C, USART, TIMx (Advanced/General/Basic Timers), DAC, I2S, SDIO, ADC, DVP and QSPI.

2.12 Real Time Clock (RTC)

The RTC is a set of continuously running counters integrated with a built-in clock module that provides a perpetual calendar functionality, as well as alarm interrupt and periodic interrupt (with a minimum of 2 clock cycles) . The RTC can be powered through V_{DD} or V_{BAT} pin. It is powered by V_{DD} when V_{DD} is valid. Otherwise, it is powered by V_{BAT} pin. The power source is automatically selected and switched by hardware. The RTC will not be reset by system or power reset sources, nor will it be reset when waking up from STANDBY mode.

The RTC can be driven by either a 32.768KHz external crystal oscillator, an internal low-power 40KHz RC oscillator, or a high-speed external clock with 128 prescalar factors.

For application scenarios that requiring very high timing accuracy, it is recommended to use an external 32.768KHz clock as the clock source, to compensate for the clock deviation of natural crystals, a 256Hz signal can be output to calibrate the clock of RTC.

The RTC features a 22-bit prescaler for a time based clock. By default, when the clock is set to 32.768kHz, it generates a 1-second time reference. In addition, the RTC can be used to trigger wake-up in low-power mode.

2.13 Timers and Watchdogs

Up to 2 advanced control timers, 4 general-purpose timers and 2 basic timers, 2 watchdog timers and 1 system tick timer.

The following table compares the functions of advanced control timer, general-purpose timer and basic timer:

Table 2-1 Comparison of Timer Functions

Timer	Counter Resolution	Counter Type	Prescaler Factor	Generate DMA Requests	Capture/Compare Channels	Complementary Output
TIM1 TIM8	16	Up, down, up/down	Any integer between 1 and 65536	Y	4	Y
TIM2 TIM3 TIM4 TIM5	16	Up, down, up/down	Any integer between 1 and 65536	Y	4	N
TIM6 TIM7	16	Up	Any integer between 1 and 65536	Y	0	N

2.13.1 Basic Timer (TIM6 and TIM7)

Basic timers TIM6 and TIM7 each contain a 16-bit auto-reload counter. These two timers are independent of each other and do not share any resources. The basic timer can provide a time base for general purpose timers. The basic timer is directly connected to the DAC inside the chip and drives the DAC directly through the trigger output.

Main features:

- 16-bit auto-reload up-counting counters
- 16-bit programmable prescaler (The prescaler factor can be configured with any value between 1 and 65536)
- Synchronization circuit for triggering DAC
- Event that generate the interrupt/DMA is as follows:
  - Update event

2.13.2 General-purpose Timer (Timx)

The general-purpose timers (TIM2, TIM3, TIM4 and TIM5) is mainly used in the following occasions: counting the input signal, measuring the pulse width of the input signal and generating the output waveform, etc.

Main features:

- 16-bit auto-reload counters. (It can realize up-counting, down-counting, up/down counting)
- 16-bit programmable prescaler. (The prescaler factor can be configured with any value between 1 and 65536)
- TIM2, TIM3, TIM4 and TIM5 up to 4 channels.
- Channel’s working modes: PWM output, output compare, one-pulse mode output, input capture.
- The events that generate the interrupt/DMA are as follows:
  - Update event
  - Trigger event
  - Input capture
  - Output compare
- Timer can be controlled by external signal
- Timers can be linked together internally for timer synchronization or chaining
- Incremental (quadrature) encoder interface: used for tracking motion and resolving rotation direction and position

- Hall sensor interface: used to do three-phase motor control

2.13.3 Advanced Control Timer (TIM1 and TIM8)

The advanced control timers (TIM1 and TIM8) is mainly used in the following purposes: counting the input signal, measuring the pulse width of the input signal and generating the output waveform, etc.

Advanced timers have complementary output function with dead-time insertion and break function. They are suitable for motor control.

Main features:

- 16-bit auto-reload counters. (It can realize up-counting, down-counting, up/down counting).
- 16-bit programmable prescaler. (The prescaler factor can be configured with any value between 1 and 65536)
- Programmable Repetition Counter
- TIM1 and TIM8 up to 6 channels
- 4 capture/compare channels:
  - PWM output
  - Output compare
  - One-pulse mode output
  - Input capture
- The events that generate the interrupt/DMA are as follows:
  - Update event
  - Trigger event
  - Input capture
  - Output compare
  - Break input
- Complementary outputs with programmable dead-time.
  - For TIM1 and TIM8, channel 1,2,3 support this feature
- Timers can be controlled by external signal
- Timers can be linked together internally for timer synchronization or chaining
- Incremental (quadrature) encoder interface: used for tracking motion and resolving rotation direction and position;
- Hall sensor interface: used to do three-phase motor control

2.13.4 SysTick Timer (SysTick)

This timer is dedicated to the real-time operating systems and can also be used as a standard down counter.

Main features:

- 24-bit down counter
- Automatic reloading function
- A maskable system interrupt is generated when the counter is 0
- Programmable clock source

2.13.5 Watchdog (WDG)

Support for two watchdog independent watchdog (IWDG) and window watchdog (WWDG). Two watchdogs provide increased security, time accuracy, and flexibility in use.

Independent Watchdog (IWDG)

The independent watchdog is based on a 12-bit down-counter and a 3-bit prescaler. It is driven by a separate low-speed RC oscillator that remains active even if the master clock fails and operates in STOP0, STOP2 and STANDBY modes. Once activated, if the watchdog is not fed (clears the watchdog counter) within the set time, the IWDG generates a reset when the counter counts to 0x000. It can be used to reset the entire system in the event of an application problem, or as a free timer to provide time-out management for applications. It is hardware or software configurable through the option byte. Reset and low power wake up are available.

Window Watchdog (WWDG)

A window watchdog is usually used to detect software failures caused by an application deviating from the normal running sequence due to external interference or unforeseen logical conditions. Unless the down-counter value is flushed before the T6 bit becomes zero, the watchdog circuit generates an MCU reset when the preset time period is reached. If the 7-bit down-counter value (in the control register) is flushed before the down-counter reaches the window register value, then an MCU reset will also occur. This indicates that the down-counter needs to be refreshed in a finite time window.

Main features:

- The clock of the window watchdog (WWDG) is obtained by dividing the APB1 clock
- Programmable free-running counter
- Reset condition:
  - When the down-counter is less than 0x40, a reset is occurs (if the watchdog is started)
  - A reset occurs when the down-counter is reloaded outside the window (if the watchdog is started)
  - If the watchdog is enabled and interrupts are allowed, an early wake up interrupt (EWINT) occurs when the down-counter equals 0x40, which can be used to reload the counter to avoid WWDG reset

2.14 I2C Bus Interface

The device integrates up to 4 independent I2C bus interfaces, which provide multi-host function and control all I2C bus-specific timing, protocol, arbitration and timeout. I2C bus interface supports multiple communication rate modes (up to 1MHz), supports DMA operations and is compatible with SMBus 2.0. The I2C module provides multiple functions, including CRC generation and verification, System Management Bus(SMBus), and Power Management Bus (PMBus).

Main features:

- Multi-master function: this module can be used as master device or slave device
- I2C master device function:
  - Generate a clock
  - Generate start and stop signals
- I2C slave device function:
  - Programmable address detection
  - The I2C interface supports 7-bit or 10-bit addressing and dual-slave address responses capability in 7-bit slave mode
  - Stop bit detection
- Generate and detect 7-bit / 10-bit addresses and broadcast calls
- Support different communication speeds

  - Standard speed (up to 100 kHz)
  - Fast (up to 400 kHz)
  - Fast + (up to 1MHz)
- Status flags:
  - Transmitter/receiver mode flag
  - Byte transfer complete flag
  - I2C bus busy flag
- Error flags:
  - Arbitration loss in master mode
  - Acknowledge (ACK) fail after address/data transfer
  - Error start or stop condition detected
  - Overrun or underrun when clock extending is disable
- Two interrupt vectors:
  - 1 interrupt for address/data communication success
  - 1 interrupt for an error
- Optional extend clock function
- DMA of single-byte buffers
- Generation or verification of configurable PEC (Packet error checking)
- In transmit mode, the PEC value can be transmitted as the last byte
- PEC error check for the last received byte
- SMBus 2.0 compatible
  - Timeout delay for 25ms clock low
  - 10 ms accumulates low clock extension time of master device
  - 25 ms accumulates low clock extension time of slave device
  - PEC generation/verification of hardware with ACK control
  - Support address resolution protocol (ARP)
  - Compatible with the PMBus

2.15 Universal Synchronous/Asynchronous Transceiver (USART)

The N32G4FR series products integrate up to 7 serial transceiver interfaces, including 3 universal synchronous/ asynchronous transceivers (USART1/USART2/USART3) and 4 universal asynchronous transceivers (UART4/ UART5/UART6/UART7). These 7 interfaces provide asynchronous communication, support for IrDA SIR ENDEC transmission codec, multi-processor communication mode, single-line half-duplex communication mode, and LIN master/slave function.

The communication rate of USART1/UART6/UART7 interface can reach 4.5Mbit/sec, and the communication rate of other interfaces can reach 2.25Mbit/sec.

The USART1, USART2 and USART3 interfaces have hardware CTS and RTS signal management, ISO7816-compatible Smart-card mode, and similar to SPI communication mode, all of which can use DMA operations.

Main features:

- Full duplex, asynchronous communication

- NRZ standard format
- Fractional baud rate generator system, baud rate programmable, used for sending and receiving, up to 4.5 Mbits/s
- Programmable data word length (8 or 9 bits)
- Configurable stop bit, supporting 1 or 2 stop bits
- LIN master's ability to send synchronous interrupters and LIN slave's ability to detect interrupters. When USART hardware is configured as LIN, it generates 13 bit interrupters and detects 10/11 bit interrupters
- Output clock for synchronous transmission
- IRDA SIR encoder decoder, supports 3/16 bit duration in normal mode
- Smart-card simulation function:
  - The smart card interface supports the asynchronous smart card protocol defined in ISO7816-3
  - 0.5 and 1.5 stop bits for smart cards
- Single-wire half duplex communication
- Configurable multi-buffer communication using DMA, receiving/sending bytes in SRAM using centralized DMA buffer
- Independent transmitter and receiver enable bits
- Detection flag
  - Receive buffer is full
  - Send buffer empty
  - Transmission complete
- Parity control
  - Send parity bit
  - Check the received data
- Four error detection flags:
  - Overflow error
  - Noise error
  - Frame error
  - Parity error
- 10 USART interrupt sources with flags
  - CTS change
  - LIN disconnect detection
  - Send data register is empty
  - Send complete
  - Received data register is full
  - Bus was detected to be idle
  - Overflow error
  - Frame error
  - Noise error
  - Parity the error

- Multi-processor communication, if the address does not match, then enter the silent mode
- Wake up from silent mode (via idle bus detection or address flag detection)
- Mode configuration:

USART modes	USART1	USART2	USART3	UART4	UART5	UART6	UART7
Asynchronous mode	Y	Y	Y	Y	Y	Y	Y
Hardware flow control	Y	Y	Y	N	N	N	N
Multiple buffer communication (DMA)	Y	Y	Y	Y	Y	Y	Y
Multiprocessor communication	Y	Y	Y	Y	Y	Y	Y
Synchronous mode	Y	Y	Y	N	N	N	N
Smart-card mode	Y	Y	Y	N	N	N	N
Half duplex (single wire mode)	Y	Y	Y	Y	Y	Y	Y
IrDA	Y	Y	Y	Y	Y	Y	Y
LIN	Y	Y	Y	Y	Y	Y	Y

2.16 Serial Peripheral Interface (SPI)

The device integrates 3 SPI interfaces(reusable as an I2S interface, SPI shares resources with I2S), which allow the chip to communicate with peripheral devices in a half/full duplex, synchronous, serial manner modes. This interface can be configured in master mode and provides a communication clock (SCK) for external slave devices. Interfaces can also work in a multi-master configuration. It can be used for a variety of purposes, including two-line simplex synchronous transmission using a two-way data line, and reliable communication using CRC checks.

Main features:

- 3-wire full-duplex synchronous transmission
- Two-wire simplex synchronous transmission with or without a third bidirectional data line
- 8 or 16-bit transmission frame format selection
- Master or slave operations
- Support multi-master mode
- 8 master mode baud rate prescaler coefficient (Max $f_{PCLK}/2$)
- Slave mode frequency (Max $f_{PCLK}/2$)
- Fast communication between master mode and slave mode
- NSS can be managed by software or hardware in both master and slave modes: dynamic change of master/slave modes
- Programmable clock polarity and phase
- Programmable data order, MSB before or LSB before
- Dedicated send and receive flags that trigger interrupts
- SPI bus busy flag
- Hardware CRC for reliable communication:
  - In send mode, the CRC value can be sent as the last byte
  - In full-duplex mode, CRC is automatically performed on the last byte received
- Master mode failures, overloads, and CRC error flags that trigger interrupts
- Single-byte send and receive buffer with DMA capability: generates send and receive requests
- Maximum speed: 36Mbps for SPI1 interface, and 18Mbps for SPI2/SPI3 interface

2.17 Serial Audio Interface (I2S)

I2S is a 3-pin synchronous serial interface communication protocol. The device integrates 2 standard I2S interfaces (multiplexed with SPI) and can operate in master or slave mode. The 2 interfaces can be configured for 16-bit, 24-bit or 32-bit transmission, or as input or output channels, supporting audio sampling frequencies from 8KHz to 96KHz. It supports four audio standards, including Philips I2S, MSB and LSB alignment, and PCM.

In half duplex communication, it can operatein two modes: master and slave mode. When it acts as a master device, it provides clock signals to external slave devices through an interface.

Main features:

- Simplex communication (send or receive only)
- Master or slave operations
- 8-bit linear programmable prescaler for accurate audio sampling frequencies (8 KHZ to 96KHz)
- The data format can be 16, 24, or 32 bits
- Audio channel fixed packet frame is 16 bit (16-bit data frame) or 32 bit (16, 24 or 32 bit data frame)
- Programmable clock polarity (steady state)
- The overflows flag bit in slave sending mode and the overflows flag bit in master/slave receiving mode
- 16-bit data registers are used for sending and receiving, with one register at each end of the channel
- Supported I2S protocols:
  - I2S Philips standard
  - MSB alignment standard (left aligned)
  - LSB alignment standard (right aligned)
  - PCM standard (16-bit channel frame with long or short frame synchronization or 16-bit data frame extension to 32-bit channel frame)
- The data direction is always MSB first
- Both send and receive have DMA capability
- The master clock can be output to external audio devices at a fixed rate of 256xFs (Fs is the audio sampling frequency)

2.18 Quard Serial Peripheral Interface (QSPI)

The device integrates with 1 channel QSPI in single-master mode, can operates in two modes:

- Memory mapping mode.
- Indirect mode

Main features:

- Can be configured to Single SPI/Dual SPI/Quard SPI mode. In Single mode, it supports standard SPI operation and can work in half-duplex and full-duplex modes
- The operation mode of QSPI can be configured in indirect mode or memory mapping mode. The command code in the instruction stage can be configured, and the alternate byte or mode byte in the alternate byte stage or mode stage can be configured
- Support 8-bit, 16-bit, 32-bit data access mode
- Data transceiver FIFO
- Support DMA operation
- Support FIFO interrupt, operation completion interrupt, timeout interrupt, data access error interrupt

- Maximum speed: 4×36Mbps
- In indirect mode or memory mapping mode, the operation is divided into instruction stage, address stage, alternate byte stage, Dummy stage, and data stage. These stages can be configured to be skipped

2.19 Secure Digital Input Output Interface (SDIO)

Secure Digital Input and Output (SDIO) provides an operation interface between AHB peripheral bus and Multimedia Card (MMC), SD memory card, SDIO card devices.

Main features:

- Support "MultiMediaCard System Specification Version 4.2", support 1-bit (default), 4-bit and 8-bit data bus
- Compatible with earlier MMC protocol
- Support "SD Memory Card Specifications Version 2.0"
- Support "SD I/O Card Specification Version 2.0", support 1-bit (default) and 4-bit data format
- The clock rate of SDIO is up to 48MHz
- SDIO does not support SPI communication

2.20 Controller Area Network (CAN)

The device integrates 2 CAN bus interfaces compatible with 2.0A and 2.0B (active) specifications, with bit rates up to 1Mbps. It can receive and send standard frames with 11-bit identifiers, as well as extended frames with 29-bit identifiers.

Main features:

- Support CAN protocol 2.0A and 2.0B active mode
- Baud rate up to 1Mbps
- Supports time-triggered communication
- Transmit
  - 3 sending mailboxes
  - The priority of transmit packets can be configured by software
  - Records the timestamp of the time when the SOF was sent
- Receive
  - Level 3 depth of 2 receiving FIFO
  - Variable filter group:
  - There are 14 filter groups
  - Identifier list
  - The FIFO overflow processing mode is configurable
  - Record the time stamp of the receipt for the SOF
- Time-triggered communication mode
  - Disable automatic retransmission mode
  - 16-bit free run timer
  - Timestamp can be sent in the last 2 bytes of data
- Management

  - Interrupt masking
  - The mailbox occupies a separate address space to improve software efficiency

2.21 Universal Serial Bus (USB)

The device is embedded with a full speed USB compatible device controller and follows the full speed USB device (12Mbit/s) standard. The endpoint can be configured by software and has suspend/resume functions. The USB specific 48MHz clock is generated directly from the internal main PLL. In order to ensure communication stability, the clock source must be high speed external crystal oscillator (HSE).

Main features:

- Comply with the technical specifications of USB2.0 full-speed equipment
- 1 to 8 USB endpoints can be configured
- CRC (Cyclic Redundancy Check) generation/checking, non-return-to-zero (NRZI) encoding/decoding and bit filling
- Double buffer mechanism for bulk/isochronous endpoints
- Support USB suspend/resume operation
- Frame lock clock pulse generation
- Integrated pull-up 1.5K resistor for USB DP signal line (user can enable or disable through software control), with an accuracy of ±5%

2.22 General Purpose Input/Output Interface (GPIO)

Up to 65 GPIOs, which are divided into 5 groups (GPIOA/GPIOB/GPIOC/GPIOD/GPIOE). Group GPIOA, GPIOB and GPIOC are 16 ports. Group GPIOD is 8 ports. Group GPIOE is 9 ports. Each GPIO pin can be configured by software as an output (push pull or open drain), input (with or without pull-up/pull-down), or alternate peripheral function port. Most GPIO pins are shared with digital or analog alternate peripherals, and some I/O pins are multiplexed with clock pins. All GPIO pins have high current passing capability except ports with analog input capability.

Main features:

- Each bit of the GPIO port can be configured separately by the software into multiple modes:
  - Input floating
  - Input pull up (weak pull up)
  - Input pull down (weak pull down)
  - Analog function
  - Open drain output
  - Push-pull output
  - Push-pull alternate function
  - Open drain alternate function
- General I/O (GPIO)
  - During and just after reset, the alternate function is not enabled, and the I/O ports are in analog function mode, except for BOOT0/BOOT1(which are set to input pull-down mode) and the NRST pin.
  - During and just after reset, the alternate function is not enabled, and the I/O ports are in analog function mode. After reset, the default state of pins associated with the debug system is to enable JTAG, which are set to input pull-up or pull-down mode:

  - JTDI in pull-up mode;
  - JTCK in drop down mode;
  - JTMS in pull-up mode;
  - NJTRST is placed in pull-up mode
  - When configured as output mode, values written to the output data registers are output to the appropriate I/O pins. Can be output in push pull mode or open drain mode
- Separate bit setting or bit clearing functions
- External interrupt/wake up: All ports have external interrupt capability. In order to use external interrupts, ports must be configured in input mode
- Alternate function: port configuration register must be programmed before using default alternate function
- GPIO lock mechanism, which freezes I/O configurations. When a LOCK is performed on a port bit, the configuration of the port bit cannot be changed until the next reset

2.23 Analog/Digital Converter (ADC)

The device support 2x 12-bit Successive Approximation Register (SAR) ADC with sampling rate of 4.7Msps. The ADCs support both single-ended input and differential input, capable of measuring 16 external signal sources and 3 internal signal sources. ADC1 supports 9 external channels, ADC2 supports 12 external channels.

Main features:

- Support 12/10/8/6-bit resolution configurable
  - The maximum sampling rate at 12bit resolution is 4.7MSPS
  - The maximum sampling rate at 10bit resolution is 6.1MSPS
  - The maximum sampling rate at 8bit resolution is 7.3MSPS
  - The maximum sampling rate at 6bit resolution is 8.9MSPS
- ADC clock source is divided into working clock source, sampling clock source and timing clock source
  - AHB_CLK can be configured as the working clock source, up to 144MHz
  - PLL can be configured as a sampling clock source, up to 80MHZ, support 1, 2, 4, 6, 8, 10, 12, 16, 32, 64, 128, 256 frequency division
  - AHB_CLK can be configured as the sampling clock source, up to 80MHz, and supports frequency 1, 2, 4, 6, 8, 10, 12, 16, 32
  - The timing clock is used for internal timing functions and the frequency must be configured to 1MHz
- Supports timer trigger ADC sampling
- Interrupts when conversion ends, injection conversion ends, and analog watchdog events occur
- Single and continuous conversion modes
- Automatic scan mode from channel 0 to channel N
- Support for self-calibration
- Data alignment with embedded data consistency
- Sampling intervals can be programmed separately by channel
- Both regular conversions and injection conversions have external triggering options

- Continuous mode
- Dual ADC mode, combine ADC1 with ADC2
- ADC power supply requirements: 1.8V to 3.6V
- ADC input range: $V_{REF-} \leq V_{IN} \leq V_{REF+}$
- ADC can use DMA operations, and DMA requests are generated during regular channel conversion.
- Analog watchdog function can monitor one, multiple, or all selected channels with great precision. When the monitored signal exceeds the preset threshold, an interruption will occur.

2.24 Digital/Analog Converter (DAC)

The device integrates 2x digital-to-analog converters (DAC), which are 12-bit digital input and voltage output digital/analog convert. The DAC module has 2 output channels, each channel has a separate converter, and the 2 DAC can be used at the same time without affecting each other. The DAC can input the reference voltage (V_{REF+}) through the pin to obtain more accurate conversion results.

Main features:

- 2 DAC converters: each with an output channel
- Configurable 8-bit or 12-bit output
- Configurable left and right data alignment in 12-bit mode
- Update function
- Generate of noise wave
- Generate of triangular wave
- Dual DAC channel, supports independent or synchronous conversion
- DMA support
- External triggers for conversion
- Input voltage V_{REF+}

2.25 Temperature Sensor (TS)

The temperature sensor generates a voltage that varies linearly with temperature in range of $1.8V < V_{DDA} < 3.6V$. The temperature sensor is internally connected to the ADC1_IN16 input channel for converting the output of the temperature sensor to a digital value.

2.26 Digital Video Interface (DVP)

DVP is a flexible and powerful CMOS optical sensor interface, which can easily realize the customer's image acquisition requirements, and the entire acquisition process does not require CPU intervention.

Main features:

- Pure hardware acquisition method
- Support clock output (24MHz@typical) to provide clock for external CMOS chip
- 8 x 32bits FIFO, the FIFO can transfer 4 bytes at a time
- Support DMA, image acquisition process without CPU intervention
- The image size must be a multiple of 4
- Supports the inversion operation on the captured image

2.27 Cyclic Redundancy Check Calculation Unit (CRC)

The device integrates CRC32 and CRC16 functionalities. The cyclic redundancy check (CRC) calculation unit is based on a fixed generation polynomial to obtain arbitrary CRC calculation results. In many applications, CRC-based techniques are used to verify data transfer or storage consistency. Within the scope of the EN/IEC 60335-1 standard, it provides a means of detecting flash memory errors. The CRC unit can be used to calculate signatures of software in real time and compare them with signatures generated during the link-time and generating of the software.

Main features:

- CRC16: supports polynomials $X^{16} + X^{15} + X^{2} + X^{0}$
- CRC32: supports polynomials $X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^{8} + X^{7} + X^{5} + X^{4} + X^{2} + X + 1$
- CRC16 calculation time: 1 AHB clock cycle (HCLK)
- CRC32 calculation time: 1 AHB clock cycle (HCLK)
- The initial value for cyclic redundancy computing is configurable
- Supports DMA mode

2.28 Secure Algorithm Co-processor (SAC)

The device features an embedded secure algorithm co-processor (SAC), it supports a variety of international algorithms and hash cryptographic algorithm acceleration, which can greatly improve the speed of encryption and decryption compared with pure software algorithms.

The hardware supports the following algorithms:

- Support DES symmetric algorithm
  - DES and 3DES encryption and decryption operations are supported
  - TDES supports 2KEY and 3KEY modes
  - Supports CBC and ECB modes
- Supports the SYMMETRIC AES algorithm
  - Supports128bits, 192bits, 256bits key length
  - Support CBC, ECB and CTR modes
- Supports SHA hash algorithm
  - Supports SHA1, SHA224, SHA256
- Supports the MD5 digest algorithm

2.29 Unique Device Serial Number (UID)

The N32G4FR series have two built-in unique device serial numbers of different lengths, which are 96-bit Unique Device ID (UID) and 128-bit Unique Customer ID (UCID). These two device serial numbers are stored in the system configuration block of Flash memory. The information they contain is written at the time of delivery and is guaranteed to be unique to any of the N32G4FR series microcontrollers under any circumstances and can be read by user applications or external devices through the CPU or JTAG/SWD interface and cannot be modified.

The 96-bit UID is usually used as a serial number or password. When writing Flash memory, this unique identifier is combined with software encryption and decryption algorithm to further improve the security of code in Flash memory.

The UCID is 128-bit, which complies with the definition of national technology chip serial number. It contains the information related to chip production and version.

2.30 Serial Single-Wire JTAG Debug Port (SWJ-DP)

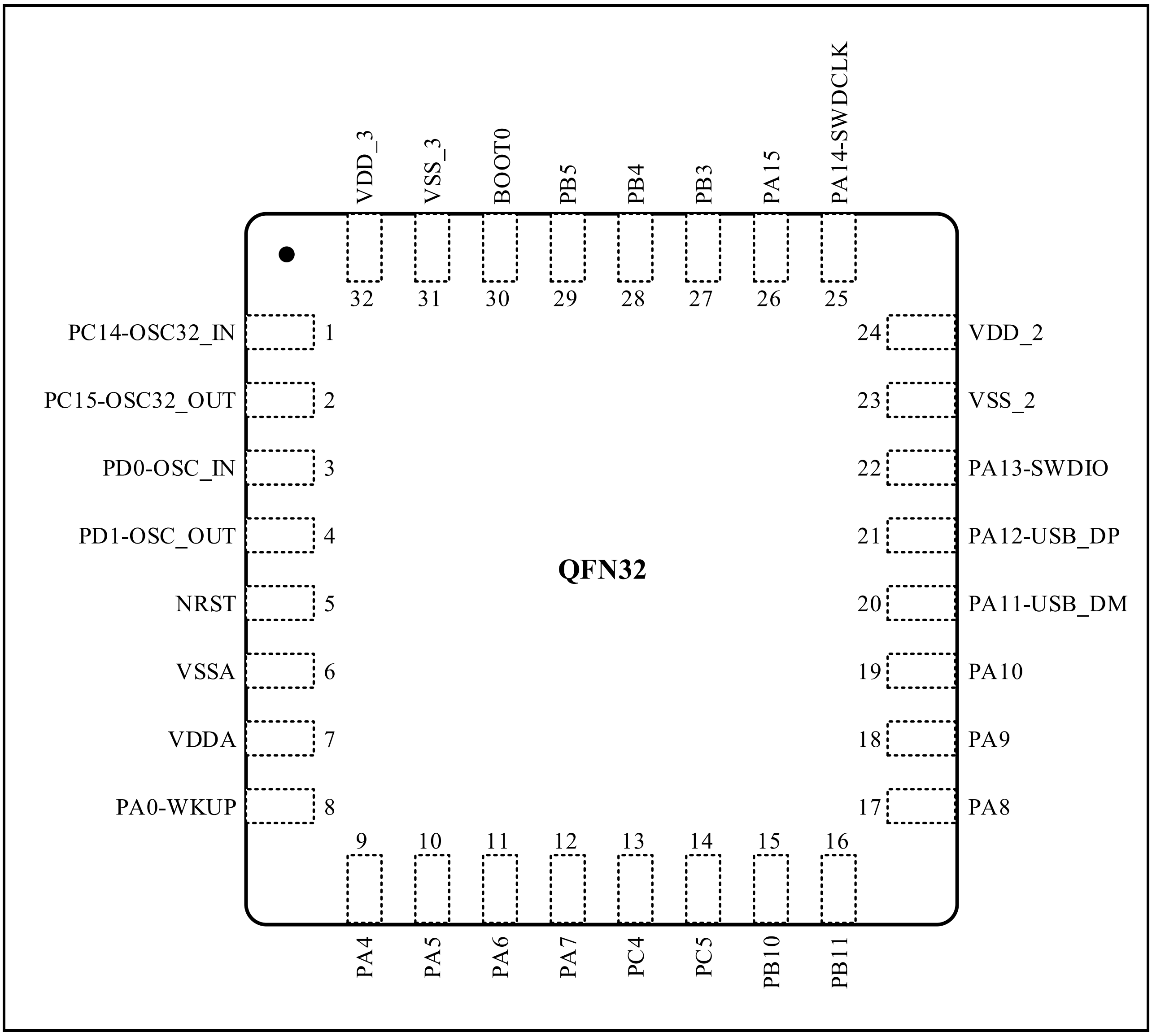
The device has an embedded ARM SWJ-DP interface, which is a combination of JTAG and serial single-line debugging interface, can achieve serial single-line debugging interface or JTAG interface connection. The JTMS and JTCK signals of JTAG share pins with SWDIO and SWCLK respectively, and a special signal sequence on the JTMS pin is used to switch between JTAG-DP and SW-DP.

3 Pinouts and Pin Description

3.1 Pinouts

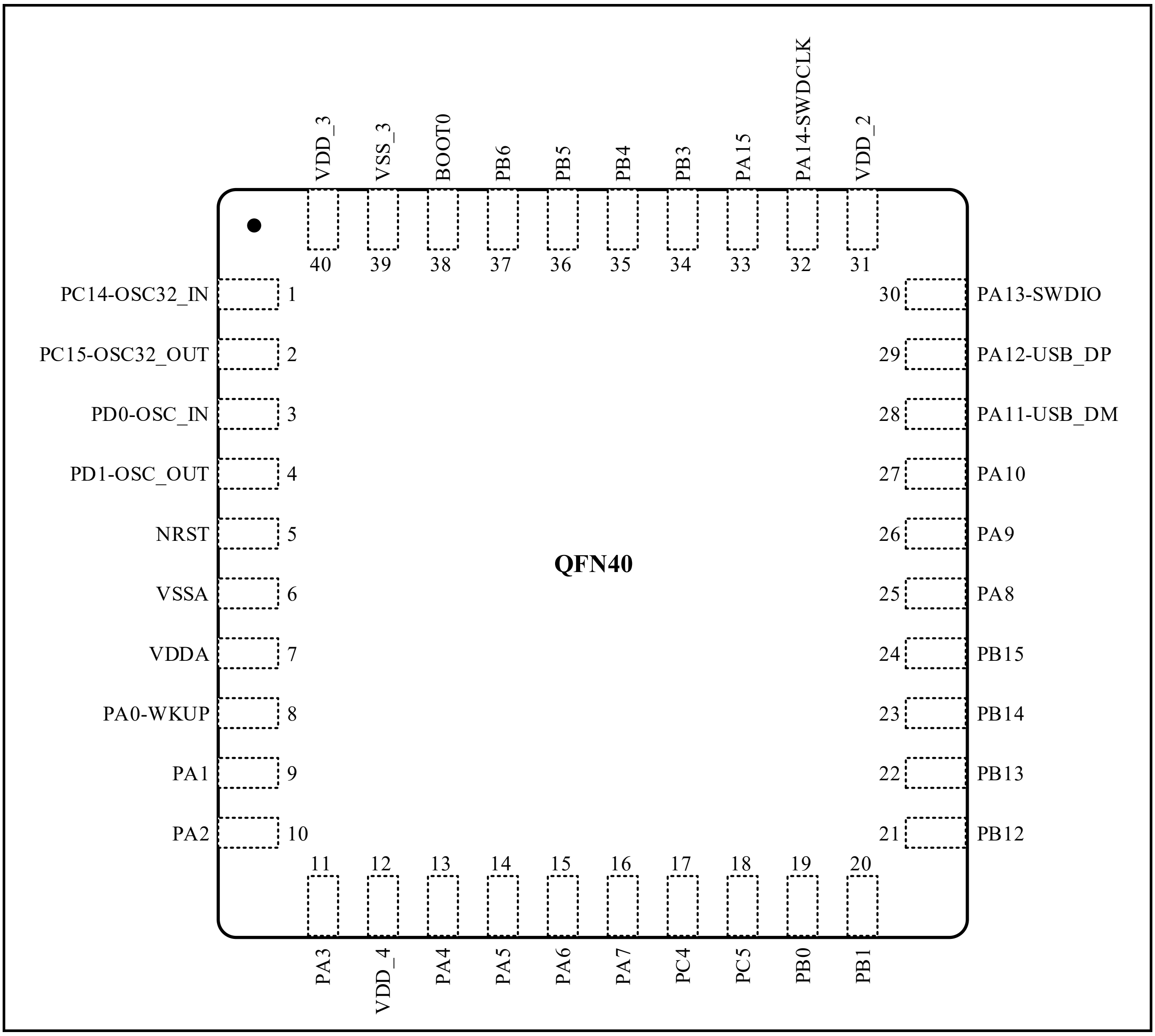
3.1.1 QFN32

Figure 3-1 N32G4FR Series QFN32 Pinout



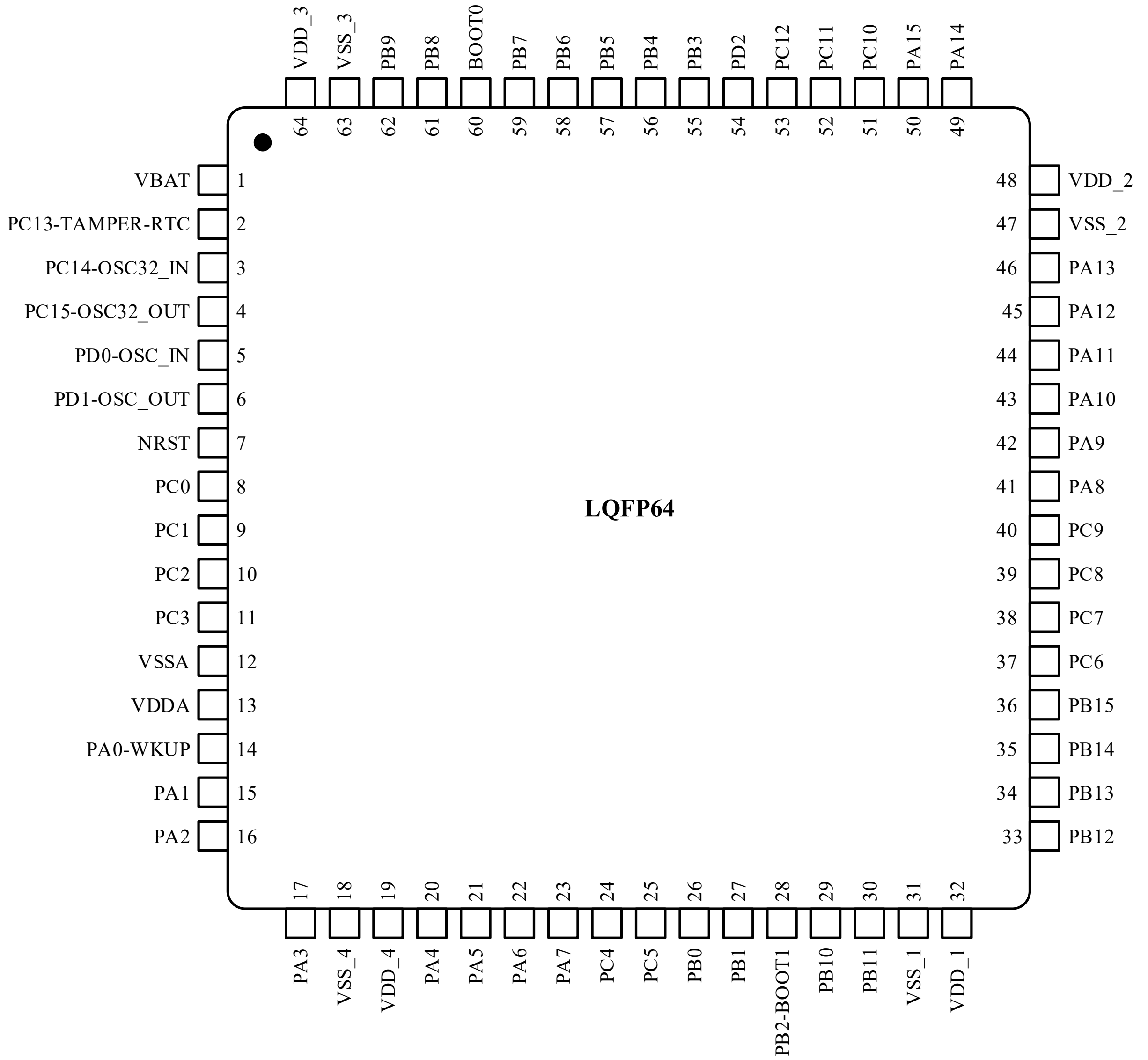
3.1.2 QFN40

Figure 3-2 N32G4FR Series QFN40 Pinout



3.1.3 LQFP64

Figure 3-3 N32G4FR Series LQFP64 Pinout



3.1.4 LQFP80

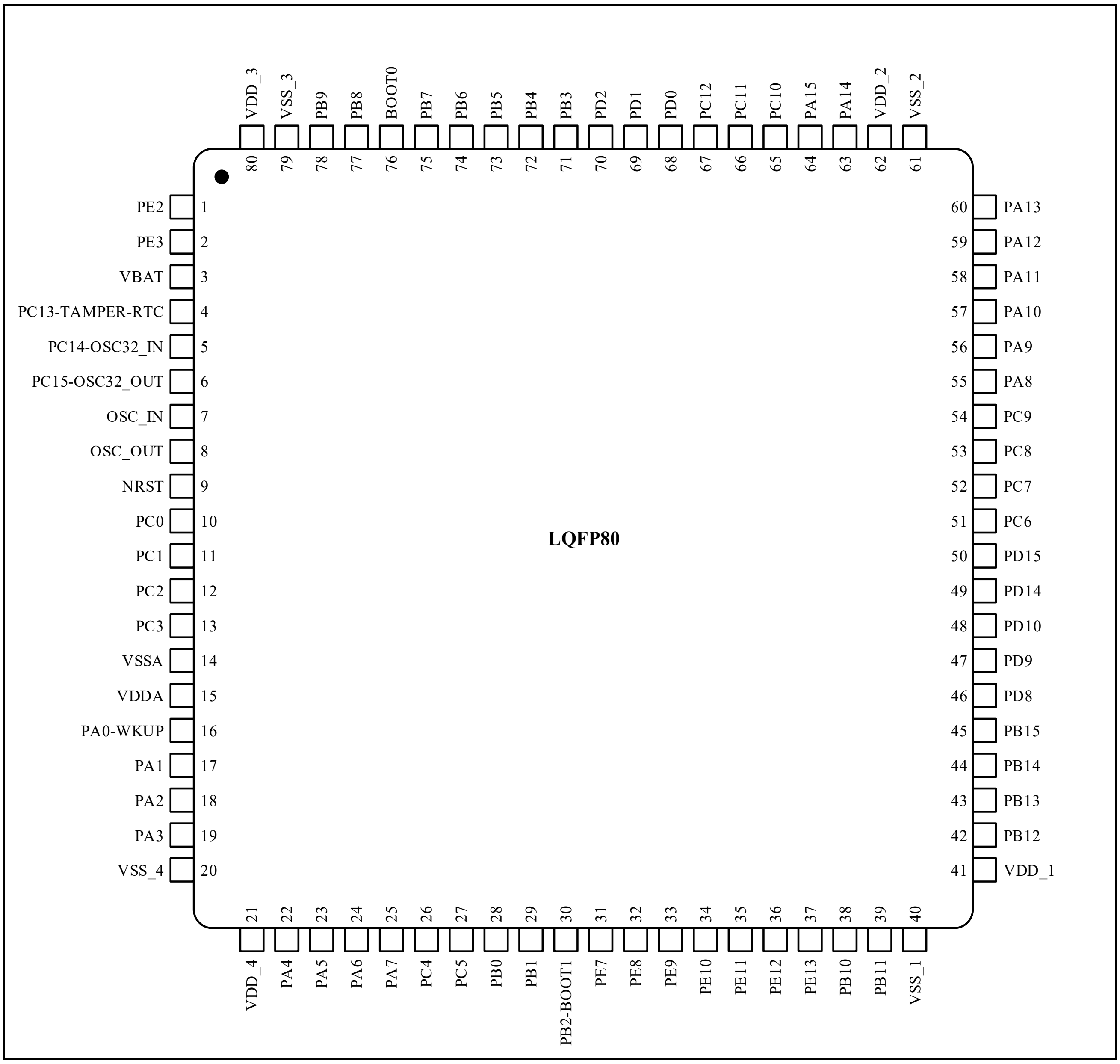


Figure 3-4 N32G4FR Series LQFP80 Pinout

3.2 Pin Description

Table 3-1 Pin Description

Package				Pin Name	Type(1)	I/O(2) structure	Fail-safe(8) support	Main Functions(3) (after reset)	Optional Multiplexing Function(6)	
QFN32	QFN40	LQFP64	LQFP80						Default	Redefine
-	-	-	1	PE2	I/O	FT	Yes	PE2	UART6_TX	DVP_HSYNC
-	-	-	2	PE3	I/O	FT	Yes	PE3	UART6_RX	DVP_VSYNC
-	-	1	3	VBAT	S	-	-	VBAT	-	-
-	-	2	4	PC13-TAMPER- RTC(4)	I/O	TC	Yes	PC13(5)	TAMPER-RTC	-
1	1	3	5	PC14- OSC32_IN(4)	I/O	TC	Yes	PC14(5)	OSC32_IN	-
2	2	4	6	PC15- OSC32_OUT(4)	I/O	TC	Yes	PC15(5)	OSC32_OUT	-
3	3	5	7	OSC_IN(7)	I	TC	Yes	OSC_IN	-	-
4	4	6	8	OSC_OUT(7)	O	TC	No	OSC_OUT	-	-
5	5	7	9	NRST	I/O	-	-	NRST	-	-
-	-	8	10	PC0	I/O	TTa	No	PC0	ADC12_IN6(10) I2C3_SCL	DVP_D2 UART6_TX
-	-	9	11	PC1	I/O	TTa	No	PC1	ADC12_IN7(10) I2C3_SDA	UART6_RX
-	-	10	12	PC2	I/O	TTa	No	PC2	ADC12_IN8(10)	UART7_TX SPI3_NSS I2S3_WS
-	-	11	13	PC3	I/O	TTa	No	PC3	ADC12_IN9(10)	UART7_RX SPI3_SCK I2S3_CK
6	6	12	14	VSSA	S	-	-	VSSA	-	-
7	7	13	15	VDDA	S	-	-	VDDA	-	-
8	8	14	16	PA0-WKUP	I/O	TTa	No	PA0	WKUP USART2_CTS ADC1_IN1(9) TIM2_CH1_ETR TIM5_CH1 TIM8_ETR	SPI3_MISO
-	9	15	17	PA1	I/O	TTa	No	PA1	USART2_RTS ADC1_IN2(9) TIM5_CH2 TIM2_CH2 DVP_HSYNC	SPI3_MOSI I2S3_SD
-	10	16	18	PA2	I/O	TTa	No	PA2	USART2_TX TIM5_CH3 ADC12_IN11(10) TIM2_CH3 DVP_VSYNC	-
-	11	17	19	PA3	I/O	TTa	No	PA3	USART2_RX TIM5_CH4 ADC1_IN4(9) TIM2_CH4 DVP_PCLK	-

Package				Pin Name	Type(1)	I/O(2) structure	Fail-safe(8) support	Main Functions(3) (after reset)	Optional Multiplexing Function(6)	
QFN32	QFN40	LQFP64	LQFP80						Default	Redefine
-	-	18	20	VSS_4	S	-	-	VSS_4	-	-
-	12	19	21	VDD_4	S	-	-	VDD_4	-	-
9	13	20	22	PA4	I/O	TTa	No	PA4	SPI1_NSS USART2_CK DAC_OUT1 ADC2_IN1(9) DVP_D0 QSPI_NSS	I2C2_SCL
10	14	21	23	PA5	I/O	TTa	No	PA5	SPI1_SCK DAC_OUT2 ADC2_IN2(9) DVP_D1 QSPI_SCK	I2C2_SDA
11	15	22	24	PA6	I/O	TTa	No	PA6	SPI1_MISO TIM8_BKIN ADC1_IN3(9) TIM3_CH1 DVP_D2 QSPI_IO0	TIM1_BKIN
12	16	23	25	PA7	I/O	TTa	No	PA7	SPI1_MOSI TIM8_CH1N ADC2_IN4(9) TIM3_CH2 DVP_D3 QSPI_IO1	TIM1_CH1N
13	17	24	26	PC4	I/O	TTa	No	PC4	ADC2_IN5(9) DVP_D4 QSPI_IO2 UART7_TX	I2C3_SCL
14	18	25	27	PC5	I/O	TTa	No	PC5	ADC2_IN12(10) DVP_D5 QSPI_IO3 UART7_RX	I2C3_SDA
-	19	26	28	PB0	I/O	TC	No	PB0	TIM3_CH3 TIM8_CH2N DVP_D6	TIM1_CH2N UART6_TX
-	20	27	29	PB1	I/O	TTa	No	PB1	ADC2_IN3(9) TIM3_CH4 TIM8_CH3N DVP_D7	TIM1_CH3N UART6_RX
-	-	28	30	PB2	I/O	TTa	No	PB2/BOOT1	ADC2_IN13(10)	DVP_D3 UART4_TX SPI1_NSS
-	-	-	31	PE7	I/O	TC	No	PE7	-	TIM1_ETR UART4_RX SPI1_SCK
-	-	-	32	PE8	I/O	TC	No	PE8	-	TIM1_CH1N UART5_TX SDIO_DAT0 SPI1_MISO
-	-	-	33	PE9	I/O	TC	No	PE9	-	TIM1_CH1 UART5_RX SDIO_DAT1 SPI1_MOSI

Package				Pin Name	Type(1)	I/O(2) structure	Fail-safe(8) support	Main Functions(3) (after reset)	Optional Multiplexing Function(6)	
QFN32	QFN40	LQFP64	LQFP80						Default	Redefine
-	-	-	34	PE10	I/O	TC	No	PE10	-	TIM1_CH2N SDIO_ DAT2 SPI2_NSS I2S2_WS
-	-	-	35	PE11	I/O	TC	No	PE11	-	TIM1_CH2 SDIO_ DAT3 SPI2_SCK I2S2_CK
-	-	-	36	PE12	I/O	TC	No	PE12	-	TIM1_CH3N SDIO_CLK SPI2_MISO
-	-	-	37	PE13	I/O	TC	No	PE13	-	TIM1_CH3 SPI2_MOSI I2S2_SD SDIO_CMD
15	-	29	38	PB10	I/O	TC	No	PB10	I2C2_SCL USART3_TX	TIM2_CH3 DVP_D4
16	-	30	39	PB11	I/O	TC	No	PB11	I2C2_SDA USART3_RX	TIM2_CH4 DVP_D5
-	-	31	40	VSS_1	S	-	-	VSS_1	-	-
-	-	32	41	VDD_1	S	-	-	VDD_1	-	-
-	21	33	42	PB12	I/O	TC	No	PB12	SPI2_NSS I2S2_WS I2C2_SMBA USART3_CK TIM1_BKIN CAN2_RX	-
-	22	34	43	PB13	I/O	TC	No	PB13	SPI2_SCK I2S2_CK USART3_CTS TIM1_CH1N CAN2_TX	UART5_TX
-	23	35	44	PB14	I/O	TC	No	PB14	SPI2_MISO TIM1_CH2N USART3_RTS	UART5_RX
-	24	36	45	PB15	I/O	TC	No	PB15	SPI2_MOSI I2S2_SD TIM1_CH3N	-
-	-	-	46	PD8	I/O	TC	No	PD8	-	USART3_TX SPI3_NSS I2S3_WS CAN1_RX
-	-	-	47	PD9	I/O	TC	No	PD9	-	USART3_RX SPI3_SCK I2S3_CK CAN1_TX
-	-	-	48	PD10	I/O	TC	No	PD10	-	USART3_CK CAN2_RX
-	-	-	49	PD14	I/O	TC	No	PD14	-	TIM4_CH3 I2C4_SCL TIM8_CH1
-	-	-	50	PD15	I/O	FT	Yes	PD15	-	TIM4_CH4 I2C4_SDA TIM8_CH2
-	-	37	51	PC6	I/O	TC	Yes	PC6	I2S2_MCK TIM8_CH1 SDIO_ DAT6 I2C4_SCL	TIM3_CH1 SPI2_NSS I2S2_WS USART2_CTS

Package				Pin Name	Type(1)	I/O(2) structure	Fail-safe(8) support	Main Functions(3) (after reset)	Optional Multiplexing Function(6)	
QFN32	QFN40	LQFP64	LQFP80						Default	Redefine
-	-	38	52	PC7	I/O	TC	Yes	PC7	I2S3_MCK TIM8_CH2 SDIO_ DAT7 I2C4_SDA	TIM3_CH2 SPI2_SCK I2S2_CK USART2_RTS
-	-	39	53	PC8	I/O	TC	Yes	PC8	TIM8_CH3 SDIO_ DAT0	TIM3_CH3 SPI2_MISO USART2_TX
-	-	40	54	PC9	I/O	TC	Yes	PC9	TIM8_CH4 SDIO_ DAT1	TIM3_CH4 SPI2_MOSI I2S2_SD USART2_RX
17	25	41	55	PA8	I/O	FT	Yes	PA8	USART1_CK TIM1_CH1 MCO	-
18	26	42	56	PA9	I/O	FT	Yes	PA9	USART1_TX TIM1_CH2	I2C4_SCL
19	27	43	57	PA10	I/O	FT	Yes	PA10	USART1_RX TIM1_CH3	I2C4_SDA
20	28	44	58	PA11	I/O	FT	Yes	PA11	USART1_CTS USBDM CAN1_RX TIM1_CH4	-
21	29	45	59	PA12	I/O	FT	Yes	PA12	USART1_RTS USBDP CAN1_TX TIM1_ETR	-
22	30	46	60	PA13	I/O	FT	Yes	JTMS- SWDIO	-	PA13 UART4_TX
23	-	47	61	VSS_2	S	-	-	VSS_2	-	-
24	31	48	62	VDD_2	S	-	-	VDD_2	-	-
25	32	49	63	PA14	I/O	FT	Yes	JTCK- SWCLK	-	PA14 UART4_RX
26	33	50	64	PA15	I/O	FT	Yes	JTDI	SPI3_NSS I2S3_WS	TIM2_CH1_ETR PA15 SPI1_NSS USART2_CTS TIM8_CH1N
-	-	51	65	PC10	I/O	TC	Yes	PC10	UART4_TX SDIO_ DAT2	USART3_TX SPI3_SCK I2S3_CK QSPI_NSS
-	-	52	66	PC11	I/O	TC	Yes	PC11	UART4_RX SDIO_ DAT3	USART3_RX SPI3_MISO QSPI_SCK
-	-	53	67	PC12	I/O	TC	Yes	PC12	UART5_TX SDIO_CLK	USART3_CK SPI3_MOSI I2S3_SD QSPI_IO0 TIM8_CH2N
-	-	-	68	PD0	I/O	FT	Yes	PD0	-	CAN1_RX UART4_TX QSPI_IO1
-	-	-	69	PD1	I/O	FT	Yes	PD1(7)	-	CAN1_TX UART4_RX QSPI_IO2
-	-	54	70	PD2	I/O	TC	Yes	PD2(7)	TIM3_ETR UART5_RX	SPI3_NSS I2S3_WS

Package				Pin Name	Type[1]	I/O[2] structure	Fail-safe[8] support	Main Functions[3] (after reset)	Optional Multiplexing Function[6]	
QFN32	QFN40	LQFP64	LQFP80						Default	Redefine
									SDIO_CMD	QSPI_IO3 TIM8_CH3N
27	34	55	71	PB3	I/O	FT	Yes	JTDO	SPI3_SCK I2S3_CK	PB3 TRACESWO TIM2_CH2 SPI1_SCK USART2_RTS TIM8_BKIN
28	35	56	72	PB4	I/O	FT	Yes	NJTRST	SPI3_MISO	PB4 TIM3_CH1 SPI1_MISO USART2_TX TIM8_ETR
29	36	57	73	PB5	I/O	FT	Yes	PB5	I2C1_SMBA SPI3_MOSI I2S3_SD	TIM3_CH2 SPI1_MOSI CAN2_RX USART2_RX TIM1_BKIN
-	37	58	74	PB6	I/O	TC	Yes	PB6	I2C1_SCL TIM4_CH1	USART1_TX CAN2_TX
-	-	59	75	PB7	I/O	TC	Yes	PB7	I2C1_SDA TIM4_CH2	USART1_RX
30	38	60	76	BOOT0	I	-	-	BOOT0	-	-
-	-	61	77	PB8	I/O	TC	Yes	PB8	TIM4_CH3 SDIO_ DAT4	I2C1_SCL CAN1_RX UART5_TX
-	-	62	78	PB9	I/O	TC	Yes	PB9	TIM4_CH4 SDIO_ DAT5	I2C1_SDA CAN1_TX UART5_RX
31	39	63	79	VSS_3	S	-	-	VSS_3	-	-
32	40	64	80	VDD_3	S	-	-	VDD_3	-	-

Notes:

1. *I = input, O = output, S = power supply, HiZ = high impedance.*
2. *FT: tolerate 5V; TTa: tolerates 3.3V and supports analog peripherals; TC: ordinary 3.3V I/O*
3. *Some functions are only supported in some models of chips.*
4. *Pin PC13, PC14 and PC15 are powered by the power switch, which can only absorb limited current (3mA). Therefore, when these three pins are used as output pins, they have the following limitations: they can only work in 2MHz mode, the maximum driving load is 30pF, and the total output current of the three pins at the same time cannot exceed 3mA.*
5. *When the backup area is powered on for the first time, these pins are in the main function state. After that, even if they are reset, the state of these pins is controlled by the backup area registers (these registers will not be reset by the main reset system). For specific information on how to control these IO ports, please refer to the battery backup area of N32G4FR series user's reference manual and relevant chapters of BKP register.*
6. *Some multiplexing functions can be configured to other pins by software (if the corresponding package model has this pin). For details, please refer to the multiplexing function I/O chapter and debugging setting chapter of N32G4FR series user reference manual.*

7. *Pin 5 and pin 6 of QFN32, QFN40, LQFP64 package are configured as OSC_IN and OSC_OUT function pins by default after the chip is reset. Software can reset these two pins to PD0 and PD1 functions. When used as PD0 and PD1, these two pins can only be used as ordinary IO functions. However, for LQFP80 package, because PD0 and PD1 are inherent functional pins, there is no need to remap by software. For more details, please refer to the reuse function I/O chapter and debugging settings chapter of N32G4FR user reference manual.*
8. *Fail-safe means that when the chip has no power input, the input high level is added to IO, and there is no phenomenon that the input high level is poured into the chip, which leads to a certain voltage on the power supply and consumes current.*
9. *Corresponding ADC channels are fast channels, supporting the maximum sampling rate 5.14MSPS(12bit).*
10. *Corresponding ADC channels are slow channels, supporting the maximum sampling rate 4.23MSPS(12bit).*

Note: ADC12_INx appears in the pin name label in the Table, indicating that this pin can be ADC1_INx or ADC2_INx. For example, ADC12_IN9 indicates that this pin can be configured as ADC1_IN9 or ADC2_IN9.

TIM2_CH1_ETR in the multiplexing function corresponding to pin PA0 in the Table indicates that the function can be configured as TIM2_TI1 or TIM2_ETR. Similarly, the name of the remapping multiplexing function corresponding to PA15, TIM2_CH1_ETR, has the same meaning.

For the port of FT in the Table, it is necessary to ensure that the difference between IO voltage and power supply voltage is less than 3.6V

4 Electrical Characteristics

4.1 Parameter Conditions

All voltages are based on V_{SS} unless otherwise specified.

4.1.1 Minimum and Maximum Values

Unless otherwise specified, all minimums and maximums will be guaranteed under the worst ambient temperature, supply voltage and clock frequency conditions by performing tests on 100% of the product on the production line at ambient temperatures T_A=25°C.

Note at the bottom of each form that data obtained through comprehensive evaluation, design simulation and/or process characteristics will not be tested on the production; Base on comprehensive evaluation, the minimum and maximum values are obtained by taking the average of the samples tested and adding or subtracting three times the standard distribution (mean ±3∑).

4.1.2 Typical Values

Unless otherwise specified, typical data are based on T_A= 25 C and V_{DD}=3.3V. These data is untested and used only as a design guide for the user.

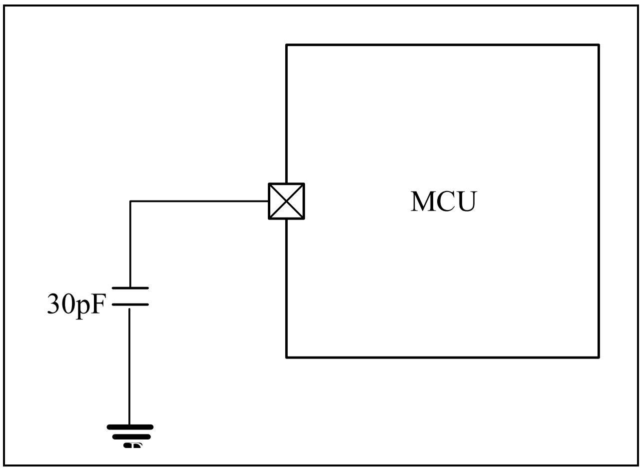
4.1.3 Typical Curve

Unless otherwise specified, these typical data are based on T_A = 25°C and V_{DD} = 3.3V. These data are for design guidance only and not tested.

4.1.4 Loading Capacitors

The load conditions for measuring pin parameters are shown in Figure 4-1.

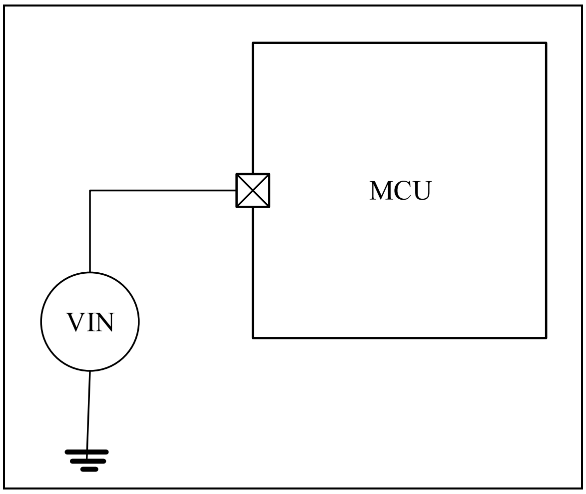
Figure 4-1 Load Conditions of Pins



4.1.5 Pin Input Voltage

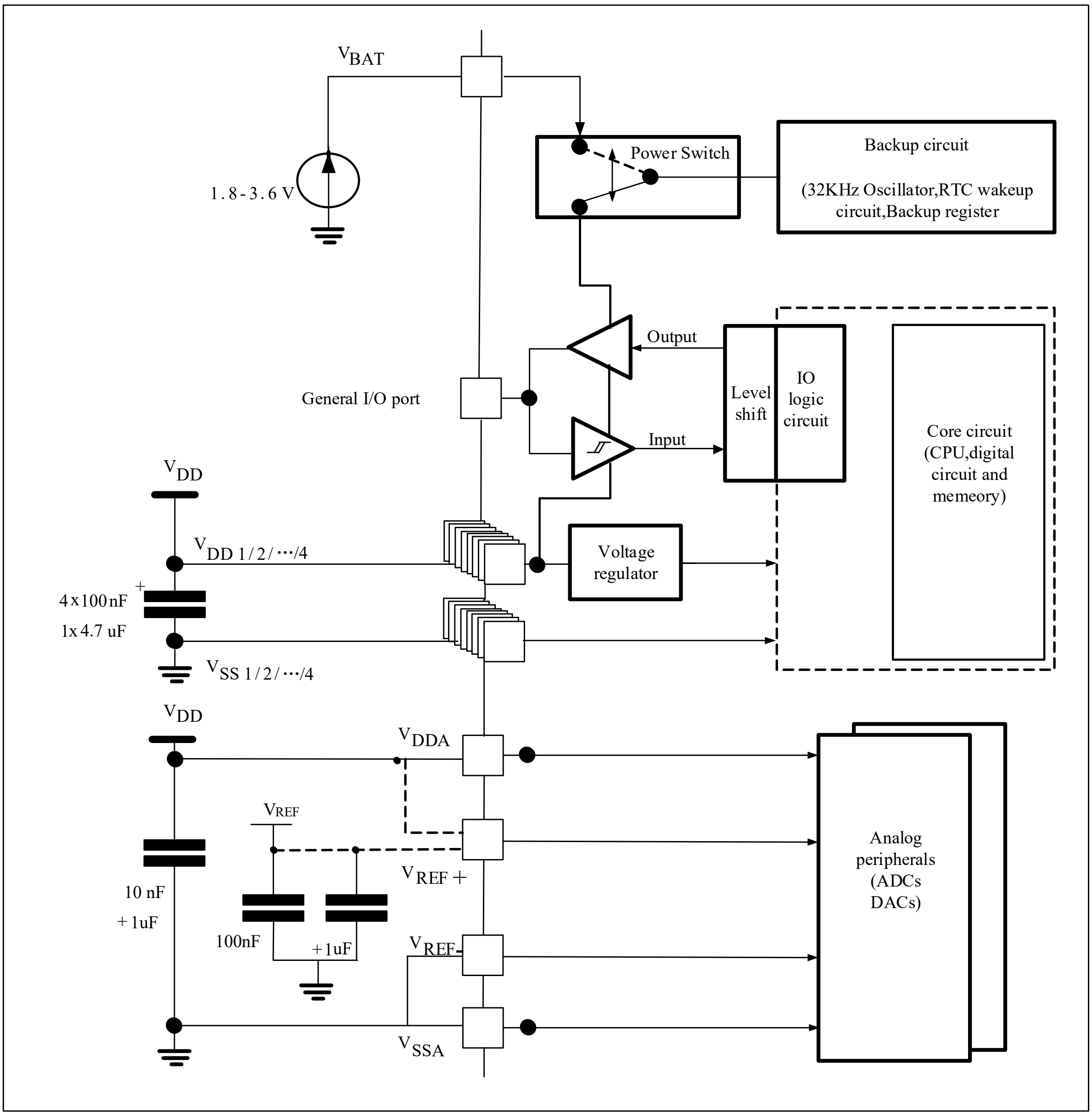
The measurement of the input voltage on pin is shown in Figure 4-2.

Figure 4-2 Pin Input Voltage



4.1.6 Power Supply Scheme

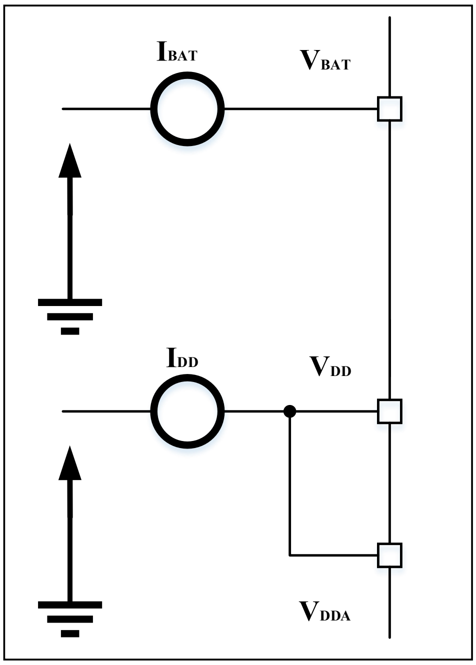
Figure 4-3 Power Supply Scheme



Note: The 4.7μF capacitor in the above figure must be connected to V_{DD3}.

4.1.7 Current Consumption Measurement

Figure 4-4 Current Consumption Measurement Scheme



4.2 Absolute Maximum Rating

The load applied to the device may permanently damage the device if it exceeds the values given in the Absolute maximum rating list (Table 4-1、Table 4-2、Table 4-3). The maximum load that can be sustained is only given here, and it does not mean that the functional operation of the device under such conditions is correct. The reliability of the device will be affected when the device works for a long time under the maximum condition.

Table 4-1 Voltage Characteristics

Symbol	Describe	Min	Max	Unit
V_{DD}- V_{SS}	Main power supply voltage (including V_{DDA} and V_{DD})[1]	-0.3	4.0	V
V_{IN}	Input voltage on 5V tolerant pin[3]	V_{SS}-0.3	5.5	
	Input voltage on other pins[2]	V_{SS}-0.3	V_{DD} + 0.3	
$\|\Delta V_{DDx}\|$	Voltage difference between different supply pins	-	50	mV
$\|V_{SSx}- V_{SS}\|$	Voltage difference between different grounding pins	-	50	
$V_{ESD(HBM)}$	Electrostatic discharge voltage (Human body mode)	See paragraph 4.3.11 festival		

Note:

[1] All power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply system within permissible limits.

[2] V_{IN} shall not exceed its maximum value. Refer to Table 4-2 for current characteristics.

[3] When 5.5V is applied to the 5V tolerant pin, V_{DD} cannot be less than 2.25V.

Table 4-2 Current Characteristics

Symbol	Describe	Max[1]	Unit
I_{VDD}	Total current (supply current) through V_{DD}/V_{DDA} power line[1][4]	100	**mA**
I_{VSS}	Total current (outflow current) through V_{SS} ground wire	100	
I_I	Output sink current on any I/O and control pins	12	
	Output current on any I/O and control pins	-12	
$I_{INJ(PIN)}$[2][3]	Injection current of NRST pin	-5/0	
	Injection current of other pins[4]	+/-5	

Notes:

(1) All the power supply (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA})pins of must always be connected to the power supply system within the external allowable range.

(2) When V_{IN}>V_{DD}, there is a forward injection current; when V_{IN}<V_{SS}, there is a reverse injection current. $I_{INJ(PIN)}$ should not exceed its maximum value. Refer to Table 4-1 for voltage characteristics.

(3) Reverse injection current can interfere with the analog performance of the device. See section 4.3.22.

(4) When the maximum current occurs, the maximum allowable voltage drop of V_{DD} is 0.1V_{DD}.

Table 4-3 Temperature Characteristics

Symbol	Describe	Value	Unit
T_{STG}	Storage temperature range	-40 ~ +125	℃
T_J	Maximum junction temperature	125	℃

4.3 Operating Conditions

4.3.1 General Operating Conditions

Table 4-4 General Operating Conditions

Symbol	Parameter	Condition	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency	-	0	144	MHz
f_{PCLK1}	Internal APB1 clock frequency	-	0	36	
f_{PCLK2}	Internal APB2 clock frequency	-	0	72	
V_{DD}	Standard operating voltage	-	1.8	3.6	V
V_{DDA}	Analog operating voltage	Must be the same as V_{DD}(1)	1.8	3.6	V
V_{BAT}	Backup partial operating voltage	-	1.8	3.6	V
T_A	Ambient temperature (temperature number 7)	7 suffix version	-40	105	℃
T_J	Junction temperature range	7 suffix version	-40	125	℃

Note: (1) It is recommended that the same power supply be used to power the V_{DD} and V_{DDA}. During power-on and normal operation, a maximum of 300mV difference is allowed between the V_{DD} and V_{DDA}.

4.3.2 Operating Conditions at Power-on and Power-off

The parameters given in the following table are based on the ambient temperatures listed in Table 4-4.

Table 4-5 Operating Conditions at Power-on and Power-off

Symbol	Parameter	Condition	Min	Max	Unit
t_{VDD}	V_{DD} rising rate	Supply voltage goes from 0 to V_{DD}	20	∞	µs/V
	V_{DD} falling rate	Supply voltage drops from V_{DD} to 0	80	∞	

4.3.3 Embedded Reset and Power Control Module Features

The parameters given in the following table are based on the ambient temperature and V_{DD} supply voltage listed in Table 4-4.

Table 4-6 Features of Embedded Reset and Power Control Modules

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{PVD}	Level selection of programmable voltage detector (MSB of PWR_CTRL is 0)	PRS[2:0]=000 (rising edge)	2.09	2.18	2.27	V
		PRS[2:0]=000 (falling edge)	2	2.08	2.16	V
		PRS[2:0]=001 (rising edge)	2.19	2.28	2.37	V
		PRS[2:0]=001 (falling edge)	2.09	2.18	2.27	V
		PRS[2:0]=010 (rising edge)	2.28	2.38	2.48	V
		PRS[2:0]=010 (falling edge)	2.19	2.28	2.37	V
		PRS[2:0]=011 (rising edge)	2.38	2.48	2.58	V
		PRS[2:0]=011 (falling edge)	2.28	2.38	2.48	V
		PRS[2:0]=100 (rising edge)	2.47	2.58	2.69	V
		PRS[2:0]=100 (falling edge)	2.37	2.48	2.59	V
		PRS[2:0]=101 (rising edge)	2.57	2.68	2.79	V
		PRS[2:0]=101 (falling edge)	2.47	2.58	2.69	V
		PRS[2:0]=110 (rising edge)	2.66	2.78	2.9	V
		PRS[2:0]=110 (falling edge)	2.56	2.68	2.8	V
		PRS[2:0]=111 (rising edge)	2.76	2.88	3	V
		PRS[2:0]=111 (falling edge)	2.66	2.78	2.9	V
	Level selection of programmable voltage detector (MSB of PWR_CTRL is 1)	PRS[2:0]=000 (rising edge)	1.7	1.78	1.85	V
		PRS[2:0]=000 (falling edge)	1.61	1.68	1.75	V
		PRS[2:0]=001 (rising edge)	1.8	1.88	1.96	V
		PRS[2:0]=001 (falling edge)	1.7	1.78	1.85	V
		PRS[2:0]=010 (rising edge)	1.9	1.98	2.06	V
		PRS[2:0]=010 (falling edge)	1.8	1.88	1.96	V
		PRS[2:0]=011 (rising edge)	2	2.08	2.16	V
		PRS[2:0]=011 (falling edge)	1.9	1.98	2.06	V
		PRS[2:0]=100 (rising edge)	3.15	3.28	3.41	V
		PRS[2:0]=100 (falling edge)	3.05	3.18	3.31	V
		PRS[2:0]=101 (rising edge)	3.24	3.38	3.52	V
		PRS[2:0]=101 (falling edge)	3.15	3.28	3.41	V
		PRS[2:0]=110 (rising edge)	3.34	3.48	3.62	V
		PRS[2:0]=110 (falling edge)	3.24	3.38	3.52	V
		PRS[2:0]=111 (rising edge)	3.44	3.58	3.72	V
		PRS[2:0]=111 (falling edge)	3.34	3.48	3.62	V
$V_{PVD\ hyst}$(1)	PVD hysteresis	-	-	100	-	mV
V_{POR}	VDD power-on/power-off reset threshold	-	-	1.64/1.62	-	V
$T_{RSTTEMPO}$(1)	Reset duration	-	-	0.8	4	ms

Note: (1) Guaranteed by design, not tested in production.

4.3.4 Internal Reference Voltage

The parameters given in the following table are based on the ambient temperature and VDD supply voltage listed in Table 4-4.

Table 4-7 Internal Reference Voltage

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{REFINT}	Built-in reference voltage	-40°C< T_A< +105°C	1.164	1.20	1.236	V
$T_{S\_vrefint}$(1)	The sampling time of ADC when reading out internal reference voltage	-	-	5.1	10(2)	µs

Notes:

[1] The shortest sampling time is obtained through multiple cycles in the application.

[2] Guaranteed by design, not tested in production.

4.3.5 Power Supply Current Characteristics

The current consumption is a combination of several parameters and factors, including operating voltage, ambient temperature, load of I/O pins, software configuration of the product, operating frequency, toggle rate of I/O pin, program location in memory, and code executed.

The measurement method of current consumption is described in Figure 4-4.

All of the current consumption measurements given in this section are while executing a reduced set of code.

4.3.5.1 Maximum current consumption

The device is under the following conditions:

- All I/O pins are in input mode and are connected to a static level -- V_{DD} or V_{SS} (no load).
- All peripherals are disabled except otherwise noted.
- The access time of the Flash memory is adjusted to the fastest operating frequency (0 waiting periods from 0 to 32MHz, 1 waiting period from 32 to 64MHz, 2 waiting periods from 64MHz to 96MHz, 3 waiting periods from 96MHz to 128MHz, 4 waiting periods from 128MHz to 144MHz).
- Instruction prefetch is enabled (note: this parameter must be set before setting the clock and bus divider).
- When the peripheral is enable: $f_{PCLK1} = f_{HCLK}/4$, $f_{PCLK2} = f_{HCLK}/2$.
- V_{DD}=3.63V, ambient temperature is 105°C.

The parameters given in Table 4-8 and Table 4-9 are based on the test at ambient temperature and V_{DD} supply voltage listed in Table 4-4.

Table 4-8 Maximum Current Consumption in Operating Mode Running From Embedded Flash

Symbol	Parameter	Condition	f_{HCLK}	Typ [1]	Unit
				T_A = 105°C	
I_{DD}	Supply current in operation mode	External clock[2], enable all peripherals	144MHz	29	mA
			72MHz	17	
			36MHz	11	
		External clock[2], disable all peripherals.	144MHz	15.8	
			72MHz	9.7	
			36MHz	6.7	

Note:

[1] Based on comprehensive evaluation result, not tested in production.

[2] Enable PLL when f_{HCLK}>8MHz.

Table 4-9 Maximum Current Consumption in SLEEP Mode

Symbol	Parameter	Condition	f_{HCLK}	Typ [1]	Unit
				T_A = 105 °C	
I_{DD}	Supply current in sleep mode	External clock[2], enable all peripherals	144MHz	24.5	mA
			72MHz	14.2	
			36MHz	9.8	
		External clock[2], disable all peripherals.	144MHz	8.4	
			72MHz	6.0	
			36MHz	4.6	

Note:

[1] Based on comprehensive evaluation result, not tested in production.

[2] Enable PLL when f_{HCLK}>8MHz.

4.3.5.2 Typical current consumption

MCU is under the following conditions:

- All I/O pins are in input mode and are connected to a static level -- V_{DD} or V_{SS} (no load).
- All peripherals are disabled unless otherwise noted.
- The access time of the flash memory is adjusted to the fastest operating frequency (0 waiting periods from 0 to 32MHz, 1 waiting period from 32 to 64MHz, 2 waiting periods from 64MHz to 96MHz, 3 waiting periods from 96MHz to 128MHz, 4 waiting periods from 128MHz to 144MHz).
- Ambient temperature and V_{DD} supply voltage conditions are listed in Table 4-4.
- Instruction prefetch is enabled (note: this parameter must be set before setting the clock and bus divider).When the peripheral is turned on: $f_{PCLK1} = f_{HCLK}/4$, $f_{PCLK2} = f_{HCLK}/2$, $f_{ADCCLK} = f_{PCLK2}/4$.

Table 4-10 Typical Current Consumption in Operating Mode Running From Embedded Flash

Symbol	Parameter	Condition	f_{HCLK}	Typ [1]		Unit
				Enable all peripherals[2]	Disable all peripherals.	
I_{DD}	Supply current in operation mode	External clock[3]	144MHz	28.6	14.2	mA
			72MHz	17.7	8.1	
			36MHz	9.1	5.3	
		Run in high-speed internal RC oscillator (HSI), use AHB prescaler to reduce frequency.	128MHz	27.9	12.7	mA
			72MHz	17.5	7.2	
			36MHz	8.4	3.9	

Notes:

[1] Typical values are measured at T_A=25°C and V_{DD}= 3.3V.

[2] Add an additional 0.8mA current consumption to each analog section of the ADC. In an application environment, this current is only increased when the ADC is turned on (set ADC_CTRL2.ON bit).

[3] External clock is 8MHz, enable PLL when f_{HCLK}>8MHz.

Table 4-11 Typical Current Consumption in SLEEP Mode

Symbol	Parameter	Condition	f_{HCLK}	Typ [1]		Unit
				Enable all peripherals[2]	Disable all peripherals	
I_{DD}	Supply current in sleep mode	External clock[3]	144MHz	23.3	8	mA
			72MHz	12.9	5.3	
			36MHz	7.7	3.6	
		Run in high-speed internal RC oscillator (HSI), use AHB prescaler to reduce frequency.	128MHz	22.5	6.1	mA
			72MHz	11.8	3.5	
			36MHz	7.0	2.2	

Notes:

[1] *Typical values are measured at T_A=25°C and V_{DD}= 3.3v.*

[2] *Add an additional 0.8mA current consumption to each analog section of the ADC. In the application environment, this current is only increased when the ADC is turned on (set ADC_CTRL2.ON bit).*

[3] *External clock is 8MHz, enable PLL when f_{HCLK}>8MHz.*

4.3.5.3 Low power mode current consumption

The device is under the following conditions:

- All I/O pins are in input mode and are connected to a static level -- V_{DD} or V_{SS} (no load).
- All peripherals are disabled unless otherwise noted.

Table 4-12 Typical and Maximum Current Consumption in SHUTDOWN and STANDBY Mode

Symbol	Parameter	Condition	Typ [(1)]		Unit
			T_A =25°C	T_A =105°C	
I_{DD}	Supply current in STOP0 mode	The voltage regulator is in operation mode, low-speed and high-speed internal RC oscillators and high-speed oscillators are off (Independent watchdog is off)	260	1000	μA
		The voltage regulator is in low power consumption mode, and the low-speed and high-speed internal RC oscillators and high-speed oscillators are off (Independent watchdog is off)	120	650	
	Supply current in STOP2 mode	The external low-speed clock is turned on, RTC is running, RET-SRAM is maintained, all I/O states are maintained, and the independent watchdog is off.	5	66	
	Supply current in STANDBY mode	Low-speed RC oscillator and independent watchdog are on.	3	36	
		The internal low-speed RC oscillator is on, and the independent watchdog is off.	2.8	35	
		The internal low-speed RC oscillator and independent watchdog are off, and the low-speed oscillator and RTC is off.	2.6	34	
I_{DD_VBAT}	Supply current of Backup Area (VBAT)	Low speed oscillator and RTC is on.	2	10	

Note: (1) Based on comprehensive evaluation result, not tested in production.

4.3.6 External Clock Source Characteristics

4.3.6.1 High-speed external clock source (HSE)

The characteristic parameters given in the following table are measured using a high-speed external clock source, and the ambient temperature and supply voltage refer to the conditions specified in Table 4-4.

Table 4-13 High-speed External Clock Characteristics (Bypass Mode)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{HSE_ext}	User external clock frequency[(1)]	-	4	8	32	MHz
V_{HSEH}	OSC_IN input pin high voltage		$0.8V_{DD}$	-	V_{DD}	V
V_{HSEL}	OSC_IN input pin low voltage		V_{SS}	-	$0.3V_{DD}$	
$t_{w(HSE)}$	The time when OSC_IN is high or low[(1)]		16	-	-	ns
$t_{r(HSE)}$ $t_{f(HSE)}$	The rising or falling time of OSC_IN[(1)]		-	-	20	
$C_{in(HSE)}$	OSC_IN input capacitive reactance[(1)]	-	-	5	-	pF
$DuCy_{(HSE)}$	Duty cycle	-	45	-	55	%
I_L	OSC_IN input leakage current	$V_{SS} \leq V_{IN} \leq V_{DD}$	-	-	±1	μA

Note: (1) Guaranteed by design, not tested in production.

4.3.6.2 Low-speed external clock source (LSE)

The characteristic parameters given in the following table are measured using a low speed external clock source, and the ambient temperature and supply voltage refer to the conditions specified in Table 4-4.

Table 4-14 Low-speed External Clock Characteristics (Bypass Mode)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{LSE_ext}	User external clock frequency(1)	-	0	32.768	1000	KHz
V_{LSEH}	OSC32_IN input pin high voltage		$0.7V_{DD}$	-	V_{DD}	V
V_{LSEL}	OSC32_IN input pin low voltage		V_{SS}	-	200	mV
$t_{w(LSE)}$	The time when OSC32_IN is high or low(1)		450	-	-	ns
$t_{r(LSE)}$ $t_{f(LSE)}$	The rising or falling time of OSC32_IN(1)		-	-	50	
$DuCy_{(LSE)}$	Duty cycle	-	30	-	70	%
I_L	OSC32_IN input leakage current	$V_{SS} \le V_{IN} \le V_{DD}$	-	-	±1	µA

Note: (1) *Guaranteed by design, not tested in production.*

Figure 4-5 AC Timing Diagram of High-speed External Clock Source

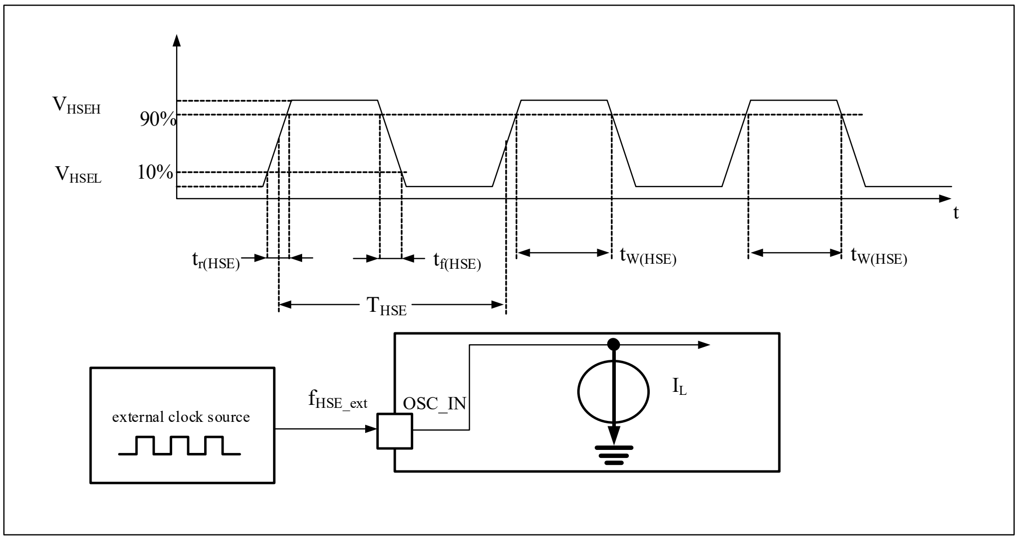
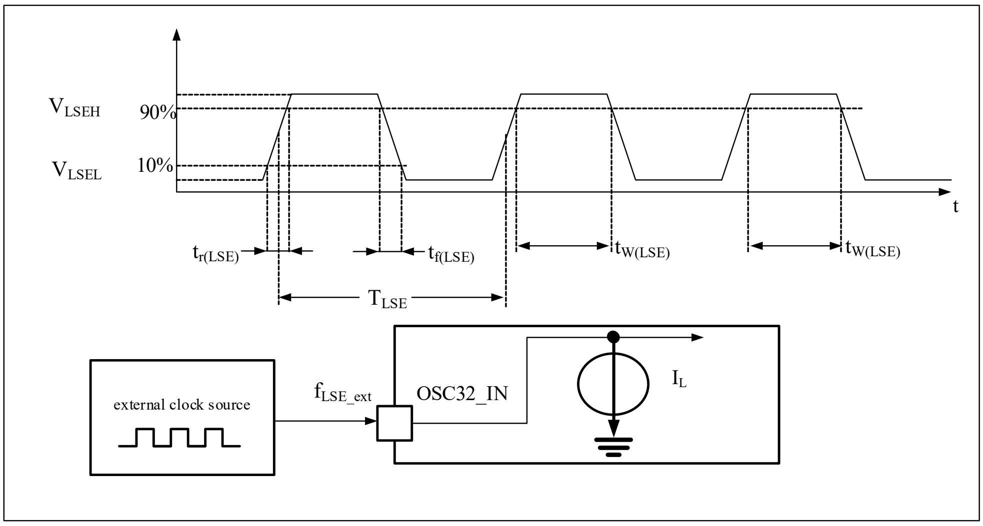


Figure 4-6 Ac Timing Diagram of Low-speed External Clock Source



High-speed external clock generated using a crystal/ceramic resonator

High speed external clocks (HSE) can be generated using an oscillator consisting of a 4~32MHz crystal/ceramic resonator. The information presented in this section is based on a comprehensive feature evaluation using typical external components listed in the table below. In applications, the resonator and load capacitance must be as close to the oscillator pins as possible to reduce output distortion and stabilization time at startup. For detailed crystal resonator parameters (frequency, package, accuracy, etc.), please consult the appropriate manufacturer. (The crystal resonator mentioned here is usually referred to as passive crystal oscillator).

Table 4-15 HSE 4~32mhz Oscillator Characteristics(1)(2)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{OSC_IN}	Oscillator frequency	-	4	8	32	MHz
R_F	Feedback resistance	-	-	160	-	kΩ
i_2	HSE driving current	V_{DD}=3.3V,V_{IN}=V_{SS} 30pF load	-	1.3	-	mA
g_m	Oscillator transconductance	Startup	-	10	-	mA/V
$t_{SU(HSE)}$ (3)	Start time(8M crystal)	V_{DD} is stabilized	-	3	-	ms

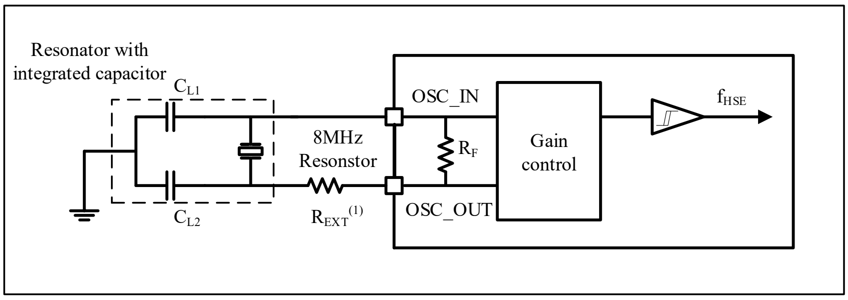
Note:

(1) The characteristic parameters of the resonator are given by the crystal/ceramic resonator manufacturer.

(2) Guaranteed by design, it is not tested in production.

(3) $t_{SU(HSE)}$ is the start time, from the time when HSE is enabled by the software to the time when a stable 8MHz oscillation is obtained. This value is measured on a standard crystal resonator and can vary widely depending on the crystal manufacturer.

Figure 4-7 Typical Application Using 8MHz Crystal



Note: (1) The REXT value depends on the properties of the crystal.

Low-speed external clock generated by a crystal/ceramic resonator

The low speed external clock (LSE) can be generated using an oscillator consisting of a 32.768KHz crystal/ceramic resonator. The information presented in this section is based on a comprehensive feature evaluation using typical external components listed in table below. In applications, the resonator and load capacitance must be as close to the oscillator pins as possible to reduce output distortion and stabilization time at startup. For detailed crystal resonator parameters (frequency, package, accuracy, etc.), please consult the appropriate manufacturer. (The crystal resonator mentioned here is usually referred to as passive crystal oscillator)

Note: For C_{L1} and C_{L2}, it is recommended to use high quality ceramic dielectric containers. Usually C_{L1} and C_{L2} have the same parameters. Crystal manufacturers usually give parameters for load capacitance as serial combinations of C_{L1} and C_{L2}.

Load capacitance C_L is calculated by the following formula: $C_L = C_{L1} \times C_{L2} / (C_{L1} + C_{L2}) + C_{stray}$, where C_{stray} is the capacitance of the pin and the PCB or PCB-related capacitance.

For example, if a resonator with a load capacitance of C_L=6pF is selected and C_{stray}=2pF, then C_{L1}=C_{L2}=8pF.

Table 4-16 LSE Oscillator Characteristics (f_{LSE}=32.768kHz)(1)

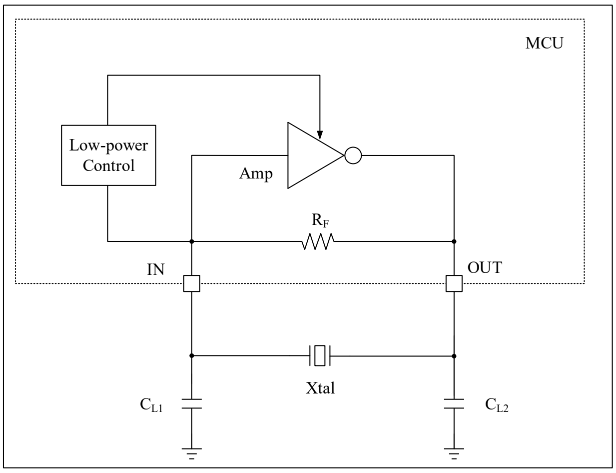
Symbol	Parameter	Condition	Min	Typ	Max	Unit
R_F	Feedback resistance	-	-	5	-	MΩ
g_m	Oscillator transconductance	-	5	-	-	µA/V
$t_{SU(LSE)}$(2)	Startup time	V_{DD} is stabilized	-	2	-	s

Note:

(1) Guaranteed by design, it is not tested in production.

(2) $T_{SU(LSE)}$ is the startup time, which is the period from the LSE enabled by the software to the stable 32.768kHz oscillation. This value is measured on a standard crystal resonator and can vary widely depending on the crystal manufacturer.

Figure 4-8 Typical Application of 32.768kHz Crystal(1)(2)



Notes:

(1) Please refer to the Crystal Selection Guide.

(2) To ensure the working stability of the crystal, do not flip the adjacent pins when the crystal is working.

4.3.7 Internal Clock Source Characteristics

The characteristic parameters given in the following table were measured using ambient temperature and supply voltage in accordance with Table 4-4.

4.3.7.1 High speed internal (HSI) RC oscillator

Table 4-17 HSI Oscillator Characteristics(1)(2)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{HSI}	frequency	VDD=3.3V, T_A=25°C, after calibration	7.92(3)	8	8.08(3)	MHz
$DuCy_{(HSI)}$	Duty cycle	-	45	-	55	%
ACC_{HSI}	Temperature drift of HSI oscillator(4)	VDD=3.3V， T_A= -40~105°C	-2.5	-	2.5	%
$t_{SU(HSI)}$	HSI oscillator start-up time	-	-	-	5	µs
$I_{DD(HSI)}$	HSI oscillator power consumption	-	-	40	-	µA

Notes:

(1) V_{DD}= 3.3V, T_A=-40 ~ 105°C, unless otherwise specified.

(2) Guaranteed by design, not tested in production.

(3) Production calibration accuracy, excluding welding effects. Welding brings about +1.5% frequency deviation range.

(4) Frequency deviation includes the effect of welding, data is from sample testing, not tested in production.

4.3.7.2 Low speed internal (LSI) RC oscillator

Table 4-18 LSI Oscillator Characteristics(1)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{LSI}(2)	Output frequency	25°C calibration, VDD =3.3V	38	40	42	KHz
		VDD =1.8V ~3.6V, T_A = -40~105°C	30	40	60	KHz
$t_{SU(LSI)}$ (2)	LSI oscillator start-up time	-	-	40	80	µs
$I_{DD(LSI)}$ (2)	LSI oscillator power consumption	-	-	0.1	-	µA

Note:

(1) V_{DD}= 3.3V, T_A=-40 ~ 105°C, unless otherwise specified.

(2) Guaranteed by design, not tested in production.

4.3.8 Time To Wake Up From Low Power Mode

The wake-up time listed in Table 4-19 is measured during the wake-up phase of an 8MHz HSI RC oscillator. The clock source used when waking up depends on the current operating mode:

- STOP0/STOP2/STANDBY mode: Clock source is RC oscillator.
- SLEEP mode: Clock source is the clock used when entering SLEEP mode.

All times were measured using ambient temperature and supply voltage in accordance with Table 4-4.

Table 4-19 Wake-up Time in Low Power Mode

Symbol	Parameter	Typ	Unit
$t_{WUSLEEP}$(1)	Wake up from sleep mode	480	ns
$t_{WUSTOP0}$(1)	Wake up from STOP0 (voltage regulator is in running mode)	20	µs
	Wake up from STOP0 (voltage regulator is in low power mode)	22	
$t_{WUSTOP2}$(1)	Wake up from STOP2	40	
$t_{WUSTDBY}$(1)	Wake up from STANDBY mode	100	

Note: (1) The wake-up time is measured from the start of the wake-up event to the first instruction read by the user program.

4.3.9 PLL Characteristics

The parameters listed in Table 4-20 are measured when the ambient temperature and power supply voltage refer to the conditions in Table 4-4.

Table 4-20 PLL Characteristic

Symbol	Parameter	Value			Unit
		Min	Typ	Max (1)	
f_{PLL_IN}	PLL input clock(2)	4	8.0	32	MHz
	PLL input clock duty cycle	40	-	60	%
f_{PLL_OUT}	PLL frequency doubling output clock	32	-	144	MHz
t_{LOCK}	PLL Ready indicates the signal output time.	-	-	150	µs
Jitter	Rms cycle-to-cycle jitter @144MHz	-	5	-	ps
Ipll	Operating Current of PLL @144MHz VCO frequency.	-	700	-	uA

Notes:

(1) Based on comprehensive evaluation, not tested in production.

(2) Care needs to be taken to use the correct frequency doubling factor to input the clock frequency according to PLL so that f_{PLL_OUT} is within the allowable range.

4.3.10 FLASH Memory Characteristics

Unless otherwise specified, all characteristic parameters are obtained at T_A= -40~105°C.

Table 4-21 Flash Memory Characteristics

Symbol	Parameter	Condition	Min(1)	Typ (1)	Max(1)	Unit
tprog	32-bit programming time	T_A = -40~105°C	-	112	225	µs
t_{ERASE}	Page (2K bytes) erase time	T_A = -40~105°C	-	2	20(2) 100(3)	ms
t_{ME}	Whole erase time	T_A = -40~105°C	-	-	100	ms
I_{DD}	Power supply current	Read mode, f_{HCLK}=144MHz,3 waiting cycles, V_{DD}=3.3V	-	-	3.62	mA
		Write mode, f_{HCLK}=144MHz, V_{DD}=3.3V	-	-	6.5	mA
		Erase mode, f_{HCLK}=144MHz, V_{DD}=3.3V	-	-	4.5	mA
		Power-down mode/shutdown, V_{DD}= 3.3 ~ 3.6V.	-	-	0.035	µA
Vprog	Programming voltage	-	1.8	3.0	3.6	V

Notes:

(1) Guaranteed by design, not tested in production.

(2) Memory space with 10k erase times

(3) Memory space with 100k erasing times

Table 4-22 Flash Endurance and Data Retention

Symbol	Parameter	Condition	Min(1)	Unit
N_{END}	Endurance (Note: number of erasures)	Ta =-40 ~ 105°C (suffix 7); The Flash capacity is 256KB.	10	Thousand times
		Ta =-40 ~ 105°C (suffix 7); The Flash capacity is 512KB, of which the first 256KB of storage space	10	
		Ta =-40 ~ 105°C (suffix 7); The Flash capacity is 512KB, including the last 256KB of storage space.	100	
t_{RET}	Data retention period	T_A= 85°C	20	year

Note: (1) Based on comprehensive evaluation, not tested in production.

4.3.11 Absolute Maximum (Electrical Sensitivity)

Based on three different tests (ESD, LU), a specific measurement method is used to test the strength of the chip to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharge (a positive pulse followed by a negative pulse one second later) is applied to all pins of all samples.

Table 4-23 Absolute Maximum ESD Value

Symbol	Parameter	Condition	Type	Min(1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (Human body model)	T_A = +25 °C, In accordance with MIL-STD-883K Method 3015.9	3A	4000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (Charging device model)	T_A = +25 °C, In accordance with ESDA/JEDEC JS-002-2018	C3	1000	

Note: (1) Based on comprehensive evaluation, not tested in production.

Static latch-up

In order to evaluate the latch-up performance, two complementary static latching tests need to be performed on 6 samples:

- Supply voltage exceeding limit for each power pin.
- Current is injected into each input, output, and configurable I/O pin.

This test conforms to JEDEC78E integrated circuit latch-up standard.

Table 4-24 Electrical Sensitivity

Symbol	Parameter	Condition	Type	Min(1)
LU	Static latch-up type	T_A = +25 °C , in accordance with JEDEC78E	Class II A	±100mA, 1.5*V_{DDMAX}

1. Test at room temperature.

4.3.12 I/O Port Characteristics

General input/output characteristics

Unless otherwise specified, the parameters listed in the following table are measured according to the conditions in Table 4-4. All I/O ports are CMOS and TTL compatible.

Table 4-25 I/O Static Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{IL}	Input low level voltage	TTL port	Vss	-	0.8	V
V_{IH}	Input high level voltage		2	-	V_{DD}	
V_{IL}	Input low level voltage	CMOS port	Vss	-	0.35 V_{DD}	
V_{IH}	Input high level voltage		0.65 V_{DD}	-	V_{DD}	
Vhys	Schmitt trigger voltage hysteresis(1)	V_{DD}=3.3V	200	-	-	mV
		V_{DD}=2.5V	200	-	-	
		V_{DD}=1.8V	0.1*V_{DD}(2)	-	-	
I_{lkg}	Input leakage current(3)	V_{DD}=Maximum V_{PAD}=0 or V_{PAD}=V_{DD}(5)	-1	-	1	µA
R_{PU}	Weak pull-up equivalent resistance(4)	V_{DD}=3.3V,V_{IN}= V_{SS}	75	-	220	kΩ
		V_{DD} =2.5V, V_{IN} = V_{SS}	95	-	310	
		V_{DD} = 1.8V, V_{IN} = V_{SS}	135	-	500	
R_{PD}	Weak pull-down equivalent resistance(4)	V_{DD}=3.3V,V_{IN}= V_{DD}	75	-	235	kΩ
		V_{DD} = 2.5V, V_{IN} = V_{DD}	85	-	315	
		V_{DD} = 1.8V, V_{IN} = V_{DD}	120	-	495	
C_{IO}	Capacitance of I/O pin	-	-	5	-	pF

Notes:

(1) Hysteresis voltage of Schmitt trigger switch level. Based on comprehensive evaluation, not tested in production.

(2) At least 100mV.

(3) If there is reverse current backflow at the adjacent pins, the leakage current may be higher than the maximum value.

(4) Pull-up and pull-down resistors are implemented with a switchable PMOS/NMOS.

(5) V_{PAD} refers to the input voltage of the IO pin.

All I/O ports are CMOS and TTL compatible (no software configuration required) and their features take into account most of the strict CMOS process or TTL parameters:

- For VIH:

  If VDD is between [1.8V ~ 3.08V]; Uses CMOS features but includes TTL.

  If VDD is between [3.08V ~ 3.60V]; Uses TTL feature but includes CMOS.

- For VIL:

  If VDD is between [1.8V ~ 2.28V]; Uses TTL feature but includes CMOS.

  If VDD is between [2.28V ~ 3.60V]; Uses CMOS features but includes TTL.

Output drive current

GPIO (general purpose input/output port) can absorb or output up to +/-12mA current. In user applications, the number of I/O pins must ensure that the driving current does not exceed the absolute maximum rating given in Section

4.2:

- The sum of the current drawn from V_{DD} by all I/O ports, plus the maximum operating current drawn by the MCU on V_{DD}, cannot exceed the absolute maximum rating of I_{VDD} (Table 4-2).
- The sum of the current drawn by all I/O ports and drawn from V_{SS}, plus the maximum operating current drawn by the MCU on V_{SS}, cannot exceed the absolute maximum ratings, I_{VSS} (Table 4-2).

Output voltage

Unless otherwise specified, the parameters listed in Table 4-27 were measured using ambient temperature and VDD supply voltage in accordance with Table 4-4. All I/O ports are CMOS and TTL compatible.

Table 4-26 IO Driving Capability Table

Driving grade	I_{OH}(1), VDD=3.3V	I_{OL}(1), VDD=3.3V	I_{OH}(1), VDD=2.5V	I_{OL}(1), VDD=2.5V	I_{OH}(1), VDD=1.8V	I_{OL}(1), VDD=1.8V	Unit
2	-2	2	-1.5	1.5	-1.2	1.2	mA
4	-4	4	-3	3	-2.5	2.5	mA
8	-8	8	-7	7	-5	5	mA
12	-12	12	-11	11	-7.5	7.5	mA

Note: (1) Guaranteed by design, not tested in production.

Table 4-27 Output Voltage Characteristics

Symbol	Parameter	Condition	Min	Max	Unit
V_{OL}(1)	Output low level	V_{DD} = 3.3 V, I_{OL}= 2mA, 4mA, 8mA, and 12mA	V_{SS}	0.4	V
		V_{DD} = 2.5 V, I_{OL}= 1.5mA,3mA, 7mA, and 11mA	V_{SS}	0.4	
		V_{DD} = 1.8 V, I_{OL}=1.2mA, 2.5mA, 5mA, and 7.5mA	V_{SS}	0.2*V_{DD}	
V_{OH}(2)	Output high level	V_{DD} = 3.3 V, I_{OH}= -2mA, -4mA, -8mA, and -12mA	2.4(3)	V_{DD}	
		V_{DD} = 2.5 V, I_{OH}= -1.5mA, -3mA, -7mA, and -11mA	1.8(3)	V_{DD}	
		V_{DD} = 1.8 V, I_{OH}= -1.2mA, -2.5mA, -5mA, and -7.5mA	0.8*V_{DD}	V_{DD}	

Notes:

(1) The current I_{IO} absorbed by the chip must always follow the absolute maximum rating given in Table 4-2, and the sum of I_{IO} (all I/O pins and control pins) must not exceed I_{VSS}.

(2) The current I_{IO} output from the chip must always follow the absolute maximum rating given in Table 4-2, and the sum of I_{IO} (all I/O pins and control pins) must not exceed I_{VDD}.

(3) PC13, PC14 and PC15 are not in this range.

Input-output AC characteristics

The definitions and values of input and output AC characteristics are shown in Figure 4-9 and Table 4-28.

Unless otherwise specified, the parameters listed in Table 4-28 were measured using ambient temperature and supply voltage in accordance with Table 4-4.

Table 4-28 Output AC Characteristics(1)

DS_CFGy Configuration	PMODEy[1:0] Configuration	Symbol	Parameter	Condition	Min	Max	Unit
0	xx (2mA)	$f_{max(IO)out}$	Maximum frequency(2)	C_L=5pF,V_{DD}=3.3V	-	75	MHz
				C_L=5pF,V_{DD}=2.5V	-	50	
				C_L=5pF,V_{DD}=1.8V	-	30	
		$t_{(IO)out}$	Output delay	C_L=5pF,V_{DD}=3.3V	-	3.66	ns
				C_L=5pF,V_{DD}=2.5V	-	4.72	
				C_L=5pF,V_{DD}=1.8V	-	7.12	
		$t_{(IO)in}$	Input delay	C_L=50fF,V_{DD}=2.97V,V_{DDD}=0.81V input characteristics at 1.8V and 2.5V are derated	-	2	ns
1	00/01	$f_{max(IO)out}$		C_L= 10pF, V_{DD}= 3.3V	-	90	MHz

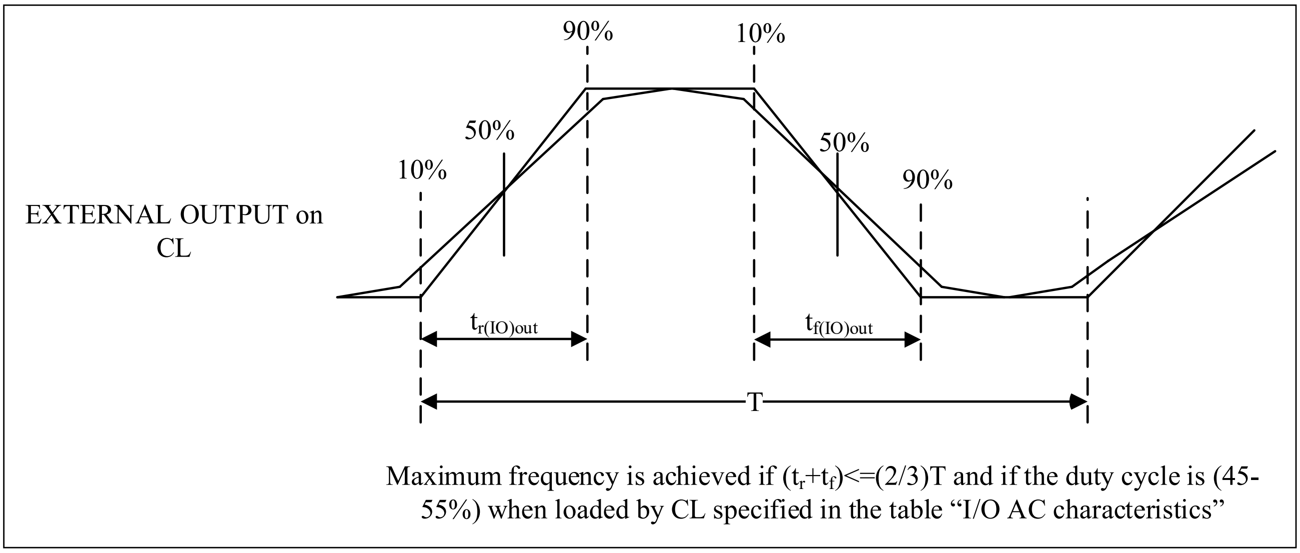
DS_CFGy Configuration	PMODEy[1:0] Configuration	Symbol	Parameter	Condition	Min	Max	Unit
	(4mA)		Maximum frequency(2)	C_L=10pF,V_{DD}=2.5V	-	60	
				C_L=10pF,V_{DD}=1.8V	-	40	
		$t_{(IO)out}$	Output delay	C_L= 10pF, V_{DD}= 3.3V	-	3.5	ns
				C_L=10pF,V_{DD}=2.5V	-	4.5	
				C_L=10pF,V_{DD}=1.8V	-	6.74	
		$t_{(IO)in}$	Input delay	C_L=50fF,V_{DD}=2.97V,V_{DDD}=0.81V input characteristics at 1.8V and 2.5V are derated	-	2	
1	10 (8mA)	$f_{max(IO)out}$	Maximum frequency(2)	C_L= 20pF, V_{DD}= 3.3V	-	100	MHz
				C_L=20pF,V_{DD}=2.5V	-	75	
				C_L=20pF,V_{DD}=1.8V	-	50	
		$t_{(IO)out}$	Output delay	C_L= 20pF, V_{DD}= 3.3V	-	3.42	ns
				C_L=20pF,V_{DD}=2.5V	-	4.73	
				C_L=20pF,V_{DD}=1.8V	-	6.53	
		$t_{(IO)in}$	Input delay	C_L=50fF,V_{DD}=2.97V,V_{DDD}=0.81V input characteristics at 1.8V and 2.5V are derated	-	2	
1	11 (12mA)	$f_{max(IO)out}$	Maximum frequency(2)	C_L= 30pF, V_{DD}= 3.3V	-	120	MHz
				C_L=30pF,V_{DD}=2.5V	-	90	
				C_L=30pF,V_{DD}=1.8V	-	60	
		$t_{(IO)out}$	Output delay	C_L= 30pF, V_{DD}= 3.3V	-	3.34	ns
				C_L=3pF,V_{DD}=2.5V	-	4.26	
				C_L=3pF,V_{DD}=1.8V	-	6.34	
		$t_{(IO)in}$	Input delay	C_L=50fF,V_{DD}=2.97V,V_{DDD}=0.81V input characteristics at 1.8V and 2.5V are derated	-	2	

Notes:

(1) I/O port speed can be configured by DS_CFGy and PMODEy[1:0]. See N32G4FR Series User Manual for the description of GPIO port configuration register.

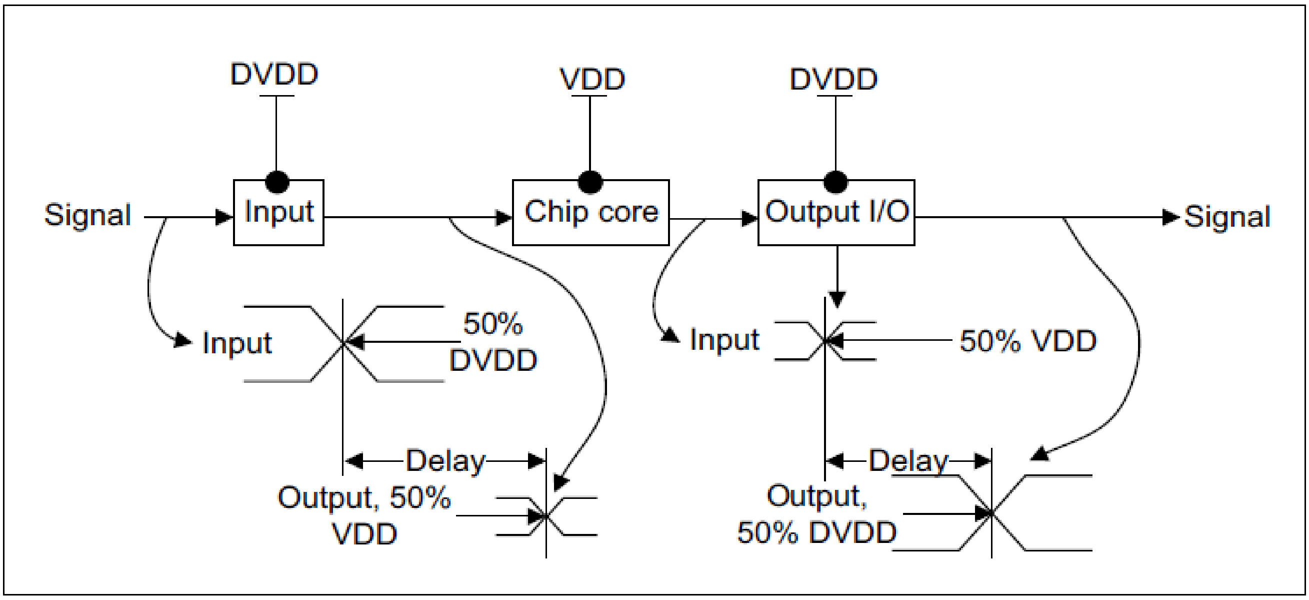
(2) The maximum frequency is Figure 4-9 Define.

Figure 4-9 Input Output AC Characteristic Definition



Maximum frequency is achieved if (t_r+t_f)<=(2/3)T and if the duty cycle is (45-55%) when loaded by CL specified in the table “I/O AC characteristics”

Figure 4-10 Transmission Delay



4.3.13 NRST Pin Characteristics

The NRST pin input driver uses CMOS technology and integrates a pull-up resistor that cannot be disconnected, R_{PU} (see Table 4-29). Unless otherwise specified, the parameters listed in Table 4-29 are measured using the ambient temperature and supply voltage in accordance with the conditions in Table 4-4.

Table 4-29 NRST Pin Characteristics

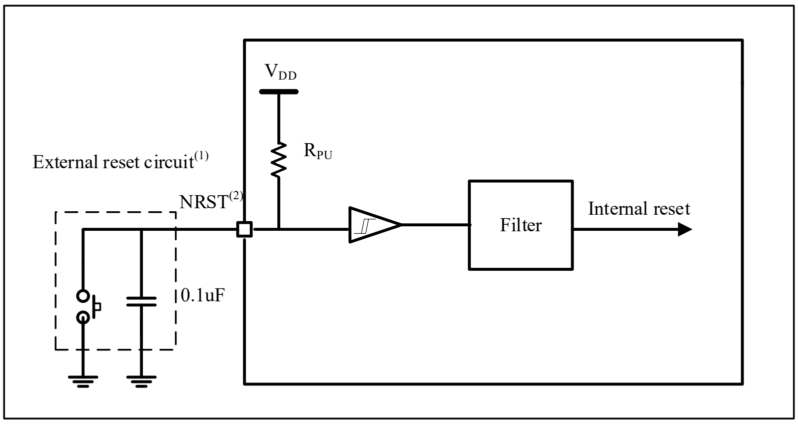
Symbol	Parameter	Condition	Min	Typ	Max	Unit
$V_{IL(NRST)}$(1)	NRST input low voltage	V_{DD} = 3.3 V	Vss	-	0.8	V
		V_{DD} = 1.8 V	Vss		0.3*VDD	
$V_{IH(NRST)}$(1)	NRST input high voltage	V_{DD} = 3.3 V	2	-	VDD	
		V_{DD} = 1.8 V	0.7*VDD	-	VDD	
$V_{hys(NRST)}$	NRST Schmitt trigger voltage hysteresis	V_{DD} = 3.3 V	200	-	-	mV
		V_{DD} = 1.8 V	0.1*VDD	-	-	V
R_{PU}	Weak pull-up equivalent resistance(2)	V_{DD} = 3.3 V	30	50	70	KΩ
$V_{F(NRST)}$(1)	NRST input filtered pulse	-	-	-	100	ns
$V_{NF(NRST)}$(1)	NRST input unfiltered pulse	-	300	-	-	ns

Notes:

(1) Guaranteed by design, not tested in production.

(2) The pull-up resistor is designed as a real resistor in series with a switchable PMOS. The resistance of this PMON/NMOS switch is very small (about 10%).

Figure 4-11 Recommended NRST Pin Protection



Notes:

(1) Filter action.

(2) The user must ensure that the NRST pin potential is below the maximum $V_{IL(NRST)}$ listed in Table 4-29, otherwise the MCU cannot be reset.

4.3.14 Timer and Watchdog Characteristics

I/O Port Characteristics for details on the features of the I/O reuse function pins (output comparison, input capture, external clock, PWM output), See section 4.3.12

Table 4-30 TIM1/8 Characteristics(1)

Symbol	Parameter	Condition	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time	-	1	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$= 144MHz	6.95	-	ns
f_{EXT}	Timer CH1 to CH4 external clock frequency	-	0	$f_{TIMxCLK}/2$	MHz
		$f_{TIMxCLK}$= 144MHz	0	72	MHz
Res_{TIM}	Timer resolution	-	-	16	bit
$t_{COUNTER}$	16-bit counter clock cycle when internal clock is selected	-	1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$= 144MHz	0.00695	455	µs
t_{MAX_COUNT}	Maximum count	-	-	65536 x 65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$= 144MHz	-	29.8	s

1. Guaranteed by design, not tested in production.

Table 4-31 TIM2/3/4/5 Characteristics(1)

Symbol	Parameter	Condition	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time	-	1	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$= 72MHz	13.9	-	ns
f_{EXT}	Timer CH1 to CH4 external clock frequency	-	0	$f_{TIMxCLK}/2$	MHz
		$f_{TIMxCLK}$= 72MHz	0	36	MHz
Res_{TIM}	Timer resolution	-	-	16	bit
$t_{COUNTER}$	16-bit counter clock cycle when internal clock is selected	-	1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$= 72MHz	0.0139	910	µs
t_{MAX_COUNT}	Maximum count	-	-	65536 x 65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$= 72MHz	-	59.6	s

Note: (1) Guaranteed by design, not tested in production.

Table 4-32 IWDG Counting Maximum and Minimum Reset Time (LSI = 40 KHz)

Prescaler	IWDG_PREDIV.PD[2:0]	Min[1] IWDG_RELV.REL[11:0]=0	Max[1] IWDG_RELV.REL[11:0]=0xFFF	Unit
/4	000	0.1	409.6	ms
/8	001	0.2	819.2	
/16	010	0.4	1638.4	
/32	011	0.8	3276.8	
/64	100	1.6	6553.6	
/128	101	3.2	13107.2	
/256	11x	6.4	26214.4	

Note: (1) Guaranteed by design, not tested in production.

Table 4-33 WWDG Counting Maximum and Minimum Reset Time (APB1 PCLK1 = 36MHz)

Prescaler	WWDG_CFG.TIMERB[1:0]	Min[1] WWDG_CGF.W[6:0]=0x3F	Max[1] WWDG_CFG.W[6:0]=0x7F	Unit
/1	00	0.113	7.28	ms
/2	01	0.227	14.56	
/3	10	0.455	29.12	
/4	11	0.910	58.25	

Note: (1) Guaranteed by design, not tested in production.

4.3.15 I2C Interface Characteristics

Unless otherwise specified, the parameters listed in Table 4-34 were measured using ambient temperature, f_{PCLK1} frequency, and V_{DD} supply voltage in accordance with Table 4-4.

The I2C interface of the N32G4FR product conforms to the standard I2C communication protocol, but has the following limitations: SDA and SCL are not "true" open leak pins, and when configured for open leak output, the PMOS tube between the pin and VDD is closed, but still exists.

I2C interface features are listed in Table 4-34. See Section 4.3.12 for details about the features of the input/output multiplexing function pins (SDA and SCL).

Table 4-34 I2C Interface Characteristics

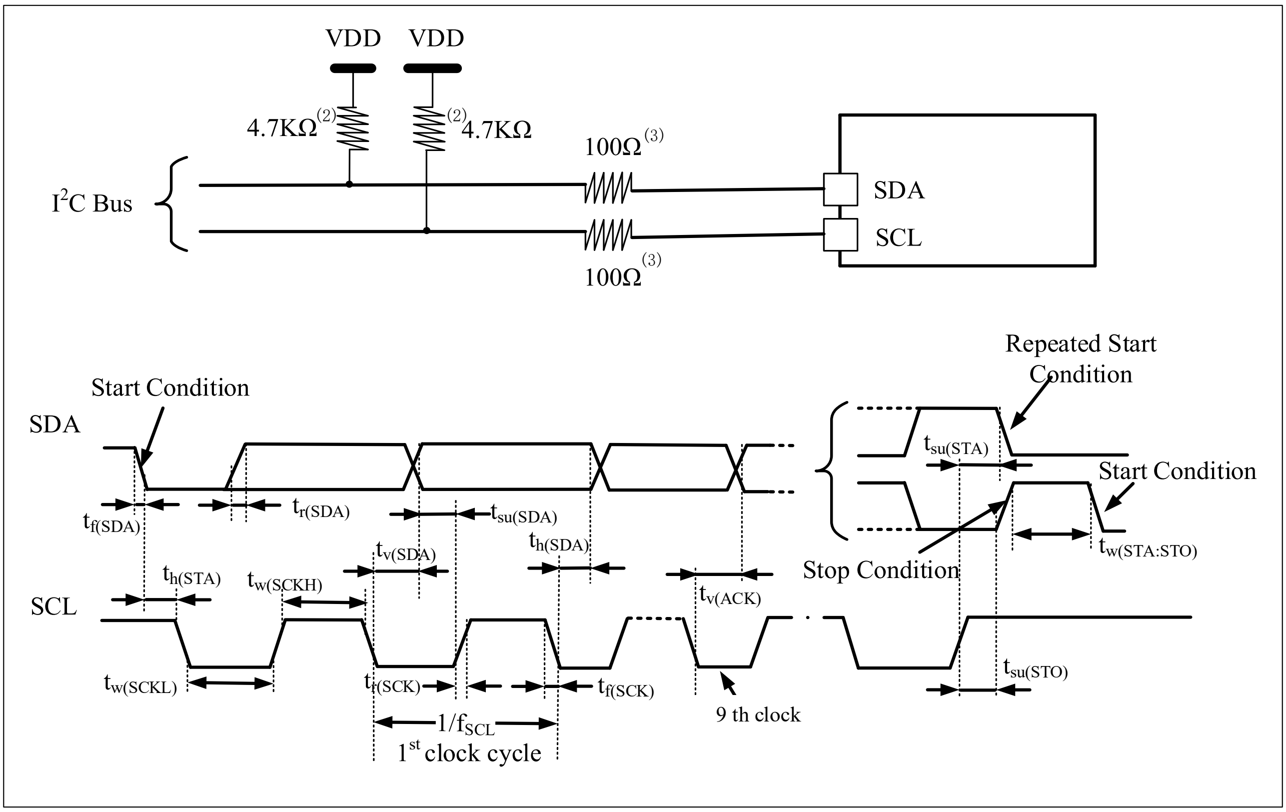
Symbol	Parameter	Standard mode(1)(2)		Fast mode(1)(2)		Fast+ mode(1)(2)		Unit
		Min	Max	Min	Max	Min	Max	
f_{SCL}	I2C interface frequency	0.0	100	0	400	0	1000	KHz
$t_{h(STA)}$	Start condition holding time	4.0	-	0.6	-	0.26	-	µs
$t_{w(SCLL)}$	SCL clock low time	4.7	-	1.3	-	0.5	-	µs
$t_{w(SCLH)}$	SCL clock high time	4.0	-	0.6	-	0.26	-	µs
$t_{su(STA)}$	Start condition establishment time of repetition	4.7	-	0.6	-	0.26	-	µs
$t_{h(SDA)}$	SDA data retention time	-	3.4	-	0.9	-	0.4	µs
$t_{su(SDA)}$	SDA setup time	250.0	-	100	-	50	-	ns
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rising time	-	1000	20+0.1Cb	300	-	120	ns
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL falling time	-	300	20+0.1Cb	300	-	120	ns
$t_{su(STO)}$	Stop condition establishment time	4.0	-	0.6	-	0.26	-	µs
$t_{w(STO:STA)}$	Time from stop condition to start condition (bus idle)	4.7	-	1.3	-	0.5	-	µs
Cb	Capacitive load per bus	-	400	-	400	-	100	pF
$t_{v(SDA)}$	Data validity time	-	3.45	-	0.9	-	0.45	µs
$t_{v\ (ACK)}$	Response effective time	-	3.45	-	0.9	-	0.45	µs

Notes:

(1) Guaranteed by design, not tested in production.

(2) To achieve the maximum frequency of standard mode I2C, f_{PCLK1} must be greater than 2MHz. To achieve the maximum frequency of fast mode I2C, f_{PCLK1} must be greater than 4MHz.

Figure 4-12 I2C Bus AC Waveform and Measurement Circuit(1)



Notes:

(1) The measuring points are set at CMOS level: 0.3V_{DD} and 0.7V_{DD}.

(2) The pull-up resistor depends on the I2C interface speed.

(3) The resistance value depends on the actual electrical characteristics. The signal line can be directly connected without serial resistance.

4.3.16 SPI/I2S Interface Characteristics

Unless otherwise specified, the SPI parameters listed in Table 4-35 / Table 4-36 and the I2S parameters listed in Table 4-37 are measured using ambient temperature, f_{PCLKx} frequency, and V_{DD} supply voltage in accordance with Table 4-4.

See Section 4.3.12 for details on the characteristics of the I/O multiplexed pins (NSS, SCLK, MOSI, MISO for SPI, WS, CLK, SD for I2S).

Table 4-35 SPI1 Features(1)

Symbol	Parameter	Condition	Min	Max	Unit
f_{SCLK} $1/t_{c(SCLK)}$	SPI clock frequency	Master mode	-	36	MHz
		Slave mode	-	36	
$t_{r(SCLK)}$ $t_{f(SCLK)}$	SPI clock rise and fall time	Capacitance: C = 30pF	-	6	ns
DuCy(SCK)	SPI slave input clock duty cycle	SPI slave mode	45	55	%
$t_{su(NSS)}^{(1)}$	NSS setup time	Slave mode	4t_{PCLK}	-	ns
$t_{h(NSS)}^{(1)}$	NSS hold time	Slave mode	2t_{PCLK}	-	
$t_{w(SCLKH)}^{(1)}$ $t_{w(SCLKL)}^{(1)}$	SCLK high and low time	Master mode	t_{PCLK} – 2	t_{PCLK} + 2	
$t_{su(MI)}^{(1)}$	Enter the data setup time.	Master mode	3.5	-	
$t_{su(SI)}^{(1)}$		Slave mode	3	-	
$t_{h(MI)}^{(1)}$	Enter the data retention time	Master mode	3	-	
$t_{h(SI)}^{(1)}$		Slave mode	3	-	
$t_{a(SO)}^{(1)(2)}$	Data output access time	Slave mode, f_{PCLK}= 20MHz	0	3t_{PCLK}	
$t_{dis(SO)}^{(1)(3)}$	Data output prohibition time	Slave mode	2	10	
$t_{v(SO)}^{(1)}$	Data output effective time	Slave mode (after enabling edge)	-	12.5	
$t_{v(MO)}^{(1)}$		Master mode (after enable edge)	-	6.5	
$t_{h(SO)}^{(1)}$	Data output holding time	Slave mode (after enabling edge)	5	-	
$t_{h(MO)}^{(1)}$		Master mode (after enable edge)	-0.5	-	

Table 4-36 SPI2/3 Features(1)

Symbol	Parameter	Condition	Min	Max	Unit
f_{SCLK} $1/t_{c(SCLK)}$	SPI clock frequency	Master mode	-	18	MHz
		Slave mode	-	18	
$t_{r(SCLK)}$ $t_{f(SCLK)}$	SPI clock rise and fall time	Capacitance: C = 30pF	-	8	ns
DuCy(SCK)	SPI slave input clock duty cycle	SPI slave mode	45	55	%
$t_{su(NSS)}^{(1)}$	NSS setup time	Slave mode	4t_{PCLK}	-	ns
$t_{h(NSS)}^{(1)}$	NSS hold time	Slave mode	2t_{PCLK}	-	
$t_{w(SCLKH)}^{(1)}$ $t_{w(SCLKL)}^{(1)}$	SCLK high and low time	Master mode	t_{PCLK} – 2	t_{PCLK} + 2	

$t_{su(MI)}$(1)	Enter the data setup time.	Master mode	SPI2	4	-	
			SPI3	5	-	
$t_{su(SI)}$(1)		Slave mode	SPI2	4	-	
			SPI3	5	-	
$t_{h(MI)}$(1)	Enter the data retention time	Master mode	SPI2	2	-	
			SPI3	2.5	-	
$t_{h(SI)}$(1)		Slave mode	SPI2	2	-	
			SPI3	2	-	
$t_{a(SO)}$(1)(2)	Data output access time	Slave mode, f_{PCLK}= 20MHz		0	$3t_{PCLK}$	
$t_{dis(SO)}$(1)(3)	Data output prohibition time	Slave mode		2	10	
$t_{v(SO)}$(1)	Data output effective time	Slave mode (after enabling edge)	SPI2	-	13.5	
			SPI3	-	17.5	
$t_{v(MO)}$(1)		Master mode (after enable edge)	SPI2	-	6.5	
			SPI3	-	9	
$t_{h(SO)}$(1)	Data output holding time	Slave mode (after enabling edge)	SPI2	4	-	
			SPI3		-	
$t_{h(MO)}$(1)		Master mode (after enable edge)	SPI2	1	-	
			SPI3		-	

Notes:

(1) *Guaranteed by design, not tested in production.*

(2) *The minimum value represents the minimum time to drive the output, and the maximum value represents the maximum time to get the data correctly.*

(3) *The minimum value represents the minimum time for turning off the output and the maximum value represents the maximum time for placing the data line in a high resistance state.*

Figure 4-13 SPI Timing Diagram-slave Mode and CLKPHA=0

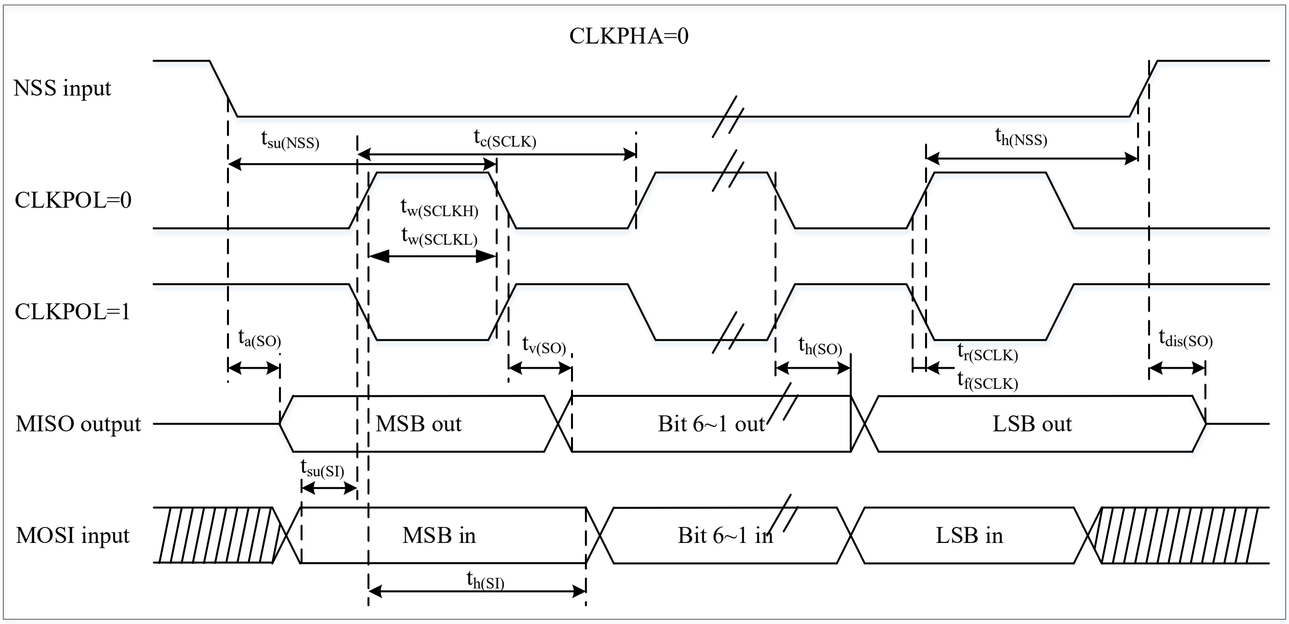
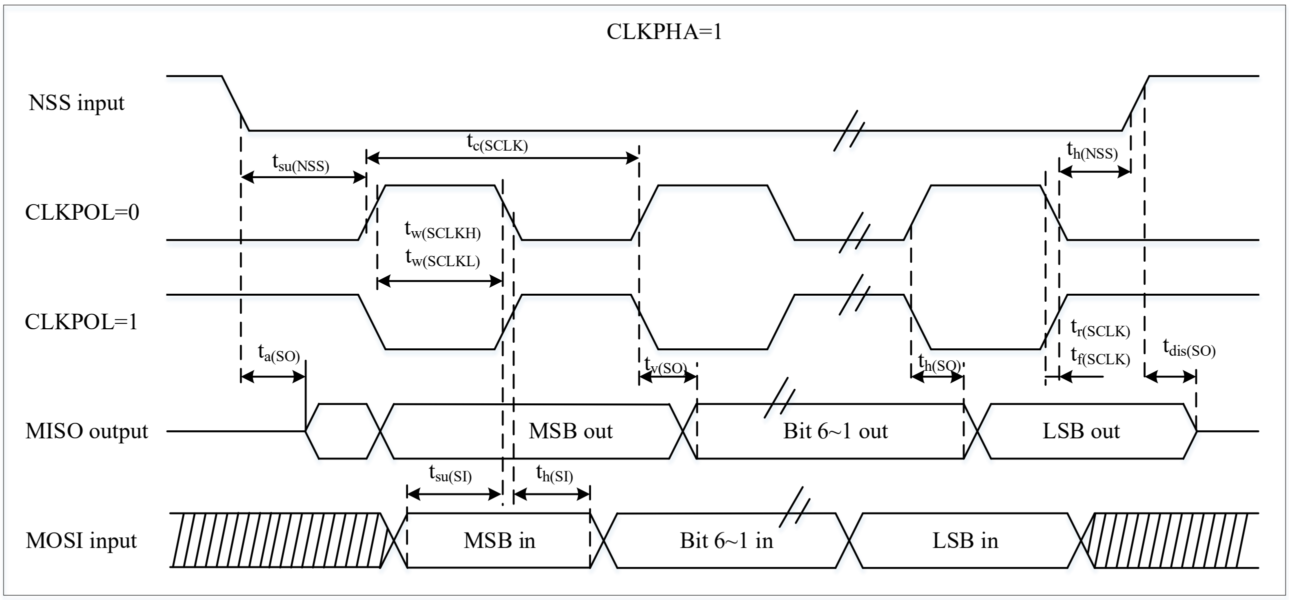
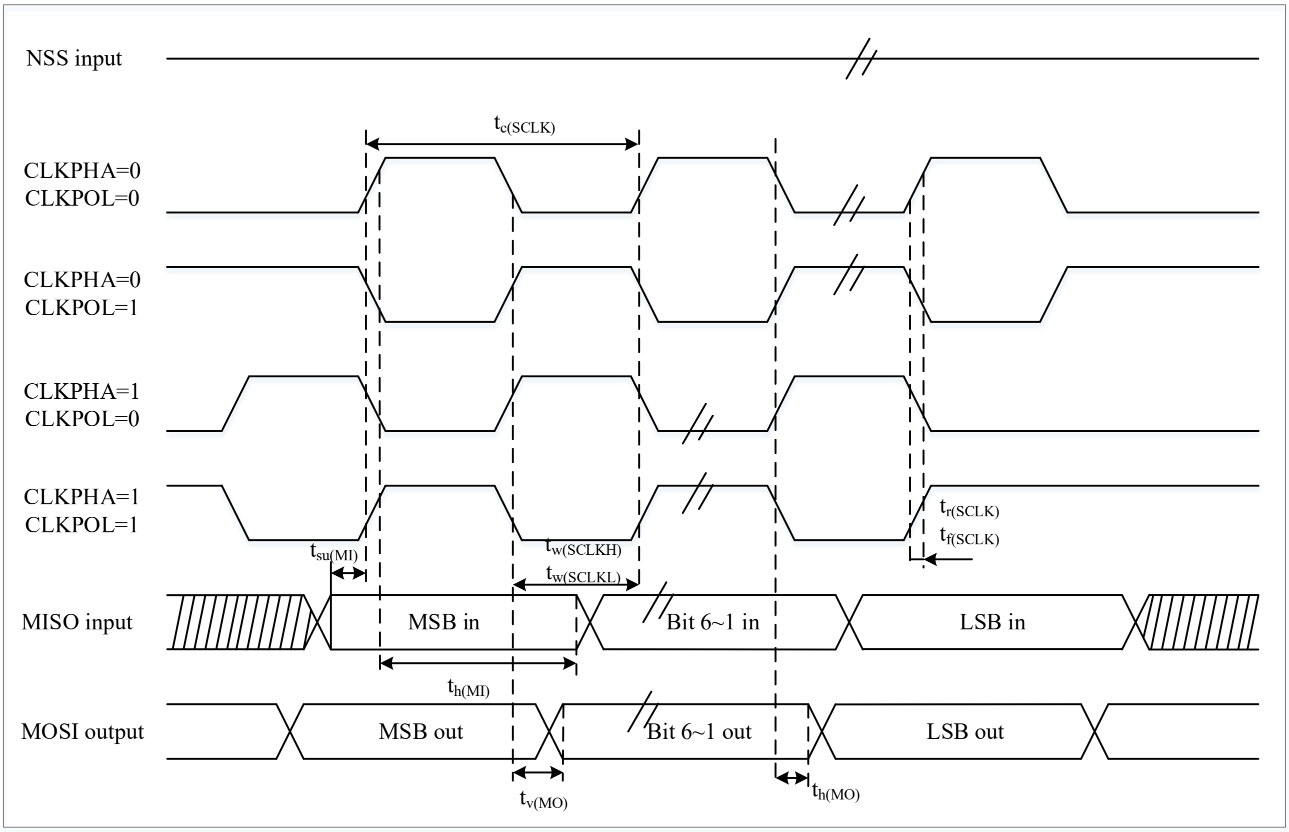


Figure 4-14 SPI Timing Diagram-slave Mode and CLKPHA=1(1)



Note: (1) The measuring points is set at $0.3V_{DD}$ and $0.7V_{DD}$.

Figure 4-15 SPI Timing Diagram-master Mode(1)



Note: (1) The measuring points is set at $0.3V_{DD}$ and $0.7V_{DD}$.

Table 4-37 I2S Characteristics(1)

Symbol	Parameter	Condition	Min	Max	Unit
f_{MCLK}	I2S master clock	Master mode	-	256Fs(3)	MHz
f_{CLK} $1/t_{c(CLK)}$	I2S clock frequency	Master mode (32bit)	-	64*Fs	
		Slave mode (32bit)	-	64*Fs	

Symbol	Parameter	Condition		Min	Max	Unit
DuCy(SCK)	I2S slave input clock duty cycle	I2S slave mode		30	70	%
$t_{r(CLK)}$ $t_{f(CLK)}$	I2S clock rise and fall time	Capacitance: CL = 50pF		-	8	ns
$t_{v(WS)}$(1)	WS valid time	Master mode	I2S2	4.5	-	
			I2S3	6.5	-	
$t_{h(WS)}$(1)	WS holding time	Master mode	I2S2	4.5	-	
			I2S3	0.5	-	
$t_{su(WS)}$(1)	WS setup time	Slave mode	I2S2	5.5	-	
			I2S3	7	-	
$t_{h(WS)}$(1)	WS holding time	Slave mode	I2S2	1.5	-	
			I2S3	2.5	-	
$t_{w(CLKH)}$(1)	CLK high and low time	Master mode, f_{PCLK}= 16MHz, audio frequency 48kHz		312.5	-	
$t_{w(CLKL)}$(1)				345	-	
$t_{su(SD\_MR)}$(1)	Enter the data setup time.	Master receiver	I2S2	4	-	
			I2S3	5	-	
$t_{su(SD\_SR)}$(1)		Slave receiver	I2S2	4	-	
			I2S3	4.5	-	
$t_{h(SD\_MR)}$(1)(2)	Enter the data retention time	Master receiver	I2S2	1.5	-	
			I2S3	1.5	-	
$t_{h(SD\_SR)}$(1)(2)		Slave receiver	I2S2	1.5	-	
			I2S3	1.5	-	
$t_{v(SD\_ST)}$(1)(2)	Data output effective time	Slave transmitter (after enable edge)	I2S2	-	14	
			I2S3	-	16.5	
$t_{h(SD\_ST)}$(1)	Data output holding time	Slave generator (after enable edge)	I2S2	3.5	-	
			I2S3	4.5	-	
$t_{v(SD\_MT)}$(1)(2)	Data output effective time	Master generator (after enable edge)	I2S2	-	6.5	
			I2S3	-	6	
$t_{h(SD\_MT)}$(1)	Data output holding time	Master generator (after enable edge)	I2S2	-0.5	-	
			I2S3	-0.5	-	

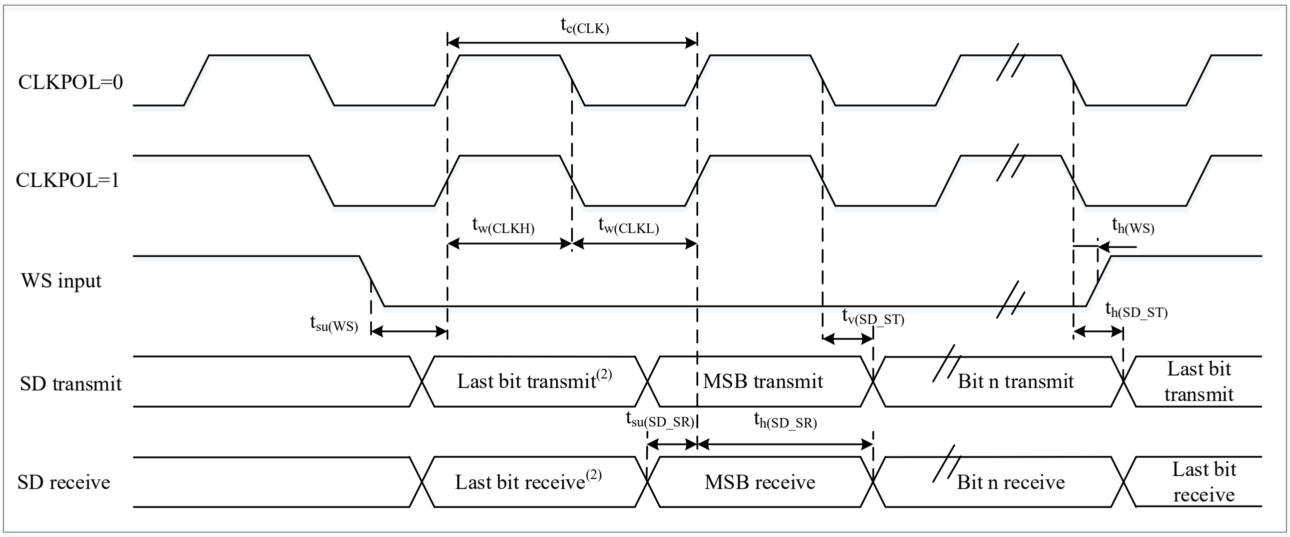
Notes:

(1) *Guaranteed by design, not tested in production.*

(2) *Depends on* f_{PCLK}. *For example, if* f_{PCLK}*=8MHz, then* $T_{PCLK}=1/f_{PCLK}$ *=125ns.*

(3) *Audio signal sampling frequency.*

Figure 4-16 I2S Slave Mode Timing Diagram (Philips Protocol)(1)

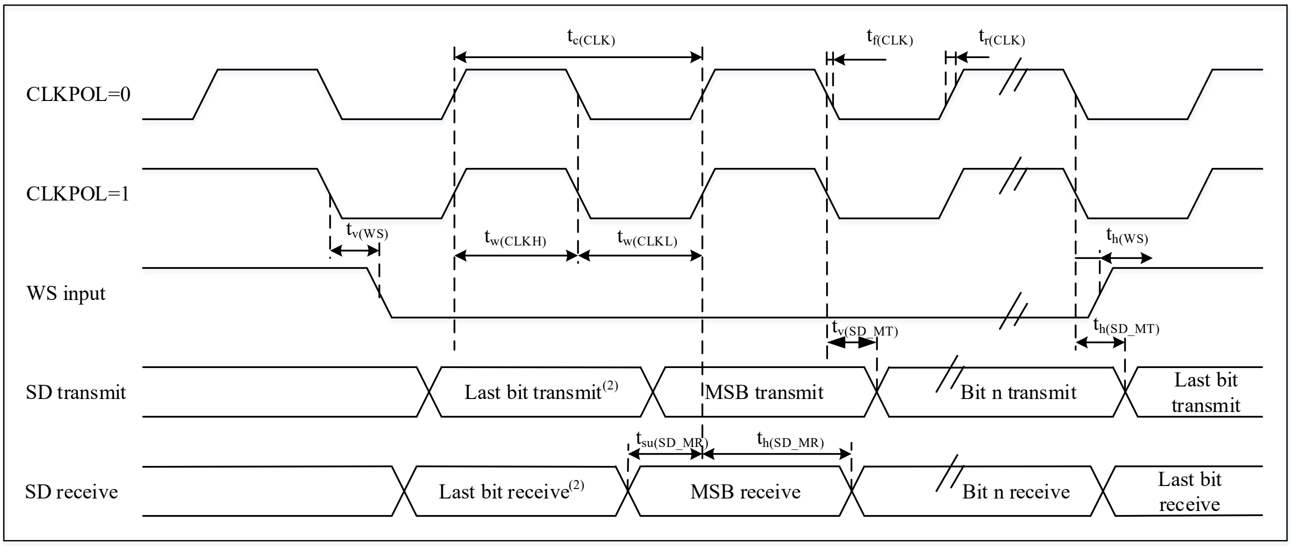


Notes:

(1) *The measuring points is set at* $0.3V_{DD}$*and* $0.7V_{DD}$*.*

(2) *Transmit/receive of the last byte. There is no transmit/receive of this least significant bit before the first byte.*

Figure 4-17 I2S Master Mode Timing Diagram (Philips Protocol)(1)



Notes:

(1) *The measuring points is set at* $0.3V_{DD}$ *and* $0.7V_{DD}$*.*

(2) *Transmit/receive of the last byte. There is no transmit/receive of this last bit before the first byte.*

4.3.17 QSPI Characteristics

Table 4-38 Characteristics of QSPI in SDR Mode

Symbol	Parameter	Min	Max	Unit
f_{CK} $1/t_{(CK)}$	QSPI clock frequency	-	36	MHz
$t_{w(CKH)}$	SCK high and low time	$t_{(CK)}/2-2$	$t_{(CK)}/2$	ns
$t_{w(CKL)}$		$t_{(CK)}/2$	$t_{(CK)}/2+2$	ns
$t_{s(IN)}$	Enter data setup time.	4.5	-	ns
$t_{h(IN)}$	Enter the data retention time	4	-	ns
$t_{v(OUT)}$	Effective time of output data	-	5.5	ns
$t_{h(OUT)}$	Output data retention time	-0.15	-	ns

Figure 4-18 Timing of QSPI in SDR Mode

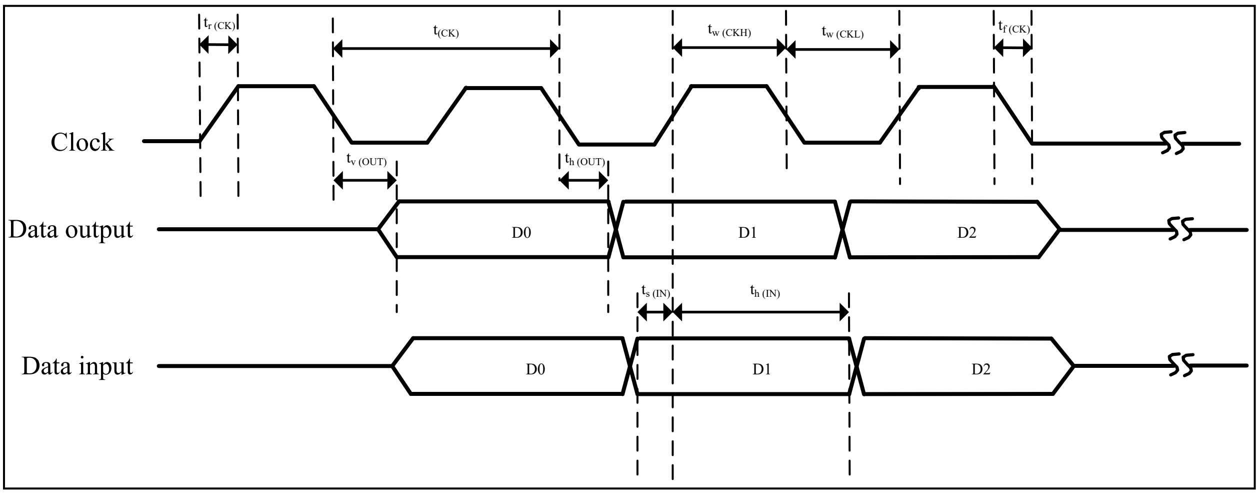
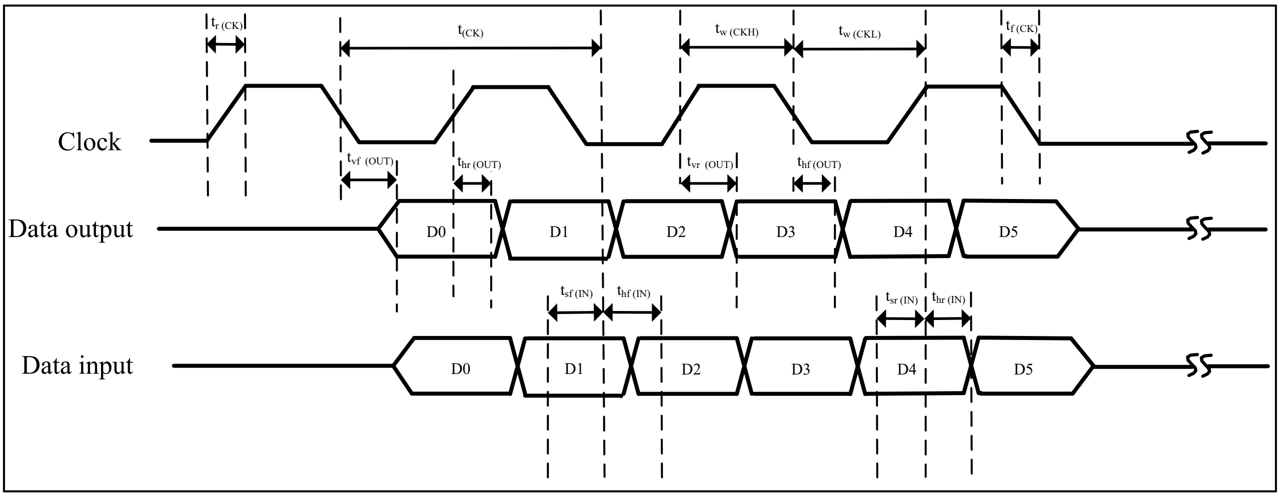


Table 4-39 Characteristics of QSPI in DDR Mode

Symbol	Parameter	Min	Max	Unit
f_{CK} $1/t_{(CK)}$	QSPI clock frequency	-	36	MHz
$t_{w(CKH)}$	SCK high and low time	$t_{(CK)}/2-2$	$t_{(CK)}/2$	ns
$t_{w(CKL)}$		$t_{(CK)}/2$	$t_{(CK)}/2+2$	ns
$t_{sf(IN)}$; $t_{sr(IN)}$	Enter data setup time.	4.5	-	ns
$t_{hf(IN)}$; $t_{hr(IN)}$	Enter the data retention time	4.5	-	ns
$t_{vf(OUT)}$; $t_{vr(OUT)}$	Effective time of output data	-	12	ns
$t_{hf(OUT)}$; $t_{hr(OUT)}$	Output data retention time	6	-	ns

Figure 4-19 Timing of QSPI in DDR Mode



4.3.18 SD/SDIO Master Interface Characteristics

Unless otherwise specified, the parameters listed in Table 4-40 are measured using ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage in accordance with the conditions in Table 4-4.

For details on the characteristics of the I/O alternate function pins (D[7:0], CMD, CK), see Section 4.3.12.

Figure 4-20 SDIO High-speed Mode

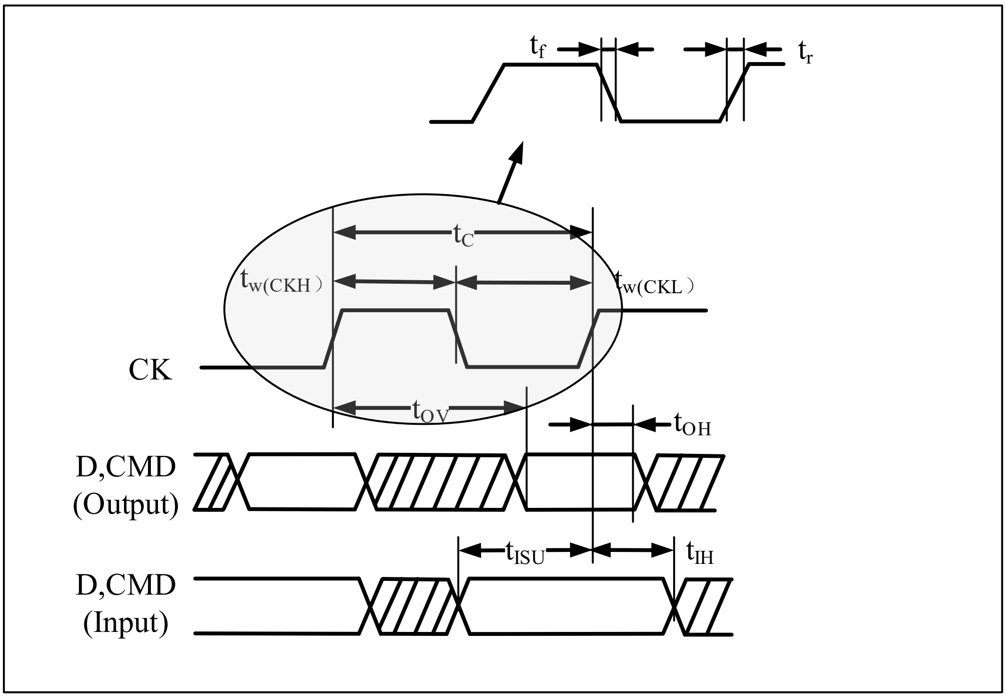


Figure 4-21 SD Default Mode

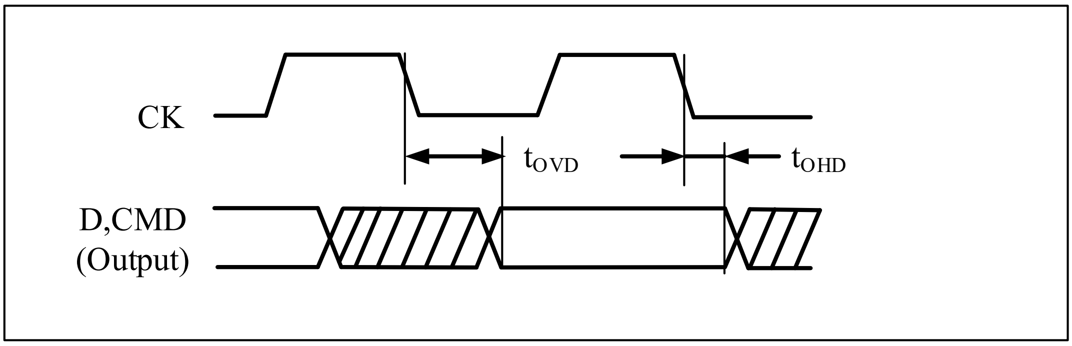


Table 4-40 SD/MMC Interface Features

Symbol	Parameter	Condition	Min	Max	Unit
f_{PP}	Clock frequency in data transmission mode	CL ≤ 30pF	0	48	MHz
$t_{W(CKL)}$	Clock low time, f_{PP} = 16 MHz	CL ≤ 30pF	32	-	ns
$t_{W(CKH)}$	Clock high time	CL ≤ 30pF	30	-	
t_r	Clock rising time	CL ≤ 30pF	-	6	
t_f	Clock falling time	CL ≤ 30pF	-	6	
CMD, D input (refer to CK)					
t_{ISU}	Enter the setup time.	CL ≤ 30pF	1	-	ns
T_{IH}	Enter holding time	CL ≤ 30pF	1	-	
CMD, D output in MMC and SD high-speed mode (refer to CK)					
t_{OV}	Output effective time	CL ≤ 30pF	-	6	ns
t_{OH}	Output holding time	CL ≤ 30pF	0	-	
CMD, D output in SD default mode (refer to CK)					
t_{OVD}	Output valid default time	CL ≤ 30pF	-	8	ns
t_{OHD}	Output holding default time	CL ≤ 30pF	-1	-	

4.3.19 USB Characteristics

USB (full speed) interface has been certified by USB-IF.

Table 4-41 USB Startup Time

Symbol	Parameter	Max	Unit
$t_{STARTUP}$(1)	USB transceiver startup time	1	µs

Note: (1) Guaranteed by design, not tested in production.

Table 4-42 USB DC Characteristic

Symbol	Parameter	Condition	Min(1)	Max(1)	Unit
Input level					
V_{DD}	USB operating voltage(2)	-	3.0(3)	3.6	V
V_{DI}(4)	Differential input sensitivity	I(USBDP，USBDM)	0.2	-	V
V_{CM}(4)	Differential common mode range	Include V_{DI} scope	0.8	2.5	
V_{SE}(4)	Single ended receiver threshold	-	1.3	2.0	
Output level					
V_{OL}	Static output low level	1.5kΩ R_L connected to 3.6V(5)	-	0.3	V
V_{OH}	Static output high level	15kΩ R_L connected to V_{SS}(5)	2.8	3.6	

Notes:

(1) All voltage measurements are based on the ground wire of the device.

(2) USB operating voltage is 3.0~3.6V in order to be compatible with the USB2.0 full-speed electrical specification.

(3) The correct USB function of N32G4FR series products can be guaranteed at 2.7V, instead of degraded electrical characteristics in the voltage range of 2.7~3.0V.

(4) Guaranteed by comprehensive evaluation, not tested in production.

(5) R_L is the load connected to the USB drive.

Figure 4-22 USB Timing: Definition of Data Signal Rise and Fall Time

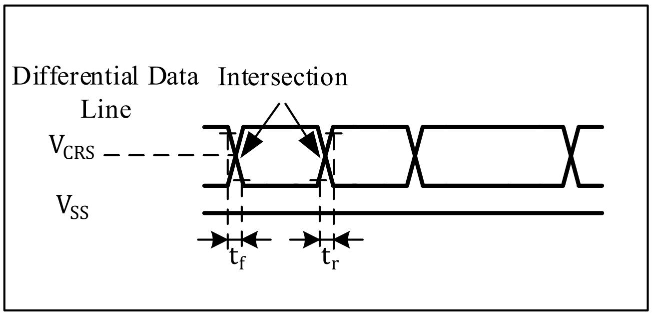


Table 4-43 Full-speed of USB Electrical Characteristics

Symbol	Parameter	Condition	Min[1]	Max[1]	Unit
t_r	Rise time[2]	CL ≤ 50pF	4	20	ns
t_f	Falling time[2]	CL ≤ 50pF	4	20	ns
t_{rfm}	Rising-falling time matching	t_r / t_f	90	110	%
V_{CRS}	Output signal cross voltage	-	1.3	2.0	V
Rs	Output series matching resistor	The matching resistor needs to be external, close to the chip pin.	27	39	Ω

Notes:

(1) Guaranteed by design, not tested in production.

(2) Measurement data signal from 10% to 90%. For more details, see Chapter 7 (Version 2.0) of the USB Specification.

4.3.20 Digital Video Port (DVP) Interface Characteristics

Table 4-44 shows the characteristics of DVP interface signal, Figure 4-23 shows the relevant time sequence.

Figure 4-23 DVP Interface Timing Diagram

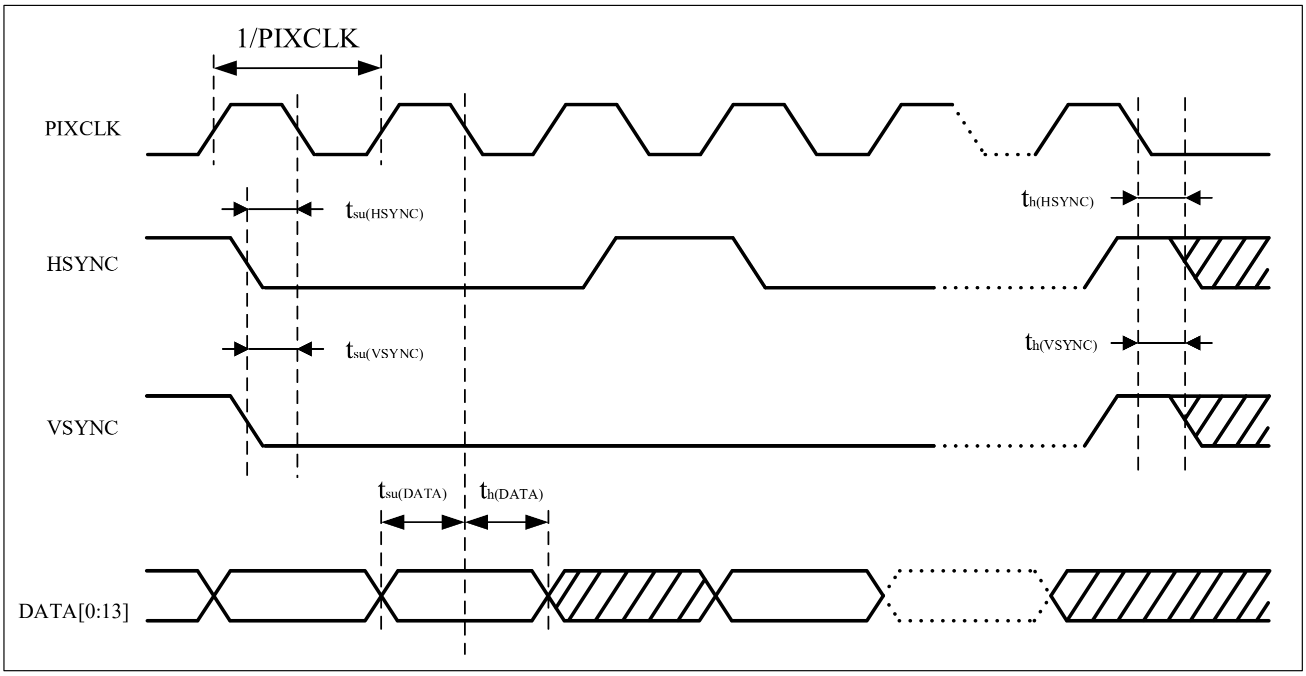


Table 4-44 Dynamic Characteristics of DVP Signal

Symbol	Parameter	Condition	Min	Max	Unit
PCLK	Pixel clock input	-	0	24	MHz
Dpixel	Pixel clock input duty cycle	-	30	70	%
$t_{su(DATA)}$	Enter the data setup time.	-	4	-	ns
$t_{h(DATA)}$	Data retention time	-	5	-	
$t_{su(HSYNC)}$	HSYNC Enter Setup Time	-	6.5	-	
$t_{su(VSYNC)}$	VSYNC Enter the setup time	-	6	-	
$t_{h(HSYNC)}$ $t_{h(VSYNC)}$	HSYNC/VSYNC input hold time	-	3.5	-	

4.3.21 Controller Area Network (CAN) Interface Characteristics

See Section 4.3.12 for details on the features of the input/output alternate function pins (CAN_TX and CAN_RX).

4.3.22 12-bit Analog-to-digital converter (ADC) Electrical Parameters

Unless otherwise specified, the parameters in Table 4-45 are measured using ambient temperature, f_{HCLK} frequency, and V_{DDA} supply voltage in accordance with the conditions in Table 4-4.

Note : It is recommended to perform a calibration at each power up.

Table 4-45 ADC Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{DDA}	supply voltage	-	1.8	-	3.6	V
V_{REF+}	Positive reference voltage	-	1.8	-	V_{DDA}	
f_{ADC}	ADC clock frequency	-	-	-	80	MHz
$fs^{(2)}$	Sampling rate	$1.8V \leq VDD \leq 3.6V$ Resolution 12-bit	$0.01^{(2)}$	-	$4.7^{(1)}$	MHz
		$1.8V \leq V_{DD} \leq 3.6V$, Resolution 10-bit	$0.012^{(2)}$	-	$6.1^{(1)}$	MHz
		$1.8V \leq V_{DD} \leq 3.6V$, Resolution 8-bit	$0.014^{(2)}$	-	$7.3^{(1)}$	MHz
		$1.8V \leq V_{DD} \leq 3.6V$, Resolution 6-bit	$0.0175^{(2)}$	-	$8.9^{(1)}$	MHz
V_{AIN}	Conversion voltage range$^{(3)}$	-	0(V_{IN} or V_{REF-} Connect to ground)	-	V_{REF+}	V
$R_{ADC}^{(2)}$	Sampling switch resistance	Fast channel, Under the condition of 3.6V voltage	-	-	137.6	Ω
		Slow channel, Under the condition of 3.6V voltage	-	-	147	Ω
$C_{ADC}^{(2)}$	Internal sample and hold capacitor	-	-	5	-	pF
SNDR	Signal noise distortion ration	-	-	65	-	dBFS
T_{cal}	Calibration time	-	82			$1/f_{ADC}$
$t_S^{(2)}$	Sampling time	f_{ADC} = 80 MHz fast channel Resolution 12-bit	0.056	-	8.35	µs
		f_{ADC} = 80 MHz slow channel Resolution 12-bit	0.056	-	8.35	
$Ts^{(2)}$	Sampling cycles	f_{ADC} = 80 MHz fast channel Resolution 12-bit	4.5	-	601.5	$1/f_{ADC}$
		f_{ADC} = 80 MHz slow channel Resolution 12-bit	4.5	-	601.5	
$t_{STAB}^{(2)}$	Power-up time	-	6	10	20	µs
$t_{CONV}^{(2)}$	Total conversion time of (including sampling time)	-	8~614 (sampling T_S + gradually approaching 6.5/8.5/10.5/12.5)			$1/f_{ADC}$

Notes:

(1) *Only fast channel support, $f_{ADC} = 80$ MHz.*

(2) *Guaranteed by design, not tested in production.*

(3) *V_{REF+} internally connects to V_{DDA} and V_{REF-} internally connects to V_{SSA}.*

Formula 1: maximum R_{AIN} formula

$$R_{AIN} < \frac{T_S}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$$

The above formula (Formula 1) is used to determine the maximum external impedance so that the error can be less than 1/4 LSB. Where N=12 (representing 12-bit resolution).

Table 4-46 ADC Sampling Time(1)(2)

Input	Resolution	Rin(kΩ)	Typical value of minimum sampling time（ns）	Input	Resolution	Rin(kΩ)	Typical value of minimum sampling time（ns）
Fast channel	12-bit	0.06	37	Slow channel	12-bit	0.05	53
		0.36	45			0.35	73
		0.86	79			0.85	103
		4.86	300			4.85	345
		9.86	576			9.85	651
		19.86	1131			19.85	1257
		49.86	2776			49.85	3051
		99.86	5475			99.85	5982
Fast channel	10-bit	0.06	25	Slow channel	10-bit	0.05	46
		0.36	39			0.35	61
		0.86	64			0.85	88
		4.86	250			4.85	357
		9.86	478			9.85	540
		19.86	935			19.85	1040
		49.86	2294			49.85	2526
		99.86	4532			99.85	4963
Fast channel	8-bit	0.06	22	Slow channel	8-bit	0.05	39
		0.36	33			0.35	50
		0.86	52			0.85	71
		4.86	202			4.85	234
		9.86	391			9.85	457
		19.86	800			19.85	1012
		49.86	1838			49.85	2027
		99.86	3632			99.85	3984
Fast channel	6-bit	0.06	19	Slow channel	6-bit	0.05	32
		0.36	27			0.35	40
		0.86	41			0.85	56
		4.86	153			4.85	177
		9.86	292			9.85	330
		19.86	569			19.85	642
		49.86	1435			49.85	1666

Input	Resolution	Rin(kΩ)	Typical value of minimum sampling time（ns）	Input	Resolution	Rin(kΩ)	Typical value of minimum sampling time（ns）
		99.86	3001			99.85	3919

Notes:

(1) Guaranteed by design, not tested in production.

(2) Typical values are measured at TA=25°C and VDD= 3.3V.

Table 4-47 ADC Accuracy-limited Test Conditions(1)(2)

Symbol	Parameter	Test condition	Typ	Max	Unit
ET(4)	Composite error	f_{HCLK} = 72 MHz, f_{ADC} = 72 MHz, sample rate=1.75Msps, V_{DDA} = 3.3V,T_A = 25 °C The measurement is performed after ADC calibration. V_{REF+}= V_{DDA}	±1.3	-	LSB
EO(4)	Offset error		±1	-	
ED	Differential linear error		±0.7	-	
EL	Integral linear error		±0.8	-	

Notes:

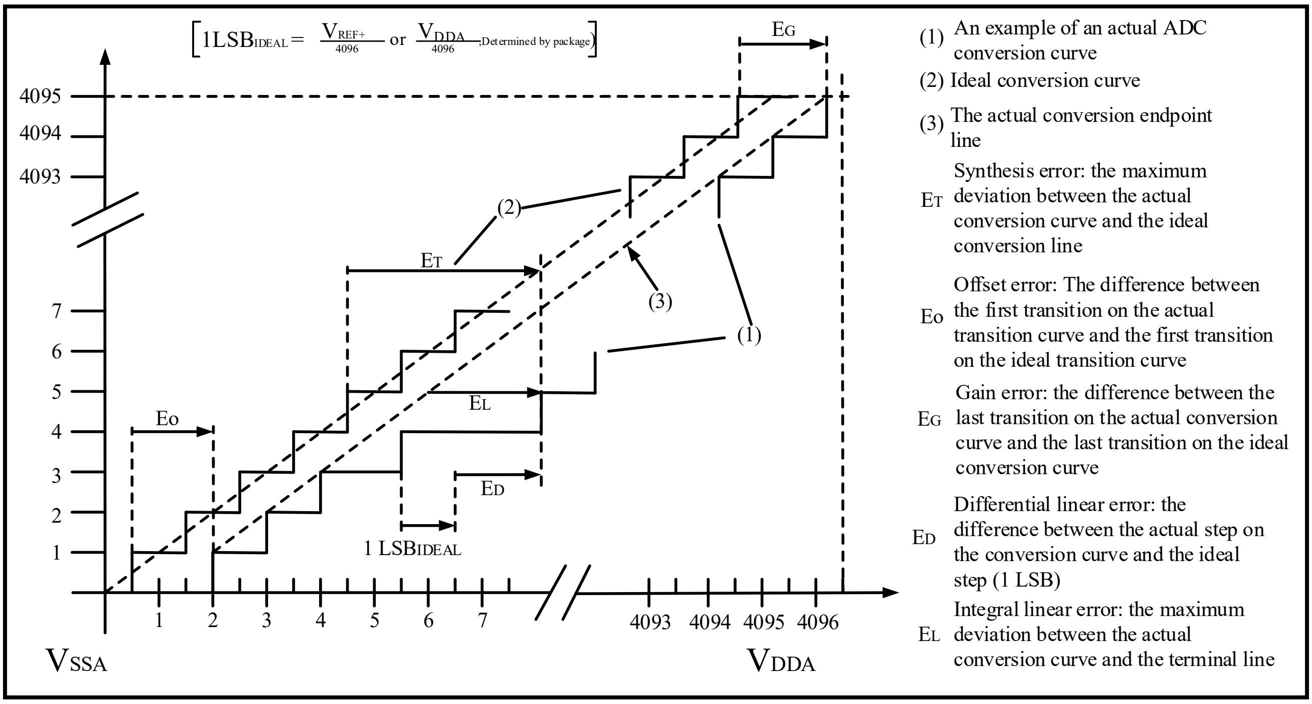
(1) The DC accuracy values of the ADC are measured after internal calibration.

(2) ADC Accuracy vs. Reverse Injection Current: Injecting reverse current on any standard analog input pin needs to be avoided, as this will significantly degrade the accuracy of an ongoing conversion on another analog input pin. It is recommended to add a Schottky diode (between the pin and ground) to standard analog pins where reverse injection current may occur.

(3) The forward injection current does not affect the ADC accuracy as long as it is within the range of $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ given in Section 4.3.12.

(4) Guaranteed by comprehensive evaluation, not tested in production.

Figure 4-24 ADC Precision Characteristics



(1) An example of an actual ADC conversion curve

(2) Ideal conversion curve

(3) The actual conversion endpoint line

ET Synthesis error: the maximum deviation between the actual conversion curve and the ideal conversion line

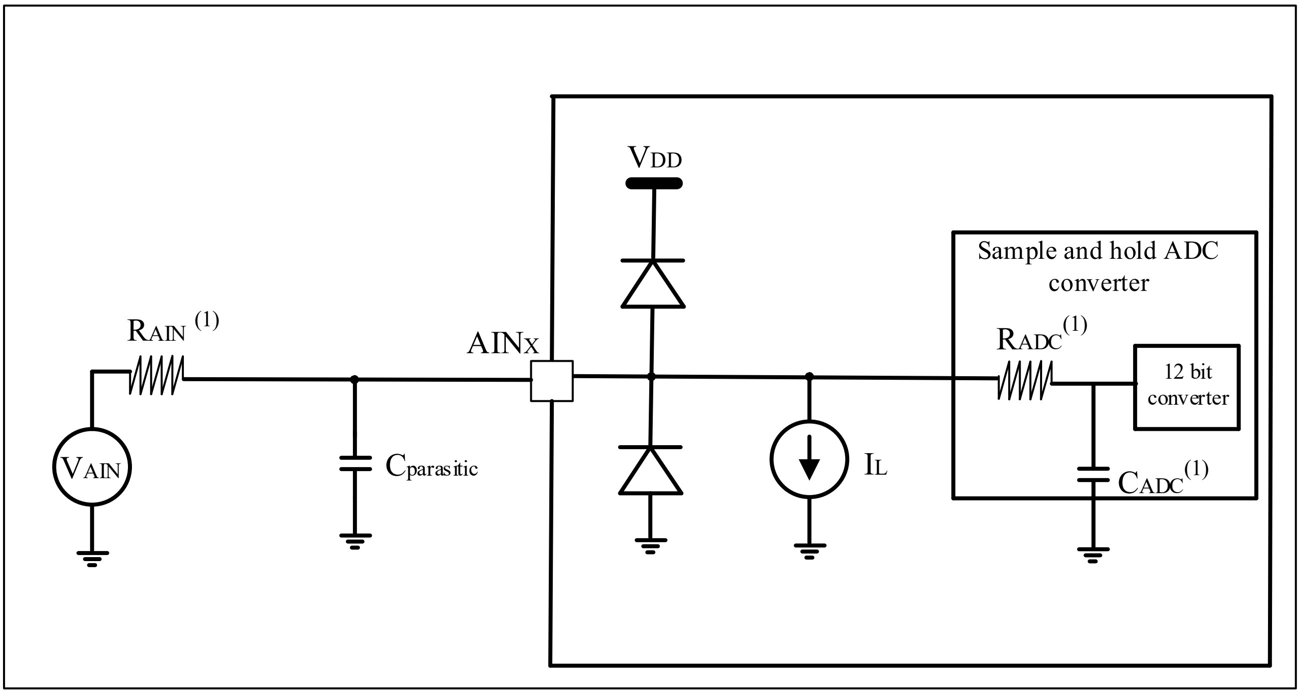
Eo Offset error: The difference between the first transition on the actual transition curve and the first transition on the ideal transition curve

EG Gain error: the difference between the last transition on the actual conversion curve and the last transition on the ideal conversion curve

ED Differential linear error: the difference between the actual step on the conversion curve and the ideal step (1 LSB)

EL Integral linear error: the maximum deviation between the actual conversion curve and the terminal line

Figure 4-25 Typical Connection Diagram Using ADC



Note:

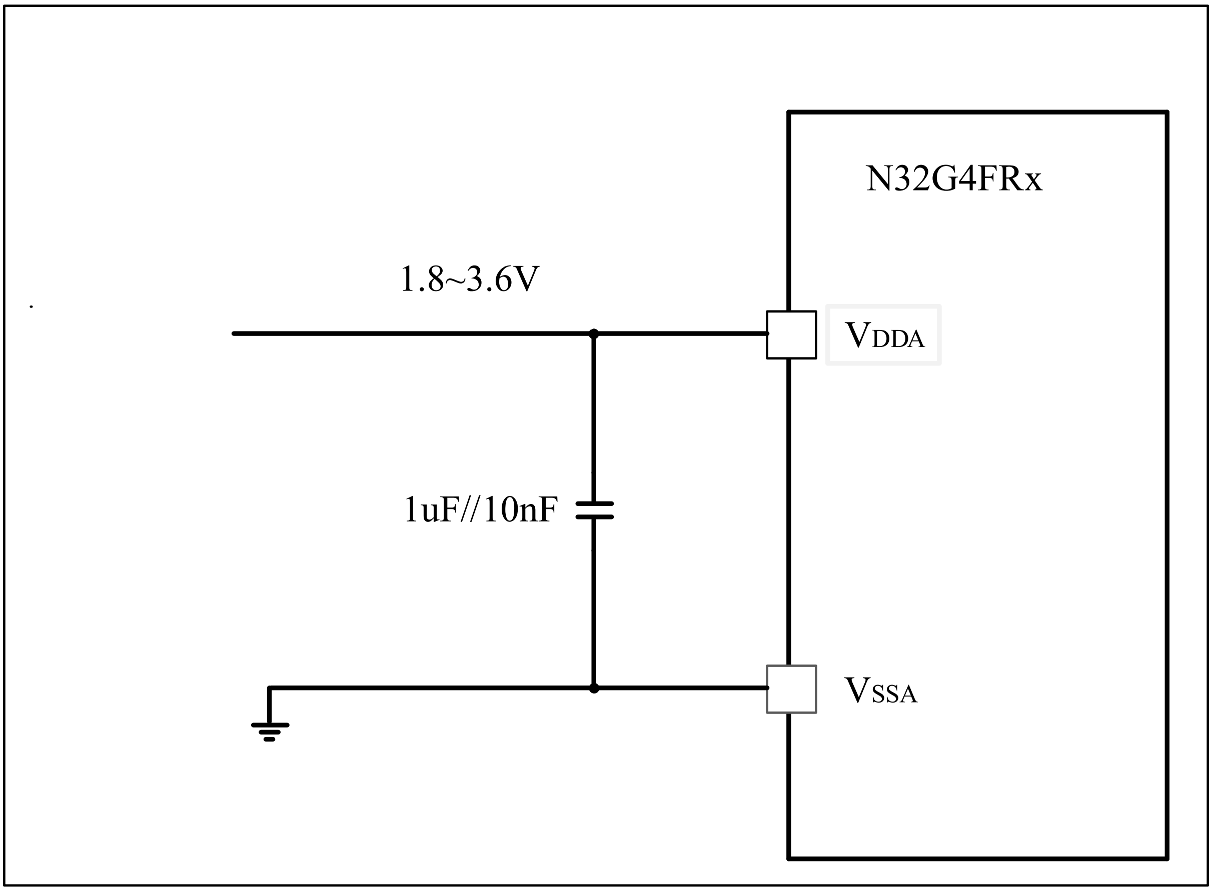
(1) On the numerical values of R_{AIN}, R_{ADC} and C_{ADC}, see Table 4-45.

Caution: ***$C_{parasitic}$ represents parasitic capacitance on PCB (related to soldering and PCB layout quality) and pads(approximately 7pF). A larger $C_{parasitic}$ value would reduce the accuracy of conversion, and the solution was to reduce f_{ADC}.***

PCB design suggestions

The decoupling of the power supply must be connected as shown in Figure 4-26. The 10nF capacitors in the picture must be ceramic capacitors (good quality), and they should be as close to the MCU chip as possible.

Figure 4-26 Decoupling Circuit of Power Supply and Reference Power Supply



4.3.23 12-bit digital-to-analog converter (DAC) Electrical Parameters

Unless otherwise specified, the parameters in Table 4-48 are measured using ambient temperature, fHCLK frequency, and VDDA supply voltage in accordance with the conditions in Table 4-4.

Table 4-48 DAC Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Annotate
V_{DDA}	Analog supply voltage	2.4	-	3.6	V	-
V_{DDD}	Digital supply voltage	1.0	1.1	1.2	V	-
V_{REF+}	Reference voltage	2.4	-	3.6	V	V_{REF+} must always be lower than V_{DDA}
V_{SSA}	Ground wire	0	-	0	V	-
R_L	Load resistance when buffer is open	5	-	-	KΩ	The minimum load resistance between DAC_OUT and V_{SSA}
C_L	Load Capacitance	-	-	50	pF	Maximum capacitance on DAC_OUT pin
DAC_OUT minimum	DAC_OUT voltage when buffer is open	0.2	-	-	V	The maximum DAC output span is given. When V_{REF+}=3.6V corresponds to a 12-bit input value 0x0E0~0xF1C， When V_{REF+}=2.4V corresponds to a 12-bit input value 0x155~0xEAB.
DAC_OUT maximum	DAC_OUT voltage when buffer is open	-	-	V_{REF+} - 0.2	V	
	DAC_OUT voltage when buffer is closed	-	-	V_{REF+}– 5LSB		
I_{DD}	In static mode (standby mode), DAC DC consumption (V_{DDD}+V_{DDA}+V_{REF+})	-	425	600	µA	No load, enter the median 0x800
		-	500	700		No load, enter the maximum value when V_{REF+}= 3.6V.
I_{DDQ}	DC consumption of DAC in power-down mode (V_{DDD}+V_{DDA}+V_{REF+})	-	5	350	nA	non-loaded

Symbol	Parameter	Min	Typ	Max	Unit	Annotate
	DC consumption of DAC in power-down mode (V_{DDA}+V_{REF+})	-	5	200		
DNL	Nonlinear distortion (deviation between two consecutive codes)	-	±0.5	-	LSB	DAC is configured with 10 bits (B1=B0=0 at all times)
		-	±2	-	LSB	DAC is configured with 12 bits
INL	Non-linearity accumulation (deviation between the measured value at code I and the line between code 0 and code 4095)	-	±6	-	LSB	DAC is configured as 12-bit
offset	Offset error (the deviation between the measured value of code 0x800 and the ideal value $V_{REF+}/2$)	-	±15	-	mV	DAC is configured as 12-bit
		-	±17	-	LSB	With V_{REF+}=3.6V, the DAC is configured with 12 bits.
Gain error	Gain error	-	±0.5	-	%	DAC is configured as 12-bit
$t_{SETTLING}$	Setting time (full range: 10-bit input code changes from minimum value to maximum value, and DAC_OUT reaches ±1 LSB of its final value)	-	5	7	µs	$C_{LOAD} \leq 50pF$ $R_{LOAD} \geq 5k\Omega$
Update rate	When the input code changes slightly (from the value i to i+1LSB), the maximum frequency of the correct DAC_OUT is obtained.	-	-	1	MS/s	$C_{LOAD} \leq 50pF$ $R_{LOAD} \geq 5k\Omega$
t_{WAKEUP}	Time to wake up from off state (setting the CHxEN bit in DAC control register)	-	6.5	10	µs	$C_{LOAD} \leq 50pF$,$R_{LOAD} \geq 5k\Omega$ The input code is between the minimum and maximum possible values.
PSRR+	Power supply rejection ratio (relative to V_{DD33A}) (static DC measurement)	-	-67	-40	dB	Without R_{LOAD},$C_{LOAD} \leq 50pF$

4.3.24 Temperature Sensor (TS) Characteristics

Unless otherwise specified, the parameters in Table 4-49 are measured using ambient temperature, f_{HCLK} frequency, and V_{DDA} supply voltage in accordance with the conditions in Table 4-4.

Table 4-49 Temperature Sensor Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_L(1)	Linearity of V_{SENSE} with respect to temperature	-	±1	±4	°C
Avg_Slope(1)	Average slope	-	-4.1	-	mV/°C
V_{30}(1)	Voltage at 30°C	-	1.32	-	V
t_{START}(1)	setting time	-	10	-	µs
$Ts_{\_temp}$(2)(3)	When reading temperature, ADC sampling time	8.3	-	-	µs

Notes:

(1) Guaranteed by comprehensive evaluation, not tested in production.

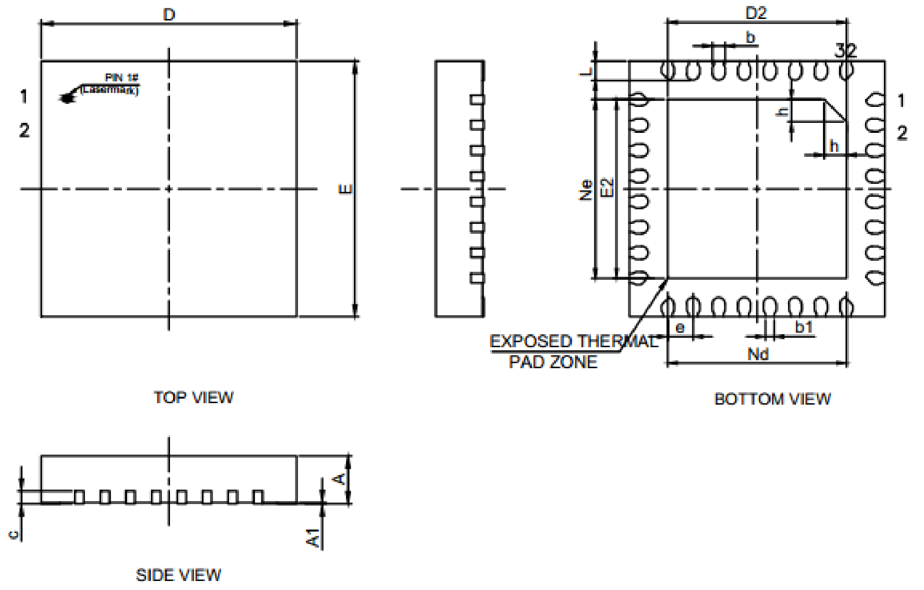
(2) Guaranteed by design, not tested in production.

(3) The shortest sampling time of can be determined by the application through multiple cycles.

5 Packages

5.1 QFN32 (4mm x 4mm)

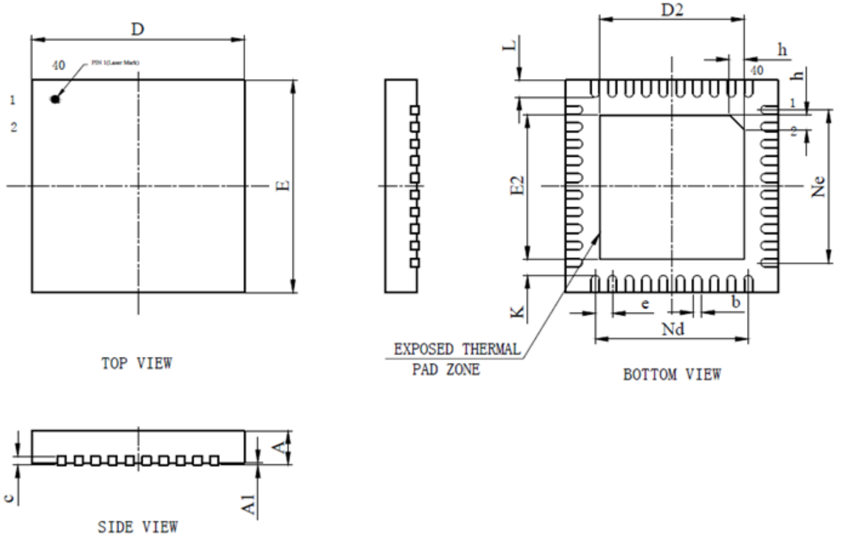
Figure 5-1 QFN32 (4mm x 4mm) Package Dimensions



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0	0.02	0.05
b	0.15	0.20	0.25
b1	0.14REF		
c	0.18	0.20	0.25
D	3.90	4.00	4.10
D2	2.70	2.80	2.90
e	0.40BSC		
Ne	2.80BSC		
Nd	2.80BSC		
E	3.90	4.00	4.10
E2	2.70	2.80	2.90
L	0.25	0.30	0.35
h	0.30	0.35	0.40

5.2 QFN40 (5mm x 5mm)

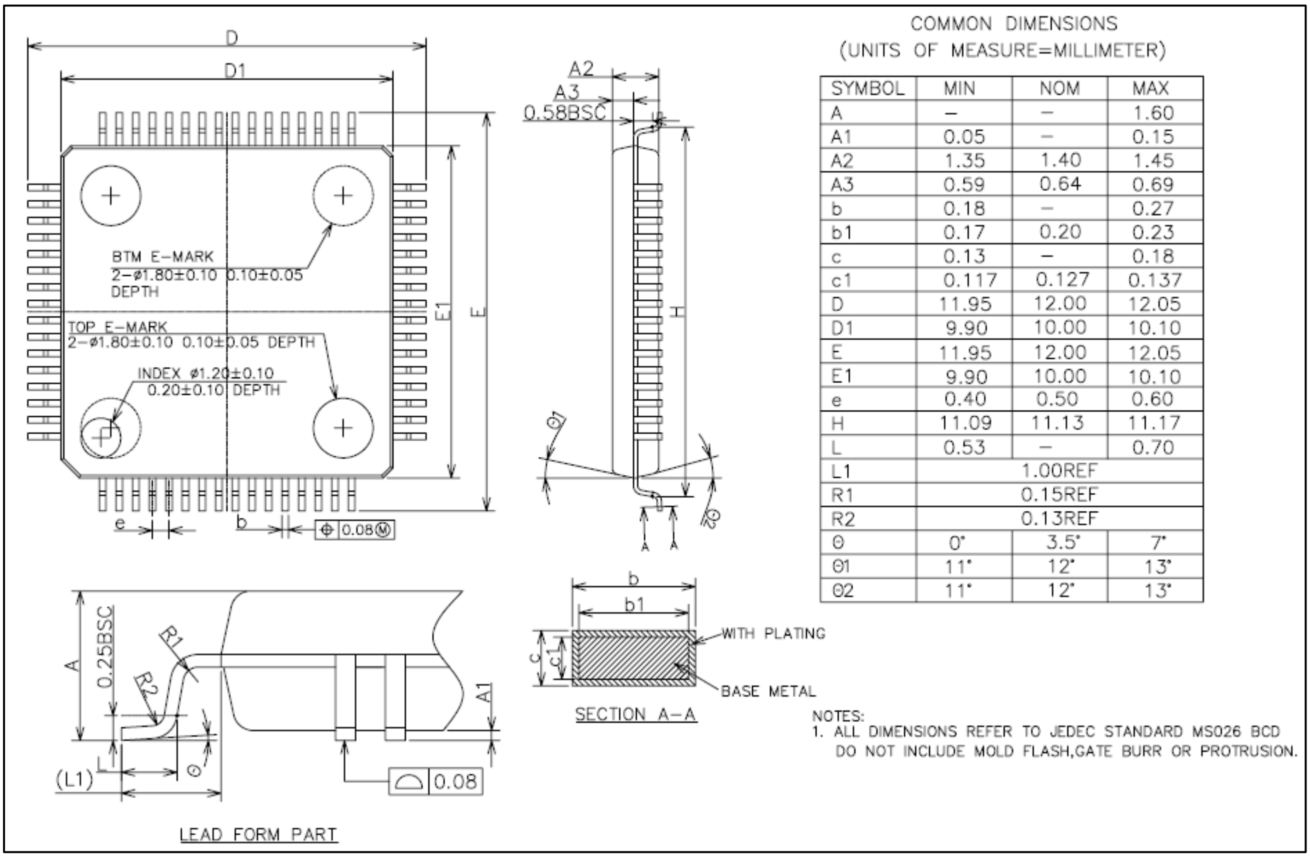
Figure 5-2 QFN40 (5mm x 5mm) package Dimensions



SYMBOL	MILLIMETER			
	MIN	NOM	MAX	
A	0. 70	0. 75	0. 80	
	0. 85	0. 90	0. 95	△3
A1	—	0. 02	0. 05	
b	0. 15	0. 20	0. 25	
c	0. 18	0. 20	0. 25	
D	4. 90	5. 00	5. 10	
D2	3. 30	3. 40	3. 50	
e	0. 40BSC			
Nd	3. 60BSC			
E	4. 90	5. 00	5. 10	
E2	3. 30	3. 40	3. 50	
Ne	3. 60BSC			
L	0. 35	0. 40	0. 45	
K	0. 20	--	--	
h	0. 30	0. 35	0. 40	
L/F Carrier size (mil)	150*150			

5.3 LQFP64 (10mm x 10mm)

Figure 5-3 LQFP64 (10mm x 10mm) Package Dimensions



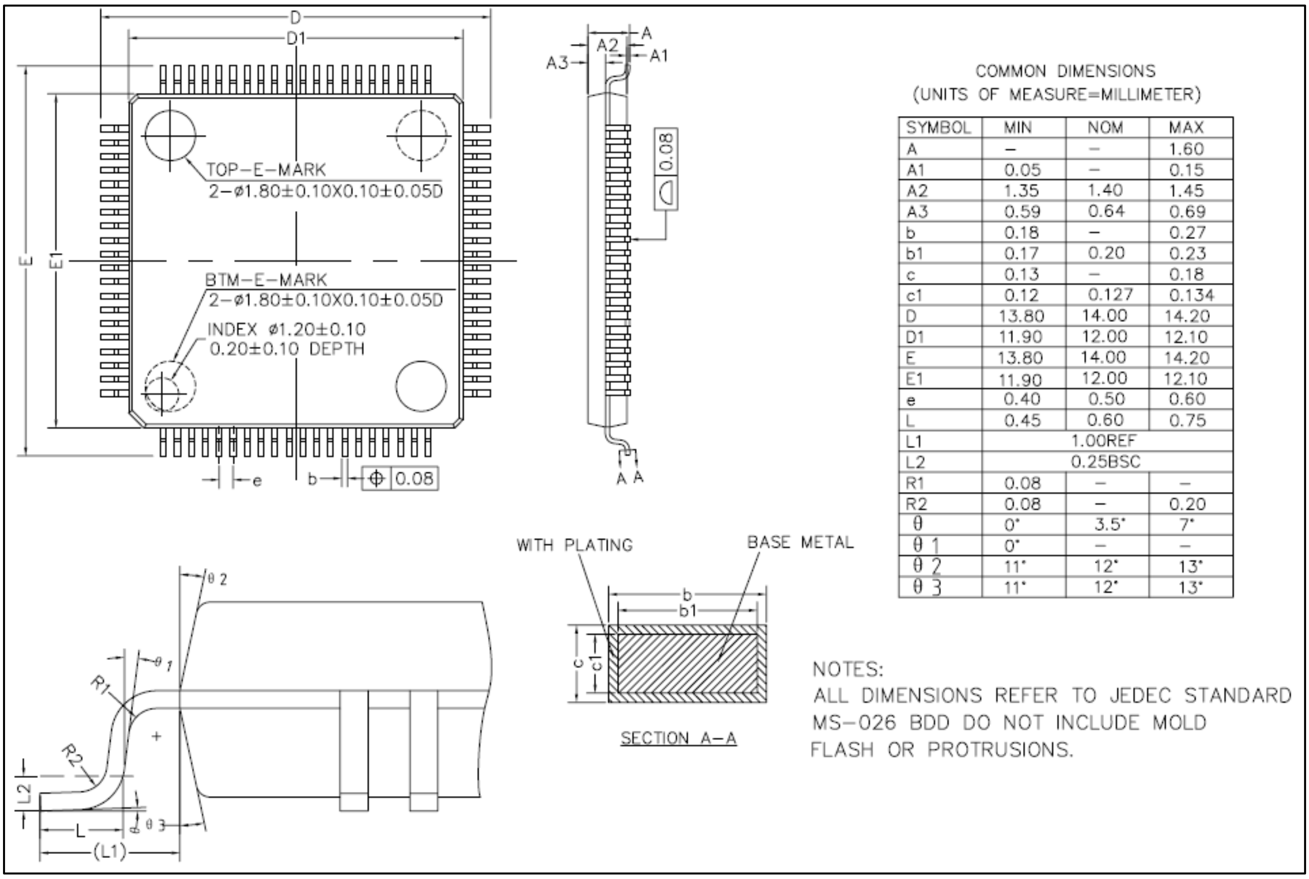
COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	–	–	1.60
A1	0.05	–	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	–	0.27
b1	0.17	0.20	0.23
c	0.13	–	0.18
c1	0.117	0.127	0.137
D	11.95	12.00	12.05
D1	9.90	10.00	10.10
E	11.95	12.00	12.05
E1	9.90	10.00	10.10
e	0.40	0.50	0.60
H	11.09	11.13	11.17
L	0.53	–	0.70
L1	1.00REF		
R1	0.15REF		
R2	0.13REF		
θ	0°	3.5°	7°
θ1	11°	12°	13°
θ2	11°	12°	13°

NOTES:
1. ALL DIMENSIONS REFER TO JEDEC STANDARD MS026 BCD DO NOT INCLUDE MOLD FLASH,GATE BURR OR PROTRUSION.

5.4 LQFP80 (12mm x 12mm)

Figure 5-4 LQFP80 (12mm x 12mm) Package Dimensions



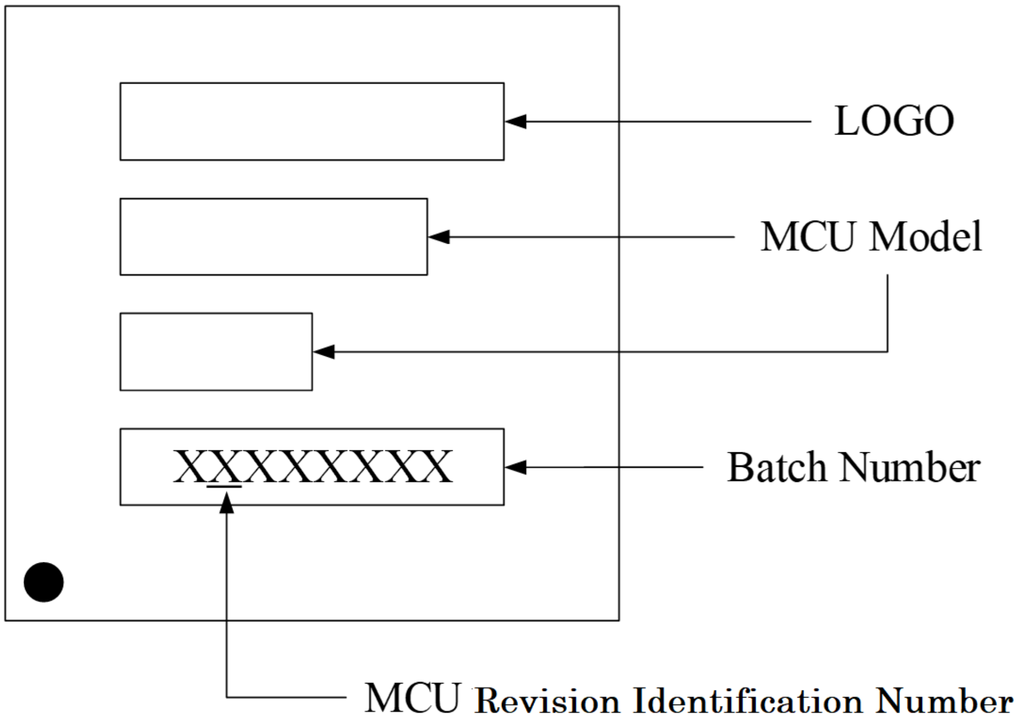
COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	–	–	1.60
A1	0.05	–	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	–	0.27
b1	0.17	0.20	0.23
c	0.13	–	0.18
c1	0.12	0.127	0.134
D	13.80	14.00	14.20
D1	11.90	12.00	12.10
E	13.80	14.00	14.20
E1	11.90	12.00	12.10
e	0.40	0.50	0.60
L	0.45	0.60	0.75
L1	1.00REF		
L2	0.25BSC		
R1	0.08	–	–
R2	0.08	–	0.20
θ	0°	3.5°	7°
θ 1	0°	–	–
θ 2	11°	12°	13°
θ 3	11°	12°	13°

NOTES:
ALL DIMENSIONS REFER TO JEDEC STANDARD MS-026 BDD DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.

5.5 Marking Information

Figure 5-5 Marking Information



6 Version History

Version	Date	Changes
V1.0	2020.4.18	Initial release
V1.1	2020.6.19	1. Modify the definition of pin multiplexing in Section 3.2 2. Modify some electrical characteristics in Chapter 4
V1.2	2020.9.16	1. Modify the DVP FIFO size in Section 2.26: 32 x 32bit to 8 x 32bit 2. Modified 4.1.6 power supply scheme 3. Modified some parameters in 4.2 Absolute Maximum Ratings 4. Modified 4.3.2 Operating conditions at power-up and power-down VDD rise rate minimum value 5. Modified 4.3.3 Embedded Reset and Power Control Module Features 6. Modified 4.3.5 Supply Current Characteristics f_{HCLK} frequency and f_{PCLK1}/f_{PCLK2} 7. Modified the LSI parameters of 4.3.7 Internal clock source characteristics 8. Modified 4.3.9 FLASH storage characteristic parameters 9. Modified 4.3.12 I/O port characteristics 10. Modified 4.3.13 NRST pin characteristics 11. Modified 4.3.14 TIM feature tCOUNTER parameter 12. Modified 4.3.16 SPI/I2S Interface Characteristics Figure 4-20 13. Modified 4.3.21 12-bit analog-to-digital converter (ADC) electrical parameters 14. Modified 4.3.22 DAC electrical parameters 15. Modified 4.3.24 Temperature sensor characteristics
V1.2.1	2020.11.27	1. Modify the schematic diagram of 3.1 package 2. Modify the memory map in Figure 2-1 3. Modify the supplementary description of the pin definitions in Table 3-1
V.1.2.2	2021.08.02	1. Modify the parameters related to the current characteristics 2. Modify the parameters related to embedded reset and power control module characteristics 3. Modify the typical and maximum current consumption related parameters in shutdown and standby mode 4. Modify the parameters related to the high-speed external user clock characteristics 5. Modify parameters related to low-speed external user clock characteristics

		6. Modify the parameters related to flash memory characteristics 7. Modify the parameters related to flash memory lifetime and data retention period 8. Modify the conditions related to the absolute maximum value of ESD 9. Modify I/O static characteristics related parameters 10. Modify the output voltage characteristic conditions, refer to the new drive capability table 11. Modify the parameters related to the input and output AC characteristics 12. Modify the parameters related to the input NRST pin characteristics 13. Modify the parameters related to the input I2C interface characteristics 14. Modify the parameters related to the input SPI1 characteristics 15. Modify the parameters related to the input SPI2 characteristics 16. Modify the parameters related to the input I2S characteristics 17. Modify the input I2S master mode timing diagram identification error 18. Modify the parameters related to the input QSPI characteristics 19. Modify the parameters related to the input SD/MMC interface characteristics 20. Modify the parameters related to the dynamic characteristics of the input DVP signal 21. Modify the input ADC characteristic conditions and related parameters 22. Modify the parameters related to the input DAC characteristics 23. Modify the parameters related to the input temperature sensor characteristics
V.1.2.2	2021.09.17	1. Modify the general working conditions related conditions 2. Remarks for increased electrical sensitivity 3. Added remarks for IO static features 4. Added remarks for output voltage characteristics 5. Added silkscreen instructions
V2.0.0	2021.10.22	1. Version change 2. Modify the description of I/O port characteristic conditions
V2.1	2022.05.23	1. Pin multiplexing defines the ADC pin to indicate whether it is a slow channel or a fast channel

		2. Added note on HSI oscillator characteristics 3. Modify the power-on time parameters of ADC characteristics 4. ADC characteristics indicate that the maximum sampling rate is 5MHz, only fast channel support 5. LSE oscillator feature to remove ESR CL limit 6. Update typical application using 32.768kH crystal 7. Modified resource Configuration description (The N32G4FRHC/E model supports only three I2C channels) 8. Update the input and output AC characteristics table 9. Updated recommended NRST pin protection diagram 10. Fixed TA conditions for static latch-up LU 11. Add Timer electrical characteristics section parameter table 12. Fixed SPI input clock duty cycle parameters 13. Modify the description of embedded RET-SRAM hold 14. CRC calculation time changed to 1 HCLK 15. Added STOP2 wake source: RTC intrusion, NRST reset, IWDG reset wake 16. Modified the RTC real-time clock output frequency from 512Hz to 256Hz 17. Modify the figure 4-4/4-3/4-5/4-6/4-17/4-25 18. Modify Table 4-7 Built-in reference voltage 19. Add Table 4-13/4-14 Bypass mode description 20. Modify The description in 4-15/4-17/4-18/4-20/4-50 21. Modified Table 4-17 Welding deviation notes 22. Modify Table 4-22 data retention period 23. Modify static locking test criteria 24. Modified Table 4-25 description and added the description of VIH/VIL 25. Modify The description in Table 4-29 26. Modify The description in Table 4-45 27. Modify The description in Table 4-47 28. Modify The description in Table 4-18 29. Add table 4-46 ADC sampling time 30. Modify the number of EXTI edge detectors to 21 31. Modify the IWDG prescaler to 3-bit 32. Modified reset description in Key features 33. Modify The description in Table 3-1

		34. Modified STOP0 mode description of the working mode of the main voltage regulator 35. Add DMA available peripheral QSPI
V2.2.0	2022.08.30	1. Modify the QFN32 package size diagram 2. Modify Table 4-34 I2C Interface Characteristics 3. Modify the parameters related to the input ADC characteristics 4. Modify the parameters related to the ADC sampling time

7 Disclaimer

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