Application Note

Low Power Application Note

Introduction

In the process of embedded product development, there are scenarios where battery usage is required. In these scenario, it is desirable for the battery to have a longer lifespan, so the low power settings are necessary.
This document mainly focus on the application of the Nsing MCU series products in the above scenarios, guiding users on how to use the MCU, and realize the control of battery power consumption by implementing the MCU into different low-power modes through the PWR module.

The N32G45x, N32G4FR, N32WB452 series integrate the latest generation of embedded ARM Cortex®-M4F processor, which enhances computational capabilities based on the Cortex®-M3 core, adds a floating-point unit (FPU), DSP and parallel computing instructions. Providing excellent performance of 1.25DMIPS/MHz. Its efficient signal processing capabilities combined with low power consumption, low cost, and ease of use of the Cortex-M series processors to meet the requirements that need a mix of control and signal processing capabilities while being user-friendly. The N32G45x, N32G4FR, N32WB452 feature five low-power operation modes (SLEEP mode, STOP0 mode, STOP2 mode, STANDBY mode, VBAT mode), and users should choose the optimal low-power mode according to factors such as power consumption, short startup time and available wake-up source.

This document is only applicable to Nsing MCU products. Currently, the supported product series include N32G45x series, N32G4FR series, N32WB452 series.

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Contents

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1 Low Power Operation Mode

1.1 SLEEP Mode

In SLEEP mode, only the CPU is stoped while all peripherals remain active and can wake up the CPU upon interrupt/event occurrence.

1.1.1 Entering SLEEP Mode

Entering SLEEP mode by executing the WFI (wait interrupt) or WFE (wait event) command and setting SLEEPDEEP = 0. Based on the value of the SLEEPONEXIT bit in the Cortex®-M4F system control register, there are two options available for selecting mechanism of entering the SLEEP mode:

- Sleep-now: If the SLEEPONEXIT bit is cleared, the WFI or WFE command will be executed immediately and the system will enter SLEEP mode immediately.
- Sleep-on-exit: If the SLEEPONEXIT bit is set to 1, the system will enter SLEEP mode immediately upon exiting the lowest-priority interrupt handler.

In SLEEP mode, all I/O pins maintain the same state/function as in run mode.

1.1.2 Exiting SLEEP Mode

If the WFI command is used to enter SLEEP mode, any peripheral interrupts handled by the nested vector interrupt controller (NVIC) can wake the device up from SLEEP mode.

If the WFE command is used to enter SLEEP mode, the device will immediately exit SLEEP mode upon the occurrence of an event. Wake-up events can be generated in the following ways:

- Enable an interrupt in the peripheral control register instead of in the NVIC, while also enabling the SEVONPEND bit in the Cortex®-M4F system control register. When the MCU resumes from WFE, the peripheral interrupt pending bit and the peripheral NVIC interrupt channel pending bit (in the NVIC Interrupt clear-pending register) must be cleared.
- Configure an external or internal EXTI event mode so that when the CPU resumes from WFE, the peripheral interrupt pending bit and the peripheral NVIC interrupt channel pending bit (in the NVIC Interrupt clear-pending register) do not need to be cleared because the pending bit corresponding to the event line is not set. This mode offers the shortest wake-up time since there is no time lost in interrupt entry or exit.

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1.2 STOP0 Mode

The STOP0 mode is based on the Cortex®-M4F deep sleep mode, combined with the peripheral clock control mechanism. The voltage regulator can be configured in normal or low power mode. In STOP0 mode, most clock sources in the core domainare disabled, such as PLL, HSI, and HSE. However, SRAM, RET-SRAM, and all register contents are perserved. In STOP0 mode, all I/O pins maintain the same state as in run mode.

1.2.1 Entering STOP0 Mode

When entering STOP0 mode, the main differences are setting SLEEPDEEP= 1 and PDS=0.Another difference is that MR can operate in normal mode or low power mode by configuring the PWR_CTRL bit LPS. When LPS = 1, MR operates in low power mode. When LPS = 0, MR operates in normal mode. In STOP0 mode, all I/O pins maintain the same state and function as in run mode. If Flash operations are in progress, the entry into STOP0 mode will be delayed until memory access is completed. If access to the APB area is in progress, the entry into STOP0 mode will be delayed until the APB access is completed. In STOP0 mode, the following features can be selected by programming the individual control bits:

- Independent watchdog (IWDG): the independent watchdog is started upon software writing to its associated register or hardware operation. Once started, it operates until a reset message is generated
- RTC: this can be enabled by configuring the RTCEN bit in register RCC_BDCTRL
- Internal RC oscillator (LSI RC): can be enabled by configuring the LSIEN bit in register RCC_CTRLSTS
- External 32.768khz crystal oscillator (LSE OSC): can be enabled by configuring the LSEEN bit in register RCC_BDCTRL
- ADC or DAC can also consume power in STOP0 mode. ADC and DAC can be disabled before entering STOP0 mode.

Note: if the application needs to disable the external clock before entering stop mode, the HSEEN bit must be disabled first, and then the system clock should be switched to HSI. Otherwise, if the HSEEN bit remains enabled when entering stop mode and the external clock (external oscillator) is removed, the Clock Safety System (CSS) feature must be enabled to detect any external oscillator failure and avoid failure behavior when entering stop mode.

1.2.2 Exiting STOP0 Mode

When exiting STOP0 mode due to an interrupt or wake-up event, the HSI RC oscillator is selected as the system clock.

When the voltage regulator operates in low power mode, there is an additional startup delay when awakened from STOP0 mode. In STOP0 mode, setting the internal regulator to normal mode can reduce the startup time, but will result in increased power consumption.

1.3 STOP2 Mode

STOP2 mode is based on the Cortex®-M4F deep sleep mode, and all the core digital logic domain are powered off. The main voltage regulator (MR) is switched off, HSE/HSI/PLL is switched off. The CPU registers are maintained, LSE/LSI can be configured, GPIOs are remained, and peripheral I/O multiplexing is not maintained.The 16K bytes of RET-SRAM are maintained, while data in other SRAM and registers are lost.The 84-byte backup register are maintained. GPIO and

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EXTI are enabled.

1.3.1 Entering STOP2 Mode

When entering STOP2 mode, the main differences are setting SLEEPDEEP= 1, PWR_CTRL2.STOP2S =1, PWR_CTRL bit PDS=0, LPS=0.

In STOP2 mode, if Flash operations are in progress, the entry into STOP2 mode will be delayed until memory access is completed.

If access to the APB area is in progress, the entry into STOP2 mode will be delayed until the APB access is completed.

In STOP2 mode, the following features can be selected by programming the individual control bits:

- Independent watchdog: the independent watchdog is started upon software writing to its associated register or hardware operation. Once started, it operates until a reset message is generated
- RTC: this can be enabled by configuring the RTCEN bit in register RCC_BDCTRL
- Internal RC oscillator (LSI RC): can be enabled by configuring the LSIEN bit in register RCC_CTRLSTS
- External 32.768khz crystal oscillator (LSE OSC): can be enabled by configuring the LSEEN bit in register RCC_BDCTRL

Note: if you want to preserve data (global variables, stacks, etc.) in STOP2 mode, the data should be placed in R-SRAM.

1.3.2 Exiting STOP2 Mode

When exiting STOP2 mode by issuing interrupt or wake up events, the HSI RC oscillator is as the system clock. Upon exiting STOP2 mode, the code resumes execution from the stopped position..

1.4 STANDBY Mode

The STANDBY mode can achieve lower power consumption as it is based on the Cortex®-M4F deep sleep mode. The core domain is completely shut down while the backup domain is powered on to supply the VDD and BKR.

1.4.1 Entering STANDBY Mode

When entering STANDBY mode, the main differences are setting SLEEPDEEP= 1, PDS=1.

In STANDBY mode, all I/O pins maintain the high resistance state except NRST, PA0_WKUP, PC13_TAMPER, PC14, and PC15.

If Flash operations are in progress, the entry into STANDBY mode will be delayed until the memory access is completed.

If access to the APB area is in progress, the entry into STANDBY mode will be delayed until the APB access is completed.

In STANDBY mode, the following features can be selected by programming the individual control bits：

- Independent watchdog: the independent watchdog is started during software writing or hardware operation of its related registers, Once started, it operates until a reset message is generated.

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- RTC: this can be enabled by configuring the RTCEN bit in register RCC_BDCTRL
- Internal RC oscillator (LSI RC): can be enabled by configuring the LSIEN bit in register RCC_CTRLSTS
- External 32.768khz crystal oscillator (LSE OSC): can be enabled by configuring the LSEEN bit in register RCC_BDCTRL
- R-SRAM data retention can be enabled by configuring the SR2STBRET bit in register PWR_CTRL2

1.4.2 Exiting STANDBY Mode

The device exits STANDBY mode when an external reset (NRST pin), IWDG reset, rising edge on the WKUP pin, or rising edge of an RTC alarm event occurs. All registers except for the power control status register (PWR_CTRLSTS) will be reset upon waking up from the STANDBY state.

Upon waking up from STANDBY mode, the code execution is equivalent to that after a reset (boot pins are triggered, reset vectors are read, and so on).The SBF status flag in the power control status register (PWR_CTRLSTS) indicates that the MCU has exited from STANDBY mode.

1.5 VBAT Mode

In VBAT mode the CPU is switched off, all peripherals are switched off, the main voltage regulator is switched off, LSE/LSI can be configured, HSE/HSI/PLL is switched off. Except for NRST/ PC13-TAMper /PC14-OSC32_IN/PC15-OSC32_OUT, most I/O ports are in high resistance state.

In VBAT mode, based on the configuration before VDD power-down, the following features can be used :

- RTC: this can be enabled by configuring the RTCEN bit in register RCC_BDCTRL
- Internal RC oscillator (LSI RC): can be enabled by configuring the LSIEN bit in register RCC_CTRLSTS
- External 32.768khz crystal oscillator (LSE OSC): can be enabled by configuring the LSEEN bit in register RCC_BDCTRL
- R-SRAM data retention can be enabled by configuring the SR2VBRET bit in register PWR_CTRL2

1.5.1 Entering VBAT Mode

When the VDD is powered off, it enters VBAT mode at any time.

1.5.2 Exiting VBAT Mode

When the VDD is restored to the power-on reset threshold, the device exits the VBAT mode. Upon the VDD is restored, the device core domain will execute in the same order as power-on. Upon waking up from VBAT mode, code execution is equivalent to reset execution. The VBATF status flag in the power control status register (PWR_CTRLSTS) indicates that the MCU exits from VBAT mode.

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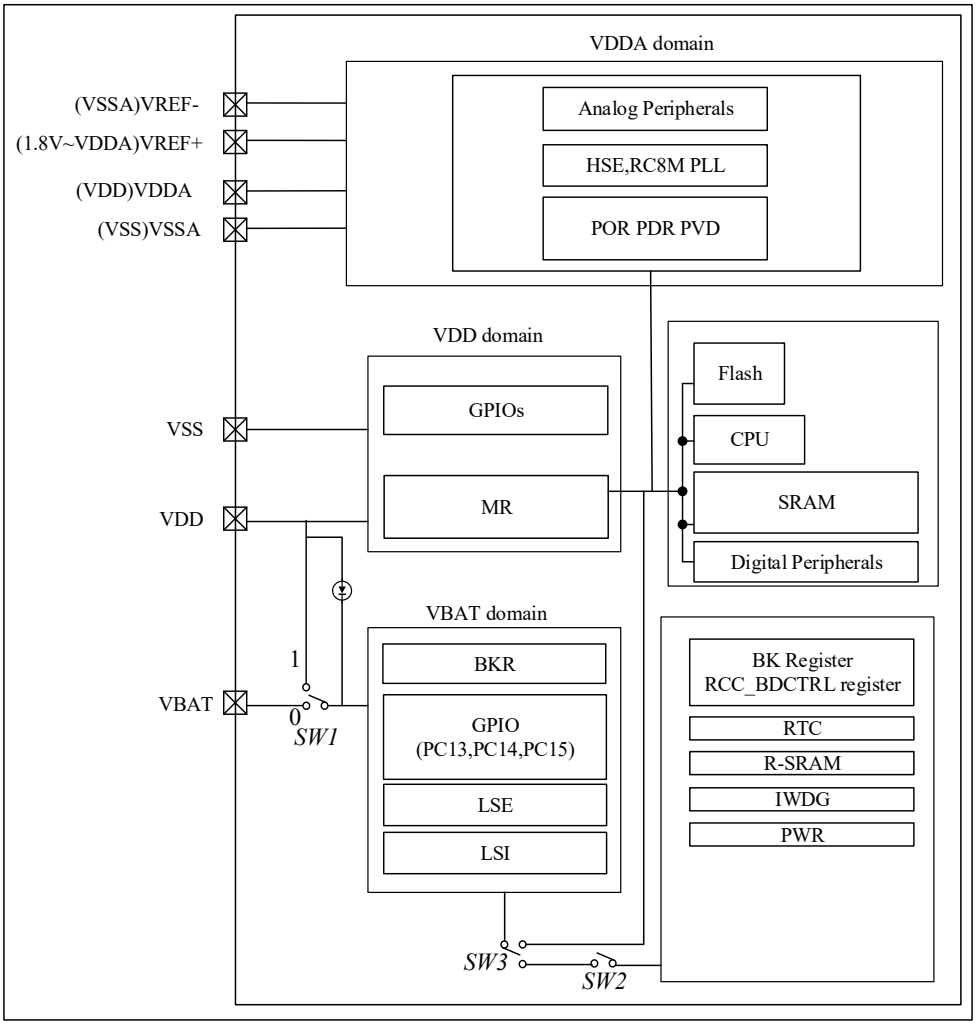
2 Power Control (PWR)

2.1 Power System Introduction

The operating voltage of N32G45x, N32G4FR, N32WB452 (VDD) are 1.8V~3.6V.It mainly has 3 analog/digital power domains (VDD, VBAT, VDDA). Refer to Figure 2-1 for the power diagram.

The PWR module, serving as the power control module of the whole device, the main function of the PWR is to control the device into different power modes and can be woken up by other events or interruptions. The N32G45x, N32G4FR, and N32WB452 support RUN, SLEEP, STOP0, STOP2, STANDBY, and VBAT modes.

Figure 2-1 Power Block



2.1.1 Power Supply

In order to illustrate the functions of different power domains, some power domains are described below. The digital parts of the power domains are described in later chapters of this document.

- VDD domain: the input voltage ranges from 1.8V to 3.6V, mainly providing power input for the MR and supplying

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power to the CPU, AHB, APB, SRAM, FLASH and most of the digital peripheral interface power.

- VBAT domain: the input voltage ranges from 1.8V to 3.6V, supplying power to BKR and some special IO ports (PC13, PC14, PC15).When the VDD is powered off, the switch transfers the power supply system VDD to VBAT.
- VDDA domain: the input voltage ranges from 1.8V to 3.6V, mainly supplying power to the clock and reset systems, as well as most analog peripherals.

2.1.1.1 Digital module power supply system

The VDD and VBAT input voltages of N32G45x, N32G4FR and N32WB452 range from 1.8V to 3.6V. The BKR and MR are internal voltage regulators that can supply power to the digital module power supply system. VDD and VBAT are powered directly by external power supply. VBAT is powered by batteries to maintain the contents of the backup area, while VDD is powered by other external power supply systems. In addition, if the battery is not needed, the VBAT must be directly connected to the VDD.

- MR(RUN,SLEEP,STOP0)

The MR is the internal main power controller, mainly used in RUN mode, SLEEP mode and STOP0 mode.MR has two modes, normal mode and low power mode, the low power mode is used for STOP0 to further reduce power consumption.

When the MR enters low power mode, the CPU enters a deep sleep state. In this case, the PWR_CTRL.PDS bit should be set to 0, and the LPS bit should be set to 1.When the MR enters normal mode, the PWR_CTRL.PDS bit should be set to 0, and the LPS bit should also be set to 0.

- BKR(STOP2,STANDBY,VBAT)

The BKR is the internal backup domain power controller and is used in STOP2, STANDBY, and VBAT modes. In STOP2 mode, the CPU state is maintained, and the digital backup area, GPIO and EXTI are additionally powered. When the CPU enters a deep sleep state, the PWR_CTRL2.STOP2S bit should be set to 1.

The main modules in the digital backup area include PWR, IO (PA0_WAKUP, PC13_TAMPER, PC14, PC15), RET-SRAM, TSC, RTC, BKR, and RCC_BDCTRL registers. When SW3 is switched on, the CPU will enters a deep sleep. When SW1 switches the power supply system to VBAT, it indicates that VDD has been powered off.

2.1.2 Backup Power Domain

During the reset, SW1 switches the power supply system to the VDD power domain. In STOP2, STANDBY and VBAT modes, the internal voltage regulator BKR will supply power to the digital backup area.

Note:

- The switch between VBAT and VDD remains connected to the VBAT domain during rising phase of VDD or when PDR is detected.
- During the startup phase, if the VDD is quickly established and VDD > VBAT + 0.6V, current can be injected into the VBAT via an internal diode connection. If the power supply or battery connected to VBAT does not support this current injection. It is strongly recommended to place a low voltage diode between the power supply and the VBAT pin.

If there is no external battery in the application, it is recommended to connect the VBAT pins to the VDD with a 100nF ceramic capacitor. In RUN, SLEEP, and STOP0 modes, the backup area is powered by the VDD (SW1 is connected to the

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VDD). The following functions are available:

- PC14 and PC15 can be used for normal IO ports or LSE pins
- PC13 can be used for common IO ports, TAMPER pins, RTC parity clock pins, RTC alarm clocks and second outputs

Notes:

1) *As the current flowing through SW1 and SW2 is limited to a maximum of 3mA, the IO output modes of PA0_WAKUP, PC13 to PC15 are restricted. When an external 30pF capacitor is connected, the maximum output speed is 2MHz.In addition, these IO cannot be used for current driving, such as driving LEDs. The current of SW2 will be maintained at 3mA or lower because GPIO and EXTI operate together to consume current.*

When VBAT supplies power for the backup area, the following functions can be used:

- PC14 and PC15 can only be used for LSE pins
- PC13 is used for TAMPER pins, RTC alarm clocks, or second outputs

2.2 Supply Current Characteristic

2.2.1 General Operating Conditions

Table 2-1 General Operating Conditions

Symbol	Parameter	Condition	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency	-	0	144	MHz
f_{PCLK1}	Internal APB1 clock frequency	-	0	36	
f_{PCLK2}	Internal APB2 clock frequency	-	0	72	
V_{DD}	Standard operating voltage	-	1.8	3.6	V
V_{DDA}	Analog operating voltage	Must be the same as V_{DD}(1)	1.8	3.6	V
V_{BAT}	Backup operating voltage	-	1.8	3.6	V
T_A	Ambient temperature (Temperature label 7)	Maximum power consumption	- 40	105	℃
		Low power consumption(3)	- 40	125	
T_J	Junction temperature range	Temperature label 7	- 40	125	℃

Notes:

1) *It is recommended power VDD and VDDA with the same power supply, during power up and normal operation, a maximum difference of 300mV is allowed between VDD and VDDA.*

2) *If T_A lower, as long as T_J no more than $T_J$max, a higher PD value is allowed.*

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3) At lower power dissipation, as long as T_J no more than $T_J$max, T_A it can be extended to this scope.

4) The above are the operating conditions of N32G457 series.

Current consumption is a comprehensive indicator influenced by various parameters and factors, including operating voltage, ambient temperature, I/O pin load, product software configuration, operating frequency, I/O pin toggle rate, program location in memory, and executed code, among others..

Current consumption measurement method description, refer to Table 2-1.

All of the current consumption measurements given in this section are performed in a simplified set of code that is equivalent to the Dhrystone 2.1 code.

2.2.2 Maximum Current Consumption

The microcontroller is under the following conditions:

- All I/O pins are in input mode and connected to a static level V_{DD} or V_{SS}(No load).
- All peripherals in the disabled state unless otherwise noted.
- The access time of the Flash memory is adjusted to F_{HCLK}(0 wait cycles for 0-32MHz, 1 wait cycle for 32-64MHz, 2 wait cycles for 64-96MHz, 3 wait cycles for 96-128MHz, and 4 wait cycles for 128-144MHz).
- Instruction prefetch is enabled (note: this parameter must be set before setting the clock and bus divider).
- When the peripheral is enabled: $f_{PCLK1} = f_{HCLK}/4$, $f_{PCLK2} = f_{HCLK}/2$.

The parameters given in Table 2-2 and Table 2-3 are based on tests at ambient temperature and VDD supply voltage listed in Table 2-1.

Table 2-2 Maximum Current Consumption in RUN Mode, Data Processing Code Is Run From Internal Flash

Symbol	Parameter	Condition	f_{HCLK}	Max (1)	Unit
				T_A = 105 ℃	
I_{DD}	Supply current in RUN mode	External clock(2). Enable all peripherals	144MHz	32	mA
			72MHz	18	
			36MHz	11	
		External clock(2). Disable all peripherals	144MHz	15.8	
			72MHz	9.7	
			36MHz	6.7	

Notes:

1) Derived from comprehensive evaluation and not tested in production.

2) The external clock is 8MHz, PLL is enabled when f_{HCLK} >8MHz.

3) The above are the working conditions of N32G457 series.

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Table 2-3 Maximum Current Consumption in SLEEP Mode, Code Running in Flash Or RAM

Symbol	Parameter	Condition	f_{HCLK}	Max (1)	Unit
				T_A = 105 ℃	
I_{DD}	Supply current in SLEEP mode	External clock(2). Enable all peripherals	144MHz	27	mA
			72MHz	15.5	
			36MHz	10	
		External clock(2). Disable all peripherals	144MHz	9.2	
			72MHz	6.6	
			36MHz	5.1	

Notes:

1) *Derived from comprehensive evaluation, testing during production is conducted under the conditions of VDDmax and $f_{HCLKmax}$ with enabling peripheral.*

2) *The external clock is 8MHz, PLL is enabled when f_{HCLK} >8MHz.*

3) *The above are the working conditions of N32G457 series.*

Table 2-4 Typical And Maximum Current Consumption in Shutdown And Standby Mode

Symbol	Parameter	Condition	Typical (1)	Max	Unit
			T_A=25℃	T_A =105℃	
I_{DD}	Supply current in STOP0 mode	The regulator is in operation mode with low and high speed internal RC oscillators and high speed oscillators off (no independent watchdog)	300	1200	uA
		The regulator is in low power mode with low and high speed internal RC oscillators and high speed oscillators off (no independent watchdog)	150	800	
	Supply current in STOP2 mode	The external low speed clock is on, RTC is running, R-SRAM is on, all I/O states are on, and the independent watchdog is off	10	100	
	Supply current in STANDBY mode	Low speed internal RC oscillator and independent watchdog are on	3	40	
		The low speed internal RC oscillator is on	2.9	40	

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		and the independent watchdog is off			
		The low speed internal RC oscillator and independent watchdog are closed, and the low speed oscillator and RTC are closed	2.7	3.5	
I_{DD_VBAT}	Backup domain(VBAT) supply current	The low speed oscillator and RTC are on	2	15	

Note:

1. *The typical value is tested at V_{DD}/V_{BAT}= 3.3V.*
2. *Derived from comprehensive evaluation and not tested in production.*
3. *The above are the working conditions of N32G457 series.*

2.2.3 Typical Current Consumption

MCU is under the following conditions:

- All I/O pins are in input mode and connected to a static level -- V_{DD} or V_{SS}(No load).
- All peripherals are in the disabled state unless otherwise noted.
- The access time of the Flash memory is adjusted to F_{HCLK}(0 wait cycles for 0-32MHz, 1 wait cycle for 32-64MHz, 2 wait cycles for 64-96MHz, 3 wait cycles for 96-128MHz, and 4 wait cycles for 128-144MHz).
- Ambient temperature and the supply voltage conditions of VDD are listed in Table 2-1.
- Instruction prefetch is enabled (note: this parameter must be set before setting the clock and bus divider). When the peripheral is switched on: $f_{PCLK1}= f_{HCLK}/4$, $f_{PCLK2} = f_{HCLK}/2$, $f_{ADCCLK} = f_{PCLK2}/4$.

Table 2-5 Typical Current Consumption in RUN Mode, Data Processing Code Is Run From Internal Flash

Symbol	Parameter	Conditions	f_{HCLK}	Typical Values(1)		Unit
				Enable All Peripherals(2)	Disable All Peripherals	
I_{DD}	Supply current in RUN mode	External clock(3)	144MHz	30.3	14.2	mA
			72MHz	17	8.1	
			36MHz	9.3	5.3	
		Run on high speed internal RC oscillator (HSI), using AHB predivision to reduce frequency	128MHz	30	12.7	mA
			72MHz	22.5	7.2	
			36MHz	8.8	3.9	

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Notes:

1) The typical value is tested at T_A= 25 ℃, V_{DD}=3.3V.

2) An additional 0.8mA of current consumption is added to each analog portion of the ADC. In the application environment, this part of the current is increased only when the ADC is enabled (setting the ON bit of the ADC_CTRL2 register).

3) The external clock is 8MHz, PLL is enabled when f_{HCLK} >8MHz.

4) *The above are the working conditions of N32G457 series.*

Table 2-6 Typical Current Consumption in SLEEP Mode, With Data Processing Code Running From Internal Flash Or RAM

Symbol	Parameter	Conditions	f_{HCLK}	Typical Values(1)		Unit
				Enable All Peripherals(2)	Close All Peripherals	
I_{DD}	Supply current in SLEEP mode	External clock(3)	144MHz	25.3	8	mA
			72MHz	13.9	5.3	
			36MHz	8	3.6	
		Run on high speed internal RC oscillator (HSI), using AHB predivision to reduce frequency	128MHz	24.2	6.1	mA
			72MHz	13.9	3.5	
			36MHz	7.2	2.2	

Notes:

1) The typical value is tested at T_A= 25 ℃, V_{DD}=3.3V.

2) An additional 0.8mA of current consumption is added to each analog portion of the ADC. In the application environment, this part of the current is increased only when the ADC is enabled (setting the ON bit of the ADC_CTRL2 register).

3) The external clock is 8MHz, PLL is enabled when f_{HCLK} >8MHz.

4) The above are the working conditions of N32G457 series.

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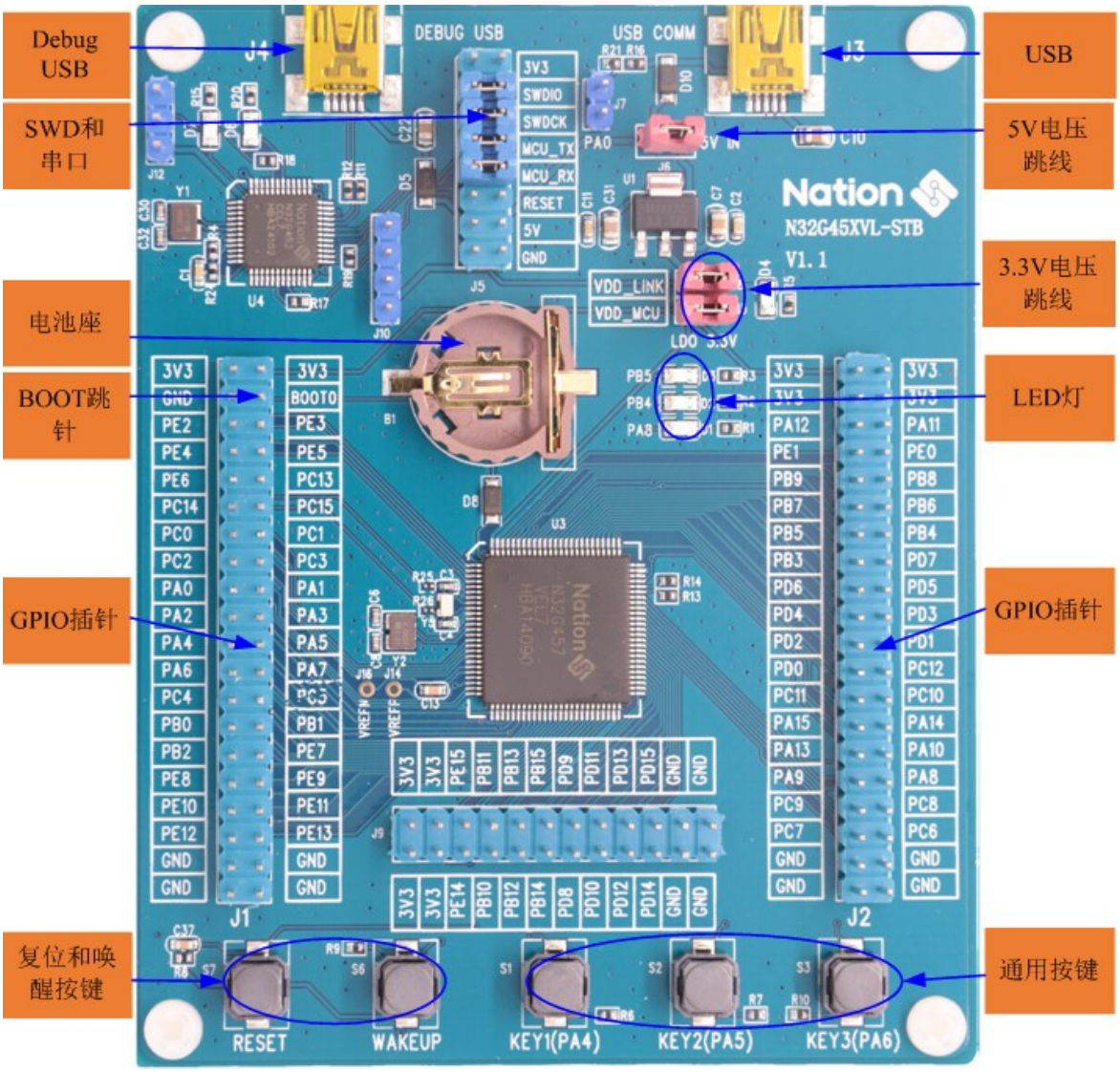
3 Hardware Environment

3.1 Development Board Layout

Figure 3-1 Development Board Layout



1) Power supply for development board

The development board can be powered by USB interface (J3) and Debug USB (J4), connected to 3.3V LDO input port through J6 jumper.

2) USB port (J3)

Mini USB interface (J3), connected to MCU DP DM, can be used for USB interface communication.

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3) Debug USB (J4)

The MCU can be used to download programs through the Debug USB or as a serial port.

4) SWD Interface (J5)

SWD interface can also be used for program download debugging, using ULINK2 or JLINK to download programs to the chip. You can also use the jumper to short SWDIO and SWDCK, and use the Debug USB to download programs.

5) Reset and wake up buttons (S7, S6)

S7 and S6 are reset buttons and wake buttons respectively, which are connected to NRST pins and PA0-WKUP pins of the chip respectively for chip reset and wake functions.

6) Universal keys (S1, S2, S3)

S1, S2 and S3 are respectively connected to PA4, PA5 and PA6 pins of the chip.

7) Battery holder (BAT)

A CR1220 battery can be placed in the battery holder, which is connected to the chip VBAT pin to provide power.

8) GPIO port (J1, J2)

All the GPIO interfaces of the chip are elicited, and 3.3V voltage and GND pins are reserved on the pins for easy testing. Refer to N32G45x Series Data Manual, DS_N32G4FR Series Data Manual, DS_N32WB452 Series Data Manual for the specific definition of the interface.

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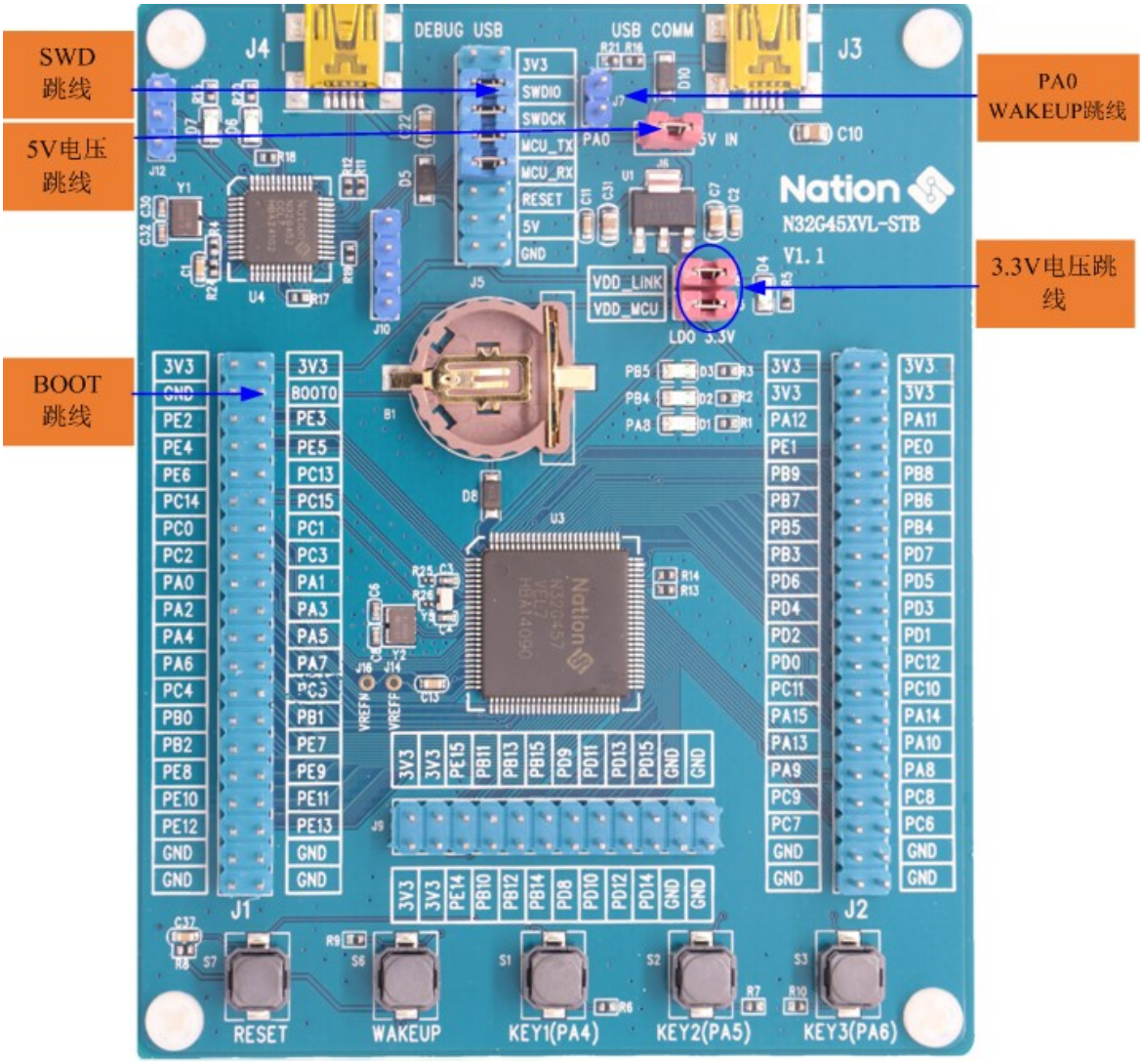
3.2 Development Board Jumper Instructions

Figure 3-2 Development Board Jumper Description



Jumper descriptions are as follows:

No.	Jump Line Item Number	Jump Line Function	Directions
1	J6	5V voltage jumper	The J6 jumper connects the J3 and J4 USB ports and supplies power to the LDO3.3V input port.
2	J8 and J15	3.3V power supply jumper	J8: Supply 3.3V power to NS-LINK MCU chip. J15: Supply 3.3V power to main MCU chip.
3	J5	SWD jumper, Serial jumper	Use NS-LINK to download program to MCU through USB Debug port, need to short SWDIO and SWDCK pin.

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			When using NS-LINK as a serial port through the USB Debug port, the two pins MCU_TX and MCU_RX need to be short-circuited.

3.3 Development Board Schematic Diagram

N32G45XML-STB Development board schematic refer to N32G45XVL-STB_V1.1

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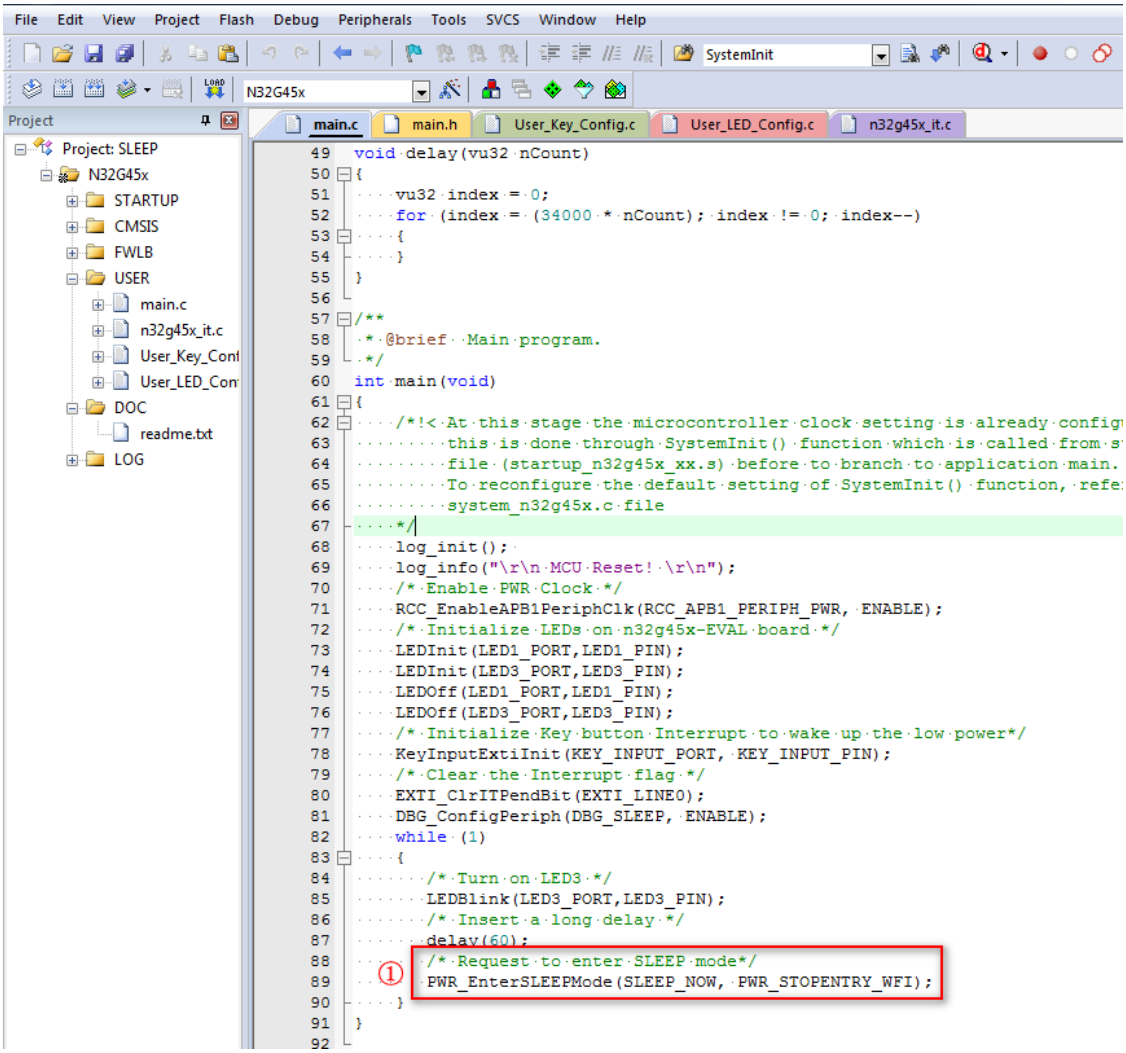
4 Programming Instructions

4.1 Setting to Enter SLEEP Mode

Open the SLEEP project in SDK. The part in circle ① in Figure 4-1 is the API function to enter SLEEP mode. After compiling, download it to the development board.

Figure 4-1 SLEEP Entering Settings



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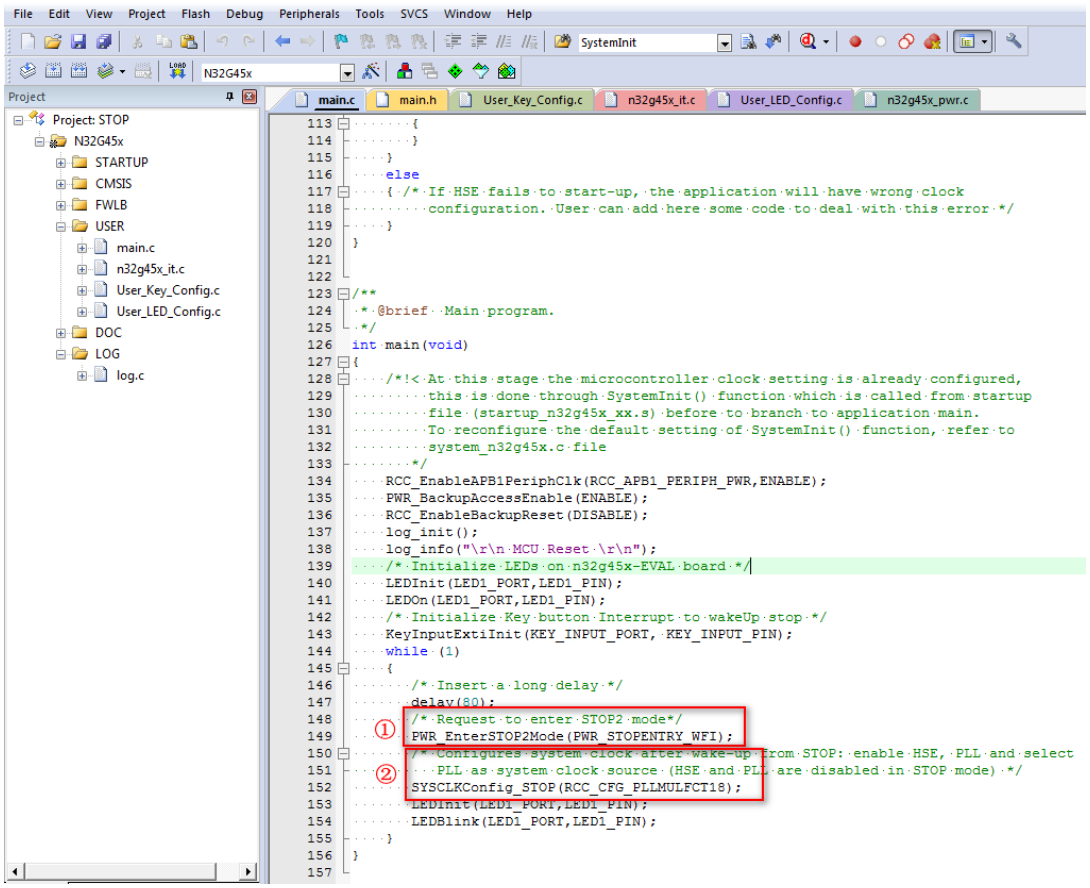
4.2 Setting to Enter STOP2 Mode

STOP2 mode is based on the Cortex®-M4F deep sleep mode, and all the core digital logic domain power are switched off. The main voltage regulator (MR) is switched off, HSE/HSI/PLL are switched off. The CPU registers are maintained, LSE/LSI can be configured, GPIOs are remained, and peripheral I/O multiplexing is not maintained. The 16K bytes of RET-SRAM are maintained, while data in other SRAM and registers are lost. The 84-byte backup register are maintained and GPIO, IOM and EXTI are enabled.

Open the STOP2 project in the SDK, the circled part labeled as ① in Figure 4-2 is the API function for entering STOP2, which sets the entry into STOP2 by interrupt. The circled part labeled as ② in Figure 4-2 is for exiting STOP2 mode and switching the system clock back to the high-speed clock of the system. This mode needs to pay attention to the change of the system clock, so the peripherals need to be reconfigured according to the actual clock source.

Figure 4-2 STOP2 Enter Settings



4.3 Setting to Enter STOP0 Mode

The STOP0 mode is based on the Cortex®-M4F deep sleep mode, combined with the peripheral clock control mechanism. The voltage regulator can be configured in normal or low power mode. In STOP0 mode, most clock sources in the core domain are disabled, such as PLL, HSI, and HSE. However, SRAM, RET-SRAM, and all register contents are preserved.

In STOP0 mode, all I/O pins maintain the same state as in run mode.

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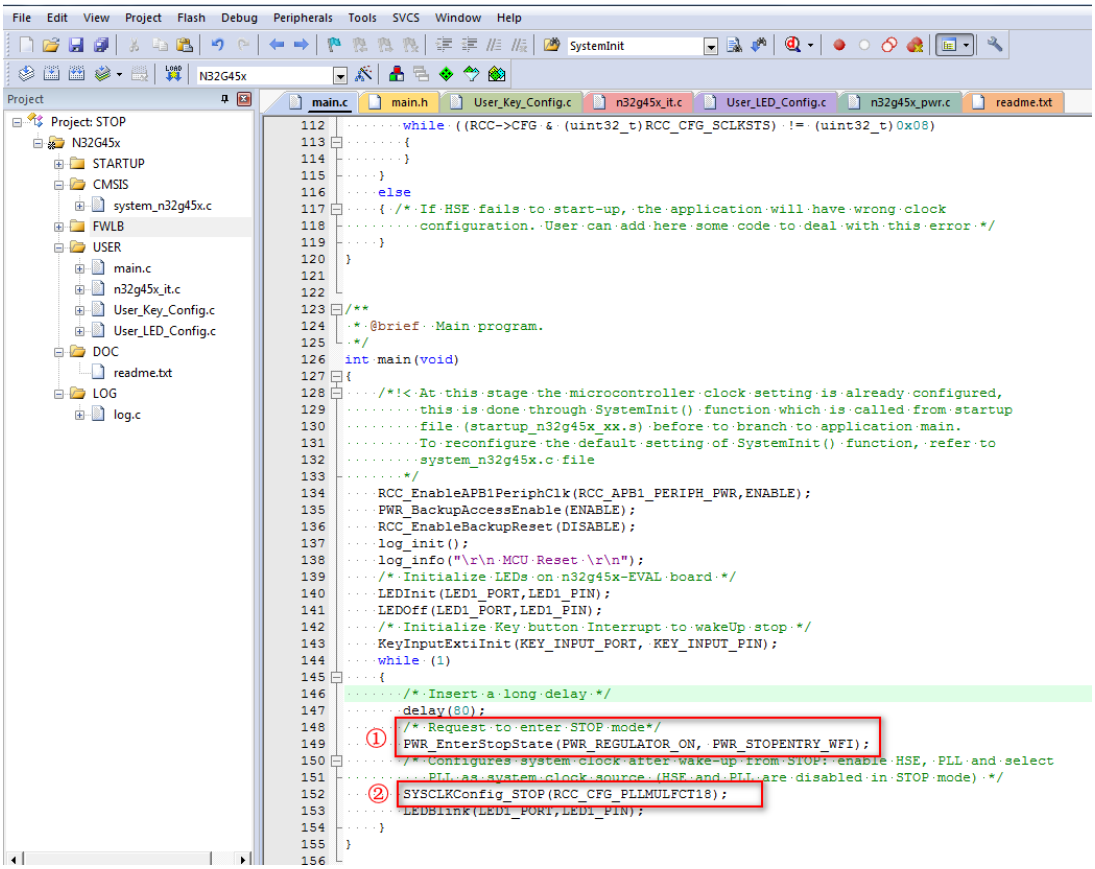
Open the STOP0 project in the SDK, the circled part labeled as ① in Figure 4-3 is the API function for entering STOP0, which sets the entry into STOP0 by interrupt. The circled part labeled as ② in Figure 4-3 is for exiting STOP0 mode and switching the system clock back to the high-speed clock of the system. This mode needs to pay attention to the change of the system clock, so the peripherals need to be reconfigured according to the actual clock source.

Figure 4-3 STOP0 Entering Settings



4.4 Setting to Enter STANDBY Mode

STANDBY mode can achieve lower power consumption, it is based on Cortex®-M4 deep sleep mode, the core domain is completely turned off, and the backup power domain is turned on to supply power to VDD and BKR.

Open the STANDBY project in the SDK, the circled part labeled as ① in Figure 4-4 is the API function for entering STANDBY, which sets the entry into STANDBY by interrupt..

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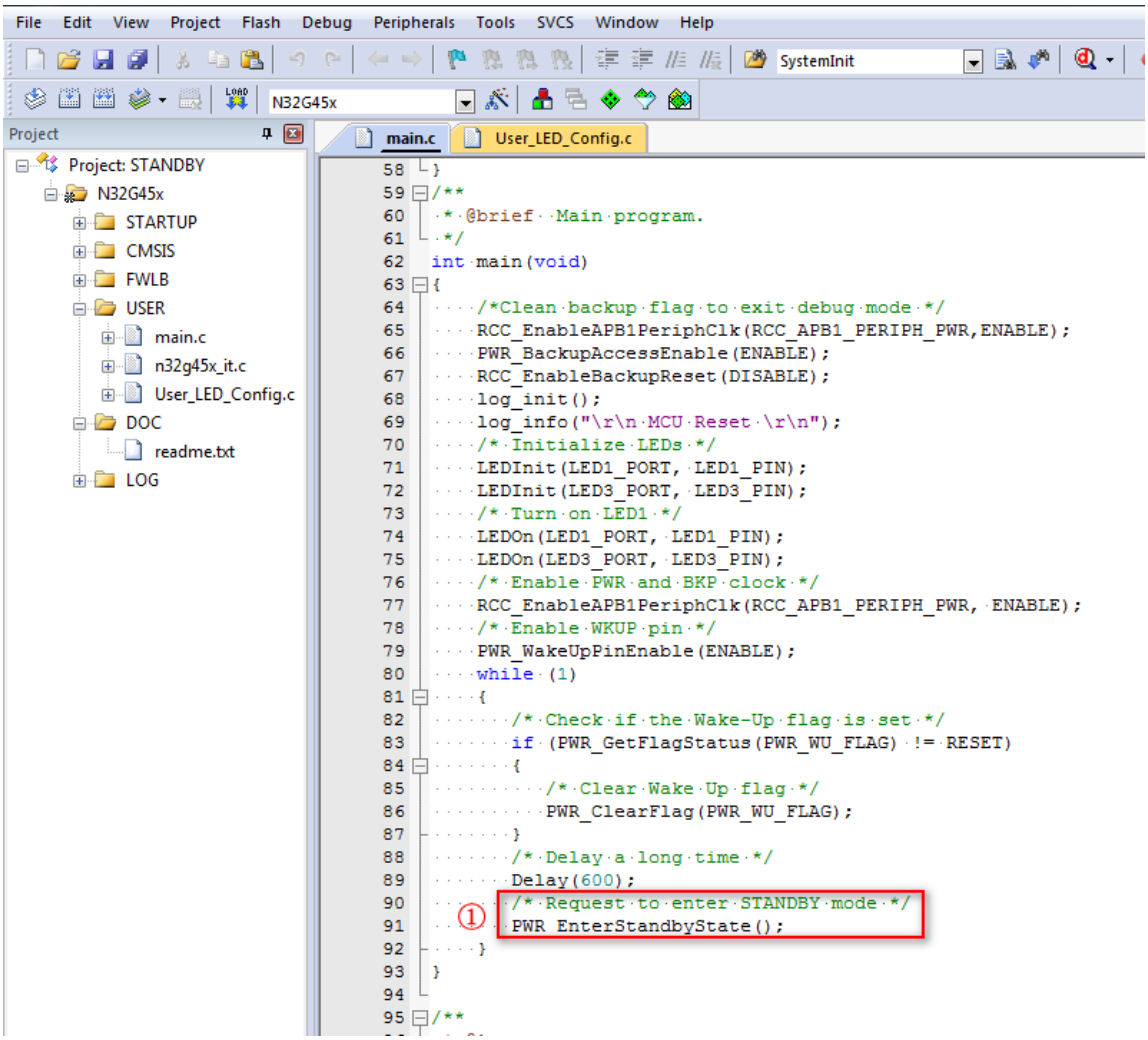
Figure 4-4 STANDBY Entering Settings



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5 Version History

Version	Date	Changes
V1.0	2021-8-6	Create the document
V1.1	2022-7-6	1. Update the power supply block diagram 2. Add remarks about the operating conditions of N32G457 series 3. Optimize the description
V1.2	2024.04.04	Error correction

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