N32G45x series

32-bit ARM® Cortex®-M4 microcontroller

User manual

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Contents

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1 Abbreviations

1.1 List of Abbreviations for Registers

The following abbreviations are used in register descriptions:

read/write(rw)	Software can read and write these bits.
read-only(r)	Software can only read these bits.
write-only(w)	Software can only write this bit, and reading this bit will return the reset value.
read/clear(rc_w1)	Software can read this bit or clear it by writing' 1', and writing' 0' has no effect on this bit.
read/clear(rc_w0)	Software can read this bit or clear it by writing' 0', and writing' 1' has no effect on this bit.
read/clear by read(rc_r)	Software can read this bit. Reading this bit will automatically clear it to' 0'. Writing' 0' has no effect on this bit.
read/set(rs)	Software can read or set this bit. Writing' 0' has no effect on this bit.
read-only write trigger(rt_w)	Software can read this bit and write' 0' or' 1' to trigger an event, but it has no effect on this bit value.
toggle(t)	Software can only flip this bit by writing' 1', and writing' 0' has no effect on this bit.
Reserved(Res.)	Reserved bit, must be kept at reset value.

1.2 Available Peripherals

For all models of N32G45x microcontroller series, the existence and number of a peripheral, please refer to the data sheet of the corresponding model.

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2 Interrupts and Events

2.1 Nested Vectored Interrupt Controller

Features

- 86 maskable interrupt channels (excluding 16 interrupt lines of Cortex-M4).
- 16 programmable priority levels (4-bit interrupt priority level is used);
- Low-latency exception and interrupt handling;
- Power management control;
- Implementation of system control register;

Nested Vector Interrupt Controller (NVIC) is closely connected with the interface of processor core, which can realize low-latency interrupt handling and efficiently handle late interrupts. The nested vector interrupt controller manages interrupts including kernel exceptions.

2.1.1 SysTick Calibration Value Register

The system tick calibration value is fixed at 18000. When the system tick clock is set to 18 MHz (the maximum value of HCLK/8), a 1ms time reference is generated.

2.1.2 Interrupt and Exception Vectors

Table 2-1 Vector table

Position	Priority	Type of priority	Acronym	Description	Address
	-	-	-	Reserved	0x0000_0000
	-3	Fixed	Reset	Reset	0x0000_0004
	-2	Fixed	NMI	Unmatchable interrupt RCC Clock Security System (CSS) is coupled to NMI vector	0x0000_0008
	-1	Fixed	Hardware failure (HardFault)	All types of failures	0x0000_000C
	0	Settable	Management (MemManage)	Memory management	0x0000_0010
	1	Settable	BusFault (bus fault)	Refers to prefetch failure, memory access failure.	0x0000_0014
	2	Settable	Error (UsageFault)	Undefined instruction or illegal status	0x0000_0018
	-	-	-	Reserved	0x0000_001C ~0x0000_002B
	3	Settable	SVCall	System service call through SWI instruction	0x0000_002C
	4	Settable	DebugMonitor (debug monitor)	Debugging monitor	0x0000_0030
	-	-	-	Reserved	0x0000_0034
	5	Settable	PendSV	System services that can be suspended	0x0000_0038
	6	Settable	SysTick	System tick timer	0x0000_003C

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Position	Priority	Type of priority	Acronym	Description	Address
0	7	Settable	WWDG	Window timer interrupt	0x0000_0040
1	8	Settable	PVD	Power supply voltage detection (PVD) interrupt connected to EXTI line 16	0x0000_0044
2	9	Settable	TAMPER	Intrusion detection interrupt	0x0000_0048
3	10	Settable	RTC_WKUP	The real-time clock (RTC) wake-up interrupt connected to EXTI line 20	0x0000_004C
4	11	Settable	FLASH	Flash global interrupt	0x0000_0050
5	12	Settable	RCC	Reset and clock control (RCC) interrupt	0x0000_0054
6	13	Settable	EXTI0	EXTI line 0 interrupt	0x0000_0058
7	14	Settable	EXTI1	EXTI line 1 interrupt	0x0000_005C
8	15	Settable	EXTI2	EXTI line 2 interrupt	0x0000_0060
9	16	Settable	EXTI3	EXTI line 3 interrupt	0x0000_0064
10	17	Settable	EXTI4	EXTI line 4 interrupt	0x0000_0068
11	18	Settable	DMA1 channel 1	DMA1 channel 1 global interrupt	0x0000_006C
12	19	Settable	DMA1 channel 2	DMA1 channel 2 global interrupt	0x0000_0070
13	20	Settable	DMA1 channel 3	DMA1 channel 3 global interrupt	0x0000_0074
14	21	Settable	DMA1 channel 4	DMA1 channel 4 global interrupt	0x0000_0078
15	22	Settable	DMA1 channel 5	DMA1 channel 5 global interrupt	0x0000_007C
16	23	Settable	DMA1 channel 6	DMA1 channel 6 global interrupt	0x0000_0080
17	24	Settable	DMA1 channel 7	DMA1 channel 7 global interrupt	0x0000_0084
18	25	Settable	ADC1_2	ADC1 and ADC2 global interrupts	0x0000_0088
19	26	Settable	USB_HP_CAN1_TX	USB high priority interrupt /CAN1 send interrupt	0x0000_008C
20	27	Settable	USB_LP_CAN1_RX0	USB low priority interrupt /CAN1 receives 0 interrupt	0x0000_0090
21	28	Settable	CAN1_RX1	CAN1 receive 1 interrupt	0x0000_0094
22	29	Settable	CAN_SCE	CAN1 SCE interrupt	0x0000_0098
23	30	Settable	EXTI9_5	EXTI line [9:5] interrupt	0x0000_009C
24	31	Settable	TIM1_BRK	TIM1 brake interrupt	0x0000_00A0
25	32	Settable	TIM1_UP	TIM1 update interrupt	0x0000_00A4
26	33	Settable	TIM1_TRG_COM	TIM1 trigger and communication interrupt	0x0000_00A8
27	34	Settable	TIM1_CC	TIM1 capture comparison interrupt	0x0000_00AC
28	35	Settable	TIM2	TIM2 global interrupt	0x0000_00B0
29	36	Settable	TIM3	TIM3 global interrupt	0x0000_00B4
30	37	Settable	TIM4	TIM4 global interrupt	0x0000_00B8
31	38	Settable	I2C1_EV	I2C1 event interrupt	0x0000_00BC
32	39	Settable	I2C1_ER	I2C1 error interrupt	0x0000_00C0
33	40	Settable	I2C2_EV	I2C2 event interrupt	0x0000_00C4
34	41	Settable	I2C2_ER	I2C2 error interrupt	0x0000_00C8
35	42	Settable	SPI1	SPI1 global interrupt	0x0000_00CC
36	43	Settable	SPI2_I2S2	SPI2/I2S2 global interrupt	0x0000_00D0

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Position	Priority	Type of priority	Acronym	Description	Address
37	44	Settable	USART1	USART1 global interrupt	0x0000_00D4
38	45	Settable	USART2	USART2 global interrupt	0x0000_00D8
39	46	Settable	USART3	USART3 global interrupt	0x0000_00DC
40	47	Settable	EXTI15_10	EXTI line [15:10] interrupt	0x0000_00E0
41	48	Settable	RTCAlarm	RTC alarm interrupt connected to EXTI line 17	0x0000_00E4
42	49	Settable	USBWKUP	USB wake-up interrupt connected to EXTI line 18	0x0000_00E8
43	50	Settable	TIM8_BRK	TIM8 brake interrupt	0x0000_00EC
44	51	Settable	TIM8_UP	TIM8 update interrupt	0x0000_00F0
45	52	Settable	TIM8_TRG_COM	TIM8 trigger and communication interrupt	0x0000_00F4
46	53	Settable	TIM8_CC	TIM8 capture comparison interrupt	0x0000_00F8
47	54	Settable	ADC3_4	ADC3 and ADC4 global interrupts	0x0000_00FC
48	55	Settable	Reserved	Reserved	0x0000_0100
49	56	Settable	SDIO	SDIO global interrupt	0x0000_0104
50	57	Settable	TIM5	TIM5 global interrupt	0x0000_0108
51	58	Settable	SPI3_I2S3	SPI3/I2S3 global interrupt	0x0000_010C
52	59	Settable	UART4	UART4 global interrupt	0x0000_0110
53	60	Settable	UART5	UART5 global interrupt	0x0000_0114
54	61	Settable	TIM6	TIM6 global Interrupt	0x0000_0118
55	62	Settable	TIM7	TIM7 global interrupt	0x0000_011C
56	63	Settable	DMA2 channel 1	DMA2 channel 1 global interrupt	0x0000_0120
57	64	Settable	DMA2 channel 2	DMA2 channel 2 global interrupt	0x0000_0124
58	65	Settable	DMA2 channel 3	DMA2 channel 3 global interrupt	0x0000_0128
59	66	Settable	DMA2 channel 4	DMA2 channel 4 global interrupt	0x0000_012C
60	67	Settable	DMA2 channel 5	DMA2 channel 5 global interrupt	0x0000_0130
61	68	Settable	ETH	Ethernet global interrupt	0x0000_0134
62	69	Settable	ETH_WKUP	Ethernet wake-up interrupt connected to EXTI line 19	0x0000_0138
63	70	Settable	CAN2_TX	CAN2 send interrupt	0x0000_013C
64	71	Settable	CAN2_RX0	CAN2 receive 0 interrupt	0x0000_0140
65	72	Settable	CAN2_RX1	CAN2 receive 1 interrupt	0x0000_0144
66	73	Settable	CAN2_SCE	CAN 2SCE interrupt	0x0000_0148
67	74	Settable	QSPI	QSPI global interrupt	0x0000_014C
68	75	Settable	DMA2 channel 6	DMA2 channel 6 global interrupt	0x0000_0150
69	76	Settable	DMA2 channel 7	DMA2 channel 7 global interrupt	0x0000_0154
70	77	Settable	I2C3_EV	I2C3 event interrupt	0x0000_0158
71	78	Settable	I2C3_ER	I2C3 error interrupt	0x0000_015C
72	79	Settable	I2C4_EV	I2C4 event interrupt	0x0000_0160
73	80	Settable	I2C4_ER	I2C4 error interrupt	0x0000_0164
74	81	Settable	UART6	UART6 global interrupt	0x0000_0168

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Position	Priority	Type of priority	Acronym	Description	Address
75	82	Settable	UART7	UART7 global interrupt	0x0000_016C
76	83	Settable	DMA1 channel 8	DMA1 channel 8 global interrupt	0x0000_0170
77	84	Settable	DMA2 channel 8	DMA2 channel 8 global interrupt	0x0000_0174
78	85	Settable	DVP	DVP global interrupt	0x0000_0178
79	86	Settable	BAG	SAC global interrupt	0x0000_017C
80	87	Settable	MMU	MMU global interrupt	0x0000_0180
81	88	Settable	Reserved	Reserved	0x0000_0184
82	89	Settable	COMP_1_2_3	COMP1, COMP2, COMP3 global interrupt	0x0000_0188
83	90	Settable	COMP_4_5_6	COMP4, COMP5, COMP6 global interrupt	0x0000_018C
84	91	Settable	COMP7	COMP7 global interrupt	0x0000_0190
85	92	Settable	R-SRAM	R-SRAM error interrupt	0x0000_0194

2.2 External Interrupt/Event controller (EXTI)

2.2.1 Introduction

The external interrupt/event controller includes 21 edge detection circuits that generate interrupt/event triggers. Each input line can be independently configured with pulse or pending level input type, and three trigger event types of rising edge, falling edge or both edge can also be independently configured. The pending register holds the interrupt request of the status line, The interrupt request can be cleared by writing a '1' operation in the corresponding bit of the Pending register.

2.2.2 Main Features

The main features of EXTI controller are as follows:

- Support 21 software interrupt/event requests
- The corresponding interrupt/event of each input line can be independently configured with trigger or mask.
- Each interrupt line has an independent status bit.
- Support pulse or suspend input type
- Three types of trigger events are supported: rising edge, falling edge or double edge.
- Wake-up to exit power-saving mode

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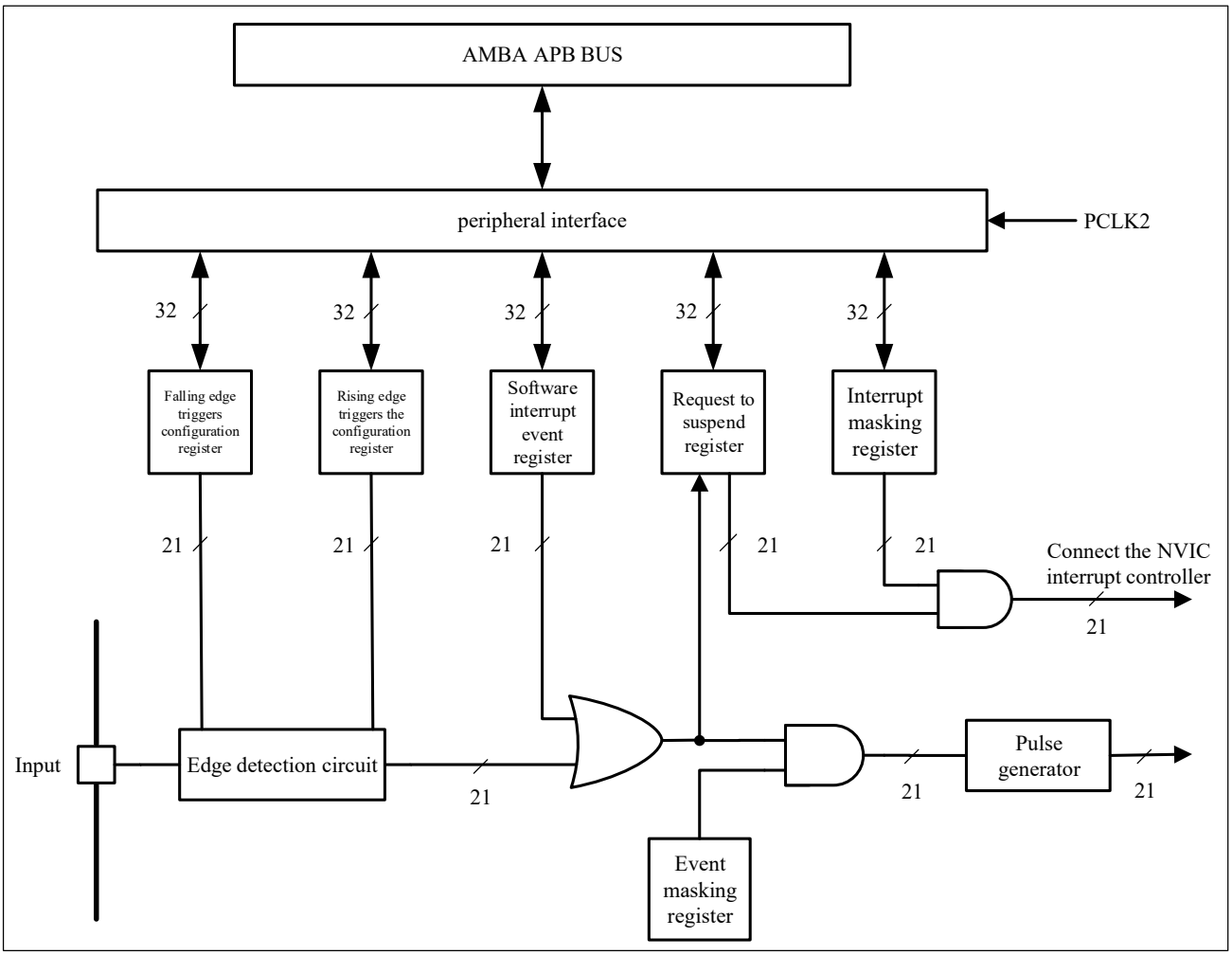
Figure 2-1 External interrupt/event controller block diagram



2.2.3 Functional Description

EXTI contains 21 interrupt lines, of which 16 are from I/O pins and 5 are from internal peripherals or modules. To generate an interrupt, the NVIC interrupt channel of the external interrupt controller must be configured to enable the corresponding interrupt line. Select the type of rising edge, falling edge or double edge trigger event through edge trigger configuration registers EXTI_RT_CFG and EXTI_FT_CFG, and write '1' to the corresponding bit of the interrupt mask register EXTI_IMASK to open the interrupt request. When the preset edge trigger polarity is detected on the external interrupt line, an interrupt request will be generated and the corresponding Pending bit will be set to '1'. Writing '1' in the corresponding bit of the Pending register will clear the interrupt request.

To generate an event, the corresponding event line must be configured and enabled. According to the required polarity of edge detection, set the rising/falling edge trigger configuration register, and write '1' in the corresponding bit of the event mask register to allow the interrupt request. When the preset edge occurs on the event line, an event request pulse will be generated, and the corresponding Pending bit will not be set to '1'.

In addition, by writing '1' in the software interrupt/event register, an interrupt/event request can also be generated by software.

- Hardware interrupt configuration, select and configure 21 lines as interrupt sources as required:

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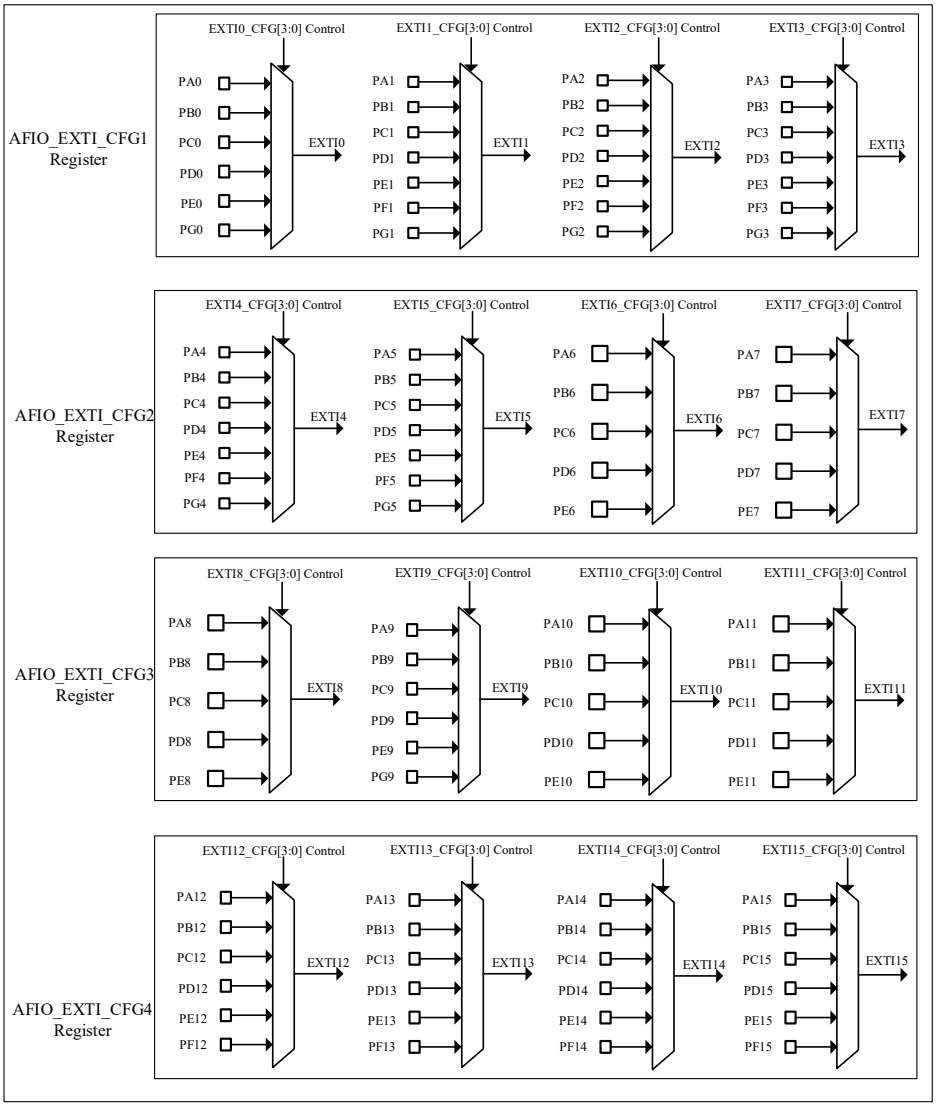
- Configure the mask bits of 21 interrupt lines (EXTI_IMASK);
- Configure the trigger configuration bits (EXTI_RT_CFG and EXTI_FT_CFG) of the selected disconnection;
- Configure the enable and mask bits that control the NVIC interrupt channel mapped to the External Interrupt Controller so that an interrupt coming from one of the 21 lines can be correctly acknowledged.

- Hardware configuration, select and configure 21 lines as event sources as required:
  - Configure the mask bits of 21 event lines (EXTI_EMASK);
  - Configure the trigger selection bits (EXTI_RT_CFG and EXTI_FT_CFG) of the event lines.
- Software interrupt/event configuration, select and configure 21 lines as software interrupt/event lines as required:
  - Configure 21 interrupt/event line mask bits (EXTI_IMASK, EXTI_EMASK);
  - Configure the request bit of the software interrupt event register (EXTI_SWIE).

2.2.4 EXTI Line Mapping

Figure 2-2 External interrupt GPIO mapping



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To configure external interrupts/events on the GPIO line through AFIO_EXTI_CFGy, the AFIO clock must be enabled first. The general I/O port is connected to 16 external interrupt/event lines in the way shown above. The other 5 EXTI lines are connected as follows:

- The EXTI line 16 is connected to PVD output
- The EXTI line 17 is connected to RTC alarm event
- The EXTI line 18 is connected to the USB wake-up event
- The EXTI line 19 is connected to the Ethernet wake-up event.
- The EXTI line 20 is connected to RTC wake-up event

2.3 EXTI Registers

EXTI base address: 0x40010400

2.3.1 EXTI Register Review

Table 2-2 EXTI register review

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
000h	EXTI_IMASK	Reserved											IMASK[20:0]																				
	Reset Value												0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
004h	EXTI_EMASK	Reserved											EMASK[20:0]																				
	Reset Value												0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
008h	EXTI_RT_CFG	Reserved											RT_CFG[20:0]																				
	Reset Value												0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
00Ch	EXTI_FT_CFG	Reserved											FT_CFG[20:0]																				
	Reset Value												0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
010h	EXTI_SWIE	Reserved											SWIE[20:0]																				
	Reset Value												0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
014h	EXTI_PEND	Reserved											PEND20	PEND19	PEND18	PEND17	PEND16	PEND15	PEND14	PEND13	PEND12	PEND11	PEND10	PEND9	PEND8	PEND7	PEND6	PEND5	PEND4	PEND3	PEND2	PEND1	PEND0
	Reset Value												0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
018h	EXTI_TS_SEL	Reserved																												TSSEL[3:0]			
	Reset Value																													0	0	0	0

2.3.2 EXTI Interrupt Mask Register (EXTI_IMASK)

Address offset: 0x00

Reset value: 0x0000 0000

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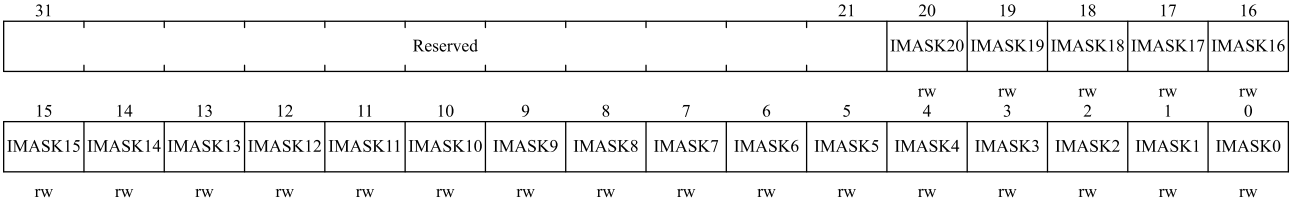
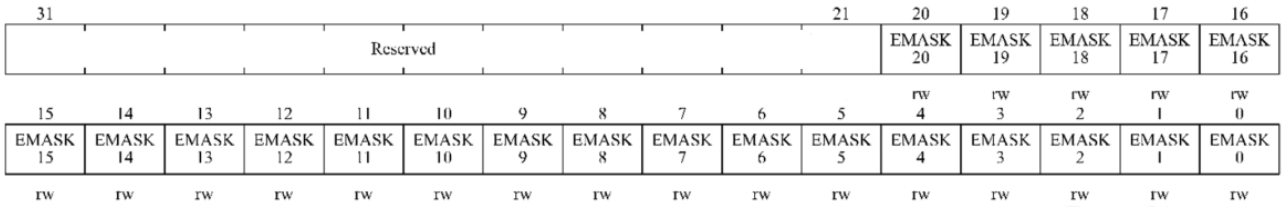


Bit field	Name	Description
31:21	Reserved	Reserved, the reset value must be maintained.
20:0	IMASKx	Interrupt mask on line x 0: Interrupt request from line x is masked; 1: Interrupt request from line x is not masked.

2.3.3 EXTI Event Mask Register (EXTI_EMASK)

Address offset: 0x04

Reset value: 0x0000 0000

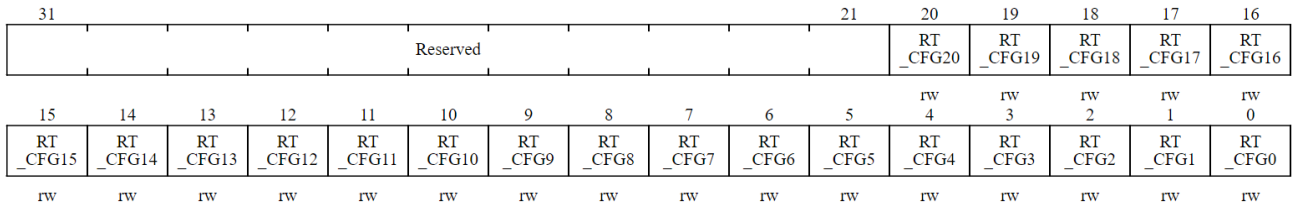


Bit field	Name	Description
31:21	Reserved	Reserved, the reset value must be maintained.
20:0	EMASKx	Event mask on line x 0: Event request from line x is masked; 1: Event request from line x is not masked

2.3.4 Rising Trigger Selection Register (EXTI_RT_CFG)

Address offset: 0x08

Reset value: 0x0000 0000



Bit field	Name	Description
31:21	Reserved	Reserved, the reset value must be maintained.
20:0	RT_CFGx	Rising trigger event configuration bit of line x. 0: Rising trigger disabled (interrupts and events) for input line x. 1: Rising trigger enabled (interrupts and events) for input line x.

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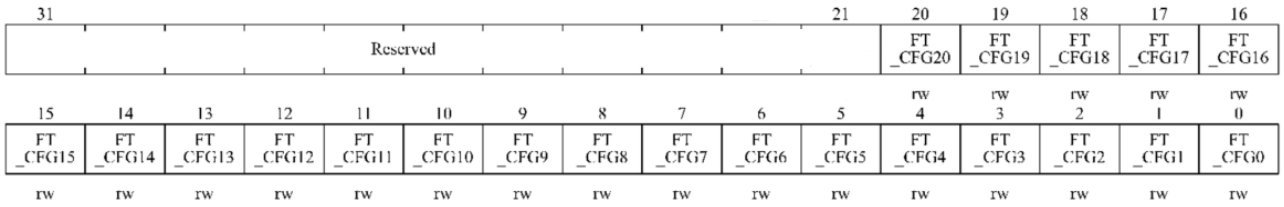
2.3.5 Falling Trigger Selection Register (EXTI_FT_CFG)

Address offset: 0x0C

Reset value: 0x0000 0000

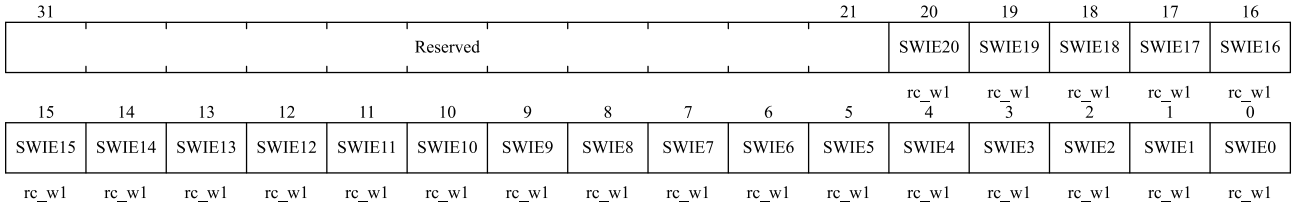


Bit field	Name	Description
31:21	Reserved	Reserved, the reset value must be maintained.
20:0	FT_CFGx	Falling trigger event configuration bit of line x. 0: Falling trigger disabled (interrupts and events) for input line x. 1: Falling trigger enabled (interrupts and events) for input line x.

2.3.6 EXTI Software Interrupt Event Register (EXTI_SWIE)

Address offset: 0x10

Reset value: 0x0000 0000



Bit field	Name	Description
31:21	Reserved	Reserved, the reset value must be maintained.
20:0	SWIEx	Software interrupt on line x When this bit is '0', writing '1' will set the corresponding Pending bit in EXTI_PEND. If this interrupt is allowed in EXTI_IMASK and EXTI_EMASK, an interrupt will be generated at this time. *Note: By writing '1' to clear the corresponding bit of EXTI_PEND, this bit can be cleared to '0'.*

2.3.7 EXTI Pending Register (EXTI_PEND)

Address offset: 0x14

Reset value: 0x0000 0000

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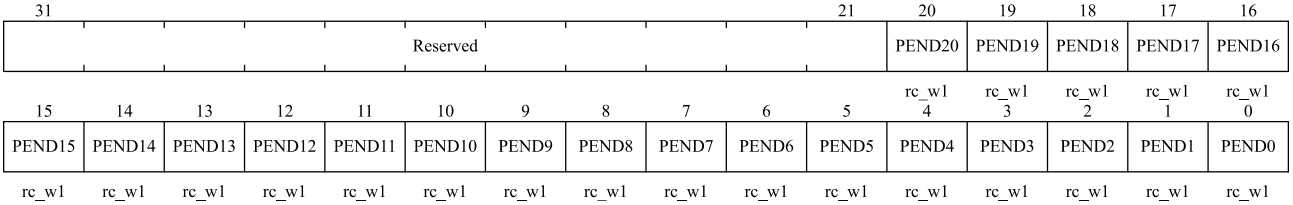
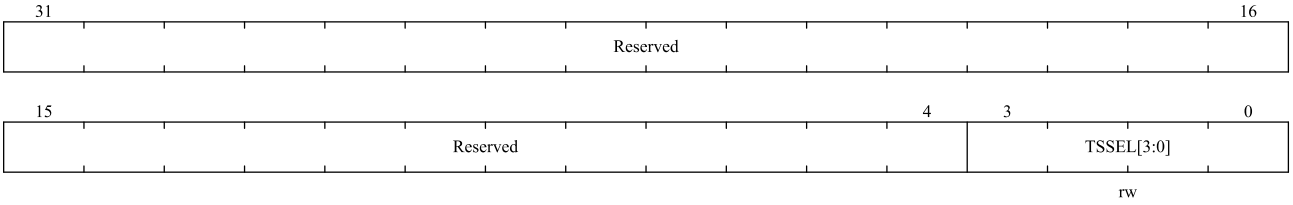


Bit field	Name	Description
31:21	Reserved	Reserved, the reset value must be maintained.
20:0	PENDx	Pending bit on line x 0: No pending request occurred. 1: A pending trigger request has occurred. This bit is set to '1' when a selected edge trigger event occurs on the external interrupt line. Write '1' in this bit to clear it, or change the polarity of edge detection to clear this bit.

2.3.8 EXTI Timestamp Trigger Source Selection Register (EXTI_TS_SEL)

Address offset: 0x18

Reset value: 0x0000 0000



Bit field	Name	Description
31:4	Reserved	Reserved, the reset value must be maintained.
3:0	TSSEL[3:0]	Select external interrupt input as trigger source of timestamp event. 0: Select EXTI0 as the trigger source of timestamp event; 1: Select EXTI1 as the trigger source of timestamp event; …… 15: Select EXTI15 as the trigger source of timestamp event.

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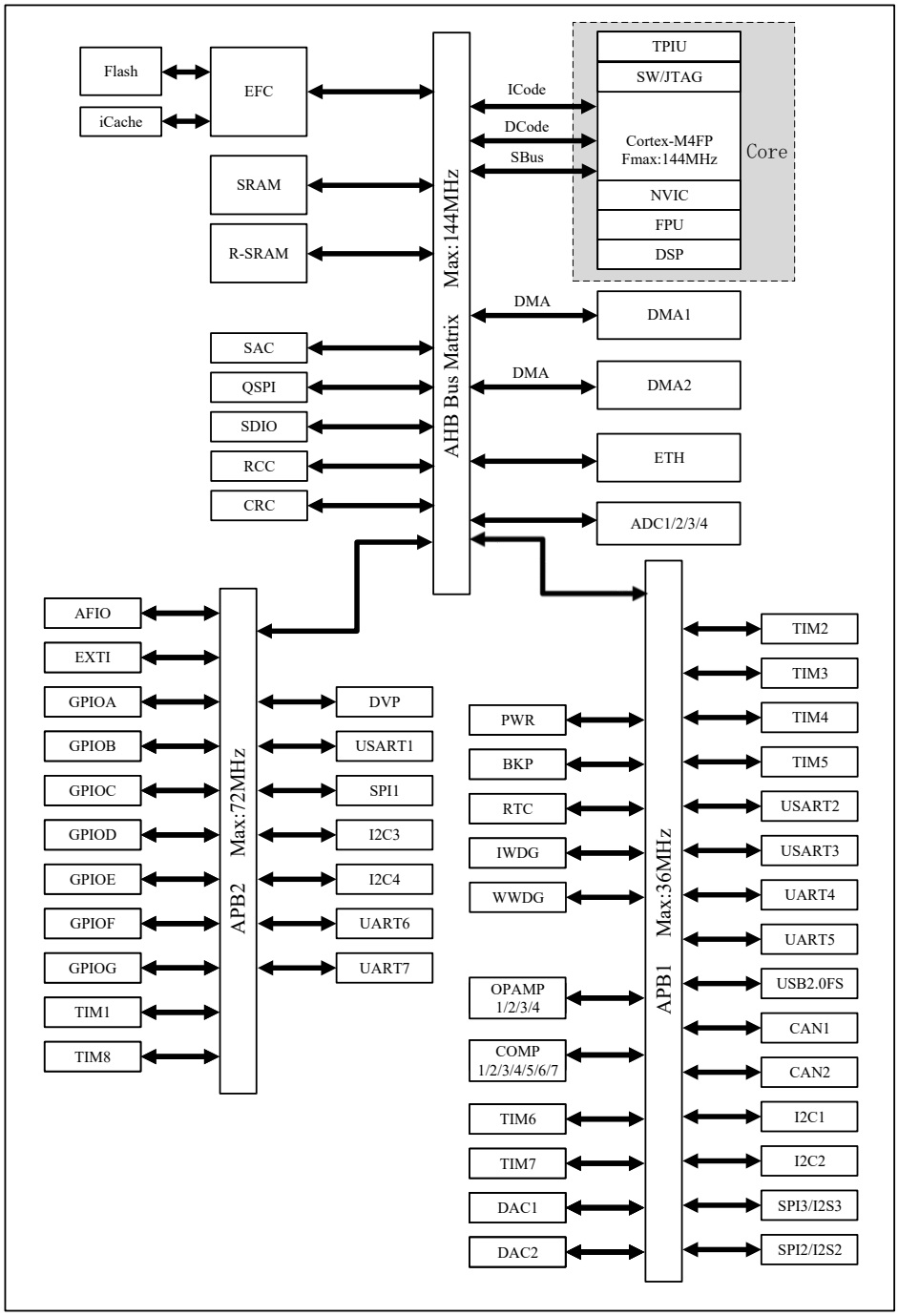
3 Memory and Bus Architecture

3.1 System Architecture

3.1.1 Bus Architecture

Figure 3-1 Bus architecture



- ICode bus: Connect the ICode bus of Cortex™-M4FP core with the flash instruction interface. Instruction prefetching is completed on this bus.

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- The DCode bus connects the DCode bus of Cortex™-M4FP core with the data interface of flash memory (constant loading and debugging access).
- SBus bus connects the SBus bus (peripheral bus) of Cortex™-M4FP core to the bus matrix, which coordinates the access between the core and DMA.
- SAC/CRC has designed matrix interconnection, which supports DMA transmission by software triggering.
- The system consists of two AHB2APB Bridges, i.e. AHB2APB1 and AHB2APB2. Among them, APB1 contains 26 low-speed APB peripherals, and the maximum speed of PCLK1 is 36MHz; APB2 contains 18 high-speed APB peripherals, and the maximum speed of PCLK2 is equal to 72MHz.

3.1.2 Bus Address Mapping

The address mapping includes all AHB and APB peripherals: AHB peripherals, APB1 peripherals, APB2 peripherals, Flash, SRAM, System Memory, etc. And the address space of SRAM is located in the bit-band Region of SRAM, and atomic accesses can be made through the bit-band Alias to performed read-modify-write operations on the target bits of the bit-band region. The address spaces of all APB and AHB peripherals are located in the bit-band Region of the peripherals. Atomic accesses can be made through the bit-band Alias to performed read-modify-write operations on the target bits of the bit-band region. The specific mapping is as follows:

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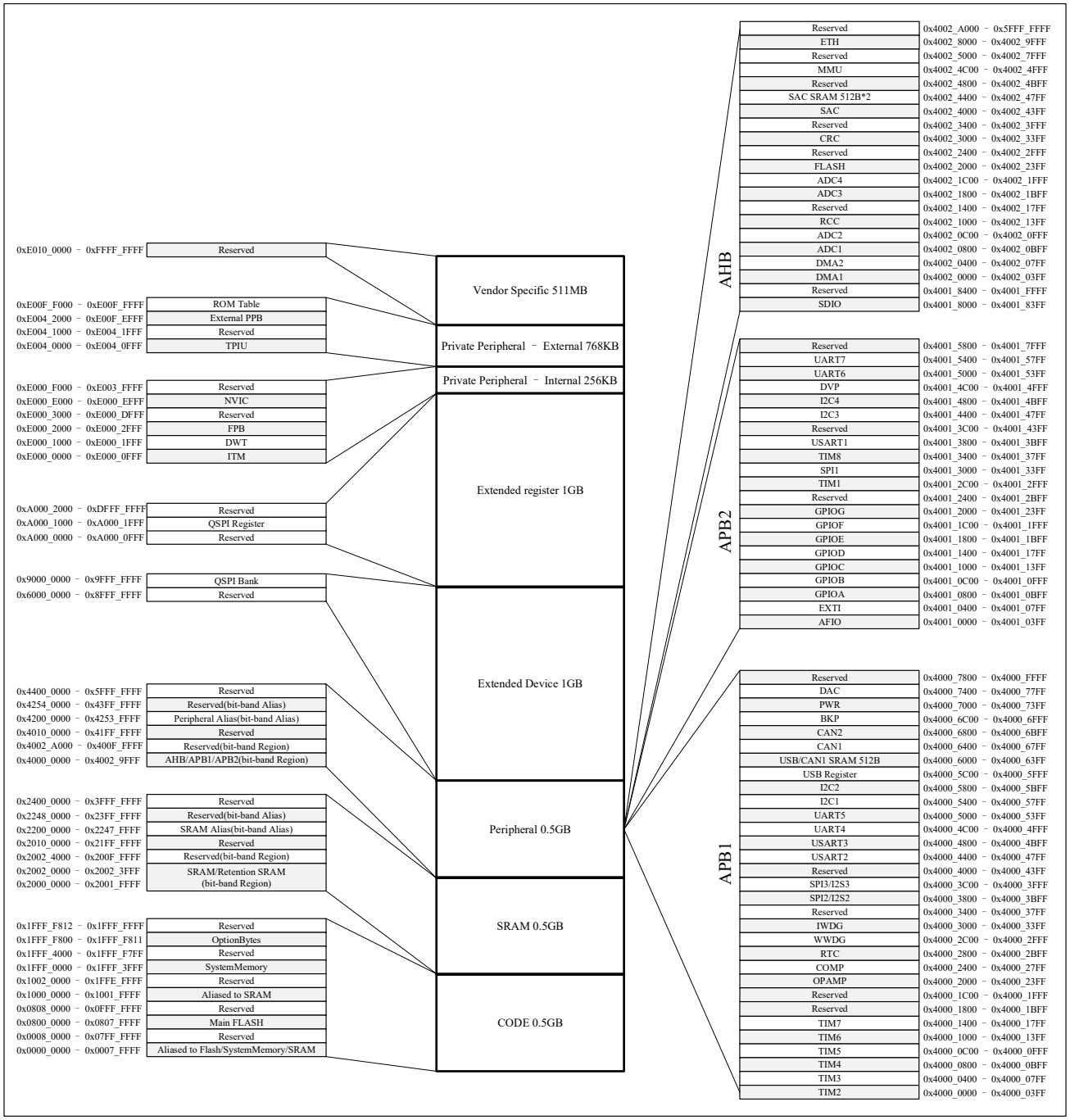
Figure 3-2 Bus address map



3.1.2.1 Bit Banding

Cortex™-M4FP memory image includes two bit-band areas. These two bit-band areas map each word in the alias memory area to a bit in the bit-band memory area. When writing a word in the alias area, it is equivalent to performing a read-modify-write operation on the target bits of the bit segment area.

Both the peripheral registers and SRAM are mapped into a bit-band area, which allows a single bit-band area write and read operation to be performed.

The following mapping formula shows how each byte in the alias area corresponds to the corresponding bit in the bit band area:

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bitband_byte _addr = bitband _base + (byte_offset×32) + (bit_number×4)

In which:

bitband_byte_addr is the address of the byte in the alias memory area, which is mapped to a certain target bit;

bitband_base is the starting address of alias area;

byte_offset is the serial number of the byte containing the target bit in the bit-band;

bit_number is the position of the target bit (0-7).

For example:

The following example shows how to map bit 4 in bytes with SRAM address 0x20000400 in alias area:

0x22008010 = 0x22000000 + (0x400×32) + (4×4).

Writing to address 0x22008010 has the same effect as reading-modify-writing to bit 4 of address 0x20000400 bytes in SRAM.

Reading 0x22008010 address returns the value of bit 4 (0x01 or 0x00) of address 0x20000400 bytes in SRAM. Please refer to “Cortex™-M4 Technical Reference Manual” for more information about bit-banding.

3.1.3 Boot Management

3.1.3.1 Boot Address

When the system starts, the boot mode after reset can be selected through BOOT1 and BOOT0 pins. After system reset or exit from standby mode, the value of BOOT pin will be re-latched. After a startup delay, the CPU gets the address at the top of the stack from address 0x0000_0000 and executes the code from the reset vector address indicated by address 0x0000_0004.Because of the Cortex™-M4 always gets the stack top pointer and reset vector from addresses 0x0000_0000 and 0x0000_0004, so boot is only suitable for starting from the CODE area, and address remapping is designed for boot space. There are three boot modes to choose from:

- Boot from Main Flash:
  - Mian flash memory is mapped to the boot space (0x0000_0000);
  - Mian flash memory is accessible in two address areas, 0x0000_0000 or 0x0800_0000（ICode/DCode/DMA1/DMA2);
- Boot from System Memory:
  - System memory is mapped to boot space (0x0000_0000);
  - System memory can be accessed in two address areas, 0x0000_0000 or 0x1FFF_0000（ICode/DCode/DMA1/DMA2);
- Boot from the built-in SRAM:
  - The built-in SRAM is mapped to boot space (0x0000_0000);
  - The built-in SRAM is accessible in two address areas, 0x0000_0000 or 0x2000_0000（ICode/DCode/SBus/DMA1/DMA2);

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3.1.3.2 Boot Configuration

In addition, SRAM can also be accessed through virtual address segment 0x1000_0000, which makes the CPU jump to SRAM to run programs through ICode/DCode after starting from Main Flash or System Memory (note that programs are not started from SRAM and do not belong to startup mode). In addition to the BOOT pin configuration boot program, there are two ways to run the program in SRAM:

- Jump directly to the physical address segment 0x2000_0000 of SRAM to run the program. At this time, the program will be run through SBus.
- Jump to the virtual address segment 0x1000_0000 of SRAM, and internally remap to the physical address segment 0x2000_0000 to run the program. At this time, the program will run efficiently through ICode/DCode.

Table 3-1 List of boot mode

Boot mode select pin		**Boot mode**	**Specifies the start address for accessing memory space in boot mode**		
BOOT1	BOOT0		Main Flash	System Memory	SRAM
X	0	Mian Flash start	0x0000_0000 0x0800_0000	0x1FFF_0000	0x1000_0000 0x2000_0000
0	1	System Memory start	0x08000000	0x0000_0000 0x1FFF_0000	0x1000_0000 0x2000_0000
1	1	SRAM start	0x08000000	0x1FFF_0000	0x0000_0000 0x1000_0000 0x2000_0000

3.1.3.3 Embedded boot loader

Embedded boot loader program is stored in the system memory System Memory and is used to reprogram the flash memory through the USART1 or USB-FS interface (full-speed USB device, DFU protocol). The USB-FS interface can only be run when the external clock (HSE) of 4MHz, 6MHz, 8MHz, 12MHz, 16MHz, 18MHz, 24MHz and 32MHz is used. In addition to the above-mentioned 8-frequency external clock (HSE), the USART1 interface can also rely on the internal 8MHz oscillator (HSI) to run. Consult the bootloader manual for further details.

3.2 Memory system

The program memory, data memory, registers and I/O ports are organized in the same 4GB linear address space. Data bytes are stored in the memory in little endian format. The lowest address byte in a word is regarded as the least significant byte of the word, while the highest address byte is the most significant byte. The specifications of program memory and data memory are as follows.

3.2.1 FLASH Specification

Flash consists of a main storage area and an information area, which are described separately below: (Capacity values in the following description do not include ECC)

- The maximum main memory area is 512KB, also known as main flash memory, which contains 256 Page for storing and running user programs and storing data.
- The information area is 20KB, including 10 Page, and consists of system storage area (16KB), system

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configuration area (2KB) and option byte area (2KB).

- The System Memory area is 16KB, which contains 8 Page, also known as System Memory, and is used to store and run the BOOT program.
- The system configuration area is 2KB, including 1 Page.
- The Option Byte area is 2KB, containing 1 Page, also known as Option Byte, and the effective space is 18B, BOOT programs and user programs can be read, written or erased.

3.2.1.1 Flash Memory Mdule Organization

Bus address space is allocated to the main storage area and the information area.

Table 3-2 Flash bus address list

Memory area	Page name	Address range	Size
Main memory area	Page 0	0x0800_0000 – 0x0800_07FF	2KB
	Page 1	0x0800_0800 – 0x0800_0FFF	2KB
	Page 2	0x0800_1000 – 0x0800_17FF	2KB
	⋮	⋮	⋮
	Page 255	0x0807_F800 – 0x0807_FFFF	2KB
Information area	System memory area	0x1FFF_0000 – 0x1FFF_3FFF	16KB
	System configuration area	0x1FFF_F000 – 0x1FFF_F7FF	2KB
	Option byte area	0x1FFF_F800 – 0x1FFF_F811	18B
Memory area interface register	FLASH_AC	0x4002_2000 – 0x4002_2003	4B
	FLASH_KEY	0x4002_2004 – 0x4002_2007	4B
	FLASH_OPTKEY	0x4002_2008 – 0x4002_200B	4B
	FLASH_STS	0x4002_200C – 0x4002_200F	4B
	FLASH_CTRL	0x4002_2010 – 0x4002_2013	4B
	FLASH_ADD	0x4002_2014 – 0x4002_2017	4B
	Reserved	0x4002_2018 – 0x4002_201B	4B
	FLASH_OB	0x4002_201C – 0x4002_201F	4B
	FLASH_WRP	0x4002_2020 – 0x4002_2023	4B
	FLASH_ECC	0x4002_2024 – 0x4002_2027	4B
	Reserved	0x4002_2028 – 0x4002_202B	4B
	FLASH_RDN	0x4002_202C – 0x4002_202F	4B
	FLASH_CAHR	0x4002_2030 – 0x4002_2033	4B

Flash memory is organized into 32-bit wide memory units, which can store codes and data constants.

Information is divided into three parts:

- The system memory area is used for storing a boot program for boot loader mode of the system memory. The boot program uses USART1 and USB (DFU) serial interface to program the flash memory.
- System configuration area, which contains basic information of the chip.
- Option byte area, writing to main memory and information block is managed by embedded flash

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programming/erasing controller.

There are two ways to protect flash memory from illegal access (read, write and erase):

- Page write protection (WRP)
- Read protection (RDP)

When the flash memory write operation is executed, any read operation to the flash memory will lock the bus, and the read operation can only be carried out correctly after the write operation is completed. That is, when writing or erasing, cannot have any read access to the code or data.

The internal RC oscillator (HSI) must be turned on when the flash memory is programmed (written or erased).

Note: In the low power consumption mode, all flash memory operations are suspended.

3.2.1.2 Read and Write Operation

The Flash operation only supports 32-bit operation, and the Flash should be erased before the write operation, and the minimum block size for erasing is one Page 2KB. Write operation is divided into programming and erasing phases.

When reading Flash, the number of waiting cycles for reading can be configured by the register. When using, it needs to be calculated in combination with the clock frequency of AHB interface. For example, when HCLK<=32MHz, the minimum number of waiting periods is 0; When 32MHz<HCLK<=64MHz, the minimum number of waiting periods is 1; When 64MHz<HCLK<=96MHz, the minimum number of waiting periods is 2; When 96MHz<HCLK<=128MHz, the minimum number of waiting periods is 3;When 128MHz<HCLK<=144MHz, the minimum number of waiting periods is 4.

Note: Enable prefetch buffer whether number of wait periods is not zero can improve overall efficiency.

3.2.1.3 Unlock Flash

After reset, the Flash module is protected and cannot be written into the FLASH_CTRL register to prevent accidental operation of Flash due to electrical interference and other reasons. By writing a specific sequence of key values into the FLASH_KEY register, you can open the operation authority of the FLASH_CTRL register. The specific sequence is: Firstly, writing KEY1 = 0x45670123 in the FLASH_KEY register. Secondly, write KEY2 = 0xCDEF89AB in the FLASH_KEY register.

If there is an error in sequence or key value, a bus error will be returned and the FLASH_CTRL register will be locked until the next reset. The software can check whether the Flash has been unlocked by looking at the FLASH_CTRL.LOCK bit. If normal lock setting is needed, it can be realized by setting the FLASH_CTRL.LOCK bit to 1 by software. After that, you can unlock the Flash by writing the correct key value series in FLASH_KEY.

3.2.1.4 Erase and Program

3.2.1.4.1 Erase of Main Memory Area

The main memory area can be erased page by page or whole.

Page Erase

Page Erase process:

- Check the FLASH_ STS.BUSY bit to confirm that there are no other flash operations in progress;
- Set the FLASH_CTRL.PER bit to' 1';

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- Select the page to be erased with the FLASH_ADD register;
- Set the FLASH_CTRL.START bit to' 1';
- Wait for the FLASH_ STS.BUSY bit to change to' 0';
- Read out the erased page and verify it.

Mass Erase

Mass Erase process:

- Check the FLASH_ STS.BUSY bit to confirm that there are no other flash operations in progress;
- Set the FLASH_CTRL.MER bit to' 1';
- Set the FLASH_CTRL.START bit to' 1';
- Wait for the FLASH_ STS.BUSY bit to change to' 0';
- Read out all pages and verify.

3.2.1.4.2 Main memory area programming

The main memory area can be programmed with 32 bits at a time. When the FLASH_CTRL.PG bit is' 1', writing a word in a flash address will start programming once; Writing any half word of data will result in a bus error. During the programming process (the FLASH_ STS.BUSY bit is' 1'), any operation of reading or writing the flash memory will cause the CPU to pause until the end of the flash programming.

Main memory programming process:

- Check the FLASH_ STS.BUSY bit to confirm that there are no other flash operations in progress;
- Set the FLASH_CTRL.PG bit to '1';
- Write the word to be programmed at the specified address;
- Wait for the FLASH_ STS.BUSY bit to change to '0';
- Read the written address and verify the data.

Note: When the FLASH_STS.BUSY bit is '1', you cannot write to any register.

3.2.1.4.3 Option byte erase and programming

The option byte area is programmed differently from the main storage area. The number of option bytes is only 9 bytes (4 bytes for write protection, 2 bytes for read protection, 1 byte for configuration and 2 bytes for storing user data). After unlocking the Flash, you must write KEY1 and KEY2 respectively (see 3.2.1.3) to the FLASH_OPTKEY register, and then set the FLASH_CTRL.OPTWE bit to' 1'. At this time, the option byte area can be programmed: set the FLASH_CTRL.OPTPG bit to' 1' and then write the word to the specified address.

When programming the word in the option byte area, use the low byte in the half-word and automatically calculate the high byte (the high byte is the complement of the low byte), and start the programming operation, which will ensure that the option byte and its complement are always correct.

Option byte erase process:

- Check the FLASH_ STS.BUSY bit to confirm that there are no other flash operations in progress;
- Unlock the FLASH_CTRL.OPTWE bit;

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- Set the FLASH_CTRL.OPTER bit to '1';
- Set the FLASH_CTRL.START bit to '1';
- Wait for the FLASH_ STS.BUSY bit to change to '0';
- Read the erased option byte and verify it.

Option byte area programming process:

- Check the FLASH_ STS.BUSY bit to confirm that there are no other flash operations in progress;
- Unlock the FLASH_CTRL.OPTWE bit;
- Set the FLASH_CTRL.OPTPG bit to '1';
- Writing the word to be programmed to the specified address;
- Wait for the FLASH_ STS.BUSY bit to change to '0';
- Read the written address and verify the data.

3.2.1.5 ECC function

The Flash module supports the ECC function to realize 1-bit error detection and 1-bit error correction. ECC encoding and decoding (error correction, error detection) are automatically performed by hardware. If an error is detected, the error bit is set and an interrupt is generated.

3.2.1.6 Instruction prefetching

The instruction prefetch function of Flash module supports the prefetch Buffer of 16B. Through instruction prefetching, the instruction execution efficiency of CPU can be improved. The instruction prefetch function can be configured to be enabled or disabled through the register, and it is enabled by default.

3.2.1.7 Option byte

Option byte block is mainly used to configure read-write protection, boot mode configuration, software/hardware watchdog configuration and reset options when the system is in standby/stop0/stop2 mode, and bus address space is allocated for read-write access. They consist of byte with 9 options: 4 byte for write protection, 2 bytes for read protection, 1 byte for configuration option, 2 bytes defined by user, These 9 bytes need to be written through the bus. The option byte block also contains the complement codes corresponding to these 9 option bytes. These complement codes need to be automatically calculated by hardware when the option bytes are written in the bus, and written into Flash together, and used for verification when the option bytes are read.

By default, the option byte block is always readable and write-protected. To write (program/erase) the option byte block, first unlock the Flash, then unlock the option byte: write the correct key-value sequence (KEY1 = 0x45670123, KEY2 = 0xCDEF89AB) in the FLASH_OPTKEY, and then write the option byte block will be allowed. If the sequence is wrong or the key value is wrong, a bus error will be returned and the option byte will be locked until the next reset. If it is necessary to set the lock normally, it can be realized by writing 0 to the FLASH_CTRL.OPTWE bit by software, and then the option byte can be unlocked by writing the correct key-value series in the FLASH_OPTKEY.

After each system reset, the option byte data is read out from the option byte block of Flash and stored in the option byte register (FLASH_OB/FLASH_WRP) with read-only property. At the same time, the option byte complement data read out together will be used to verify whether the option byte data is correct. If it does not match, an option

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byte error flag (FLASH_OB.OBERR) will be generated. When an option byte error occurs, the corresponding option byte is forced to 0xFF. When the option byte and its complement are both 0xFF (the state after erasing), the above verification steps are skipped and verification is not required.

Table 3-3 Option byte list

Address	[31:24] Corresponding complement code	[23:16] Option byte	[15:8] Corresponding complement code	[7:0] Option byte
0x1FFF_F800	nUSER	USER	nRDP1	RDP1
0x1FFF_F804	nData1	Data1	nData0	Data0
0x1FFF_F808	nWRP1	WRP1	nWRP0	WRP0
0x1FFF_F80C	nWRP3	WRP3	nWRP2	WRP2
0x1FFF_F810	-	-	nRDP2	RDP2

- Read protection L1 level option byte: RDP1
  - Protect the code stored in the flash memory;
  - When the correct value is written, it will be forbidden to read the flash memory;
  - The result of whether RDP1 is turned on or not can be inquired through FLASH_OB[1];
- User configuration options: USER
  - USER[7:3]：Reserved
  - USER[2]：nRST_STDBY configuration options, read through FLASH_OB [4]

    0：Reset when entering standby mode

    1：No reset occurs when entering standby mode
  - USER[1]：nRST_STOP, read through FLASH_OB[3]

    0：Reset occurs when entering stop0/stop2 mode

    1：No reset occurs when entering stop0/stop2 mode
  - USER[0]：WDG_SW configuration options, read through FLASH_OB [2]

    0：Hardware watchdog

    1：Software watchdog
- 2 bytes of user data: Datax
  - Data1 (stored in FLASH_OB[25:18]);
  - Data0 (stored in FLASH_OB [17:10]);
- Write protection option byte: WRP0 ~ 3, which can be written through the register FLASH _WRP [31:0] query
  - WRP0: write protection of pages 0-15, bit [0] corresponds to Page0 / 1,., bit [7] corresponds to page14 / 15;
  - WRP1: write protection on pages 16-31, bit [0] corresponds to Page16 / 17,., bit [7] corresponds to Page30 / 31;
  - WRP2: write protection on pages 32-47 bit [0] corresponds to Page32 / 33,., bit [7] corresponds to Page46

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/ 47;

- WRP3: write protection on pages 48-255, bit [0] corresponds to Page48 /49., bit [6] corresponds to Page60 / 61， bit [7] corresponds to Page62 / 255;

- Read protection L2 level option byte: RDP2
  - Add protection function on the basis of L1, see 3.2.1.9 detailed description of read protection;
  - Whether RDP2 is turned on or not can be determined by FLASH_OB [31] query;

3.2.1.8 Write protect

Write protection can be configured for all pages in the flash main storage area (maximum 512KB) to prevent accidental write operations caused by program runaway or electrical interference. The basic unit of write protection is: for Page0 ~ 61, every 2 pages is a basic protection unit, for Page62~255, together as a protection unit. Write protection can be configured by setting WRP0 ~ 3 in the option byte block; After each configuration, A system reset is required for the configured value to be reloaded to take effect. If an attempt is made to program or erase a protected page, a protection error flag will be returned in the FLASH_STS.

The system memory block (16KB) in the system information area stores the boot program and cannot be changed.

The system configuration block (2KB) in the system information area stores the basic information of the chip and cannot be changed.

The option byte block (2KB) in the system information area stores the user-configurable option byte information. The write protection of the option byte block is achieved by writing 0 to the FLASH_CTRL.OPTWE bit by software, and after that, you can write the correct key value series in FLASH_OPTKEY to release the write protection of the option byte.

3.2.1.9 Read protection

The user code in flash can be protected from illegal reading by setting read protection. Read protection is mainly aimed at protecting the access operation of main memory area and option byte block after chip sealing operation. Read protection is set by configuring RDP bytes in the option byte block. Three different read protection levels can be configured, as shown in the following Table

Table 3-4 Read protection configuration list

Read protection status	RDP1	nRDP1	nRDP2	RDP2
L1 level	0xFF	0xFF	RDP2! = 0xCC || nRDP2! = 0x33	
Unprotected	0xA5	0x5A	RDP2! = 0xCC || nRDP2! = 0x33	
L2 level	0xXX	0xXX	0x33	0xCC
L1 level	Not the above three configurations			

- L0 level:
  - In unprotected state, corresponding (RDP1 == 0xA5 & nRDP1 == 0x5A) && (RDP2!= 0xCC | nRDP2!= 0x33);
  - The main memory area and option byte block can be read arbitrarily;
  - The write protection property of each page can be configured for programming and erasing;
- L1 level:

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- The corresponding ~ (((RDP1 == 0xA5 & nRDP1 == 0x5A) && (RDP2!= 0xCC | nRDP2!= 0x33)) | (RDP2 == 0xCC & nRDP2 == 0x33));
- Only the read operation of the main storage area from the user code is allowed, that is, when the program is started from the main flash memory in non debugging mode, the read operation of the main storage area is allowed;
- Pages 0~1 are automatically write-protected;
- Other pages can be programmed by the code executed in the main flash memory (realizing IAP or data storage and other functions);
- All pages are not allowed to write or erase in debug mode or after booting from internal SRAM (except for mass erase);
- All functions of loading code into the built-in SRAM through JTAG/SWD and then execute it are still valid, or they can be started from the built-in SRAM through JTAG/SWD, which can be used to remove read protection;
- When the read-protected option byte is rewritten to the unprotected L0 level, all the main storage areas will be automatically erased, and the process is as follows: (Erasing the option byte block will not result in automatic whole erasing operation, because the result of erasing is 0xFF, which is equivalent to still being in the protection state of L1 level)
    - Write the correct key value sequence to unlock the option byte area in FLASH_OPTKEY;
    - The bus initiates a command to erase the entire option byte area (Page erase);
    - Bus write 0xA5 to read protection option byte;
    - Automatically erase all main storage areas internally;
    - Automatically write 0xA5 to read protection option byte internally;
    - When the system is reset (such as software reset, etc.), the option byte block (including the new RDP value 0xA5) will be reloaded into the system, and the read protection will be released;
- The following access operations to the flash memory will be prohibited:
    - Access main flash memory from built-in SRAM start execution code (including using DMA);
    - Access the main flash memory by JTAG, SWV (serial line observer), SWD (serial line debugging) and boundary scanning;

- L2 level: Except that SRAM boot disabled, debug mode disabled, option byte write/page erase disabled and the protection level cannot be modified (irreversible), other features are the same as L1 level. The L2 level is realized by configuring another option byte, RDP2. No matter what the value of RDP1 is, as long as it satisfies (RDP2==0xCC & nRDP2==0x33), it is L2 level.

Table 3-5 Flash read-write-erase (1) permission control table

protect level	Boot mode	Main Flash				Changing a Protection Level
	Perform user	JTAG/	Mian Flash	System Memory	SRAM	

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	Access area	SWD				
L0 level	Before 4KB of flash main memory area	Read-Write-Erase	Read-Write-Erase	Read-Write-Erase	Read-Write-Erase	Change to L1 or L2 is allowed
	After 4KB of flash main memory area	Read-Write-Erase	Read-Write-Erase	Read-Write-Erase	Read-Write-Erase	
	Flash main memory area mass erase	Allow	Allow	Allow	Allow	
	Flash option byte area	Read-Write-Erase	Read-Write-Erase	Read-Write-Erase	Read-Write-Erase	
	Flash system memory area	prohibit	prohibit	Read-Write-Erase	prohibit	
	SRAM (All)	Read and write	Read and write	Read and write	Read and write	
L1 level	Before 4KB of flash main memory area	Prohibit	Read-only	Read-only	Read-only	L0 or L2 is allowed. When changed to L0, the main memory area is automatically erased.
	After 4KB of flash main memory area	Prohibit	Read-Write-Erase	Read-Write-Erase	Read-Write-Erase	
	Flash main memory area mass erase	Allow	Allow	Allow	Allow	
	Flash option byte area	Read-Write-Erase	Read-Write-Erase	Read-Write-Erase	Read-Write-Erase	
	Flash system memory area	Prohibit	Prohibit	Read-write-erase	Prohibit	
	SRAM (All)	Read and write	Read and write	Read and write	Read and write	
L2 level	Before 4KB of flash main memory area	JTAG/SWD interface is disabled.	Read-only	Read-only	Read-only	No modification is allowed.
	After 4KB of flash main memory area		Read-write-erase	Read-write-erase	Read-write-erase	
	Flash main memory area mass erase		Allow	Allow	Allow	

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	Flash option byte area		Read-only	Read-only	Read-only	
	Flash system memory area		Prohibit	Read-write-erase	Prohibit	
	SRAM (All)		Read and write	Read and write	Read and write	
protect level	Boot mode / Perform user / Access to areas	SRAM				Changing a Protection Level
		JTAG/SWD	Main Flash	System Memory	SRAM	
L0 level	Before 4KB of flash main memory area	Read-write-erase	Read-write-erase	Read-write-erase	Read-write-erase	Change to L1 or L2 is allowed
	After 4KB of flash main memory area	Read-write-erase	Read-write-erase	Read-write-erase	Read-write-erase	
	Flash main memory area mass erase	Allow	Allow	Allow	Allow	
	Flash option byte area	Read-write-erase	Read-write-erase	Read-write-erase	Read-write-erase	
	Flash system memory area	Prohibit	Prohibit	Read-write-erase	Prohibit	
	SRAM (All)	Read and write	Read and write	Read and write	Read and write	
L1 level	Before 4KB of flash main memory area	Prohibit	Read-only	Read-only	Prohibit	L0 or L2 is allowed. When changed to L0, the main memory area is automatically erased.
	After 4KB of flash main memory area	Prohibit	Read-write-erase	Read-write-erase	Prohibit	
	Flash main memory area mass erase	Allow	Allow	Allow	Allow	
	Flash option byte area	Read-write-erase	Read-write-erase	Read-write-erase	Read-write-erase	

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	Flash system memory area	Prohibit	Prohibit	Prohibit	Prohibit	
	SRAM (All)	Read and write	Read and write	Read and write	Read and write	
L2 level	Before 4KB of flash main memory area	L2 protection level, cannot boot from SRAM				No modification is allowed. JTAG/SWD is banned.
	After 4KB of flash main memory area					
	Flash main memory area mass erase					
	Flash option byte area					
	Flash system memory area					
	SRAM (All)					
protect level	Boot mode	System Memory				Changing a Protection Level
	Perform user / Access to areas	JTAG/SWD	Main Flash	System Memory	SRAM	
L0 level	Before 4KB of flash main memory area	Read-write-erase	Read-write-erase	Read-write-erase	Read-write-erase	Change to L1 or L2 is allowed
	After 4KB of flash main memory area	Read-write-erase	Read-write-erase	Read-write-erase	Read-write-erase	
	Flash main memory area mass erase	Allow	Allow	Allow	Allow	
	Flash option byte area	Read-write-erase	Read-write-erase	Read-write-erase	Read-write-erase	
	Flash system memory	Prohibit	Prohibit	Read-write-erase	Prohibit	

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	area					
	SRAM (All)	Read and write	Read and write	Read and write	Read and write	
L1 level	Before 4KB of flash main memory area	Prohibit	Read-only	Read-only	Read-only	L0 or L2 is allowed. When changed to L0, the main memory area is automatically erased.
	After 4KB of flash main memory area	Prohibit	Read-write-erase	Read-write-erase	Read-write-erase	
	Flash main memory area mass erase	Allow	Allow	Allow	Allow	
	Flash option byte area	Read-write-erase	Read-write-erase	Read-write-erase	Read-write-erase	
	Flash system memory area	Prohibit	Prohibit	Read-write-erase	Prohibit	
	SRAM (All)	Read and write	Read and write	Read and write	Read and write	
L2 level	Before 4KB of flash main memory area	JTAG/SWD interface is disabled.	Read-only	Read-only	Read-only	No modification allowed
	After 4KB of flash main memory area		Read-write-erase	Read-write-erase	Read-write-erase	
	Flash main memory area mass erase		Allow	Allow	Allow	
	Flash option byte area		Read-only	Read-only	Read-only	
	Flash system memory area		Prohibit	Read-write-erase	Prohibit	
	SRAM (All)		Read and write	Read and write	Read and write	

Note: 1. Erase here refers to flash page erase.

3.2.2 iCache

In order to achieve higher system performance, an instruction buffer needs to be added between the high-speed CPU and the low-speed Flash to improve the instruction execution efficiency. Because of the existence of the instruction buffer, the CPU will be able to work at a higher frequency. When the instruction requested by the CPU is in the

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instruction buffer, the CPU can obtain the instruction without delay and realize zero waiting for execution. When the current instruction sequence, instruction prefetch sequence and instruction buffer all miss, Flash will be re-read and the Cache will be backfilled and updated. Accordingly, it is equivalent to storing only the jump header of the program in the Cache.

The main features of the instruction buffer are as follows:

- 8KB iCache.
- Support connection mode: 4WAY.

3.2.2.1 Software interface

- Enable
  - Provide configuration for software to enable/disable iCache. There is no limit to the switching conditions (see the FLASH_AC.ICAHEN bit).
- Reset
  - Provide software to clear the iCache interface, which must be initiated when iCache is closed. Reset and switching cannot be switched at the same time. First, turn off FLASH_AC.ICAHEN, then write 1 to FLASH_AC.ICAHRST, and then turn on FLASH_AC.ICAHEN.
- Lock
  - Cache locking mechanism is supported, and the software configuration puts the program into its designated way. When all the ways are locked, the new data will not be written into the cache. After the software resets the cache, the lock state is automatically cleared.
- Additional remarks
  - Selection of Cache replacement algorithm is not supported.
  - When using icache, there is no WB/WT selection when the CPU writes operation.

3.2.2.2 Register description

FLASH_AC.ICAHEN and FLASH_AC.ICAHRST are the iCache enable switch and iCache data clear switch respectively.

FLASH_CAHR.LOCKSTRT and FLASH_CAHR.LOCKSTOP are the start latch and stop latch of iCache corresponding mode lock, respectively. After iCache is reset, the FLASH_CAHR register automatically returns to the reset value. See for detailed usage method of 3.2.2.3.3 ICache locking.

3.2.2.3 Operating process

3.2.2.3.1 iCache enable and disable

Users can turn on and switch off iCache at any time. If the user program needs to jump between the main memory area and other memory areas, the iCache must be closed and the data of the iCache must be cleared, otherwise, the instruction acquisition error will occur.

3.2.2.3.2 iCache data refresh

The iCache is designed as instruction cache. When the instruction is updated by application software or the instruction jumps between the main memory area and other memory areas, the software must set the FLASH_AC.ICAHRST bit

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to 1 to clear the data in the instruction cache.

Note: FLASH_AC.ICAHRST bit is a write-only bit, and it returns to 0 when read.

3.2.2.3.3 iCache locking

The software controls the FLASH_CAHR register to lock some repeatedly used codes in iCache to improve the efficiency of code execution. iCache module has four latch channels, and the size of each channel is 1/4 of the whole cache. When using a single channel, you must ensure that the amount of code to latch is less than the size of each channel. Otherwise need to use more channels to latch the code. The latch function can be used according to the following control flow:

1. Set FLASH_CAHR.LOCKSTRT[0] to 1;
2. Execute function 1 that needs to be locked in channel 0 (the code amount of function 1 should be less than the size of a single channel);
3. Set FLASH_CAHR.LOCKSTOP[0] to 1 after the function 1 is executed;
4. Then set FLASH_CAHR.LOCKSTRT[1] to 1;
5. Execute function 2 that needs to be locked in channel 1 (the code amount of function 2 should be less than the size of a single channel);
6. After the function 2 is executed, set FLASH_CAHR.LOCKSTOP[1] to 1;

Attention: 1. when the channel is latched, the register operation must follow a fixed process -First set FLASH_CAHR.LOCKSTRT then set FLASH_CAHR.LOCKSTOP;

2. The order of channel latch must be 0~3, otherwise it will reduce the execution efficiency.

3.2.3 SRAM

SRAM is mainly used for code operation to store variables and data or stacks during program execution. The maximum capacity is 128KB.

SRAM supports read-write access of byte, half-word and word.

SRAM supports code running (supports access of SBus, ICode and DCode), and can run programs at full speed in SRAM. The maximum address range of SRAM is 0x2000 0000~0x2001 FFFF.

SRAM data cannot be retained in Stop2, Standby and VBAT modes; data in other working modes (Run/Sleep/Stop0) can be retained normally.

The main features are as follows:

- The maximum capacity is 128KB in total.
- Support byte/half-word/word reading and writing
- I/D/S/DMA1/MDA2/ETH can be accessed.
- I/D BUS can run programs at full speed from Remap to SRAM.

3.2.4 R-SRAM（Retention SRAM）

R-SRAM is also mainly used for code operation, storing variables and data or stacks during program execution, with

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a total capacity of 16KB. The bus address of R-SRAM and SRAM are connected continuously. In application, SRAM and R-SRAM can be treated as a piece of SRAM. In the maximum case, the physical address of R-SRAM No.0 corresponds to the bus start address of 0x2002 0000, and the corresponding bus address range is 0x2002 0000~0x2002 3FFF. R-SRAM supports read and write access of bytes, half words and words, and supports access to SBus, DMA1, DMA2, and ETH.

Because the bus address of R-SRAM is continuously connected to SRAM, and for different product models, the capacity of SRAM available for effective use is different, so for different product models, the bus start address of R-SRAM are different.

R-SRAM supports Retention, which can retain data in VBAT and Standby modes (can be configured to retain or not retain); other working modes (RUN/SLEEP/STOP0/STOP2) data can be retained by default; PWR is required to control and manage its Retention.

Table 3-6 SRAM Capacity Configuration Table

SRAM capacity	R-SRAM capacity	SRAM bus address range	R-SRAM bus address range
64KB	16KB	0x2000 0000~0x2000 FFFF	0x2001 0000~0x2001 3FFF
128KB	16KB	0x2000 0000~0x2001 FFFF	0x2002 0000~0x2002 3FFF

The main features of R-SRAM are as follows:

- The total capacity is 16KB(Supports parity check and needs to be initialized before use)
- Byte/halfword/word read and write
- SBus/DMA1/DMA2/ETH can be accessed
- The bus start address is continuously connected to the main memory SRAM
- The bus start address changes with the main memory SRAM capacity
- Retention is possible, data still needs to be retained in stop2 and standby modes (can be configured not to retain)

3.2.5 FLASH register

These peripheral registers must be operated as words (32 bits).

3.2.5.1 FLASH register overview

Table 3-7 FLASH register overview

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
000h	FLASH_AC	Reserved																								ICAHEN	ICAHRST	PRFTBFS	PRFTBFE	Reserved	LATENCY		
	Reset Value																									0	0	1	1		0	0	0
004h	FLASH_KEY	FKEY																															
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
008h	FLASH_OPTKEY	OPTKEY																															
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
00Ch	FLASH_STS	Reserved																								ECCERR	EVERR	EOP	WRPERR	PVERR	PGERR	RDKEYERR	BUSY
	Reset Value																									0	0	0	0	0	0	0	0

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Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
010h	FLASH_CTRL	Reserved																		ECCERRITE	EOPITE	FERRITE	ERRITE	OPTWE	SMPSEL	LOCK	START	OPTER	OPTPG	Reserved	MER	PER	PG
	Reset Value																			0	0	0	0	0	0	1	0	0	0		0	0	0
014h	FLASH_ADD	FADD																															
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
018h	Reserved																																
01Ch	FLASH_OB	RDPRT2	Reserved						Data1								Data0								Not Used					nRST_STDBY	nRST_STOP	WDG_SW	RDPRT1	OBERR
	Reset Value	0						1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0
020h	FLASH_WRP	WRPT																															
	Reset Value	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
024h	FLASH_ECC	Reserved																		ECCHW						Reserved		ECCLW					
	Reset Value																			0	0	0	0	0	0		0	0	0	0	0	0	0
028h	Reserved																																
02Ch	FLASH_RDN	Reserved							FLASH_RDN1									Reserved								FLASH_RDN0							
	Reset Value								0	0	0	0	0	0	0	0	0									0	0	0	0	0	0	0	0	0
030h	FLASH_CAH	Reserved																								LOCKSTOP					LOCKSTRT		
	Reset Value																									0	0	0	0	0	0	0	0

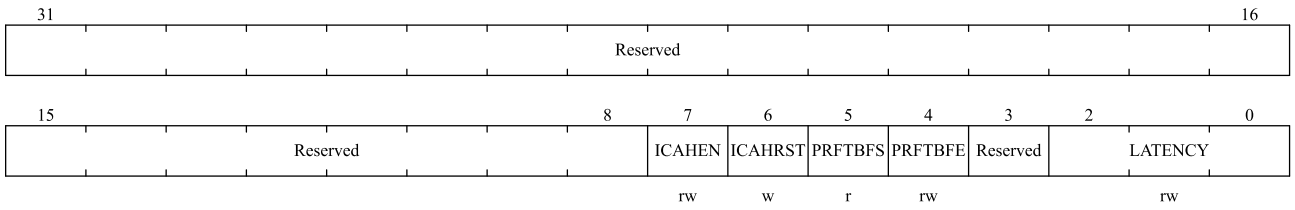
3.2.5.2 FLASH control and status register

See for abbreviations in register descriptions 1.1 section.

3.2.5.2.1 The FLASH access control register (FLASH_AC)

Address offset: 0x00

Reset value: 0x0000 0030



Bit field	Name	Description
31:8	Reserved	Reserved, the reset value must be maintained.
7	ICAHEN	iCache enable 0: turn off iCache; 1: enable iCache.
6	ICAHRST	iCache reset 0: writing '0' is invalid; 1: write '1' to reset.
5	PRFTBFS	Prefetch buffer status

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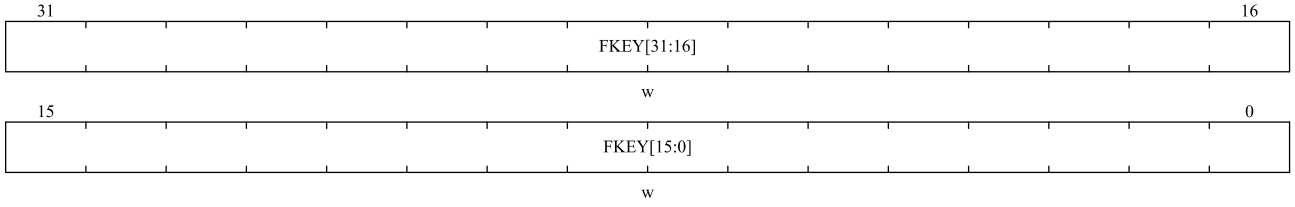
Bit field	Name	Description
		This bit indicates the status of the prefetch buffer 0: The prefetch buffer is closed; 1: The prefetch buffer is open.
4	PRFTBFE	Prefetch buffer enable 0: Close the prefetch buffer; 1: Enable prefetch buffer.
3	Reserved	Reserved, the reset value must be maintained.
2:0	LATENCY	time delay These bits represent the ratio of SYSCLK (system clock) period to flash memory access time. 000: zero period delay, when 0 < SYSCLK <=32MHz 001: one cycle delay, when 32MHz < SYSCLK <=64MHz 010: two cycle delay, when 64MHz < SYSCLK <=96MHz 011: three cycle delay, when 96MHz < SYSCLK <= 128MHz 011: three cycle delay, when 128MHz < SYSCLK <= 144MHz Other values: reserved

3.2.5.2.2 The FLASH key register (FLASH_KEY)

Address offset: 0x04

Reset value: 0xXXXX XXXX

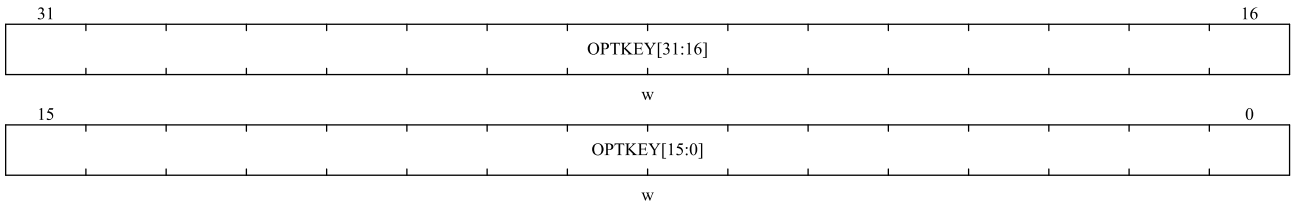


Bit field	Name	Description
31:0	FKEY	Used to unlock the FLASH_CTRL.LOCK bit.

3.2.5.2.3 The FLASH OPTKEY register (FLASH_OPTKEY)

Address offset: 0x08

Reset value: 0xXXXX XXXX



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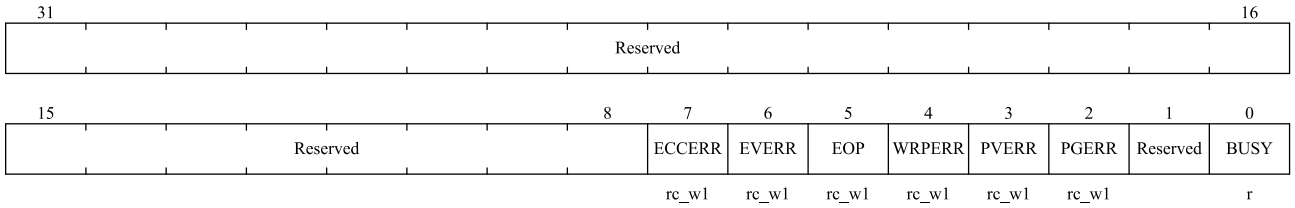
Bit field	Name	Description
31:0	OPTKEY	Used to unlock the FLASH_CTRL.OPTWE bit.

3.2.5.2.4 The FLASH status register (FLASH_STS)

Address offset: 0x0C

Reset value: 0x0000 0000



Bit field	Name	Description
31:8	Reserved	Reserved, the reset value must be maintained.
7	ECCERR	ECC error Read FLASH error, hardware set this bit to '1', write '1' to clear this state.
6	EVERR	Erase check error When the page is erased and the check reports an error, the hardware sets this bit to '1', and writing '1' can clear this state.
5	EOP	End of operation When the flash operation (programming/erasing) is completed, the hardware sets this bit to '1', and writing '1' can clear this bit status. *Note: Every successful programming or erasing will set the EOP state.*
4	WRPERR	Write protection error When trying to program a write-protected flash address, the hardware sets this bit to '1', and writing '1' can clear this bit.
3	PVERR	programming verification error When an error is reported during verification after programming, the hardware sets this bit to '1', and writing '1' can clear this state.
2	PGERR	Programming error When trying to program an address whose content is not '0xFFFF_FFFF', the hardware sets this bit to '1', and writing '1' can clear this state. *Note: Before programming, the FLASH_CTRL.START bit must be cleared.*
1	Reserved	Reserved, the reset value must be maintained.
0	BUSY	Busy This bit indicates that a flash operation is in progress. At the beginning of flash operation, this bit is set to '1'; This bit is cleared to '0' when the operation ends or an error occurs.

3.2.5.2.5 The FLASH control register (FLASH_CTRL)

Address offset: 0x10

Reset value: 0x0000 0080

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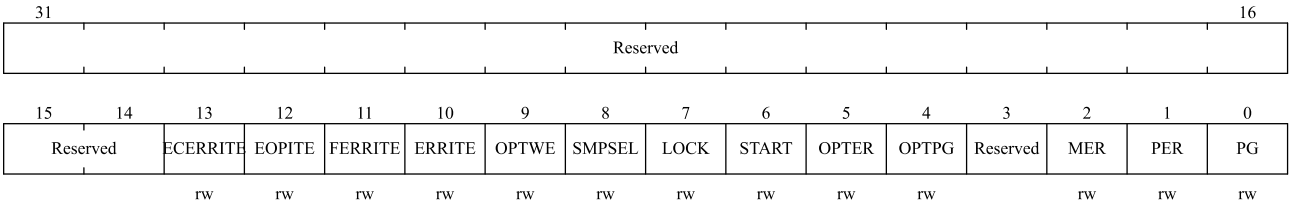

Bit field	Name	Description
31:14	Reserved	Reserved, the reset value must be maintained.
13	ECERRITE	ECC error interrupt This bit allows an interrupt to be generated when the FLASH_STS.ECCERR bit goes to '1'. 0: Interrupt generation is prohibited; 1: Enable interrupt generation.
12	EOPITE	Allow operation completion interrupt. This bit allows an interrupt to be generated when the FLASH_STS.EOP bit becomes '1'. 0: interrupt generation is prohibited; 1: interrupt generation is allowed.
11	FERRITE	Erase/Program Verify Error Interrupt This bit allows an interrupt to be generated when the FLASH_STS.EVERR/PVERR bit goes to '1'. 0: Interrupt generation is prohibited; 1: Enable interrupt generation.
10	ERRITE	Error status interrupt allowed This bit allows an interrupt to be generated when a Flash error occurs (when FLASH_STS.PGERR/ FLASH_STS.WRPERR is set to '1'). 0: interrupt generation is prohibited; 1: interrupt generation is allowed.
9	OPTWE	Allow write option byte When this bit is '1', the option byte is allowed to be programmed. When the correct key sequence is written in the FLASH_OPTKEY register, this bit is set to '1'. Software can clear this bit.
8	SMPSEL	Flash programming mode options 0: SMP1 mode. Before programming, you need to read the content of the address where the programming is located, and check whether it has been erased. If it has not been erased, the programming operation will not be performed, and the FLASH_STS.PGERR warning bit will be set; 1: SMP2 mode. Before programming, it will not judge whether the content of the address where the programming is located has been erased, and the Flash will directly start programming. If the programming address has been written with data before, only the same data can be written when programming the address in SMP2 mode, otherwise the data cannot be guaranteed to be written correctly.
7	LOCK	Lock

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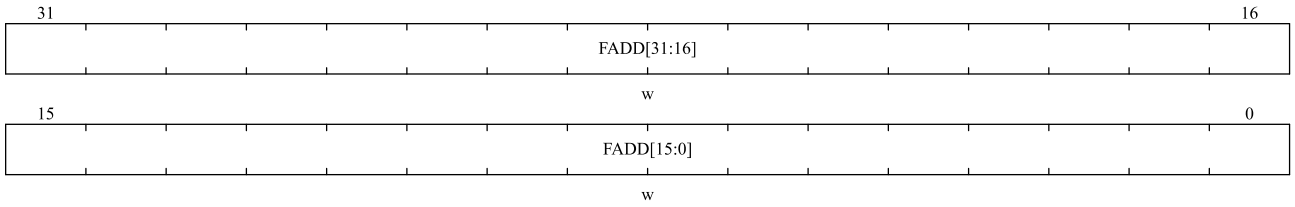
Bit field	Name	Description
		You can only write '1'. When this bit is '1', Flash and FLASH_CTRL are locked. After detecting the correct unlocking sequence, hardware clears this bit to '0'. After an unsuccessful unlocking operation, this bit cannot be changed until the next system reset.
6	START	Start When this bit is '1', an erase operation will be triggered. This bit can only be set to '1' by software and cleared to '0' when FLASH_STS.BUSY becomes '1'.
5	OPTER	Erase option bytes. 0: Disable option bytes erase mode; 1: Enable option bytes erase mode.
4	OPTPG	Program option bytes. 0: Disable option bytes program mode; 1: Enable option bytes program mode.
3	Reserved	Reserved, the reset value must be maintained.
2	MER	Mass erase. 0: disable mass erase mode; 1: enable mass erase mode.
1	PER	Page erase. 0: disable page erase mode; 1: enable page erase mode
0	PG	Program. 0: disable program mode; 1: enable program mode.

Note: Please refer to section 3.2.1.4 for programming and erasing.

3.2.5.2.6 The FLASH address register (FLASH_ADD)

Address offset: 0x14

Reset value: 0x0000 0000



Bit field	Name	Description
31:0	FADD	Flash address Select the address to be programmed when programming, and select the page to be erased when page erasing. *Note: When the FLASH_STS.BUSY bit is '1', this register cannot be written.*

3.2.5.2.7 Option byte register (FLASH_OB)

Address offset: 0x1C

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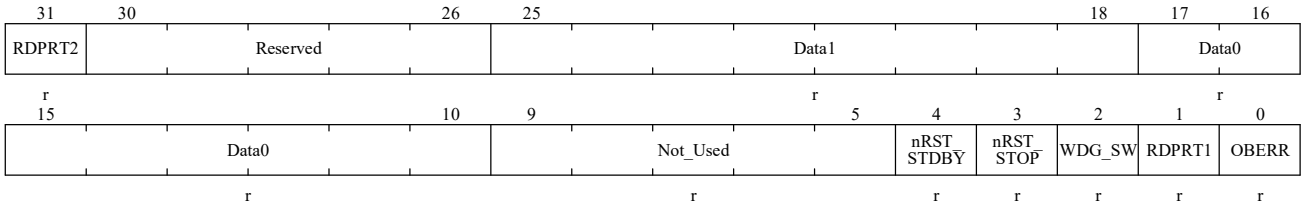
Reset value: 0x03FF FFFC



Bit field	Name	Description
31	RDPRT2	Read protection L2 level protection 0: Read protection L2 level is not enabled; 1: Read protection L2 level is enabled. *Note: This bit is read-only.*
30:26	Reserved	Reserved, the reset value must be maintained.
25:18	Data1[7:0]	Data1 *Note: This bit is read-only.*
17:10	Data0[7:0]	Data0 *Note: This bit is read-only.*
9:5	Reserved	Not used, the hardware remains at 1.
4	nRST_STDBY	Enter Standby mode reset configuration. 0: Reset immediately after entering Standby mode; 1: No reset occurs after entering Standby mode. *Note: This bit is read-only.*
3	nRST_STOP	Enter STOP0/STOP2 mode reset configuration. 0: Reset occurs immediately after entering STOP0/STOP2 mode; 1: No reset occurs after entering the STOP0/STOP2 mode. *Note: This bit is read-only.*
2	WDG_SW	Set watchdog 0: hardware watchdog; 1: Software watchdog. *Note: This bit is read-only.*
1	RDPRT1	Read protection L1 level protection 0: Read protection L1 level is not enabled; 1: read protection L1 level is enabled. *Note: This bit is read-only.*
0	OBERR	Option byte error When this bit is '1', it means that the option byte does not match its complement. *Note: This bit is read-only.*

3.2.5.2.8 Write protection register (FLASH_WRP)

Address offset: 0x20

Reset value: 0xFFFF FFFF

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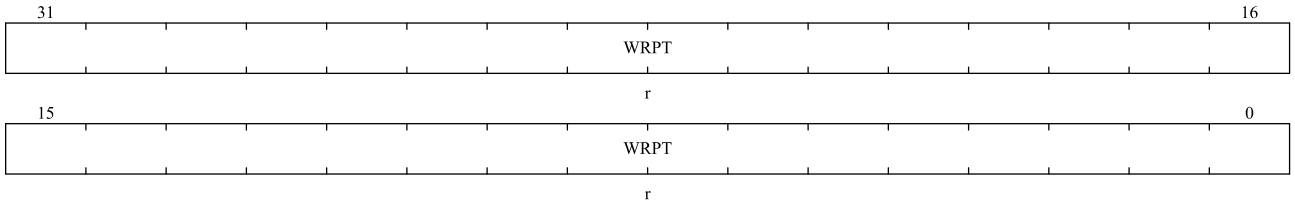
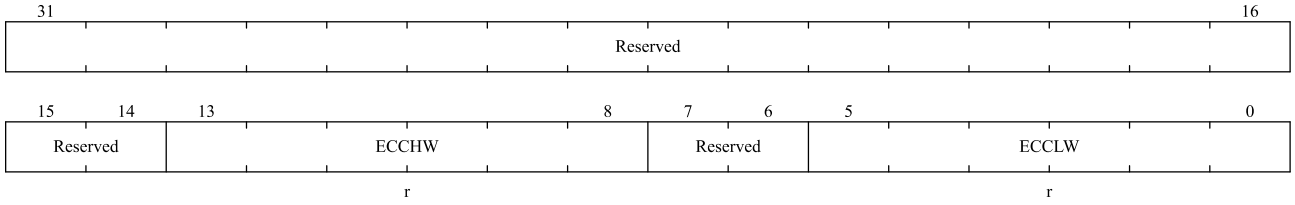


Bit field	Name	Description
31:0	WRPT	Write protect This register contains the write protection option byte loaded by option byte area. 0: write protection takes effect; 1: Write protection is invalid. *Note: These bits are read-only.*

3.2.5.2.9 ECC register（FLASH_ECC）

Address offset: 0x24

Reset value: 0x0000 0000

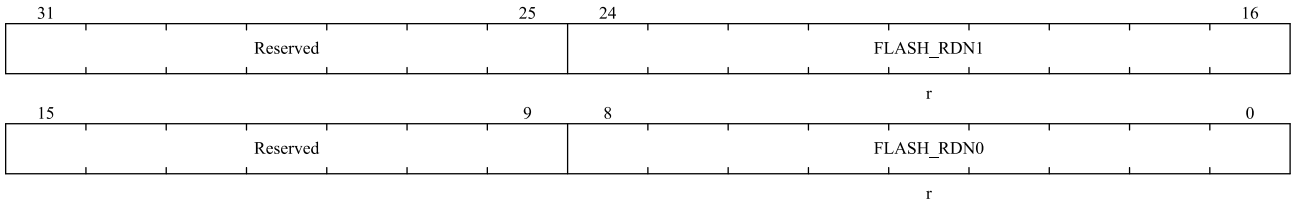


Bit field	Name	Description
31:14	Reserved	Reserved, the reset value must be maintained.
13:8	ECCHW	After writing a word to a 32-bit Flash address, the corresponding higher 6-bit ECC value.
7:6	Reserved	Reserved, the reset value must be maintained.
5:0	ECCLW	After writing a word to a 32-bit Flash address, the corresponding lower 6-bit ECC value.

3.2.5.2.10 RDN register (FLASH_RDN)

Address offset：0x2C

Reset value：0x0000 0000



Bit field	Name	Description
31:25	Reserved	Reserved, the reset value must be maintained.
24:16	FLASH_RDN1	The address of Flash redundant block page 1

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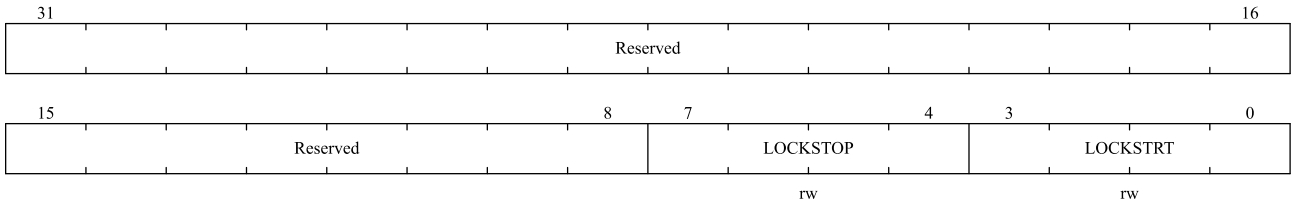
Bit field	Name	Description
15:9	Reserved	Reserved, the reset value must be maintained.
8:0	FLASH_RDN0	The address of Flash redundant block page 0

3.2.5.2.11 CAHR register (FLASH_CAHR)

Address offset: 0x30

Reset value: 0x0000 0000



Bit field	Name	Description
31:8	Reserved	Reserved, the reset value must be maintained.
7:4	LOCKSTOP[3:0]	iCache lock stop (see for detailed operation instructions 3.2.2.3.3 iCache locking_ Chapter). 0: disable 1: enable
3:0	LOCKSTRT[3:0]	iCache lock start. 0: disable 1: enable

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4 Power Control (PWR)

4.1 General Description

PWR is power management unit to control status of different modules in different power modes. Its major function is to control MCU to enter different power modes and wakeup when events or interrupts happen. MCU supports RUN、SLEEP、STOP0、STOP2、STANDBY and VBAT mode.

4.1.1 Power supply

- MCU working voltage (VDD) is 1.8V~3.6V. It mainly has 3 analog/digital power supply regions (VDD, VBAT, VDDA). For details, please refer to Figure 4-1 power supply block diagram. In order to illustrate the functions of different power domains, some power domains will be introduced below, and the digital parts of power domains will be introduced in later chapters of this document.
  - V_{DD} domain: The voltage input range is 1.8V~3.6V, mainly for MR,CPU,AHB,APB,SRAM,FLASH and most digital peripheral interfaces power supply.
  - VBAT domain: The input voltage range is 1.8V~3.6V, which supplies power for BKR and some special IO (PC13, PC14, PC15) ports. When VDD is powered down, the switch switches the power supply system VDD to VBAT.
  - VDDA domain: voltage input range is 1.8V~3.6V, mainly used for clock and reset system, most analog peripherals powered.
- BKR and MR are internal voltage regulators that can provide power for the digital module power supply system. VDD and VBAT are generally powered directly from the outside, VBAT is powered by the battery to keep the contents of the backup area, and VDD is powered by other external power supply systems. In addition, if no battery is required, then VBAT must be connected directly to VDD.
  - **MR**

    MR is the internal main power controller, mainly used in RUN mode, SLEEP mode and STOP0 mode. MR has two modes, normal mode and low power mode, the low power mode is used for STOP0 to further reduce power consumption.

    When the MR enters a low power mode, the CPU goes into a deep sleep state. In this case, the PWR_CTRL.PDS bit should be set to 0 and the PWR_CTRL.LPS bit should be set to 1. When the MR enters the normal mode, the PWR_CTRL.PDS bit needs to be set to 0, and the PWR_CTRL.LPS bit is also 0.
  - **BKR**

    BKR is an internal backup domain power controller, used in STOP2, STANDBY and VBAT modes. In STOP2 mode, the CPU state is maintained and additionally supplies power to the digital backup area, GPIO and EXTI. When the CPU enters deep sleep, the PWR_CTRL2.STOP2S bit should be set to 1 at this time.

    The main modules of the digital backup area include PWR, IO (PA0_WAKUP, PC13_TAMPER, PC14, PC15), R-SRAM, RTC, BKR and RCC_BDCTRL registers. When the SW3 switch is on, the CPU goes into a deep sleep state. When SW1 switches the power supply system to VBAT, it indicates that VDD has

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been powered down at this time.

- When reset, SW1 will switch the power supply system to the VDD power supply area. In STOP2, STANDBY and VBAT modes, the internal voltage regulator BKR will power the digital backup area.
  - During the VDD rising phase or when PDR is detected, the switch between VBAT and VDD remains connected to the VBAT area.
  - During startup, if VDD is settling quickly and VDD > VBAT + 0.6V, current can be injected to VBAT through the internal diode connection. If the power supply connected to VBAT or the battery does not support this injection of current. It is strongly recommended to add a low voltage diode between this supply and the VBAT pin.

  If there is no external battery in the application. It is recommended to connect the VBAT pin to VDD with a 100nF ceramic capacitor. In RUN, SLEEP, STOP0 mode, the backup area is powered by VDD (SW1 is connected to VDD), the following functions are available:
  - PC14 and PC15 can be used for common IO ports or LSE pins
  - PC13 can be used for common IO port, TAMPER pin, RTC check clock pin, RTC alarm and periodic wake-up output

  Notice:

  Due to the fact that the current flowing through SW1 and SW2 is limited to a maximum of 3mA. Therefore, the IO output modes of PA0_WAKUP, PC13 to PC15 are limited. When a 30PF capacitor is attached, the maximum output speed is 2MHz. In addition, these IOs cannot be driven by current, for example, they cannot drive LEDs. The current of SW2 will be maintained at 3mA or lower, because GPIO, and EXTI work together to consume current.

  When VBAT supplies power to the backup area, the following functions can be used at this time:
  - PC14 and PC15 can only be used for LSE pins.
  - PC13 is used for TAMPER pin, RTC alarm or periodic wake-up output

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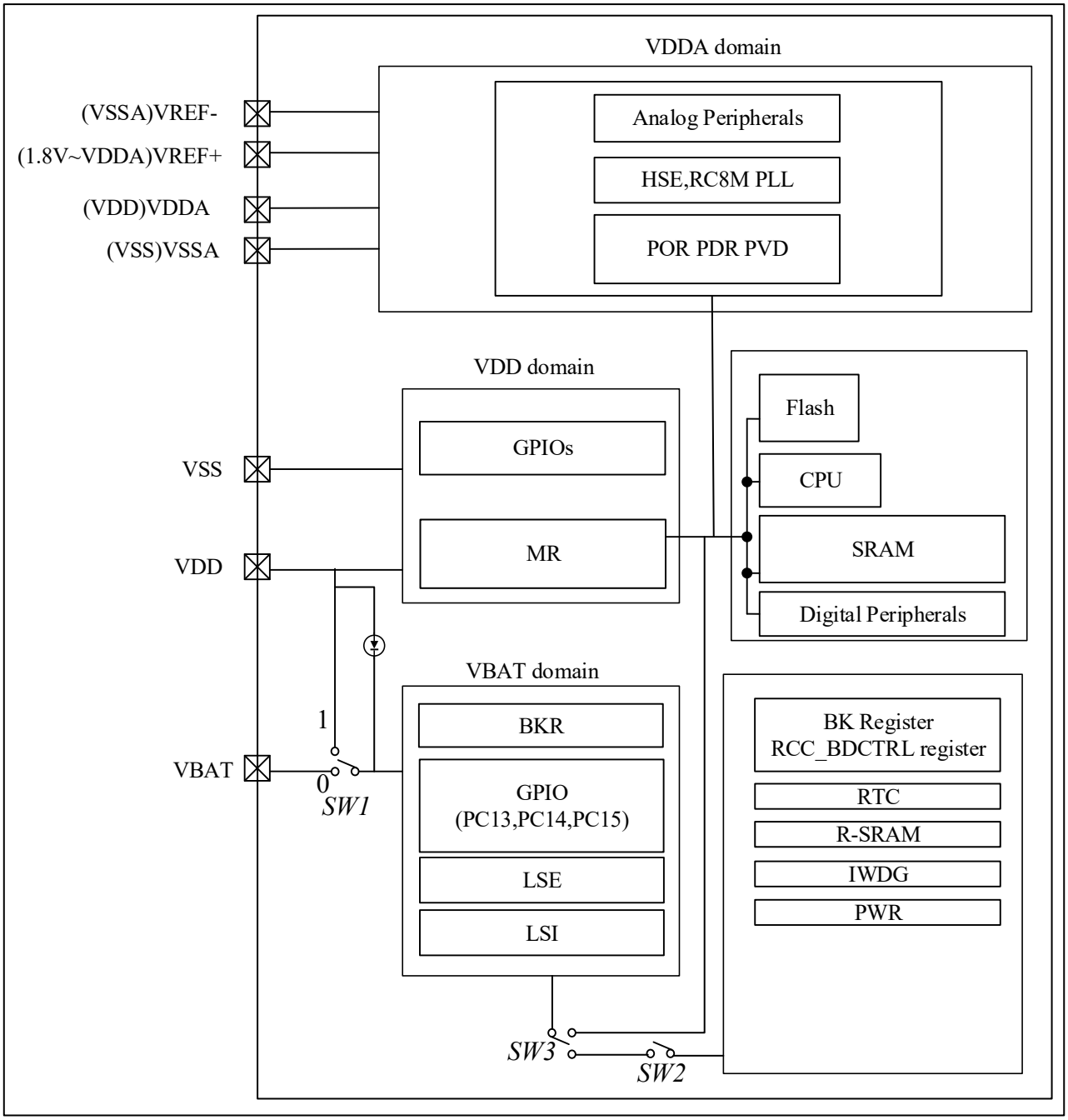
Figure 4-1 Power supply block diagram



4.1.2 Power Supply Supervisor

4.1.2.1 Power on reset (POR) and power down reset (PDR)

Power-on reset (POR) and power down reset (PDR) circuits are integrated inside the chip. Can work with a minimum voltage of 1.8V. No external reset circuit is required. When VDD or VDDA is lower than the specified threshold ($V_{POR/PDR}$), the chip will remain in reset state.

For more information on switching power supply reset thresholds, see the Electrical Characteristics section of the relevant data sheet.

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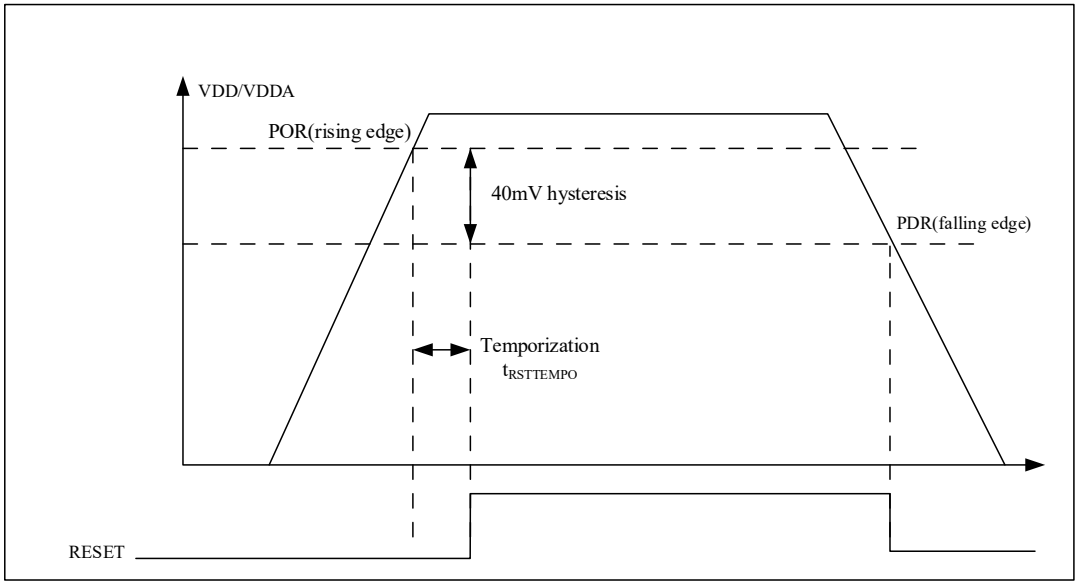
Figure 4-2 Waveforms of power-on reset and power-down reset



4.1.2.2 Programmable voltage detector (PVD)

The PVD can be used to monitor the VDD/VDDA power supply by comparing with the thresholds set by the PWR_CTRL.PRS[2:0] bits of the power supply control register.

The PWR_CTRLSTS.PVDO flag is used to indicate if VDD/VDDA is above/below the PVD voltage threshold. This event is internally connected to the interrupt line 16 of the external interrupt, which will generate an interrupt if enabled in the external interrupt register. Depending on the rising/falling edge trigger settings of the external interrupt line 16, a PVD interrupt will occur when VDD/VDDA falls below the PVD threshold or VDD/VDDA rises above the PVD threshold. For example, this feature can be used to perform emergency shutdown tasks.

Notice: MCU PVD threshold needs to be configured with the PWR_CTRL3.EXMODE bit. For details, please refer to the registers PWR_CTRL.MSB and PWR_CTRL.PRS[2:0], their combination can form a 4-bit PVD threshold configuration.

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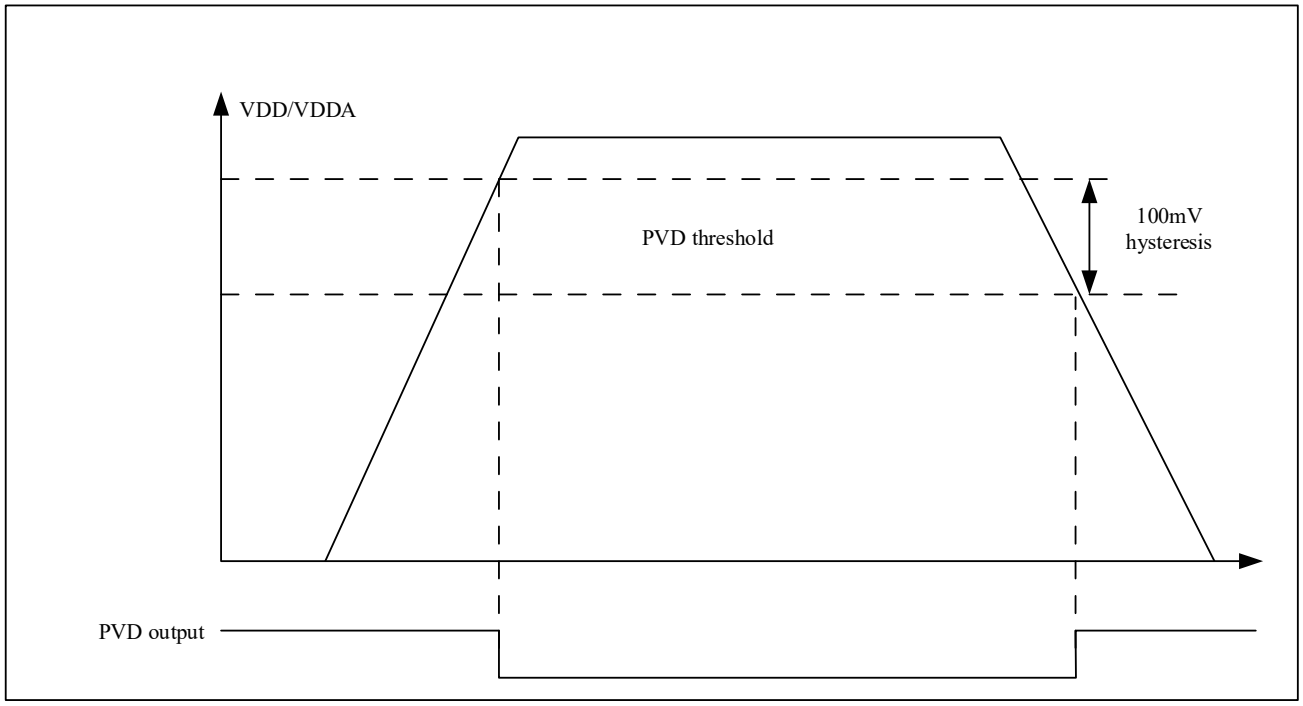
Figure 4-3 PVD threshold waveform



4.1.2.3 Brown_out reset（BOR）

BOR is a power-down reset controller built into the device, when the VDD voltage is lower than 1.62V (typ), the device will remain in reset state.

4.2 Power Modes

Overall MCU has 6 power modes: RUN,SLEEP,STOP0,STOP2,STANDBY and VBAT. Different mode has different performance and power consumption. A summary of MCU power modes is shown below.

Table 4-1 Power modes

Mode	Condition	Enter	Exit
RUN	CPU boot Peripheral configuration	Power on, system reset, low power wake-up	Enter sleep, STOP0, STOP2, standby and VBAT modes
SLEEP	CPU goes to sleep mode and the kernel stops. With all peripherals configured, the voltage regulator is still running. Any interrupt and event can wake up the CPU	1）SCB_SCR.SLEEPDEEP = 0, SCB_SCR.SLEEPONEXIT = 0, WFI/WFE 2）SCB_SCR.SLEEPDEEP = 0, SCB_SCR.SLEEPONEXIT = 1, No interrupt waiting, CPU returns from ISR	wake: 1) If entered via WFI or set SCB_SCR.SLEEPONEXIT = 1, any NVIC interrupt can exit 2) If entered via WFE or set SCB_SCR.SEVONPEND=1, any peripheral interrupt can exit; SCB_SCR.SEVONPEND=0, the external interrupt line exits
STOP0[1]	CPU deep sleep mode: Peripheral clocks, all digital blocks and	WFI / WFE： 1）SCB_SCR.SLEEPDEEP =	wake: 1) If entered by WFI, any from

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Mode	Condition	Enter	Exit
	voltage regulators are still running. HSE/HSI/PLL is turned off. LSE/LSI, RTC or other peripherals can be configured to wake up. All SRAM data retention, all IO ports, IWDG and RTC can be used to wake up the CPU. After waking up, HSI is turned on, and the code starts from where it hangs.	1，PWR_CTRL.PDS＝0， 2）PWR_CTRL.LPS=0/1， Select the main voltage regulator operating mode	external interrupt/event line (NVIC enabled), it can be external interrupt or internal peripheral 2) If entered by WFE, SCB_SCR.SEVONPEND=0, any event line from external 3) If entered by WFE, SCB_SCR.SEVONPEND=1, any interrupt from external or internal peripheral
STOP2[2]	CPU deep sleep mode: CPU registers are maintained, and all core digital logic areas are powered off. The main voltage regulator (MR) is turned off and the HSE/HSI/PLL is turned off. LSE/LSI configurable, GPIO is maintained, and peripheral IO multiplexing is not maintained. 16KB R-SRAM data retention, other SRAM and register data are lost. 84B BK register retention. GPIOs and EXTI are enabled.	WFI/WFE： 1）SCB_SCR.SLEEPDEEP = 1 2）PWR_CTRL2.STOP2S =1	wake: 1) If entered by WFI, any from external interrupt/event line (NVIC enabled), it can be external interrupt or internal peripheral 2) If entered by WFE, SCB_SCR.SEVONPEND=0, any event line from external 3) If entered by WFE, SCB_SCR.SEVONPEND=1, any interrupt from external or internal peripheral
STANDBY	The main voltage regulator is turned off and the HSE/HSI/PLL is turned off. LSE/LSI is configurable. 16KB bytes of R-SRAM retention, configured through PWR_CTRL2.SR2STBRET. Other SRAM and register data are lost. Except for the following NRST/PA0_WKUP/PC13-TAMPER/PC14-OSC32_IN/PC15-OSC32_OUT, other IOs are high impedance. The 84-byte BK register data retention, IWDG, RTC/PA0WKUP/NRST/TAMPER can wake up the CPU.	WFI/WFE： 1）SCB_SCR.SLEEPDEEP = 1 interrupt/event 2）PWR_CTRL.PDS=1	WKUP rising edge, RTC alarm rising edge, NRST reset, IWDG reset
VBAT	CPU off, all peripherals off, main voltage regulator off, LSE/LSI configurable, HSE/HSI/PLL off. Except for NRST/PC13-TAMPER/PC14-OSC32_IN/PC15-OSC32_OUT, most IO ports are in high impedance state.	VDD disable	VDD enable

Note:

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1. *STOP0 mode, after wake-up, the code can continue running from the stop position.*
2. *In STOP2 mode, after waking up, the heap and global variables in the R-SRAM area can resume and continue from the stopped position, and the peripherals need to be re-initialized at this time.*

The running enable conditions of different modules in different power consumption modes are shown in the following table:

Table 4-2 Blocks running state(1)

Peripheral	Run	Sleep	Stop 0		Stop 2		Standby		VBAT
			-	Wakeup capability	-	Wakeup capability	-	Wakeup capability	
MR	Y	Y	(3)	-	OFF	-	OFF	-	OFF
BKR	Y	Y	Y	-	Y	-	Y	-	Y
POR	Y	Y	Y	-	Y	-	Y	Y	
PDR	Y	Y	Y	-	Y	-	Y	Y	-
PVD	O	O	O	O	O	O	-	-	-
BKPOR/PDR	Y	Y	Y	-	Y	-	Y	-	Y
CPU	Y	HCLK （O）	HCLK（O）	-	-	-	OFF	-	OFF
Flash	O	O	(4)	-	OFF	-	OFF	-	OFF
SRAM	Y	Y	Y	-	OFF	-	OFF	-	OFF
R-SRAM	Y	O	Y	-	O	-	O	-	O
Backup Registers	Y	Y	Y	-	Y	-	Y	-	Y
DMA	O	O	-	-	-	-	-	-	-
HSI	O	O	OFF	-	OFF	-	OFF	-	OFF
HSE	O	O	OFF	-	OFF	-	OFF	-	OFF
LSI	O	O	O	-	O	-	O	-	O
LSE	O	O	O	-	O	-	O	-	O

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Peripheral	Run	Sleep	Stop 0		Stop 2		Standby		VBAT
			-	Wakeup capability	-	Wakeup capability	-	Wakeup capability	
CSS	O	O	-	-	-	-	-	-	-
RTC / Auto wakeup	O	O	O	O	O	O	O	O	O
Number of RTC Tamper pins	1	1	1	O	1	O	1	O	1
USART1/2/3	O	O	-	-	-	-	-	-	-
UART4/5/6/7	O	O	-	-	-	-	-	-	-
I2C1/2/3/4	O	O	-	-	-	-	-	-	-
SPI1/2/3	O	O	-	-	-	-	-	-	-
CAN1/2	O	O	-	-	-	-	-	-	-
USB	O	O	-	-	-	-	-	-	-
ETH MAC	O	O	-	-	-	-	-	-	-
QSPI	O	O	-	-	-	-	-	-	-
SDMMC	O	O	-	-	-	-	-	-	-
ADC	O	O	-	-	-	-	-	-	-
DAC	O	O	-	-	-	-	-	-	-
OPAMP	O	O	-	-	-	-	-	-	-
COMP	O	O	O	O	-	-	-	-	-
DVP	O	O	-	-	-	-	-	-	-
Tempsensor	O	O	-	-	-	-	-	-	-
TIMx	O	O	-	-	-	-	-	-	-
IWDG	O	O	O	O	O	O	O	O	-

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Peripheral	Run	Sleep	Stop 0		Stop 2		Standby		VBAT
			-	Wakeup capability	-	Wakeup capability	-	Wakeup capability	
WWDG	O	O	-	-	-	-	-	-	-
SysTick	O	O	-	-	-	-	-	-	-
SAC	O	O	-	-	-	-	-	-	-
RNG	O	O	-	-	-	-	-	-	-
CRC	O	O	-	-	-	-	-	-	-
GPIOs	O	O	O	O	O	O	Y	2pins	-

Note:

1. *Y means Yes (enable), O means Option (optional), - means invalid, OFF means close,*
2. *2pins represent 2 wakeup IOs, PA0_WKUP and NRST*
3. *MR can select to work in normal mode or in low power mode*
4. *FLASH is in sleep (Flash itself) mode.*

4.2.1 SLEEP mode

The CPU stops and all peripherals including peripherals around the Cortex®-M4F core (such as NVIC, SysTick, etc.) can run and wake up the CPU when an interrupt or event occurs. In SLEEP mode, all I/O pins maintain the same state/function as in RUN mode.

4.2.1.1 Enter SLEEP mode

Enter SLEEP mode by executing WFI (wait for interrupt) or WFE (wait for event) instruction with SCB_SCR.SLEEPDEEP = 0. Depending on the SCB_SCR.SLEEPONEXIT, there are two options for SLEEP mode entry:

- SLEEP-NOW: If SCB_SCR.SLEEPONEXIT = 0, then WFI or WFE instruction is executed immediately, and the system enters sleep mode immediately.
- SLEEP-ON-EXIT: If SCB_SCR.SLEEPONEXIT = 1, the system immediately enters sleep mode when exiting from the lowest priority ISR.

In SLEEP mode, all I/O pins maintain the same state/function as in RUN mode.

4.2.1.2 Exit SLEEP mode

If WFI instruction is used to enter the SLEEP mode, any NVIC interrupts can wake up the device from the SLEEP mode.

If the WFE instruction is used to enter the SLEEP mode, MCU will exit the SLEEP mode immediately when the

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event occurs. Wake-up events can be generated in the following ways:

- Enable an interrupt in the peripheral control register instead of NVIC, and enable the SCB_SCR.SEVONPEND. When MCU wakes up by WFE, the peripheral interrupt suspend bit and the peripheral NVIC interrupt channel suspend bit (in NVIC interrupt clear suspend register) must be cleared.
- Configure an external or internal EXTI event mode. When the MCU wakes up, it is not necessary to clear the peripheral interrupt suspend bit and the peripheral NVIC interrupt channel suspend bit (in the NVIC interrupt clear suspend register) because the suspend bit corresponding to the event line is not set. This mode provides the shortest wake-up time because there is no time spent on interrupt entry or exit.

4.2.2 STOP0 mode

STOP0 mode is based on Cortex®-M4 deep sleep mode combined with peripheral clock control mechanism. The voltage regulator can be configured in normal or low power mode. In STOP0 mode, most of the clock sources in the core domain are disabled, such as PLL, HSI and HSE. But SRAM, R-SRAM and all register contents are preserved.

In STOP0 mode, all I/O pins maintain the same state as in RUN mode.

4.2.2.1 Enter STOP0 mode

When entering STOP0 mode, the main difference is to set SCB_SCR.SLEEPDEEP=1, PWR_CTRL.PDS=0. Another difference is that MR can run in normal mode or low power mode by configuring register PWR_CTRL.LPS. When PWR_CTRL.LPS = 1, MR runs in low power mode.

When PWR_CTRL.LPS = 0, MR operates in normal mode.

In STOP0 mode, all I/O pins maintain the same state and function as in RUN mode.

If a FLASH operation is in progress, the time to enter STOP0 mode will be delayed until the memory access is completed.

If an access to the APB area is in progress, the time to enter STOP0 mode will be delayed until the APB access is complete.

In STOP0 mode, the following characteristics can be selected by programming the individual control bits:

- Independent watchdog (IWDG): The independent watchdog will be activated when its related registers are written by software or operated by hardware. Once activated, it will keep working until a reset message is generated.
- RTC: can be turned on by register RCC_BDCTRL.RTCEN bit
- Internal RC oscillator (LSI RC): can be turned on by register RCC_CTRLSTS.LSIEN bit
- External 32.768kHz crystal oscillator (LSE OSC): can be turned on by register RCC_BDCTRL.LSEEN.

ADC or DAC can also consume power in STOP0 mode, ADC and DAC can be disabled before entering STOP0 mode.

Note: If the application needs to disable the external clock before entering stop mode, it must first disable the RCC_CTRL.HSEEN bit and then switch the system clock to HSI. Otherwise, if the RCC_CTRL.HSEEN bit remains enabled when entering stop mode and the external clock (external oscillator) is removed, the Clock Safety System (CSS) feature must be enabled to detect any external oscillator failure and avoid entering stop Failed behavior when

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mode.

4.2.2.2 Exit STOP0 mode

When an interrupt or wake-up event is generated to exit STOP0 mode, the HSI RC oscillator is selected as the system clock.

When the voltage regulator is operating in low power mode, there is an additional startup delay when waking up from STOP0 mode. In STOP0 mode, the internal regulator is in normal mode, which can reduce the startup time, but the corresponding power consumption will increase.

4.2.3 STOP2 mode

STOP2 mode is based on Cortex®-M4F deep sleep mode, all core digital logic areas are powered off. The main voltage regulator (MR) is turned off and the HSE/HSI/PLL is turned off. CPU register retention, LSE/LSI configurable, GPIO retention, peripheral IO multiplexing is not retained. 16K bytes R-SRAM retention, other SRAM and register data are lost. 84 bytes of backup register retention. GPIOs and EXTI enabled.

4.2.3.1 Enter STOP2 mode

To enter STOP2 mode, should be configured: SCB_SCR.SLEEPDEEP = 1, PWR_CTRL2.STOP2S = 1, PWR_CTRL.PDS = 0, PWR_CTRL.LPS = 0.

In STOP2 mode, if FLASH is being operated, the time to enter STOP2 mode will be delayed until the memory access is completed.

If the access to the APB area is in progress, the time to enter the STOP2 mode will be delayed until the APB access is completed.

In STOP2 mode, the following peripherals are available:

- Independent Watchdog (IWDG) optional: Once enabled, it will keep counting until a reset is generated.
- RTC optional: It can be turned on by RCC_BDCTRL.RTCEN.
- Internal RC oscillator (LSI RC) optional: It can be turned on by RCC_CTRLSTS.LSIEN.
- External 32.768kHz crystal oscillator (LSE OSC) optional: It can be turned on by RCC_BDCTRL.LSEEN bit.

Note: If you want to keep data (global variables, stack, etc.) when entering STOP2, you should put it in R-SRAM.

4.2.3.2 Exit STOP2 mode

When the STOP2 mode is exited by generating an interrupt or a wake-up event, the HSI RC oscillator is selected as the system clock, and the code execution will continue from where it stopped.

4.2.4 STANDBY mode

STANDBY mode is a Cortex®-M4 based Deep-Sleep mode. The core domain is completely closed, and the backup region is open to supply power to BKR.

4.2.4.1 Enter STANDBY mode

When entering STANDBY mode. The main difference is to set SCB_SCR.SLEEPDEEP=1, PWR_CTRL.PDS=1.

In STANDBY mode, all I/O pins remain high impedance except NRST, PA0_WKUP, PC13_TAMPER, PC14, PC15.

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If an operation is in progress on FLASH, the time to enter STANDBY mode will be delayed until the memory access is complete.

If an access to the APB area is in progress, the time to enter STANDBY mode will be delayed until the APB access is complete.

In STANDBY mode, the following features can be selected by programming individual control bits:

- Independent Watchdog (IWDG) optional: Once enabled, it will keep counting until a reset is generated.
- RTC optional: It can be turned on by RCC_BDCTRL.RTCEN.
- Internal RC oscillator (LSI RC) optional: It can be turned on by RCC_CTRLSTS.LSIEN.
- External 32.768kHz crystal oscillator (LSE OSC) optional: It can be turned on by RCC_BDCTRL.LSEEN bit.
- R-SRAM data retention, which can be turned on by register PWR_CTRL2.SR2STBRET.

4.2.4.2 Exit STANDBY mode

MCU exits STANDBY mode when an external reset (NRST pin), IWDG reset, rising edge of the WKUP pin, or a rising edge of the RTC alarm event occurs. Except for the power status register (PWR_CTRLSTS), all registers are reset after waking up from STANDBY state.

After waking up from STANDBY mode, code execution is the same as reset (detecting BOOT pin, getting reset vector, etc.). The PWR_CTRLSTS.SBF status flag indicates that the MCU exits STANDBY mode.

4.2.5 VBAT mode

In VBAT mode the CPU is turned off, all peripherals are turned off, the main voltage regulator is turned off, the LSE/LSI is configurable, and the HSE/HSI/PLL is turned off. Except for NRST/PC13-TAMPER/PC14-OSC32_IN/PC15-OSC32_OUT, most IO ports are in high impedance state.

In VBAT mode, depending on the configuration before VDD is powered down, the following features are available:

- RTC optional: It can be turned on by RCC_BDCTRL.RTCEN.
- Internal RC oscillator (LSI RC) optional: It can be turned on by RCC_CTRLSTS.LSIEN.
- External 32.768kHz crystal oscillator (LSE OSC) optional: It can be turned on by RCC_BDCTRL.LSEEN bit.
- R-SRAM data retention, which can be turned on by register PWR_CTRL2.SR2STBRET.

4.2.5.1 Enter VBAT mode

When VDD is powered down, it will enter VBAT mode at any time.

4.2.5.2 Exit VBAT mode

When VDD returns to the power-on reset threshold, the MCU exits VBAT mode. After VDD is restored, the core area of the MCU will be completely executed according to the power-on sequence. After waking up from VBAT mode, code execution is identical to execution after reset. The PWR_CTRLSTS.VBATF status flag indicates that the MCU exits from VBAT mode.

4.3 Low-power Auto-wakeup（AWU）Mode

In automatic wake-up mode, the RTC can be used to wake up from different low-power modes without relying on

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external interrupts. The RTC provides a programmable clock reference for timed wake-up from STOP0, STOP2 and STANDBY modes. To do this, two of the three optional RTC clock sources can be selected by software programming RCC_BDCTRL.RTCSEL[1:0] as follows:

- 32.768kHz external crystal clock (LSE OSC)

  This clock source provides an accurate clock reference with very low power consumption.

- RC internal crystal clock (LSI RC)

  This clock source has the advantage of saving the cost of the 32.768 kHz crystal, but the clock accuracy is worse than the LSE.

To wake up from STOP2 mode using the RTC alarm event, you need:

- Configure EXTI 17 rising edge trigger.
- Configure RTC to enable RTC alarm event.

To wake up from STANDBY mode using RTC alarm event, EXTI 17 does not need to be configured.

VBAT mode cannot wake up via RTC.

4.4 PWR Registers

4.4.1 PWR Register Overview

Table 4-3 PWR register overview

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
000h	PWR_CTRL	Reserved																						MSB	DBKP	PRS[2:0]			PVDEN	CSBYBAT	CWKUP	PDS	LPS
	Reset Value																							0	0	0	0	0	0	0	0	0	0
004h	PWR_CTRLSTS	Reserved																							WKUPEN	Reserved				VBATF	PVDO	SBF	WKUPF
	Reset Value																								0					0	0	0	0
008h	PWR_CTRL2	Reserved																					IWDGRSTEN	IWDGWPEN	LSITRIM[4:0]					TMPWPEN	SR2STBRET	SR2VBRET	STOP2S
	Reset Value																						1	1	0	1	1	1	0	0	1	0	0
00Ch	PWR_CTRL3	Reserved																															EXMODE
	Reset Value																																0

4.4.2 Power Control Register (PWR_CTRL)

Address offset: 0x00

Reset value: 0x0000 0700 (reset by wakeup from STANDBY mode)

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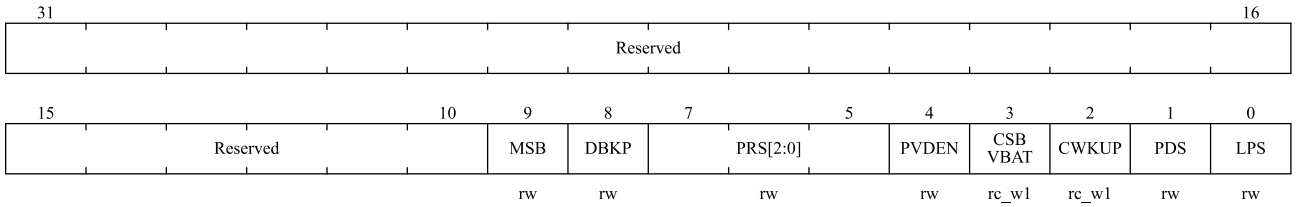

Bit field	Name	Description
31:10	Reserved	Reserved, the reset value must be maintained.
9	MSB	4-bit PVD threshold setting bits. This bit is operational when PWR_CTRL3.EXMODE = 1. Therefore, the PWR_CTRL3.EXMODE bit needs to be configured first. When the MSB bit is 0, the threshold is as follows: register(4bits) / Voltage 0000 / 2.2v 0001 / 2.3v 0010 / 2.4v 0011 / 2.5v 0100 / 2.6v 0101 / 2.7v 0110 / 2.8v 0111 / 2.9v When the MSB bit is 1, the threshold is as follows: register(4bits) / Voltage 1000 / 1.78v 1001 / 1.88v 1010 / 1.98v 1011 / 2.08v 1100 / 3.28v 1101 / 3.38v 1110 / 3.48v 1111 / 3.58v
8	DBKP	Cancel the write protection of the backup power domain. In the reset state, the RTC and backup domain registers should be protected to prevent illegal writing. This bit must be set to enable write access to these registers. 0: Disable access to RTC and backup registers 1: Enable access to RTC and backup registers *Note: This bit must remain 1 if the RTC clock is HSE/128.*
7:5	PRS[2:0]	PVD monitoring voltage selection. Combinations of different bits represent different voltage thresholds of the voltage detector. These bits need to be configured in conjunction with the MSB bit. For specific voltage thresholds, see the description of the MSB bit. *NOTE: See the Electrical Characteristics section in the datasheet for detailed*

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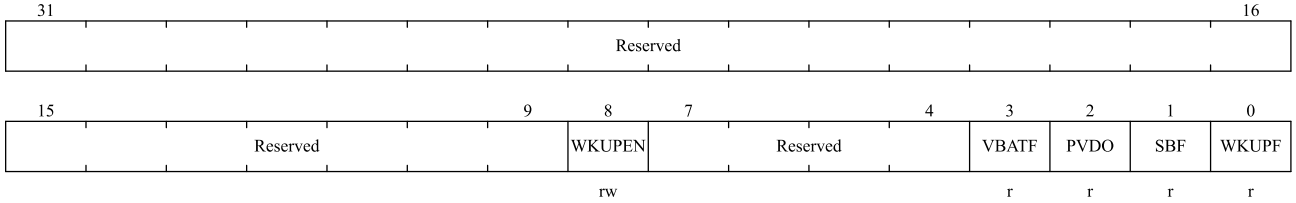
Bit field	Name	Description
		descriptions.
4	PVDEN	Power supply voltage monitor (PVD) enabled. 0: Disable PVD 1: Enable PVD
3	CSBVBAT	Clear STANDBY/VBAT bit. always reads as 0 0: invalid 1: Clear PWR_CTRLSTS.SBF and PWR_CTRLSTS.VBATF standby bits (write)
2	CWKUP	Clear wakeup bit. always reads as 0 0: invalid 1: Clear PWR_CTRLSTS.WKUPF wake-up bit after 2 system clock cycles (write)
1	PDS	Power-down deep-sleep bit. Operates in conjunction with the LPS bit 0: Enters shutdown mode when the CPU enters deep sleep, the state of the voltage regulator is controlled by the LPS bit. 1: Enter standby mode when the CPU enters deep sleep.
0	LPS	Low power consumption in deep sleep. When PDS=0, cooperate with the PDS bit 0: Voltage regulator on in shutdown mode 1: Voltage regulator in low power mode in shutdown mode

4.4.3 Power Control Status Register(PWR_CTRLSTS)

Address offset: 0x04

Reset value: 0x0000 0000 (not cleared when waking up from standby mode)



Bit field	Name	Description
31:9	Reserved	Reserved, the reset value must be maintained.
8	WKUPEN	Enable WKUP pin bit 0: The WKUP pin is a general purpose I/O. An event on the WKUP pin cannot wake the CPU from standby mode 1: WKUP pin is used to wake up CPU from standby mode, WKUP pin is forced to input pull-down configuration (rising edge on WKUP pin wakes up system from standby mode) *Note: This bit is cleared on system reset.*
7:4	Reserved	Reserved, the reset value must be maintained.

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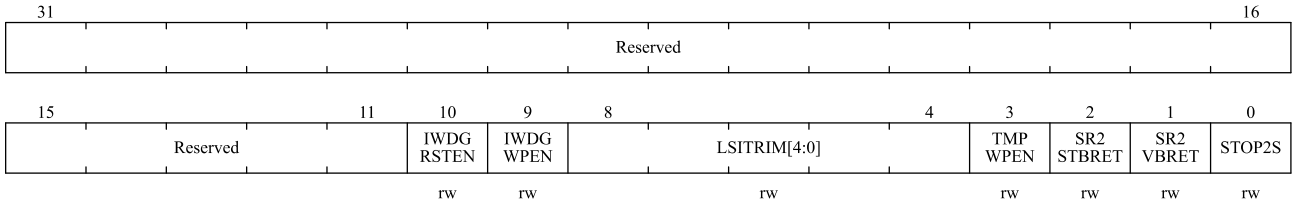
Bit field	Name	Description
3	VBATF	VBAT flag bit. This bit is set by hardware and is only cleared by POR or PDR (power-on reset/power-down reset) or set by setting the PWR_CTRL.CSBVBAT bit. 0: The device is not in VBAT mode 1: The device is already in VBAT mode
2	PVDO	PVD output. This bit is only valid when PVD is enabled by the PWR_CTRL.PVDEN bit 0: VDD/VDDA is higher than the PVD threshold selected by PWR_CTRL.PRS[2:0] 1: VDD/VDDA is lower than the PVD threshold selected by PWR_CTRL.PRS[2:0] *Note: PVD is stopped in standby mode. Therefore, after standby mode or after reset, this bit is 0 until the PWR_CTRL.PVDEN bit is set.*
1	SBF	Standby flag. This bit is set by hardware and can only be cleared by POR/PDR (power-on/power-down reset) or by setting the PWR_CTRL.CSBVBAT bit. 0: The system is not in standby mode 1: The system enters standby mode
0	WKUPF	Wake up flag. This bit is set by hardware and can only be cleared by POR/PDR (power-on/power-down reset) or by setting the PWR_CTRL.CWKUP bit. 0: No wakeup event occurred 1: A wake-up event occurred on the WKUP pin or a RTC alarm event occurred. *Note: An additional event is detected when the WKUP pin is enabled (by setting the WKUPEN bit) when the WKUP pin is already high.*

4.4.4 Power Control Register 2 (PWR_CTRL2)

Address offset: 0x08

Reset value: 0x0000 06E4 (reset by wakeup from STANDBY mode)



Bit field	Name	Description
31:11	Reserved	Reserved, the reset value must be maintained.
10	IWDGRSTEN	Independent watchdog reset enable. 0: Independent watchdog cannot generate reset to RCC 1: Independent watchdog can generate reset to RCC
9	IWDGWPEN	Independent watchdog wakeup enable. 0: Independent watchdog wakeup disable 1: Independent watchdog wake-up enable

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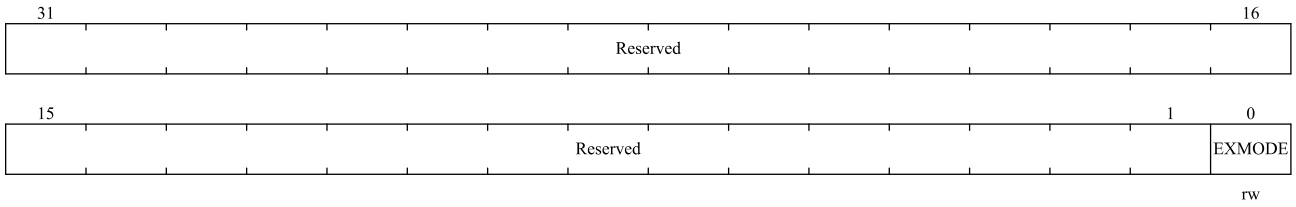
Bit field	Name	Description
8:4	LSITRIM[4:0]	LSI correction value
3	TMPWPEN	TAMPER wake-up enable. 0: Disable 1: Enable
2	SR2STBRET	R-SRAM holds the enable bit in standby mode. 0: In standby mode, R-SRAM remains disable 1: In standby mode, R-SRAM remains enable
1	SR2VBRET	R-SRAM holds the enable bit in VBAT mode. 0: In VBAT mode, R-SRAM remains disabled 1: In VBAT mode, R-SRAM remains enbale
0	STOP2S	STOP2 mode enable bit. 0: Not used 1: Enable STOP2 mode

4.4.5 Power Control Register 3 (PWR_CTRL3)

Address offset: 0x0C

Reset value: 0x0000 5B70



Bit field	Name	Description
31:1	Reserved	Reserved, the reset value must be maintained.
0	EXMODE	Extended mode control bits. 0: Normal mode 1: Extended mode

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5 Backup Registers (BKP)

5.1 Introduction

The backup memory is located in the backup domain, and is maintained by VBAT after the power supply VDD is turned off. BKP has a total of 42 16-bit registers that can be used to store and protect user application data. These 84 bytes are not affected by wake-up from system standby mode or system reset.

In addition, the BKP control register has an tamper detection function.

When the system is reset, all write operations are disabled to protect the backup domain from accidental operations. To enable, first set the RCC_APB1PCLKEN.PWREN and RCC_APB1PCLKEN.BKPEN bits to enbale the power supply and the backup interface clock, and then set the PWR_CTRL.DBKP bit to enable the write operation to the backup register.

5.2 Main Features

- Only need VBAT power supply to maintain 84-byte data backup register
- The effective level of the tamper source can be configured
- Can realize the control of tamper detection interrupt or event (BKP_CTRLSTS)

5.3 Function Description

- **Power-down backup**
- **Tamper detection**

An tamper detection event clears all backup data register contents. The detection function of the TAMPER pin can be enabled by configuring the BKP_CTRL.TP_EN bit. It should be noted that the tamper detection signal is the logical AND of the level detection signal and the BKP_CTRL.TP_EN bit, so the tamper detection should be configured before the TAMPER pin is enabled.

When an tamper event is detected, the BKP_CTRLSTS.TEF bit is set to '1'. If the tamper detection interrupt is enabled (bit '1' in BKP_CTRLSTS.TPINT_EN), an interrupt will be generated.

In order to prevent the software from writing the backup data register when there is still an tamper event on the tamper detection pin, when the tamper event is cleared, the detection function of the tamper detection pin TAMPER should be turned off. After the backup data register operation is completed, set the BKP_CTRL.TP_EN bit to '1'.

The BKP_CTRL.TP_ALEV bit is used to set the active level of the tamper detection event. When BKP_CTRL.TP_ALEV = 0 or 1, if the TAMPER pin has been high or low before enabling, an additional tamper event will occur even though there is no rising or falling edge signal on the TAMPER pin. Therefore, the TAMPER pin should be connected to the correct level off-chip.

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5.4 BKP Registers

5.4.1 BKP Register Overview

The BKP register is a 16-bit addressable register.

Table 5-1 BKP Register overview

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
000h	Reserved																																
004h	BKP_DAT1	Reserved																DAT[15:0]															
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
008h	BKP_DAT2	Reserved																DAT[15:0]															
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
00Ch	BKP_DAT3	Reserved																DAT[15:0]															
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
010h	BKP_DAT4	Reserved																DAT[15:0]															
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
014h	BKP_DAT5	Reserved																DAT[15:0]															
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
018h	BKP_DAT6	Reserved																DAT[15:0]															
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
01Ch	BKP_DAT7	Reserved																DAT[15:0]															
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
020h	BKP_DAT8	Reserved																DAT[15:0]															
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
024h	BKP_DAT9	Reserved																DAT[15:0]															
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
028h	BKP_DAT10	Reserved																DAT[15:0]															
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
02Ch	Reserved																																
030h	BKP_CTRL	Reserved																														TP_ALEV	TP_EN
	Reset Value																															0	0
034h	BKP_CTRLSTS	Reserved																						TINTF	TEF						TPINT_EN	CLRTINT	CLRTE
	Reset Value																							0	0						0	0	0
038h	Reserved																																
03Ch	Reserved																																
040h	BKP_DAT11	Reserved																DAT[15:0]															
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
044h	BKP_DAT12	Reserved																DAT[15:0]															

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Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
048h	BKP_DAT13	Reserved																DAT[15:0]															
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
04Ch	BKP_DAT14	Reserved																DAT[15:0]															
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
050h	BKP_DAT15	Reserved																DAT[15:0]															
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
054h	BKP_DAT16	Reserved																DAT[15:0]															
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
058h	BKP_DAT17	Reserved																DAT[15:0]															
	Reset Value																		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
05Ch	BKP_DAT18	Reserved																DAT[15:0]															
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
060h	BKP_DAT19	Reserved																DAT[15:0]															
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
064h	BKP_DAT20	Reserved																DAT[15:0]															
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
068h	BKP_DAT21	Reserved																DAT[15:0]															
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
06Ch	BKP_DAT22	Reserved																DAT[15:0]															
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
070h	BKP_DAT23	Reserved																DAT[15:0]															
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
074h	BKP_DAT24	Reserved																DAT[15:0]															
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
078h	BKP_DAT25	Reserved																DAT[15:0]															
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
07Ch	BKP_DAT26	Reserved																DAT[15:0]															
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
080h	BKP_DAT27	Reserved																DAT[15:0]															
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
084h	BKP_DAT28	Reserved																DAT[15:0]															
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
088h	BKP_DAT29	Reserved																DAT[15:0]															
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
08Ch	BKP_DAT30	Reserved																DAT[15:0]															
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
090h	BKP_DAT31	Reserved																DAT[15:0]															
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
094h	BKP_DAT32	Reserved																DAT[15:0]															
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
098h	BKP_DAT33	Reserved																DAT[15:0]															
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
09Ch	BKP_DAT34	Reserved																DAT[15:0]															
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0A0h	BKP_DAT35	Reserved																DAT[15:0]															

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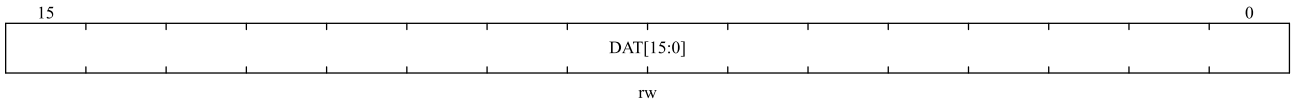
Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0A4h	BKP_DAT36	Reserved																DAT[15:0]															
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0A8h	BKP_DAT37	Reserved																DAT[15:0]															
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0ACh	BKP_DAT38	Reserved																DAT[15:0]															
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0B0h	BKP_DAT39	Reserved																DAT[15:0]															
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0B4h	BKP_DAT40	Reserved																DAT[15:0]															
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0B8h	BKP_DAT41	Reserved																DAT[15:0]															
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0BCh	BKP_DAT42	Reserved																DAT[15:0]															
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

5.4.2 Backup Data Register x (BKP_DATx) (x = 1 … 42)

Address offset: 0x04 to 0x28,0x40 to 0xBC

Reset value: 0x0000 0000

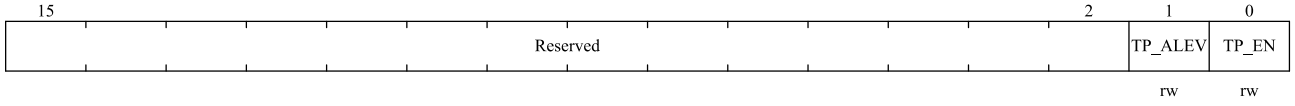


Bit field	Name	Description
15:0	DAT[15:0]	backup data These bits can be used to write user data. Note: BKP_DATx registers are not reset by system reset, power reset, wake-up from standby mode. They can be reset by a backup domain reset or (if the tamper detection pin TAMPER function is enabled) by a tamper pin event.

5.4.3 Backup Control Register (BKP_CTRL)

Address offset: 0x30

Reset value: 0x0000 0000



Bit field	Name	Description
15:2	Reserved	Reserved, the reset value must be maintained.
1	TP_ALEV	Tamper detection TAMPER pin active level 0: A high level on the tamper detection TAMPER pin clears all data backup registers 1: A low level on the tamper detection TAMPER pin clears all data backup registers

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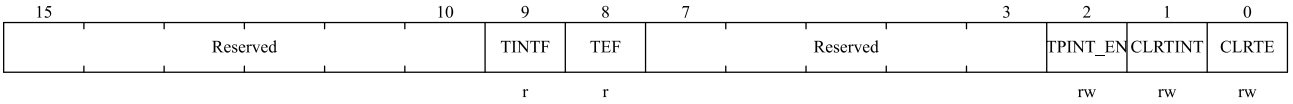
Bit field	Name	Description
0	TP_EN	Start tamper detection TAMPER pin 0: Tamper detection TAMPER pin is used as a general IO port 1: Enbale the tamper detection pin for tamper detection

Note: It is always safe to set the BKP_CTRL.TP_ALEV and BKP_CTRL.TP_EN bits at the same time. However, clearing both at the same time produces a false tamper event. Therefore, it is recommended to change the state of the BKP_CTRL.TP_ALEV bit only when BKP_CTRL.TP_EN is 0.

5.4.4 Backup Control/Status Register (BKP_CTRLSTS)

Address offset: 0x34

Reset value: 0x0000 0000



Bit field	Name	Description
15:10	Reserved	Reserved, the reset value must be maintained.
9	TINTF	Tamper interrupt flag This bit is set by hardware when an tamper event is detected and the TPINT_EN bit is 1. This flag is cleared by writing a 1 to the CLRTINT bit (which also clears the interrupt). This bit is also cleared if the TPINT_EN bit is cleared. 0: No tamper interrupt 1: Generate tamper interrupt *Note: This bit is only reset after system reset or wake-up from standby mode*
8	TEF	Tamper event sign This bit is set by hardware when an tamper event is detected. This flag can be cleared by writing a 1 to the CLRTE bit 0: No tamper event 1: Tamper event detected *Note: A tamper event resets all BKP_DATx registers. All BKP_DATx registers remain reset as long as TEF is 1. When this bit is set to 1, if a write operation is performed to BKP_DATx, the written value will not be saved.*
7:3	Reserved	Reserved, the reset value must be maintained.
2	TPINT_EN	Allow tamper of TAMPER pin interrupt 0: Disable tamper detection interrupt 1: Tamper detection interrupt is enabled (the TP_EN bit of the BKP_CTRL register must also be set to 1) *Note 1: Intrusive interrupts cannot wake up the system core from low power modes.* *Note 2: This bit is reset only after system reset or wake-up from standby mode.*
1	CLRTINT	Clear Tamper Detection Interrupt This bit can only be written, and the read value is 0. 0: invalid

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Bit field	Name	Description
		1: Clear the tamper detection interrupt and TINTF tamper detection interrupt flags
0	CLRTE	Clear tamper detection events This bit can only be written, and the read value is 0. 0: invalid 1: Clear the TEF tamper detection event flag (and reset the tamper detector).

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6 Reset and Clock Control (RCC)

6.1 Reset Control Unit

Supports the following three types of reset:

- Power Reset
- System Reset
- Backup domain Reset

6.1.1 Power Reset

A Power reset occurs in the following circumstances:

- Power-on reset (POR reset).
- Power-down reset(PDR reset).
- When exiting STANDBY mode.

Power resets will reset all registers except the backup domain (see Figure 4-1).

The reset source in the figure will finally act on the NRST pin and remain low during the reset process. The reset entry vector is fixed at address 0x0000_0004. For more details, see Table 2-1 vector table.

6.1.2 System Reset

Except the reset flags in the Control/Status Register (RCC_CTRLSTS)and the registers in the backup domain (see Figure 4-1), a system reset sets all registers to their reset values.

A system reset is generated when one of the following events occurs:

- A low level on the NRST pin (external reset)
- Window watchdog end of count condition (WWDG reset)
- Independent watchdog end of count condition (IWDG reset)
- Software reset (SW reset)
- Low power management reset
- Power reset
- MMU protection reset
- RAM parity error reset
- Backup domain EMC reset
- Retention domain EMC reset
- BOR reset

The source of the reset event can be identified by looking at the reset status flag bits in the RCC_CTRLSTS control

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status register.

6.1.2.1 Software reset

A software reset can be generated by setting the SYSRESETREQ bit in Cortex™-M4 Application Interrupt and Reset Control Register. Refer to Cortex™-M4 technical reference manual for further information.

6.1.2.2 Low-power management reset

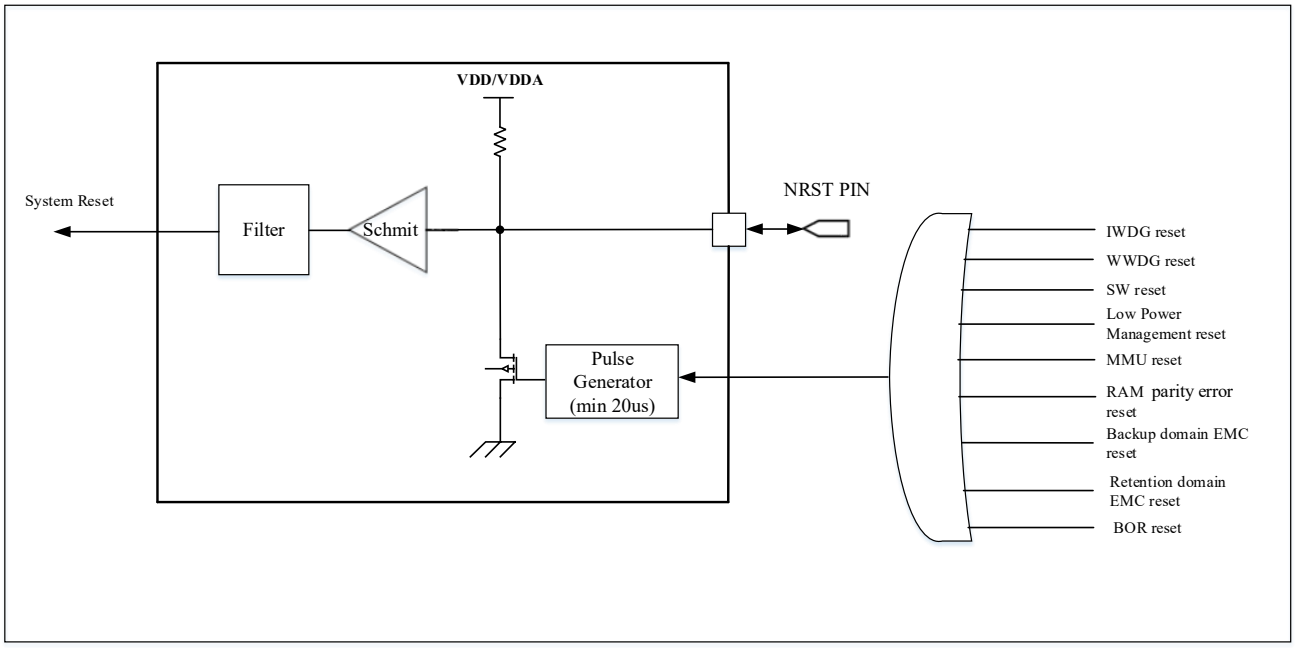
Low-power management reset can be generated by using the following methods:

- Generate low power management reset when entering STANDBY mode: This reset is enabled by setting the nRST_STDBY bit in the user option byte. At this time, even if the procedure to enter STANDBY mode is performed, the system will be reset instead of entering STANDBY mode.
- Generate low power management reset when entering STOP0/STOP2 mode: This reset is enabled by setting the nRST_STOP bit in the user option byte. At this time, even if the process to enter STOP0/STOP2 mode is performed, the system will be reset instead of entering STOP0/STOP2 mode.

The system reset signal provided to the chip is output on the NRST pin. The pulse generator guarantees a minimum reset pulse duration of 20μs for each reset source (external or internal). For external reset, the reset pulse is generated while the NRST pin is asserted low.

The Figure below shows the system reset generation circuit.

Figure 6-1 System reset generation



6.1.3 Backup domain reset

The backup domain has two dedicated resets that only affect the backup domain (see Figure 4-1 Power Supply Block Diagram).

The backup domain reset is generated when one of the following events occurs:

- Software reset: The backup domain reset can be generated by setting the RCC_BDCTRL.BDSFTRST bit.

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- Under the premise that both VDD and VBAT are powered off, the backup area will be reset only when VDD or VBAT is powered on.

6.2 Clock Control Unit

Three different clock sources can be used to drive the system clock (SYSCLK):

- HSI oscillator clock;
- HSE oscillator clock;
- PLL clock;

The devices have the following two secondary clock sources:

- LSI: 40 kHz low-speed internal RC which drives independent watchdog (IWDG) can be selected by software to drive RTC. RTC is used to automatically wake up the system from STOP0/STOP2/STANDBY mode.
- LSE: 32.768 kHz low-speed external crystal can also be selected by software to drive RTC(RTCCLK).

Each clock source can be turned on or off independently when it is not used to optimize power consumption.

Several prescalers can be used to configure the frequencies of the AHB, the high-speed APB (APB2), and the low-speed APB (APB1) domains. The maximum frequencies of the AHB, APB2, and APB1 domains are 144MHz, 72MHz, and 36MHz respectively. The clock frequency of the SDIO interface is fixed at HCLK/2.

RCC provides the Cortex System Timer (SysTick) external clock with the AHB clock (HCLK) divided by 8. This clock or Cortex clock(HCLK) can be selected to drive the SysTick by programming the SysTick Control and Status Register. The ADC clock is generated by dividing the AHB clock or PLL clock.

The clock frequencies of timers are automatically set by hardware. There are two scenarios:

- If the APB prescaler is 1, the timer clock frequencies are set to the same frequency as that of the APB domain to which the timers are connected.
- Otherwise, they are set to twice the frequency of the APB domain to which the timers are connected.

FCLK is the free-running clock of Cortex™-M4F. For more details, refer to the ARM Cortex™-M4 technical reference manual.

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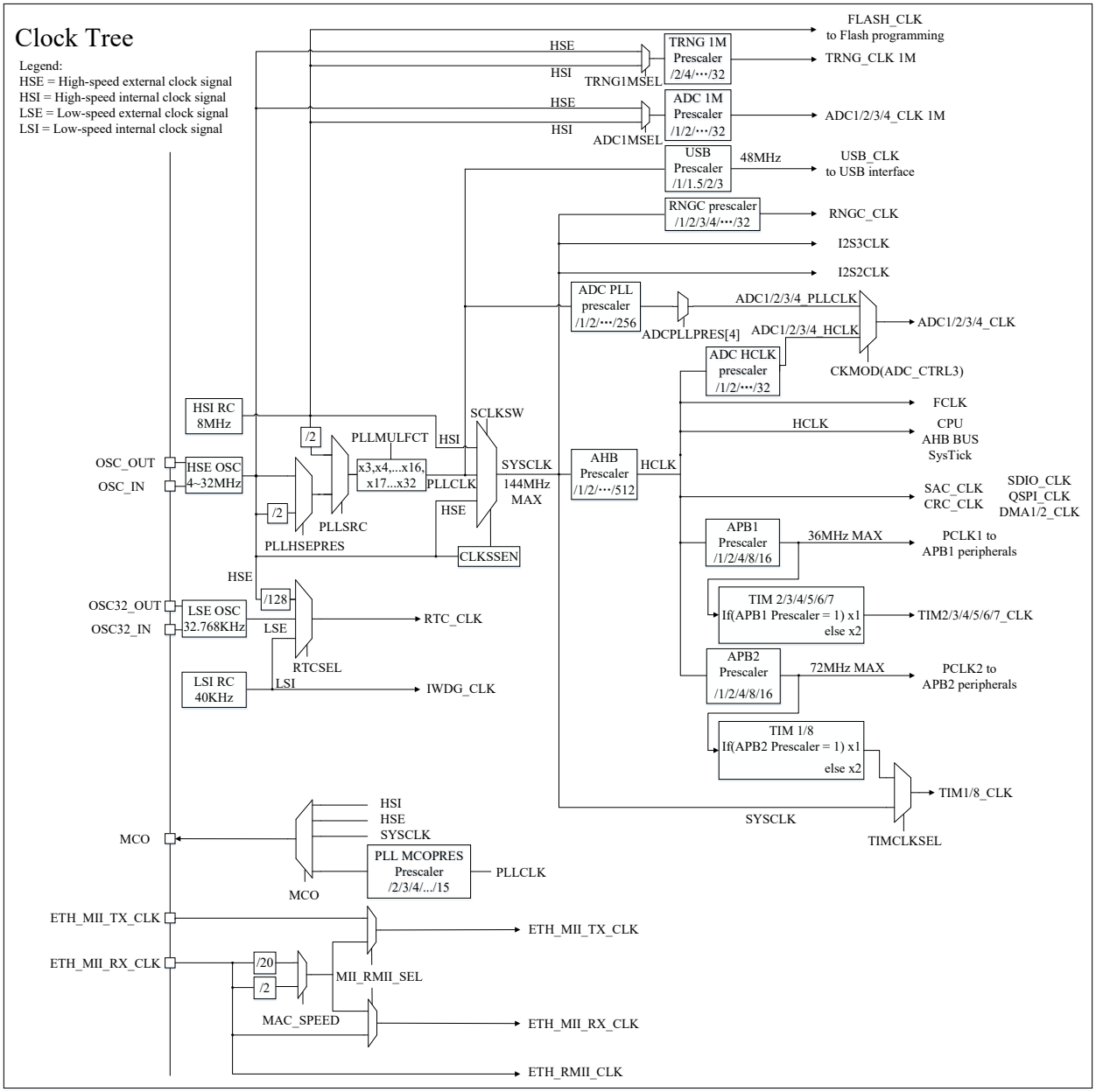
6.2.1 Clock Tree Diagram

Figure 6-2 Clock Tree



1. When HSI is used as the input of the PLL clock, the maximum frequency that the system clock can get is 128MHz.
2. For more details about the internal and external clock source characteristics, please refer to the "Electrical Characteristics" section in the product datasheet.
3. When PLL is selected as system clock source, PLL minimum clock output is 32MHz.

6.2.2 HSE Clock

The high-speed external clock signal (HSE) can be generated from the following two clock sources:

- HSE external crystal/ceramic resonator

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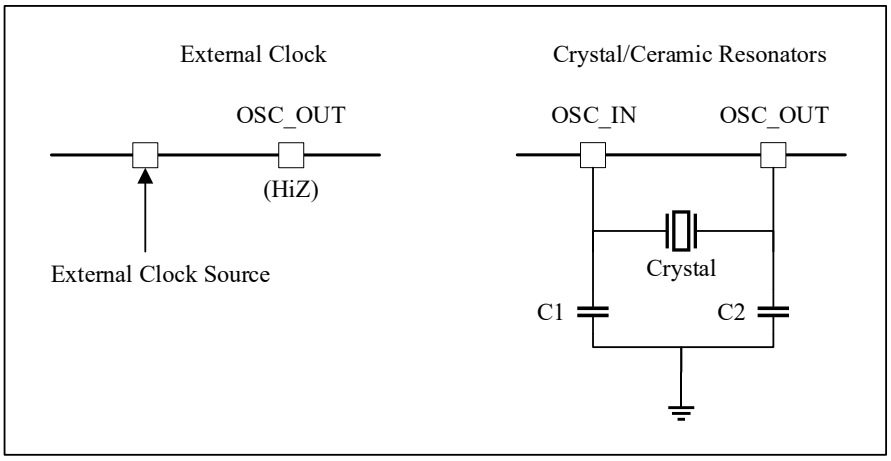
- HSE user external clock

To reduce distortion of the clock output and shorten the start-up Stablize time, the crystal/ceramic resonator and load capacitor must be placed as close as possible to the oscillator pins. The load capacitance value must be adjusted according to the chosen oscillator.

Figure 6-3 HSE/LSE clock source



6.2.2.1 External clock source (HSE bypass)

In this mode, an external clock source must be provided. Its frequency can be up to 32MHz. Users can select this mode by setting the RCC_CTRL.HSEBP and RCC_CTRL.HSEEN bits. The external clock signal(50% duty cycle square, sine or triangle wave) must be connected to the OSC_IN pin while the OSC_OUT pin must be left floating (Hi-Z). See Figure 6-3.

6.2.2.2 External crystal/ceramic resonator (HSE crystal)

The 4 to 32 MHz external oscillator has the advantage of producing a more accurate master clock for the system. The associated hardware configuration is shown in See Figure 6-3. For more details, please refer to the electrical characteristics section of the datasheet.

The RCC_CTRL.HSERDF bit indicates whether the high-speed external oscillator is stable or not. At startup, the clock is not released until this bit is set by hardware. An interrupt can be generated if enabled in the Clock Interrupt Register (RCC_CLKINT).

HSE clock can be switched on and off by setting the RCC_CTRL.HSEEN bit.

6.2.3 HSI Clock

The HSI (High Speed Internal) clock signal is generated by an internal 8MHz RC oscillator and can be used directly as system clock or as PLL input after dividing by 2. The HSI RC oscillator can provide a clock source without any external devices. It also has a shorter startup time than the HSE crystal oscillator. However, its frequency is less accurate even with calibration.

The HSI clock frequency of each chip has been calibrated to 1% (25°C) before leaving the factory. After the system reset, the factory calibration value is loaded into the RCC_CTRL.HSICAL[7:0] bits.

If the user application is subject to voltage or temperature variations, this may affect the accuracy of the RC oscillator. The HSI frequency can be trimmed by using the RCC_CTRL.HSITRIM[4:0] bits.

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The RCC_CTRL.HSIRDF bit flag indicates if the HSI RC oscillator is stable. At startup, the HSI RC output clock is not released until this bit is set by hardware. HSI clock can be switched on and off using the RCC_CTRL.HSIEN bit.

If the HSE crystal oscillator fails, the HSI clock is used as a backup clock source. Refer to Section 6.2.8 Clock Security System.

6.2.4 PLL Clock

The internal PLL can be used to multiply the HSI or the HSE clock frequency. Refer to Figure 6-2 Clock Tree,The PLL configuration (selection of PLL input clock (HSI/HSE and divider) and multiplication factor) must be done before enabling PLL. Once the PLL is enabled, these parameters cannot be changed. The PLL can be configured using control bits in RCC_CTRL and RCC_CFG registers.

If the PLL interrupt is enabled in the clock interrupt register, an interrupt request can be generated when the PLL is ready.

If the USB interface needs to be used in the application, the PLL must be set to output 48, 72, 96,144MHz clocks to provide the 48MHz USBCLK clock.

6.2.5 LSE Clock

The LSE crystal is a 32.768KHz low speed external crystal or ceramic resonator. It provides a low-power and accurate clock source for the real-time clock or other timing functions.

The LSE clock is enabled and disabled by the RCC_BDCTRL.LSEEN bit.

The RCC_BDCTRL.LSERD bit indicates whether the LSE clock is stable. During the startup phase, the LSE clock signal is not released until this bit is set by hardware. If enabled in the clock interrupt register, an interrupt request can be generated.

6.2.5.1 LSE external clock source(LSE bypass)

In this mode, an external clock source with a frequency of up to 1 MHz can be provided. Users can select this mode by setting the RCC_BDCTRL.LSEBP and RCC_BDCTRL.LSEEN bits. The external clock signal(square, sine or triangle wave) with 50% duty cycle must be connected to the OSC32_IN pin while the OSC32_OUT pin must be left floating (Hi-Z).

6.2.6 LSI Clock

The LSI RC can clock the IWDG and AWU in STOP0/STOP2 and STANDBY modes. The LSI clock frequency is about 40kHz. For further information please refer to the Electrical Characteristics section of the data sheet.

The LSI clock can be turned on or off using the RCC_CTRLSTS.LSIEN bit.

The RCC_CTRLSTS.LSIRD bit flag indicates if the LSI clock is stable. At startup, the clock is not released until this bit is set by hardware. An interrupt can be generated if enabled in the Clock Interrupt Register (RCC_CLKINT).

6.2.6.1 LSI calibration

The internal low-speed oscillator LSI can be calibrated to compensate for its frequency offset to obtain an RTC time base with acceptable accuracy, and an independent watchdog (IWDG) timeout (when these peripherals are clocked from the LSI).

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Calibration can be achieved by measuring the LSI clock frequency using the TIM5's input clock (TIM5_CLK). The measurement is guaranteed by the accuracy of the HSE. The software can obtain the accurate RTC clock base by adjusting the 20 bit prescaler of the RTC, and obtain the accurate independent watchdog (IWDG) timeout time by calculation.

The LSI calibration steps are as follows:

1. Turn on TIM5 and set channel 4 to input capture mode;

2. Set the AFIO_RMP_CFG.TIM5CH4_RMP bit to 1, and connect the LSI to channel 4 of TIM5 internally;

3. Measure LSI clock frequency through TIM5 capture/compare 4 events or interrupts;

4. Set the 20 bit prescaler based on the measurement results and the desired RTC time base and independent watchdog timeout.

6.2.7 System clock (SYSCLK) selection

After a system reset, the HSI oscillator is selected as the system clock. It cannot be stopped when the clock source is used directly or indirectly through the PLL as the system clock.

Switching from one clock source to another will only occur when the target clock source is ready (either after a delay to start the stabilization phase or PLL stabilization). When the selected clock source is not ready, the switching of the system clock will not occur until the target clock source is ready.

Status bits in the clock control register (RCC_CTRL) indicate which clock is ready and which clock is currently used as the system clock.

6.2.8 Clock Security System (CLKSS)

Clock security system can be activated by software by setting the RCC_CTRL.CLKSSEN bit. Once activated, the clock detector is enabled after the startup delay of the HSE oscillator, and disabled when the HSE clock is turned off.

If the HSE clock fails, the HSE oscillator will be automatically turned off, and a clock failure event will be sent to the break input of the advanced timers (TIM1 and TIM8), and the Clock Security System Interrupt CLKSSIF will be generated, allowing the software to execute rescue operations. The CLKSSIF interrupt is connected to the NMI (Non-Maskable Interrupt) interrupt of the Cortex™-M4.

Once the CSS is activated and the HSE clock fails, the CSS interrupt is generated and the NMI is automatically generated. The NMI will be executed continuously until the CSS interrupt pending bit is cleared. Therefore, it is necessary to clear the CSS interrupt by setting the RCC_CLKINT.CLKSSICLR bit in the NMI handler.

If the HSE oscillator is directly or indirectly used as the system clock (indirectly means: it is used as the PLL input clock, and the PLL clock is used as the system clock), the clock failure will cause a switch of the system clock to the HSI oscillator and the disabling of the external HSE oscillator. If HSE clock (divided or not) is selected as PLL input clock then upon HSE clock failure, the PLL will be turned off.

6.2.9 RTC Clock

By programming RCC_BDCTRL.RTCSEL[1:0] bits, the RTCCLK clock source can be either the HSE/128, LSE, or LSI clocks. This selection cannot be changed unless the backup domain is reset.

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The LSE clock is in the backup domain, but the HSE and LSI clocks are not. therefore:

- If LSE is selected as RTC clock:
  - As long as VBAT remains powered, the RTC continues to work even though the VDD power supply is cut off.
- If LSI is selected as the automatic wake-up unit (AWU) clock:
  - If the VDD supply is cut off, the AWU status cannot be guaranteed. For LSI calibration, see Section 6.2.6 LSI Clock.
- If the HSE clock is divided by 128 as the RTC clock:
  - If the VDD power supply is cut off or the internal voltage regulator is turned off (the power supply in the 1.8V domain is cut off), the RTC state is indeterminate.
  - The PWR_CTRL.DBKP bit of the power control register (see Section 4.4.2) must be set (to cancel the write protection of the backup power domain) to 1.

6.2.10 Watchdog Clock

If the IWDG is started by either hardware option or software access, the LSI oscillator will be forced ON and cannot be disabled. After the LSI oscillator is stabilized, the clock is provided to the IWDG.

6.2.11 Clock output(MCO)

The microcontroller clock output (MCO) capability allows the clock signal to be output onto the external MCO pin.

The corresponding GPIO port register must be configured for the corresponding function.The following 4 clock signals can be selected as the MCO clock:

- SYSCLK
- HSI
- HSE
- PLL clock division

The clock selection is controlled by RCC_CFG.MCO[2:0] bits.

6.3 RCC Registers

The RCC registers are accessible through AHB bus. The register description is as follows.

6.3.1 RCC Register Overview

Table 6-1 RCC register overview

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
000h	RCC_CTRL	Reserved						PLLRDF	PLLEN	Reserved				CLKSSEN	HSEBP	HSERDF	HSEEN	HSICAL[7:0]								HSITRIM[4:0]					Reserved	HSIRDF	HSIEN
	Reset Value							0	0					0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0		1	1

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Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
004h	RCC_CFG	MCOPRES[3:0]				PLLMULFCT[4]	MCO[2:0]			USBPRES[1:0]		PLLMULFCT[3:0]				PLLHSEPRES	PLLSRC	Reserved		APB2PRES[2:0]			APB1PRES[2:0]			AHBPRES[3:0]				SCLKSTS[1:0]		SCLKSW[1:0]	
	Reset Value	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0			0	0	0	0	0	0	0	0	0	0	0	0	0	0
008h	RCC_CLKINT	Reserved								CLKSSICLR	Reserved	PLLRDICLR	HSERDICLR	HSIRDICLR	LSERDICLR	LSIRDICLR		Reserved			PLLRDIEN	HSERDIEN	HSIRDIEN	LSERDIEN	LSIRDIEN	CLKSSIF	Reserved			PLLRDIF	HSERDIF	HSIRDIF	LSERDIF	LSIRDIF
	Reset Value									0		0	0	0	0	0					0	0	0	0	0	0				0	0	0	0	0
00Ch	RCC_APB2PRST	Reserved										I2C4RST	I2C3RST	UART7RST	UART6RST	DVPRST		Reserved	USART1RST	TIM8RST	SPI1RST	TIM1RST	Reserved		IOPGRST	IOPFRST	IOPERST	IOPDRST	IOPCRST	IOPBRST	IOPAMPRST	Reserved	AFIORST
	Reset Value											0	0	0	0	0			0	0	0	0			0	0	0	0	0	0	0		0
010h	RCC_APB1PRST	Reserved		DACRST	PWRRST	BKPRST	CAN2RST	CAN1RST	Reserved	USBRST	I2C2RST	I2C1RST	UART5RST	UART4RST	USART3RST	USART2RST	Reserved	SPI3RST	SPI2RST	Reserved		WWDGRST	Reserved					TIM7RST	TIM6RST	TIM5RST	TIM4RST	TIM3RST	TIM2RST
	Reset Value			0	0	0	0	0		0	0	0	0	0	0	0		0	0			0					0	0	0	0	0	0	
014h	RCC_AHBPCLKEN	Reserved														QSPIEN	ETHMACEN	ADC4EN	ADC3EN	ADC2EN	ADC1EN	SACEN	SDIOEN	RNGCEN	Reserved		CRCEN	Reserved	FLITFEN	Reserved	SRAMEN	DMA2EN	DMA1EN
	Reset Value															0	0	0	0	0	0	0	0	0			0		1		1	0	0
018h	RCC_APB2PCLKEN	Reserved											I2C4EN	I2C3EN	UART7EN	UART6EN	DVPEN	Reserved	USART1EN	TIM8EN	SPI1EN	TIM1EN	Reserved		IOPGEN	IOPFEN	IOPEEN	IOPDEN	IOPCEN	IOPBEN	IOPAMPEN	Reserved	AFIOEN
	Reset Value												0	0	0	0	0		0	0	0	0			0	0	0	0	0	0	0		0
01Ch	RCC_APB1PCLKEN	OPAMPEN	Reserved	DACEN	PWREN	BKPEN	CAN2EN	CAN1EN	Reserved	USBEN	I2C2EN	I2C1EN	UART5EN	UART4EN	USART3EN	USART2EN	Reserved	SPI3EN	SPI2EN	Reserved		WWDGEN	Reserved			COMPFILTEN	COMPEN	TIM7EN	TIM6EN	TIM5EN	TIM4EN	TIM3EN	TIM2EN
	Reset Value	0		0	0	0	0	0		0	0	0	0	0	0	0		0	0			0				0	0	0	0	0	0	0	0
020h	RCC_BDCTRL	Reserved															BDSFTRST	RTCEN	Reserved				RTCSEL[1:0]		Reserved						LSEBP	LSERDIF	LSEEN
	Reset Value																0	0					0	0							0	0	0
024h	RCC_CTRLSTS	LPWRRSTF	WWDGRSTF	IWDGRSTF	SFTRSTF	PORRSTF	PINRSTF	MMURSTF	RMRSTF	RAMRSTF	Reserved	BKPEMCF	RETEMCF	BORRSTF	Reserved																		LSIRD	LSIEN
	Reset Value	0	0	0	0	1	1	0	0	0		0	0	0																		1	1
028h	RCC_AHBPRST	Reserved														QSPIRST	ETHMACRST	ADC4RST	ADC3RST	ADC2RST	ADC1RST	SACRST	Reserved	RNGCRST	Reserved									
	Reset Value															0	0	0	0	0	0	0		0									
02Ch	RCC_CFG2	Reserved		TIMCLKSEL	RNGCPRES[4:0]					Reserved								ADC1MPRES[4:0]					ADC1MSEL	Reserved	ADCPLLPRES[4:0]					ADCHPRES [3:0]			
	Reset Value			0	0	0	0	0	0									0	0	1	1	1	0		0	0	0	0	0	0	0	0	0
030h	RCC_CFG3	Reserved													TRNG1MEN	TRNG1MSEL	Reserved	TRNG1MPRES[4:0]					Reserved			BORRSTEN	Reserved							
	Reset Value														0	0		0	0	1	1	1				1							

6.3.2 Clock Control Register (RCC_CTRL)

Address offset: 0x00

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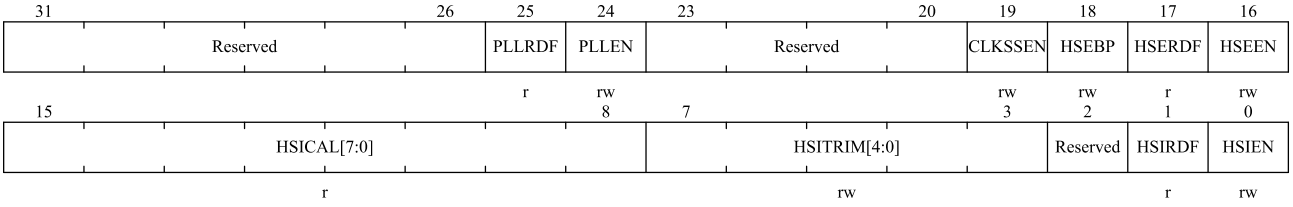
Reset value: 0x0000 0083



Bit Field	Name	Description
31:26	Reserved	Reserved, the reset value must be maintained.
25	PLLRDF	PLL clock ready flag Set by hardware once PLL is ready. 0: PLL is not ready 1: PLL is ready
24	PLLEN	PLL enable Set and cleared by software. When entering the stop0/stop2/standby mode, it is cleared by hardware. This bit cannot be cleared when PLL is used as the system clock. When the HSI/HSE is used as the clock source for the PLL, the PLL will not be turned on until the HSI/HSE clock is ready. 0: Disable PLL 1: Enable PLL
23:20	Reserved	Reserved, the reset value must be maintained.
19	CLKSSEN	Clock security system enable Set and cleared by software. 0: Disable the clock detector 1: Enable the clock detector if the HSE oscillator is ready
18	HSEBP	External high-speed clock bypass enable Set and cleared by software. This bit can only be written when the HSE oscillator is disabled. 0: Disable the bypass function of HSE oscillator 1: Enable the bypass function of HSE oscillator
17	HSERDF	External high-speed clock ready flag Set by hardware once HSE is ready. This bit takes 6 HSE clock cycles to clear after the HSEEN bit is cleared. 0: HSE is not ready 1: HSE is ready
16	HSEEN	External high-speed clock enable Set and cleared by software. When entering the stop0/stop2 or standby mode, it is cleared by hardware. This bit cannot be cleared when HSE is used directly or indirectly as the system clock. 0: Disable HSE oscillator 1: Enable HSE oscillator
15:8	HSICAL[7:0]	Internal high-speed clock calibration value

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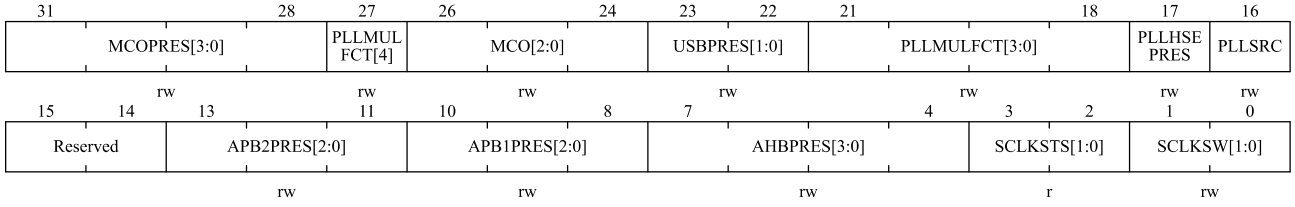
Bit Field	Name	Description
		These bits are automatically initialized at startup.
7:3	HSITRIM[4:0]	Internal high-speed clock correction value Written by software. The values of these bits will be added to the HSICAL[7:0] bits in order to form the final value for calibrating the frequency of the internal HSI RC oscillator. The trimming step is around 40 kHz between two consecutive HSICAL steps, and the default value is 16, which can adjust the HSI to 8 MHz ±1%.
2	Reserved	Reserved, the reset value must be maintained.
1	HSIRDF	Internal high-speed clock ready flag Set by hardware once HSI is stable. After the HSIEN bit is cleared, it takes 6 internal 8 MHz oscillator clock cycles to go low. 0: HSI is not ready 1: HSI is ready
0	HSIEN	Internal high-speed clock enable Set and cleared by software. This bit cannot be cleared when HSI is used as the system clock. When returning from stop0/stop2 or standby mode or HSE failure occurs, set by hardware to enable the HSI oscillator. This bit cannot be reset if the HSI is used directly or indirectly as system clock. 0: Disable HSI oscillator 1: Enable HSI oscillator

6.3.3 Clock Configuration Register (RCC_CFG)

Address offset: 0x04

Reset value: 0x2000 0000



Bit Field	Name	Description
31:28	MCOPRES[3:0]	MCO prescaler Set and cleared by software. 0010: Divide PLL clock by 2 as MCO clock 0011: Divide PLL clock by 3 as MCO clock 0100: Divide PLL clock by 4 as MCO clock 0101: PLL clock divided by 5 as MCO clock 0110: Divide PLL clock by 6 as MCO clock 0111: Divide PLL clock by 7 as MCO clock 1000: Divide PLL clock by 8 as MCO clock 1001: PLL clock divided by 9 as MCO clock 1010: Divide PLL clock by 10 as MCO clock

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Bit Field	Name	Description
		1011: Divide PLL clock by 11 as MCO clock 1100: PLL clock divided by 12 as MCO clock 1101: Divide PLL clock by 13 as MCO clock 1110: Divide PLL clock by 14 as MCO clock 1111: Divide PLL clock by 15 as MCO clock Other values: not allowed to set
27	PLLMULFCT[4]	This bit is combined with bit[21:18] to form a PLL multiplication factor. Please refer to PLLMULFCT[3:0].
26:24	MCO[2:0]	Microcontroller clock output selection Set and cleared by software. 0xx: no clock output 100: Select system clock (SYSCLK) output 101: select internal high-speed clock (HSI) output 110: select external high-speed clock (HSE) output 111: Select the output after PLL frequency division *Notice: This clock output may be truncated when starting and switching the MCO clock source.* *When the system clock is output to the MCO pin, the output clock frequency should not exceed 50MHz (the highest frequency of the I/O port).*
23:22	USBPRES[1:0]	USB prescaler. Set or cleared by software to generate a 48MHz USB clock. The values of these bits must be valid before enabling the USB clock in the RCC_APB1PCLKEN register. 00: Divide the PLL clock by 1.5 as the USB clock 01: The PLL clock is directly used as the USB clock 10: Divide the PLL clock by 2 as the USB clock 11: Divide the PLL clock by 3 as the USB clock
21:18	PLLMULFCT[3:0]	PLL multiplication factor (including bit 27) Written by software to define PLL multiplication factor. These bits can only be written when the PLL is disabled. The PLL output frequency must not exceed 144MHz. 00000: PLL input clock × 2 00001: PLL input clock × 3 00010: PLL input clock × 4 00011: PLL input clock × 5 00100: PLL input clock × 6 00101: PLL input clock × 7 00110: PLL input clock × 8 00111: PLL input clock × 9 01000: PLL input clock × 10 01001: PLL input clock × 11 01010: PLL input clock × 12 01011: PLL input clock × 13

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Bit Field	Name	Description
		01100: PLL input clock × 14 01101: PLL input clock × 15 01110: PLL input clock × 16 01111: PLL input clock × 16 10000: PLL input clock × 17 10001: PLL input clock × 18 10010: PLL input clock × 19 10011: PLL input clock × 20 10100: PLL input clock × 21 10101: PLL input clock × 22 10110: PLL input clock × 23 10111: PLL input clock × 24 11000: PLL input clock × 25 11001: PLL input clock × 26 11010: PLL input clock × 27 11011: PLL input clock × 28 11100: PLL input clock × 29 11101: PLL input clock × 30 11110: PLL input clock × 31 11111: PLL input clock × 32
17	PLLHSEPRES	HSE prescaler for PLL input Set and cleared by software to divide HSE before PLL entry. This bit can only be written when PLL is disabled. 0: HSE clock not divided 1: HSE divided by 2
16	PLLSRC	PLL clock source Set and cleared by software to select PLL clock source. This bit can only be written when PLL is disabled. 0: HSI clock divided by 2 is used as the PLL input clock 1: HSE clock selected as PLL input clock
15:14	Reserved	Reserved, the reset value must be maintained.
13:11	APB2PRES[2:0]	APB high-speed (APB2) prescaler Set and cleared by software to configure the division factor of APB2 clock (PCLK2). Make sure that PCLK2 does not exceed 72MHz. 0xx: HCLK not divided 100: HCLK divided by 2 101: HCLK divided by 4 110: HCLK divided by 8 111: HCLK divided by 16
10:8	APB1PRES[2:0]	APB low-speed (APB1) prescaler Set and cleared by software to configure the division factor of APB1 clock (PCLK1). Make sure that PCLK1 does not exceed 36MHz. 0xx: HCLK not divided

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Bit Field	Name	Description
		100: HCLK divided by 2 101: HCLK divided by 4 110: HCLK divided by 8 111: HCLK divided by 16
7:4	AHBPRES[3:0]	AHB prescaler Set and cleared by software to configure the division factor of the AHB clock (HCLK). 0xxx: SYSCLK not divided 1000: SYSCLK divided by 2 1001: SYSCLK divided by 4 1010: SYSCLK divided by 8 1011: SYSCLK divided by 16 1100: SYSCLK divided by 64 1101: SYSCLK divided by 128 1110: SYSCLK divided by 256 1111: SYSCLK divided by 512
3:2	SCLKSTS[1:0]	System clock switching status Set and cleared by hardware to indicate which clock source is used as system clock 00: The system clock comes from HSI 01: The system clock comes from HSE 10: The system clock comes from the PLL output 11: Unavailable
1:0	SCLKSW[1:0]	System clock switch Set and cleared by software to select the system clock source. Set by hardware to force HSI selection when exiting from the stop2 or standby mode, or when the HSE oscillator fails (RCC_CTRL.CLKSSEN is enabled). 00: Select HSI as system clock 01: Select HSE as system clock 10: Select PLL output as system clock 11: Unavailable

6.3.4 Clock Interrupt Register (RCC_CLKINT)

Address offset: 0x08

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved								CLKSSI CLR	Reserved		PLLRDI CLR	HSERDI CLR	HSIRDI CLR	LSERDI CLR	LSIRDI CLR
								w			w	w	w	w	w
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved			PLLRDI EN	HSERDI EN	HSIRDI EN	LSERDI EN	LSIRDI EN	CLKSSIF	Reserved		PLLRDIF	HSERDIF	HSIRDIF	LSERDIF	LSIRDIF
			rw	rw	rw	rw	rw	r			r	r	r	r	r

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Bit Field	Name	Description
31:24	Reserved	Reserved, the reset value must be maintained.
23	CLKSSICLR	Clock security system interrupt clear Set by the software to clear the CLKSSIF flag. 0: No effect 1: Clear the CLKSSIF flag
22:21	Reserved	Reserved, the reset value must be maintained.
20	PLLRDICLR	PLL ready interrupt clear Set by the software to clear the PLLRDIF flag. 0: No effect 1: Clear the PLLRDIF flag
19	HSERDICLR	HSE ready interrupt clear Set by the software to clear the HSERDIF flag. 0: Not used 1: Clear HSERDIF flag
18	HSIRDICLR	HSI ready interrupt clear Set by the software to clear the HSIRDIF flag. 0: Not used 1: Clear the HSIRDIF flag
17	LSERDICLR	LSE ready interrupt clear Set by the software to clear the LSERDIF flag. 0: Not used 1: Clear LSERDIF flag
16	LSIRDICLR	LSI ready interrupt clear Set by software to clear the LSIRDIF flag. 0: Not used 1: Clear the LSIRDIF flag
15:13	Reserved	Reserved, the reset value must be maintained.
12	PLLRDIEN	PLL ready interrupt enable Set and cleared by software to enable and disable PLL ready interrupt 0: Disable PLL ready interrupt 1: Enable PLL ready interrupt
11	HSERDIEN	HSE ready interrupt enable Set and cleared by software to enable and disable HSE ready interrupt. 0: Disable HSE ready interrupt 1: Enable HSE Ready Interrupt
10	HSIRDIEN	HSI ready interrupt enable Set and cleared by software to enable and disable HSI ready interrupt. 0: Disable HSI ready interrupt 1: Enable HSI ready interrupt
9	LSERDIEN	LSE ready interrupt enable Set and cleared by software to enable and disable LSE ready interrupt. 0: Disable LSE ready interrupt 1: Enable LSE ready interrupt

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Bit Field	Name	Description
8	LSIRDIEN	LSI ready interrupt enable Set and cleared by software to enable and disable LSI ready interrupt. 0: Disable LSI ready interrupt 1: Enable LSI ready interrupt
7	CLKSSIF	Clock security system interrupt flag Set by hardware when a failure is detected in the external HSE oscillator. 0: No clock security system interrupt caused by HSE clock failure 1: Clock security system interrupt caused by HSE clock failure
6:5	Reserved	Reserved, the reset value must be maintained.
4	PLLRDIF	PLL ready interrupt flag This bit is set by hardware when PLLRDIEN is set and PLL clock is ready. This bit is cleared by software by setting the PLLRDICLR bit. 0: No clock ready interrupt caused by PLL lock 1: Clock ready interrupt caused by PLL lock
3	HSERDIF	HSE ready interrupt flag Set by hardware when HSERDIEN is set and the HSE clock is ready. This bit is cleared by software by setting the HSERDICLR bit. 0: No clock ready interrupt caused by HSE oscillator 1: Clock ready interrupt caused by HSE oscillator
2	HSIRDIF	HSI ready interrupt flag Set by hardware when HSIRDIEN is set and the HSI clock is ready. This bit is cleared by software by setting the HSERDICLR bit. 0: No clock ready interrupt caused by HSI oscillator 1: Clock ready interrupt caused by HSI oscillator
1	LSERDIF	LSE ready interrupt flag Set by hardware when LSERDIEN is set and the LSE clock is ready. This bit is cleared by the software by setting the LSERDICLR bit. 0: No clock ready interrupt caused by LSE oscillator 1: Clock ready interrupt caused by LSE oscillator
0	LSIRDIF	LSI ready interrupt flag Set by the hardware when LSIRDIEN is set and the LSI clock is ready. This bit is cleared by software by setting the LSIRDICLR bit. 0: No clock ready interrupt caused by LSI oscillator 1: Clock ready interrupt caused by LSI oscillator

6.3.5 APB2 Peripheral Reset Register (RCC_APB2PRST)

Address offset: 0x0c

Reset value: 0x0000 0000

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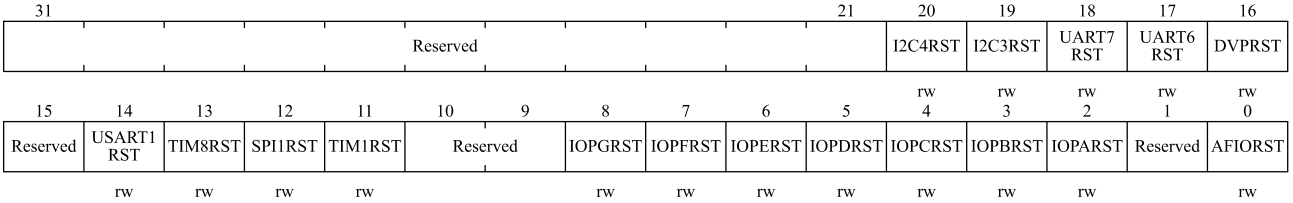

Bit Field	Name	Description
31:21	Reserved	Reserved, the reset value must be maintained.
20	I2C4RST	I2C4 reset Set and cleared by software. 0: Clear the reset 1: Reset I2C4
19	I2C3RST	I2C3 reset Set and cleared by software. 0: Clear the reset 1: Reset I2C3
18	UART7RST	UART7 reset Set and cleared by software. 0: Clear the reset 1: Reset UART7
17	UART6RST	UART6 reset Set and cleared by software. 0: Clear the reset 1: Reset UART6
16	DVPRST	DVP reset Set and cleared by software. 0: Clear the reset 1: Reset DVP
15	Reserved	Reserved, the reset value must be maintained.
14	USART1RST	USART1 reset Set and cleared by software. 0: Clear the reset 1: Reset USART1
13	TIM8RST	TIM8 timer reset Set and cleared by software. 0: Clear the reset 1: Reset TIM8 timer
12	SPI1RST	SPI1 reset Set and cleared by software. 0: Clear the reset 1: Reset SPI1

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Bit Field	Name	Description
11	TIM1RST	TIM1 timer reset Set and cleared by software. 0: Clear the reset 1: Reset TIM1 timer
10:9	Reserved	Reserved, the reset value must be maintained.
8	IOPGRST	GPIO port G reset. Set or cleared by software. 0: Clear the reset 1: Reset GPIO port G
7	IOPFRST	GPIO port F reset. Set or cleared by software. 0: Clear the reset 1: Reset GPIO port F
6	IOPERST	GPIO port E reset. Set or cleared by software. 0: Clear the reset 1: Reset GPIO port E
5	IOPDRST	GPIO port D reset. Set or cleared by software. 0: Clear the reset 1: Reset GPIO port D
4	IOPCRST	GPIO port C reset. Set or cleared by software. 0: Clear the reset 1: Reset GPIO port C
3	IOPBRST	GPIO port B reset. Set or cleared by software. 0: Clear the reset 1: Reset GPIO port B
2	IOPAMPRST	GPIO port A reset. Set or cleared by software. 0: Clear the reset 1: Reset GPIO port A
1	Reserved	Reserved, the reset value must be maintained.
0	AFIORST	Alternate function IO reset Set and cleared by software. 0: Clear the reset 1: Reset Alternate Function

6.3.6 APB1 Peripheral Reset Register (RCC_APB1PRST)

Address offset: 0x10

Reset value: 0x0000 0000

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved		DACRST	PWRRST	BKPRST	CAN2RST	CAN1RST	Reserved	USBRST	I2C2RST	I2C1RST	UART5 RST	UART4 RST	USART3 RST	USART2 RST	Reserved
		rw	rw	rw	rw	rw		rw	rw	rw	rw	rw	rw	rw	

15	14	13	12	11	10	6	5	4	3	2	1	0
SPI3RST	SPI2RST	Reserved		WWDG RST	Reserved		TIM7RST	TIM6RST	TIM5RST	TIM4RST	TIM3RST	TIM2RST
rw	rw			rw			rw	rw	rw	rw	rw	rw

Bit Field	Name	Description
31:30	Reserved	Reserved, the reset value must be maintained.
29	DACRST	DAC interface reset. Set or cleared by software. 0: Clear the reset 1: Reset the DAC interface
28	PWRRST	Power interface reset Set and cleared by software. 0: Clear the reset 1: Reset the power interface
27	BKPRST	Backup interface reset. Set or cleared by software. 0: Clear the reset 1: Reset the Backup interface
26	CAN2RST	CAN2 reset Set or cleared by software. 0: Clear the reset 1: Reset CAN2
25	CAN1RST	CAN1 reset Set or cleared by software. 0: Clear the reset 1: Reset CAN1
24	Reserved	Reserved, the reset value must be maintained.
23	USBRST	USB reset. Set or cleared by software. 0: clear the reset 1: Reset USB
22	I2C2RST	I2C2 reset Set and cleared by software. 0: Clear the reset 1: Reset I2C2
21	I2C1RST	I2C1 reset Set and cleared by software. 0: Clear the reset 1: Reset I2C1
20	UART5RST	UART5 reset. Set or cleared by software.

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Bit Field	Name	Description
		0: clear the reset 1: Reset UART5
19	UART4RST	UART4 reset Set and cleared by software. 0: Clear the reset 1: Reset UART4
18	USART3RST	USART3 reset. Set or cleared by software. 0: clear the reset 1: Reset USART3
17	USART2RST	USART2 reset Set and cleared by software. 0: Clear the reset 1: Reset USART2
16	Reserved	Reserved, the reset value must be maintained.
15	SPI3RST	SPI3 reset. Set or cleared by software. 0: clear the reset 1: Reset SPI3
14	SPI2RST	SPI2 reset. Set or cleared by software. 0: clear the reset 1: Reset SPI2
13:12	Reserved	Reserved, the reset value must be maintained.
11	WWDGRST	Window watchdog reset Set and cleared by software. 0: Clear the reset 1: Reset window watchdog
10:6	Reserved	Reserved, the reset value must be maintained.
5	TIM7RST	TIM7 timer reset. Set or cleared by software. 0: clear the reset 1: Reset the TIM7 timer
4	TIM6RST	TIM6 timer reset Set and cleared by software. 0: Clear the reset 1: Reset TIM6 timer
3	TIM5RST	TIM5 timer reset Set and cleared by software. 0: Clear the reset 1: Reset TIM5 timer
2	TIM4RST	TIM4 timer reset Set and cleared by software.

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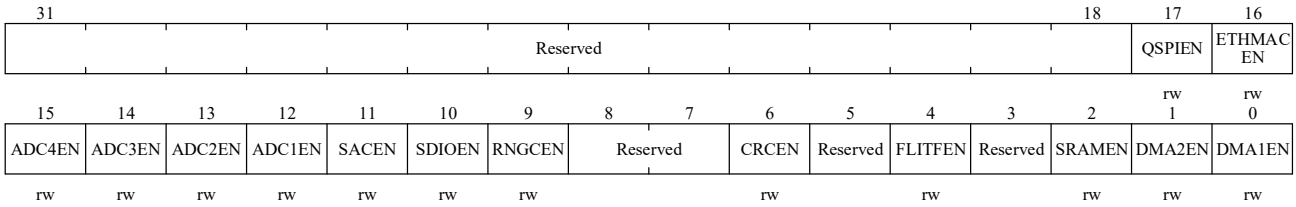
Bit Field	Name	Description
		0: Clear the reset 1: Reset TIM4 timer
1	TIM3RST	TIM3 timer reset Set and cleared by software. 0: Clear the reset 1: Reset TIM3 timer
0	TIM2RST	TIM2 timer reset Set and cleared by software. 0: Clear the reset 1: Reset TIM2 timer

6.3.7 AHB Peripheral Clock Enable Register (RCC_AHBPCLKEN)

Address offset: 0x14

Reset value: 0x0000 0014



Bit Field	Name	Description
31:18	Reserved	Reserved, the reset value must be maintained.
17	QSPIEN	QSPI clock enable Set and cleared by software. 0: QSPI clock disabled 1: QSPI clock enabled
16	ETHMACEN	ETHMAC clock enable Set and cleared by software. 0: ETHMAC clock disabled 1: ETHMAC clock enabled
15	ADC4EN	ADC4 clock enable Set and cleared by software. 0: ADC4 clock disabled 1: ADC4 clock enabled
14	ADC3EN	ADC3 clock enable Set and cleared by software. 0: ADC3 clock disabled 1: ADC3 clock enabled
13	ADC2EN	ADC2 clock enable

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Bit Field	Name	Description
		Set and cleared by software. 0: ADC2 clock disabled 1: ADC2 clock enabled
12	ADC1EN	ADC1 clock enable Set and cleared by software. 0: ADC1 clock disabled 1: ADC1 clock enabled
11	SACEN	SAC clock enable Set and cleared by software. 0: SAC clock disabled 1: SAC clock enabled
10	SDIOEN	SAC clock enable Set and cleared by software. 0: SAC clock disabled 1: SAC clock enabled
9	RNGCEN	RNGC clock enable Set and cleared by software. 0: RNGC clock disabled 1: RNGC clock enabled
8:7	Reserved	Reserved, the reset value must be maintained.
6	CRCEN	CRC clock enable Set and cleared by software. 0: CRC clock disabled 1: CRC clock enabled
5	Reserved	Reserved, the reset value must be maintained.
4	FLITFEN	Flash interface circuit clock enable. Set or cleared by software. 0: Disable the clock of the flash interface circuit 1: Enable the clock of the flash interface circuit
3	Reserved	Reserved
2	SRAMEN	SRAM interface clock enable Set and cleared by software to disable/enable SRAM interface clock during Sleep mode. 0: SRAM interface clock disabled during Sleep mode. 1: SRAM interface clock enabled during Sleep mode
0	DMA2EN	DMA2 clock enable Set and cleared by software.

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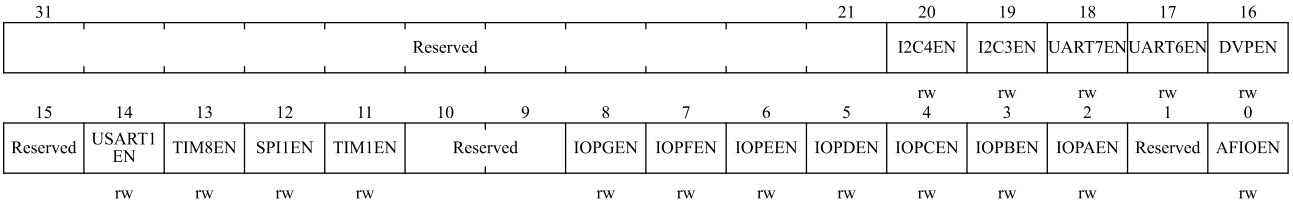
Bit Field	Name	Description
		0: DMA2 clock disabled 1: DMA2 clock enabled
0	DMA1EN	DMA1 clock enable Set and cleared by software. 0: DMA1 clock disabled 1: DMA1 clock enabled

6.3.8 APB2 Peripheral Clock Enable Register (RCC_APB2PCLKEN)

Address offset: 0x18

Reset value: 0x0000 0000



Bit Field	Name	Description
31:21	Reserved	Reserved, the reset value must be maintained.
20	I2C4EN	I2C4 clock enable Set and cleared by software. 0: I2C4 clock disabled 1: I2C4 clock enabled
19	I2C3EN	I2C3 clock enable Set and cleared by software. 0: I2C3 clock disabled 1: I2C3 clock enabled
18	UART7EN	UART7 clock enable Set and cleared by software. 0: UART7 clock disabled 1: UART7 clock enabled
17	UART6EN	UART6 clock enable Set and cleared by software. 0: UART6 clock disabled 1: UART6 clock enabled

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Bit Field	Name	Description
16	DVPEN	DVP clock enable Set and cleared by software. 0: DVP clock disabled 1: DVP clock enabled
15	Reserved	Reserved, the reset value must be maintained.
14	USART1EN	USART1 clock enable Set and cleared by software. 0: USART1 clock disabled 1: USART1 clock enabled
13	TIM8EN	TIM8 Timer clock enable Set and cleared by software. 0: TIM8 timer clock disabled 1: TIM8 timer clock enabled
12	SPI1EN	SPI1 clock enable Set and cleared by software. 0: SPI1 clock disabled 1: SPI1 clock enabled
11	TIM1EN	TIM1 timer clock enable Set and cleared by software. 0: TIM1 timer clock disabled 1: TIM1 timer clock enabled
10:9	Reserved	Reserved, the reset value must be maintained.
8	IOPGEN	IO Port G clock enable Set and cleared by software. 0: IO Port G clock disabled 1: IO Port G clock enabled
7	IOPFEN	IO Port F clock enable Set and cleared by software. 0: IO Port F clock disabled 1: IO Port F clock enabled
6	IOPEEN	IO Port E clock enable Set and cleared by software. 0: IO Port E clock disabled 1: IO Port E clock enabled
5	IOPDEN	IO Port D clock enable Set and cleared by

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Bit Field	Name	Description
		software. 0: IO Port D clock disabled 1: IO Port D clock enabled
4	IOPCEN	IO Port C clock enable Set and cleared by software. 0: IO Port C clock disabled 1: IO Port C clock enabled
3	IOPBEN	IO Port B clock enable Set and cleared by software. 0: IO Port B clock disabled 1: IO Port B clock enabled
2	IOPAEN	IO Port A clock enable Set and cleared by software. 0: IO Port A clock disabled 1: IO Port A clock enabled
1	Reserved	Reserved, the reset value must be maintained.
0	AFIOEN	Alternate function IO clock enable Set and cleared by software. 0: Alternate Function IO clock disabled 1: Alternate Function IO clock enabled

6.3.9 APB1 Peripheral Clock Enable Register (RCC_APB1PCLKEN)

Address offset: 0x1c

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
OPAMP EN	Reserved	DACEN	PWREN	BKPEN	CAN2EN	CAN1EN	Reserved	USBEN	I2C2EN	I2C1EN	UART5EN	UART4EN	USART3 EN	USART2 EN	Reserved
rw		rw	rw	rw	rw	rw		rw	rw	rw	rw	rw	rw	rw	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SPI3EN	SPI2EN	Reserved		WWDG EN	TSCEN	Reserved		COMP FILTEN	COMPEN	TIM7EN	TIM6EN	TIM5EN	TIM4EN	TIM3EN	TIM2EN
rw	rw			rw	rw			rw	rw	rw	rw	rw	rw	rw	rw

Bit Field	Name	Description
31	OPAMPEN	OPAMP clock enable. Set or cleared by software. 0: Disable OPAMP clock 1: Enable OPAMP clock
30	Reserved	Reserved, the reset value must be maintained.
29	DACEN	DAC interface clock enable

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Bit Field	Name	Description
		Set and cleared by software. 0: DAC interface clock disabled 1: DAC interface clock enable
28	PWREN	Power interface clock enable Set and cleared by software. 0: Power interface clock disabled 1: Power interface clock enable
27	BKPEN	Backup interface clock enable Set and cleared by software. 0: Backup interface clock disabled 1: Backup interface clock enabled
26	CAN2EN	CAN2 clock enable Set and cleared by software. 0: CAN2 clock disabled 1: CAN2 clock enabled
25	CAN1EN	CAN1 clock enable Set and cleared by software. 0: CAN1 clock disabled 1: CAN1 clock enabled
24	Reserved	Reserved, the reset value must be maintained.
23	USBEN	USB clock enable Set and cleared by software. 0: USB clock disabled 1: USB clock enabled
22	I2C2EN	I2C2 clock enable Set and cleared by software. 0: I2C2 clock disabled 1: I2C2 clock enabled
21	I2C1EN	I2C1 clock enable Set and cleared by software. 0: I2C1 clock disabled 1: I2C1 clock enabled
20	UART5EN	UART5 clock enable Set and cleared by software. 0: UART5 clock disabled 1: UART5 clock enabled

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Bit Field	Name	Description
19	UART4EN	UART4 clock enable Set and cleared by software. 0: UART4 clock disabled 1: UART4 clock enabled
18	USART3EN	USART2 clock enable Set and cleared by software. 0: USART3 clock disabled 1: USART3 clock enabled
17	USART2EN	USART2 clock enable Set and cleared by software. 0: USART2 clock disabled 1: USART2 clock enabled
16	Reserved	Reserved, the reset value must be maintained.
15	SPI3EN	SPI3 clock enable Set and cleared by software. 0: SPI3 clock disabled 1: SPI3 clock enabled
14	SPI2EN	SPI2 clock enable Set and cleared by software. 0: SPI2 clock disabled 1: SPI2 clock enabled
13:12	Reserved	Reserved, the reset value must be maintained.
11	WWDGEN	Window watchdog clock enable Set and cleared by software. 0: Window watchdog clock disabled 1: Window watchdog clock enabled
10:8	Reserved	Reserved, the reset value must be maintained.
7	COMPFILTEN	COMP Filter clock enable Set and cleared by software. 0: COMP Filter clock disabled 1: COMP Filter clock enabled
6	COMPEN	COMP clock enable Set and cleared by software. 0: COMP clock disabled 1: COMP clock enabled
5	TIM7EN	TIM7 timer clock enable Set and cleared by software.

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Bit Field	Name	Description
		0: TIM7 clock disabled 1: TIM7 clock enabled
4	TIM6EN	TIM6 timer clock enable Set and cleared by software. 0: TIM6 clock disabled 1: TIM6 clock enabled
3	TIM5EN	TIM5 timer clock enable Set and cleared by software. 0: TIM5 clock disabled 1: TIM5 clock enabled
2	TIM4EN	TIM4 timer clock enable Set and cleared by software. 0: TIM4 clock disabled 1: TIM4 clock enabled
1	TIM3EN	TIM3 timer clock enable Set and cleared by software. 0: TIM3 clock disabled 1: TIM3 clock enabled
0	TIM2EN	TIM2 timer clock enable Set and cleared by software. 0: TIM2 clock disabled 1: TIM2 clock enabled

6.3.10 Backup Domain Control Register (RCC_BDCTRL)

Address offset: 0x20

Reset value: 0x0000 0000

Bit Field	Name	Description
31:17	Reserved	Reserved, the reset value must be maintained.
16	BDSFTRST	Backup domain software reset.

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Bit Field	Name	Description
		Set or cleared by software. 0: No effect 1: Reset the entire backup domain
15	RTCEN	RTC clock enable Set and cleared by software. 0: Disable RTC clock 1: Enable RTC clock
14:10	Reserved	Reserved, the reset value must be maintained.
9:8	RTCSEL[1:0]	RTC clock source selection Set by software to select RTC clock source. Once the RTC clock source is selected, it cannot be changed until the next backup domain is reset. These bits can be reset by setting the BDSFTRST bit. 00: No clock 01: LSE oscillator selected as RTC clock 10: LSI oscillator selected as RTC clock 11: HSE oscillator divided by 128 selected as RTC clock
7:3	Reserved	Reserved, the reset value must be maintained.
2	LSEBP	External low-speed oscillator bypass In debug mode, set and cleared by software to bypass oscillator. This bit can only be written when the external low-speed oscillator is disabled. 0: LSE oscillator not bypassed 1: LSE oscillator bypassed
1	LSERD	External low-speed clock oscillator ready Set and cleared by hardware to indicate if the LSE oscillator is ready. After the LSEEN bit is cleared, LSERD goes low after 6 cycles of the LSE clock. 0: External low-speed oscillator not ready 1: External low-speed oscillator ready
0	LSEEN	External low-speed clock oscillator enable Set and cleared by software. 0: Disable the external low-speed oscillator 1: Enable the external low-speed oscillator.

Note: The RCC_BDCTRL.LSEEN, RCC_BDCTRL.LSEBP, RCC_BDCTRL.RTCSEL and RCC_BDCTRL.RTCEN bits are in the backup domain. Therefore, these bits are write-protected after reset and can only be changed after the PWR_CTRL.DBKP bit is set. These bits can only be cleared by a backup domain reset. Any internal or external reset will not affect these bits.

6.3.11 Clock Control/Status Register (RCC_CTRLSTS)

Address offset: 0x24

Reset value: 0x0C000003

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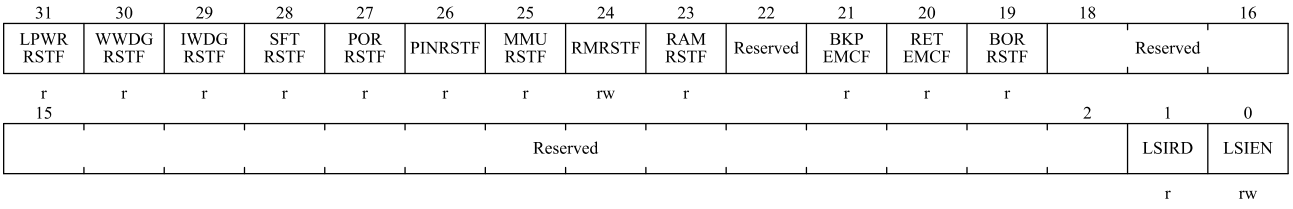

Bit Field	Name	Description
31	LPWRRSTF	Low power reset flag Set by hardware when a low-power management reset occurs. Cleared by software by writing to the RMRSTF bit. 0: No low-power management reset occurred 1: A low-power management reset occurred
30	WWDGRSTF	Window watchdog reset flag Set by hardware when a window watchdog reset occurs. Cleared by software by writing to the RMRSTF bit. 0: No windowed watchdog reset occurred 1: Window watchdog reset occurred
29	IWDGRSTF	Independent watchdog reset flag Set by hardware when an independent watchdog reset occurs Cleared by software by writing to the RMRSTF bit. 0: No independent watchdog reset occurred 1: Independent watchdog reset occurred
28	SFTRSTF	Software reset flag Set by hardware when a software reset occurs. Cleared by software by writing to the RMRSTF bit. 0: No software reset occurred 1: Software reset occurred
27	PORRSTF	Power-on/power-down reset flag Set by hardware when a power-on/power-down reset occurs Cleared by software by writing to the RMRSTF bit. 0: No power on/power off reset occurred 1: Power-on/power-off reset occurred
26	PINRSTF	External pin reset flag Set by hardware when a reset from the NRST pin occurs. Cleared by software by writing to the RMRSTF bit. 0: No NRST pin reset occurred 1: NRST pin reset occurred
25	MMURSTF	MMU reset flag Set by hardware when MMU reset occurs. Cleared by software by writing to the RMRSTF bit. 0: No MMU reset occurred 1: MMU reset occurred
24	RMRSTF	Clear the reset flag Set by the software to clear the reset flag.

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Bit Field	Name	Description
		0: No effect 1: Clear the reset flag
23	RAMRSTF	RAM reset flag. Set by hardware when a RAM reset occurs and cleared by software by writing to the RMRSTF bit. 0: No RAM reset occurred 1: A RAM reset has occurred
22	Reserved	Reserved, the reset value must be maintained.
21	BKPEMCF	Backup domain EMC reset flag. Set by hardware when a backup domain EMC reset occurs, and cleared by software writing the RMRSTF bit. 0: No backup domain EMC reset occurred 1: A backup domain EMC reset has occurred
20	RETEMCF	Retention domain EMC reset flag. Set by hardware when a Retention domain EMC reset occurs, and cleared by software writing the RMRSTF bit. 0: No Retention domain EMC reset occurred 1: A Retention domain EMC reset has occurred
19	BORRSTF	BOR reset flag Set by hardware when a BOR reset occurs, and cleared by software writing the RMRSTF bit. 0: No BOR reset occurred 1: A BOR reset has occurred
18:2	Reserved	Reserved, the reset value must be maintained.
1	LSIRD	Internal low-speed oscillator ready Set and cleared by hardware to indicate if the internal RC 40 KHz oscillator is ready. After LSIEN is cleared, LSIRD goes low after 3 internal RC 40 KHz oscillator clock cycles. 0: Internal 40KHz RC oscillator clock not ready 1: Internal 40KHz RC oscillator clock ready
0	LSIEN	Internal low-speed oscillator enable Set and cleared by software. 0: Disable the internal RC 40 kHz oscillator 1: Enable the internal RC 40 kHz oscillator

6.3.12 AHB Peripheral Reset Register (RCC_AHBPRST)

Address offset: 0x28

Reset value: 0x0000 0000

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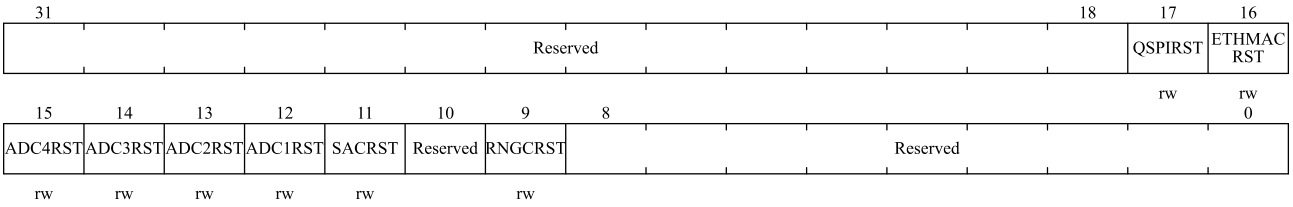

Bit Field	Name	Description
31:18	Reserved	Reserved, the reset value must be maintained.
17	QSPIRST	QSPI reset Set and cleared by software. 0: Clear the reset 1: Reset QSPI
16	ETHMACRST	ETHMAC reset Set and cleared by software. 0: Clear the reset 1: Reset ETHMAC
15	ADC4RST	ADC4 reset Set and cleared by software. 0: Clear the reset 1: Reset ADC4
14	ADC3RST	ADC3 reset Set and cleared by software. 0: Clear the reset 1: Reset ADC3
13	ADC2RST	ADC2 reset Set and cleared by software. 0: Clear the reset 1: Reset ADC2
12	ADC1RST	ADC1 reset Set and cleared by software. 0: Clear the reset 1: Reset ADC1
11	SACRST	SAC reset Set and cleared by software.

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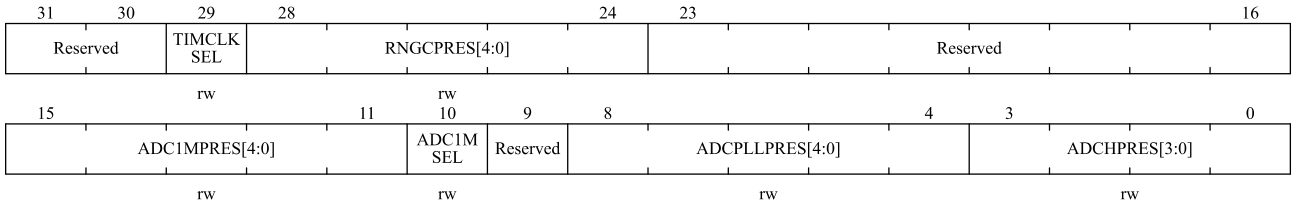
Bit Field	Name	Description
		0: Clear the reset 1: Reset SAC
10	Reserved	Reserved, the reset value must be maintained.
9	RNGCRST	RNGC reset Set and cleared by software. 0: Clear the reset 1: Reset RNGC
8:0	Reserved	Reserved, the reset value must be maintained.

6.3.13 Clock Configuration Register 2 (RCC_CFG2)

Address offset: 0x2c

Reset value: 0x0000 3800



Bit Field	Name	Description
31:30	Reserved	Reserved, the reset value must be maintained.
29	TIMCLKSEL	TIM1/8 clock source selection Set and cleared by software. 0: PCLK2 is selected as TIM1/8 clock source if APB2 prescaler is 1. Otherwise, PCLK2 × 2 is selected. 1: SYSCLK input clock is selected as TIM1/8 clock source.
28:24	RNGCPRES[4:0]	RNGC prescaler. Software sets or clears these bits to configure the prescale factor for the RNGC clock. 00000: SYSCLK is not divided 00001: SYSCLK divided by 2 00010: SYSCLK divided by 3 ... 11110: SYSCLK divided by 31 11111: SYSCLK divided by 32
23:16	Reserved	Reserved, the reset value must be maintained.
15:11	ADC1MPRES[4:0]	ADC 1M clock prescaler Set and cleared by software to configure the division factor of ADC 1M clock source. 00000: ADC 1M clock source not divided

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Bit Field	Name	Description
		00001: ADC 1M clock source divided by 2 00010: ADC 1M clock source divided by 3 ... 11110: ADC 1M clock source divided by 31 11111: ADC 1M clock source divided by 32 *Note: ADC clock must be configured to 1M*
10	ADC1MSEL	ADC 1M clock source selection. Set or cleared by software. 0: Select HSI oscillator clock as the input clock of ADC 1M 1: Select HSE oscillator clock as the input clock of ADC 1M
9	Reserved	Reserved, the reset value must be maintained.
8:4	ADCPLLPRES[4:0]	ADC PLL prescaler Set and cleared by software to configure the division factor from the PLL clock to the ADC. 0xxxx: ADC PLL clock is disabled 10000: PLL clock not divided 10001: PLL clock divided by 2 10010: PLL clock divided by 4 10011: PLL clock divided by 6 10100: PLL clock divided by 8 10101: PLL clock divided by 10 10110: PLL clock divided by 12 10111: PLL clock divided by 16 11000: PLL clock divided by 32 11001: PLL clock divided by 64 11010: PLL clock divided by 128 11011: PLL clock divided by 256 Others: PLL clock divided by 256
3:0	ADCHPRES[3:0]	ADC HCLK prescaler Set and cleared by software to configure the division factor from the HCLK clock to the ADC. 0000: HCLK clock not divided 0001: HCLK clock divided by 2 0010: HCLK clock divided by 4 0011: HCLK clock divided by 6 0100: HCLK clock divided by 8 0101: HCLK clock divided by 10 0110: HCLK clock divided by 12 0111: HCLK clock divided by 16 1000: HCLK clock divided by 32 Others: HCLK clock divided by 32

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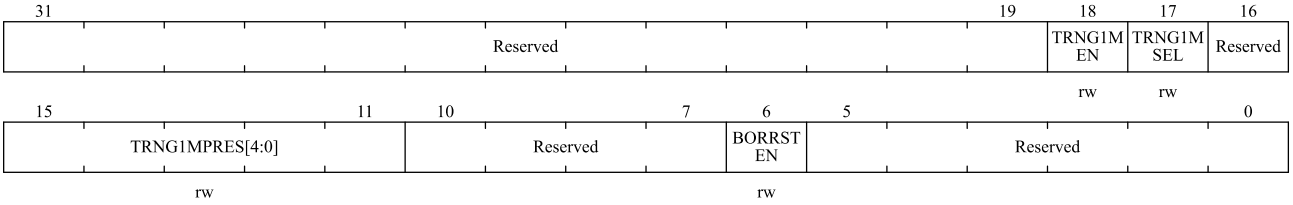
6.3.14 Clock Configuration Register 3 (RCC_CFG3)

Address offset: 0x30

Reset value: 0x0000 3800



Bit Field	Name	Description
31:19	Reserved	Reserved, the reset value must be maintained.
18	TRNG1MEN	TRNG analog interface clock enable. Set or cleared by software. 0: Disable TRNG analog interface clock 1: Enable TRNG analog interface clock
17	TRNG1MSEL	TRNG 1M clock selection. Set or cleared by software. 0: Select HSI oscillator as TRNG 1M input clock 1: Select HSE oscillator as TRNG 1M input clock
16	Reserved	Reserved, the reset value must be maintained.
15:11	TRNG1MPRES[4:0]	TRNG 1M clock prescaler. Software sets or clears these bits to generate the TRNG 1M clock. 0000x: TRNG 1M clock source divided by 2 0001x: TRNG 1M clock source divided by 4 0010x: TRNG 1M clock source divided by 6 0011x: TRNG 1M clock source divided by 8 0100x: TRNG 1M clock source divided by 10 ... 1111x: TRNG 1M clock source divided by 32
10:7	Reserved	Reserved, the reset value must be maintained.
6	BORRSTEN	BOR reset enable Set and cleared by software. 0: Disable BOR reset 1: Enable BOR reset
5:0	Reserved	Reserved, the reset value must be maintained.

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7 GPIO and AFIO

7.1 Summary

GPIO is general purpose input/output, and AFIO is alternate function input/output. Up to 97 GPIO are supported on the chip, which are divided into 7 groups (GPIOA/GPIOB/GPIOC/GPIOD/GPIOE/GPIOF/GPIOG) with 16 ports in each group (10 in group F and 7 in group G). GPIO port and other alternate peripherals share pins, which can be configured by users according to requirements. Each GPIO pin can be independently configured as an output, input or alternate peripheral function port. Except for the analog function pin, all other GPIO pins have the ability to pass large current.

GPIO ports can be configured in the following modes by software:

- Input floating
- Input pull-up
- Input pull-down
- Analog function
- Open drain output
- Push-pull output
- Push-pull alternate function
- Open-drain alternate function

Each I/O port bit can be programmed arbitrarily, but the I/O port register must be accessed as a 32-bit word (16-bit half word or 8-bit byte access is not allowed). The figure below shows the basic structure of an I/O port.

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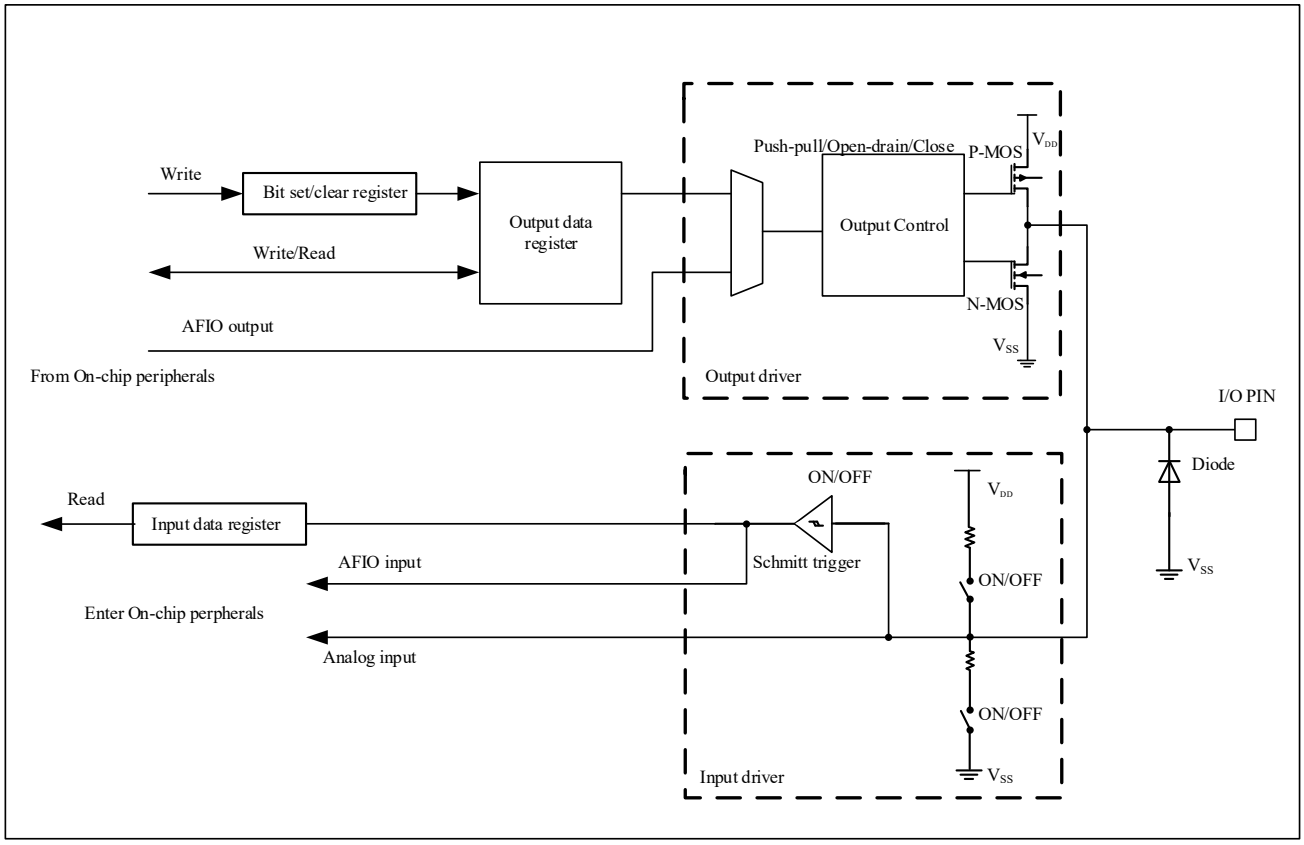
Figure 7-1 Basic structure of I/O port



7.2 I/O Function Description

7.2.1 I/O Mode Configuration

I/O mode control is set by configuration registers GPIOx_PL_CFG, GPIOx_PH_CFG and output register GPIOx_POD(x=A,B,C,D,E,F,G). The I/O configurations in different operation modes are shown in the following table:

Table 7-1 I/O mode and configuration relationship

Configuration mode		PCFG1	PCFG0	PMODE1	PMODE0	PODx register
Universal output	Push-Pull	0	0	01: 10MHz max 10: 2MHz max 1: 50MHz max		0 or 1
	Open-Drain		1			0 or 1
Alternate function output	Push-Pull	1	0			Not use
	Open-Drain		1			Not use
Input	Analog mode	0	0	00: reserved		Not use
	Input floating		1			Not use
	Input pull-down	1				0
	Input pull-up		0			1

I/O characteristics under different configurations are shown in the following table:

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Table 7-2 I/O characteristics of different I/O configurations

Characteristic	GPIO input	GPIO output	Analog mode	Peripheral alternate
Output buffer	Disable	Enable	Disable	According to peripheral function configuration
Schmitt trigger	Enable	Enable	Disable The output value is forced to 0.	According to peripheral function configuration
Pull up/Pull down/floating	Configurable	Disable	Disable	According to peripheral function configuration
Open-drain mode	Disable	Configurable, GPIO outputs 0 when the data is "0" and high impedance when he data is "1"	Disable	Configurable, GPIO outputs 0 when the data is "0" and high impedance when he data is "1".
Input data register (I/O status)	Read-write	Readable	Read as 0.	Readable
Output data register (write value)	Invalid	Read-write	Invalid	Readable

7.2.1.1 Input mode

When I/O port is configured in input mode:

- The data that appears on the I/O pin is sampled to the input data register on each APB2 clock.
- Read access to the input data register can get I/O status.
- Output buffer is disabled.
- Schmidt trigger input is activated.
- Weak pull-up and pull-down resistors are connected according to the input configuration (pull-up, pull-down or floating).

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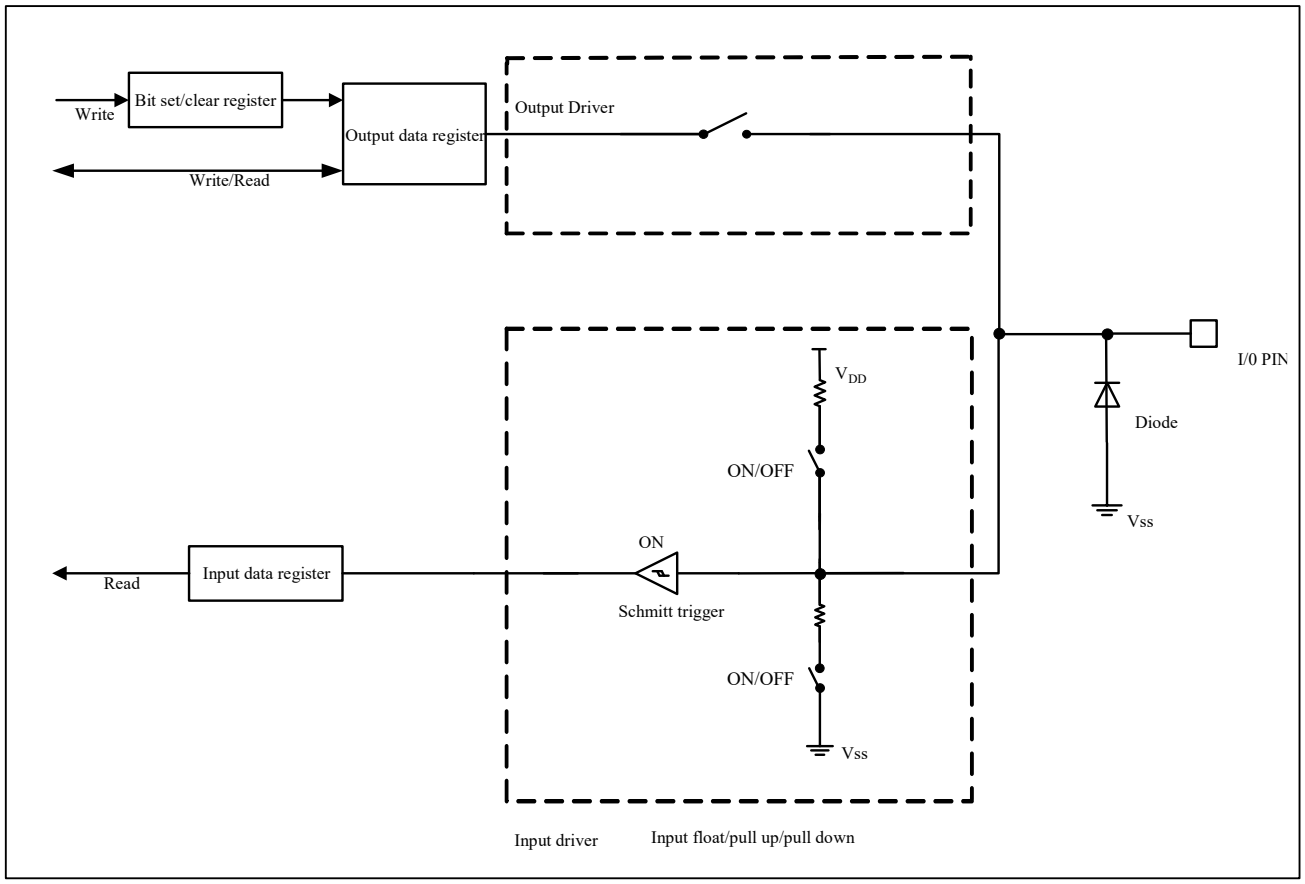
Figure 7-2 Input float/pull-up/pull-down configuration



7.2.1.2 Output mode

When I/O port is configured as output mode:

- Schmidt trigger input is activated
- Weak pull-up and pull-down resistors are disabled.
- Output buffer is activated.
  - Open-drain mode: '0' on the output register activates N-MOS, and the pin outputs low level.
    '1' port on the output register make the pin in a high impedance state (P-MOS is never activated)
  - Push-pull mode: '0' on the output register activates N-MOS, and the pin outputs low level.
    '1' on the output register activates P-MOS, and the pin outputs high level.
- The data appearing on the I/O pin is sampled to the input data register at every APB2 clock cycle..
- Read access to the input data register can get I/O status.
- The read access to the output data register gets the last written value.

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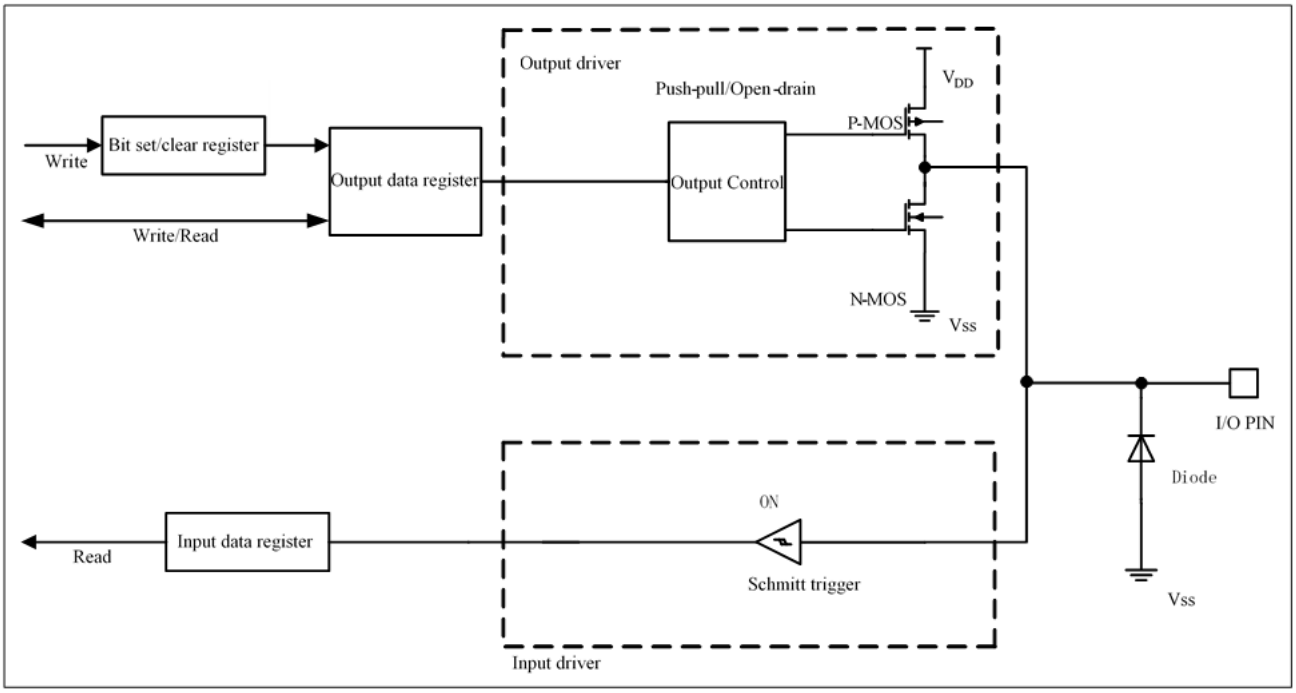
Figure 7-3 Output mode configuration



7.2.1.3 Alternate function mode

When I/O ports are configured for alternate function mode:

- Schmidt trigger input is activated.
- Weak pull-up and pull-down resistors are disabled.
- In the open-drain or push-pull configuration, the output buffer is turned on.
- Signals of built-in peripherals drive the output buffer.
- The data appearing on the I/O pin is sampled to the input data register at every APB2 clock cycle.
- I/O status can be obtained by reading and accessing the input data register.
- The read access to the output data register gets the last written value.

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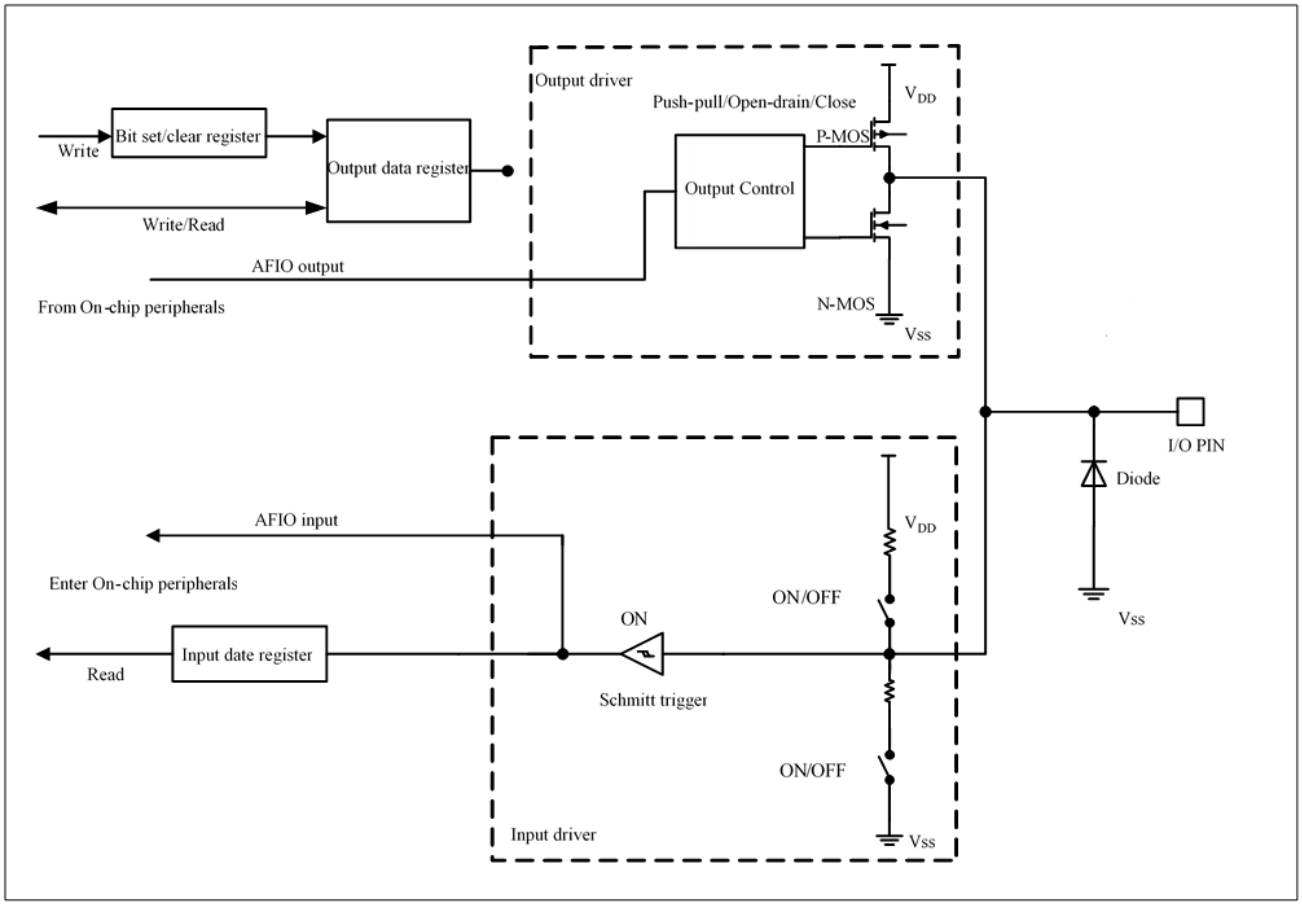
Figure 7-4 Alternate function configuration



7.2.1.4 Analog mode

When the I/O port is configured in analog mode:

- Weak pull-up and pull-down resistors are disabled.
- Read access to the input data register gets the value “0”.
- Output buffer is disabled.
- Schmidt trigger input is disabled and output value is forced to '0' (zero consumption on each analog I / O pin is achieved)

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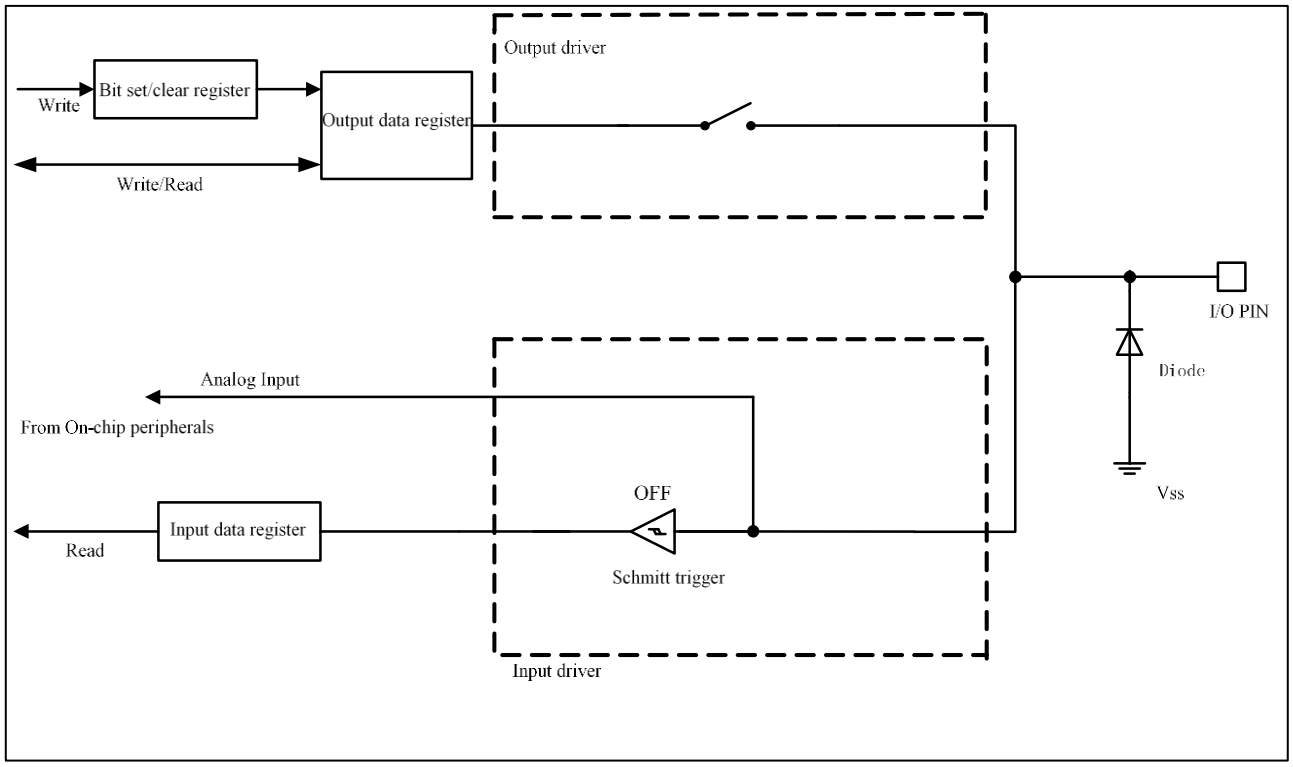
Figure 7-5 High impedance analog mode configuration



7.2.2 Status after Reset

During and just after the reset, the alternate functions are not active, and the I/O port is configured to be in analog mode (PCFGy[1:0]=00b，PMODEy[1:0]=00b) by default. But there are several exceptional signals:

- BOOT0、NRST、OSC_IN、OSC_OUT has no GPIO function by default
  - BOOT0 pin default configuration is input pull down
  - NRST pull up input and output
- After the reset, the default state of the pin associated with the debug system is to enable the SWD-JTAG, and the JTAG pin is placed on the input pull-up or pull-down mode
  - PA15: JTDI is placed in input pull-up mode
  - PA14: JTCK is placed in input pull-down mode
  - PA13: JTMS is placed in input pull-up mode
  - PB4: NJTRST is placed in input pull-up mode
  - PB3:JTD0 is placed in the push-pull output without pull-down.
- PD0 and PD1:
  - PD0 and PD1 default to analog mode in 80 and above pin packages.
  - PD0 and PD1 are multiplexed to OSC_IN/OUT for pin packages with less than 80 pins.
- PC13、PC14、PC15：

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  - PC13~15 are the three IOs in the backup domain. After the backup domain is powered on for the first time, these three IOs default to analog mode;.

- PB2/BOOT1：
  - PB2/BOOT1 is in the pull-down input state by default;
  - BOOT0 default configuration is input pull-down. Refer to the following Table (If the BOOT pins are not connected, the main flash storage area is selected by default).

Start mode select pin		Start mode	Description
BOOT1	BOOT0		
x	0	Main flash memory	The main flash memory serves as the boot area.
0	1	System memory	System memory as boot area
1	1	Built in SRAM	Built-in SRAM as startup area

7.2.3 Individual Bit Setting and Bit Clearing

By writing '1' to the bit to be changed in the set register (GPIOx_PBSC) and reset register (GPIOx_PBC), the individual bit operation of the data register (GPIOx_POD) can be realized, and one or more bits can be set/reset. The bit written with '1' is set or cleared accordingly, and the bit not written with '1' will not be changed. The software does not need to disable interrupts, and is completed in a single APB2 write operation.

7.2.4 External Interrupt/Wake-up line

All ports have external interrupt capability, which can be configured in EXTI module:

- The port must be configured in input mode.
- All ports can be configured for wake-up in SLEEP/STOP0/STOP2 mode, and the rising or falling edge can be configured.
- PA0 can be used to wake up in STANDBY mode.
- The general purpose I/O port (as shown in External interrupt GPIO mapping) is connected to 16 external interrupt/event lines and is configured by register AFIO_EXTI_CFGx.

7.2.5 Alternate Function

When I/O ports are configured for alternate function mode, the port bit configuration register (GPIOx_PL_CFG/ GPIOx_PH_CFG) must be programmed before use, as follows:

- Input alternate function: The port must be configured in input mode (floating, pull-up or pull-down) and the input pin must be externally driven.
- Output alternate function: The port must be configured to alternate output mode (push-pull or open-drain).
- Bidirectional alternate function: The port bit must be configured with the alternate function output mode (push-pull or open-drain). At this time, the input driver is configured to input floating mode.

In the output alternate function mode, the pin is disconnected from the output data register and connected with the

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output signal of the on-chip peripheral. If the software configures a GPIO pin as output alternate function, but the peripheral is not activated, then its output will be uncertain.

7.2.5.1 Clock output MCO

The microcontroller allows the clock signal to be output to the external MCO pin (PA8). PA8 must be configured to push-pull alternate output function mode. The following four clock signals can be selected as MCO clocks, and the selection of the clock is controlled by RCC_CFG.MCO[2:0] bits:

- SYSCLK divided clock
- HSI
- HSE
- PLL divided clock

7.2.5.2 Software remapping I/O alternate function

In order to expand the flexibility of alternate peripheral functions under different device packages, some peripheral alternate functions can be remapped to other pins. You can configure the corresponding register (AFIO_RMP_CFG, AFIO_RMP_CFGx) by software. At this time, the alternate function is disconnected from its original pin and remapped to the new pin.

7.2.5.3 Functional remapping of backup domain pins PC13~PC15

7.2.5.3.1 Functional description of backup power domain pins PC13~PC15

PC13~PC15 pins are located in the backup domain and can be used in GPIO mode or alternate function mode:

- When the backup domain is powered by VDD (internal analog switch connected to VDD), the following functions are available:
  - PC14 and PC15 can be used for GPIO or LSE pins.
  - PC13 can be used as a general-purpose I/O port, TAMPER pin, RTC calibration clock, RTC alarm clock or second output (see backup register 5.4 chapter)

Note: Because the analog switch can only pass low current (3mA), the functions of I/O ports of PC13, PC14, PC15 in the output mode are limited: the speed must be limited below 2MHz, the maximum load is 30pF, and these I/O ports must not be used as current sources (such as driving LEDs).

- When the backup domain is powered by VBAT (the analog switch is connected to VBAT after VDD is off), the following functions can be used:
  - PC14 and PC15 can only be used for LSE pins.
  - PC13 can be used as a TAMPER pin, RTC alarm clock or second output (see 14.2.8), and output RTC calibration clock, RTC alarm clock pulse or second pulse on PC13 pin (when this pin is not used for intrusion detection). For the convenience of measurement, the RTC clock can be divided by 64 and output to the intrusion detection pin TAMPER. Turn on this function by setting the RTC_CTRL.COEN bit.

7.2.5.3.2 PC13~PC15 function mapping

According to the previous description, the configuration conditions of different modes of PC13~PC15 are sorted out as follows:

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PC14 and PC15	condition	PAD mode configuration
GPIO mode	LSE is off, the backup domain is powered by VDD, and it can only be used in GPIO mode when the 1.1V power supply is turned off without entering the low power mode(Standby, Stop2)	The mode of GPIO depends on the application.
LSE mode	The LSE priority is high, and the LSE mode will be entered if the above conditions are not met.	Analog mode
PC13	condition	PAD mode configuration
GPIO mode	The backup domain is powered by VDD, and can only be used in GPIO mode when the 1.1V power supply is turned off without entering the the low power mode(Standby, Stop2)	The mode of GPIO depends on the application.
TAMPER pin	You can configure this input at any time.	Input floating
RTC calibration clock, RTC alarm clock pulse or second pulse	When this pin is not used for intrusion detection, it can be used to output RTC calibration clock, RTC alarm clock pulse or second pulse, so the priority is lower than the TAMPER function.	Alternate push-pull output

From the above, the power domain division managed by the three pins PC13~PC15:

- GPIOx_PH_CFG/GPIOx_PID/GPIOx_POD/GPIOx_PBSC/GPIOx_PBC/GPIOx_PLOCK_CFG and other GPIO related configuration registers are in the Core power domain;
- The Mux logic of these three pins are in VBAT domain, and the default mode is GPIO input floating mode; PC14 and PC15 decide which mode and Mux they are in according to LSEEN, backup domain power supply control signal, chip mode signal, GPIOC_PH_CFG, TAMPER and clock output control.

Note: The control signal of whether the backup domain is powered by VDD or VBAT is automatically switched by PWR module, which should be obtained by POR signal of VDD domain.

7.2.5.4 Use the OSC_IN/OSC_OUT pin as the GPIO port PD0/PD1

If the external high-speed oscillator is not turned on in the application, the pin OSC_IN/OSC_OUT can be used as PD0/PD1 of GPIO, which is realized by setting the alternate remapping and debugging I/O configuration register (AFIO_RMP_CFG), as described below:

Bit 15	PD01_RMP: PD0/ PD1 is mapped to OSC_ in/OSC_out (PD0/PD1 mapping on OSC_IN/OSC_OUT) This bit can be set to '1' or '0' by software. It controls the GPIO function image of PD0 and PD1. PD0 and PD1 can be mapped to the OSC_IN and OSC_OUT pins when the main oscillator HSE is not used (the system runs on the internal 8MHz RC oscillator). 0: Do not remap PD0 and PD1; 1:PD0 is mapped to OSC _ in, and pd1 is mapped to OSC_OUT.

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	This function can only be applied to 48-pin and 64-pin packages (there are PD0 and PD1 on 80-pin, 100-pin and 128-pin packages, and there is no need to remap them).

Note: The external interrupt/event function has not been remapped. On 48-pin and 64-pin packages, PD0 and PD1 cannot be used to generate external interrupts/events. That is, for LQFP48/64 package, there are only two pins OSC_IN and OSC_OUT (without PD0 and PD1), which can be mapped to PD0 and PD1 when external crystal oscillator is not used. For 80-pin and above packages, PD0 and PD1 pins are available, and OSC_IN and OSC_OUT are available, so there is no need to remap PD0/ PD1 to OSC_IN/OSC_OUT.

7.2.5.5 JTAG/SWD alternate function remapping

The SWD-JTAG debug interface is enabled by default when the chip is powered on, and the debug interface is mapped to the GPIO port, as shown in the following Table.

Alternate function	GPIO port
JTMS/SWDIO	PA13
JTCK/SWCLK	PA14
JTDI	PA15
JTDO	PB3
NJTRST	PB4

If you need to use its GPIO function during debugging, you can set the AFIO_RMP_CFG.SW_JTAG_CFG[2:0] bits can change the above remapping configuration. See the Table below.

Table 7-3 Debug port image

SW_JTAG_CFG[2:0]	Possible debug ports for	SWJ I/O pin allocation				
		PA13/ JTMS/ SWDIO	PA14/ JTCK/ SWCLK	PA15/ JTDI	PB3/ JTDO	PB4/ NJTRST
000	Complete SWJ(JTAG-DP+SW-DP) (reset state)	I/O is not available	I/O is not available	I/O is not available	I/O is not available	I/O is not available
001	Complete SWJ(JTAG-DP+SW-DP) But there is no NJTRST.	I/O is not available	I/O is not available	I/O is not available	I/O is not available	I/O available
010	Turn off JTAG-DP and enable SW-DP.	I/O is not available	I/O is not available	I/O available	I/O available	I/O available
100	Turn off JTAG-DP and SW-DP.	I/O available	I/O available	I/O available	I/O available	I/O available
other	Forbidden					

7.2.5.5.1 SWJ_CFG configuration items

When the write buffer of APB bridge is full, one more APB cycle is needed when writing AFIO_RMP_CFG register. This is because the release of SWD_JTAG pin takes two APB cycles to ensure that the input signals of NJTRST and JTCK are clean.

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The first cycle: the signal input to the kernel by SWD_JTAG with 1/0 input is connected to 0 or 1(NJTRST /TDI/TMS is connected to 1,JTCK is connected to 0);

Second cycle: IOM controls the control signals of SWD_JTAG pin (such as direction, pull-down, schmidt input, etc.).

7.2.5.5.2 Pull-down configuration

Since the pins of JTAG are directly connected to the internal debug register (JTCK/SWCLK is directly connected to the clock terminal), it is necessary to ensure that the input pins of JTAG cannot be floating. In order to avoid any uncontrollable I/O level, JTAG's input pin is fixed with internal pull-down and pull-up:

- NJTRST: internal pull-up
- JTDI: Internal pull-up
- JTMS/SWDIO: Internal pull-up
- JTCK/SWCLK: Internal pull-down

7.2.5.6 ADC external trigger alternate function remapping

The external trigger source of injection conversion and regular conversion of ADC supports remapping. See alternate remapping and debug I/O configuration register (AFIO_RMP_CFG).

Table 7-4 ADC1 external trigger injection conversion alternate function remapping

Alternate function	ADC1_ETRI = 0	ADC1_ETRI = 1
ADC1 external trigger injection conversion	ADC1 external trigger injection conversion is connected to EXTI15.	ADC1 external trigger injection conversion is connected to TIM8_CH4

Table 7-5 ADC1 external trigger regular conversion alternate function remapping

Alternate function	ADC1_ETRR = 0	ADC1_ETRR = 1
ADC1 external trigger rule conversion	ADC1 external trigger regular conversion is connected to EXTI11.	ADC1 external trigger regular conversion is connected to TIM8_TRGO

Table 7-6 ADC2 external trigger injection conversion alternate function remapping

Alternate function	ADC2_ETRI = 0	ADC2_ETRI = 1
ADC2 external trigger injection conversion	ADC2 external trigger injection conversion is connected to EXTI15.	ADC2 external trigger injection conversion is connected to TIM8_CH4

Table 7-7 ADC2 external trigger regular conversion alternate function remapping

Alternate function	ADC2_ETRR = 0	ADC2_ETRR = 1
ADC2 external trigger rule conversion	ADC2 external trigger regular conversion is connected to EXTI11.	ADC2 external trigger regular conversion is connected to TIM8_TRGO

Table 7-8 ADC3 external trigger injection conversion alternate function remapping

Alternate function	ADC3_ETRI = 0	ADC3_ETRI = 1
ADC3 external trigger injection conversion	ADC3 external trigger injection conversion is connected to EXTI14.	ADC3 external trigger injection conversion is connected to TIM5_CH4

Table 7-9 ADC3 external trigger regular conversion alternate function remapping

Alternate function	ADC3_ETRR = 0	ADC3_ETRR = 1

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ADC3 external trigger rule conversion	ADC3 external trigger regular conversion is connected to EXTI10.	ADC3 external trigger regular conversion is connected to TIM5_CH3

Table 7-10 ADC4 external trigger injection conversion alternate function remapping

Alternate function	ADC4_ETRI = 0	ADC4_ETRI = 1
ADC4 external trigger injection conversion	ADC4 external trigger injection conversion is connected to EXTI14.	ADC4 external trigger injection conversion is connected to TIM5_CH4

Table 7-11 ADC4 external trigger regular conversion alternate function remapping

Alternate function	ADC4_ETRR = 0	ADC4_ETRR = 1
ADC4 external trigger rule conversion	ADC4 external trigger regular conversion is connected to EXTI10.	ADC4 external trigger regular conversion is connected to TIM5_CH3

7.2.5.7 TIMx alternate function remapping

Table 7-12 TIM5 alternate function remapping

Alternate function	TIM5CH4_RMP = 0	TIM5CH4_RMP = 1
TIM5_CH4	TIM5_CH4 is connected to PA3	The LSI internal oscillator is connected to TIM5_CH4 to calibrate the LSI

Table 7-13 TIM4 alternate function remapping

Alternate function	TIM4_RMP = 0	TIM4_RMP = 1
TIM4_ETR	PE0	
TIM4_CH1	PB6	PD12
TIM4_CH2	PB7	PD13
TIM4_CH3	PB8	PD14
TIM4_CH4	PB9	PD15

Table 7-14 TIM3 alternate function remapping

Alternate function	TIM3_RMP[1:0] = 00 (No remapping)	TIM3_RMP[1:0] = 10 (partial remapping)	TIM3_RMP[1:0] = 11 (Full remapping)
TIM3_ETR	PD2		
TIM3_CH1	PA6	PB4	PC6
TIM3_CH2	PA7	PB5	PC7
TIM3_CH3	PB0		PC8
TIM3_CH4	PB1		PC9

Table 7-15 TIM2 alternate function remapping

Alternate function	TIM2_RMP[1:0] = 00 (No remapping)	TIM2_RMP[1:0] = 01 (Partial remapping)	TIM2_RMP[1:0] = 10 (Partial remapping)	TIM2_RMP[1:0] = 11 (Full remapping)
TIM2_CH1_ETR	PA0	PA15	PA0	PA15
TIM2_CH2	PA1	PB3	PA1	PB3
TIM2_CH3	PA2		PB10	
TIM2_CH4	PA3		PB11	

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Table 7-16 TIM1 alternate function remapping

Alternate function	TIM1_RMP[1:0] = 00 (No remapping)	TIM1_RMP[1:0] = 01 (Partial remapping)	TIM1_RMP[1:0] = 10 (Partial remapping)	TIM1_RMP[1:0] = 11 (Full remapping)
TIM1_ETR	PA12		PA12	PE7
TIM1_CH1	PA8		PA8	PE9
TIM1_CH2	PA9		PA9	PE11
TIM1_CH3	PA10		PA10	PE13
TIM1_CH4	PA11		PA11	PE14
TEAM1_BKIN	PB12	PA6	PB5	PE15
TIM1_CH1N	PB13	PA7	PB13	PE8
TIM1_CH2N	PB14	PB0	PB14	PE10
TIM1_CH3N	PB15	PB1	PB15	PE12

Table 7-17 TIM8 alternate function remapping

Alternate function	TIM8_RMP[1:0] = 00 (No remapping)	TIM8_RMP[1:0] = 01 (Partial remapping)	TIM8_RMP[1:0] = 11 (Full remapping)
TIM8_ETR	PA0	PB4	PB4
TIM8_CH1	PC6	PC6	PD14
TIM8_CH2	PC7	PC7	PD15
TIM8_CH3	PC8	PC8	PC8
TIM8_CH4	PC9	PC9	PC9
TEAM8_BKIN	PA6	PB3	PB3
TIM8_CH1N	PA7	PA15	PA15
TIM8_CH2N	PB0	PC12	PC12
TIM8_CH3N	PB1	PD2	PD2

7.2.5.8 CAN alternate function remapping

7.2.5.8.1 CAN1 alternate function remapping

The CAN1 signal can be mapped to port A, port B or port D, as shown in the following Table. For port D, there is no remapping function on 48-pin and 64-pin packages (there are no PD0 and PD1 on these packages).

Table 7-18 CAN1 alternate function remapping

Alternate function	CAN1_RMP[1:0] = 00	CAN1_RMP[1:0] = 01	CAN1_RMP[1:0] = 10	CAN1_RMP[1:0] = 11
CAN1_RX	PA11	PD8	PB8	PD0
CAN1_TX	PA12	PD9	PB9	PD1

7.2.5.8.2 CAN2 alternate function remapping

CAN2 signal can be mapped to port B or port D, as shown in the following Table.

Table 7-19 CAN2 alternate function remapping

Alternate function	CAN2_RMP[1:0] = 00	CAN2_RMP[1:0] = 01	CAN2_RMP[1:0] = 11
CAN2_RX	PB12	PB5	PD10
CAN2_TX	PB13	PB6	PD11

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7.2.5.9 DVP alternate function remapping

The mapping relationship of DVP signals is shown in the following Table.

Table 7-20 DVP alternate function remapping

Alternate function	DVP_RMP[1:0] = 00	DVP_RMP[1:0] = 01	DVP_RMP[1:0] = 11
DVP_HSYNC	PA1	PE2	PE2
DVP_VSYNC	PA2	PE3	PE3
DVP_PCLK	PA3	PE4	PE4
DVP_D0	PA4	PE5	PE5
DVP_D1	PA5	PE6	PE6
DVP_D2	PA6	PC0	PC0
DVP_D3	PA7	PB2	PB2
DVP_D4	PC4	PF12	PB10
DVP_D5	PC5	PF13	PB11
DVP_D6	PB0	PF14	PF14
DVP_D7	PB1	PF15	PF15

7.2.5.10 USARTx alternate function remapping

7.2.5.10.1 USART1 pin remapping

USART1/2/3 interfaces have remapping function. See the alternate remapping configuration register (AFIO_RMP_CFG).

Table 7-21 USART1 alternate function remapping

Alternate function	USART1_RMP = 0	USART1_RMP = 1
USART1_CTS	PA11	
USART1_RTS	PA12	
USART1_TX	PA9	PB6
USART1_RX	PA10	PB7
USART1_CK	PA8	

7.2.5.10.2 USART2 pin remapping

Table 7-22 USART2 alternate function remapping

Alternate function	USART2_RMP[1:0] = 00	USART2_RMP[1:0] = 01	USART2_RMP[1:0] = 10	USART2_RMP [1:0] =11
USART2_CTS	PA0	PD3	PC6	PA15
USART2_RTS	PA1	PD4	PC7	PB3
USART2_TX	PA2	PD5	PC8	PB4
USART2_RX	PA3	PD6	PC9	PB5
USART2_CK	PA4	PD7	/	PA4

7.2.5.10.3 USART3 pin remapping

Table 7-23 USART3 alternate function remapping

Alternate function	USART3_RMP[1:0] = 00	USART3_RMP[1:0] = 01	USART3_RMP[1:0] = 11
USART3_TX	PB10	PC10	PD8

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Alternate function	USART3_RMP[1:0] = 00	USART3_RMP[1:0] = 01	USART3_RMP[1:0] = 11
USART3_RX	PB11	PC11	PD9
USART3_CK	PB12	PC12	PD10
USART3_CTS	PB13		PD11
USART3_RTS	PB14		PD12

7.2.5.11 UARTx alternate function remapping

UART4/5/6/7 interfaces have remapping function. See the alternate remapping configuration register (AFIO_RMP_CFG3).

7.2.5.11.1 UART4 pin remapping

Table 7-24 UART4 alternate function remapping

Alternate function	UART4_RMP[1:0] = 00	UART4_RMP[1:0] = 01	UART4_RMP[1:0] = 10	UART4_RMP [1:0] =11
UART4_TX	PC10	PB2	PA13	PD0
UART4_RX	PC11	PE7	PA14	PD1

7.2.5.11.2 UART5 pin remapping

Table 7-25 UART5 alternate function remapping

Alternate function	UART5_RMP[1:0] = 00	UART5_RMP[1:0] = 01	UART5_RMP[1:0] = 10	UART5_RMP [1:0] =11
UART5_TX	PC12	PB13	PE8	PB8
UART5_RX	PD2	PB14	PE9	PB9

7.2.5.11.3 UART6 pin remapping

Table 7-26 UART6 alternate function remapping

Alternate function	UART6_RMP[1:0] = 00	UART6_RMP[1:0] = 10	UART6_RMP[1:0] = 11
UART6_TX	PE2	PC0	PB0
UART6_RX	PE3	PC1	PB1

7.2.5.11.4 UART7 pin remapping

Table 7-27 UART7 alternate function remapping

Alternate function	UART7_RMP[1:0] = 00	UART7_RMP[1:0] = 01	UART7_RMP[1:0] = 11
UART7_TX	PC4	PC2	PG0
UART7_RX	PC5	PC3	PG1

7.2.5.12 I2C alternate function remapping

7.2.5.12.1 I2C1 pin remapping

See alternate remapping configuration register (AFIO_RMP_CFG).

Table 7-28 I2C1 pin remapping

Alternate function	I2C1_RMP= 0	I2C1_RMP= 1
I2C1_SCL	PB6	PB8
I2C1_SDA	PB7	PB9
I2C1_SMBA	PB5	

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7.2.5.12.2 I2C2 pin remapping

See alternate remapping configuration register (AFIO_RMP_CFG3).

Table 7-29 I2C2 pin remapping

Alternate function	I2C2_RMP[1:0] = 00	I2C2_RMP[1:0] = 01	I2C2_RMP[1:0] = 11
I2C2_SCL	PB10	PG2	PA4
I2C2_SDA	PB11	PG3	PA5
I2C2_SMBA	PB12		

7.2.5.12.3 I2C3 pin remapping

See alternate remapping configuration register (AFIO_RMP_CFG3).

Table 7-30 I2C3 pin remapping

Alternate function	I2C3_RMP[1:0] = 00	I2C3_RMP[1:0] = 10	I2C3_RMP[1:0] = 11
I2C3_SCL	PC0	PF4	PC4
I2C3_SDA	PC1	PF5	PC5

7.2.5.12.4 I2C4 pin remapping

See alternate remapping configuration register (AFIO_RMP_CFG3).

Table 7-31 I2C4 pin remapping

Alternate function	I2C4_RMP[1:0] = 00	I2C4_RMP[1:0] = 01	I2C4_RMP[1:0] = 11
I2C4_SCL	PC6	PD14	PA9
I2C4_SDA	PC7	PD15	PA10

7.2.5.13 SPI/I2S alternate function remapping

7.2.5.13.1 SPI1 pin remapping

See alternate remapping configuration register (AFIO_RMP_CFG).

Table 7-32 SPI1 pin remapping

Alternate function	SPI1_RMP[1:0] = 00	SPI1_RMP[1:0] = 01	SPI1_RMP[1:0] = 10	SPI1_RMP [1:0] =11
SPI1_NSS	PA4	PA15	PB2	PB2
SPI1_SCK	PA5	PB3	PA5	PE7
SPI1_MISO	PA6	PB4	PA6	PE8
SPI1_MOSI	PA7	PB5	PA7	PE9

7.2.5.13.2 SPI2/I2S2 pin remapping

See alternate remapping configuration register (AFIO_RMP_CFG3).

Table 7-33 SPI2/I2S2 pin remapping

Alternate function	SPI2_RMP[1:0] = 00	SPI2_RMP[1:0] = 01	SPI2_RMP[1:0] = 11
SPI2_NSS/I2S2_WS	PB12	PC6	PE10
SPI2_SCK/I2S2_CK	PB13	PC7	PE11
SPI2_MISO	PB14	PC8	PE12
SPI2_MOSI/I2S2_SD	PB15	PC9	PE13

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7.2.5.13.3 SPI3/I2S3 pin remapping

See alternate remapping configuration register (AFIO_RMP_CFG3).

Table 7-34 SPI3/I2S3 pin remapping

Alternate function	SPI3_RMP[1:0] = 00	SPI3_RMP[1:0] = 01	SPI3_RMP[1:0] = 10	SPI3_RMP[1:0] = 11
SPI3_NSS/I2S3_WS	PA15	PD2	PD8	PC2
SPI3_SCK/I2S3_CK	PB3	PC10	PD9	PC3
SPI3_MISO	PB4	PC11	PD11	PA0
SPI3_MOSI/I2S3_SD	PB5	PC12	PD12	PA1

7.2.5.14 SDIO alternate function remapping

See alternate remapping configuration register (AFIO_RMP_CFG3).

Table 7-35 SDIO pin remapping

Alternate function	SDIO_RMP = 0	SDIO_RMP = 1
SDIO_0	PC8	PE8
SDIO_1	PC9	PE9
SDIO_2	PC10	PE10
SDIO_3	PC11	PE11
SDIO_4	PB8	
SDIO_5	PB9	
SDIO_6	PC6	
SDIO_7	PC7	
SDIO_CK	PC12	PE12
SDIO_CMD	PD2	PE13

7.2.5.15 QSPI alternate function remapping

QSPI only supports master mode, and does not support multi-master mode. In single-line mode, QSPI_IO1 acts as MISO, supports push-pull alternate output, input floating or input pull-up. See alternate remapping configuration register (AFIO_RMP_CFG3).

Table 7-36 QSPI pin remapping

Alternate function	QSPI_RMP[1:0] = 00	QSPI_RMP[1:0] = 01	QSPI_RMP[1:0] = 11
QSPI_NSS	PA4	PF0	PC10
QSPI_CLK	PA5	PF1	PC11
QSPI_IO0	PA6	PF2	PC12
QSPI_IO1	PA7	PF3	PD0
QSPI_ IO2	PC4	PF4	PD1
QSPI_ IO3	PC5	PF5	PD2

7.2.5.16 ETH alternate function remapping

See alternate remapping configuration register (AFIO_RMP_CFG).

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Table 7-37 ETH pin remapping

Alternate function	ETH_RMP[1:0] = 00	ETH_RMP[1:0] = 01	ETH_RMP[1:0] = 10	ETH_RMP[1:0] = 11
ETH_MII_MDC ETH_RMII_MDC	PC1			
ETH_MII_TX2	PC2			
ETH_MII_TX_CLK	PC3			
ETH_MII_CRS_WKUP	PA0			
ETH_MII_RX_CLK ETH_MII_REF_CLK	PA1			
ETH_MII_MDIO ETH_RMII_MDIO	PA2			
ETH_MII_COL	PA3			
ETH_MII_RX_DV ETH_RMII_CRS_DV	PA7	PD8	PA7	PD8
ETH_MII_RXD0 ETH_RMII_RXD0	PC4	PD9	PC4	PD9
ETH_MII_RXD1 ETH_RMII_RXD1	PC5	PD10	PC5	PD10
ETH_MII_RXD2 ETH_RMII_RXD2	PB0	PD11	PB0	PB0
ETH_MII_RXD3 ETH_RMII_RXD3	PB1	PD12	PB1	PB1
ETH MII RX ER	PB10			
Ethernet Ethernet	PB11			
ETH_MII_TXD0 ETH_RMII_TXD0	PB12			
ETH_MII_TXD1 ETH_RMII_TXD1	PB13			
ETH_MII_PPS_OUT ETH_RMII_PPS_OUT	PB5		PB6	
ETH_MII_TXD3	PB8		PB7	

7.2.6 I/O Configuration of Peripherals

Table 7-38 ADC/DAC

ADC/DAC pin	GPIO configuration
ADC	Analog mode
DAC	Analog mode

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Table 7-39 TIM1/TIM8

TIM1/TIM8 pin	Configuration	PAD configuration mode
TIM1/8_CHx	Input capture channel x	Input floating
	Output channel x	Push-pull alternate output
TIM1/8_CHxN	Complementary output channel x	Push-pull alternate output
TIM1/8_BKIN	Brake input	Input floating
TIM1/8_ETR	External trigger clock input	Input floating

Table 7-40 TIM2/3/4/5

TIM2/3/4/5 pin	Configuration	PAD configuration mode
TIM2/3/4/5_CHx	Input capture channel x	Input floating
	Output channel x	Push-pull alternate output
TIM2/3/4/5_ETR	External trigger clock input	Input floating

Table 7-41 bxCAN

bxCAN pin	GPIO configuration
CAN_TX	Push-pull alternate output
CAN_RX	Input floating or input pull-up

Table 7-42 DVP

DVP pin	GPIO configuration
DVP_HSYNC	Input floating
DVP_VSYNC	Input floating
DVP_PCLK	Input floating
DVP_D0	Input floating
DVP_D1	Input floating
DVP_D2	Input floating
DVP_D3	Input floating
DVP_D4	Input floating
DVP_D5	Input floating
DVP_D6	Input floating
DVP_D7	Input floating

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Table 7-43 USART

USART pin	Configuration	GPIO configuration
USARTx_TX	full duplex transmissions	Push-pull alternate output
	Half duplex synchronous mode	Push-pull alternate output
USARTx_RX	full duplex transmissions	Input floating or input pull-up
	Half duplex synchronous mode	Unused, can be used as general I/O.
USARTx_CK	Synchronous mode	Push-pull alternate output
USARTx_RTS	Hardware flow control	Push-pull alternate output
USARTx_CTS	Hardware flow control	Input floating or input pull-up

Table 7-44 I2C

I2C pin	Description	GPIO configuration
I2Cx_SCL	I2C clock	Open-drain alternate output
I2Cx_SDA	I2C data	Open-drain alternate output
I2Cx_SMBA	SMBA data	Push-pull alternate output

Table 7-45 SPI

SPI pin	Description	GPIO configuration
SPIx_SCK	Master mode	Push-pull alternate output
	Slave mode	Input floating
SPIx_MOSI	Full duplex mode/ Master mode	Push-pull alternate output
	Full duplex mode/slave mode	Floating input or input pull-up or push-pull alternate output
	Simple bidirectional data line/ Master mode	Push-pull alternate output
	Simple bidirectional data line/slave mode	Unused, can be used as general I/O.
SPIx_MISO	Full duplex mode/ Master mode	Floating input or input pull-up or push-pull alternate output
	Full duplex mode/slave mode	Push-pull alternate output
	Simple bidirectional data line/ Master mode	Unused, can be used as general I/O.
	Simple bidirectional data line/slave mode	Push-pull alternate output

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SPI pin	Description	GPIO configuration
SPIx_NSS	Hardware master/slave mode	Input floating or pull-up input or input pull-down
	Hardware mode /NSS output enable	Push-pull alternate output (NSS can choose idle high resistance or idle is 1 when it is the master)
	Software mode	Unused, can be used as general I/O.

Table 7-46 I2S

I2S pin	Configuration	GPIO configuration
I2Sx_WS	Master mode	Push-pull alternate output
	Slave mode	Floating input
I2Sx_CK	Master mode	Push-pull alternate output
	Slave mode	Input floating
I2Sx_SD	transmitter	Push-pull alternate output
	receiver	Input floating or pull-up input or input pull-down
I2Sx_MCK	Master mode	Push-pull alternate output
	Slave mode	Unused, can be used as general I/O.

Table 7-47 SDIO

SDIO pin	GPIO configuration
SDIO_CK	Push-pull alternate output
SDIO_CMD	Push-pull alternate output
SDIO[D7:D0]	Push-pull alternate output

Table 7-48 QSPI

QSPI pin	GPIO configuration	remarks
QSPI_IO3	Push-pull alternate output	QSPI only supports master mode, and does not support multi-master mode.
QSPI_IO2	Push-pull alternate output	
QSPI_IO1	Push-pull alternate output	
QSPI_IO0	Push-pull alternate output	
QSPI_CLK	Push-pull alternate output	
QSPI_NSS	Push-pull alternate output	

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Table 7-49 ETH

MAC signal	Pin configuration
ETH_MDC	Push-pull alternate output, high speed (50MHz)
ETH_MII_TXD2	Push-pull alternate output
ETH_MII_TX_CLK	Input floating (reset state)
ETH_MII_CRS	Input floating (reset state)
ETH_MII_RX_CLK ETH_RMII_REF_CLK	Input floating (reset state)
ETH_MDIO	Push-pull alternate output, high speed (50MHz)
ETH_MII_COL	Input floating (reset state)
ETH_MII_RX_DV ETH_RMII_CRS_DV	Input floating (reset state)
ETH_MII_RXD0 ETH_RMII_RXD0	Input floating (reset state)
ETH_MII_RXD1 ETH_RMII_RXD1	Input floating (reset state)
ETH_MII_RXD2	Input floating (reset state)
ETH_MII_RXD3	Input floating (reset state)
ETH MII RX ER	Input floating (reset state)
Ethernet Ethernet	Push-pull alternate output, high speed (50MHz)
ETH_MII_TXD0 ETH_RMII_TXD0	Push-pull alternate output, high speed (50MHz)
ETH_MII_TXD1 ETH_RMII_TXD1	Push-pull alternate output, high speed (50MHz)
ETH_PPS_OUT	Push-pull alternate output, high speed (50MHz)
ETH_MII_TXD3	Push-pull alternate output, high speed (50MHz)
ETH_RMII_CRS_DV	Input floating (reset state)
ETH_MII_RXD0 ETH_RMII_RXD0	Input floating (reset state)
ETH_MII_RXD1 ETH_RMII_RXD1	Input floating (reset state)
ETH_MII_RXD2	Input floating (reset state)
ETH_MII_RXD3	Input floating (reset state)

Table 7-50 USB

USB pin	GPIO configuration
USB_DM USB_DP	Once the USB module is enabled, these pins are automatically

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USB pin	GPIO configuration
	connected to the internal USB transceiver.

Table 7-51 Other

pin	Alternate function	GPIO configuration
TAMPER-RTC	RTC output	When configuring BKP_CR and BKP_RTCCR registers, it is forced by hardware.
	Intrusion event input	
MCO	Clock output	Push-pull alternate output
EXTI input line	External interrupt input	Input floating or pull-up input or input pull-down

7.2.7 GPIO Locking Mechanism

The locking mechanism is used to freeze the I/O configuration to prevent accidental changes. When a LOCK program is executed on a port bit, the port configuration cannot be changed until the next reset. Refer to the port configuration lock register GPIOx_PLOCK_CFG.

- PLOCKK_CFG is GPIOx_PLOCK_CFG[16], which will become 1 only after the PLOCKK_CFG is operated according to the correct sequence w1->w0->w1->r0 (where r0 is required); After that, it will become 0 only after system reset.
- PLOCK_CFGy is GPIOx_PLOCK_CFG [15:0], which can only be modified when PLOCKK_ CFG = 0, that is, it is unlocked.
- The sequence w1->w0->w1->r0 is valid only when the PLOCKK_CFG is written at the same time as the non-zero GPIOx_PLOCKK_CFG [15: 0]. GPIOx_PLOCK_CFG [15:0] must not be changed during sequence writing;
- GPIOx_PH_CFG/GPIOx_PL_CFG bits can be modified as long as PLOCK _ CFG = 0, which is not affected by the configuration of GPIOx_PLOCK_CFG [15:0].
- PLOCKK_CFG=1, GPIOx_PH_CFG/GPIOx_PL_CFG is controlled by GPIOx_PLOCK_CFG [15:0], corresponding to PLOCK_CFGy（y = 0…15）=1 which is a locked configuration and cannot be modified, and PLOCK_CFGy=0, can be modified.
- If the sequence operation is wrong, w1->w0->w1->r0 must be performed again to initiate the locking operation again.

7.3 GPIO Registers

These peripheral registers must be operated as 32-bit words.

7.3.1 GPIO Register Overview

GPIOA base address: 0x40010800

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GPIOB base address: 0x40010C00

GPIOC base address: 0x40011000

GPIOD base address: 0x40011400

GPIOE base address: 0x40011800

GPIOF base address: 0x40011C00

GPIOG base address: 0x40012000

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Table 7-52 GPIO registers overview

Offset	Register		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
000h	GPIOx_PL_CFG		PCFG7[1:0]		PMODE7[1:0]		PCFG6[1:0]		PMODE6[1:0]		PCFG5[1:0]		PMODE5[1:0]		PCFG4[1:0]		PMODE4[1:0]		PCFG3[1:0]		PMODE3[1:0]		PCFG2[1:0]		PMODE2[1:0]		PCFG1[1:0]		PMODE1[1:0]		PCFG0[1:0]		PMODE0[1:0]	
	Reset Value	x=B	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
		x=A,C,D,E,F,G	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
004h	GPIOx_PH_CFG		PCFG15[1:0]		PMODE15[1:0]		PCFG14[1:0]		PMODE14[1:0]		PCFG13[1:0]		PMODE13[1:0]		PCFG12[1:0]		PMODE12[1:0]		PCFG11[1:0]		PMODE11[1:0]		PCFG10[1:0]		PMODE10[1:0]		PCFG9[1:0]		PMODE9[1:0]		PCFG8[1:0]		PMODE8[1:0]	
	Reset Value	x=A	1	0	0	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		x=B,C,D,E,F,G	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
008h	GPIOx_PID		Reserved																PID15	PID14	PID13	PID12	PID11	PID10	PID9	PID8	PID7	PID6	PID5	PID4	PID3	PID2	PID1	PID0
	Reset Value																		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
00Ch	GPIOx_POD		Reserved																POD15	POD14	POD13	POD12	POD11	POD10	POD9	POD8	POD7	POD6	POD5	POD4	POD3	POD2	POD1	POD0
	Reset Value	x=A																	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
		x=B																	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
		x=C,D,E,F,G																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
010h	GPIOx_PBSC		PBC15	PBC14	PBC13	PBC12	PBC11	PBC10	PBC9	PBC8	PBC7	PBC6	PBC5	PBC4	PBC3	PBC2	PBC1	PBC0	PBS15	PBS14	PBS13	PBS12	PBS11	PBS10	PBS9	PBS8	PBS7	PBS6	PBS5	PBS4	PBS3	PBS2	PBS1	PBS0
	Reset Value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
014h	GPIOx_PBC		Reserved																PBC15	PBC14	PBC13	PBC12	PBC11	PBC10	PBC9	PBC8	PBC7	PBC6	PBC5	PBC4	PBC3	PBC2	PBC1	PBC0
	Reset Value																		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
018h	GPIOx_PLOCK_CFG		Reserved															PLOCKK_CFG	PLOCK_CFG15	PLOCK_CFG14	PLOCK_CFG13	PLOCK_CFG12	PLOCK_CFG11	PLOCK_CFG10	PLOCK_CFG9	PLOCK_CFG8	PLOCK_CFG7	PLOCK_CFG6	PLOCK_CFG5	PLOCK_CFG4	PLOCK_CFG3	PLOCK_CFG2	PLOCK_CFG1	PLOCK_CFG0
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
01Ch	Reserved																																	
020h	GPIOx_DS_CFG		Reserved																DS_CFG15	DS_CFG 14	DS_CFG13	DS_CFG12	DS_CFG11	DS_CFG10	DS_CFG9	DS_CFG8	DS_CFG7	DS_CFG6	DS_CFG5	DS_CFG4	DS_CFG3	DS_CFG2	DS_CFG1	DS_CFG0
	Reset Value	x=F																	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1
		x=G																	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1
		x=A,B,C,D,E																	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
024h	GPIOx_SR_CFG		Reserved																SR_CFG15	SR_CFG14	SR_CFG13	SR_CFG12	SR_CFG11	SR_CFG10	SR_CFG9	SR_CFG8	SR_CFG7	SR_CFG6	SR_CFG5	SR_CFG4	SR_CFG3	SR_CFG2	SR_CFG1	SR_CFG0
	Reset Value	x=F																	0	0	0	0	0	0	1	0	0	0	1	1	1	1	1	1
		x=G																	0	0	0	0	0	0	1	0	0	0	1	1	1	1	1	1
		x=A,B,C,D,E																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

7.3.2 GPIO Port Low Configuration Register (GPIOx_PL_CFG)

Address offset: 0x00

Reset value: 0x0000 0000 (x=A, C, D, E, F, G); 0x0008 0800 (x=B)

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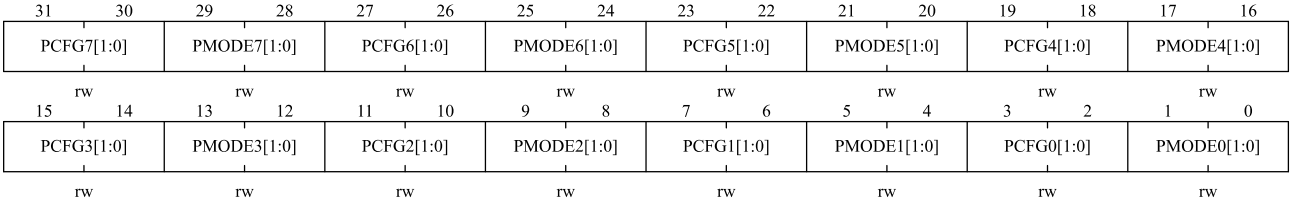
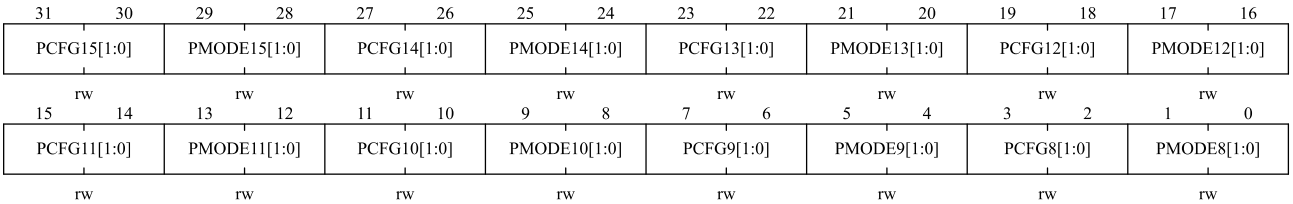


Bit field	Name	Description
31:30 27:26 23:22 19:18 15:14 11:10 7:6 3:2	PCFGy[1:0]	Port x configuration bit (y = 0…7) PMODE[1:0]=00 input mode: 00: analog function mode (state after reset) 01: Input floating mode 10: input pull-up/ input pull-down mode (note: when configuring the input pull-up/ input pull-down mode, you need to set/reset the corresponding GPIOx_POD register) 11: reserved When PMODE[1:0]>00 output mode: 00: General push-pull output mode 01: General open-drain output mode 10: Alternate function push-pull output mode 11: Open-drain output mode of alternate function
29:28 25:24 21:20 17:16 13:12 9:8 5:4 1:0	PMODEy[1:0]	Mode bit of port x (y = 0…7) 00: input mode (state after reset) 01: output mode, maximum speed 2MHz 10: output mode, maximum speed 10MHz 11: output mode, maximum speed 50MHz

7.3.3 GPIO Port High Configuration Register (GPIOx_PH_CFG)

Address offset: 0x04

Reset value: 0x8880 0000(x=A); 0x0000 0000(x=B,C,D,E,F,G)



Bit field	Name	Description
31:30 27:26 23:22 19:18	PCFGy[1:0]	Port x configuration bit (y = 8…15) PMODE[1:0]=00 In input mode: 00: analog function mode (state after reset) 01: Input floating mode

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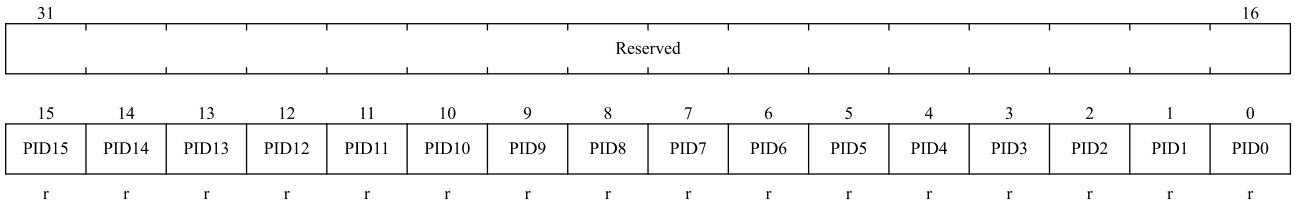
Bit field	Name	Description
15:14 11:10 7:6 3:2		10: input pull-up/ input pull-down mode (note: when configuring the input pull-up/ input pull-down mode, you need to set/reset the corresponding GPIOx_POD register) 11: reserved When MODE[1:0]>00 output mode: 00: General push-pull output mode 01: General open-drain output mode 10: Alternate function push-pull output mode 11: Open-drain output mode of alternate function
29:28 25:24 21:20 17:16 13:12 9:8 5:4 1:0	PMODEy[1:0]	Mode bit of port x (y = 8…15) 00: input mode (state after reset) 01: output mode, maximum speed 2MHz 10: output mode, maximum speed 10MHz 11: output mode, maximum speed 50MHz

7.3.4 GPIO Port Input Data Register (GPIOx_PID)

Address offset: 0x08

Reset value: 0x0000 0000



Bit field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained.
15:0	PIDy	Port input data (y = 0…15) These bits are read-only and can only be read in the form of 16-bit words, and the read value is the state of the corresponding I/O port.

7.3.5 GPIO Port Output Data Register (GPIOx_POD)

Address offset: 0x0C

Reset value: 0x0000 A000(x=A); 0x0000 0010(x=B); 0x0000 0000(x=C,D,E,F,G)

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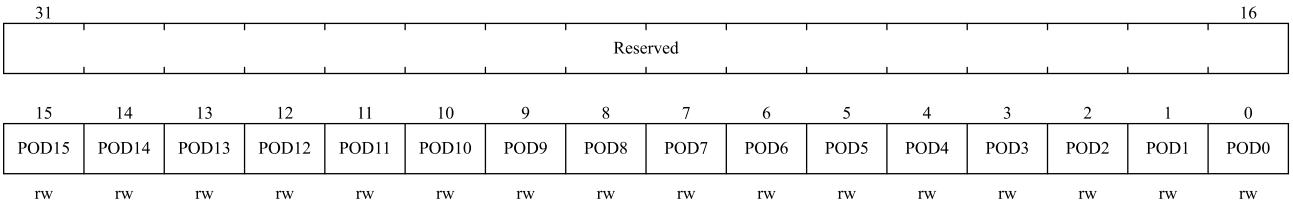
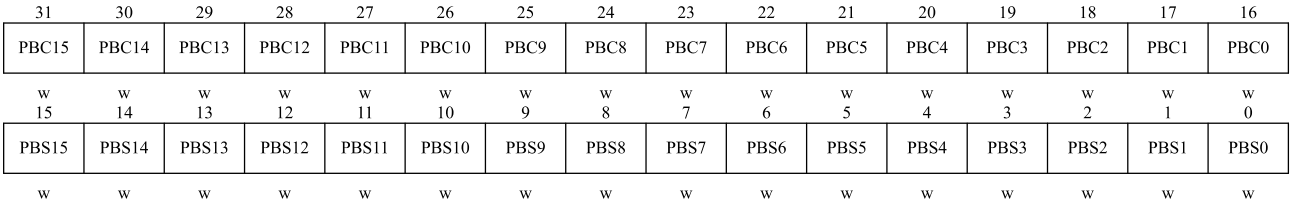


Bit field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained.
15:0	PODy	Port output data (y = 0…15) These bits can only be read or written in the form of 16-bit words. GPIOx_PBSC(x = A…G) can be independently set/cleared for the corresponding POD bit.

7.3.6 GPIO Port Bit Setting/Clearing Register (GPIOx_PBSC)

Address offset: 0x10

Reset value: 0x0000 0000



Bit field	Name	Description
31:16	PBCy	Clear bit y of port GPIOx (y = 0…15) These bits can only be written and operated as words (16 bits). 0: does not affect the corresponding PODy bit 1: Clear the corresponding PODy bit to 0 *Note: if the corresponding bits of PBSy and PBCy are set at the same time, the PBSy bit works.*
15:0	PBSy	Set bit y of port GPIOx (y = 0…15) These bits can only be written and operated as words (16 bits). 0: does not affect the corresponding PODy bit 1: Set the corresponding PODy bit to 1

7.3.7 GPIO Port Bit Clear Register (GPIOx_PBC)

Address offset: 0x14

Reset value: 0x0000 0000

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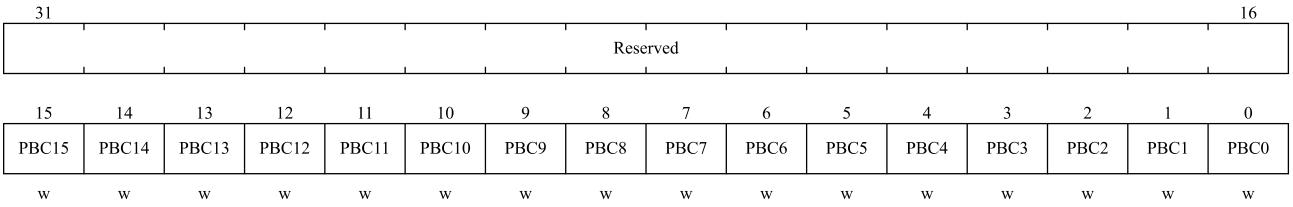
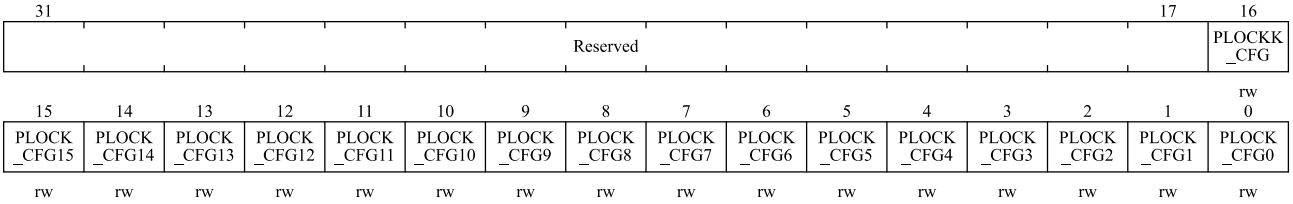


Bit field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained.
15:0	PBCy	Clear bit y of port GPIOx (y = 0...15) These bits can only be written and operated as words (16 bits). 0: does not affect the corresponding PODy bit 1: Clear the corresponding PODy bit to 0

7.3.8 GPIO Port Lock Configuration Register (GPIOx_PLOCK_CFG)

Address offset: 0x18

Reset value: 0x0000 0000



Bit field	Name	Description
31:17	Reserved	Reserved, the reset value must be maintained.
16	PLOCKK_CFG	Lock key. This bit can be read at any time, and it can only be modified by the key lock write sequence. 0: Port configuration lock key is activated 1: The port configuration lock key is activated, and the GPIOx_PLOCK_CFG register is locked before the next system reset. The write sequence of the lock key: Write 1 -> write 0 -> write 1 -> read 0 -> read 1 The last reading can be omitted, but it can be used to confirm that the lock key has been activated. *Note: the value of PLOCK_CFG[15:0] cannot be changed when the writing sequence of lock key is operated. Any error in the operation key writing sequence will not activate the key.*
15:0	PLOCK_CFGy	Configuration lock bit y of port GPIOx (y = 0…15) These bits are readable and writable but can only be written when the PLOCKK_CFG bit is 0. 0: Do not lock the configuration of the port 1: Lock the configuration of the port

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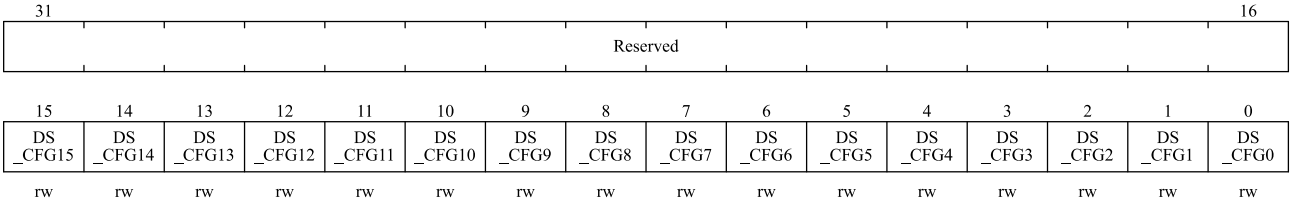
7.3.9 GPIO Driver Capability Configuration Register (GPIOx_DS_CFG)

Address offset: 0x20

Reset value: 0x0000 FFFF（x = A,B,C,D,E）；0x0000 F03F（x=F）；0x0000 023F（x=G）

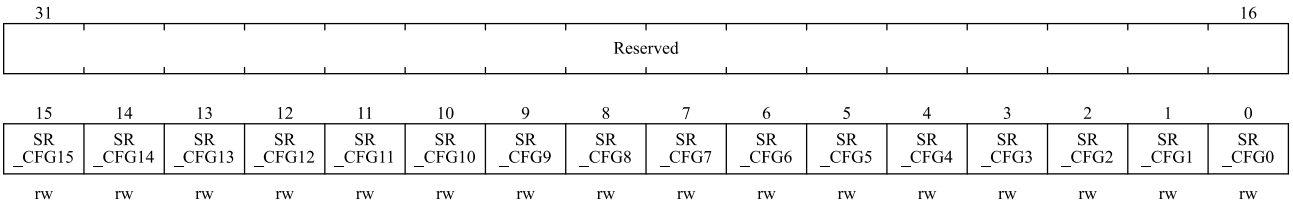


Bit field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained.
15:0	DS_CFGy	The drive capability configuration bit y of port GPIOx (y = 0…15) These bits can only be read or written in the form of 16-bit words. 0: 2mA 1: Controlled by PMODEy of GPIOx_PH_CFG/GPIOx_PL_CFG. PMODE: 00/01, 8mA; PMODEy: 10, 4mA; PMODEy: 11, 12mA.

7.3.10 GPIO Flip Rate Configuration Register (GPIOx_SR_CFG)

Address offset: 0x24

Reset value: 0x0000 FFFF（x= A,B,C,D,E）；0x0000 F03F（x=F）；0x0000 023F（x=G）



Bit field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained.
15:0	SR_CFGy	Port GPIOx flip rate configuration bit y (y = 0…15) These bits can only be read or written in the form of 16-bit words. 0: fast flip 1: Slow flip

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7.4 AFIO Registers

7.4.1 AFIO Register Overview

AFIO base address: 0x40010000

Table 7-53 AFIO register overview

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
000h	AFIO_ECTRL	Reserved																								EOE	PORT_SEL[2:0]			PIN_SEL[3:0]			
	Reset Value																									0	0	0	0	0	0	0	0
004h	AFIO_RMP_CFG	Reserved				SW_JTAG_CFG[2:0]			MII_RMII_SEL	Reserved		ADC2_ETRR	ADC2_ETRI	ADC1_ETRR	ADC1_ETRI	TIM5CH4_RMP	PD01_RMP	CAN1_RMP[1:0]		TIM4_RMP	TIM3_RMP[1:0]		TIM2_RMP[1:0]		TIM1_RMP[1:0]		USART3_RMP[1:0]		USART2_RMP_0	USART1_RMP	I2C1_RMP	SPI1_RMP_0
	Reset Value					0	0	0	0			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
008h	AFIO_EXTI_CFG1	Reserved																EXTI3_CFG[3:0]				EXTI2_CFG[3:0]				EXTI1_CFG[3:0]				EXTI0_CFG[3:0]			
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
00Ch	AFIO_EXTI_CFG2	Reserved																EXTI7_CFG[3:0]				EXTI6_CFG[3:0]				EXTI5_CFG[3:0]				EXTI4_CFG[3:0]			
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
010h	AFIO_EXTI_CFG3	Reserved																EXTI11_CFG[3:0]				EXTI10_CFG[3:0]				EXTI9_CFG[3:0]				EXTI8_CFG[3:0]			
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
014h	AFIO_EXTI_CFG4	Reserved																EXTI15_CFG[3:0]				EXTI14_CFG[3:0]				EXTI13_CFG[3:0]				EXTI12_CFG[3:0]			
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
01Ch	Reserved																																
020h	AFIO_RMP_CFG3	TIM8_RMP[1:0]		Reserved		UART7_RMP[1:0]		UART6_RMP[1:0]		UART5_RMP[1:0]		UART4_RMP[1:0]		USART2_RMP_1	SPI1_RMP_1	ETH_RMP[1:0]		SPI3_RMP[1:0]		SPI2_RMP[1:0]		I2C4_RMP[1:0]		I2C3_RMP[1:0]		I2C2_RMP[1:0]		QSPI_RMP[1:0]		Reserved		CAN2_RMP[1:0]		SDIO_RMP
	Reset Value	0	0			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0			0	0	0
024h	AFIO_RMP_CFG4	Reserved						QSPI_MISO	SPI3_NSS	SPI2_NSS	SPI1_NSS	DVP_RMP[1:0]		QSPI_XIP_EN	Reserved	ADC4_ETRR	ADC4_ETRI	ADC3_ETRR	ADC3_ETRI	Reserved	COMP7_RMP	COMP6_RMP[1:0]		COMP5_RMP[1:0]		COMP4_RMP[1:0]		COMP3_RMP[1:0]		COMP2_RMP[1:0]		COMP1_RMP[1:0]	
	Reset Value							0	0	0	0	0	0	0		0	0	0	0		0	0	0	0	0	0	0	0	0	0	0	0	0	0
028h	AFIO_RMP_CFG5	Reserved								EMC_GB4_DETECT_EN	EMC_GB3_DETECT_EN	EMC_GB2_DETECT_EN	EMC_GB1_DETECT_EN	EMC_GBN4_DETECT_EN	EMC_GBN3_DETECT_EN	EMC_GBN2_DETECT_EN	EMC_GBN1_DETECT_EN	EMC_CLAMP4_DETECT_EN	EMC_CLAMP3_DETECT_EN	EMC_CLAMP2_DETECT_EN	EMC_CLAMP1_DETECT_EN	EMC_GB4_RST_EN	EMC_GB3_RST_EN	EMC_GB2_RST_EN	EMC_GB1_RST_EN	EMC_GBN4_RST_EN	EMC_GBN3_RST_EN	EMC_GBN2_RST_EN	EMC_GBN1_RST_EN	EMC_CLAMP4_RST_EN	EMC_CLAMP3_RST_EN	EMC_CLAMP2_RST_EN	EMC_CLAMP1_RST_EN
	Reset Value									0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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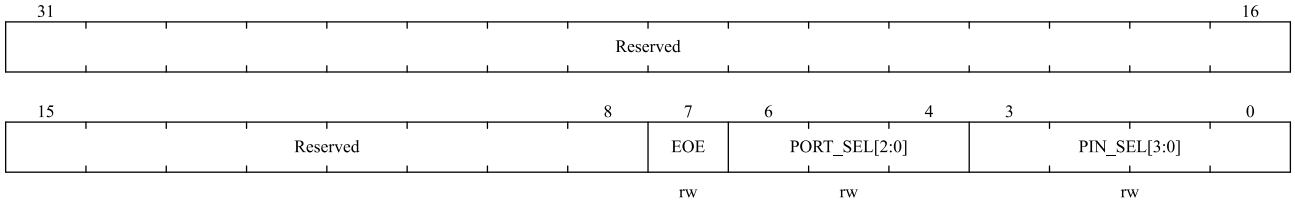
7.4.2 AFIO Event Control Register (AFIO_ECTRL)

Address offset: 0x00

Reset value: 0x0000 0000

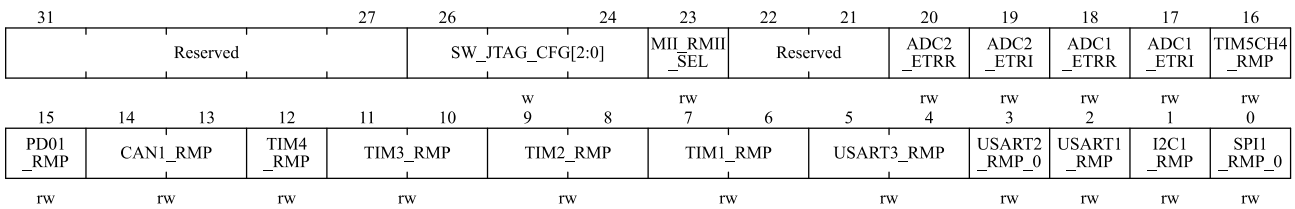


Bit field	Name	Description
31:8	Reserved	Reserved, the reset value must be maintained.
7	EOE	Event output enable bit. When this bit is set, the Cortex event output signal will be connected to the I/O port selected by PORT_SEL[2:0] and PIN_SEL[3:0]. 0: Output disable 1: Output enable
6:4	PORT_SEL[2:0]	Port selection bit Select the port used to output the event output signal of cortex: 000: select port A 001: select port B 010: select port C 011: select port D 100: select port E
3:0	PIN_SEL[3:0]	Pin select bit Select the pin used to output the Cortex event output signal, (x=A...E) corresponding to the I/O selected by PORT_SEL[2:0]. 0000: select Px0 0001: select Px1 0010: select Px2 0011: select Px3 0100: select Px4 0101: select Px5 0110: select Px6 0111: select Px7 1000: select Px8 1001: select Px9 1010: select Px10 1011: select Px11 1100: select Px12 1101: select Px13 1110: select Px14 1111: select Px15

7.4.3 AFIO Alternate Remap Configuration Register (AFIO_RMP_CFG)

Address offset: 0x04

Reset value: 0x0000 0000



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Bit field	Name	Description
31:27	Reserved	Reserved, the reset value must be maintained.
26:24	SW_JTAG_CFG[2:0]	Serial wire JTAG configuration These bits can only be written by software (reading these bits will return an undefined value) and are used to configure the I/O ports of the SWD-JTAG alternate function. SWD-JTAG (Serial Wire JTAG) supports JTAG or SWD to access Cortex's debug port. The default state after system reset is to enable SWD-JTAG. In this state, JTAG or SW (serial wire) mode can be selected through a specific signal on the JTMS/JTCK pin. 000: Full SWJ (JTAG-DP + SW-DP): reset state; 001: Full SWJ (JTAG-DP + SW-DP) but no NJTRST; 010: Turn off JTAG-DP and enable SW-DP; 100: Turn off JTAG-DP, turn off SW-DP; Other values: no effect.
23	MII_RMII_SEL	Ethernet MAC connection mode selection bit. This bit can be set to '1' or set to '0' by software. It configures the internal Ethernet MAC to use the external MII interface or the transceiver PHY of the RMII interface. 0: Configure the Ethernet MAC to use the transceiver of the external MII interface; 1: Configure the Ethernet MAC to use the transceiver of the external RMII interface.
22:21	Reserved	Reserved, the reset value must be maintained.
20	ADC2_ETRR	ADC2 regular conversion external trigger remapping This bit can be set to '1' or set to '0' by software. It controls the trigger input connected to the external trigger of ADC2 regular conversion. 0: ADC2 regular conversion external trigger is connected to EXTI11 1: ADC2 regular conversion external trigger is connected to TIM8_TRGO
19	ADC2_ETRI	ADC2 injection conversion external trigger remapping This bit can be set to '1' or set to '0' by software. It controls the trigger input connected to the ADC2 injection conversion external trigger. 0: ADC2 injection conversion external trigger is connected to EXTI15 1: ADC2 injection conversion external trigger is connected to TIM8_CH4.
18	ADC1_ETRR	ADC1 regular conversion external trigger remapping This bit can be set to '1' or set to '0' by software. It controls the trigger input connected to the external trigger of ADC1 regular conversion. 0: ADC1 regular conversion external trigger is connected to EXTI11 1: ADC1 regular conversion external trigger is connected to TIM8_TRGO
17	ADC1_ETRI	ADC1 injection conversion external trigger remapping This bit can be set to '1' or set to '0' by software. It controls the trigger input connected to the ADC1 injection conversion external trigger. 0: ADC1 injection conversion external trigger is connected to EXTI15 1: ADC1 injection conversion external trigger is connected to TIM8_CH4
16	TIM5CH4_RMP	TIM5_CH4 internal remapping

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Bit field	Name	Description
		This bit can be set to '1' or set to '0' by software. It controls the internal image of TIM5_CH4. 0: TIM5_CH4 is connected to PA3 1: LSI internal oscillator is connected to TIM5_CH4, the purpose is to calibrate the LSI
15	PD01_RMP	PD0/PD1 mapping on OSC_IN/OSC_OUT (PD0/PD1 mapping on OSC_IN/OSC_OUT) This bit can be set to '1' or set to '0' by software. It controls the GPIO function image of PD0 and PD1. When the main oscillator HSE is not used (the system runs on the internal 8MHz RC oscillator), PD0 and PD1 can be mapped to the OSC_IN and OSC_OUT pins. This function can only be applied to packages with pins below 80 (PD0 and PD1 appear on packages with pins 80 and above and do not need to be remapped). 0: Do not remap PD0 and PD1; 1: PD0 is mapped to OSC_IN, PD1 is mapped to OSC_OUT.
14:13	CAN1_RMP[1:0]	CAN1 alternate function remapping These bits can be set to '1' or set to '0' by software to control the re-mapping of the alternate functions CAN1_RX and CAN1_TX on products with only a single CAN1 interface. 00: CAN1_RX is mapped to PA11, CAN1_TX is mapped to PA12; 01: CAN1_RX is mapped to PD8, CAN1_TX is mapped to PD9; 10: CAN1_RX is mapped to PB8, CAN1_TX is mapped to PB9 (cannot be used for 36-pin package); 11: CAN1_RX is mapped to PD0, CAN1_TX is mapped to PD1.
12	TIM4_RMP	Remapping of Timer 4 This bit can be set to '1' or set to '0' by software to control the mapping of channels 1-4 of TIM4 to the GPIO port. 0: No remapping (TIM4_CH1/PB6, TIM4_CH2/PB7, TIM4_CH3/PB8, TIM4_CH4/PB9); 1: Full image (TIM4_CH1/PD12, TIM4_CH2/PD13, TIM4_CH3/PD14, TIM4_CH4/PD15). *Note: Remapping does not affect TIM4_ETR on PE0.*
11:10	TIM3_RMP[1:0]	Remapping of Timer 3 These bits can be set to '1' or set to '0' by software to control the image of Timer 3 channels 1 to 4 on the GPIO port. 00: no remapping (CH1/PA6, CH2/PA7, CH3/PB0, CH4/PB1); 01: unused combination; 10: Partial image (CH1/PB4, CH2/PB5, CH3/PB0, CH4/PB1); 11: Full image (CH1/PC6, CH2/PC7, CH3/PC8, CH4/PC9). *Note: Remapping does not affect TIM3_ETR on PD2.*
9:8	TIM2_RMP[1:0]	Remapping of Timer 2 These bits can be set to '1' or set to '0' by software to control the image of Timer 2 channels 1 to 4 and external trigger (ETR) on the GPIO port.

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Bit field	Name	Description
		00: no remapping (CH1/ETR/PA0, CH2/PA1, CH3/PA2, CH4/PA3); 01: Partial image (CH1/ETR/PA15, CH2/PB3, CH3/PA2, CH4/PA3); 10: Partial image (CH1/ETR/PA0, CH2/PA1, CH3/PB10, CH4/PB11); 11: Complete image (CH1/ETR/PA15, CH2/PB3, CH3/PB10, CH4/PB11).
7:6	TIM1_RMP[1:0]	Remapping of Timer 1 These bits can be set to '1' or set to '0' by software to control timer 1 channels 1 to 4, 1N to 3N, external trigger (ETR) and brake input (BKIN) The image on the GPIO port. 00: no remap (ETR/PA12, CH1/PA8, CH2/PA9, CH3/PA10, CH4/PA11, BKIN/PB12, CH1N/PB13, CH2N/PB14, CH3N/PB15); 01: partial image (ETR/ PA12, CH1/PA8, CH2/PA9, CH3/PA10, CH4/PA11, BKIN/PA6, CH1N/PA7, CH2N/PB0, CH3N/PB1); 10: Partial image (ETR/PA12, CH1/PA8, CH2/PA9, CH3/PA10, CH4/PA11, BKIN/PB5, CH1N/PB13, CH2N/PB14, CH3N/PB15); 11: Full image (ETR/PE7, CH1/PE9, CH2/PE11, CH3/PE13, CH4/PE14, BKIN/PE15, CH1N/PE8, CH2N/PE10, CH3N/PE12).
5:4	USART3_RMP[1:0]	Remapping of USART3 These bits can be set to '1' or set to '0' by software to control the image of the CTS, RTS, CK, TX and RX alternate functions of USART3 on the GPIO port. 00: No remapping (TX/PB10, RX/PB11, CK/PB12, CTS/PB13, RTS/PB14); 01: Partial image (TX/PC10, RX/PC11, CK/PC12, CTS/PB13, RTS/PB14); 10: Unused combination; 11: Full image (TX/PD8, RX/PD9, CK/PD10, CTS/PD11, RTS/PD12)..
3	USART2_RMP_0	Remapping of USART2 These bits can be set to '1' or set to '0' by software and used in conjunction with USART2_RMP_1 to form USART2_RMP[1:0] to control the image of the CTS, RTS, CK, TX and RX alternate functions of USART2 on the GPIO port. 00: No remapping (CTS/PA0, RTS/PA1, TX/PA2, RX/PA3, CK/PA4); 01: Remapping (CTS/PD3, RTS/PD4, TX/PD5, RX/PD6, CK/PD7); 10: Remapping (CTS/PC6, RTS/PC7, TX/PC8, RX/PC9, CK/-); 11: Remapping (CTS/PA15, RTS/PB3, TX/PB4, RX/PB5, CK/PA4). *Note: Synchronous mode is not supported when the* USART2_RMP[1:0] is 10 .
2	USART1_RMP[1:0]	Remapping of USART1 This bit can be set to '1' or set to '0' by software to control the image of the TX and RX alternate functions of USART1 on the GPIO port. 0: No remapping (TX/PA9, RX/PA10); 1: Remapping (TX/PB6, RX/PB7).
1	I2C1_RMP	Remapping of I2C1 This bit can be set to '1' or set to '0' by software to control the image of I2C1's SCL and SDA alternate functions on the GPIO port. 0: No remapping (SCL/PB6, SDA/PB7); 1: Remapping (SCL/PB8, SDA/PB9).
0	SPI1_RMP_0	Remapping of SPI1

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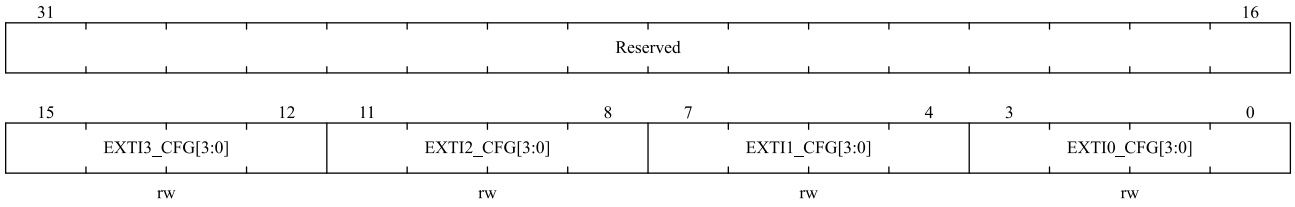
Bit field	Name	Description
		This bit can be set to '1' or set to '0' by software and used in conjunction with SPI1_RMP_1 to form SPI1_RMP[1:0] to control the image of SPI1's NSS, SCK, MISO and MOSI alternate functions on the GPIO port. 00: No remapping (NSS/PA4, SCK/PA5, MISO/PA6, MOSI/PA7); 01: Remapping (NSS/PA15, SCK/PB3, MISO/PB4, MOSI/PB5); 10: Remapping (NSS/PB2, SCK/PA5, MISO/PA6, MOSI/PA7); 11: Remapping (NSS/PB2, SCK/PE7, MISO/PE8, MOSI/PE9);

7.4.4 AFIO External Interrupt Configuration Register 1(AFIO_EXTI_CFG1)

Address offset: 0x08

Reset value: 0x0000 0000



Bit field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained.
15:0	EXTIx_CFG[3:0]	EXTIx configuration (x = 0… 3) These bits can be read and written by software and used to select the input source of the EXTIx external interrupt. EXTI0 configuration： 0000: PA0 pin 0001: PB0 pin 0010: PC0 pin 0011: PD0 pin 0100: PE0 pin 0101: Reserved 0110: PG0 pin EXTI1 configuration： 0000: PA1 pin 0001: PB1 pin 0010: PC1 pin 0011: PD1 pin 0100: PE1 pin 0101: PF1 pin 0110: PG1 pin EXTI2 configuration： 0000: PA2 pin 0001: PB2 pin 0010: PC2 pin 0011: PD2 pin 0100: PE2 pin 0101: PF2 pin 0110: PG2 pin EXTI3 configuration： 0000: PA3 pin 0001: PB3 pin 0010: PC3 pin 0011: PD3 pin 0100: PE3 pin 0101: PF3 pin 0110: PG3 pin

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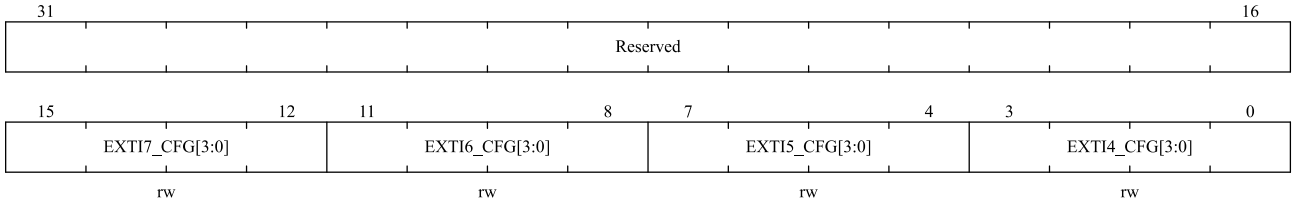
7.4.5 AFIO External Interrupt Configuration Register 2(AFIO_EXTI_CFG2)

Address offset: 0x0C

Reset value: 0x0000 0000

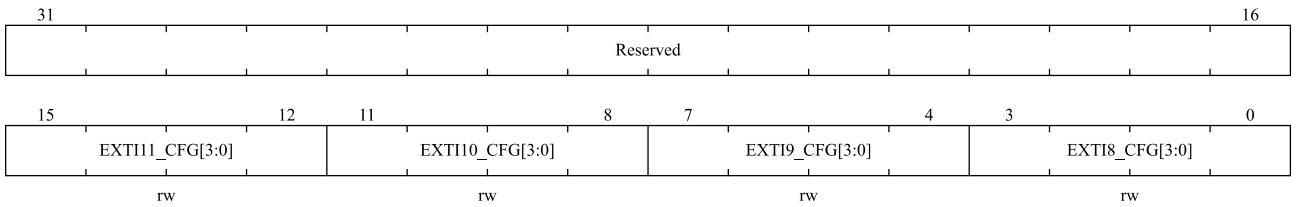


Bit field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained.
15:0	EXTIx_CFG[3:0]	EXTIx configuration (x = 4… 7) These bits can be read and written by software and used to select the input source of the EXTIx external interrupt. EXTI4 configuration： 0000: PA4 pin 0001: PB4 pin 0010: PC4 pin 0011: PD4 pin 0100: PE4 pin 0101: PF4 pin 0110: PG4 pin EXTI5 configuration： 0000: PA5 pin 0001: PB5 pin 0010: PC5 pin 0011: PD5 pin 0100: PE5 pin 0101: PF5 pin 0110: PG5 pin EXTI6 configuration： 0000: PA6 pin 0001: PB6 pin 0010: PC6 pin 0011: PD6 pin 0100: PE6 pin 0101: Reserved 0110: Reserved EXTI7 configuration： 0000: PA7 pin 0001: PB7 pin 0010: PC7 pin 0011: PD7 pin 0100: PE7 pin 0101: Reserved 0110: Reserved

7.4.6 AFIO External Interrupt Configuration Register 3(AFIO_EXTI_CFG3)

Address offset: 0x10

Reset value: 0x0000 0000



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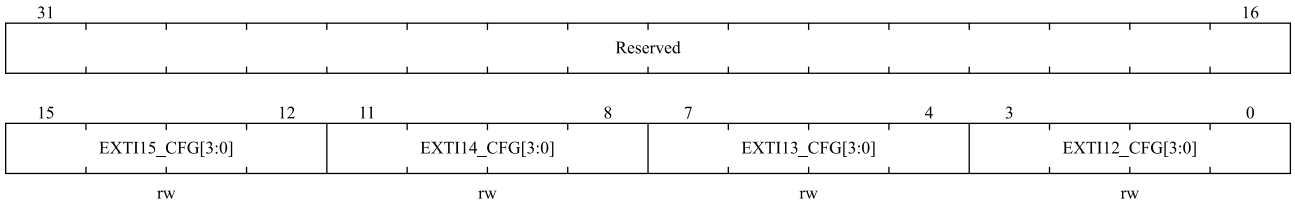
Bit field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained.
15:0	EXTIx_CFG[3:0]	EXTIx configuration (x = 8… 11) These bits can be read and written by software and used to select the input source of the EXTIx external interrupt. EXTI8 configuration： 0000: PA8 pin 0001: PB8 pin 0010: PC8 pin 0011: PD8 pin 0100: PE8 pin 0101: Reserved 0110: Reserved EXTI9 configuration： 0000: PA9 pin 0001: PB9 pin 0010: PC9 pin 0011: PD9 pin 0100: PE9 pin 0101: Reserved 0110: PG9 pin EXTI10 configuration： 0000: PA10 pin 0001: PB10 pin 0010: PC10 pin 0011: PD10 pin 0100: PE10 pin 0101: Reserved 0110: Reserved EXTI11 configuration： 0000: PA11 pin 0001: PB11 pin 0011: PC10 pin 0011: PD11 pin 0100: PE11 pin 0101: Reserved 0110: Reserved

7.4.7 AFIO External Interrupt Configuration Register 4(AFIO_EXTI_CFG4)

Address offset: 0x14

Reset value: 0x0000 0000



Bit field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained.
15:0	EXTIx_CFG[3:0]	EXTIx configuration (x = 12… 15) These bits can be read and written by software and used to select the input source of the EXTIx external interrupt. EXTI12 configuration： 0000: PA12 pin 0001: PB12 pin 0011: PC12 pin 0011: PD12 pin 0100: PE12 pin 0101: PF12 pin 0110: Reserved EXTI13 configuration： 0000: PA13 pin 0001: PB13 pin 0011: PC13 pin

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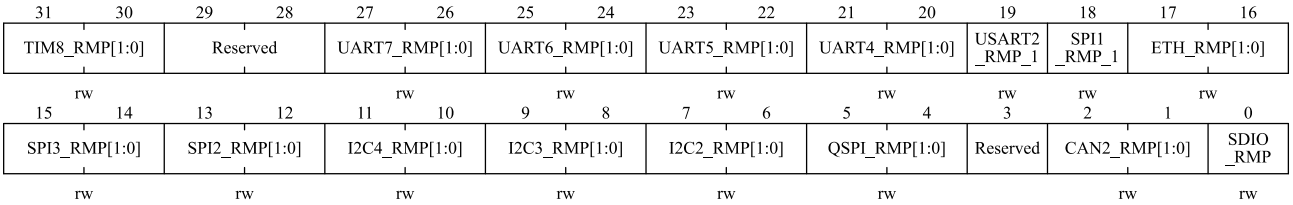
Bit field	Name	Description
		0011: PD13 pin 0100: PE13 pin 0101: PF13 pin 0110: Reserved EXTI14 configuration： 0000: PA14 pin 0001: PB14 pin 0011: PC14 pin 0011: PD14 pin 0100: PE14 pin 0101: PF14 pin 0110: Reserved EXTI15 configuration： 0000: PA15 pin 0001: PB15 pin 0011: PC15 pin 0011: PD15 pin 0100: PE15 pin 0101: PF15 pin 0110: Reserved

7.4.8 AFIO Alternate Remapping Configuration Register 3(AFIO_RMP_CFG3)

Address offset: 0x20

Reset value: 0x0000 0000



Bit field	Name	Description
31:30	TIM8_RMP[1:0]	Remapping of Timer 8 These bits can be set to '1' or set to '0' by software to control the image of Timer 8 channels 1 to 2 on the GPIO port. 00: No remapping (ETR/PA0, CH1/PC6, CH2/PC7, CH3/PC8, CH4/PC9, BKIN/PA6, CH1N/PA7, CH2N/PB0, CH3N/PB1); 01: Partial image (ETR/PB4, CH1/PC6, CH2/PC7, CH3/PC8, CH4/PC9, BKIN/PB3, CH1N/PA15, CH2N/PC12, CH3N/PD2); 10: Unused combination; 11: Partial image (ETR/PB4, CH1/PD14, CH2/PD15, CH3/PC8, CH4/PC9, BKIN/PB3, CH1N/PA15, CH2N/PC12, CH3N/PD2).
29:28	Reserved	Reserved, the reset value must be maintained.
27:26	UART7_RMP[1:0]	Remapping of UART7 These bits can be set to '1' or set to '0' by software to control the image of the TX and RX alternate functions of UART7 on the GPIO port. 00: No remapping (TX/PC4, RX/PC5); 01: Remapping (TX/PC2, RX/PC3); 10: Unused combination; 11: Remapping (TX/PG0, RX/PG1).
25:24	UART6_RMP[1:0]	Remapping of UART6

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Bit field	Name	Description
		These bits can be set to '1' or set to '0' by software to control the image of the TX and RX alternate functions of UART6 on the GPIO port. 00: No remapping (TX/PE2, RX/PE3); 01: Unused combination; 10: Remapping (TX/PC0, RX/PC1); 11: Remapping (TX/PB0, RX/PB1).
23:22	UART5_RMP[1:0]	Remapping of UART5 These bits can be set to '1' or set to '0' by software to control the image of the TX and RX alternate functions of UART5 on the GPIO port. 00: No remapping (TX/PC12, RX/PD2); 01: Remapping (TX/PB13, RX/PB14); 10: Remapping (TX/PE8, RX/PE9); 11: Remapping (TX/PB8, RX/PB9).
21:20	UART4_RMP[1:0]	Remapping of UART4 These bits can be set to '1' or set to '0' by software to control the image of the TX and RX alternate functions of UART4 on the GPIO port. 00: No remapping (TX/PC10, RX/PC11); 01: Remapping (TX/PB2, RX/PE7); 10: Remapping (TX/PA13, RX/PA14); 11: Remapping (TX/PD0, RX/PD1).
19	USART2_RMP_1	Remapping of USART2 These bits can be set to '1' or set to '0' by software and used in conjunction with USART2_RMP_0 to form USART2_RMP[1:0] to control the image of the CTS, RTS, CK, TX and RX alternate functions of USART2 on the GPIO port. 00: No remapping (CTS/PA0, RTS/PA1, TX/PA2, RX/PA3, CK/PA4); 01: Remapping (CTS/PD3, RTS/PD4, TX/PD5, RX/PD6, CK/PD7); 10: Remapping (CTS/PC6, RTS/PC7, TX/PC8, RX/PC9, CK/-); 11: Remapping (CTS/PA15, RTS/PB3, TX/PB4, RX/PB5, CK/PA4). *Note: Synchronous mode is not supported when the* USART2_RMP[1:0] is 10 .
18	SPI1_RMP_1	Remapping of SPI1 This bit can be set to '1' or set to '0' by software and used in conjunction with SPI1_RMP_0 to form SPI1_RMP[1:0] to control the image of NSS, SCK, MISO and MOSI alternate functions of SPI1 on the GPIO port. 00: No remapping (NSS/PA4, SCK/PA5, MISO/PA6, MOSI/PA7); 01: Remapping (NSS/PA15, SCK/PB3, MISO/PB4, MOSI/PB5); 10: Remapping (NSS/PB2, SCK/PA5, MISO/PA6, MOSI/PA7); 11: Remapping (NSS/PB2, SCK/PE7, MISO/PE8, MOSI/PE9);
17:16	ETH_RMP[1:0]	Pin configuration of Ethernet MAC This bit can be set to '1' or '0' by software. It controls the connection of the Ethernet MAC to the external transceiver PHY. 00: No remapping (RX_DV/CRS_DV/PA7, RXD0/PC4, RXD1/PC5, RXD2/PB0, RXD3/PB1, PPS_OUT/PB5, TXD3/PB8); 01: Remapping (RX_DV/CRS_DV/PD8, RXD0/PD9, RXD1/PD10, RXD2/PD11,

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Bit field	Name	Description
		RXD3/PD12, PPS_OUT/PB5, TXD3/PB8); 10: Remapping (RX_DV/CRS_DV/PA7, RXD0/PC4, RXD1/PC5, RXD2/PB0, RXD3/PB1, PPS_OUT/PB6, TXD3/PB7); 11: Remapping (RX_DV/CRS_DV/PD8, RXD0/PD9, RXD1/PD10, RXD2/PB0, RXD3/PB1, PPS_OUT/PB6, TXD3/PB7).
15:14	SPI3_RMP[1:0]	Remapping of SPI3 This bit can be set to '1' or set to '0' by software to control the image of the NSS, SCK, MISO and MOSI alternate functions of SPI3 on the GPIO port. 00: No remapping (NSS/WS/PA15, SCK/CK/PB3, MISO/PB4, MOSI/PB5); 01: Remapping (NSS/WS/PD2, SCK/CK/PC10, MISO/PC11, MOSI/PC12); 10: Remapping (NSS/WS/PD8, SCK/CK/PD9, MISO/PD11, MOSI/PD12); 11: Remapping (NSS/WS/PC2, SCK/CK/PC3, MISO/PA0, MOSI/PA1).
13:12	SPI2_RMP[1:0]	Remapping of SPI2 This bit can be set to '1' or set to '0' by software to control the image of the NSS, SCK, MISO and MOSI alternate functions of SPI2 on the GPIO port. 00: No remapping (NSS/WS/PB12, SCK/CK/PB13, MISO/PB14, MOSI/PB15); 01: Remapping (NSS/WS/PC6, SCK/CK/PC7, MISO/PC8, MOSI/PC9); 10: Unused combination; 11: Remapping (NSS/WS/PE10, SCK/CK/PE11, MISO/PE12, MOSI/PE13).
11:10	I2C4_RMP[1:0]	I2C4 remapping This bit can be set to '1' or set to '0' by software to control the image of I2C4's SDA and SCL alternate functions on the GPIO port. 00: No remapping (SCL/PC6, SDA/PC7); 01: Remapping (SCL/PD14, SDA/PD15); 10: Unused combination; 11: Remapping (SCL/PA9, SDA/PA10).
9:8	I2C3_RMP[1:0]	I2C3 remapping This bit can be set to '1' or set to '0' by software to control the image of I2C3's SDA and SCL alternate functions on the GPIO port. 00: No remapping (SCL/PC0, SDA/PC1); 01: Unused combination; 10: Remapping (SCL/PF4, SDA/PF5); 11: Remapping (SCL/PA4, SDA/PC5).
7:6	I2C2_RMP[1:0]	I2C2 remapping This bit can be set to '1' or set to '0' by software to control the image of I2C2's SDA and SCL alternate functions on the GPIO port. 00: No remapping (SCL/PB10, SDA/PB11); 01: Remapping (SCL/PG2, SDA/PG3); 10: Unused combination; 11: Remapping (SCL/PC4, SDA/PA5).
5:4	QSPI_RMP[1:0]	Remapping of QSPI This bit can be set to '1' or set to '0' by software to control the image of QSPI's IO0, IO1, IO2, IO3, CLK, and NSS alternate functions on the GPIO port.

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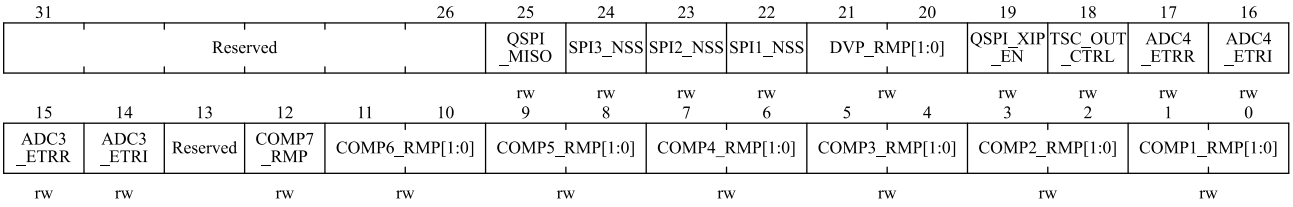
Bit field	Name	Description
		00: No remapping (NSS/PA4, SCK/PA5, IO0/PA6, IO1/PA7, IO2/PC4, IO3/PC5); 01: Unused combination; 10: Remapping (NSS/PF0, SCK/PF1, IO0/PF2, IO1/PF3, IO2/PF4, IO3/PF5); 11: Remapping (NSS/PC10, SCK/PC11, IO0/PC12, IO1/PD0, IO2/PD1, IO3/PD2).
3	Reserved	Reserved, the reset value must be maintained.
2:1	CAN2_RMP[1:0]	CAN2 remapping This bit can be set to '1' or set to '0' by software to control the image of the CAN2_RX and CAN2_TX alternate functions of CAN2 on the GPIO port. 00: No remapping (RX/PB12, TX/PB13); 01: Remapping (RX/PB5, TX/PB6); 10: Unused combination; 11: Remapping (RX/PD10, TX/PD11).
0	SDIO_RMP	SDIO remapping This bit can be set to '1' or set to '0' by software to control the image of the alternate function port. D4/PB8, D5/PB9, D6/PC6, D7/PC7 are not re-imaged. 0: No remapping (DO/PC8, D1/PC9, D2/PC10, D3/PC11, CK/PC12, CMD/PD2); 1: Remapping (DO/PE8, D1/PE9, D2/PE10, D3/PE11, CK/PE12, CMD/PE13);

7.4.9 AFIO Alternate Remap Configuration Register 4 (AFIO_ RMP_CFG4)

Address offset: 0x24

Reset value: 0x0000 0000



Bit field	Name	Description
31:26	Reserved	Reserved, the reset value must be maintained.
25	QSPI_MISO	The IO1 pin of QSPI is equivalent to MISO in standard single-wire mode, and the pin attributes can be configured as: 0: The QSPI module automatically controls whether it is input or output 1: Fixed as input floating
24	SPI3_NSS	NSS mode bit of SPI3 (when NSS is configured as AFIO push-pull). 0: NSS is high impedance when idle 1: NSS is 1 when idle
23	SPI2_NSS	NSS mode bit of SPI2 (when NSS is configured as AFIO push-pull). 0: NSS is high impedance when idle 1: NSS is 1 when idle
22	SPI1_NSS	NSS mode bit of SPI1 (when NSS is configured as AFIO push-pull). 0: NSS is high impedance when idle

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Bit field	Name	Description
		1: NSS is 1 when idle
21:20	DVP_RMP[1:0]	Remapping of DVP This bit can be set to '1' or '0' by software. 00: No remapping (HSYNC/PA1, VSYNC/PA2, CLK/PA3, D0/PA4, D1/PA5, D2/PA6, D3/PA7, D4/PC4, D5/PC5, D6/PB0, D7/PB1) ； 01: Remapping (HSYNC/PE2, VSYNC/PE3, CLK/PE4, D0/PE5, D1/PE6, D2/PC0, D3/PB2, D4/PF12, D5/PF13, D6/PF14, D7/PF15); 10: Unused combination; 11: Remapping (HSYNC/PE2, VSYNC/PE3, CLK/PE4, D0/PE5, D1/PE6, D2/PC0, D3/PB2, D4/PB10, D5/PB11, D6/PF14, D7/PF15).
19	QSPI_XIP_EN	QSPI XIP memory mapping mode enable control 0: Disable 1: Enable
18	Reserved	Reserved, the reset value must be maintained.
17	ADC4_ETRR	ADC4 regular conversion external trigger remapping This bit can be set to '1' or '0' by software. It controls the trigger input connected to the external trigger of ADC4 regular conversion. 0: ADC4 regular conversion external trigger is connected to EXTI10 1: ADC4 regular conversion external trigger is connected to TIM5_CH3
16	ADC4_ETRI	ADC4 injection conversion external trigger remapping This bit can be set to '1' or '0' by software. It controls the trigger input connected to the ADC4 injection conversion external trigger. 0: ADC4 injection conversion external trigger is connected to EXTI14 1: ADC4 injection conversion external trigger is connected to TIM5_CH4.
15	ADC3_ETRR	ADC3 regular conversion external trigger remapping This bit can be set to '1' or '0' by software. It controls the trigger input connected to the external trigger of ADC3 regular conversion. 0: ADC3 regular conversion external trigger is connected to EXTI10 1: ADC3 regular conversion external trigger is connected to TIM5_CH3
14	ADC3_ETRI	ADC3 injection conversion external trigger remapping This bit can be set to '1' or '0' by software. It controls the trigger input connected to the ADC3 injection conversion external trigger. 0: ADC3 injection conversion external trigger is connected to EXTI14 1: ADC3 injection conversion external trigger is connected to TIM5_CH4
13	Reserved	Reserved, the reset value must be maintained.
12	COMP7_RMP	Remapping of COMP7_OUT This bit can be set to '1' or '0' by software. 0: No remapping (COMP7_OUT/PC2); 1: Remapping (COMP7_OUT/PD12).
11:10	COMP6_RMP[1:0]	Remapping of COMP6_OUT This bit can be set to '1' or '0' by software. 00: No remapping (COMP6_OUT/PC9); 01: Remapping (COMP6_OUT/PA12);

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Bit field	Name	Description
		10: Unused combination; 11: Remapping (COMP6_OUT/PB7).
9:8	COMP5_RMP[1:0]	Remapping of COMP5_OUT This bit can be set to '1' or '0' by software. 00: No remapping (COMP5_OUT/PB0); 01: Remapping (COMP5_OUT/PB11); 10: Remapping (COMP5_OUT/PB6); 11: Remapping (COMP5_OUT/PA11).
7:6	COMP4_RMP[1:0]	Remapping of COMP4_OUT This bit can be set to '1' or '0' by software. 00: No remapping (COMP4_OUT/PC5); 01: Remapping (COMP4_OUT/PB12); 10: Unused combination; 11: Remapping (COMP4_OUT/PC11).
5:4	COMP3_RMP[1:0]	Remapping of COMP3_OUT This bit can be set to '1' or '0' by software. 00: No remapping (COMP3_OUT/PB10); 01: Remapping (COMP3_OUT/PC10); 10: Unused combination; 11: Remapping (COMP3_OUT/PA2).
3:2	COMP2_RMP[1:0]	Remapping of COMP2_OUT This bit can be set to '1' or '0' by software. 00: No remapping (COMP2_OUT/PA6); 01: Remapping (COMP2_OUT/PA7); 10: Remapping (COMP2_OUT/PA12); 11: Remapping (COMP2_OUT/PB9).
1:0	COMP1_RMP[1:0]	Remapping of COMP1_OUT This bit can be set to '1' or '0' by software. 00: No remapping (COMP1_OUT/PA0); 01: Remapping (COMP1_OUT/PB1); 10: Remapping (COMP1_OUT/PA11); 11: Remapping (COMP1_OUT/PB8).

7.4.10 AFIO Alternate Remapping Configuration Register 5(AFIO_RMP_CFG5)

Address offset: 0x28

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved								EGB4_DET_EN	EGB3_DET_EN	EGB2_DET_EN	EGB1_DET_EN	EGBN4_DET_EN	EGBN3_DET_EN	EGBN2_DET_EN	EGBN1_DET_EN
								rw	rw	rw	rw	rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ECLAMP4_DET_EN	ECLAMP3_DET_EN	ECLAMP2_DET_EN	ECLAMP1_DET_EN	EGB4_RST_EN	EGB3_RST_EN	EGB2_RST_EN	EGB1_RST_EN	EGBN4_RST_EN	EGBN3_RST_EN	EGBN2_RST_EN	EGBN1_RST_EN	ECLAMP4_RST_EN	ECLAMP3_RST_EN	ECLAMP2_RST_EN	ECLAMP1_RST_EN
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

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Bit field	Name	Description
31:24	Reserved	Reserved, the reset value must be maintained.
23	EGB4_DET_EN	EMC GB4 detection enable bit (ground bounce detection). 0: Disable 1: Enable
22	EGB3_DET_EN	EMC GB3 detection enable bit. 0: Disable 1: Enable
21	EGB2_DET_EN	EMC GB2 detection enable bit. 0: Disable 1: Enable
20	EGB1_DET_EN	EMC GB1 detection enable bit. 0: Disable 1: Enable
19	EGBN4_DET_EN	EMC GBN4 detection enable bit. 0: Disable 1: Enable
18	EGBN3_DET_EN	EMC GBN3 detection enable bit. 0: Disable 1: Enable
17	EGBN2_DET_EN	EMC GBN2 detection enable bit. 0: Disable 1: Enable
16	EGBN1_DET_EN	EMC GBN1 detection enable bit. 0: Disable 1: Enable
15	ECLAMP4_DET_EN	EMC CLAMP4 detection enable bit for VDD_4. 0: Disable 1: Enable
14	ECLAMP3_DET_EN	EMC CLAMP3 detection enable bit for VDD_3. 0: Disable 1: Enable
13	ECLAMP2_DET_EN	EMC CLAMP2 detection enable bit for VDD_2. 0: Disable 1: Enable
12	ECLAMP1_DET_EN	EMC CLAMP1 detection enable bit for VDD_1. 0: Disable 1: Enable
11	EGB4_RST_EN	When EMC GB4 detects it, the system resets the enable bit. 0: Disable 1: Enable
10	EGB3_RST_EN	When EMC GB3 detects it, the system resets the enable bit. 0: Disable 1: Enable

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Bit field	Name	Description
9	EGB2_RST_EN	When EMC GB2 detects it, the system resets the enable bit. 0: Disable 1: Enable
8	EGB1_RST_EN	When EMC GB1 detects it, the system resets the enable bit. 0: Disable 1: Enable
7	EGBN4_RST_EN	When EMC GBN4 detects it, the system resets the enable bit. 0: Disable 1: Enable
6	EGBN3_RST_EN	When EMC GBN3 detects it, the system resets the enable bit. 0: Disable 1: Enable
5	EGBN2_RST_EN	When EMC GBN2 is detected, the system resets the enable bit. 0: Disable 1: Enable
4	EGBN1_RST_EN	When EMC GBN1 is detected, the system resets the enable bit. 0: Disable 1: Enable
3	ECLAMP4_RST_EN	When EMC CLAMP4 detects it, the system resets the enable bit. 0: Disable 1: Enable
2	ECLAMP3_RST_EN	When EMC CLAMP3 detects, the system resets the enable bit. 0: Disable 1: Enable
1	ECLAMP2_RST_EN	When EMC CLAMP2 detects, the system resets the enable bit. 0: Disable 1: Enable
0	ECLAMP1_RST_EN	When EMC CLAMP1 detects, the system resets the enable bit. 0: Disable 1: Enable

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8 DMA Controller

8.1 Introduction

The DMA controller can access totally 8 AHB slaves: Flash, SRAM, ADC, SDIO, QSPI, ETH, ABP1 and APB2. DMA Controller is controlled by CPU to perform fast data movement from source to destination. After configuration, data can be transferred without CPU intervention. Thus, CPU can be released for other computation/control tasks or save overall system power consumption.

The chip has two DMA (DMA1, DMA2) controllers, and each DMA controller has 8 logical channels. Each logic channel is to serve memory access requests from single or multiple peripherals. Internal arbiter controls the priority of different DMA channels.

8.2 Main Features

- 16 independently configurable DMA channels: 8 channels each for DMA1 and DMA2.
- Support three transfer types which are Memory-to-Memory, Memory-to-Peripheral and Peripheral-to-Memory.
- Each DMA channel supports hardware requests and software triggers to initiate transfer, and is configured by software.
- Each DMA channel has dedicated software priority level (DMA_CHCFGx.PRIOLVL [1:0] bits, corresponding to 4 levels of priority) which can be configured individually. Channels with the same software priority level will further compare hardware index (channel number) to decide final priority (lower index number channel will has higher priority).
- Configurable source and destination size. Address setting should correspond to data size.
- Configurable circular transfer mode for each channel.
- Each channel has 3 independent event flags and interrupts (Transfer complete, Half transfer, Transfer error), and 1 global interrupt flag (set by logical OR of 3 events).
- Access totally 8 AHB slaves: Flash, SRAM, ADC, SDIO, QSPI, ETH, APB1 and APB2.
- Configurable data transmit number (0~65535).

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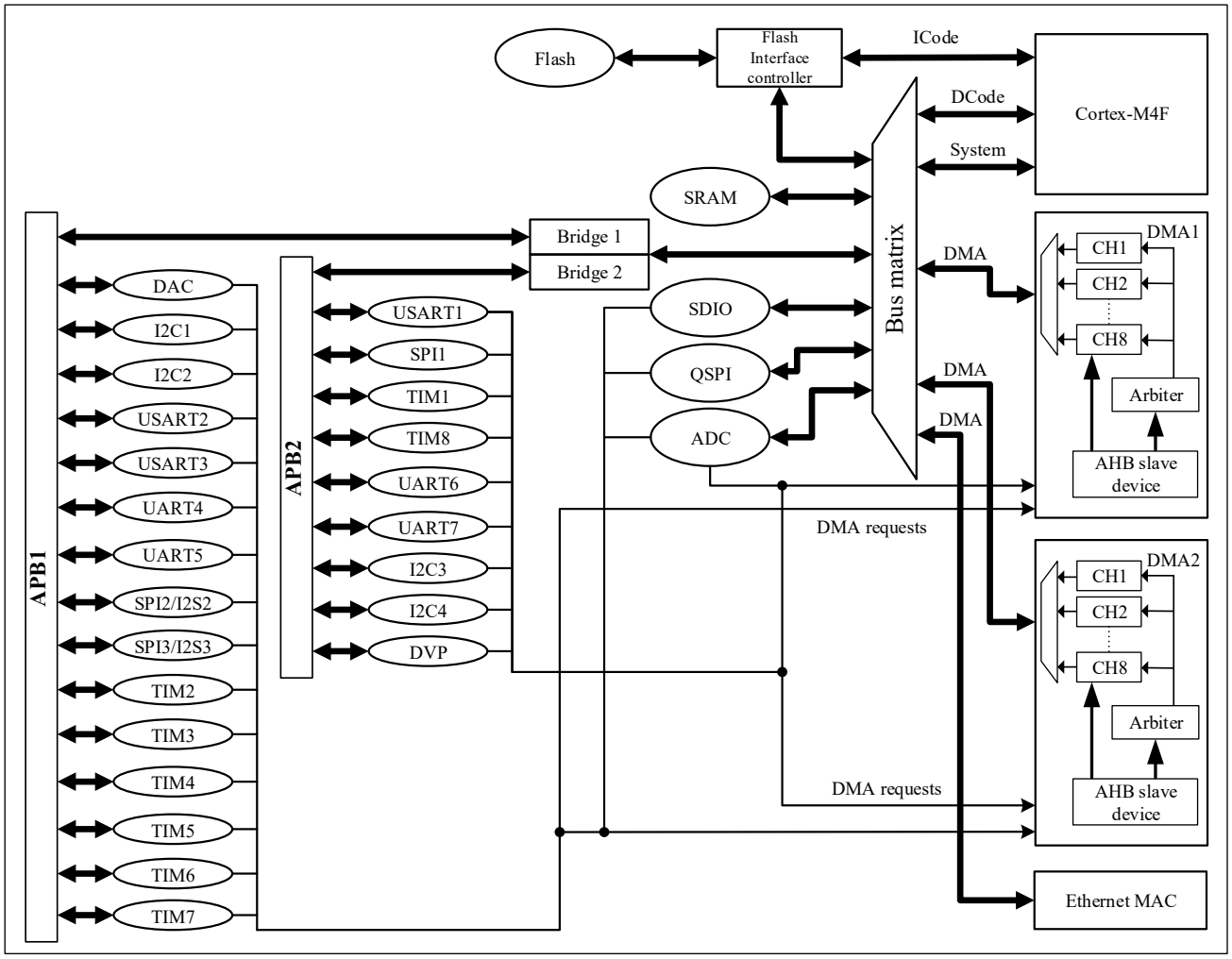
8.3 Block Diagram

Figure 8-1 DMA block diagram



8.4 Function Description

DMA controller and Cortex™-M4F core share the same system data bus. When CPU and DMA access the same target (RAM or peripheral) at the same time, DMA request will suspend CPU from accessing the system bus for several cycles, and the bus arbiter will perform cyclic scheduling. This allows the CPU to get at least half of the system bus (memory or peripheral) bandwidth.

8.4.1 DMA Operation

A DMA request can be triggered by hardware peripherals or software, and the DMA controller processes the request according to the priority level of the channel. The data is read from the source address according to the configured transfer address and bit width, and then the read data is stored in the destination address space. After one operation, the controller calculates the number of remaining transfers and updates the source address and the destination address of the next transfer.

Each DMA data transfer consists of three operations:

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- Data access: determine the source address (DMA_PADDRx or DMA_MADDRx) according to the transfer direction and read data from the source address.
- Data storage: determine the destination address (DMA_PADDRx or DMA_MADDRx) according to the transfer direction and store the read data into the destination address space.
- Calculate the number of outstanding operations, perform a decrement operation of the DMA_TXNUMx register, and update the source and destination addresses of the next operation.

8.4.2 Channel Priority and Arbitration

The DMA uses an arbitration strategy to handle multiple requests from different channels. The priority of each channel is programmable in the channel control register (DMA_CHCFGx).

4 levels of priority:

- Very high priority
- High priority
- Medium priority
- Low priority

By default, channel with lower index has higher priority if the programmed priority is the same.

8.4.3 DMA Channels and Number of Transfers

Each channel can perform DMA transfer between the peripheral register at the specified address and the memory address. The number of data transferred by DMA is programmable, and the maximum supported value is 65535. The DMA_TXNUM register is decremented after each transfer.

8.4.4 Programmable Data Bit Width

Peripheral and memory transfer data bit width supports byte, half-word and word, which can be programmed through DMA_CHCFGx.PSIZE and DMA_CHCFGx.MSIZE.

When DMA_CHCFGx.PSIZE and DMA_CHCFGx.MSIZE are different, the DMA module aligns the data according to the Table 8-1 below.

Table 8-1 Programmable data width and endian operation (when PINC = MINC = 1)

Source width (bit)	Destination width (bit)	Number of transfer (bit)	Source: Address / data	Transfer operations (R: Read,W: Write)	Destination: Address / data
8	8	4	0x0 / B0 0x1 / B1 0x2 / B2 0x3 / B3	1: R B0 [7:0] @0x0, W B0 [7:0] @0x0 2: R B1 [7:0] @0x1, W B1 [7:0] @0x1 3: R B2 [7:0] @0x2, W B2 [7:0] @0x2 4: R B3 [7:0] @0x3, W B3 [7:0] @0x3	0x0 / B0 0x1 / B1 0x2 / B2 0x3 / B3
8	16	4	0x0 / B0	1: R B0 [7:0] @0x0, W 00B0 [15:0] @0x0	0x0 / 00B0

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Source width (bit)	Destination width (bit)	Number of transfer (bit)	Source: Address / data	Transfer operations (R: Read,W: Write)	Destination: Address / data
			0x1 / B1	2: R B1 [7:0] @0x1, W 00B1 [15:0] @0x2	0x2 / 00B1
			0x2 / B2	3: R B2 [7:0] @0x2, W 00B2 [15:0] @0x4	0x4 / 00B2
			0x3 / B3	4: R B3 [7:0] @0x3, W 00B3 [15:0] @0x6	0x6 / 00B3
8	32	4	0x0 / B0	1: R B0 [7:0] @0x0, W 000000B0 [31:0] @0x0	0x0 / 000000B0
			0x1 / B1	2: R B1 [7:0] @0x1, W 000000B1 [31:0] @0x4	0x4 / 000000B1
			0x2 / B2	3: R B2 [7:0] @0x2, W 000000B2 [31:0] @0x8	0x8 / 000000B2
			0x3 / B3	4: R B3 [7:0] @0x3, W 000000B3 [31:0] @0xC	0xC / 000000B3
16	8	4	0x0 / B1B0	1: R B1B0 [15:0] @0x0, W B0 [7:0] @0x0	0x0 / B0
			0x2 / B3B2	2: R B3B2 [15:0] @0x2, W B2 [7:0] @0x1	0x1 / B2
			0x4 / B5B4	3: R B5B4 [15:0] @0x4, W B4 [7:0] @0x2	0x2 / B4
			0x6 / B7B6	4: R B7B6 [15:0] @0x6, W B6 [7:0] @0x3	0x3 / B6
16	16	4	0x0 / B1B0	1: R B1B0 [15:0] @0x0, W B1B0 [15:0] @0x0	0x0 / B1B0
			0x2 / B3B2	2: R B3B2 [15:0] @0x2, W B3B2 [15:0] @0x2	0x2 / B3B2
			0x4 / B5B4	3: R B5B4 [15:0] @0x4, W B5B4 [15:0] @0x4	0x4 / B5B4
			0x6 / B7B6	4: R B7B6 [15:0] @0x6, W B7B6 [15:0] @0x6	0x6 / B7B6
16	32	4	0x0 / B1B0	1: R B1B0 [15:0] @0x0, W 0000B1B0 [31:0] @0x0	0x0 / 0000B1B0
			0x2 / B3B2	2: R B3B2 [15:0] @0x2, W 0000B3B2 [31:0] @0x4	0x4 / 0000B3B2
			0x4 / B5B4	3: R B5B4 [15:0] @0x4, W 0000B5B4 [31:0] @0x8	0x8 / 0000B5B4
			0x6 / B7B6	4: R B7B6 [15:0] @0x6, W 0000B7B6 [31:0] @0xC	0xC / 0000B7B6
32	8	4	0x0 / B3B2B1B0	1: R B3B2B1B0 [31:0] @0x0, W B0 [7:0] @0x0	0x0 / B0
			0x4 / B7B6B5B4	2: R B7B6B5B4 [31:0] @0x4, W B4 [7:0] @0x1	0x1 / B4
			0x8 / BBBAB9B8	3: R BBBAB9B8 [31:0] @0x8, W B8 [7:0] @0x2	0x2 / B8
			0xC / BFBEBDBC	4: R BFBEBDBC [31:0] @0xC, W BC [7:0] @0x3	0x3 / BC
32	16	4	0x0 / B3B2B1B0	1: R B3B2B1B0 [31:0] @0x0, W B1B0 [15:0] @0x0	0x0 / B1B0
			0x4 / B7B6B5B4	2: R B7B6B5B4 [31:0] @0x4, W B5B4 [15:0] @0x2	0x2 / B5B4
			0x8 / BBBAB9B8	3: R BBBAB9B8 [31:0] @0x8, W B9B8 [15:0] @0x4	0x4 / B9B8
			0xC / BFBEBDBC	4: R BFBEBDBC [31:0] @0xC, W BDBC [15:0] @0x6	0x6 / BDBC
32	32	4	0x0 / B3B2B1B0	1: R B3B2B1B0 [31:0] @0x0, W B3B2B1B0 [31:0] @0x0	0x0 / B3B2B1B0
			0x4 / B7B6B5B4	2: R B7B6B5B4 [31:0] @0x4, W B7B6B5B4 [31:0] @0x4	0x4 / B7B6B5B4
			0x8 / BBBAB9B8	3: R BBBAB9B8 [31:0] @0x8, W BBBAB9B8 [31:0] @0x8	0x8 / BBBAB9B8
			0xC / BFBEBDBC	4: R BFBEBDBC [31:0] @0xC, W BFBEBDBC [31:0] @0xC	0xC / BFBEBDBC

Note:

DMA always provide full 32-bits data to HWDATA[31:0] no matter what destination size it is (HSIZE still follows destination size setting for device supports byte/half-word operation). The HWDATA[31:0] it provides follow rules as follow:

- When source size is smaller than destination size, DMA pads the MSB with 0 until their sizes match and duplicates it to be 32 bits. E.g., source is 8 bits data 0x55 and destination size is 16 bits. DMA pads the source data with 0 to make it 16 bits and become 0x0055, then duplicate it to 32-bit data 0x0055_0055 and provide to HWDATA[31:0]; (if destination size is 32-bit then DMA will only pad source data with 0).

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- When source size is larger or equal to destination size and smaller than 32 bits, DMA duplicates source data to 32 bits data. E.g., source data is 8 bits data 0x1F, HWDATA[31:0] =0x1F1F_1F1F. if source data is 16 bits data 0x2345, then HWDATA[31:0] = 0x2345_2345.

This guarantees peripherals that only support word operation won't generate bus error and the desired data can still move to the place we want with extra bits i.e. 0 padding. If user wants to configure an 8-bit register but is aligned to a 32-bit address boundary, the source size should be set to 8 bits and destination to 32 bits so extra bits will be padded with 0.

8.4.5 Peripheral/Memory Address Incrementation

DMA_CHCFGx.PINC and DMA_CHCFGx.MINC respectively control whether the peripheral address and memory address are enabled in auto-increment mode. The software cannot (can read) write the address register during transfer.

- In auto-increment mode, the next address to be transferred is automatically increased according to the data bit width (1, 2 or 4) after each transfer. The address of the first transfer is stored in DMA_PADDRx or DMA_MADDRx register.
- In fixed mode, the address is always fixed to the initial address.

At the end of transfer (i.e. the transfer count changes to 0), different processes will be carried out according to whether the current work is under circular mode or not.

- In acyclic mode, DMA stops after the transfer is completed. To start a new DMA transfer, need to rewrite the transfer number in the DMA_TXNUMx register with the DMA channel disabled.
- In circular mode, at the end of a transfer, the content of the DMA_TXNUMx register will be automatically reloaded to its initial value, and the current internal peripheral or memory address register will also be reloaded to the initial base address set by the DMA_PADDRx or DMA_MADDRx register.

8.4.6 Channel Configuration Procedure

The detail configuration flow is as below：

1. Configure interrupt mask bits, 1: enable interrupts, 0 disable interrupts.
2. Configure channel peripheral address and memory address and transfer direction.
3. Configure channel priority, 0: lowest, 3: highest.
4. Configure peripheral and memory address increment.
5. Configure channel transfer block size.
6. If necessary, configure circular mode.
7. If it is memory to memory, configure MEM2MEM mode.
8. Repeat step 1~8 on channel 1~8.
9. Enable corresponding channel.

If software is used to serve interrupt, software must enquire interrupt status register to check which interrupt occurred (software needs to write 1 to interrupt flag clear bit to clear the corresponding interrupt). Before enable channel, all interrupts corresponding to the channel should be cleared.

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If the interrupt is transfer complete interrupt, software can configure the next transfer, or report to user this channel transformation is done.

8.4.7 Flow Control

Three major flow controls are supported:

- Memory to memory
- Memory to peripheral
- Peripheral to memory

Flow control is controlled by two register bits in each DMA channel configuration register. Flow control is used to control source/destination and direction of DMA channel.

Table 8-2 Flow control table

DMA_CHCFGx.MEM2MEM	DMA_CHCFGx.DIR	Source	Destination	Transfer
1	x	Memory	Memory	AHB read to AHB write, can do back2back transfer
0	1	Memory	AHB Peripheral	AHB read to AHB write, single transfer
			APB Peripheral	AHB read to APB write, single transfer
0	0	AHB Peripheral	Memory	AHB read to AHB write, single transfer
		APB Peripheral		APB read to AHB write, single transfer

8.4.8 Circular Mode

The circular mode is used to process circular buffers and continuous data transmission (such as ADC scan mode). The DMA_CHCFGx.CIRC is used to enable this function. When the circular mode is activated, if the number of data to be transferred becomes 0, it will automatically be restored to the initial value when configuring the channel, and the DMA operation will continue.

If the user wants to turn off the circular mode, the user needs to write 0 to DMA_CHCFGx.CHEN to disable the DMA channel, and then write 0 to DMA_CHCFGx.CIRC (when DMA_CHCFGx.CHEN is 1, other bits in the DMA_CHCFGx register cannot be rewritten).

8.4.9 Error Management

DMA access to a reserved address area will cause DMA transmission errors. When an error occurs, the transfer error flag is set, and the hardware automatically clears the current DMA channel enable bit (DMA_CHCFGx.CHEN), and the channel operation is stopped. If the transfer error interrupt enable bit is set in the DMA_CHCFGx register, an interrupt will be generated.

8.4.10 Interrupt

- Transfer complete interrupt:

  An interrupt is generated when channel data transfer is complete. Interrupt is a level signal. Each channel has

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its dedicated interrupt, interrupt mask control and interrupt status bit. interrupt status bit is cleared when interrupt flag clear bit is set.

- Half transfer interrupt:

  An interrupt is generated when half of the channel data is transferred. Interrupt is a level signal. Each channel has its dedicated interrupt, interrupt mask control and interrupt status bit. interrupt status bit is cleared when interrupt flag clear bit is set.

- Transfer error interrupt:

  An interrupt is generated when bus returned error. Interrupt is a level signal. Each channel has its dedicated interrupt, interrupt mask control and interrupt status bit. interrupt status bit is cleared when interrupt flag clear bit is set.

Table 8-3 DMA interrupt request

Interrupt event	Event flag bit	Enable control bit
Half transfer	HTXF	HTXIE
Transfer complete	TXCF	TXCIE
Transfer error	ERRF	ERRIE

8.4.11 DMA Request Mapping

8.4.11.1 DMA1 controller

The DMA1 request mapping is shown in the following figure. By configuring the registers of the corresponding peripherals, the DMA requests of each peripheral can be turned on or off independently, and according to the channel priority, only one request is valid at the same time.

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Figure 8-2 DMA1 request mapping

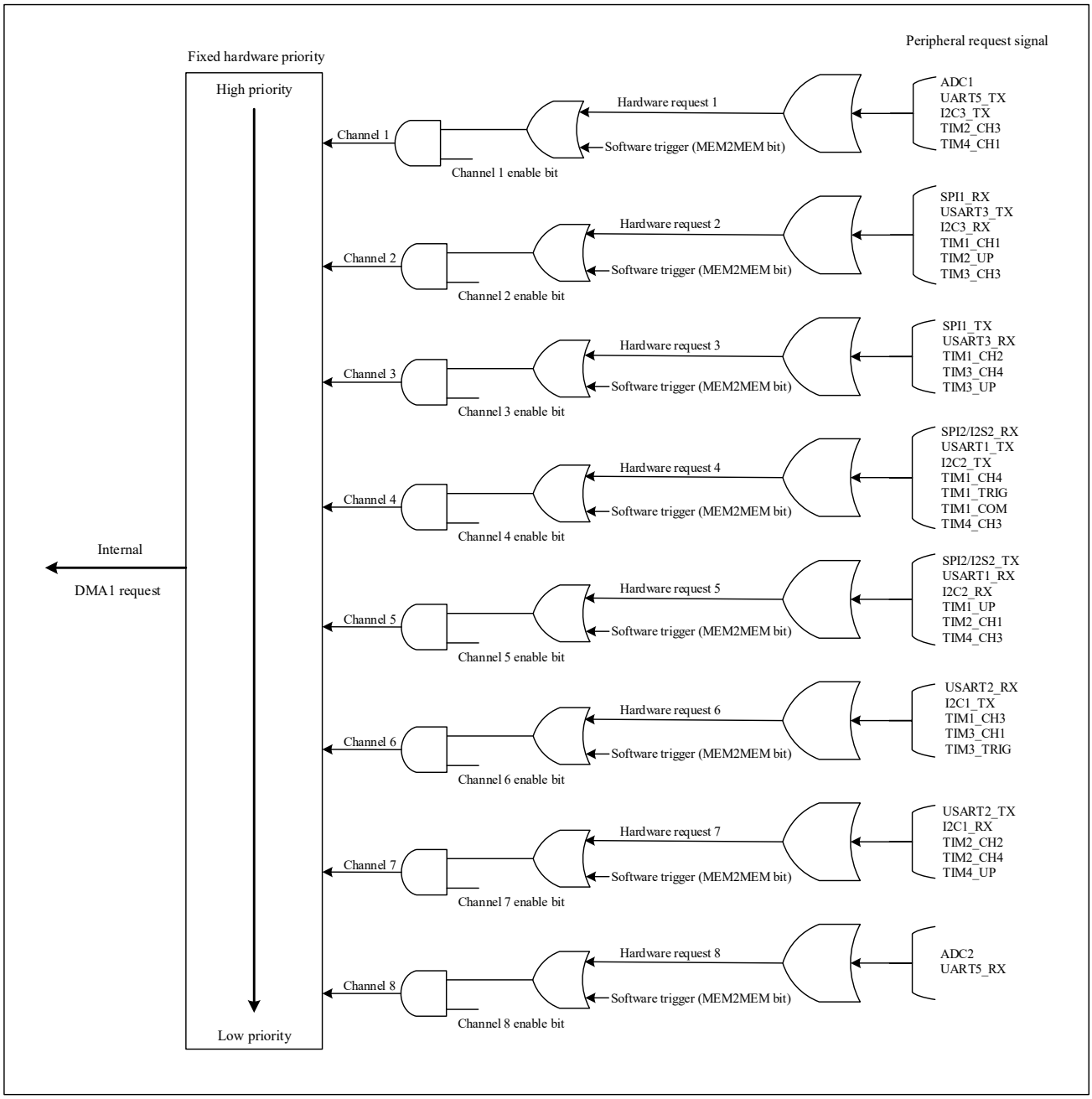

Table 8-4 DMA1 request mapping table for each channel

Peripheral	Channel 1	Channel 2	Channel 3	Channel 4	Channel 5	Channel 6	Channel 7	Channel 8
ADC	ADC1	-	-	-	-	-	-	ADC2
SPI/I2S	-	SPI1_RX	SPI1_TX	SPI2/I2S2_RX	SPI2/I2S2_TX	-	-	-
USART	UART5_TX	USART3_TX	USART3_RX	USART1_TX	USART1_RX	USART2_RX	USART2_TX	UART5_RX
I2C	I2C3_TX	I2C3_RX		I2C2_TX	I2C2_RX	I2C1_TX	I2C1_RX	
TIM1	-	TIM1_CH1	TIM1_CH2	TIM1_CH4 TIM1_TRIG TIM1_COM	TIM1_UP	TIM1_CH3	-	-
TIM2	TIM2_CH3	TIM2_UP	-	-	TIM2_CH1	-	TIM2_CH2	-

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Peripheral	Channel 1	Channel 2	Channel 3	Channel 4	Channel 5	Channel 6	Channel 7	Channel 8
							TIM2_CH4	
TIM3	-	TIM3_CH3	TIM3_CH4 TIM3_UP	-	-	TIM3_CH1 TIM3_TRIG	-	-
TIM4	TIM4_CH1	-	-	TIM4_CH2	TIM4_CH3	-	TIM4_UP	-

8.4.11.2 DMA2 controller

The DMA2 request mapping is shown in the following figure. By configuring the registers of the corresponding peripherals, the DMA requests of each peripheral can be turned on or off independently, and according to the channel priority, only one request is valid at the same time.

Figure 8-3 DMA2 request mapping

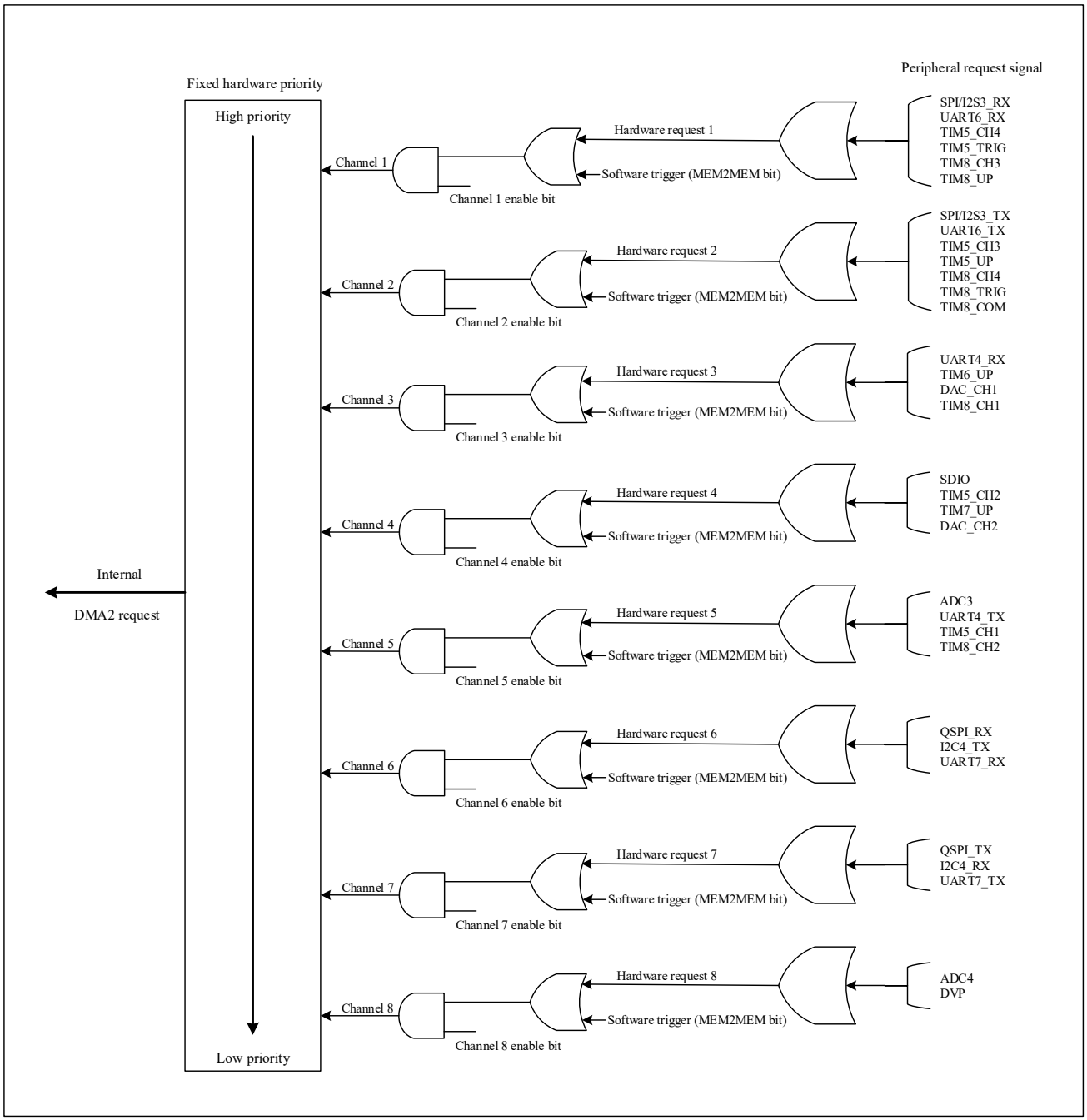

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Table 8-5 DMA2 request mapping table for each channel

Peripheral	Channel 1	Channel 2	Channel 3	Channel 4	Channel 5	Channel 6	Channel 7	Channel 8
ADC	-	-	-	-	ADC3	-	-	ADC4
SPI/I2S	SPI3/I2S3_RX	SPI3/I2S3_TX	-	-	-	QSPI_RX	QSPI_TX	-
I2C4	-	-	-	-	-	I2C4_TX	I2C4_RX	-
UART	UART6_RX	UART6_TX	UART4_RX	-	UART4_TX	UART7_RX	UART7_TX	-
SDIO	-	-	-	SDIO	-	-	-	-
TIM5	TIM5_CH4 TIM5_TRIG	TIM5_CH3 TIM5_UP	-	TIM5_CH2	TIM5_CH1	-	-	-
TIM6/DAC	-	-	TIM6_UP DAC_CH1	-	-	-	-	-
TIM7/DAC	-	-	-	TIM7_UP DAC_CH2	-	-	-	-
TIM8	TIM8_CH3 TIM8_UP	TIM8_CH4 TIM8_TRIG TIM8_COM	TIM8_CH1	-	TIM8_CH2	-	-	-
DVP	-	-	-	-	-	-	-	DVP

8.5 DMA registers

DMA1 base address: 0x4002_0000;

DMA2 base address: 0x4002_0400.

8.5.1 DMA register overview

Table 8-6 DMA register overview

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
000h	DMA_INTSTS	ERRF8	HTXF8	TXCF8	GLBF8	ERRF7	HTXF7	TXCF7	GLBF7	ERRF6	HTXF6	TXCF6	GLBF6	ERRF5	HTXF5	TXCF5	GLBF5	ERRF4	HTXF4	TXCF4	GLBF4	ERRF3	HTXF3	TXCF3	GLBF3	ERRF2	HTXF2	TXCF2	GLBF2	ERRF1	HTXF1	TXCF1	GLBF1
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
004h	DMA_INTCLR	CERRF8	CHTXF8	CTXCF8	CGLBF8	CERRF7	CHTXF7	CTXCF7	CGLBF7	CERRF6	CHTXF6	CTXCF6	CGLBF6	CERRF5	CHTXF5	CTXCF5	CGLBF5	CERRF4	CHTXF4	CTXCF4	CGLBF4	CERRF3	CHTXF3	CTXCF3	CGLBF3	CERRF2	CHTXF2	CTXCF2	CGLBF2	CERRF1	CHTXF1	CTXCF1	CGLBF1
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
008h	DMA_CHCFG1	Reserved																	MEM2MEM	PRIOLVL[1:0]		MSIZE[1:0]		PSIZE[1:0]		MINC	PINC	CIRC	DIR	ERRIE	HTXIE	TXCIE	CHEN
	Reset Value																		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
00Ch	DMA_TXNUM1	Reserved																NDTX[15:0]															
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
010h	DMA_PADDR1	ADDR[31:0]																															
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
014h	DMA_MADDR1	ADDR[31:0]																															
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
018h	DMA_CHSEL1	Reserved																										CH_SEL[5:0]					
	Reset Value																											0	0	0	0	0	0
01Ch	DMA_CHCFG2	Reserved																	MEM2MEM	PRIOLVL[1:0]		MSIZE[1:0]		PSIZE[1:0]		MINC	PINC	CIRC	DIR	ERRIE	HTXIE	TXCIE	CHEN
	Reset Value																		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
020h	DMA_TXNUM2	Reserved																NDTX[15:0]															
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
024h	DMA_PADDR2	ADDR[31:0]																															

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Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
028h	DMA_MADDR2	ADDR[31:0]																															
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
02Ch	DMA_CHSEL2	Reserved																										CH_SEL[5:0]					
	Reset Value																											0	0	0	0	0	0
030h	DMA_CHCFG3	Reserved																	MEM2MEM	PRIOLVL[1:0]		MSIZE[1:0]		PSIZE[1:0]		MINC	PINC	CIRC	DIR	ERRIE	HTXIE	TXCIE	CHEN
	Reset Value																		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
034h	DMA_TXNUM3	Reserved																NDTX[15:0]															
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
038h	DMA_PADDR3	ADDR[31:0]																															
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
03Ch	DMA_MADDR3	ADDR[31:0]																															
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
040h	DMA_CHSEL3	Reserved																										CH_SEL[5:0]					
	Reset Value																											0	0	0	0	0	0
044h	DMA_CHCFG4	Reserved																	MEM2MEM	PRIOLVL[1:0]		MSIZE[1:0]		PSIZE[1:0]		MINC	PINC	CIRC	DIR	ERRIE	HTXIE	TXCIE	CHEN
	Reset Value																		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
048h	DMA_TXNUM4	Reserved																NDTX[15:0]															
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
04Ch	DMA_PADDR4	ADDR[31:0]																															
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
050h	DMA_MADDR4	ADDR[31:0]																															
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
054h	DMA_CHSEL4	Reserved																										CH_SEL[5:0]					
	Reset Value																											0	0	0	0	0	0
058h	DMA_CHCFG5	Reserved																	MEM2MEM	PRIOLVL[1:0]		MSIZE[1:0]		PSIZE[1:0]		MINC	PINC	CIRC	DIR	ERRIE	HTXIE	TXCIE	CHEN
	Reset Value																		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
05Ch	DMA_TXNUM5	Reserved																NDTX[15:0]															
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
060h	DMA_PADDR5	ADDR[31:0]																															
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
064h	DMA_MADDR5	ADDR[31:0]																															
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
068h	DMA_CHSEL5	Reserved																										CH_SEL[5:0]					
	Reset Value																											0	0	0	0	0	0
06Ch	DMA_CHCFG6	Reserved																	MEM2MEM	PRIOLVL[1:0]		MSIZE[1:0]		PSIZE[1:0]		MINC	PINC	CIRC	DIR	ERRIE	HTXIE	TXCIE	CHEN
	Reset Value																		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
070h	DMA_TXNUM6	Reserved																NDTX[15:0]															
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
074h	DMA_PADDR6	ADDR[31:0]																															
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
078h	DMA_MADDR6	ADDR[31:0]																															
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
07Ch	DMA_CHSEL6	Reserved																										CH_SEL[5:0]					
	Reset Value																											0	0	0	0	0	0
080h	DMA_CHCFG7	Reserved																	MEM2MEM	PRIOLVL[1:0]		MSIZE[1:0]		PSIZE[1:0]		MINC	PINC	CIRC	DIR	ERRIE	HTXIE	TXCIE	CHEN
	Reset Value																		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
084h	DMA_TXNUM7	Reserved																NDTX[15:0]															
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
088h	DMA_PADDR7	ADDR[31:0]																															
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
08Ch	DMA_MADDR7	ADDR[31:0]																															
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
090h	DMA_CHSEL7	Reserved																										CH_SEL[5:0]					
	Reset Value																											0	0	0	0	0	0
094h	DMA_CHCFG8	Reserved																	MEM2MEM	PRIOLVL[1:0]		MSIZE[1:0]		PSIZE[1:0]		MINC	PINC	CIRC	DIR	ERRIE	HTXIE	TXCIE	CHEN

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Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reset Value																		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
098h	DMA_TXNUM8	Reserved																NDTX[15:0]															
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
09Ch	DMA_PADDR8	ADDR[31:0]																															
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0A0h	DMA_MADDR8	ADDR[31:0]																															
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0A4h	DMA_CHSEL8	Reserved																										CH_SEL[5:0]					
	Reset Value																											0	0	0	0	0	0
0A8h	DMA_CHMAPEN	Reserved																															MAP_EN
	Reset Value																																0

8.5.2 DMA Interrupt Status Register (DMA_INTSTS)

Address offset: 0x00

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ERRF8	HTXF8	TXCF8	GLBF8	ERRF7	HTXF7	TXCF7	GLBF7	ERRF6	HTXF6	TXCF6	GLBF6	ERRF5	HTXF5	TXCF5	GLBF5
r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ERRF4	HTXF4	TXCF4	GLBF4	ERRF3	HTXF3	TXCF3	GLBF3	ERRF2	HTXF2	TXCF2	GLBF2	ERRF1	HTXF1	TXCF1	GLBF1
r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r

Bit field	Name	Description
31/27/23/19/15/11/7/3	ERRFx	Transfer error flag for channel x (x=1…8). Hardware sets this bit when transfer error happen. This bit is cleared by software by writing '1' to DMA_INTCLR.CERRFx bit. 0: Transfer error no happened on channel x. 1: Transfer error happened on channel x.
30/26/22/18/14/10/6/2	HTXFx	Half transfer flag for channel x (x=1…8). Hardware sets this bit when half transfer is done. This bit is cleared by software by writing '1' to DMA_INTCLR.CHTXFx bit. 0: Half transfer not yet done on channel x. 1: Half transfer was done on channel x.
29/25/21/17/13/9/5/1	TXCFx	Transfer complete flag for channel x (x=1…8). Hardware sets this bit when transfer is done. This bit is cleared by software by writing '1' to DMA_INTCLR.CTXCFx bit. 0: Transfer not yet done on channel x. 1: Transfer was done on channel x.
28/24/20/16/12/8/4/0	GLBFx	Global flag for channel x (x=1…8). Hardware sets this bit when any interrupt events happen in this channel. This bit is cleared by software by writing '1' to DMA_INTCLR.CGLBFx bit. 0: No transfer error, half transfer or transfer done event happen on channel x. 1: One of transfer error, half transfer or transfer done event happen on channel x.

8.5.3 DMA Interrupt Flag Clear Register (DMA_INTCLR)

Address offset: 0x04

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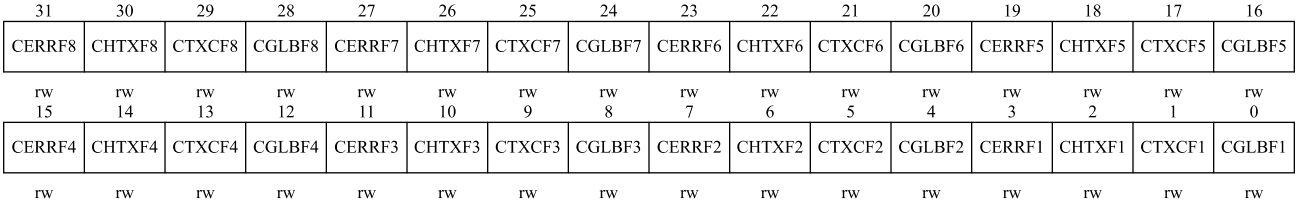
Reset value: 0x0000 0000



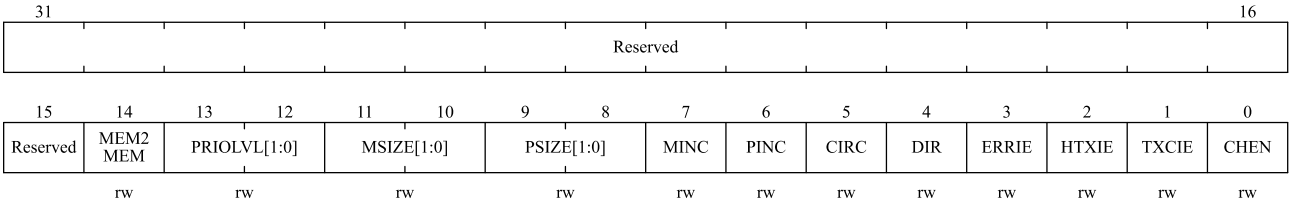
Bit field	Name	Description
31/27/23/19/15/11/7/3	CERRFx	Clear transfer error flag for channel x (x=1…8). Software can set this bit to clear ERRF of corresponding channel. 0: No action. 1: Reset DMA_INTSTS.ERRF bit of corresponding channel.
30/26/22/18/14/10/6/2	CHTXFx	Clear half transfer flag for channel x (x=1…8). Software can set this bit to clear HTXF of corresponding channel. 0: No action. 1: Reset DMA_INTSTS.HTXF bit of corresponding channel.
29/25/21/17/13/9/5/1	CTXCFx	Clear transfer complete flag for channel x (x=1…8). Software can set this bit to clear TXCF of corresponding channel. 0: No action. 1: Reset DMA_INTSTS.TXCF bit of corresponding channel.
28/24/20/16/12/8/4/0	CGLBFx	Clear global event flag for channel x (x=1…8). Software can set this bit to clear GLBF of corresponding channel. 0: No action. 1: Reset DMA_INTSTS.GLBF bit of corresponding channel.

8.5.4 DMA Channel x Configuration Register (DMA_CHCFGx)

The x is channel number, x = 1…8

Address offset: 0x08+20 * (x–1)

Reset value: 0x0000 0000



Bit field	Name	Description
31:15	Reserved	Reserved, the reset value must be maintained.
14	MEM2MEM	Memory to memory mode. Software can configure this channel to memory to memory transfer when it is not yet enabled. 0: Channel transfer between memory and peripheral.

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Bit field	Name	Description
		1: Channel set to memory to memory transfer.
13:12	PRIOLVL[1:0]	Channel priority. Software can program channel priority when channel is not enable. 00: Low 01: Medium 10: High 11: Very high
11:10	MSIZE[1:0]	Memory data size. Software can configure data size read/write from/to memory address. 00: 8-bits 01: 16-bits 10: 32-bits 11: Reserved
9:8	PSIZE[1:0]	Peripheral data size. Software can configure data size read/write from/to peripheral address. 00: 8-bits 01: 16-bits 10: 32-bits 11: Reserved
7	MINC	Memory increment mode. Software can enable/disable memory address increment mode. 0: Memory address won't increase with each transfer. 1: Memory address increase with each transfer.
6	PINC	Peripheral increment mode. Software can enable/disable peripheral address increment mode. 0: Peripheral address won't increase with each transfer. 1: Peripheral address increase with each transfer.
5	CIRC	Circular mode. Software can set/clear this bit. 0: Channel will stop after one round of transfer. 1: Channel configure as circular mode.
4	DIR	Data transfer direction Software can set/clear this bit. 0: Data transfer from Peripheral to Memory 1: Data transfer from Memory to Peripheral.
3	ERRIE	Transfer error interrupt enable. Software can enable/disable transfer error interrupt. 0: Disable transfer error interrupt of channel x. 1: Enable transfer error interrupt of channel x.
2	HTXIE	Half transfer interrupt enable. Software can enable/disable half transfer interrupt. 0: Disable half transfer interrupt of channel x. 1: Enable half transfer interrupt of channel x.

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Bit field	Name	Description
1	TXCIE	Transfer complete interrupt enable. Software can enable/disable transfer complete interrupt. 0: Disable transfer complete interrupt of channel x. 1: Enable transfer complete interrupt of channel x.
0	CHEN	Channel enable. Software can set/reset this bit. 0: Disable channel. 1: Enable channel.

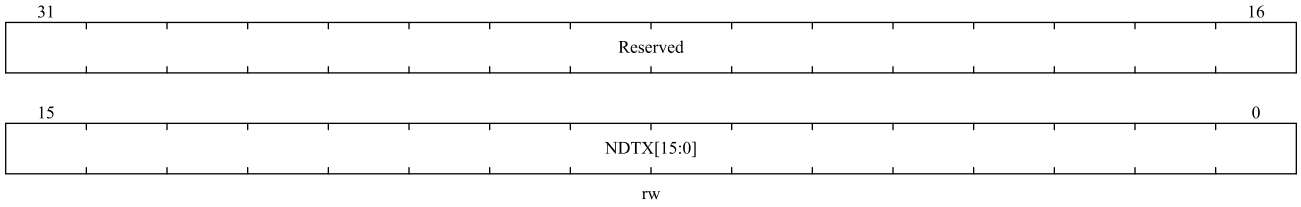
8.5.5 DMA Channel x Transfer Number Register (DMA_TXNUMx)

The x is channel number, x = 1…8

Address offset: 0x0c+20 * (x–1)

Reset value: 0x0000 0000

This register can only be written if the channel is disabled (DMA_CHCFGx.CHEN = 0).



Bit field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained.
15:0	NDTX	Number of data to transfer. Number of data to be transferred (0～65535). Software can read/write the number of transfers when channel is disable and it will be read only after channel enable. Every successful transfer of corresponding DMA channel will decrease this register by 1. If circular mode is enable, it will automatically reload pre-set value when it reach zero. Otherwise it will keep at zero and reset channel enable.

8.5.6 DMA Channel x Peripheral Address Register (DMA_PADDRx)

The x is channel number, x = 1…8

Address offset: 0x10+20 * (x–1)

Reset value: 0x0000 0000

This register can only be written if the channel is disabled (DMA_CHCFGx.CHEN = 0).

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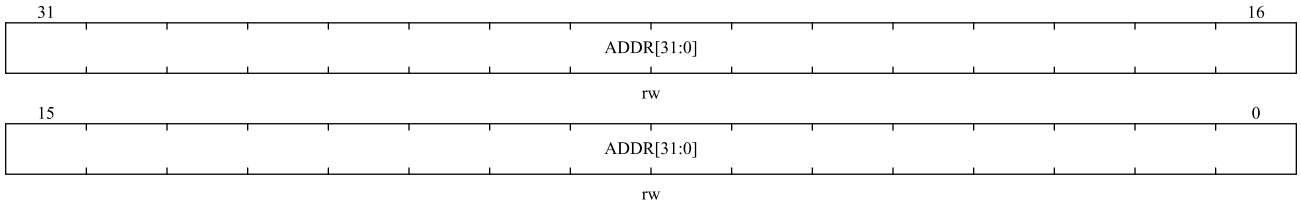


Bit field	Name	Description
31:0	ADDR	Peripheral address. Peripheral starting address for DMA to read/write from/to. Increment of address will be decided by DMA_CHCFGx.PSIZE. With DMA_CHCFGx.PSIZE equal to 01, DMA ignores bit 0 of PADDR and if DMA_CHCFGx.PSIZE equal to 10 DMA will ignore bit [1:0] of PADDR.

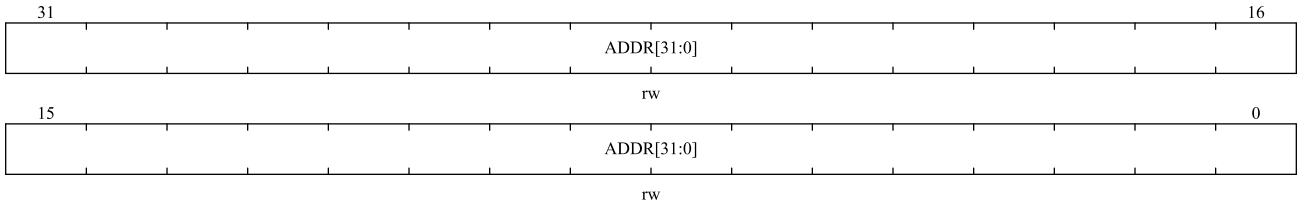
8.5.7 DMA Channel x Memory Address Register (DMA_MADDRx)

The x is channel number, x = 1…8

Address offset: 0x14+20 * (x–1)

Reset value: 0x0000 0000

This register can only be written if the channel is disabled (DMA_CHCFGx.CHEN = 0).



Bit field	Name	Description
31:0	ADDR	ADDR Memory address. Memory starting address for DMA to read/write from/to. Increment of address will be decided by DMA_CHCFGx.MSIZE. With DMA_CHCFGx.MSIZE equal to 01, DMA ignores bit 0 of MADDR and if DMA_CHCFGx.MSIZE equal to 10 DMA will ignore bit [1:0] of MADDR.

8.5.8 DMA1 Channel x Request Select Register (DMA1_CHSELx)

The x is channel number, x = 1…8

Address offset: 0x18+20 * (x–1)

Reset value: 0x0000 0000

Writing to this register is only valid when the channel MAP is enabled (DMA_CHMAPEN.MAP_EN=1). This register is used to manage the DMA1 channel mapped by the DMA1 peripheral request.

Note: After the channel MAP is enabled, DMA channel selection register will change to the default value. It is necessary to configure the corresponding mapping for each channel that has been used. If it is not reconfigured, all

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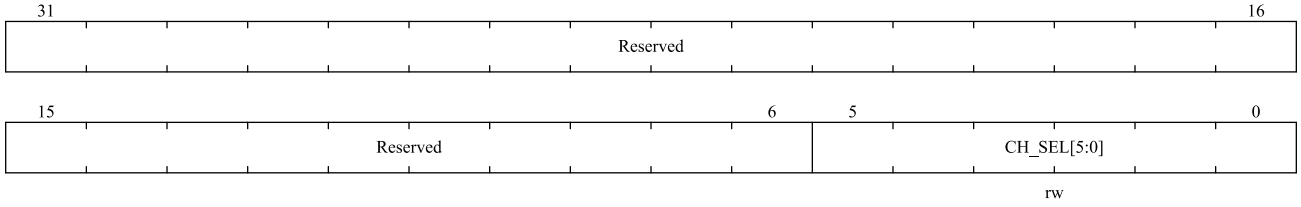
channels of DMA1 will only respond to the DMA request of ADC1.



Bit field	Name	Description
31:6	Reserved	Reserved, the reset value must be maintained.
5:0	CH_SEL[5:0]	DMA1 channel request selection 40：UART5_RX 39：ADC2 38：I2C1_RX 37：TIM4_UP 36：TIM2_CH4 35：TIM2_CH2 34：USART2_TX 33：I2C1_TX 32：TIM3_TRIG 31：TIM3_CH1 30：TIM1_CH3 29：USART2_RX 28：I2C2_RX 27：TIM4_CH3 26：TIM2_CH1 25：SPI2/I2S2_TX 24：TIM1_UP 23：USART1_RX 22：I2C2_TX 21：SPI2/I2S2_RX 20：TIM4_CH2 19：TIM1_COM 18：TIM1_TRIG 17：TIM1_CH4 16：USART1_TX 15：SPI1_TX 14：TIM3_UP 13：TIM3_CH4 12：TIM1_CH2 11：USART3_RX 10：SPI1_RX 9：TIM3_CH3 8：TIM2_UP

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Bit field	Name	Description
		7：TIM1_CH1 6：I2C3_RX 5：USART3_TX 4：TIM4_CH1 3：TIM2_CH3 2：I2C3_TX 1：UART5_TX 0：ADC1

8.5.9 DMA2 Channel x Request Select Register (DMA2_CHSELx)

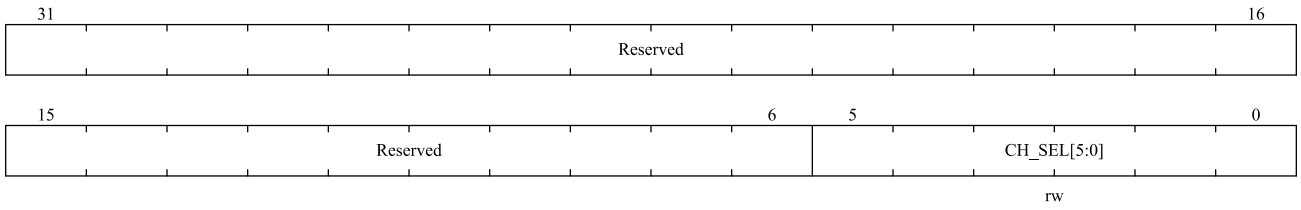
The x is channel number, x = 1…8

Address offset: 0x18+20 * (x–1)

Reset value: 0x0000 0000

Writing to this register is only valid when the channel MAP is enabled (DMA_CHMAPEN.MAP_EN=1). This register is used to manage the DMA2 channel mapped by the DMA2 peripheral request.

Note: After the channel MAP is enabled, DMA channel selection register will change to the default value. It is necessary to configure the corresponding mapping for each channel that has been used. If it is not reconfigured, all channels of DMA2 will only respond to the DMA request of TIM5_CH4.



Bit field	Name	Description
31:6	Reserved	Reserved, the reset value must be maintained.
5:0	CH_SEL[5:0]	DMA2 channel request selection 32：DVP 31：ADC4 30：UART7_TX 29：I2C4_RX 28：QSPI_TX 27：UART7_RX 26：I2C4_TX 25：QSPI_RX 24：UART4_TX 23：TIM5_CH1 22：TIM8_CH2 21：ADC3 20：DAC2

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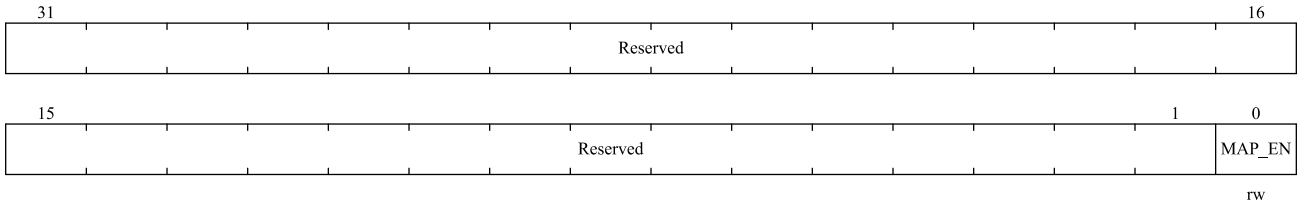
Bit field	Name	Description
		19：TIM7_UP 18：SDIO 17：TIM5_CH2 16：DAC1 15：TIM6_UP 14：UART4_RX 13：TIM8_CH1 12：UART6_TX 11：SPI3/I2S3_TX 10：TIM5_UP 9：TIM5_CH3 8：TIM8_COM 7：TIM8_TRIG 6：TIM8_CH4 5：UART6_RX 4：SPI3/I2S3_RX 3：TIM8_UP 2：TIM8_CH3 1：TIM5_TRIG 0：TIM5_CH4

8.5.10 DMA Channel MAP Enable Register (DMA_CHMAPEN)

Address offset: 0xA8

Reset value: 0x0000 0000

Note: After the MAP is enabled, DMA will respond to the DMA request according to the configuration of the selection register. It is necessary to configure the channel request selection of the peripheral. If it is not configured, DMA will only respond to the default value of the channel selection register (DMA1 is ADC1, DMA2 is TIM5_CH4).



Bit field	Name	Description
31:1	Reserved	Reserved, the reset value must be maintained.
0	MAP_EN	Channel MAP enable. 0: Disable channel MAP 1: Enable channel MAP

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9 Analog to Digital Conversion (ADC)

9.1 Introduction

The 12-bit ADC is a high-speed analog-to-digital converter using successive approximation. It has multiple channels. The A/D conversion of each channel has four execution modes: single, continuous, scan or discontinuous. ADC measurements are stored (left-aligned/ right-aligned) in 16-bit data registers. The application can detect that the input voltage is within user-defined high/low thresholds by analog watchdog and the maximum frequency of the input clock to the ADC is 80MHz.

9.2 Main Features

- Supports 4 ADC, supports single-ended and differential inputs, and can measure up to 40 external and 7 internal sources.
- ADC1 supports 11 external channels, ADC2 supports 13 external channels, ADC3 supports 15 external channels, and ADC4 supports 13 external channels.
- Support 12-bit, 10-bit, 8-bit, 6-bit resolution configurable.
  - The highest sampling rate 4.7MSPS under 12bit resolution.
  - The highest sampling rate 6.1MSPS under 10bit resolution.
  - The highest sampling rate 7.3MSPS under 8bit resolution.
  - The highest sampling rate 8.9MSPS under 6bit resolution.
- ADC clock source is divided into working clock source, sampling clock source and timing clock source
  - Only AHB_CLK can be configured as the working clock source,up to 144MHz.
  - PLL can be configured as a sampling clock source, up to 80MHz, support frequency division 1,2,4,6,8,10,12,16,32,64,128,256.
  - The AHB_CLK can be configured as the sampling clock source, up to 80MHz, and supports frequency division 1,2,4,6,8,10,12,16,32.
  - The timing clock is used for internal timing functions and the frequency must be configured to 1MHz.
- Support trigger sampling, Including EXTI/TIMER.
- Programmable channel sampling interval.
- Support auto scan mode.
- Support 2 conversion modes.
  - Single conversion.
  - Continuous conversion.
- Support discontinuous mode.
- Support self-calibration.

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- Support DMA.
- Interrupt generation.
  - At the end of conversion.
  - At the end of injection conversion.
  - Analog watchdog event.
- Data alignment with embedded data consistency.
- Both regular conversions and injection conversions have external triggering options.
- ADC power requirements: 1.8V to 3. 6V.
- ADC input voltage range: $V_{REF-} \leq V_{IN} \leq V_{REF+}$.
- Dual ADC mode, ADC1 and ADC2 combined, ADC3 and ADC4 combined.

9.3 Function Description

The block diagram and pin description of the ADC are as follows:

Figure 9-1 Block diagram of a single ADC

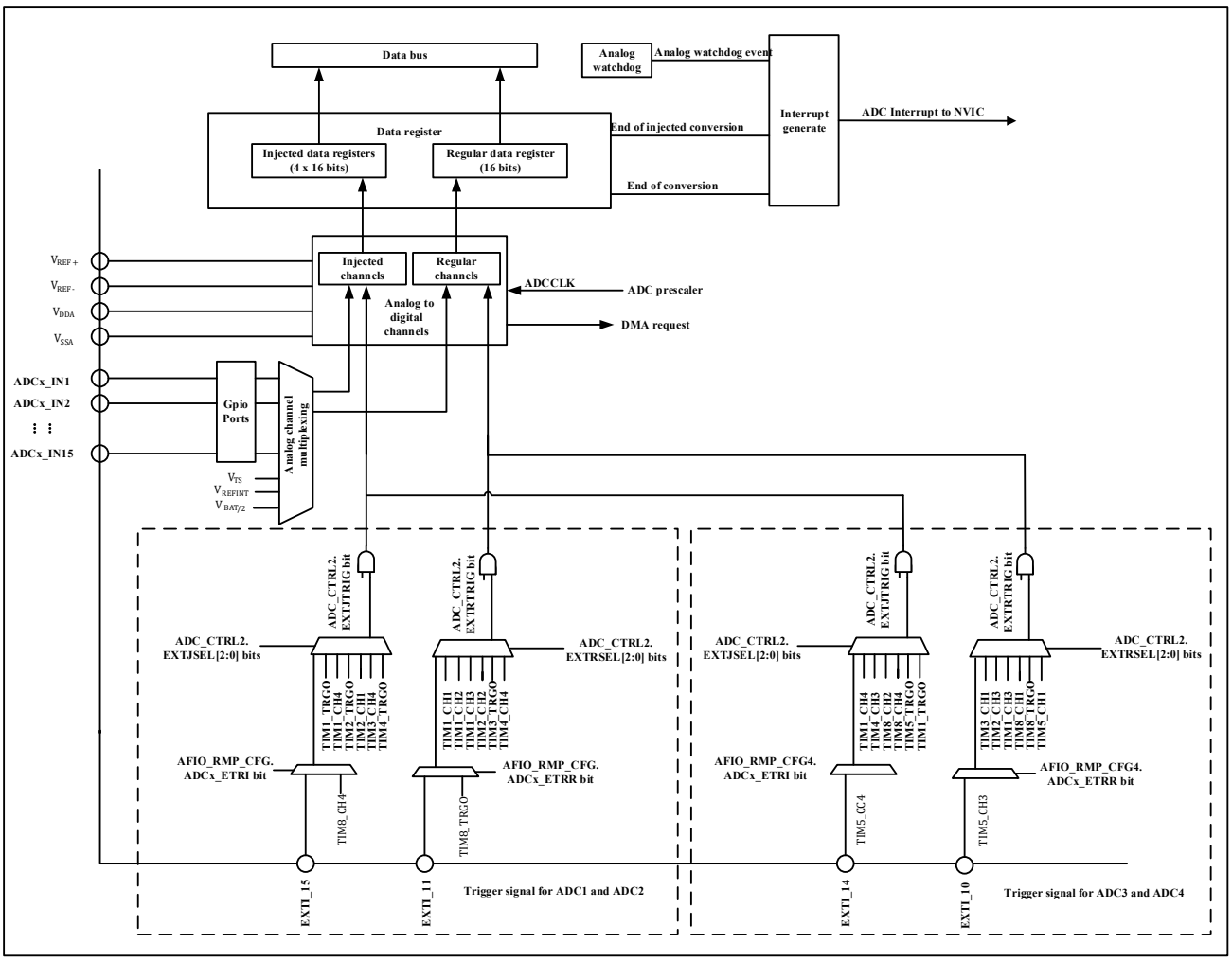

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Table 9-1 ADC pins

Name	Types	Description
V_{DDA}	Input, analog power supply	Equivalent to V_{DD} analog power supply and: 1.8V ≤ V_{DDA} ≤ V_{DD}(3.6V)
V_{SSA}	Input, analog power supply ground	Equivalent to V_{SS} analog power supply ground
V_{REF+}	Input, analog reference positive	Positive reference voltage used by ADC, 1.8V ≤ V_{REF+} ≤ V_{DDA}
V_{REF-}	Input, analog reference negative	The low/negative reference voltage used by the ADC, V_{REF-} = V_{SSA}
ADCx_IN	Analog input signal	Analog external input channels

Notes:

1. V_{DDA} and V_{SSA}. They should be separately connected to V_{DD} and V_{SS}.

2. If there is a V_{REF}- Pins (depending on the package), it must be connected to VSSA.

3. If there are no VREF+ pins (depending on the package), try to ensure that the voltage values of VDDA and VDD are the same, otherwise the ADC accuracy will be affected.

4. External channel reference data sheet.

9.3.1 ADC Clock

An ADC requires three clocks, HCLK, ADC_CLK and ADC_1MCLK.

- HCLK is used for the register access.
- ADC_CLK is the working clock of ADC. ADC_CLK has two sources (HCLK divider or PLL divider). HCLK divider and system are synchronous clock, while PLL divider and system are asynchronous clock. The advantage of using a synchronous clock is that there is no uncertainty when triggering the ADC to respond to the trigger.The advantage of using PLL's divider clock is that the ADC's working clock can be handled independently without affecting other modules attached to the HCLK
- ADC_1MCLK for internal timing function, configured in RCC, frequency size must be configured to 1MHz

Notes:

1. Configuration PLL as a clock source, up to 72 MHz, support frequency division 1,2,4,6,8,10,12,16,32, 64,128,256

2. The AHB_CLK frequency division can be configured as a working clock up to 72MHz. The AHB_CLK frequency division can be 1,2,4,6,8,10,12,16,32

3. When switching the ADC_1M clock source, you need to ensure that the HSI clock is turned on

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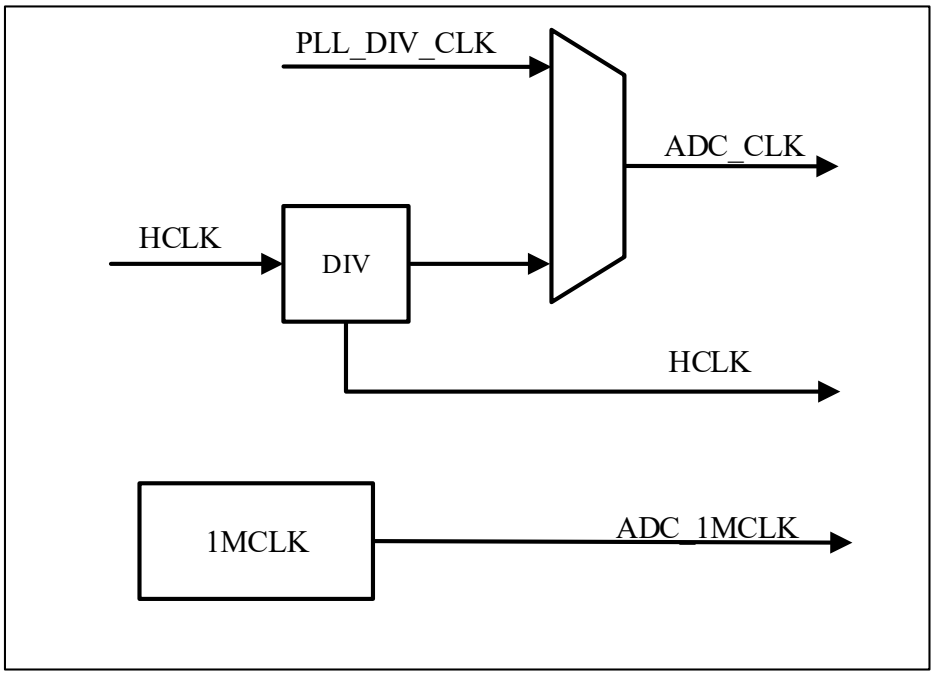
Figure 9-2 ADC clock



9.3.2 ADC Switch Control

You can proceed to the next step only after the power-up process is complete. You can check if the power-up is complete by polling the ADC_CTRL3.RDY bit.

You can set the ADC_CTRL2.ON bit to turn on the ADC. When the ADC_CTRL2.ON bit is set for the first time, it wakes up the ADC from the power-off state. After a power-on delay of ADC (t_{STAB}), and the conversion begins when the ADC_CTRL2.ON bit is set again.

The conversion can be stopped by clearing the ADC_CTRL2.ONbit and placing the ADC in power-off mode. In this mode, the ADC consumes almost no power (just a few μA). Power-down can be checked by polling the ADC_CTRL3.PDRDY bit.

When the ADC is disabled, the default mode is power-down. In this mode, as long as the power is on, there is no need to re-calibrate, and the calibration value is automatically maintained in the ADC. To further reduce power consumption, the ADC has a deep sleep mode. When ADC Disable is in deep sleep mode, the calibration value inside the ADC is lost and needs to be recalibrated. Deep sleep saves about 0.2μA of power consumption.

Note: That when in dual ADC mode, it is best to select the same sleep mode for both ADCs. Register ADC_CTRL3.DPWMOD which controls ADC deep sleep mode.

9.3.3 Channel Selection

Each channel can be configured as a regular sequence and an injection sequence.

Injection sequence consists of multiple conversions, up to a maximum of 4. The ADC_JSEQ register specifies the injection channel and the conversion order of the injection channel. The ADC_JSEQ.JLEN[1:0] bits specified injection sequence length.

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Regular sequence consists of multiple conversions, up to a maximum of 16. The ADC_RSEQx registers specify the regular channels and the conversion order of the regular channels. The ADC_RSEQ1.LEN[3:0] bits specified regular channel sequence length.

Note: During conversion, changes to the ADC_RSEQx or ADC_JSEQ registers are prohibited; the ADC_RSEQx or ADC_JSEQ registers can only be changed when the ADC is idle.

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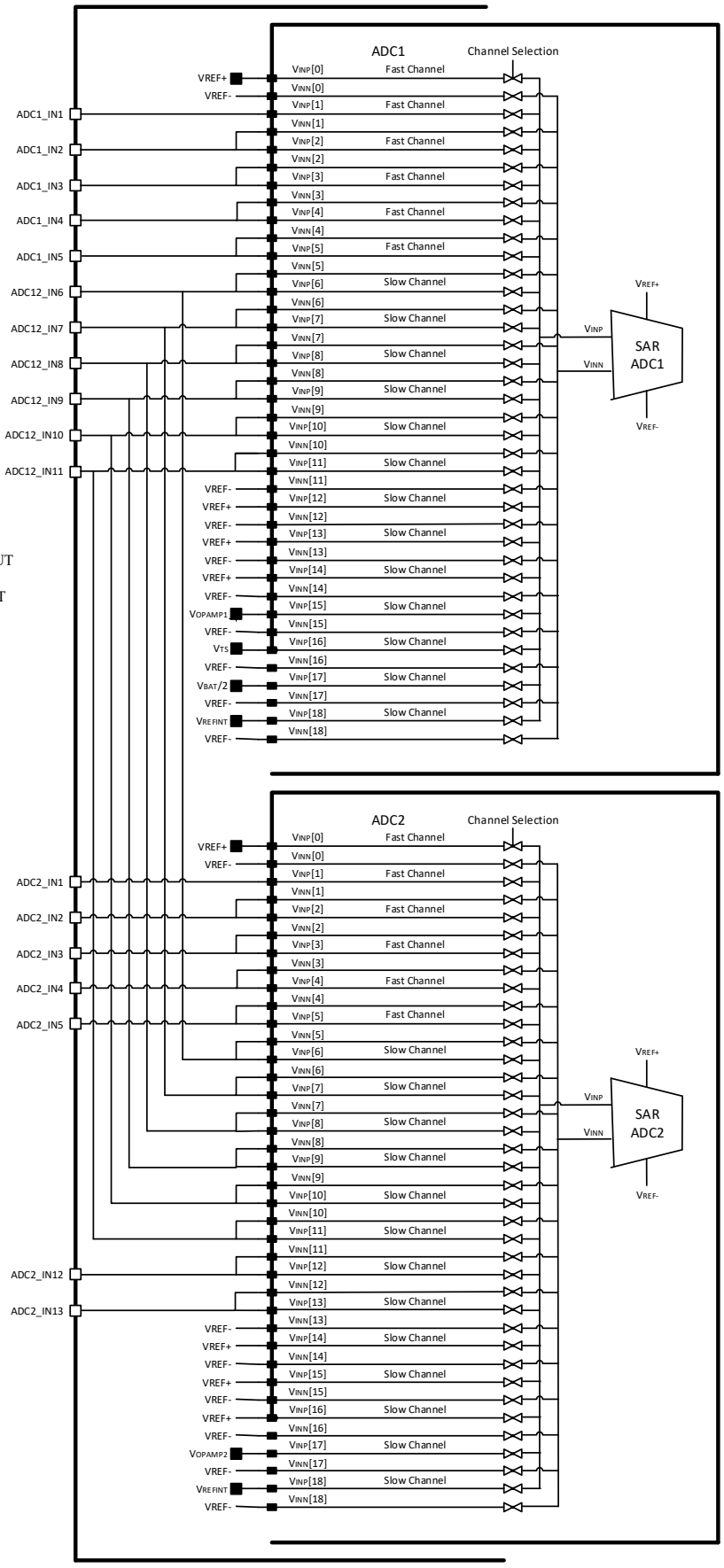
Figure 9-3 ADC1 and ADC2 channel pin connections



ADC1_IN3 is internally connected to OPAMP1_OUT
ADC2_IN3 is internally connected toOPAMP2_OUT

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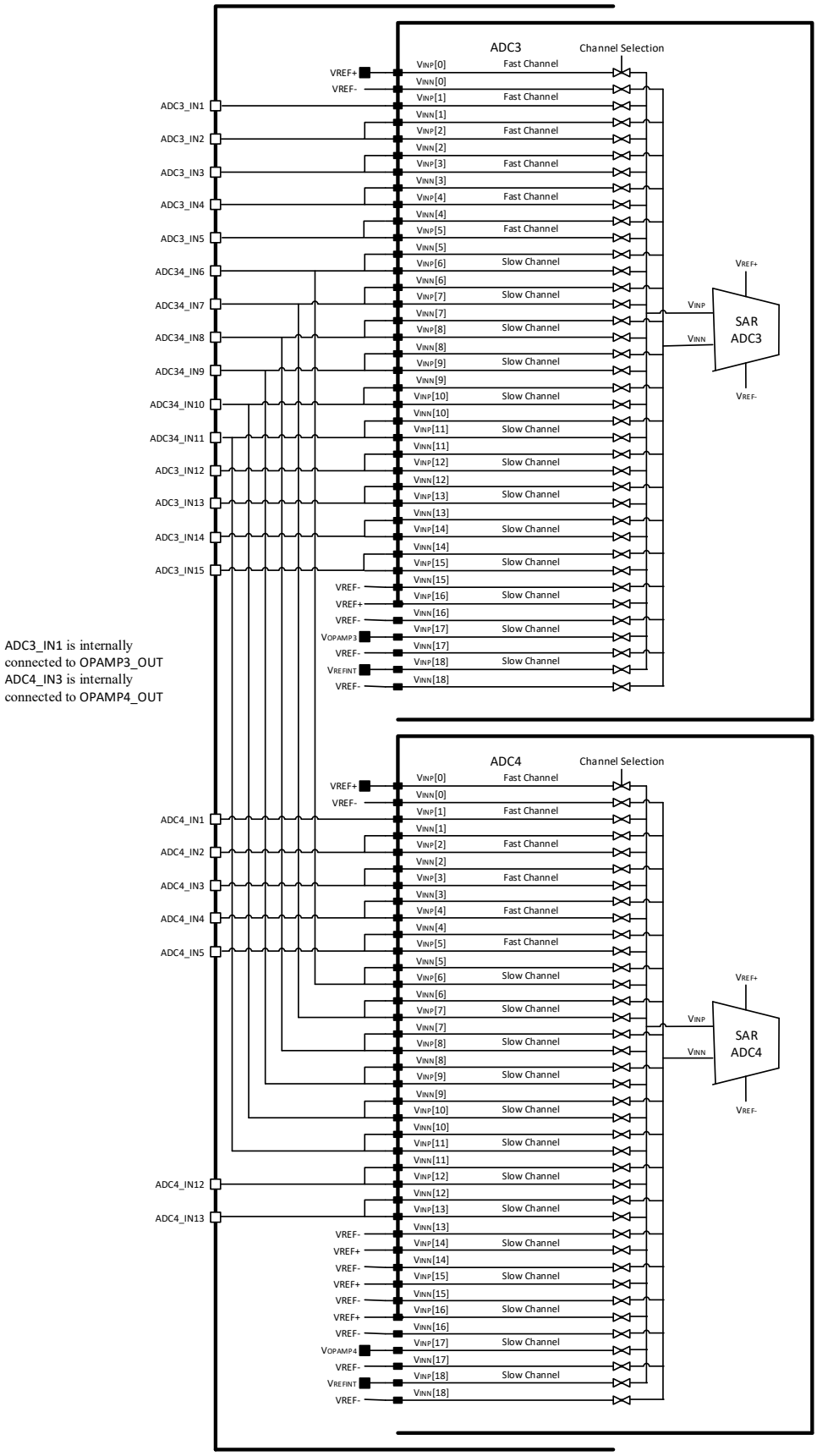
Figure 9-4 ADC3 and ADC4 channel pin connections



ADC3_IN1 is internally connected to OPAMP3_OUT
ADC4_IN3 is internally connected to OPAMP4_OUT

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9.3.4 Internal Channel

- The temperature sensor is connected to channel ADC1_IN16.
- $V_{BAT/2}$ is connected to channel ADC1_IN17.
- Internal reference voltage VREFINT is connected to ADCx_IN18.
- V_{OP1OUT} output is connected to channel ADC1_IN3.
- V_{OP2OUT} output is connected to channel ADC2_IN3.
- V_{OP3OUT} output is connected to channel ADC3_IN1.
- V_{OP4OUT} output is connected to channel ADC4_IN3.

Internal channels can be converted by injection or regular channels.

Note: The temperature sensor, $V_{BAT/2}$ can only be used in the ADC1.

9.3.5 Single Conversion Mode

The ADC can enter the single conversion mode by configuring ADC_CTRL2.CTU to 0. In this mode, external triggering(for regular channels or injection channels) or setting ADC_CTRL2.ON=1(for regular channels only) can start the ADC to start conversion, and the ADC only performs one conversion.

After the conversion starts, when an injection channel conversion is completed, the injection channel conversion end flag(ADC_STS.JENDC) will be set to 1. If the injection channel conversion end interrupt enable (ADC_CTRL1.JENDCIEN) bit is set to 1, an interrupt will be generated at this time, and the converted data will be stored in the ADC_JDATx register.

After the conversion starts, when a regular channel conversion is completed, the regular channel conversion end flag(ADC_STS.ENDC) will be set to 1. If the regular channel conversion end interrupt enable (ADC_CTRL1.ENDCIEN) bit is set to 1, an interrupt will be generated at this time, and the converted data will be stored in the ADC_DAT register.

After single conversion, the ADC stops.

9.3.6 Continuous Conversion Mode

The ADC can enter the continuous conversion mode by configuring ADC_CTRL2.CTU to 1. In this mode, external triggering or setting ADC_CTRL2.ON to 1 can start the ADC to start conversion, and the ADC will continuously convert the selected channel. Continuous mode is only valid for regular channels, not for injection channels.

After the conversion starts, when a regular channel conversion is completed, the regular channel end of conversion flag bit (ADC_STS.ENDC) will be set to 1. If the regular channel conversion end interrupt enable bit (ADC_CTRL1.ENDCIEN) is set to 1 at this time, an interrupt will be generated . The converted data will be stored in the ADC_DAT register.

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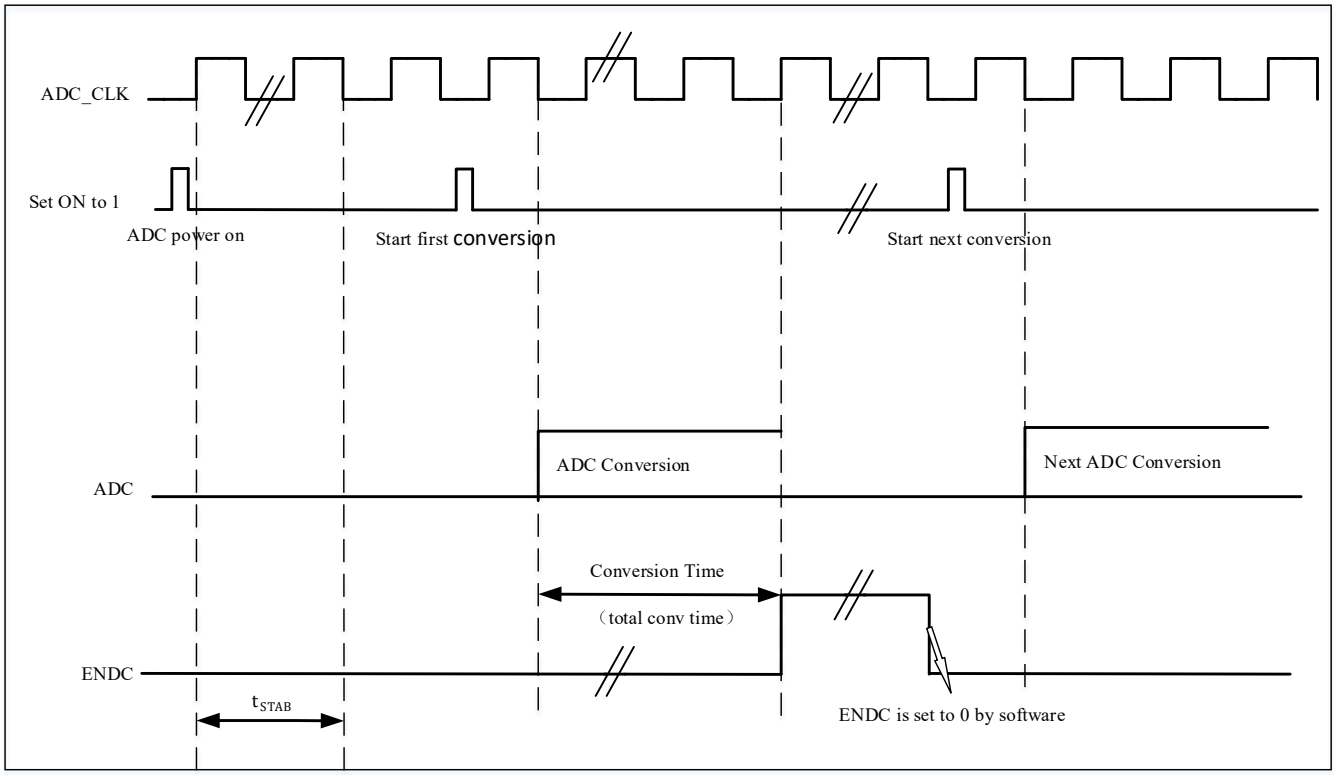
9.3.7 Timing Diagram

When ADC_CTRL2.ON is set to 1 for the first time, the ADC is powered on. After the ADC is powered on, the ADC needs a certain time(t_{STAB}) to ensure its stability. After the ADC is stable, write 1 to ADC_CTRL2.ON again, the ADC starts to convert, and the conversion end flag will be set to 1 after the conversion is completed.

Figure 9-5 Timing diagram



9.3.8 Analog Watchdog

The analog watchdog can be enabled on the regular channel by setting ADC_CTRL1.AWDGERCH to 1, or the analog watchdog on the injection channel can be enabled by setting ADC_CTRL1.AWDGEJCH to 1. The high threshold of the analog watchdog can be set by configuring ADC_WDGHIGH.HTH, and the low threshold of the analog watchdog can be set by configuring ADC_WDGLOW.LTH. The threshold of the analog watchdog has nothing to do with the way of data alignment, because the comparison of the ADC's conversion value with the threshold is done before the alignment . When the value of ADC analog conversion is higher than the high threshold of the analog watchdog or lower than the low threshold of the analog watchdog, the analog watchdog flag (ADC_STS.AWDG) will be set to 1, if ADC_CTRL1.AWDGIEN has been configured to 1, an interrupt will be generated at this time. The analog watchdog can be controlled for one or more channels by configuring ADC_CTRL1.AWDGSGLEN and ADC_CTRL1.AWDGCH[4:0].

Table 9-2 Analog watchdog channel selection

Channel	ADC_CTRL1 register control bit		
	AWDGSGLEN	AWDGERCH	AWDGEJCH
There is none	Any value	0	0

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All injection channels	0	0	1
All regular channels	0	1	0
All injection and regular channels	0	1	1
A single injection channel	1	0	1
A single regulars of the channel	1	1	0
A single injection or regular channels	1	1	1

9.3.9 Scanning Mode

By configuring ADC_CTRL1.SCAMD to 1, the scan conversion mode can be turned on, and by configuring the four registers ADC_RSEQ1, ADC_RSEQ2, ADC_RSEQ3, ADC_JSEQ, the conversion sequence can be selected, and the ADC will scan and convert all the regular or Injected channels. After the conversion is started, the channels will be converted one by one. If ADC_CTRL2.CTU is 1 at this time, the conversion will be restarted from the first channel of the conversion sequence after the conversion of all regular channels is completed. Injected channel does not support continuous mode. The DMA function can be turned on by setting ADC_CTRL2.ENDMA to 1, and the DMA will transfer the data to the SRAM after the regular channel conversion is completed.

Note: In dual ADC mode, the DMA function on the regular channel of ADC2 needs to be completed by the DMA of ADC1, and the DMA function on the regular channel of ADC4 needs to be completed by the DMA of ADC3.

9.3.10 Injection Channel Management

9.3.10.1 Automatic injection

If ADC_CTRL1.AUTOJC bit is set, then the Injected channels are automatically converted following the regular channels mentioned by ADC_RSEQ and ADC_JSEQx. A single trigger can conver up to 16+ 4 channels. Setting ADC_CTRL2.CTU the conversion sequence will be converted continuously.

When this function is turned on, the external trigger of the injection channel needs to be turned off.

This function cannot be used with the discontinuous mode at the same time.

When the ADC clock prescale factor is 2, there is a delay of two ADC clock intervals when the conversion sequence changes from regular to injection or injection to regular. When the ADC clock prescale factor is 4 to 8, there is a delay of one ADC clock intervals when the conversion sequence changes from regular to injection or injection to regular.

9.3.10.2 Trigger injection

Set ADC_CTRL1.AUTOJC to 0 and ADC_CTRL1.SCAMD to 1 to enable the trigger injection function. In this function, the regular channel of continuous conversion is triggered by setting ADC_CTRL2.ON or by external trigger.When the regular channel is converted, if an external injection trigger is generated, the current conversion will be suspended, and the injection sequence channel will start conversion. When the injection sequence channel conversion is completed, the interrupted conversion of regular sequence channel will be resumed. If a regular event is generated during the injection conversion, the regular sequence channel will start conversion after the injection sequence channel conversion is completed.

When using this function, the time interval between the injection channel triggers needs to be greater than the time required for the injection sequence to complete the conversion.

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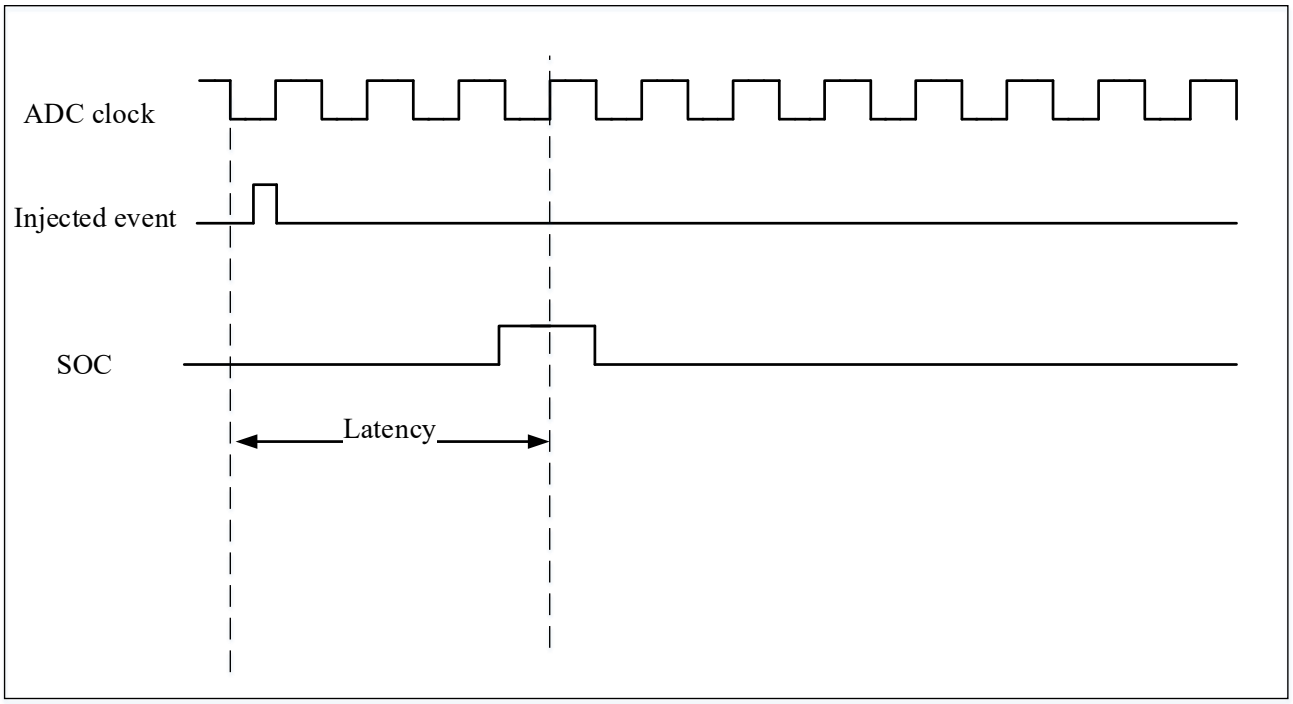
Figure 9-6 Injection conversion delay



Note:For the maximum delay value, please refer to the electrical characteristics section in the data manual.

9.3.11 Discontinuous Mode

9.3.11.1 Regular channels

Configure ADC_CTRL1.DREGCH to 1 to enable the discontinuous mode on the regular channel, obtain the regular sequence by configuring ADC_RSEQ1, ADC_RSEQ2, ADC_RSEQ3, and configure ADC_CTRL1.DCTU[2:0] to control the conversion of n channels each time a trigger signal is generated.

When the trigger signal is generated, it will convert n channels of the regular sequence and then stop, until the next trigger signal is generated. Next trigger will continue to convert n channels from the point where the previous conversion stopped, until all channels of the regular sequence are converted (If the last trigger occurs and the remaining channels in the conversion sequence are less than n, only the remaining channels will be converted and the conversion will be stopped), and the end of conversion flag bit will also be set to 1. When the conversion of all channels in the conversion sequence is completed, when the next trigger signal occurs ,the conversion starts from the first channel of the regular sequence again.

9.3.11.2 Injection channels

Configure ADC_CTRL1.DJCH to 1 to enable the discontinuous mode on the injection channel, obtain the injection sequence by configuring ADC_JSEQ.

When the trigger signal is generated, it will convert 1 channel of the injection sequence and then stop. Until the next trigger signal is generated. Next trigger will continue to convert 1 channel from the point where the previous conversion stopped until all channels of the injection sequence are converted, and the end of conversion flag bit will also be set to 1. When the conversion of all channels in the conversion sequence is completed, when the next trigger signal occurs ,the conversion starts from the first channel of the injection sequence again.

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Only one of injection conversion and regular conversion can be set to discontinuous mode at the same time, and the automatic injection function and discontinuous mode cannot be set at the same time.

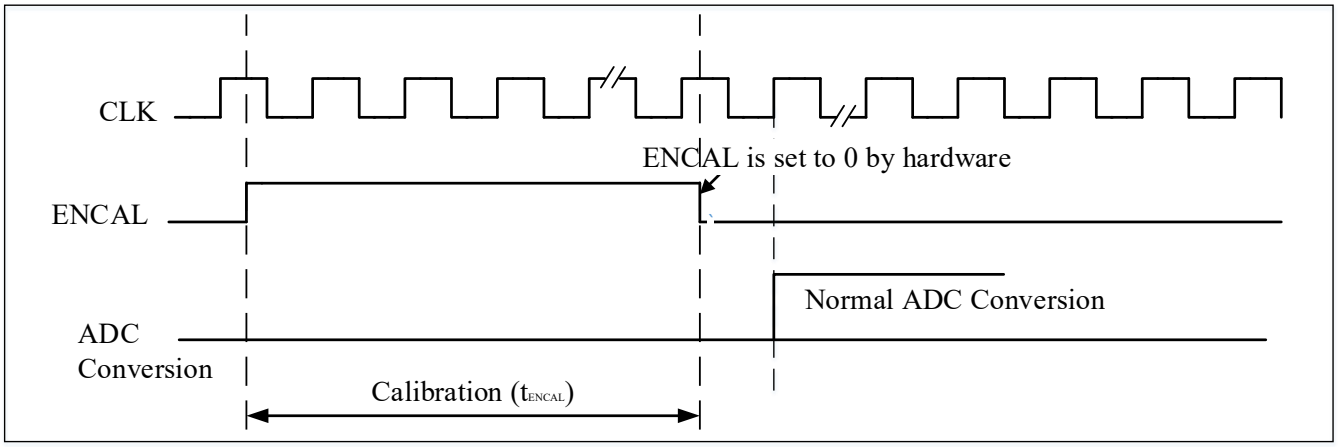
9.4 Calibration

In order to reduce the error, the ADC will have a built-in self-calibration mechanism. Before the A/D conversion, this self-calibration mechanism is used to calculate a calibration factor on each capacitor. Errors due to changes in the internal capacitor bank during conversion are eliminated by this calibration factor. The application program sets the ADC_CTRL2.ENCAL bit to 1 to start self-calibration. During the calibration, the ADC_CTRL2.ENCAL bit remains 1. After the calibration, the ADC_CTRL2.ENCAL bit is cleared by hardware, and then the A/D conversion starts.

Notes:

1. *It is recommended to perform a calibration after each power-on. If the ADC has been converted and is in continuous conversion mode, the calibration operation cannot be completed..*
2. *The default is single-end calibration, and for differential automatic calibration, you must set ADC_CTRL3.CALDIF to 1. Then write 1 to ADC_CTRL2.ENCAL bit and wait for calibrationto complete (ADC_CTRL2.ENCAL bit will clear 0 automatically after calibration).*

Figure 9-7 Calibration sequence diagram



9.5 Data Aligned

There are two alignment methods for data storage after conversion: left-aligned and right-aligned. The alignment can be set by the ADC_CTRL2.ALIG bit. ADC_CTRL2.ALIG = 0 is right-aligned, as shown in **Table 9-3**, ADC_CTRL2.ALIG = 1 is left-aligned, as shown in **Table 9-4**.

For injection sequence , the SYM bit is the extended sign value, and the data stored in the register is the conversion result minus the user-defined offset in the ADC_JOFFSETx register, so the result can be a negative value; for regular sequence , there is no need to subtract offset value.

Table 9-3 Right-align data

The Injection sequence

(12bit resolution)

SYM	SYM	SYM	SYM	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

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The regular sequence

(12bit resolution)

0	0	0	0	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Table 9-4 Left-aligne data

Injection sequence

(12bit resolution)

SYM	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	0	0	0

The regular sequence

(12bit resolution)

D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	0	0	0	0

Note: When the conversion digits are 10, 8, and 6, refer to the alignment with 12 conversion digits

9.6 Programmable Channel Sampling Time

Specify the number of sampling cycles of ADC in ADC_SAMPTx.SAMPx[2:0], and then the ADC samples the input voltage in the specified sampling cycle. For different channels, you can select different sampling time. The total conversion time is calculated as follows:

$$T_{CONV} = \text{Sampling time} + 12.5 \text{ cycles}$$

Example:

ADCCLK=72MHz, the sampling time is 1. 5 cycles and resolution is 12bit, the total conversion time is "1.5 + 12.5" ADCCLK cycles, that is:

$$T_{CONV} = 1.5 + 12.5 = 14 \text{ cycle} = 0.1944\mu s$$

9.7 Externally Triggered Conversion

For the regular sequence , software sets the ADC_CTRL2.EXTRTRIG bit to 1, then the regular channel can use the rising edge of the external event to trigger the start conversion, and then the software sets the ADC_CTRL2.EXTRSEL[2:0] bits to select the external trigger source of the regular sequence. The external trigger source selection is shown in the table below. If you select EXTI line 11 or TIM8_TRGO as the external trigger source, you can set the AFIO_RMP_CFG.ADC1_ETRR or AFIO_RMP_CFG.ADC2_ETRR bit to implement; If you select EXTI line 10 or TIM5_CC3 as the external trigger source, you can set the AFIO_RMP_CFG4.ADC3_ETRR or AFIO_RMP_CFG4.ADC4_ETRR bit to implement; if you select SWSTRRCH as the external trigger source, you can start the regular channel conversion by setting ADC_CTRL2.SWSTRRCH to 1.

Table 9-5 External trigger for regular channels of ADC1 and ADC2

EXTRSEL[2:0]	Trigger source	Type
000	TIM1_CC1 event	Internal signal from the on-chip timer
001	TIM1_CC2 event	

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EXTRSEL[2:0]	Trigger source	Type
010	TIM1_CC3 event	
011	TIM2_CC2 event	
100	TIM3_TRGO event	
101	TIM4_CC4 event	
110	EXTI line11/TIM8_TRGO event	External pin/internal signal from on-chip timer
111	SWSTRRCH	Software control bit

Table 9-6 External trigger for regular channels of ADC3 and ADC4

EXTRSEL [2:0]	Trigger source	Type
000	TIM3_CC1 event	Internal signal from the on-chip timer
001	TIM2_CC3 event	
010	TIM1_CC3 event	
011	TIM8_CC1 event	
100	TIM8_TRGO event	
101	TIM5_CC1 event	
110	EXTI line10/TIM5_CC3 event	
111	SWSTRRCH	Software control bit

For the injection sequence , the software sets the ADC_CTRL2.EXTJTRIG bit to 1, then the injection channel can use the rising edge of the external event to trigger the start conversion, and the software sets the ADC_CTRL2.EXTJSEL[2:0] bits to select the external trigger source of the injection sequence. The external trigger source selection is shown in the table below. If you select EXTI line 15 or TIM8_CC4 as the external trigger source, you can set the AFIO_RMP_CFG.ADC1_ETRI or AFIO_RMP_CFG.ADC2_ETRI bit to implement; If you select EXTI line 14 or TIM5_CC4 as the external trigger source, you can set the AFIO_RMP_CFG4.ADC3_ETRI or AFIO_RMP_CFG4.ADC4_ETRI bit to implement; if you select SWSTRJCH as the external trigger source, you can start the injection channel conversion by setting ADC_CTRL2.SWSTRJCH to 1.

Table 9-7 External trigger for injection channel of ADC1 and ADC2

EXTJSEL[2:0]	Trigger source	Type
000	TIM1_TRGO event	Internal signal from the on-chip timer
001	TIM1_CC4 event	
010	TIM2_TRGO event	
011	TIM2_CC1 event	
100	TIM3_CC4 event	
101	TIM4_TRGO event	
110	EXTI line15/TIM8_CC4 event	External pin/internal signal from on-chip timer
111	SWSTRJCH	Software control bit

Table 9-8 External trigger for injection channel of ADC3 and ADC4

EXTJSEL[2:0]	Trigger source	Type
000	TIM1_TRGO event	Internal signal from the on-chip timer
001	TIM1_CC4 event	
010	TIM4_CC3 event	

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EXTJSEL[2:0]	Trigger source	Type
011	TIM8_CC2 event	
100	TIM8_CC4 event	
101	TIM5_TRGO event	
110	EXTI line14/TIM5_CC4 event	
111	SWSTRJCH	Software control bit

Note: Injection triggers can interrupt conversion of the regular sequence.

9.8 DMA Requests

In order to avoid the loss of the regular channel conversion result saved in the ADC_DAT register due to excessive data when multiple regular channels are converted, the ADC_CTRL2.ENDMA bit can be set to 1 to use DMA. When the ADC regular channel conversion ends, a DMA request is generated. After the DMA receives the request, it will transfer the converted data from the ADC_DAT register to the destination address specified by the user.

Note: In independent ADC mode, ADC1, ADC2, ADC3, ADC4 have DMA function. In dual ADC mode, the data converted by ADC2 is in the data register of ADC1, and the data converted by ADC4 is in the data register of ADC3.

9.9 ADC Mode

ADC1 (master) and ADC2 (slave), ADC3 (master) and ADC4 (slave) can form a dual ADC mode.

The ADC working mode can be selected by configuring ADC_CTRL1.DUSEL[3:0], which can be configured as independent mode or dual ADC mode. The ADC mode can be configured as the following working modes:

- Independent mode.
- Synchronous injection mode.
- Synchronous regular mode.
- Fast alternate mode.
- Slow alternate mode.
- Rotation trigger mode.
- Synchronous regular mode + synchronous injection mode.
- Synchronous regular mode + rotation trigger mode.
- Synchronous injection mode + alternate mode.

Notes:

1. When configuring dual ADC mode, if external event trigger is required, it is necessary to configure the main ADC external event trigger, the slave ADC software trigger, the master ADC and the slave ADC external trigger must be enabled at the same time, so as to avoid the wrong trigger conversion of the slave ADC.

2. When working in dual ADC mode, even if DMA is not used to transfer data, DMA needs to be enabled, and the converted data from the ADC can be read through the data register of the main ADC.

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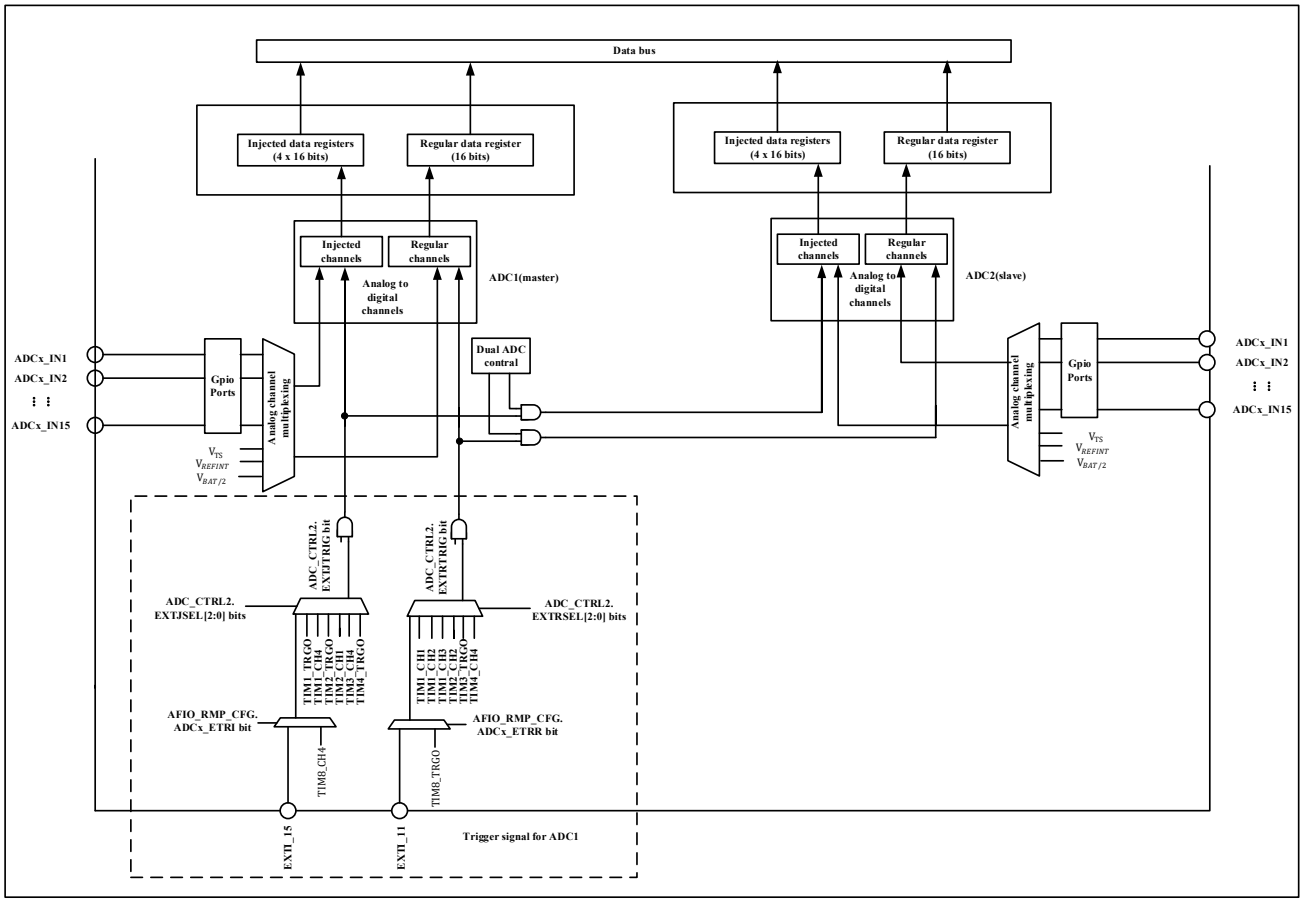
Figure 9-8 Dual ADC Block Diagram



9.9.1 Independent Mode

In this mode, each ADC works independently.

9.9.2 Synchronous Regular Mode

In this mode, a regular sequence is converted, and the external trigger comes from the multiplexer of ADC1, which is determined by ADC_CTRL2.EXTRSEL[2:0], and ADC2 will be triggered synchronously.

If ADC1 or ADC2 sets ADC_CTRL1.ENDCIEN, when the conversion of the regular sequence of ADC1 or ADC2 is completed, an ENDC interrupt will be generated, and the converted data will be stored in the ADC_DAT register. The high half word of ADC_DAT is the conversion data of ADC2. The low half word of ADC_DAT is the conversion data of ADC1, and 32-bit DMA can be used to transfer the data of ADC_DAT to SRAM.

Notes:

1. Do not convert the same channel on 2 ADCs (the sampling times of two ADCs on the same channel cannot overlap).

2. In the synchronous regular mode, the synchronous conversion regular sequence of ADC1 and ADC2 needs to be set to the same time, or the interval of the trigger signal is longer than the sequence with longer conversion time. If the interval between the trigger signals is smaller than the conversion of the longer sequence, the shorter sequence may start to convert again when the longer sequence is not completed.

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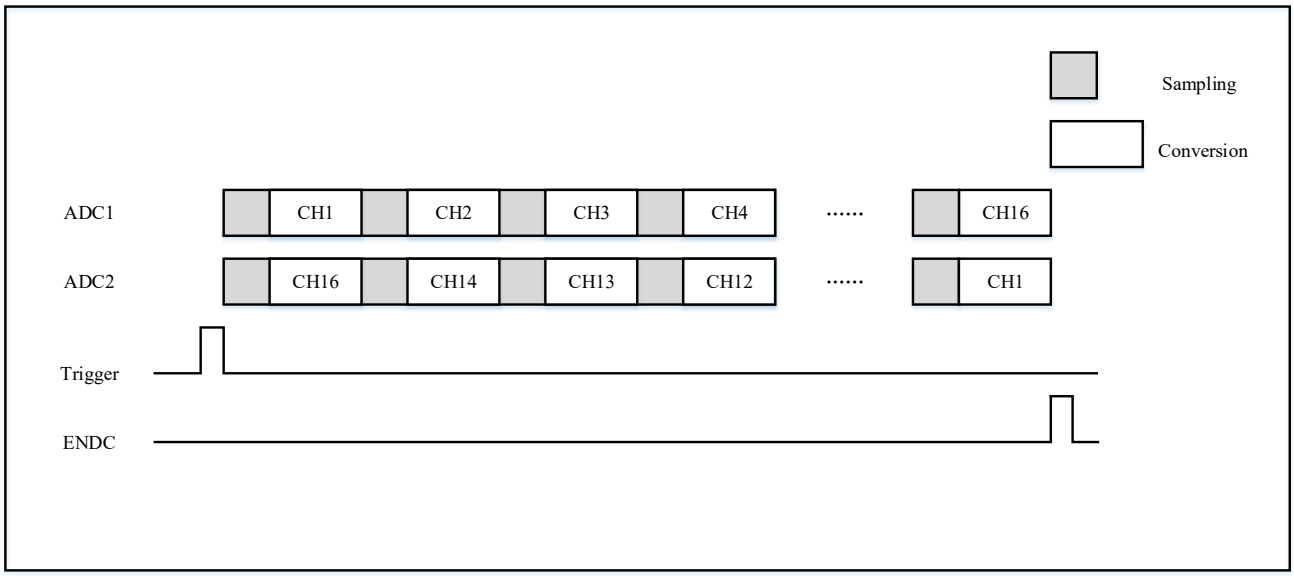
Figure 9-9 Schematic diagram of synchronous regular mode conversion of 16 channels



9.9.3 Synchronous Injection mode

Converting an injection sequence in this mode, the external trigger comes from the multiplexer of ADC1, determined by ADC_CTRL2.EXTJSEL[2:0], ADC2 will be triggered synchronously.

If ADC1 or ADC2 sets ADC_CTRL1.JENDCIEN, a JENDC interrupt will be generated when the injection sequence of ADC1 and ADC2 is converted, and the converted data will be stored in the respective ADC_JDATx registers.

Notes:

1. Do not convert the same channel on 2 ADCs (the sampling times of two ADCs on the same channel cannot overlap).

2. In the synchronous injection mode, the injection sequence of the synchronous conversion of ADC1 and ADC2 needs to be set to the same time, or the interval of the trigger signal is longer than the sequence with a longer conversion time. If the interval between the trigger signals is smaller than the conversion of the longer sequence, the shorter sequence may start to convert again when the longer sequence is not completed.

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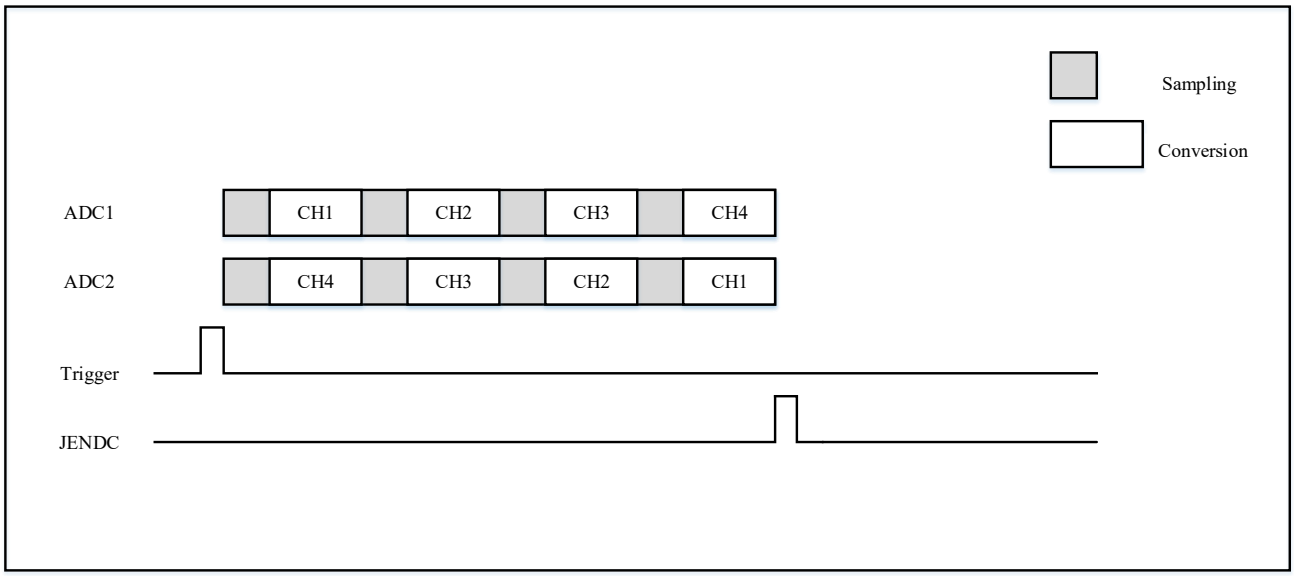
Figure 9-10 Schematic diagram of synchronous injection mode conversion of 4 channels



9.9.4 Fast Alternate Mode

This mode is for regular sequences (usually one channel). The external trigger comes from the multiplexer of ADC1, which is determined by ADC_CTRL2.EXTRSEL[2:0]. When the trigger occurs, ADC2 converts immediately and ADC1 starts converting after 7 ADC clock cycles. If ADC_CTRL2.CTU is set for ADC1 and ADC2, then the selected regular sequence will be converted continuously.

The converted data will be stored in the ADC_DAT register. The high halfword of ADC_DAT is the conversion data of ADC2, and the low halfword of ADC_DAT is the conversion data of ADC1. If ADC1 or ADC2 sets ADC_CTRL1.ENDCIEN, when the conversion of the regular sequence of ADC1 or ADC2 is completed, an ENDC interrupt will be generated. At this time, if ADC_CTRL2.ENDMA is set, a DMA transfer request can be generated, and the data of ADC_DAT can be passed through DMA transfers to SRAM.

Notes:

1. When using fast alternate mode, make sure that no injection channel is externally triggered.

2. The sampling time must be less than 7 ADC clock cycles to avoid overlapping sampling cycles when ADC1 and ADC2 convert the same channel.

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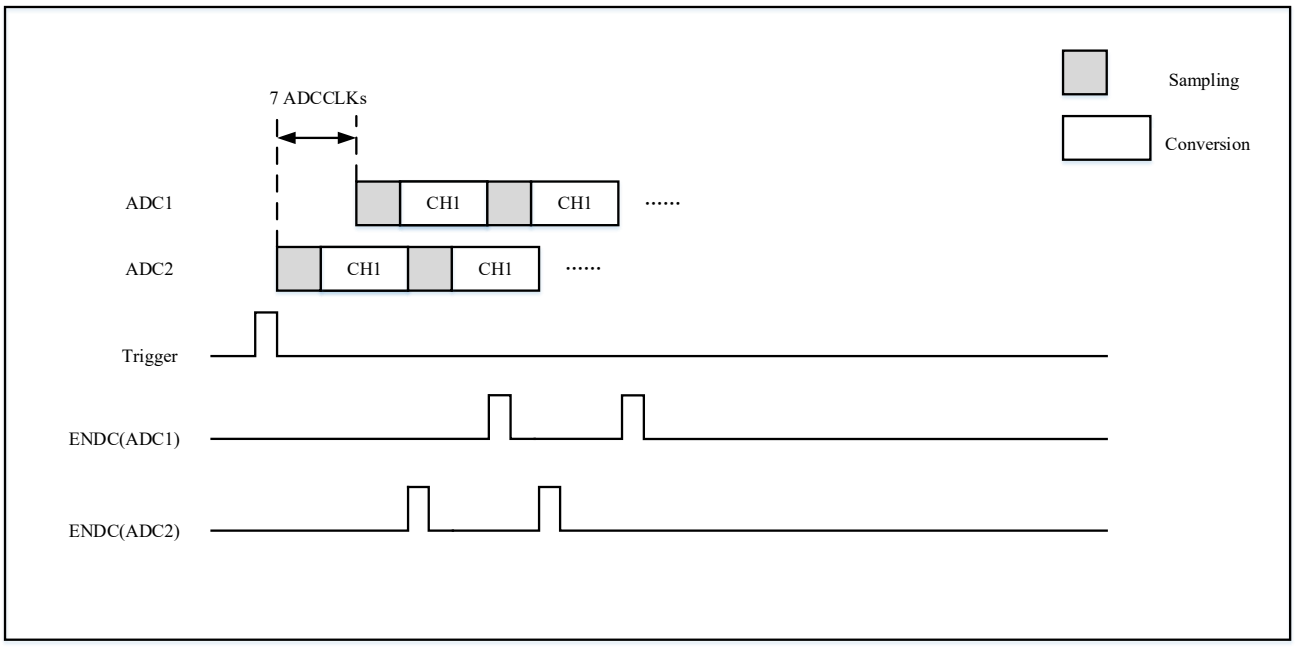
Figure 9-11 Schematic diagram of fast alternate mode conversion for continuous conversion of 1 channel



9.9.5 Slow Alternate Mode

This mode is for regular sequences (usually one channel). The external trigger comes from the multiplexer of ADC1, which is determined by ADC_CTRL2.EXTRSEL[2:0]. When the trigger is generated, ADC2 converts immediately, ADC1 starts to convert after 14 ADC clock cycles, ADC2 starts to convert again after 14 ADC clock cycles, and so on. This mode automatically continuously converts the regular sequence without the need to set ADC_CTRL2.CTU.

The converted data will be stored in the ADC_DAT register. The high half word of ADC_DAT is the conversion data of ADC2, and the low half word of ADC_DAT is the converted data of ADC1. If ADC1 or ADC2 sets ADC_CTRL1.ENDCIEN, when the conversion of the regular sequence of ADC1 or ADC2 is completed, an ENDC interrupt will be generated. At this time, if ADC_CTRL2.ENDMA is set, a DMA transfer request can be generated, and the data of ADC_DAT can be transferred to SRAM through DMA.

Notes:

1. When using slow alternate mode, make sure that no injection channel is externally triggered.

2. The sampling time must be less than 14 ADC clock cycles to avoid overlapping sampling cycles when ADC1 and ADC2 convert the same channel.

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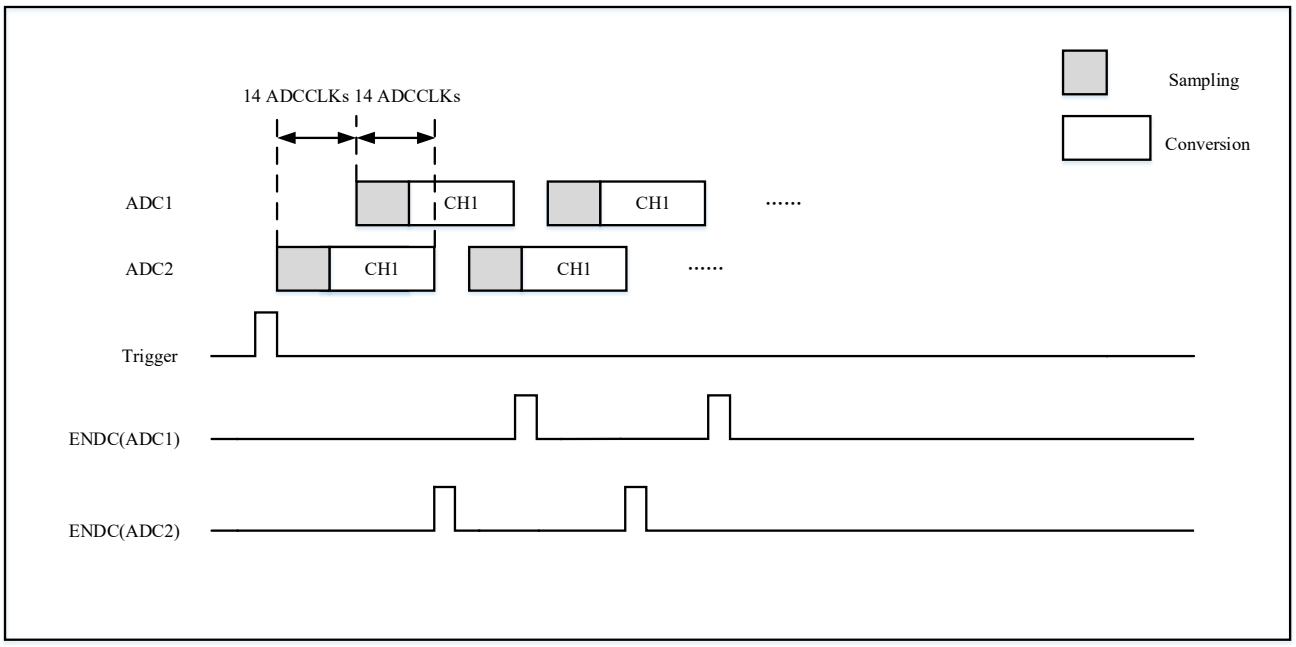
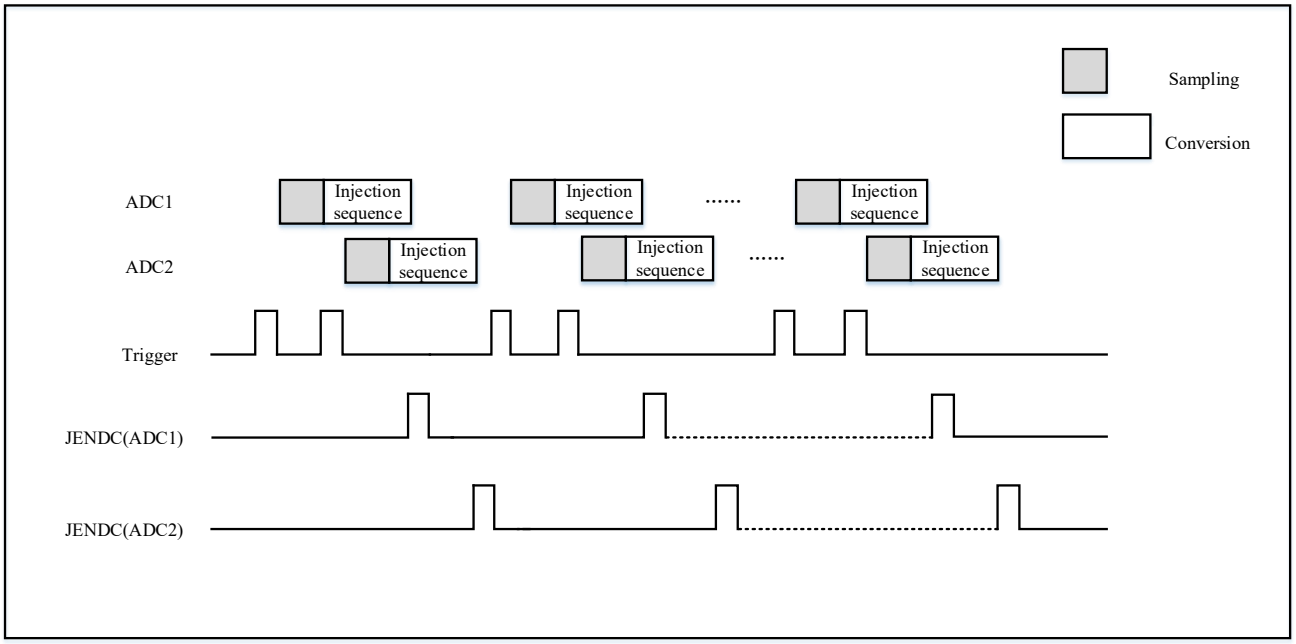
Figure 9-12 Schematic diagram of slow *alternate* mode conversion for 1 channel



9.9.6 Rotation Trigger Mode

This mode is suitable for injection sequences. The external trigger comes from the multiplexer of ADC1, which is determined by ADC_CTRL2.EXTJSEL[2:0]. When the first trigger is generated, all injection channels of ADC1 are converted, when the second trigger is generated, all injection channels of ADC2 are converted, and so on. If ADC1 or ADC2 sets ADC_CTRL1.JENDCIEN, a JENDC interrupt will be generated when the conversion of the injection sequence of ADC1 or ADC2 is completed. When all injection sequences have been converted, another external trigger is generated, and the rotation trigger starts again.

Figure 9-13 Rotation triggering: injecting channel groups



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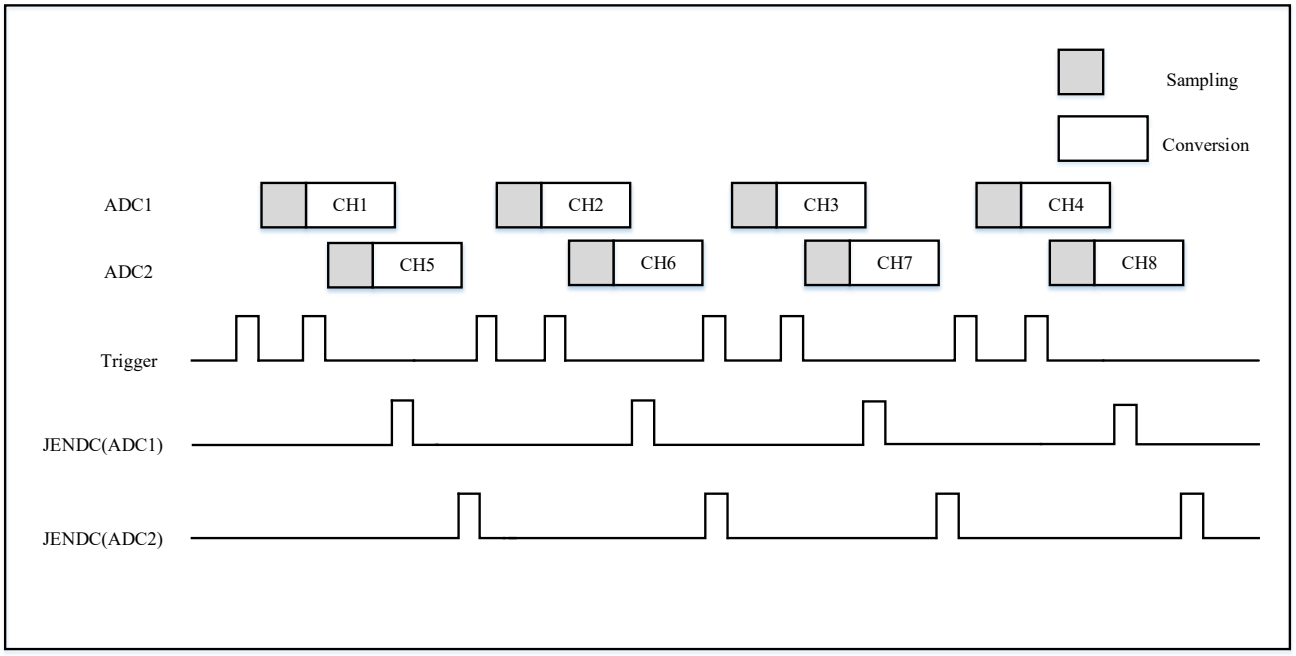
If the injection discontinuous mode is used on ADC1 and ADC2 at the same time, when the first trigger is generated, the first group of injection channels of ADC1 is converted; when the second trigger is generated, the first group of injection channels of ADC2 is converted; when the third trigger is generated, the second group of injection channels of ADC1 is converted. When the fourth trigger is generated, the second group of injection channels of ADC2 is converted, and the cycle is continues. If ADC1 or ADC2 sets ADC_CTRL1.JENDCIEN, a JENDC interrupt will be generated when the conversion of the injection sequence of ADC1 or ADC2 is completed. When all injection sequences have been converted, another external trigger is generated, and the rotation trigger starts again.

Figure 9-14 Rotation trigger: inject channel group in discontinuous mode



9.9.7 Mixed Synchronous Regular Mode + Synchronous Injection Mode

In this mode, the transition of the synchronous injection channel can interrupt the transition of the synchronous regular channel.

Note: In this mode, the sequence of synchronous conversion of ADC1 and ADC2 needs to be set to the same time, or the interval of the trigger signal is greater than that of the sequence with longer conversion time. If the interval between the trigger signals is smaller than the conversion of the longer sequence, the shorter sequence may start to convert again when the longer sequence is not completed.

9.9.8 Mixed Synchronous Regular Mode + Rotation Trigger Mode

Rotation triggered transitions of the injection channel can interrupt transitions of a synchronous regular channel.

When the injection channel event occurs, the injection rotation conversion starts immediately. If a regular conversion is in progress, both the master ADC and the slave ADC will stop the regular conversion to ensure that the regular conversion can be resumed synchronously after the injection conversion is completed.

Note: In this mode, the sequence of synchronous conversion of ADC1 and ADC2 needs to be set to the same time, or the interval of the trigger signal is greater than that of the sequence with longer conversion time. If the interval between the trigger signals is smaller than the conversion of the longer sequence, the shorter sequence may start to

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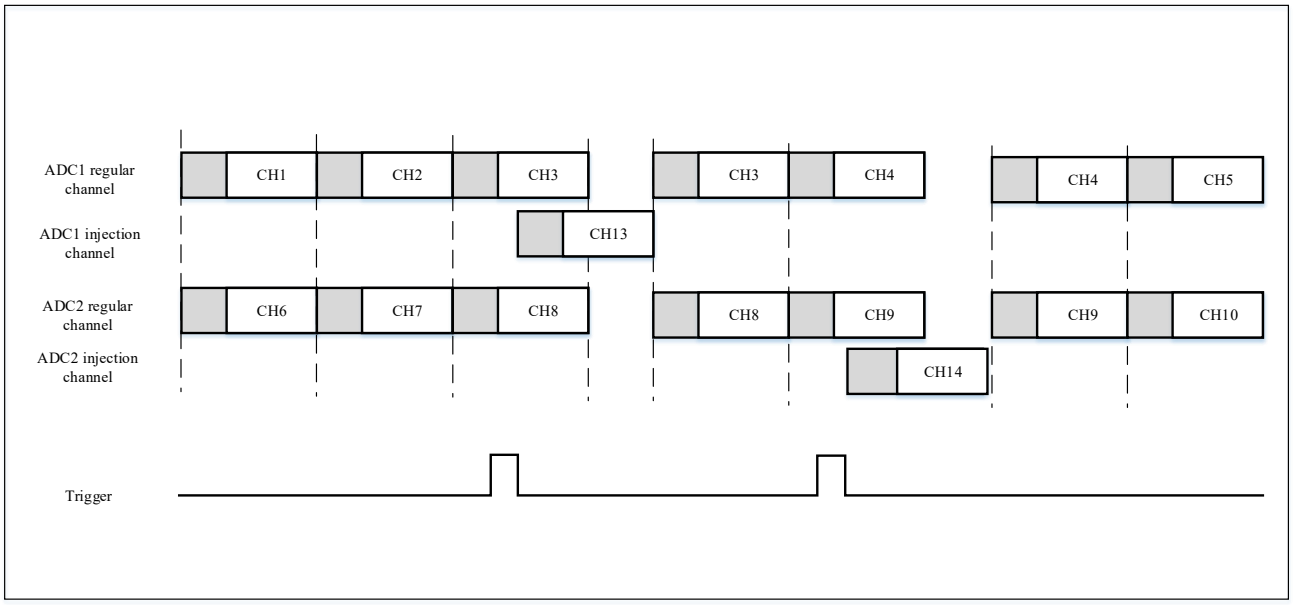
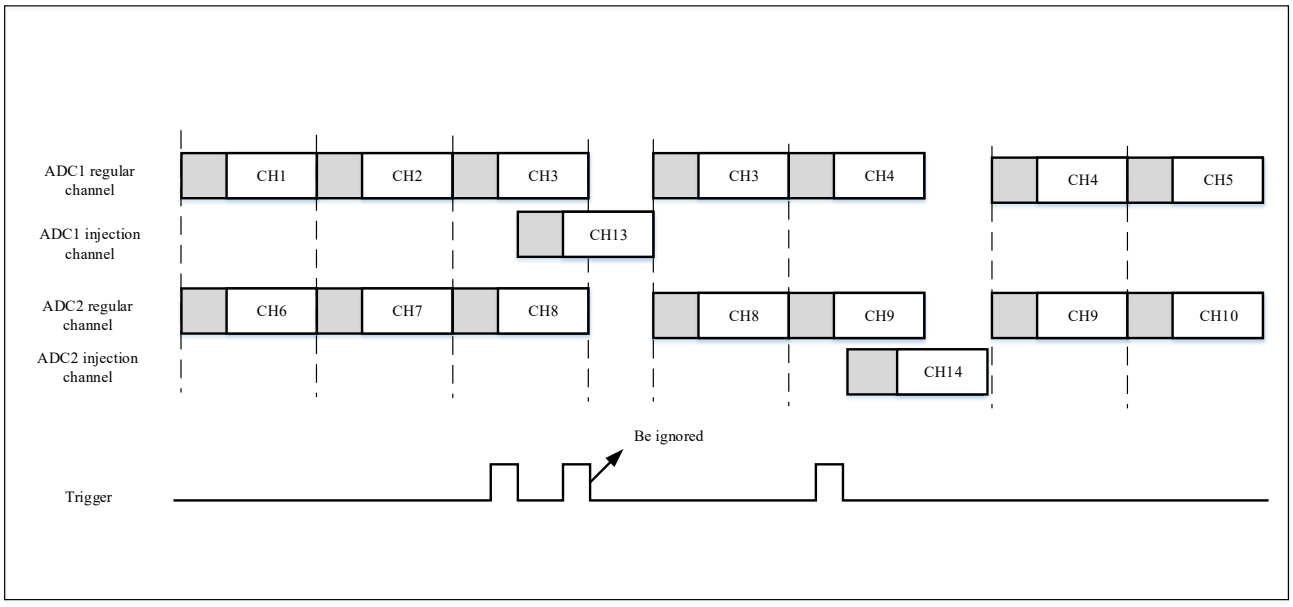
convert again when the longer sequence is not completed.

Figure 9-15 Combination of rotation mode and synchronous regular mode



If another injection trigger occurs during the injection transition, this trigger will be ignored. As shown below:

Figure 9-16 Injection trigger occurs during injection transition



9.9.9 Mixed Synchronous Injection Mode + Alternate Mode

In this mode, when the injection trigger occurs, the alternate conversion will be interrupted, the injection conversion will be started, and the alternate conversion will be resumed after the injection conversion is completed.

Note: When the ADC clock prescale factor is set to 4, the sampling time will not be evenly distributed after the alternate *mode recovery, and the sampling interval is 8 ADC clock cycles alternated with 6 ADC clock cycles instead of 7 ADCs evenly clock cycle.*

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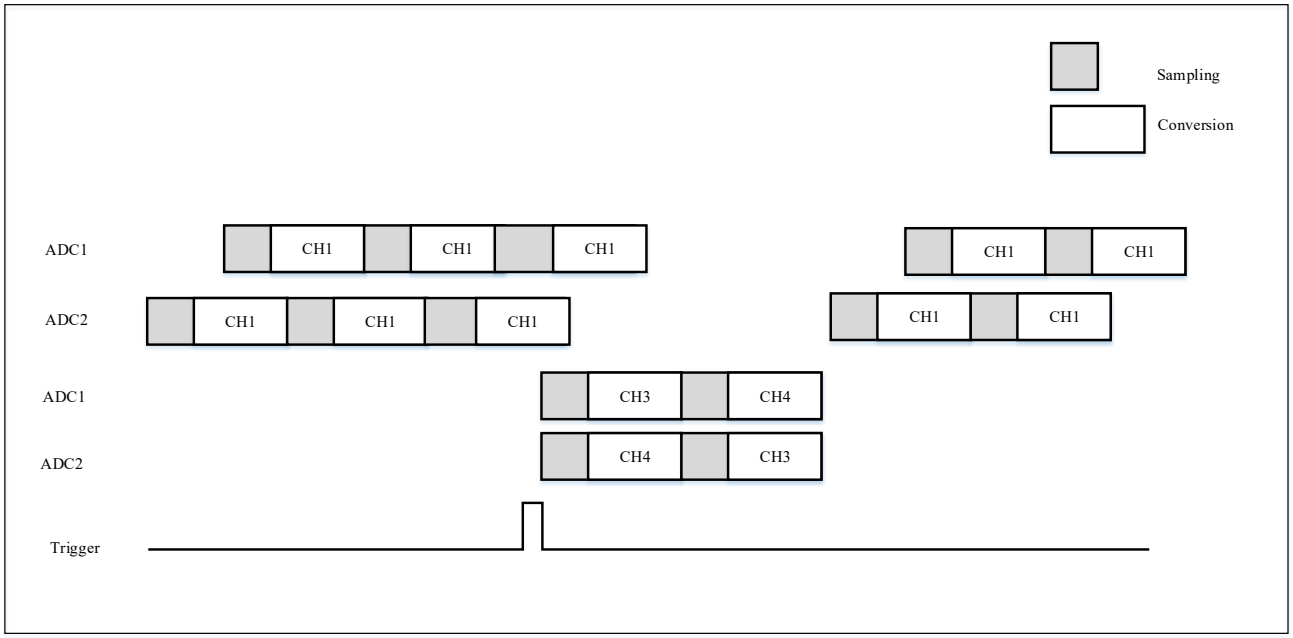
Figure 9-17 Alternate single-channel conversions are interrupted by injection sequences CH3 and CH4



9.10 Temperature Sensor

Set the ADC_CTRL2.TEMPEN bit to 1, enable the temperature sensor and $V_{REFINT,}$ and use the temperature sensor to detect the ambient temperature when the device is working. The output voltage sampled by the temperature sensor is converted into a digital value by the ADC_IN16 channel. When the temperature sensor is working, the ideal sampling time is 17.1us; when the temperature sensor is not working, the ADC_CTR2.TEMPEN bit can be cleared by software to reduce power consumption. As follows is a block diagram of a temperature sensor.

The output voltage of the temperature sensor changes linearly with temperature. Different chips will have different offsets in the temperature curve due to different production processes. Through testing, it is found that the maximum offset is 3°C. This characteristic makes the internal temperature sensor more suitable for detecting temperature changes. Not suitable for measuring absolute temperature. When accurate temperature measurement is required, an external temperature sensor should be used.

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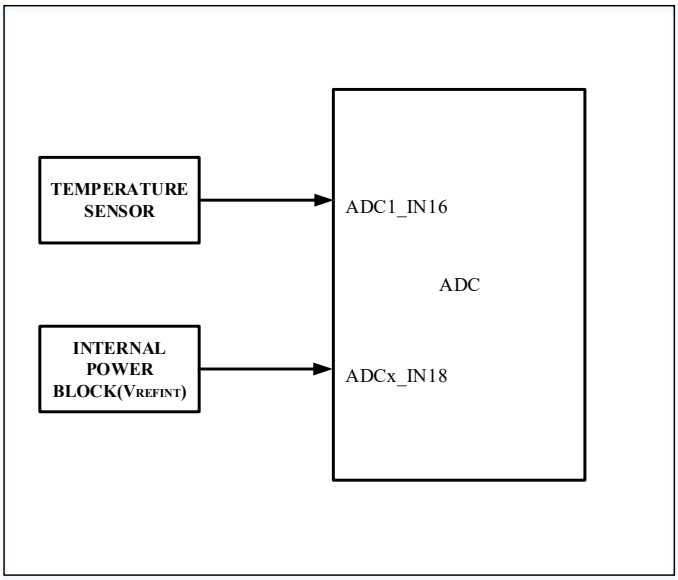
Figure 9-18 Temperature sensor and VREFINT diagram of the channel



9.10.1 Temperature Sensor Using Flow

1) Configure the channel (ADC_IN16) and sampling time of the channel to be 17.1 us

2) Set ADC_CTRL2.TEMPEN bit to 1 to enable temperature sensor and V_{REFINT}

3) Set ADC_CTRL2.ON bit to 1 to start ADC conversion (or through external trigger)

4) Read the temperature data in the ADC data register, and calculate the temperature value by the following formula:

Temperature (°C) = {(V_{30} - V_{SENSE}) / Avg_Slope} + 30- T_{offset}

In which:

V_{30} = V_{SENSE} at 30 degrees celsius

Avg_Slope = temperature and Average slope of a V_{SENSE} curve (mV/°C or µV/°C)

T_{offset} = empirical value for temperature error compensation (°C)

Refer to the values of V_{30} and Avg_Slope in the electrical characteristics chapter of the datasheet.

Note: There is a settling time before the sensor wakes up from the power-off mode to the correct output of VSENSE; there is also a settling time after the ADC is powered on, so in order to shorten the delay, the ADC_CTRL2.TEMPEN and ADC_CTRL2.ON bits should be set at the same time.

9.11 ADC Interrupt

ADC interrupts can be from an end of regular or injection sequence conversion, an analog watchdog event when input voltage exceeds the threshold, any end of regular or injection channel conversion. These interrupts have independent interrupt enable bits.

There are 2 status flags in the ADC_STS register: injection sequence channel conversion started (JSTR) and regular sequence channel conversion started (STR). But there are no interrupts associated with these two flags in the ADC.

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Note: ADC1 and ADC2 share one interrupt entry, while ADC3 and ADC4 share one interrupt entry.

Table 9-9 ADC interrupt

Interrupt event	Event flags	Enable control bit
Regular sequence or injection conversion is complete	ENDC	ENDCIEN
Injection sequence conversion is complete	JENDC	JENDCIEN
Analog watchdog status bit is set	AWDG	AWDGIEN
Any regular channel interruption is enabled	ENDCA	ENDCAIEN
Any injection channel interruption is enabled	JENDCA	JENDCAIEN

9.12 ADC Registers

9.12.1 ADC Register Overview

Table 9-10 ADC register overview

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
000h	ADC_STS	Reserved																									JENDCA	ENDCA	STR	JSTR	JENDC	ENDC	AWDG
	Reset Value																										0	0	0	0	0	0	0
004h	ADC_CTRL1	Reserved								AWDGERCH	AWDGEJCH	Reserved		DUSEL				DCTU			DJCH	DREGCH	AUTOJC	AWDGSGLEN	SCANMD	JENDCIEN	AWDGIEN	ENDIEN	AWDGCH				
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
008h	ADC_CTRL2	Reserved								TEMPEN	SWSTRRCH	SWSTRJCH	EXTRTRIG	EXTRSEL[2:0]			Reserved	EXTJTRIG	EXTJSEL			ALIG	Reserved		ENDMA	Reserved					ENCAL	CTU	ON
	Reset Value									0	0	0	0	0	0	0		0	0	0	0	0			0						0	0	0
00Ch	ADC_ SAMPT1	Reserved								SAMP17[2:0]			SAMP16[2:0]			SAMP15[2:0]			SAMP14[2:0]			SAMP13[2:0]			SAMP12[2:0]			SAMP11[2:0]			SAMP10[2:0]		
	Reset Value									0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
010h	ADC_ SAMPT2	Reserved	SAMP9[2:0]			SAMP8[2:0]				SAMP7[2:0]			SAMP6[2:0]			SAMP5[2:0]			SAMP4[2:0]			SAMP3[2:0]			SAMP2[2:0]			SAMP1[2:0]			SAMP0[2:0]		
	Reset Value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
014h	ADC_JOFFSET1	Reserved																				OFFSETJCH2[11:0]											
	Reset Value																					0	0	0	0	0	0	0	0	0	0	0	0
018h	ADC_JOFFSET2	Reserved																				OFFSETJCH2[11:0]											
	Reset Value																					0	0	0	0	0	0	0	0	0	0	0	0
01Ch	ADC_JOFFSET3	Reserved																				OFFSETJCH3[11:0]											
	Reset Value																					0	0	0	0	0	0	0	0	0	0	0	0
020h	ADC_JOFFSET4	Reserved																				OFFSETJCH4[11:0]											
	Reset Value																					0	0	0	0	0	0	0	0	0	0	0	0
024h	ADC_WDGHIGH	Reserved																HTH[11:0]															
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
028h	ADC_WDGLOW	Reserved																LTH[11:0]															
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
02Ch	ADC_RSEQ1	Reserved								LEN[3:0]				SEQ16[4:0]					SEQ15[4:0]				SEQ14[4:0]					SEQ13[4:0]				
	Reset Value									0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
030h	ADC_RSEQ2	Reserved	SEQ12[4:0]							SEQ11[4:0]				SEQ10[4:0]					SEQ9[4:0]				SEQ8[4:0]					SEQ7[4:0]				
	Reset Value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
034h	ADC_RSEQ3	Reserved	SEQ12[4:0]							SEQ11[4:0]				SEQ10[4:0]					SEQ9[4:0]				SEQ8[4:0]					SEQ7[4:0]				
	Reset Value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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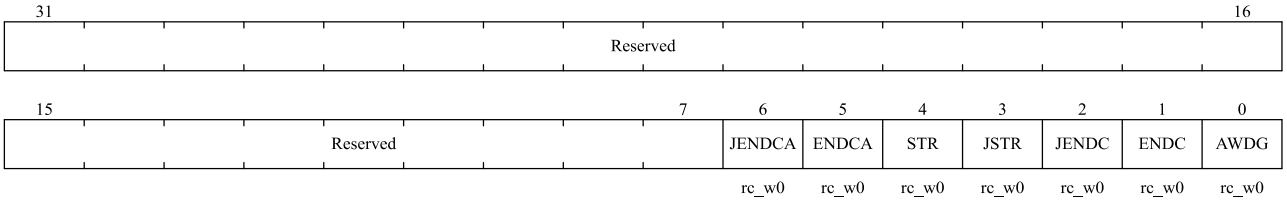
Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
038h	ADC_JSEQ	Reserved										JLEN[1:0]		JSEQ4[4:0]					JSEQ3[4:0]					JSEQ2[4:0]					JSEQ1[4:0]				
	Reset Value											0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
03Ch	ADC_JDAT1	Reserved																JDAT1[15:0]															
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
040h	ADC_JDAT2	Reserved																JDAT2[15:0]															
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
044h	ADC_JDAT3	Reserved																JDAT3[15:0]															
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
048h	ADC_JDAT4	Reserved																JDAT4[15:0]															
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
04Ch	ADC_DAT	Reserved																DAT[15:0]															
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
050h	ADC_DIFSEL	Reserved												DIFSEL[18:0]																		Reserved	
	Reset Value													0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
054h	ADC_CALFACT	Reserved										CALFACTD[6:0]							Reserved										CALFACTS[6:0]					
	Reset Value											0	0	0	0	0	0	0											0	0	0	0	0	0
058h	ADC_CTRL3	Reserved																	VBATMEN	DPWMOD	JENDCAIEN	ENDCAIEN	BPCAL	PDRDY	RDY	CKMOD	CALALD	CALDIF	RES[1:0]				
	Reset Value																		0	0	0	0	0	0	0	0	0	0	0	0			
05Ch	ADC_ SAMPT3	Reserved																												SAMPSEL	SAMP[2:0]		
	Reset Value																													0	0	0	0

9.12.2 ADC Status Register (ADC_STS)

Address offset: 0x00

Reset value: 0x0000 0000



Bit field	Name	Description
31:15	Reserved	Reserved, the reset value must be maintained
6	JENDCA	Any injected channel end of conversion flag This bit is set by hardware at the end of any injection channel conversion and cleared by software. 0: Conversion is not complete; 1: Conversion is complete.
5	ENDCA	Any channel end of conversion flag This bit is set by hardware at the end of any channel (regular or injection) conversion and cleared by software. 0: Conversion is not complete; 1: Conversion is complete.

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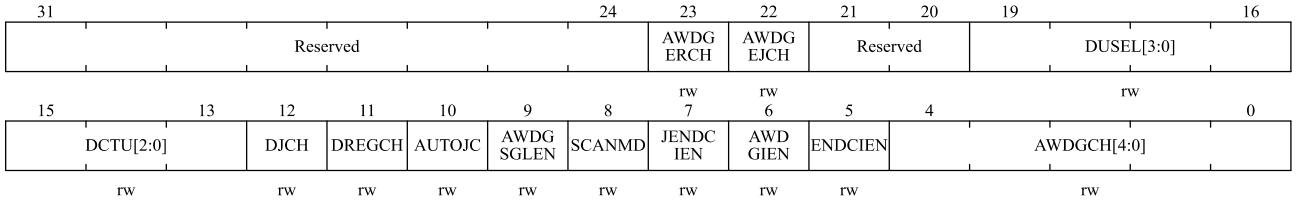
Bit field	Name	Description
4	STR	Regular channel start flag This bit is set by hardware at the start of regular channel conversion and cleared by software. 0: Regular channel conversion has not started. 1: Regular channel conversion has started.
3	JSTR	Injected channel start flag This bit is set by hardware at the start of the injection channel conversion and cleared by software. 0: Injection sequence channel conversion has not started. 1: Injection sequence channel conversion has started.
2	JENDC	Injected channel end of conversion This bit is set by hardware at the end of all injection sequence channel conversions and cleared by software 0: Conversion is not complete. 1: Conversion is complete.
1	ENDC	Conversion sequence channel end of conversion This bit is set by hardware at the end of all regular(or injection) sequence channel conversion and cleared by software 0: Conversion is not complete. 1: Conversion is complete.
0	AWDG	Analog watchdog flag This bit is set by hardware and cleared by software when converted voltage values are outside the range defined by the ADC_LTR and ADC_HTR registers 0: Analog watchdog event not occurs; 1: Analog watchdog event occurs.

9.12.3 ADC Control Register 1 (ADC_CTRL1)

Address offset: 0x04

Reset value: 0x0000 0000



Bit field	Name	Description
31:24	Reserved	Reserved, the reset value must be maintained
23	AWDGERCH	Analog watchdog enable on regular channels This bit is set and cleared by the software. 0: Disables analog watchdog on regular channel. 1: Use analog watchdog on regular channels.
22	AWDGEJCH	Analog watchdog enable on injected channels This bit is set and cleared by the software.

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Bit field	Name	Description
		0: Disables analog watchdog on injection channel. 1: Use analog watchdog on the injection channel.
21:20	Reserved	Reserved, the reset value must be maintained
19:16	DUSEL[3:0]	Dual mode selection Software uses these bits to select modes of operation. 0000: independent mode; 0001: mixed synchronous regular mode + synchronous injection mode; 0010: mixed synchronous regular mode + rotation trigger mode; 0011: mixed synchronous injection mode + fast alternate mode; 0100: mixed synchronous injection mode + slow alternate mode; 0101: synchronous injection mode; 0110: synchronous regular mode; 0111: fast alternate mode; 1000: slow alternate mode; 1001: rotation trigger mode. Note: These bits are reserved in ADC2 and ADC4. Changing the channel configuration in dual ADC mode will cause a restart condition. It is recommended to turn off the dual ADC mode before changing the configuration to avoid synchronization loss.
15:13	DCTU[2:0]	Discontinuous mode channel count The software uses these bits to define the number of channels for converting after receiving an external trigger in discontinuous mode 000: 1 channel 001: 2 channels ... 111: 8 channels
12	DJCH	Discontinuous mode on injected channels This bit is set and cleared by the software. It is used to turn on or off discontinuous mode on injected channels. 0: Disable discontinuous mode on injection sequence channel 1: Enable discontinuous mode on injection sequence channel
11	DREGCH	Discontinuous mode is on regular channels. This bit is set and cleared by the software. It is used to turn on or off discontinuous mode on regular channels. 0: Disable discontinuous mode on regular sequence channel 1: Enable discontinuous mode on regular sequence channel
10	AUTOJC	Automatic injected sequence conversion This bit is set and cleared by the software to enable or disable automatic injection sequence channel conversion after regular sequence channel conversion is complete 0: Disable automatic injection channel conversion. 1: Enable automatic injection channel conversion.
9	AWDGSGLEN	Enable the watchdog on a single channel in scan mode This bit is set and cleared by software to enable or disable analog watchdog functions on channels specified by ADC_CTRL1.AWDGCH[4:0]

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Bit field	Name	Description
		0: Use watchdog on all channels. 1: Use watchdog on single channel.
8	SCANMD	Scan mode This bit is set and cleared by the software to enable or disable scan mode. In scan mode, the conversion is made by ADC_RSEQx or the selected channel of the ADC_JSEQ register. 0: Disable scan mode. 1: Enable scan mode. *Note: If the ADC_CTRL1.ENDCIEN or ADC_CTRL1.JENDCIEN bits are set separately, ADC_STS.ENDC or ADC_STS.JENDC interrupts occur only after the last channel has been converted.*
7	JENDCIEN	Interrupt enable for injected channels This bit is set and cleared by the software to disallow or allow interrupts after all injection channel conversions have finished. 0: Disable JENDC interruption. 1: Enable JENDC interruption.
6	AWDGIEN	Analog watchdog interrupt enable This bit is set and cleared by software to disallow or allow interrupt generated by analog watchdog. In scan mode, if the watchdog detects an out-of-range value, the scan is aborted only when that bit is set. 0: Disable analog watchdog interruption. 1: Enable analog watchdog interruption.
5	ENDCIEN	Interrupt enable for any channel This bit is set and cleared by the software to disallow or allow interrupts to occur after the regular or injected channel conversion ends. 0: Disable ENDC interruption. 1: Enable ENDC interruption.
4:0	AWDGCH[4:0]	Analog watchdog channel select bits These bits are set and cleared by software to select input channels that analog watchdog protection. 00000: ADC analog input channel 0 00001: ADC analog input channel 1 ... 01111: ADC analog input channel 15 10000: ADC analog input channel 16 10001: ADC analog input channel 17 10010: ADC analog input channel 18 Reserved all other values.

9.12.4 ADC Control Register 2 (ADC_CTRL2)

Address offset: 0x08

Reset value: 0x0000 0000

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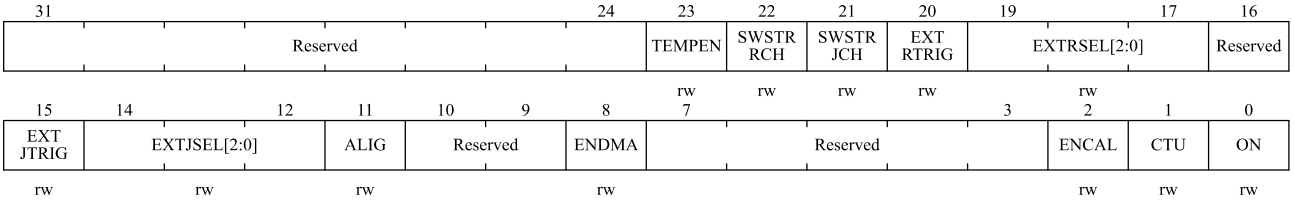

Bit field	Name	Description
31:24	Reserved	Reserved, the reset value must be maintained
23	TEMPEN	Temperature sensor and V_{REFINT} Enable This bit is set and cleared by the software to enable or disable the temperature sensor and V_{REFINT} Channel. 0: Disables the temperature sensor and V_{REFINT}. 1: Enable the temperature sensor and V_{REFINT}.
22	SWSTRRCH	Start conversion of regular channels This bit is set by the software to start the conversion and cleared by the hardware as soon as the conversion begins. If SWSTRRCH is selected as the trigger event in the ADC_CTRL2.EXTRSEL[2:0] bit, which is used to initiate the conversion of a set of regular channels 0: Reset state. 1: Starts converting the regular channel.
21	SWSTRJCH	Start conversion of injected channels This bit is set by the software to initiate the conversion and can be cleared by the software or by the hardware as soon as the conversion begins. If SWSTRJCH is selected as the trigger event in the ADC_CTRL2.EXTJSEL[2:0] bit, which is used to initiate a conversion of a set of injected channels 0: Reset state. 1: Starts converting the injection channel.
20	EXTRTRIG	External trigger conversion mode for regular channels This bit is set and cleared by software to enable or disable external triggering events that can start regular sequence conversion. 0: Start conversion without external events. 1: Use an external event to start the conversion.
19:17	EXTRSEL[2:0]	External event select for regular sequence These bits select external events to start the regular sequence conversion Trigger configuration for ADC1 and ADC2: 000: TIM1_CC1 event; 100: TIM3_TRGO event; 001: TIM1_CC2 event; 101: TIM4_CC4 event; 010: TIM1_CC3 event; 110: EXTI line 11/TIM8_TRGO event; 011: TIM2_CC2 event; 111: SWSTRRCH. Trigger configuration for ADC3 and ADC4: 000: TIM3_CC1 event; 100: TIM8_TRGO event; 001: TIM2_CC3 event; 101: TIM5_CC1 event; 010: TIM1_CC3 event; 110: EXTI line 10/TIM5_CC3 event; 011: TIM8_CC1 event; 111: SWSTRRCH.

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Bit field	Name	Description
16	Reserved	Reserved, the reset value must be maintained
15	EXTJTRIG	External trigger conversion mode for injected channels This bit is set and cleared by software to enable or disable external triggering events that can start injection sequence conversion. 0: Start conversion without external events. 1: Use an external event to start the conversion.
14:12	EXTJSEL[2:0]	External event select for injected sequence These bits select the External event used to trigger the injected sequence conversion. Trigger configuration for ADC1 and ADC2: 000: TIM1_TRGO event; 100: TIM3_CC4 event; 001: TIM1_CC4 event; 101: TIM4_TRGO event; 010: TIM2_TRGO event; 110: EXTI line 15/TIM8_CC4 event; 011: TIM2_CC1 event; 111: SWSTRRCH. Trigger configuration for ADC3 and ADC4: 000: TIM3_TRGO event; 100: TIM8_CC4 event; 001: TIM1_CC4 event; 101: TIM5_TRGO event; 010: TIM4_CC3 event; 110: EXTI line 14/TIM5_CC4 event; 011: TIM8_CC2 event; 111: SWSTRRCH.
11	ALIG	Data alignment This bit is set and cleared by the software. Refer to Table 9-3 and Table 9-4. 0: Right-aligned. 1: Left-aligned.
10:9	Reserved	Reserved, the reset value must be maintained
8	ENDMA	Direct memory access mode This bit is set and cleared by the software. See the DMA Controller chapter for details. 0: Do not use DMA mode. 1: Use DMA mode.
7:3	Reserved	Reserved, the reset value must be maintained
2	ENCAL	A/D calibration This bit is set by software to start calibration and cleared by hardware at the end of calibration. 0: Calibration completed; 1: Starts calibration.
1	CTU	Continuous conversion This bit is set and cleared by the software. If this bit is set, the conversion continues until the bit is cleared. 0: Single conversion mode. 1: Continuous conversion mode.
0	ON	A/D converter ON/OFF This bit is set and cleared by the software. When the bit is' 0 ', writing '1' will wake the ADC from power-off mode. When the bit is' 1 ', writing '1' starts the conversion. The application should note that there is a delay t_{STAB} between the time the converter is powered on and the time the conversion begins, see Figure 9-5.

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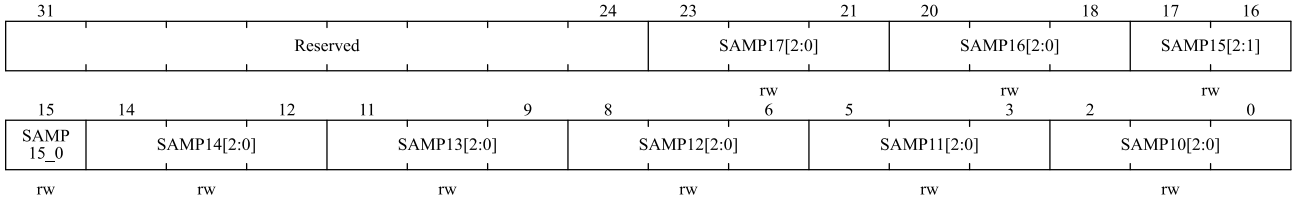
Bit field	Name	Description
		0: Close ADC conversion/calibration and enter power-down mode. 1: Start ADC and start conversion. Note: If there are other bits changed in this register along with ON, the conversion will not be triggered. This is to prevent the wrong conversion from being triggered.

9.12.5 ADC Sampling Time Register 1 (ADC_SAMPT1)

Address offset: 0x0C

Reset value: 0x0000 0000

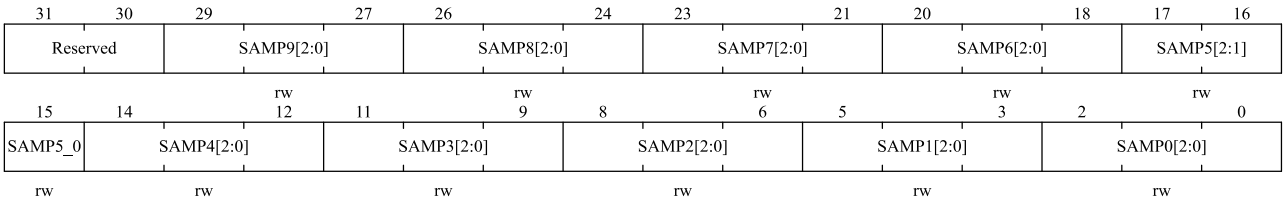


Bit field	Name	Description
31:24	Reserved	Reserved, the reset value must be maintained
23:0	SAMPx[2:0]	Channel x sample time selection These bits are used to independently select the sampling time for each channel. The channel selection bit must remain constant during the sampling period. ADC_SAMPT3.SAMPSEL = 0, the sampling time is set as follows: 000: 1.5 cycles 100: 41.5 cycles 001: 7.5 cycles 101: 55.5 cycles 010: 13.5 cycles 110: 71.5 cycles 011: 28.5 cycles 111: 239.5 cycles ADC_SAMPT3.SAMPSEL = 1, the sampling time is set as follows: 000: 1.5 cycles 100: 19.5 cycles 001: 2.5 cycles 101: 61.5 cycles 010: 4.5 cycles 110: 181.5 cycles 011: 7.5 cycles 111: 601.5 cycles

9.12.6 ADC Sampling Time Register 2 (ADC_ SAMPT2)

Address offset: 0x10

Reset value: 0x0000 0000



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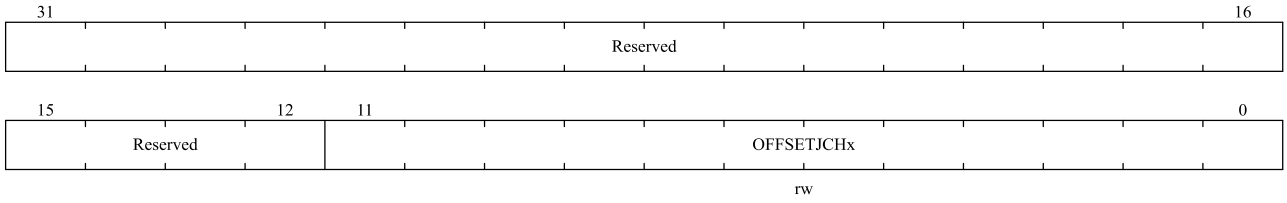
Bit field	Name	Description
31:30	Reserved	Reserved, the reset value must be maintained
29:0	SAMPx[2:0]	Channel x sample time selection These bits are used to independently select the sampling time for each channel. The channel selection bit must remain constant during the sampling period. ADC_SAMPT3.SAMPSEL = 0, the sampling time is set as follows: 000: 1.5 cycles 100: 41.5 cycles 001: 7.5 cycles 101: 55.5 cycles 010: 13.5 cycles 110: 71.5 cycles 011: 28.5 cycles 111: 239.5 cycles ADC_SAMPT3.SAMPSEL = 1, the sampling time is set as follows: 000: 1.5 cycles 100: 19.5 cycles 001: 2.5 cycles 101: 61.5 cycles 010: 4.5 cycles 110: 181.5 cycles 011: 7.5 cycles 111: 601.5 cycles

9.12.7 ADC Injected Channel Data Offset Register x (ADC_JOFFSETx) (x=1…4)

Address offset: 0x14-0x20

Reset value: 0x0000 0000

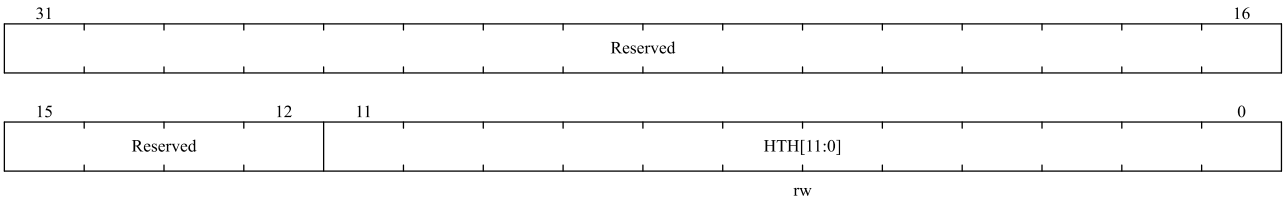


Bit field	Name	Description
31:12	Reserved	Reserved, the reset value must be maintained
11:0	OFFSETJCHx[11:0]	Data offset for injected channel x These bits define the values used to subtract from the original conversion data when the conversion is injected into the channel. The result of the conversion can be read in the ADC_JDATx register.

9.12.8 ADC Watchdog High Threshold Register (ADC_WDGHIGH)

Address offset: 0x24

Reset value: 0x0000 0FFF



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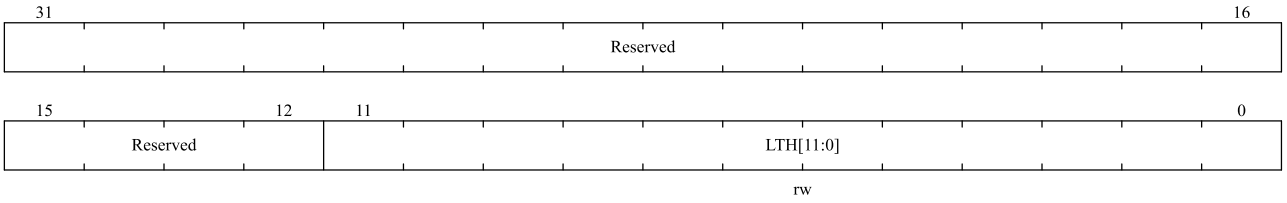
Bit field	Name	Description
31:12	Reserved	Reserved, the reset value must be maintained
11:0	HTH[11:0]	Analog watchdog high threshold These bits define the high thresholds for analog watchdog.

9.12.9 ADC Watchdog Low Threshold Register (ADC_WDGLOW)

Address offset: 0x28

Reset value: 0x0000 0000

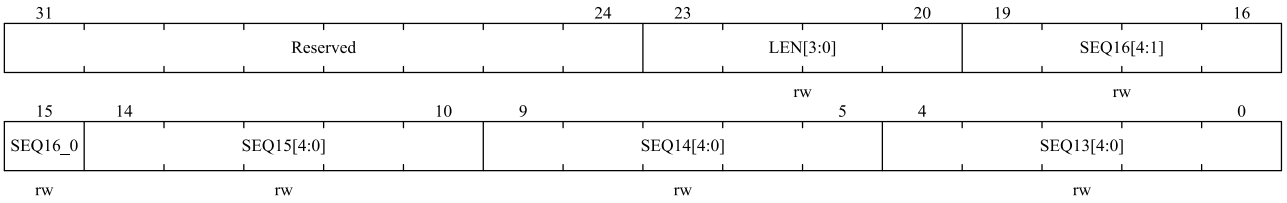


Bit field	Name	Description
31:12	Reserved	Reserved, the reset value must be maintained
11:0	LTH[11:0]	Analog watchdog low threshold These bits define the low thresholds for analog watchdog.

9.12.10 ADC Regular Sequence Register 1 (ADC_RSEQ1)

Address offset: 0x2C

Reset value: 0x0000 0000



Bit field	Name	Description
31:24	Reserved	Reserved, the reset value must be maintained
23:20	LEN[3:0]	Regular channel sequence length These bits are software-defined as the number of channels in the regular sequence channel conversion. 0000: 1 conversion 0001: 2 conversions ... 1111: 16 conversions
19:15	SEQ16[4:0]	16th conversion in regular sequence These bits are software-defined as the number (0 to 18) of the 16th conversion channel in the conversion sequence.
14:10	SEQ15[4:0]	15th conversion in regular sequence
9:5	SEQ14[4:0]	14th conversion in regular sequence

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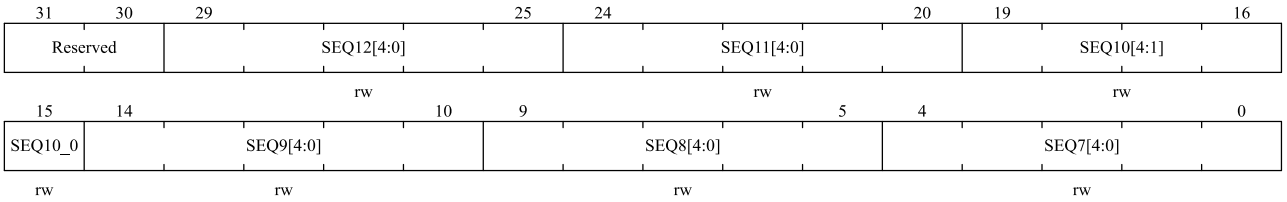
Bit field	Name	Description
4:0	SEQ13[4:0]	13th conversion in regular sequence

9.12.11 ADC Regular Sequence Register 2 (ADC_RSEQ2)

Address offset: 0x30

Reset value: 0x0000 0000

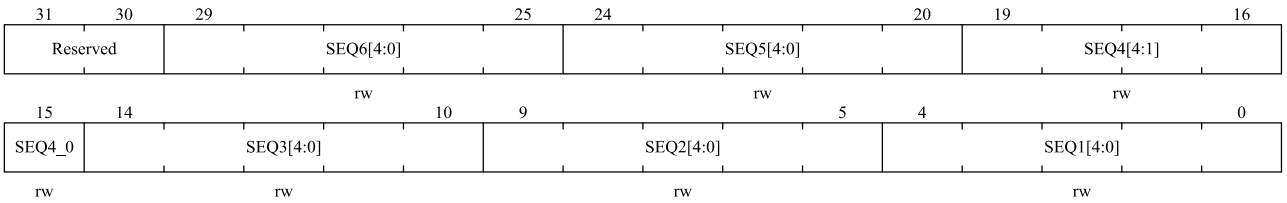


Bit field	Name	Description
31:30	Reserved	Reserved, the reset value must be maintained
29:25	SEQ12[4:0]	12th conversion in regular sequence These bits are software-defined as the number (0 to 18) of the 12th conversion channel in the conversion sequence.
24:20	SEQ11[4:0]	11th conversion in regular sequence
19:15	SEQ10[4:0]	10th conversion in regular sequence
14:10	SEQ9[4:0]	9th conversion in regular sequence
9:5	SEQ8[4:0]	8th conversion in regular sequence
4:0	SEQ7[4:0]	7th conversion in regular sequence

9.12.12 ADC Regular Sequence Register 3 (ADC_RSEQ3)

Address offset: 0x34

Reset value: 0x0000 0000



Bit field	Name	Description
31:30	Reserved	Reserved, the reset value must be maintained
29:25	SEQ6[4:0]	6th conversion in regular sequence These bits are software-defined as the number (0 to 18) of the 6th transition channel in the conversion sequence.
24:20	SEQ5[4:0]	5th conversion in regular sequence
19:15	SEQ4[4:0]	4th conversion in regular sequence
14:10	SEQ3[4:0]	3rd conversion in regular sequence
9:5	SEQ2[4:0]	2nd conversion in regular sequence

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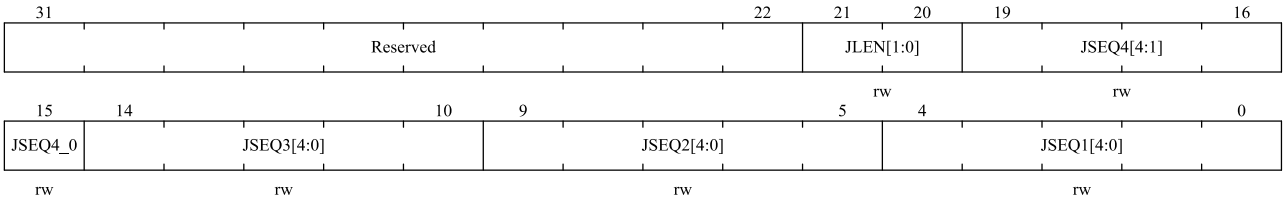
Bit field	Name	Description
4:0	SEQ1[4:0]	1st conversion in regular sequence

9.12.13 ADC Injection Sequence Register (ADC_JSEQ)

Address offset: 0x38

Reset value: 0x0000 0000

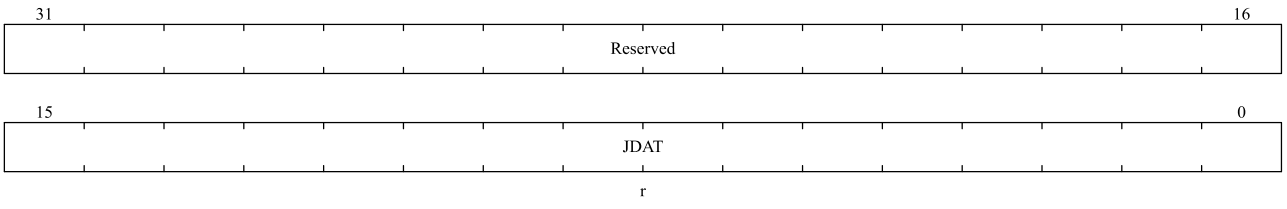


Bit field	Name	Description
31:22	Reserved	Reserved, the reset value must be maintained
21:20	JLEN[1:0]	Injected sequence length These bits are software-defined as the number of channels in the injected channel conversion sequence. 00: 1 conversion 01: 2 conversions 10: 3 conversions 11: 4 conversions
19:15	JSEQ4[4:0]	This is the 4th conversion in the injected sequence. These bits are software-defined as the number (0 to 18) of the fourth transition channel in the *conversion* sequence. *Note: Different from regular conversion sequences, if the length of ADC_JSEQ.JLEN[1:0] is less than 4, the sequence of conversion starts from (4-JLEN). For example, ADC_JSEQ[21:0] = 10 00011 00011 00111 00010 means that the scan conversion will be converted in the following channel order: 7, 3, 3 instead of 2, 7, 3.*
14:10	JSEQ3[4:0]	3rd conversion in injected sequence
9:5	JSEQ2[4:0]	2nd conversion in injected sequence
4:0	JSEQ1[4:0]	1st conversion in injected sequence

9.12.14 ADC Injection Data Register x (ADC_JDATx) (x= 1…4)

Address offset: 0x3C - 0x48

Reset value: 0x0000 0000



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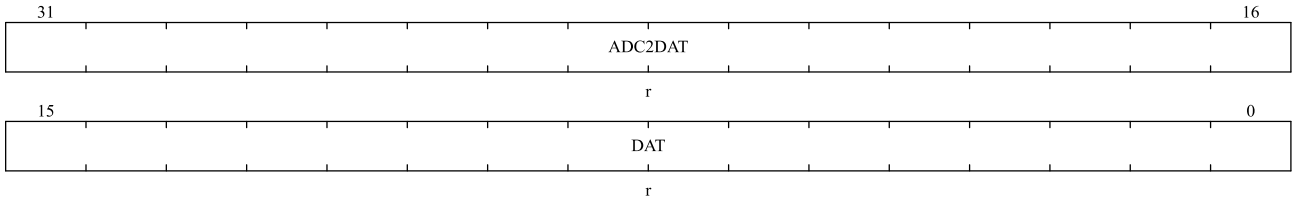
Bit field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained
15:0	JDAT[15:0]	Injected data for conversions These bits are read-only and contain the conversion results of the injected channel. The data is left-aligned or right-aligned

9.12.15 ADC Regulars Data Register (ADC_DAT)

Address offset: 0x4C

Reset value: 0x0000 0000

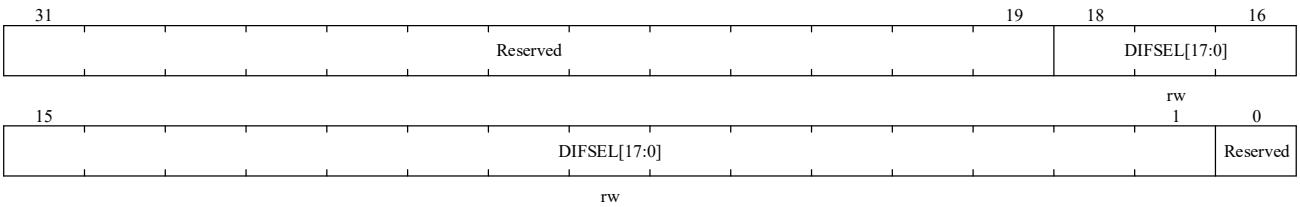


Bit field	Name	Description
31:16	ADC2DAT[15:0]	Data converted by ADC2/ADC4 (ADC2 data, ADC4 data) In ADC1 and ADC3: In dual ADC mode, these bits contain the regular channel data converted by ADC2 and ADC4. In ADC2 and ADC4: These bits are not used.
15:0	DAT[15:0]	Regular data for conversion These bits are read-only and contain the conversion results of the regular channel. The data is left-aligned or right-aligned as shown in Table 9-3 and Table 9-4.

9.12.16 ADC Differential Mode Selection Register (ADC_DIFSEL)

Address offset: 0x50

Reset value: 0x0000 0000



Bit field	Name	Description
31:19	Reserved	Reserved, the reset value must be maintained
18:1	DIFSEL[17:0]	Differential mode for channels 18 to 1 DIFSEL[i] = 0: ADC channel input i+1 is configured in single-ended mode; DIFSEL[i] = 1: ADC channel input i+1 is configured in differential mode

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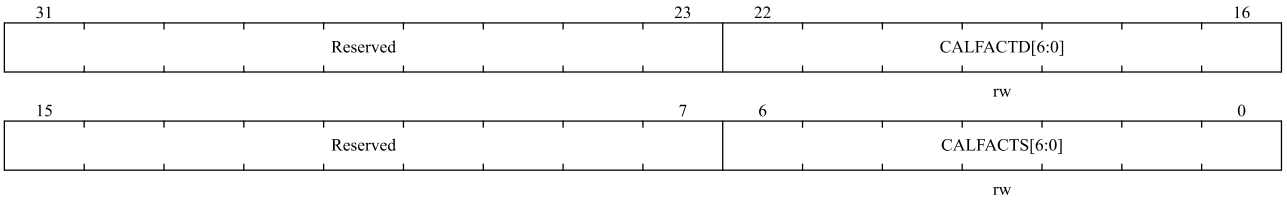
Bit field	Name	Description
0	Reserved	Reserved, the reset value must be maintained

9.12.17 ADC Calibration Factor (ADC_CALFACT)

Address offset: 0x54

Reset value: 0x0000 0000



Bit field	Name	Description
31:23	Reserved	Reserved, the reset value must be maintained
22:16	CALFACTD[6:0]	Calibration factors in differential mode This bit can be written by hardware or software After the differential input calibration is complete, the hardware will update it according to the calibration coefficient. Software can write these bits with a new calibration factor. If the new calibration coefficient is different from the current coefficient stored in the analog ADC, the coefficient will be applied after a new differential calibration is initiated. *Note: software allows write only when ADC_CTRL2.ON=1, ADC_STS.STR =0, ADC_STS.JSTR =0 (ADC does not process conversion or start conversion)*
15:7	Reserved	Reserved, the reset value must be maintained
6:0	CALFACTS[6:0]	Calibration factors in Single-Ended mode This bit can be written by hardware or software After the single-end input calibration is completed, the hardware will update it according to the calibration coefficient. Software can write these bits with a new calibration factor. If the new calibration coefficient is different from the current coefficient stored in the analog ADC, the coefficient will be applied after a new single-ended calibration is initiated. *Note: software allows write only when ADC_CTRL2.ON=1, ADC_STS.STR =0, ADC_STS.JSTR =0 (ADC does not process conversion or start conversion)*

9.12.18 ADC Control Register 3 (ADC_CTRL3)

Address offset: 0x58

Reset value: 0x0000 0043

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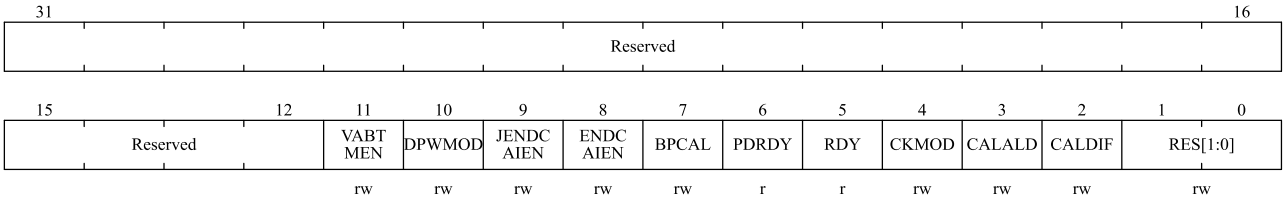

Bit field	Name	Description
31:12	Reserved	Reserved, the reset value must be maintained
11	VBATMEN	Vbat monitor enable 0: Disable 1: Enable
10	DPWMOD	Deep power mode 0: When the ADC is disabled, the ADC enters low power mode 1: When the ADC is disabled, the ADC enters deep sleep mode
9	JENDCAIEN	Interrupt enable for any injected channels This bit is set and cleared by the software to enable/disable the injection channel conversion end interrupt 0: ADC_STS.JENDCA interrupt is disabled 1: ADC_STS.JENDCA interrupt is enabled
8	ENDCAIEN	Interrupt enable for any regular channels This bit is set and cleared by the software to enable/disable any channel conversion end interrupt 0: ADC_STS.ENDCA interrupt is disabled 1: ADC_STS.ENDCA interrupt is enabled
7	BPCAL	Bypass calibration 0: Disable 1: Enabled
6	PDRDY	ADC power down ready 0: Not ready 1: Get ready
5	RDY	ADC ready 0: Not ready 1: Get ready
4	CKMOD	Clock mode 0: Select AHB for synchronization clock 1: Select PLL for asynchronous clock
3	CALALD	Calibration auto load 0: Disables automatic loading 1: Enables automatic loading
2	CALDIF	Differential mode for calibration This bit is set and cleared by software to configure the calibrated single-ended or differential input mode 0: Writing ADC_CTRL2.ENCAL bits will start calibration in single-ended input mode 1: Writing ADC_CTRL2.ENCAL bits will start calibration in differential input mode

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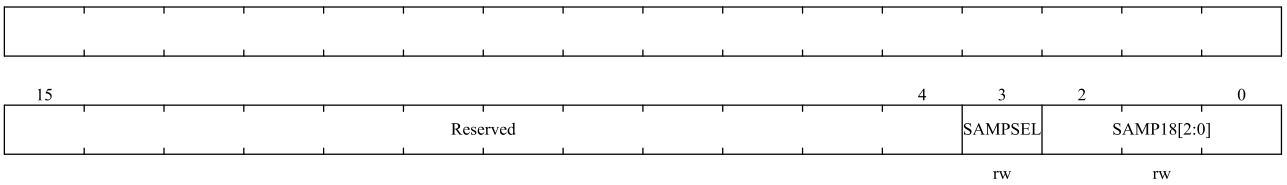
Bit field	Name	Description
1:0	RES[1:0]	Data resolution This bit is set and cleared by the software to select the resolution of the conversion 00: 6-bits 01: 8-bits 10: 10-bits 11: 12-bits

9.12.19 ADC Sampling Time Register 3 (ADC_SAMPT3)

Address offset: 0x5C

Reset value: 0x0000 0000



Bit field	Name	Description
31:4	Reserved	Reserved, the reset value must be maintained
3	SAMPSEL	Sample Time Selection When SAMPSEL = 0, the value of SAMPx[2:0] is set as follows: 000: 1.5 cycles 100: 41.5 cycles 001: 7.5 cycles 101: 55.5 cycles 010: 13.5 cycles 110: 71.5 cycles 011: 28.5 cycles 111: 239.5 cycles When SAMPSEL = 1, the value of SAMPx[2:0] is set as follows: 000: 1.5 cycles 100: 19.5 cycles 001: 2.5 cycles 101: 61.5 cycles 010: 4.5 cycles 110: 181.5 cycles 011: 7.5 cycles 111: 601.5 cycles
2:0	SAMP18[2:0]	Channel Sample Time The channel sampling time definition is consistent with ADC_SAMPT2

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10 Digital to Analog Conversion (DAC)

10.1 Introduction

DAC is a digital/analog converter, mainly digital input, voltage output.DAC data can be 8-bit or 12-bit and supports DMA functionality.When the DAC is configured in 12-bit mode, the DAC data can be right-aligned or left-aligned.When the DAC is configured in 8-bit mode, the DAC data can be right-aligned.The DAC output channel has 2, with independent converter. Both channels can be configured to convert independently or to convert simultaneously and update the output simultaneously.VREF+ is used as the DAC reference voltage through the pin input to make the DAC conversion data more accurate.

10.2 Main Features

- Two independent DAC converter, corresponding to two output channel.
- Monotonous output.
- Support 8-bit or 12-bit output, data in 12-bit mode right-aligned and left-aligned two modes.
- Synchronous update.
- DMA support.
- Noise wave, triangular waveform generation.
- Input reference voltage V_{REF+}.
- External event triggers the conversion.
- Two DAC channels are synchronized or converted independently.

DAC block diagram and pins are shown below.

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Figure 10-1 Block diagram of a DAC channel

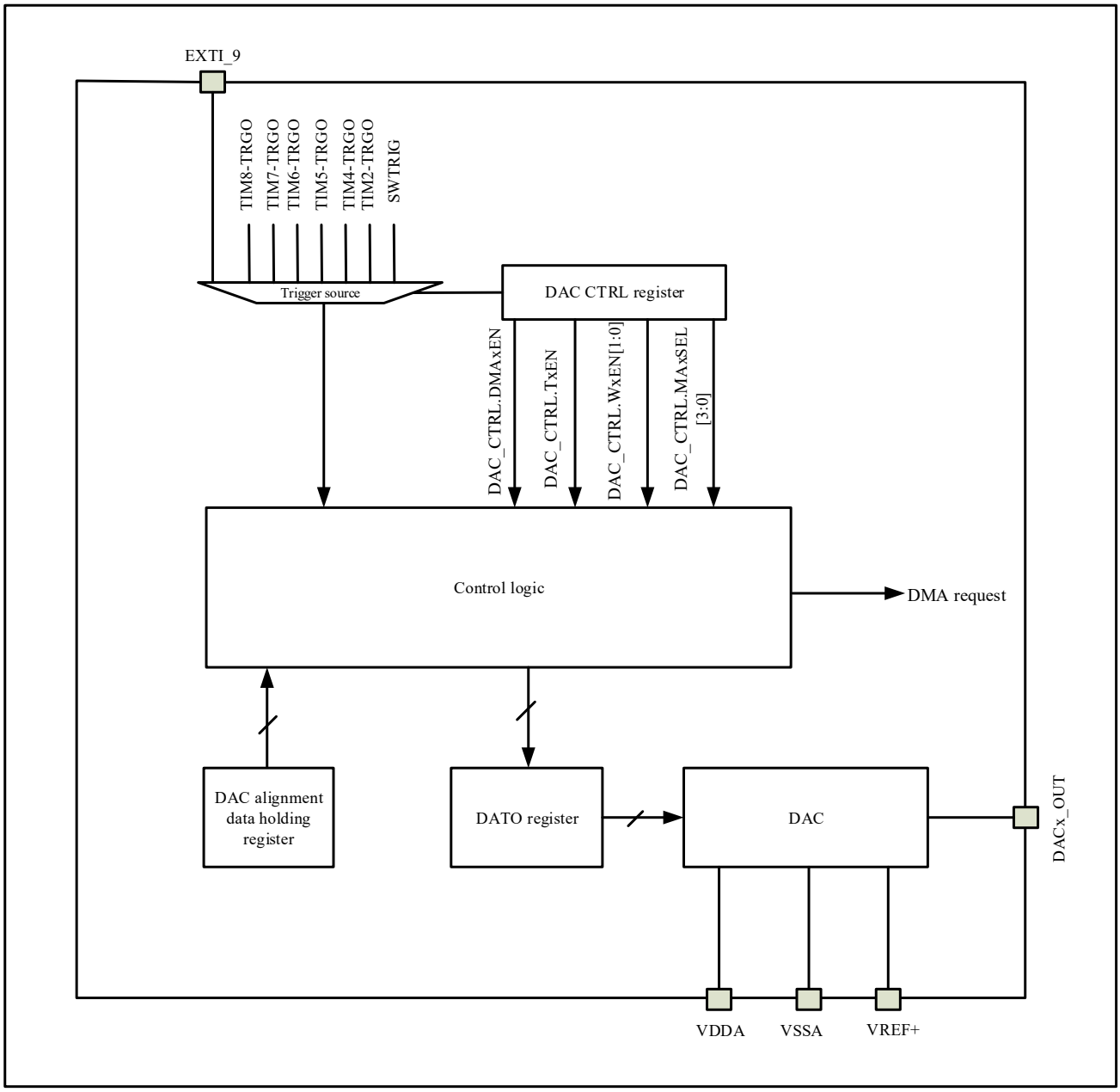

Table 10-1 DAC pins

Name	Description	Type
V_{REF+}	The positive reference voltage used by the DAC,2.4V≤V_{REF+}≤V_{DDA}（3.3V）	Input, positive analog reference voltage
V_{DDA}	Analog power	Input, analog power
V_{SSA}	Analog power ground	Input, analog power ground
DACx_OUT	DAC analog output	Analog output signal

Note: When the DACx is enabled, PA4 or PA5 needs to be configured as analog input mode. PA4 or PA5 will automatically connect to the output of the DACx.

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10.3 DAC Function Description and Operation Description

10.3.1 DAC Enable

Powering on the DAC can be done by configuring DAC_CTRL. CHxEN = 1. It takes some time for t_{WAKEUP} to open the DAC.

10.3.2 DAC Output Buffer

By configuring DAC_CTRL.BxEN to disable or enable the output buffer of DAC, if the output buffer is enable, the output impedance is reduced, the driving ability is enhanced, and the external load can be driven without the external operational amplifier.

10.3.3 DAC Data Format

According to the data alignment configuration, the corresponding registers of the data configuration are as follows:

When the DAC outputs independently, there are 3 cases:

- When the configuration data is written to the DAC_DR12CHx register, the data is written to DAC_DR12CHx [11:0], and the 12-bit data is right-aligned. (Actually stored in the register DACCHxD [11:0] bits, DACCHxD is the internal data storage register)
- When the configuration data is written to the DAC_DL12CHx register, the data is written to DAC_DL12CHx [15:4], and the 12-bit data is left-aligned. (Actually stored in the register DACCHxD [11:0] bits, DACCHxD is the internal data storage register)
- When the configuration data is written to the DAC_DR8CHx register, the data is written to DAC_DR8CHx [7:0], and the 8-bit data is right-aligned. (Actually stored in the register DACCHxD[11:4] bits, DACCHxD is the internal data storage register)

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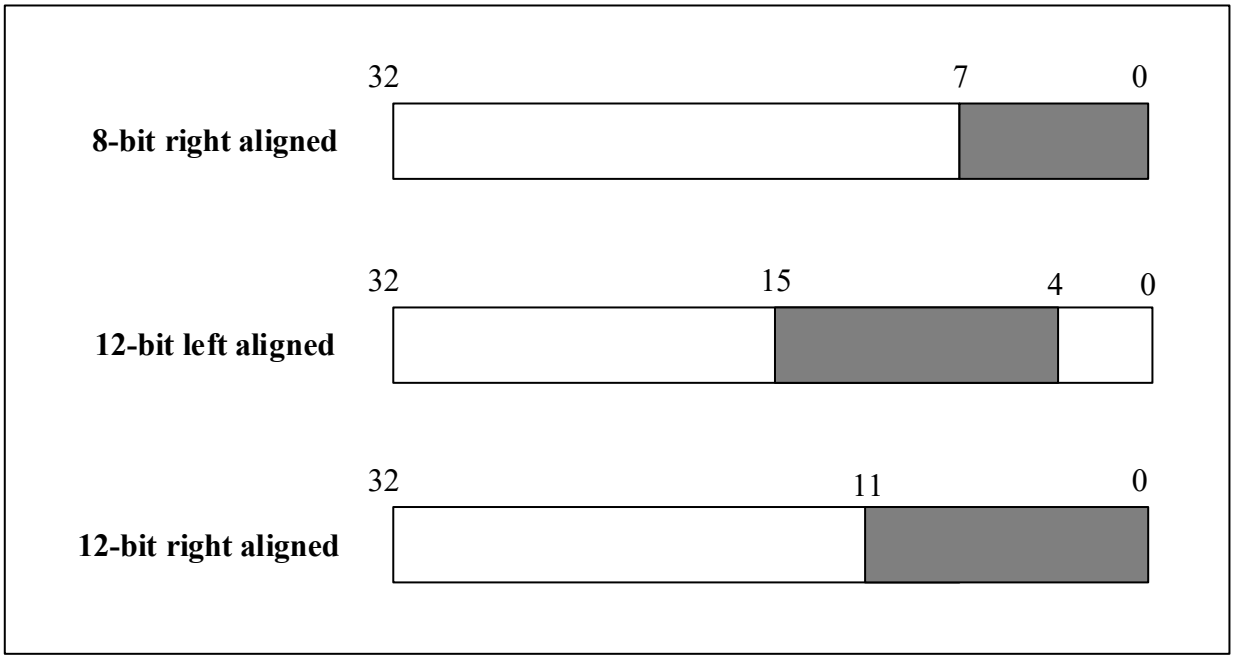
Figure 10-2 Data format when DAC independent output



When the DAC outputs synchronously, there are 3 cases:

- When the configuration data is written to the DAC_DR12DCH register, the DAC1 data is written to DAC_DR12DCH [11:0] (Actually stored in the register DACCH1D [11:0] bits, DACCH1D is the internal data storage register), the DAC2 data is written to DAC_DR12DCH [27:16] (Actually stored in the register DACCH2D [11:0] bits, DACCH2D is the internal data storage register).
- When the configuration data is written to the DAC_DR12DCH register, the DAC1 data is written to DAC_DR12DCH [15:4] (Actually stored in the register DACCH1D [11:0] bits, DACCH1D is the internal data storage register), the DAC2 data is written to DAC_DR12DCH [31:20] (Actually stored in the register DACCH2D [11:0] bits, DACCH2D is the internal data storage register).
- When the configuration data is written to the DAC_DR8DCH register, the DAC1 data is written to DAC_DR8DCH [7:0] (Actually stored in the register DACCH1D [11:4] bits, DACCH1D is the internal data storage register), the DAC2 data is written to DAC_DR8DCH [15:8] (Actually stored in the register DACCH2D [11:4] bits, DACCH2D is the internal data storage register).

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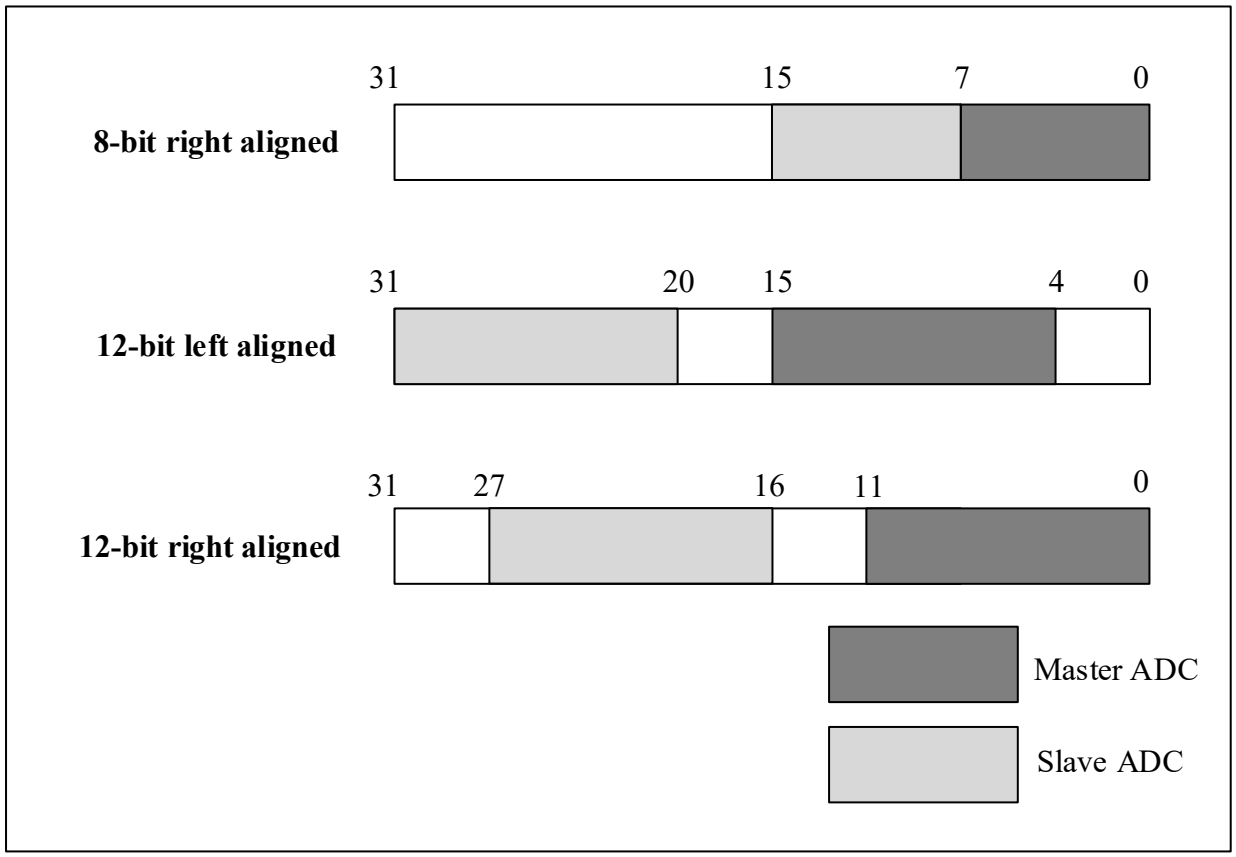
Figure 10-3 Data format for DAC sync output



10.3.4 DAC Trigger

Configure DAC_CTRL. TEN = 1 enables the external trigger of the DAC, and DAC_CTRL.TxSEL [2:0] is configured to select an external triggering event as the external triggering source for the DAC.

Table 10-2 DAC external trigger

Trigger source	Type	TSEL[2:0]
Timer 6 TRGO events	Internal signal from the on-chip timer	000
Timer 8 TRGO events		001
Timer 7 TRGO events		010
Timer 5 TRGO events		011
Timer 2 TRGO events		100
Timer 4 TRGO events		101
EXTI line 9	External pins	110
SWTRIG (Software Triggered)	Software control bit	111

When the DAC is triggered by timer output or the rising edge of EXTI line 9, when triggered, the data in the aligned data hold register will be transferred to the DAC_DATOx register. This data transfer process takes 3 APB1 clock cycles.

DAC_SOTTR.TRxEN = 1 can enable the DAC software trigger. When the DAC is triggered by the software, the

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data of the aligned data hold register will be transmitted to the DAC_DATOx register.

Note:

1. Do not change the DAC_CTRL.TxSEL[2:0] bit when the DAC is enabled.

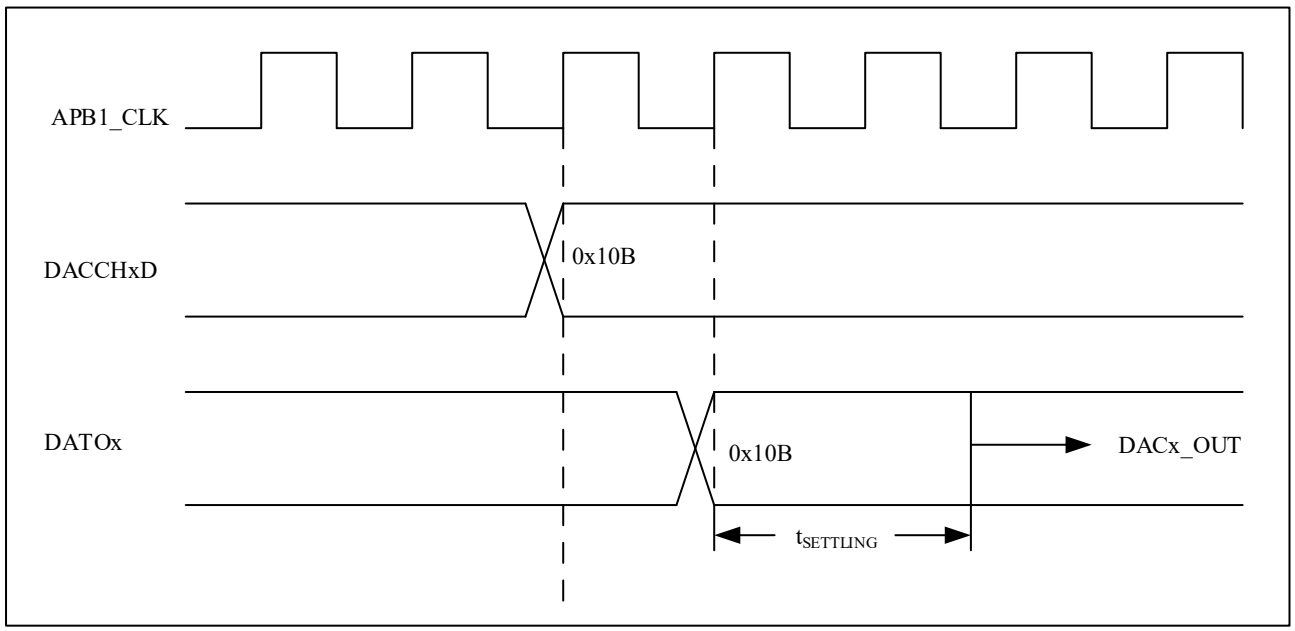
2. It takes 1 APB1 clock cycle for the data of the aligned data holding register to be transferred to the DAC_DATOx register when triggered by software..

10.3.5 DAC Conversion

If DAC trigger is on, the data in the DAC alignment data hold register will be transferred to the DAC_DATOx register after three APB1 cycles according to the selected trigger event when the hardware trigger occurs. When the software trigger occurs, the data in the DAC alignment data hold register is transferred to the DAC_DATOx register after one APB1 cycle..

After the DAC transfers data to the DAC_DATOx register from its data hold register, the output is valid for the time $t_{SETTTLING}$, which is related to the supply voltage and the analog output load.

Figure 10-4 Time diagram of transitions with trigger disabled



10.3.6 DAC Output Voltage

The digital input is converted to analog voltage output by a DAC module in a linear relationship ranging from 0 to V_{REF+}.The output voltage of DAC is calculated as follows:

DAC output = V_{REF} X (DATO / 4095).

10.3.7 DMA Requests

DAC_CTRL.DMAxEN = 1 is configured to enable DMA function. 2 DMA channels correspond to two DACs respectively.When an external trigger occurs (not a software trigger), a DMA request is generated and the data aligned

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with the data hold register is then transferred to the DAC_DATOx register.

When the dual DAC mode is turned on, only one DMA is needed to transmit data, so only one DAC is used to turn on the DMA function, and two DMA requests will appear when two DACs are turned on.

Note: DMA requests for DAC have no accumulative function, and when the second external trigger occurs before the response to the first external trigger, the second DMA request cannot be processed and there is no error reporting mechanism.

10.3.8 Noise

DAC can generate noise, by configuring DAC_CTRL.WxEN[1:0] to "01" to turn on the noise function, by configuring DAC_CTRL.MAxSEL[3:0] to select which bits of the linear feedback shift register (LFSR) are masked, the value of LFSR is added to the value of the DAC alignment data holding register and written to the DAC_DATOx register (overflow bits are discarded). The initial value of LFSR is 0xAAA, and the value of LFSR is updated after 3 APB1 cycles after the trigger event occurs.

Figure 10-5 LFSR algorithm for DAC

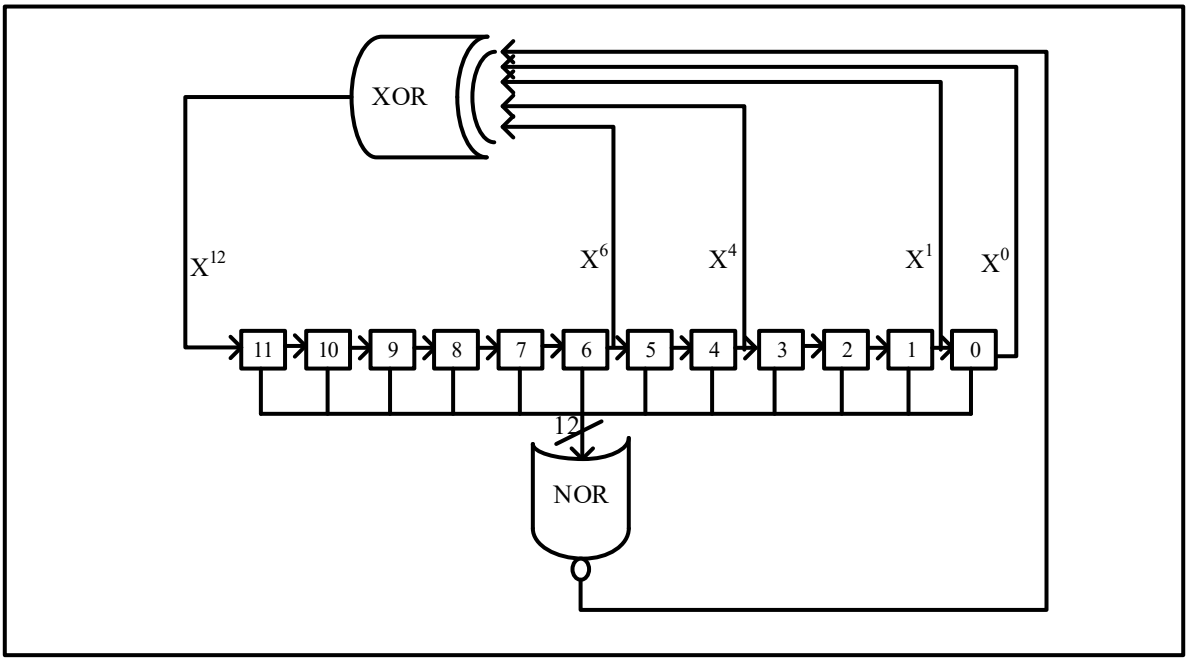

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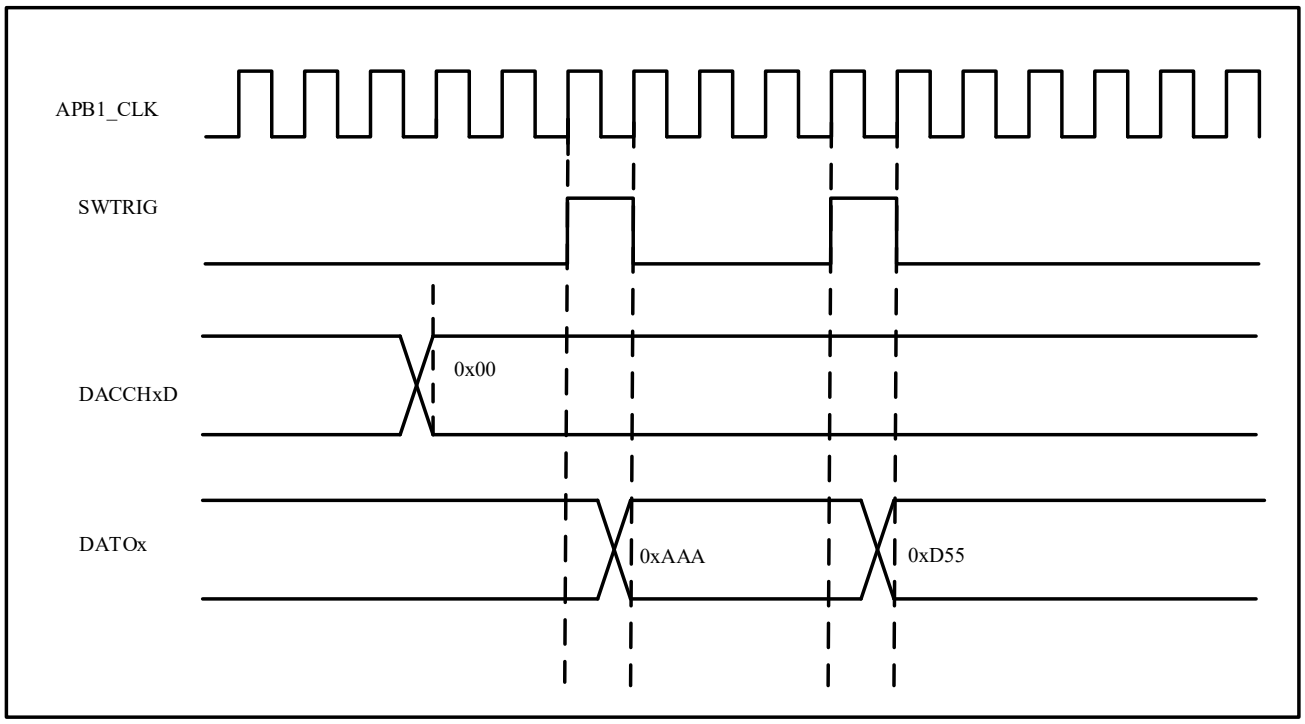
Figure 10-6 DAC conversion with LFSR waveform generation (enable software trigger)



Note: The DAC is configured to trigger to generate noise.

10.3.9 Triangular Wave Generation

The DAC can generate a triangle wave. The triangle wave function can be turned on by configuring DAC_CTRL.WxEN[1:0] as "10", and the amplitude of the triangle wave can be selected by configuring DAC_CTRL.MAxSEL[3:0]. The value of the internal triangle wave counter is added to the value of the DAC alignment data holding register and written to the DAC_DATOx register (overflow bits are discarded).The value of the triangular wave counter is updated 3 APB1 cycles after the trigger event occurs, the triangular wave counter will accumulate to the maximum amplitude value set, and then decrement to 0, and so on.

Figure 10-7 Triangle wave generation of DAC

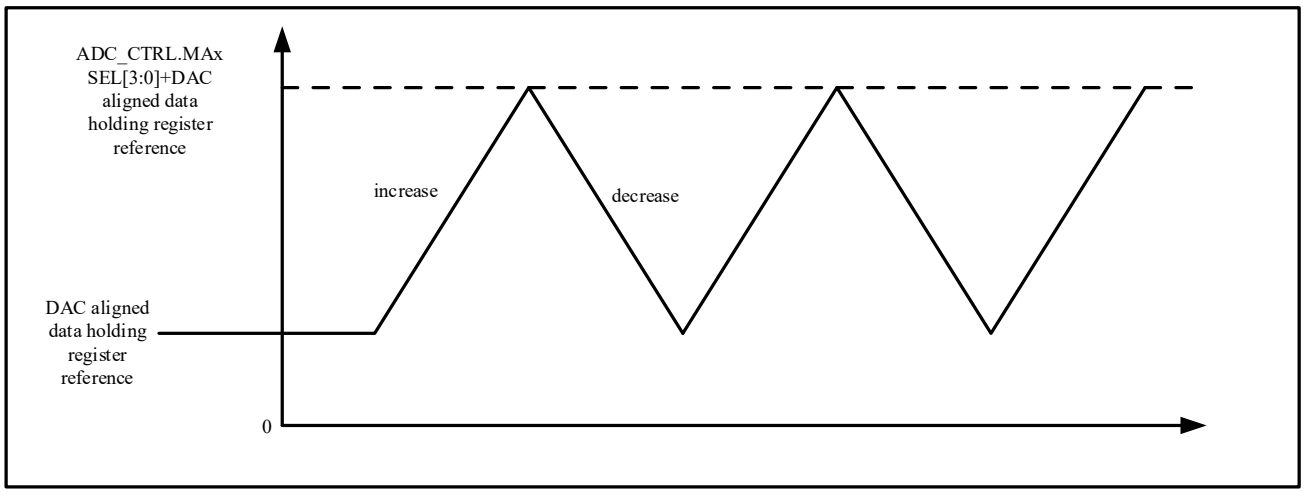


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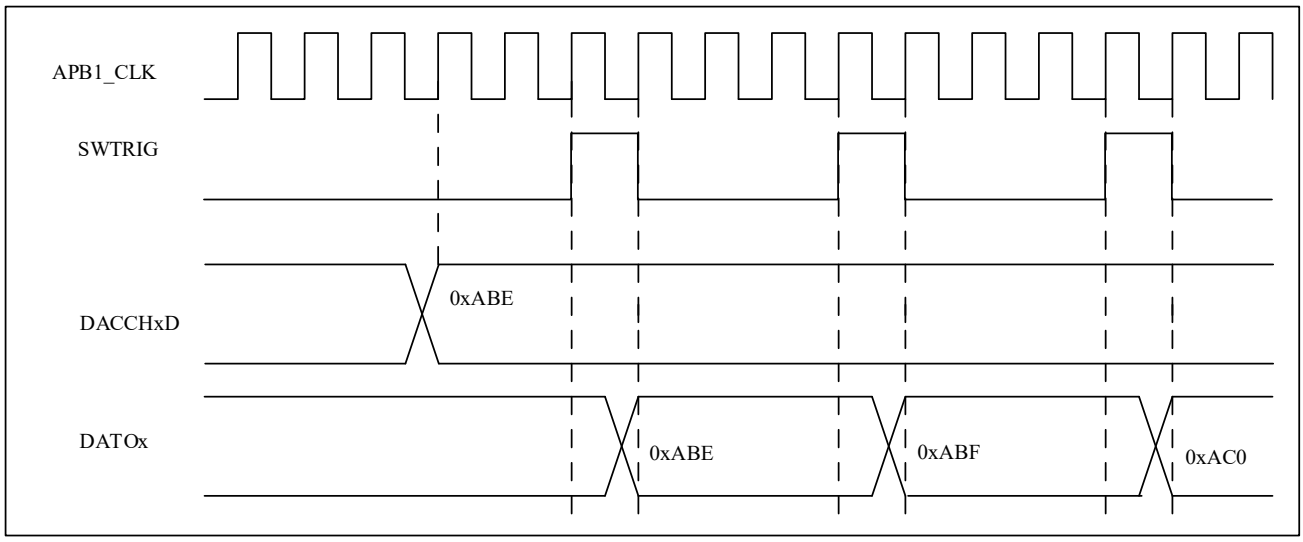
Figure 10-8 DAC conversion with trigonometry generation (enable software trigger)



Notes:

1. Only when the DAC is configured to trigger can the triangle wave be generated

2. DAC_CTRL.MAxSEL[3:0] cannot be set after DAC is enabled.

10.4 DAC Dual-channel Conversion

The two channels of the DAC can work independently or at the same time. In this mode, a total of 3 registers, DAC_DR12DCH, DAC_DL12DCH and DAC_DR8DCH, can be used, which can efficiently utilize the bus bandwidth, and each register can operate on 2 DACs at the same time.

The dual DAC channels turn on the conversion at the same time. There are 11 modes in total. When only one DAC is used for conversion, the other DAC can still operate independently. For details, please refer to the following chapter description.

10.4.1 Independent Trigger without Waveform Generator

The configuration process is as follows:

- Configure DAC_CTRL.T1EN and DAC_CTRL.T2EN to enable trigger enable of DAC1 and DAC2.
- Configure DAC_CTRL.T1SEL[2:0] and DAC_CTRL.T2SEL[2:0] as different values to select different trigger sources.
- Put the data to be converted into the corresponding alignment data holding register.

When the DAC1 trigger event occurs, the value of the aligned data holding register will be transferred to the register DAC_DATO1 after a delay of 3 APB1 clock cycles. When the DAC2 trigger event occurs, the value of the aligned data holding register will be transferred to the register DAC_DATO2 after a delay of 3 APB1 clock cycles.

10.4.2 Independent Triggers Producing Same Noise

The configuration process is as follows:

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- Configure DAC_CTRL.T1EN and DAC_CTRL.T2EN to enable trigger enable of DAC1 and DAC2.
- Configure DAC_CTRL.T1SEL[2:0] and DAC_CTRL.T2SEL[2:0] as different values to select different trigger sources.
- Configure DAC_CTRL.W1EN[1:0] and DAC_CTRL.W2EN[1:0] as “01” to select noise generation enable.
- Configure DAC_CTRL.MA1SEL3:0] and DAC_CTRL.MA2SEL3:0] to the same value to get the same LFSR register mask bit.
- Put the data to be converted into the corresponding alignment data holding register.

When the DAC1 trigger event occurs, the counter value of the LFSR register 1 is added to the value of the corresponding data holding register. The added value is transferred to the register DAC_DATO1 after a delay of 3 APB1 clock cycles, and the counter value of the LFSR register 1 will be updated at this time. When the DAC2 trigger event occurs, the counter value of the LFSR register 2 is added to the value of the corresponding data holding register. The added value is transferred to the register DAC_DATO2 after a delay of 3 APB1 clock cycles, and the counter value of the LFSR register 2 will be updated at this time.

10.4.3 Independent Triggers Generate Different Noises

The configuration process is as follows:

- Configure DAC_CTRL.T1EN and DAC_CTRL.T2EN to enable trigger enable of DAC1 and DAC2.
- Configure DAC_CTRL.T1SEL[2:0] and DAC_CTRL.T2SEL[2:0] as different values to select different trigger sources.
- Configure DAC_CTRL.W1EN[1:0] and DAC_CTRL.W2EN[1:0] as “01” to select noise generation enable.
- Configure DAC_CTRL.MA1SEL3:0] and DAC_CTRL.MA2SEL3:0] as different values to get different LFSR register mask bits.
- Put the data to be converted into the corresponding alignment data holding register.

When the DAC1 trigger event occurs, the counter value of the LFSR register 1 is added to the value of the corresponding data holding register. The added value is transferred to the register DAC_DATO1 after a delay of 3 APB1 clock cycles, and the counter value of the LFSR register 1 will be updated at this time. When the DAC2 trigger event occurs, the counter value of the LFSR register 2 is added to the value of the corresponding data holding register. The added value is transferred to the register DAC_DATO2 after a delay of 3 APB1 clock cycles, and the counter value of the LFSR register 2 will be updated at this time.

10.4.4 Independent Triggers Generate Same Triangle Wave

The configuration process is as follows:

- Configure DAC_CTRL.T1EN and DAC_CTRL.T2EN to enable trigger enable of DAC1 and DAC2.
- Configure DAC_CTRL.T1SEL[2:0] and DAC_CTRL.T2SEL[2:0] as different values to select different trigger sources.
- Configure DAC_CTRL.W1EN[1:0] and DAC_CTRL.W2EN[1:0] as “1x” to select the triangle wave generation enable.

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- Configure DAC_CTRL.MA1SEL3:0] and DAC_CTRL.MA2SEL3:0] to the same value to get the same triangle wave amplitude.
- Put the data to be converted into the corresponding alignment data holding register.

When the DAC1 trigger event occurs, the triangular wave amplitude value of DAC1 is added to the corresponding data holding register value. The added value is transferred to the register DAC_DATO1 after a delay of 3 APB1 clock cycles, and the counter value of the triangular wave of DAC1 will be updated at this time. When the DAC2 trigger event occurs, the triangular wave amplitude value of DAC2 is added to the value of the corresponding data holding register. The added value is transferred to the register DAC_DATO2 after a delay of 3 APB1 clock cycles, and the counter value of the triangular wave of DAC2 will be updated at this time.

10.4.5 Independent Trigger Generate Different Triangle Waves

The configuration process is as follows:

- Configure DAC_CTRL.T1EN and DAC_CTRL.T2EN to enable trigger enable of DAC1 and DAC2.
- Configure DAC_CTRL.T1SEL[2:0] and DAC_CTRL.T2SEL[2:0] as different values to select different trigger sources.
- Configure DAC_CTRL.W1EN[1:0] and DAC_CTRL.W2EN[1:0] as “1x” to select the triangle wave generation enable.
- Configure DAC_CTRL.MA1SEL3:0] and DAC_CTRL.MA2SEL3:0] as different values to get different triangle wave amplitudes.
- Put the data to be converted into the corresponding alignment data holding register.

When the DAC1 trigger event occurs, the triangular wave amplitude value of DAC1 is added to the corresponding data holding register value. The added value is transferred to the register DAC_DATO1 after a delay of 3 APB1 clock cycles, and the counter value of the triangular wave of DAC1 will be updated at this time. When the DAC2 trigger event occurs, the triangular wave amplitude value of DAC2 is added to the value of the corresponding data holding register. The added value is transferred to the register DAC_DATO2 after a delay of 3 APB1 clock cycles, and the counter value of the triangular wave of DAC2 will be updated at this time.

10.4.6 Simultaneous Software Startup

The configuration process is as follows:

- Configure DAC_CTRL.T1EN and DAC_CTRL.T2EN to enable trigger enable of DAC1 and DAC2.
- Configure DAC_CTRL.TR1EN and DAC_CTRL.TR2EN to select software trigger.
- Put the data to be converted into the corresponding alignment data holding register.

The value of the aligned data holding register of DAC1 will be transferred into register DAC_DATO1 after a delay of 1 APB1 clock cycle.

The value of the aligned data holding register of DAC2 will be transferred to register DAC_DATO2 after a delay of 1 APB1 clock cycle.

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10.4.7 Synchronous Trigger without Waveform Generator

The configuration process is as follows:

- Configure DAC_CTRL.T1EN and DAC_CTRL.T2EN to enable trigger enable of DAC1 and DAC2.
- Configure DAC_CTRL.T1SEL[2:0] and DAC_CTRL.T2SEL[2:0] to be the same value to select the same trigger source.
- Put the data to be converted into the corresponding alignment data holding register.

When a trigger event occurs, the value of the alignment data holding register of DAC1 will be transferred to the register DAC_DATO1 after a delay of 3 APB1 clock cycles; the value of the alignment data holding register of DAC2 will be transferred to the register DAC_DATO2 after a delay of 3 APB1 clock cycles.

10.4.8 Synchronous Triggers Generate Same Noise

The configuration process is as follows:

- Configure DAC_CTRL.T1EN and DAC_CTRL.T2EN to enable trigger enable of DAC1 and DAC2.
- Configure DAC_CTRL.T1SEL[2:0] and DAC_CTRL.T2SEL[2:0] to be the same value to select the same trigger source.
- Configure DAC_CTRL.W1EN[1:0] and DAC_CTRL.W2EN[1:0] as “01” to select noise generation enable.
- Configure DAC_CTRL.MA1SEL3:0] and DAC_CTRL.MA2SEL3:0] to the same value to get the same LFSR register mask bit.
- Put the data to be converted into the corresponding alignment data holding register.

When a trigger event occurs, the counter value of LFSR register 1 is added to the value of the corresponding data holding register. The added value is transferred to register DAC_DATO1 after a delay of 3 APB1 clock cycles, and the counter value of LFSR register 1 will be updated at this time; LFSR The counter value of register 2 is added to the value of the corresponding data holding register. The added value is transferred to register DAC_DATO2 after a delay of 3 APB1 clock cycles, and the counter value of LFSR register 2 will be updated at this time.

10.4.9 Synchronous Triggers Generate Different Noises

The configuration process is as follows:

- Configure DAC_CTRL.T1EN and DAC_CTRL.T2EN to enable trigger enable of DAC1 and DAC2.
- Configure DAC_CTRL.T1SEL[2:0] and DAC_CTRL.T2SEL[2:0] as different values to select different trigger sources.
- Configure DAC_CTRL.W1EN[1:0] and DAC_CTRL.W2EN[1:0] as “01” to select noise generation enable.
- Configure DAC_CTRL.MA1SEL3:0] and DAC_CTRL.MA2SEL3:0] to the same value to get the same LFSR register mask bit.
- Put the data to be converted into the corresponding alignment data holding register.

When a trigger event occurs, the counter value of LFSR register 1 is added to the value of the corresponding data

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holding register. The added value is transferred to register DAC_DATO1 after a delay of 3 APB1 clock cycles, and the counter value of LFSR register 1 will be updated at this time; LFSR The counter value of register 2 is added to the value of the corresponding data holding register. The added value is transferred to register DAC_DATO2 after a delay of 3 APB1 clock cycles, and the counter value of LFSR register 2 will be updated at this time.

10.4.10 Synchronous trigger Generate Same Triangle Wave

The configuration process is as follows:

- Configure DAC_CTRL.T1EN and DAC_CTRL.T2EN to enable trigger enable of DAC1 and DAC2.
- Configure DAC_CTRL.T1SEL[2:0] and DAC_CTRL.T2SEL[2:0] to be the same value to select the same trigger source.
- Configure DAC_CTRL.W1EN[1:0] and DAC_CTRL.W2EN[1:0] as "1x" to select the triangle wave generation enable.
- Configure DAC_CTRL.MA1SEL3:0] and DAC_CTRL.MA2SEL3:0] to the same value to get the same triangle wave amplitude.
- Put the data to be converted into the corresponding alignment data holding register.

When a trigger event occurs, the triangular wave amplitude value of DAC1 is added to the value of the corresponding data holding register. The added value is transferred to the register DAC_DATO1 after a delay of 3 APB1 clock cycles, and the counter value of the triangular wave of DAC1 will be updated at this time; The triangular wave amplitude is added to the value of the corresponding data holding register. The added value is transferred to the register DAC_DATO2 after a delay of 3 APB1 clock cycles, and the counter value of the triangular wave of DAC2 will be updated at this time.

10.4.11 Synchronous Trigger Generate Different Triangle Waves

The configuration process is as follows:

- Configure DAC_CTRL.T1EN and DAC_CTRL.T2EN to enable trigger enable of DAC1 and DAC2.
- Configure DAC_CTRL.T1SEL[2:0] and DAC_CTRL.T2SEL[2:0] to be the same value to select the same trigger source.
- Configure DAC_CTRL.W1EN[1:0] and DAC_CTRL.W2EN[1:0] as "1x" to select the triangle wave generation enable.
- Configure DAC_CTRL.MA1SEL3:0] and DAC_CTRL.MA2SEL3:0] as different values to get different triangle wave amplitudes.
- Put the data to be converted into the corresponding alignment data holding register.

When a trigger event occurs, the triangular wave amplitude value of DAC1 is added to the value of the corresponding data holding register. The added value is transferred to the register DAC_DATO1 after a delay of 3 APB1 clock cycles, and the counter value of the triangular wave of DAC1 will be updated at this time; The triangular wave amplitude is added to the value of the corresponding data holding register. The added value is transferred to the register DAC_DATO2 after a delay of 3 APB1 clock cycles, and the counter value of the triangular wave of DAC2 will be updated at this time.

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10.5 DAC Register

10.5.1 DAC Registers Overview

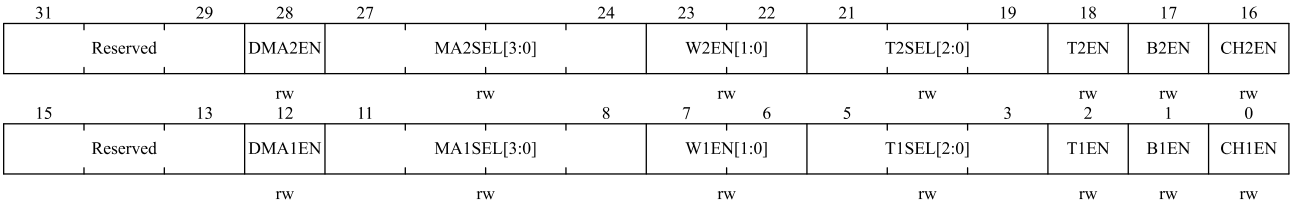
Table 10-3 DAC registers overvie

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
000h	DAC_CTRL	Reserved			DMA2EN	MA2SEL[3:0]				W2EN[1:0]		T2SEL[2:0]			T2EN	B2EN	CH2EN	Reserved			DMA1EN	MA1SEL[3:0]				W1EN[1:0]		T1SEL[2:0]			T1EN	B1EN	CH1EN
	Reset Value				0	0	0	0	0	0	0	0	0	0	0	0	0				0	0	0	0	0	0	0	0	0	0	0	0	0	0
004h	DAC_SOTTR	Reserved																														TR2EN	TR1EN
	Reset Value																															0	0
008h	DAC_DR12CH1	Reserved																				DACCH1D[11:0]											
	Reset Value																					0	0	0	0	0	0	0	0	0	0	0	0
00Ch	DAC_DL12CH1	Reserved																DACCH1D[11:0]														Reserved	
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0				
010h	DAC_DR8CH1	Reserved																								DACCH1D[7:0]							
	Reset Value																									0	0	0	0	0	0	0	0
014h	DAC_DR12CH2	Reserved																				DACCH2D[11:0]											
	Reset Value																					0	0	0	0	0	0	0	0	0	0	0	0
018h	DAC_DL12CH2	Reserved																DACCH2D[11:0]														Reserved	
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0				
01Ch	DAC_DR8CH2	Reserved																								DACCH2D[7:0]							
	Reset Value																									0	0	0	0	0	0	0	0
020h	DAC_DR12DCH	Reserved			DACCH2D[11:0]													Reserved				DACCH1D[11:0]											
	Reset Value				0	0	0	0	0	0	0	0	0	0	0	0	0					0	0	0	0	0	0	0	0	0	0	0	0
024h	DAC_DL12DCH	DACCH2D[11:0]												Reserved				DACCH1D[11:0]														Reserved	
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0					0	0	0	0	0	0	0	0	0	0	0	0				
028h	DAC_DR8DCH	Reserved																DACCH2D[7:0]								DACCH1D[7:0]							
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
02Ch	DAC_DATO1	Reserved																				DACCH1DO[11:0]											
	Reset Value																					0	0	0	0	0	0	0	0	0	0	0	0
030h	DAC_DATO2	Reserved																				DACCH2DO[11:0]											
	Reset Value																					0	0	0	0	0	0	0	0	0	0	0	0

10.5.2 DAC Control Register (DAC_CTRL)

Offset address: 0x00

Reset value: 0x0000 0000



Bit field	Name	Description
31:29	Reserved	Reserved, the reset value must be maintained.
28	DMA2EN	The DMA function of the DAC2 is enabled

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Bit field	Name	Description
		The bit is set to 1 and cleared by the software. 0: Disable DMA for the DAC2; 1: Enable the DMA function of the DAC2.
27:24	MA2SEL[3:0]	DAC2 shield/amplitude selector. These bits are configured by software to set the LFSR shielding bits for the noise function and the amplitude of the triangular wave. 0000: unmasked LFSR bit 0 / triangular amplitude equals 1; 0001: unmasked LFSR bit [1:0] / triangular amplitude equal 3; 0010: unmasked LFSR bit [2:0] / triangular amplitude equals 7; 0011: unmasked LSFR bit [3:0] / triangular amplitude equals 15; 0100: unmasked LFSR bit [4:0] / triangular amplitude equals 31; 0101: unmasked LFSR bit [5:0] / triangular amplitude equals 63; 0110: unmasked LFSR bit [6:0] / triangular amplitude equals 127; 0111: unmasked LFSR bit [7:0] / triangular amplitude equals 255; 1000: unmasked LFSR bit [8:0] / triangular amplitude equals 511; 1001: unmasked LFSR bit [9:0] / triangular amplitude equals 1023; 1010: unmasked LFSR bit [10:0] / triangular amplitude equals 2047; ≥1011: unmasked LFSR bit [11:0] / triangular amplitude equal 4095.
23:22	W2EN[1:0]	DAC2 noise/triangle wave function selection. The bits are set to 1 and cleared by the software. 00: Disable noise and triangle wave; 01: Enable the noise function; 1x: Enable the triangle wave function.
21:19	T2SEL[2:0]	DAC2 triggers selection. This bit is used for selection of DAC2 external triggers. 000: TIM6 TRGO event; 001: TIM8 TRGO event; 010: TIM7 TRGO event; 011: TIM5 TRGO event; 100: TIM2 TRGO event; 101: TIM4 TRGO event; 110: External interrupt line 9; 111: Software trigger.
18	T2EN	DAC2 trigger on This bit is set to 1 and cleared by the software to enable/disable DAC2 trigger. 0: Disable DAC2 trigger; 1: Enable DAC2 trigger.
17	B2EN	Enable the DAC2 output buffer. This bit is set to 1 and cleared by the software to enable/disable the DAC2's output buffer. 0: Disable the DAC2 output buffer; 1: Enable the DAC2 output buffer.
16	CH2EN	DAC2 on

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Bit field	Name	Description
		This bit is set to 1 and cleared by the software to enable/disable the DAC2. 0: Disable the DAC2; 1: Enable the DAC2.
15:13	Reserved	Reserved, the reset value must be maintained.
12	DMA1EN	The DMA function of the DAC1 is enabled The bit is set to 1 and cleared by the software. 0: Disable DMA for the DAC1; 1: Enable DMA for the DAC1.
11:8	MA1SEL[3:0]	DAC1 shield/amplitude selector. These bits are configured by software to set the LFSR shielding bits for the noise function and the amplitude of the triangular wave. 0000: unmasked LFSR bit 0 / triangular amplitude equals 1; 0001: unmasked LFSR LFSR bit [1:0] / triangular amplitude equal 3; 0010: unmasked LFSR bit [2:0] / triangular amplitude equals 7; 0011: unmasked LFSR bit [3:0] / triangular amplitude equals 15; 0100: unmasked LFSR bit [4:0] / triangular amplitude equals 31; 0101: unmasked LFSR bit [5:0] / triangular amplitude equals 63; 0110: unmasked LFSR bit [6:0] / triangular amplitude equals 127; 0111: unmasked LFSR bit [7:0] / triangular amplitude equals 255; 1000: unmasked LFSR bit [8:0] / triangular amplitude equals 511; 1001: unmasked LFSR bit [9:0] / triangular amplitude equals 1023; 1010: unmasked LFSR bit [10:0] / triangular amplitude equals 2047; ≥1011: unmasked LFSR bit [11:0] / triangular amplitude equal 4095.
7:6	W1EN[1:0]	DAC1 noise/triangle wave function selection. The bits are set to 1 and cleared by the software. 00: Disable noise and triangle wave; 01: Enable the noise function; 1x: Enable the triangle wave function.
5:3	T1SEL[2:0]	DAC1 triggers selection. This bit is used for selection of DAC1 external triggers. 000: TIM6 TRGO event; 001: TIM8 TRGO event; 010: TIM7 TRGO event; 011: TIM5 TRGO event; 100: TIM2 TRGO event; 101: TIM4 TRGO event; 110: External interrupt line 9; 111: Software trigger.
2	T1EN	DAC1 trigger on This bit is set to 1 and cleared by the software to enable/disable DAC2 trigger. 0: Disable DAC1 trigger; 1: Enable DAC1 trigger.
1	B1EN	Enable the DAC1 output buffer.

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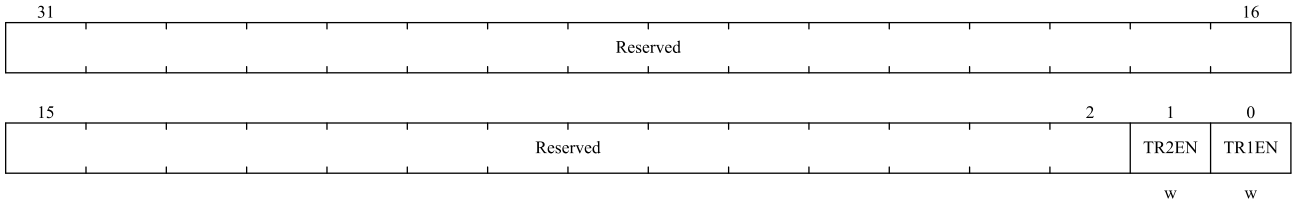
Bit field	Name	Description
		This bit is set to 1 and cleared by the software to enable/disable the DAC1's output buffer. 0: Disable the DAC1 output buffer; 1: Enable the DAC1 output buffer.
0	CH1EN	DAC1 on This bit is set to 1 and cleared by the software to enable/disable the DAC2. 0: Disable the DAC1; 1: Enable the DAC1.

10.5.3 DAC Software Trigger Register (DAC_SOTTR)

Offset address: 0x04

Reset value: 0x0000 0000



Bit field	Name	Description
31:2	Reserved	Reserved, the reset value must be maintained.
1	TR2EN	The DAC2 software trigger. This bit is setting by software to enable/disable software trigger. 0: Disable the DAC2 software trigger. 1: Enable the DAC2 software trigger. *Note: After the alignment data hold register transfers data to the DAC_DATO2 register, this bit will be cleared by the hardware after an APB1 clock.*
0	TR1EN	The DAC1 software trigger. This bit is setting by software to enable/disable software trigger. 0: Disable the DAC1 software trigger. 1: Enable the DAC1 software trigger. *Note: After the alignment data hold register transfers data to the DAC_DATO1 register, this bit will be cleared by the hardware after an APB1 clock.*

10.5.4 12-bit Right-aligned Data Hold Register for DAC1 (DAC_DR12CH1)

Offset address: 0x08

Reset value: 0x0000 0000

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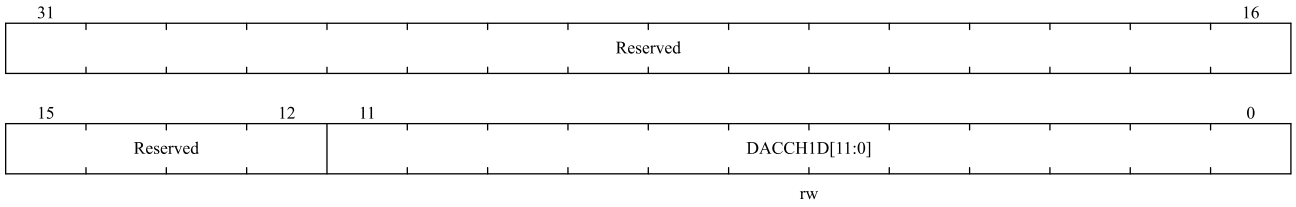
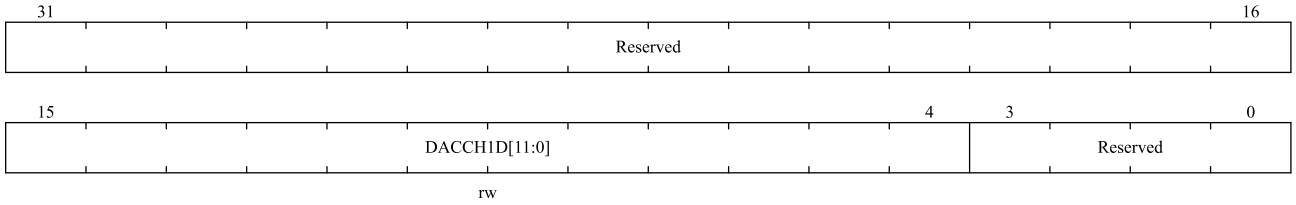


Bit field	Name	Description
31:12	Reserved	Reserved, the reset value must be maintained.
11:0	DACCH1D[11:0]	12-bit right- aligned data for DAC1 The bits are configured by the software and the DAC1 converts the data.

10.5.5 12-bit Left-aligned Data Hold Register for DAC1 (DAC_DL12CH1)

Offset address: 0x0c

Reset value: 0x0000 0000

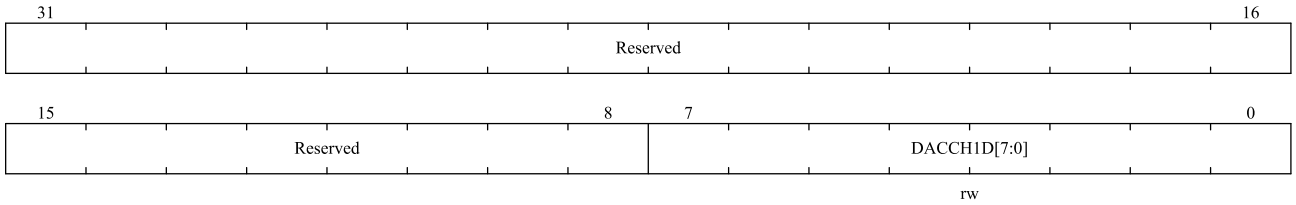


Bit field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained.
15:4	DACCH1D[11:0]	12-bit left-aligned data for DAC1 The bits are configured by the software and the DAC1 converts the data.
3:0	Reserved	Reserved, the reset value must be maintained.

10.5.6 8-bit Right-aligned Data Hold Register for DAC1 (DAC_DR8CH1)

Offset address: 0x10

Reset value: 0x0000 0000



Bit field	Name	Description
31:8	Reserved	Reserved, the reset value must be maintained.
7:0	DACCH1D[7:0]	8-bit right- aligned data for DAC1 The bits are configured by the software and the DAC1 converts the data.

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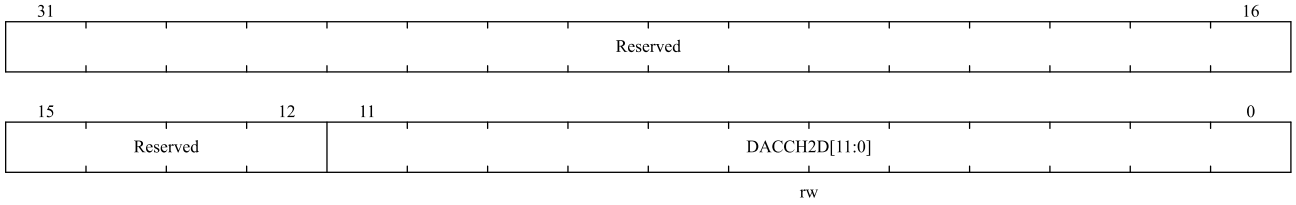
10.5.7 12-bit Right-aligned Data Hold Register for DAC2 (DAC_DR12CH2)

Offset address: 0x14

Reset value: 0x0000 0000

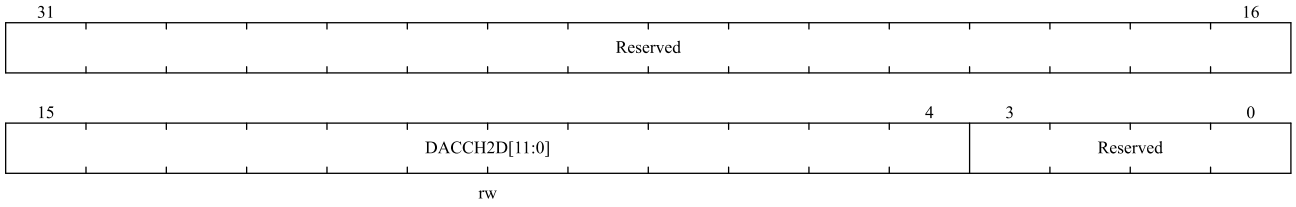


Bit field	Name	Description
31:12	Reserved	Reserved, the reset value must be maintained.
11:0	DACCH2D[11:0]	12-bit right- aligned data for DAC2 The bits are configured by the software and the DAC2 converts the data.

10.5.8 12 bit left aligned data hold register for DAC2 (DAC_DL12CH2)

Offset address: 0x18

Reset value: 0x0000 0000

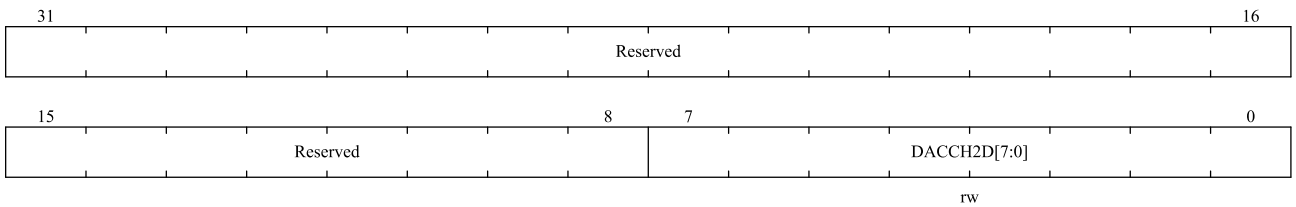


Bit field	Name	Description
31:16	Reserved	Retained, the reset value must be maintained.
15:4	DACCH2D[11:0]	12-bit left-aligned data for DAC2 The bits are configured by the software and the DAC2 converts the data.
3:0	Reserved	Retained, the reset value must be maintained.

10.5.9 8-bit Right-aligned Data Hold Register for DAC2 (DAC_DR8CH2)

Offset address: 0x1C

Reset value: 0x0000 0000



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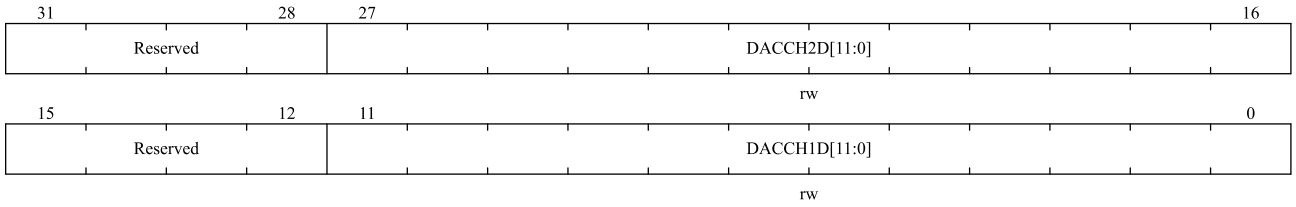
Bit field	Name	Description
31:8	Reserved	Retained, the reset value must be maintained.
7:0	DACCH2D[7:0]	8-bit right- aligned data for DAC2 The bits are configured by the software and the DAC2 converts the data.

10.5.10 12-bit Right-aligned Data Hold Register for Dual DAC (DAC_DR12DCH)

Offset address: 0x20

Reset value: 0x0000 0000

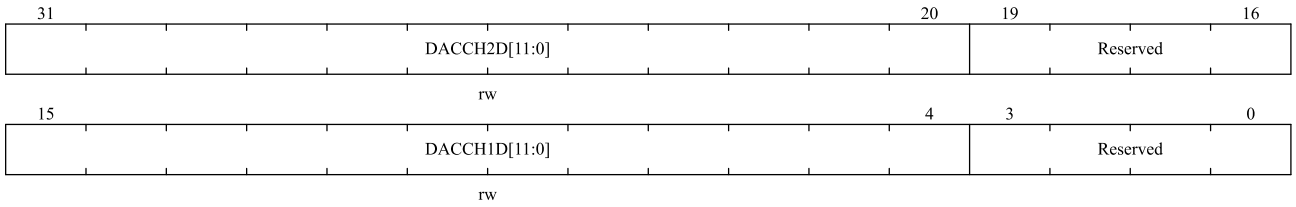


Bit field	Name	Description
31:28	Reserved	Retained, the reset value must be maintained.
27:16	DACCH2D[11:0]	12-bit right- aligned data for DAC2 The bits are configured by the software and the DAC2 converts the data.
15:12	Reserved	Retained, the reset value must be maintained.
11:0	DACCH1D[11:0]	12-bit right- aligned data for DAC1 The bits are configured by the software and the DAC1 converts the data.

10.5.11 12-bit left aligned data hold register for dual DAC (DAC_DL12DCH)

Offset address: 0x24

Reset value: 0x0000 0000



Bit field	Name	Description
31:20	DACCH2D[11:0]	12-bit left- aligned data for DAC2 The bits are configured by the software and the DAC2 converts the data.
19:16	Reserved	Retained, the reset value must be maintained.
15:4	DACCH1D[11:0]	12-bit left- aligned data for DAC1 The bits are configured by the software and the DAC1 converts the data.
3:0	Reserved	Retained, the reset value must be maintained.

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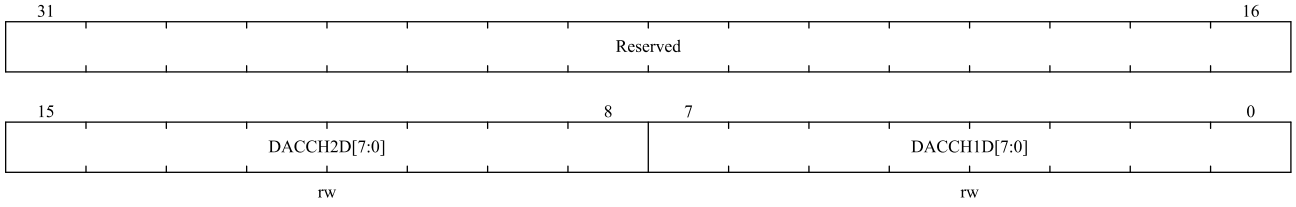
10.5.12 8 bit right aligned data hold register for dual DAC (DAC_DR8DCH)

Offset address: 0x28

Reset value: 0x0000 0000

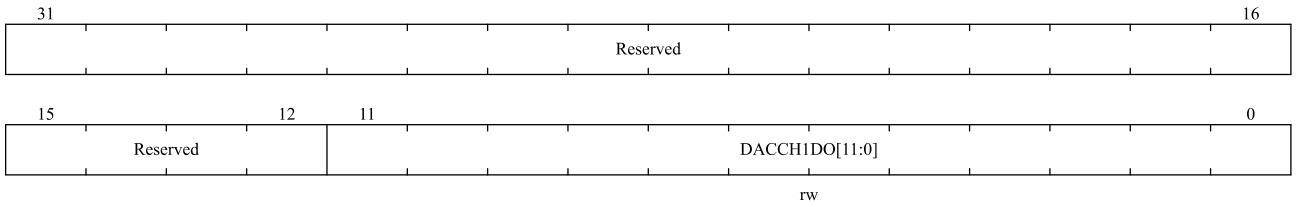


Bit field	Name	Description
31:16	Reserved	Retained, the reset value must be maintained.
15:8	DACCH2D[7:0]	8-bit right- aligned data for DAC2 The bits are configured by the software and the DAC2 converts the data.
7:0	DACCH1D[7:0]	8-bit right- aligned data for DAC1 The bits are configured by the software and the DAC1 converts the data.

10.5.13 DAC1 data output register (DAC_DATO1)

Offset address: 0x2C

Reset value: 0x0000 0000



Bit field	Name	Description
31:12	Reserved	Retained, the reset value must be maintained.
11:0	DACCH1DO[11:0]	DAC1 data output. These bits are read-only and represent the output data of the DAC1.

10.5.14 DAC2 data output register (DAC_DATO2)

Offset address: 0x30

Reset value: 0x0000 0000

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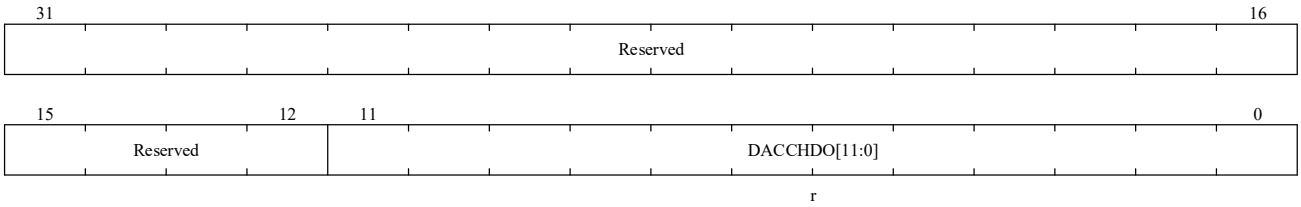

Bit field	Name	Description
31:12	Reserved	Retained, the reset value must be maintained.
11:0	DACCH2DO[11:0]	DAC2 data output. These bits are read-only and represent the output data of the DAC2.

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11 Advanced-control timers (TIM1 and TIM8)

11.1 TIM1 and TIM8 Introduction

The advanced control timers (TIM1 and TIM8) is mainly used in the following occasions: counting the input signal, measuring the pulse width of the input signal and generating the output waveform, etc.

Advanced timers have complementary output function with dead-time insertion and break function. Suitable for motor control.

11.2 Main Features of TIM1 and TIM8

- 16-bit auto-reload counters. (It can realize up-counting, down-counting, up/down counting).
- 16-bit programmable prescaler. (The frequency division factor can be configured with any value between 1 and 65536)
- Programmable Repetition Counter
- TIM1 up to 6 channels, TIM8 up to 6 channels.
- 4 capture/compare channels, the working modes are PWM output, ouput compare, one-pulse mode output, input capture.
- The events that generate the interrupt/DMA are as follows:
  - Update event
  - Trigger event
  - Input capture
  - Output compare
  - Break input
- Complementary outputs with adjustable dead-time.
  - For TIM1 and TIM8, channel 1,2,3 support this feature
- Timer can be controlled by external signal
- Timers can be linked together internally for timer synchronization or chaining
- TIM1_CC5 and TIM8_CC5 for COMP blanking.
- TIM1_CC6 is used to switch the input channel of OPAMP1 and OPAMP2; TIM8_CC6 is used to switch the input channel of OPAMP3 and OPAMP4;
- Incremental (quadrature) encoder interface: used for tracking motion and resolving rotation direction and position;
- Hall sensor interface: used to do three-phase motor control;

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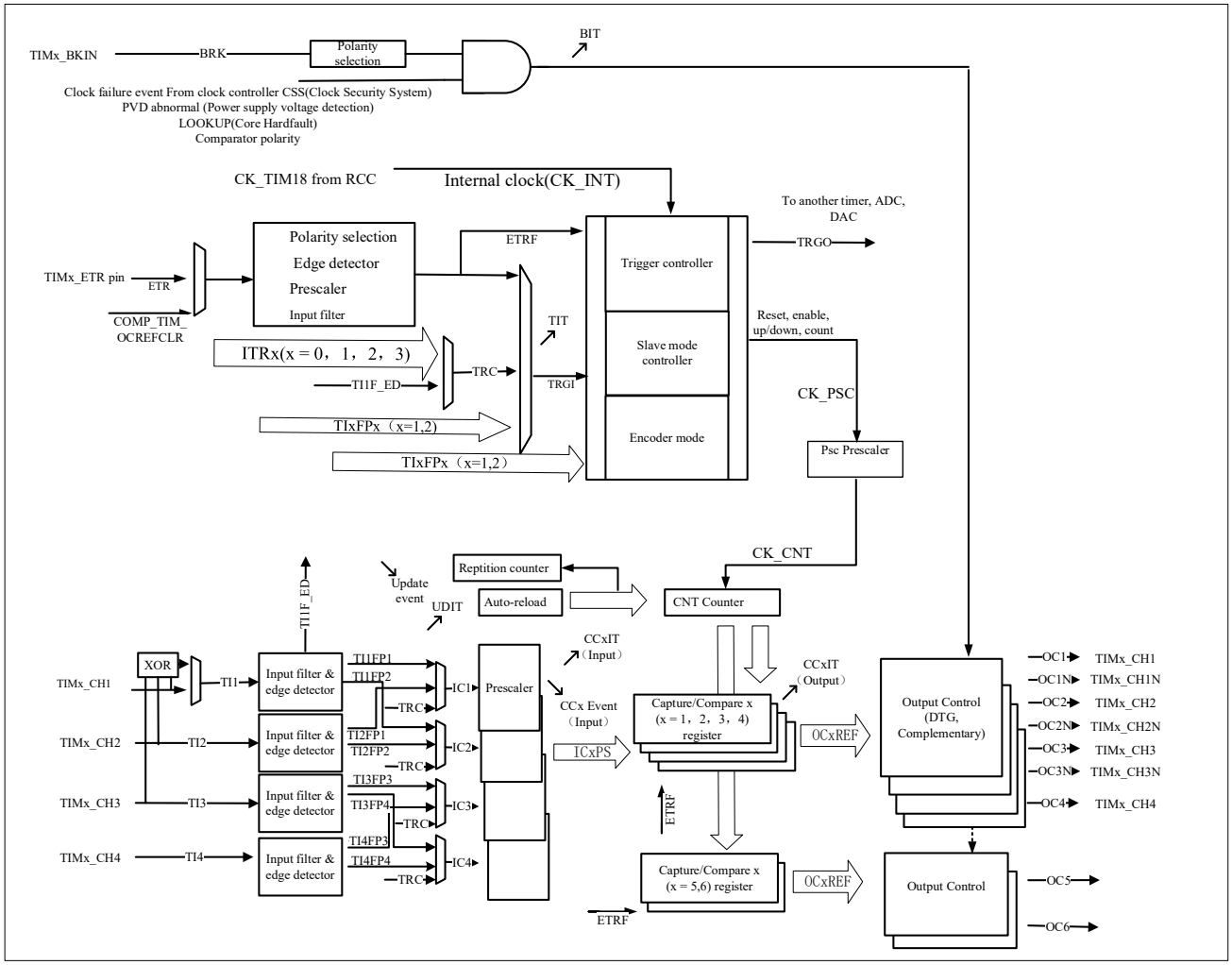
Figure 11-1 Block diagram of TIM1 and TIM8



The event *Interrupt and DMA output*

The capture channel 1 input can come from IOM or comparator output

11.3 TIM1 and TIM8 Function Description

11.3.1 Time-base Unit

The advanced-control's time-base unit mainly includes: prescaler, counter, auto-reload and repetition counter. When the time base unit is working, the software can read and write the corresponding registers (TIMx_PSC, TIMx_CNT, TIMx_AR and TIMx_REPCNT) at any time.

Depending on the setting of the auto-reload preload enable bit (TIMx_CTRL1.ARPEN), the value of the preload register is transferred to the shadow register immediately or at each update event UEV. An update event is generated when the counter reaches the overflow/underflow condition and it can be generated by software when TIMx_CTRL1.UPDIS=0. The counter CK_CNT is valid only when the TIMx_CTRL1.CNTEN bit is set. The counter starts counting one clock cycle after the TIMx_CTRL1.CNTEN bit is set.

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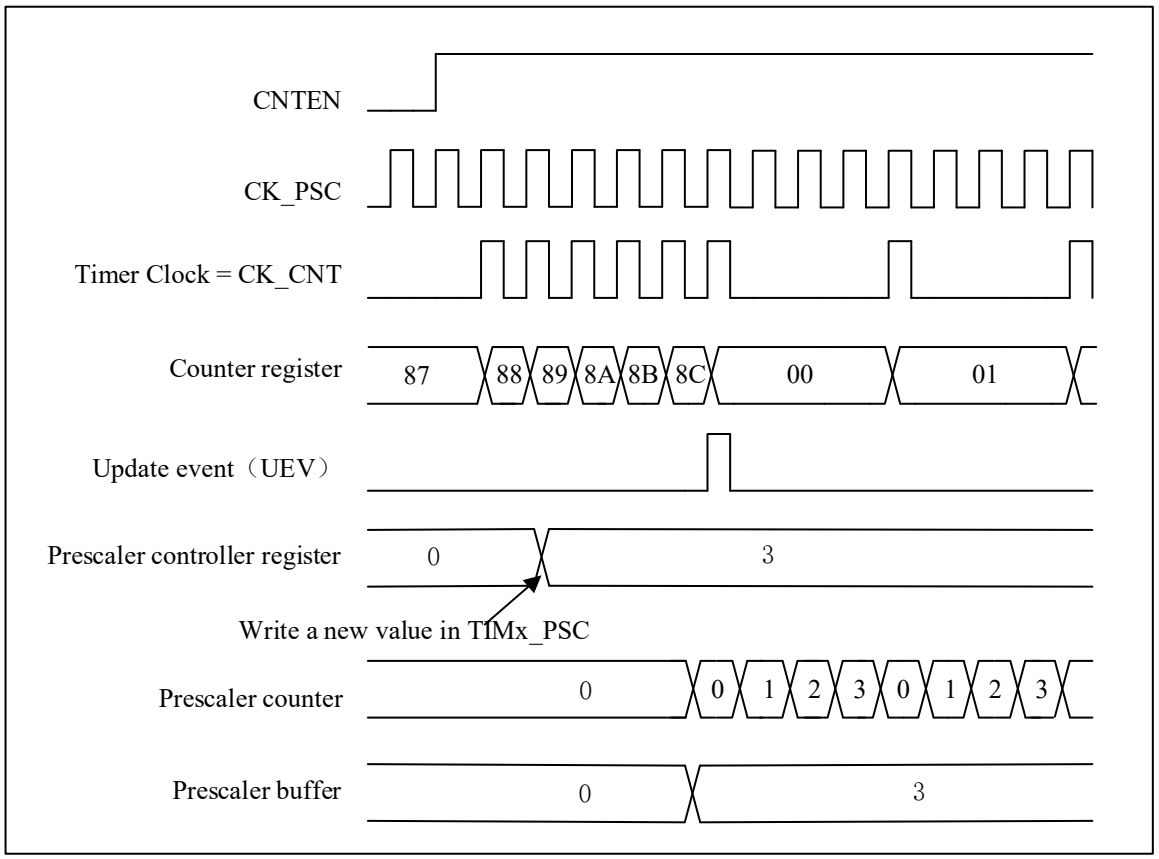
11.3.1.1 Prescaler description

The TIMx_PSC register consists of a 16-bit counter that can be used to divide the counter clock frequency by any factor between 1 and 65536. It can be changed on the fly as it is buffered. The prescaler value is only taken into account at the next update event.

Figure 11-2 Counter timing diagram with prescaler division change from 1 to 4



11.3.2 Counter Mode

11.3.2.1 Up-counting mode

In up-counting mode, the counter will count from 0 to the value of the register TIMx_AR, then it resets to 0. And a counter overflow event is generated.

If the TIMx_CTRL1.UPRS bit (select update request) and the TIMx_EVTGEN.UDGN bit are set, an update event (UEV) will generate. And TIMx_STS.UDITF will not be set by hardware, therefore, no update interrupts or update DMA requests are generated. This setting is used in scenarios where you want to clear the counter but do not want to generate an update interrupt.

Depending on the update request source is configured in the TIMx_CTRL1.UPRS, When an update event occurs, the TIMx_STS.UDITF is set, all registers are updated:

- The repetition counter reloads the contents of the TIMx_REPCNT
- Update auto-reload shadow registers with preload value(TIMx_AR), when TIMx_CTRL1.ARPEN = 1.
- The prescaler shadow register is reloaded with the preload value(TIMx_PSC).

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To avoid updating the shadow registers when new values are written to the preload registers, you can disable the update by setting TIMx_CTRL1.UPDIS=1.

When an update event occurs, the counter will still be cleared and the prescaler counter will also be set to 0 (but the prescaler value will remain unchanged).

The figure below shows some examples of the counter behavior and the update flags for different division factors in the up-counting mode.

Figure 11-3 Timing diagram of up-counting. The internal clock divider factor = 2/N

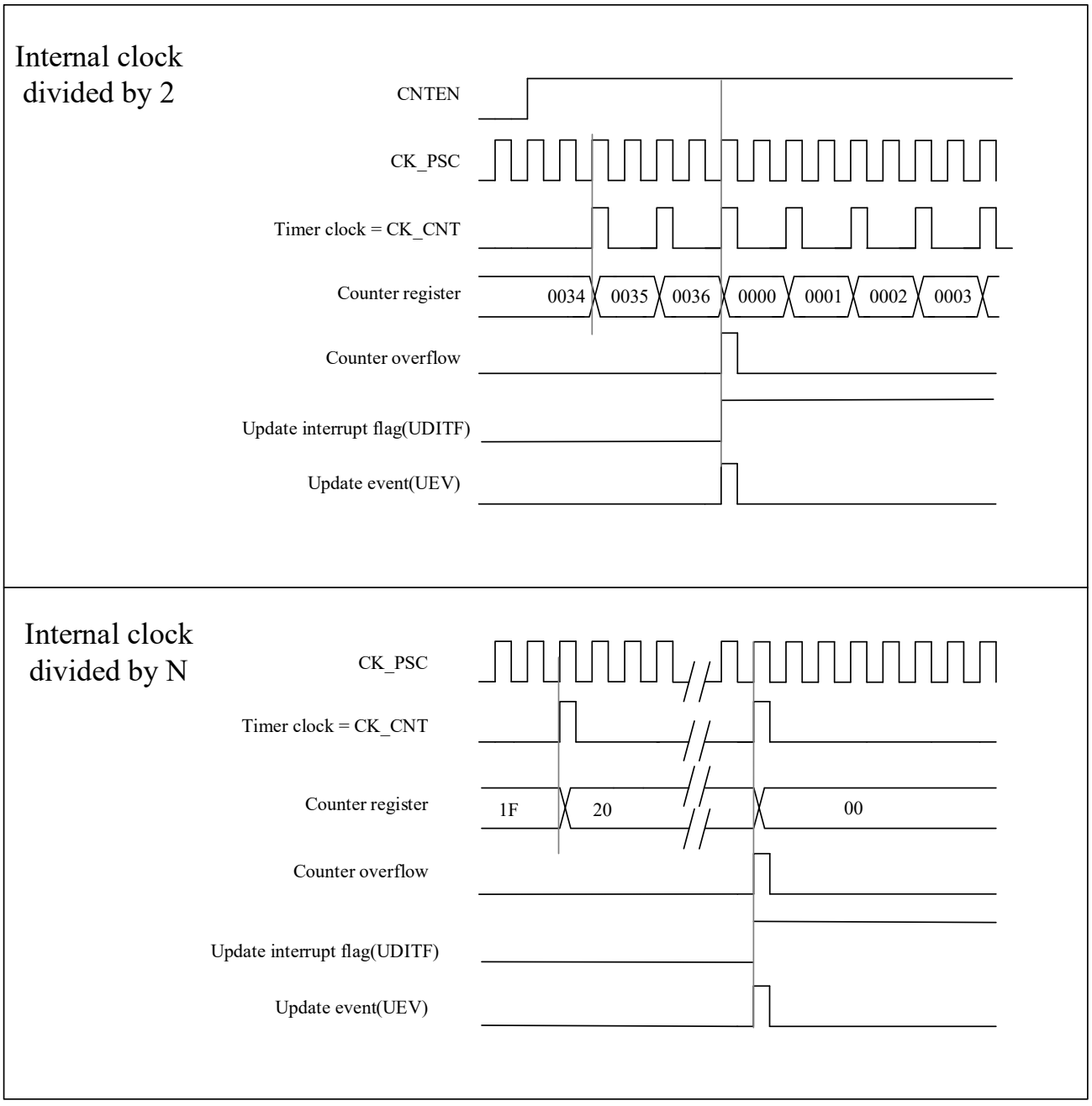

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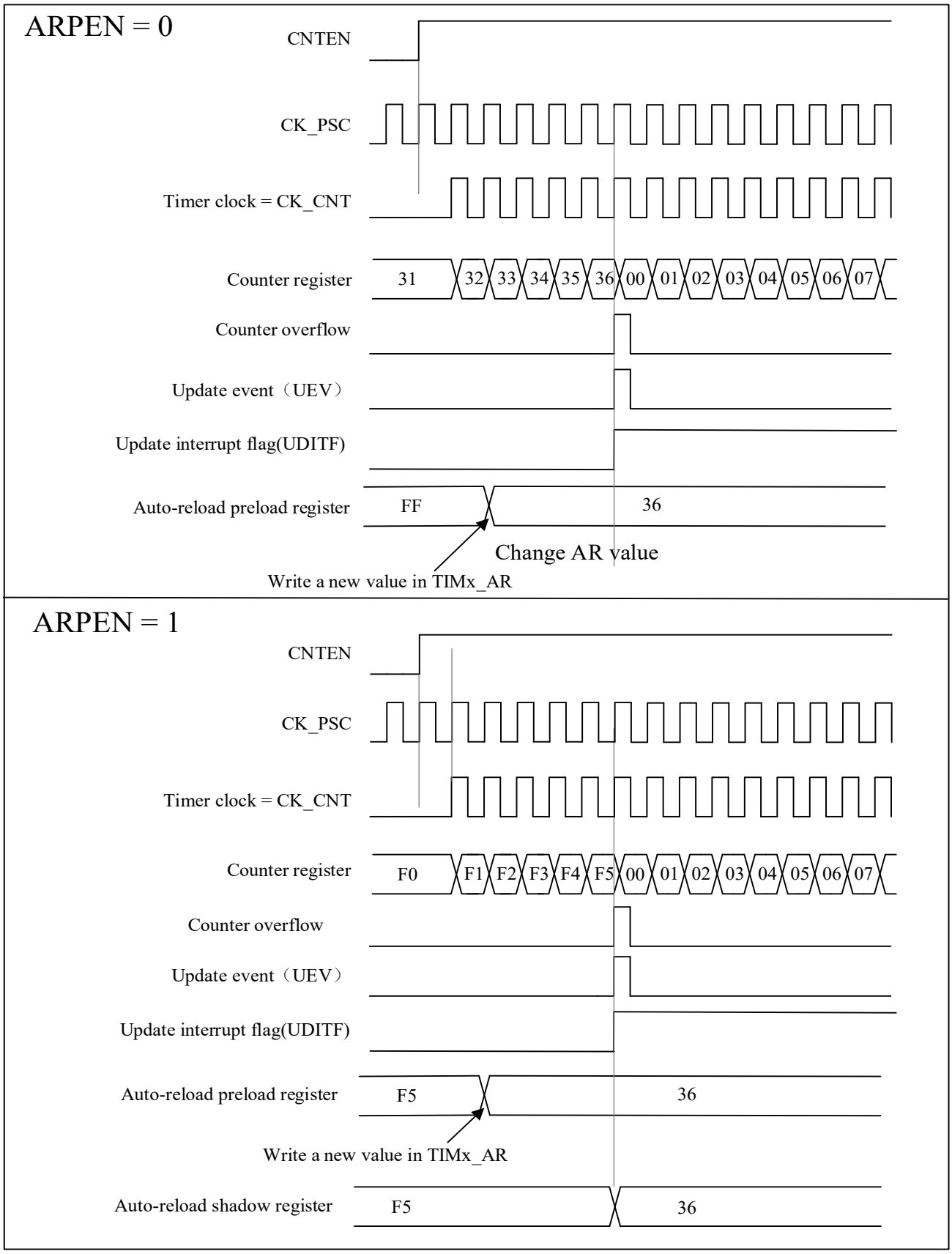
Figure 11-4 Timing diagram of the up-counting, update event when ARPEN=0/1



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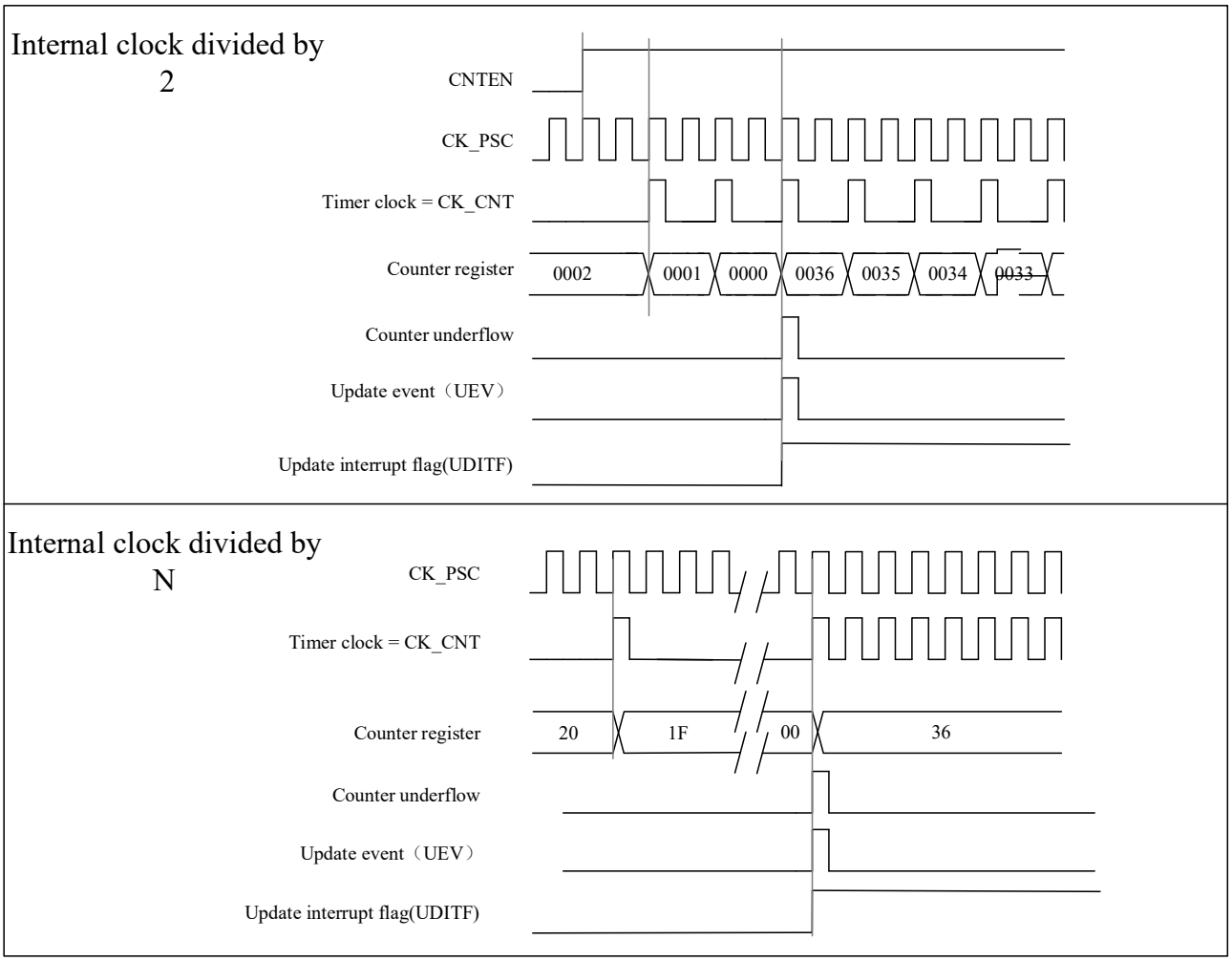
11.3.2.2 Down-counting mode

In down-counting mode, the counter will decrement from the value of the register TIMx_AR to 0, then restart from the auto-reload value and generate a counter underflow event.

The process of configuring update events and updating registers in down-counting mode is the same as in up-counting mode, see 11.3.2.1.

The figure below shows some examples of the counter behavior and the update flags for different division factors in the down-counting mode.

Figure 11-5 Timing diagram of the down-counting, internal clock divided factor = 2/N



11.3.2.3 Center-aligned mode

In center-aligned mode, the counter increments from 0 to the value (TIMx_AR) – 1, a counter overflow event is generated. It then counts down from the auto-reload value (TIMx_AR) to 1 and generates a counter underflow event. Then the counter resets to 0 and starts counting up again.

In this mode, the TIMx_CTRL1.DIR direction bits have no effect and the count direction is updated and specified by hardware. Center-aligned mode is valid when the TIMx_CTRL1. CAMSEL bit is not equal to "00".

The update events can be generated each time the counter overflows and each time the counter underflows. Alternatively, an update event can also be generated by setting the TIMx_EVTGEN. UDGN bit (either by software

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or using a slave mode controller). In this case, the counter restarts from 0, as does the prescaler's counter.

Please note: if the update source is a counter overflow, auto-reload update before reloading the counter.

Figure 11-6 Timing diagram of the Center-aligned, internal clock divided factor =2/N

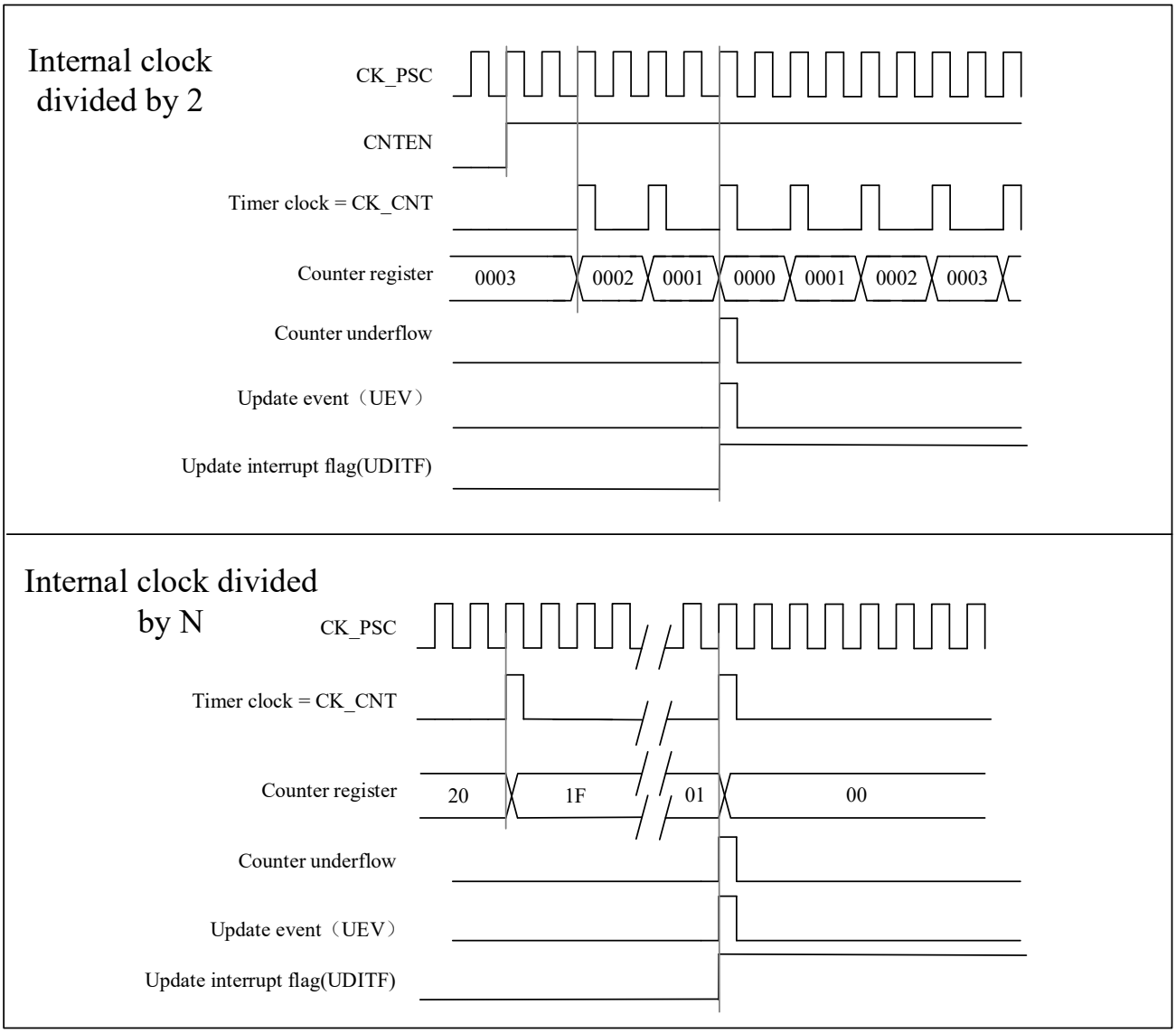

Figure 11-7 A center-aligned sequence diagram that includes counter overflows and underflows (ARPEN = 1)

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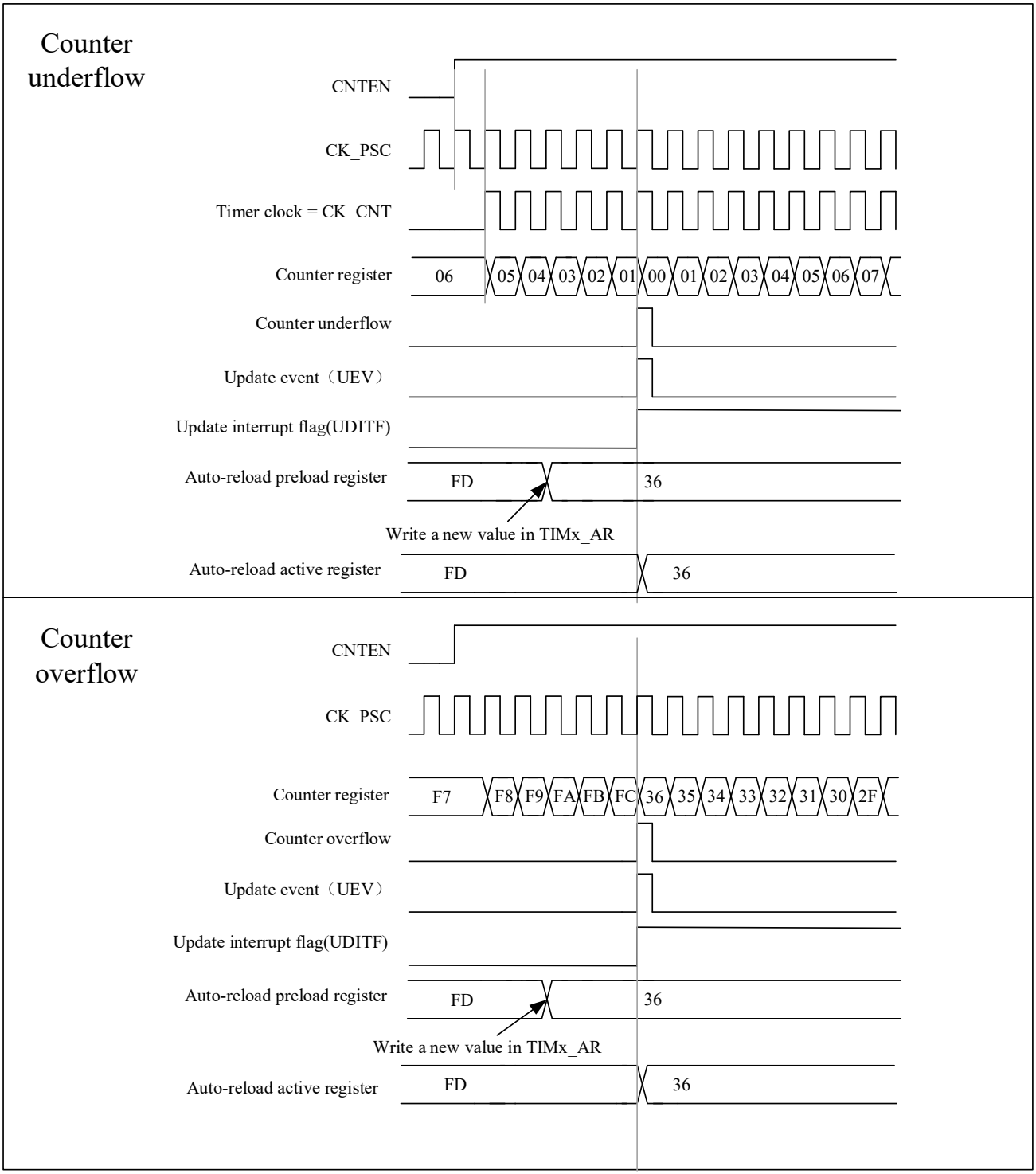

11.3.3 Repetition Counter

The basic unit of Section 11.3.1 describes the conditions for generating an update event (UEV). An update event (UEV) is actually only generated when the repeat counter reaches zero, which is valuable for generating PWM signals.

This means that data is transferred from the preload registers to the shadow registers every N+1 counter overflow or underflow, where N is the value in the TIMx_REPCNT.

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The repetition counter is decremented:

- In the up-counting mode, each time the counter reaches the maximum value, an overflow occurs.
- In down-counting mode, each time the counter decrements to the minimum value, an underflow occurs.
- In center-aligned mode, each time the counter overflows or underflows.

Its repetition rate is defined by the value of the TIMx_REPCNT register.

Repetition counters feature automatic reloading. The update event (generated by setting TIMx_EVTGEN.UDGN or hardware through slave mode controller) occurs immediately, regardless of the value of the repeat counter.

Figure 11-8 Repeat count sequence diagram in down-counting mode

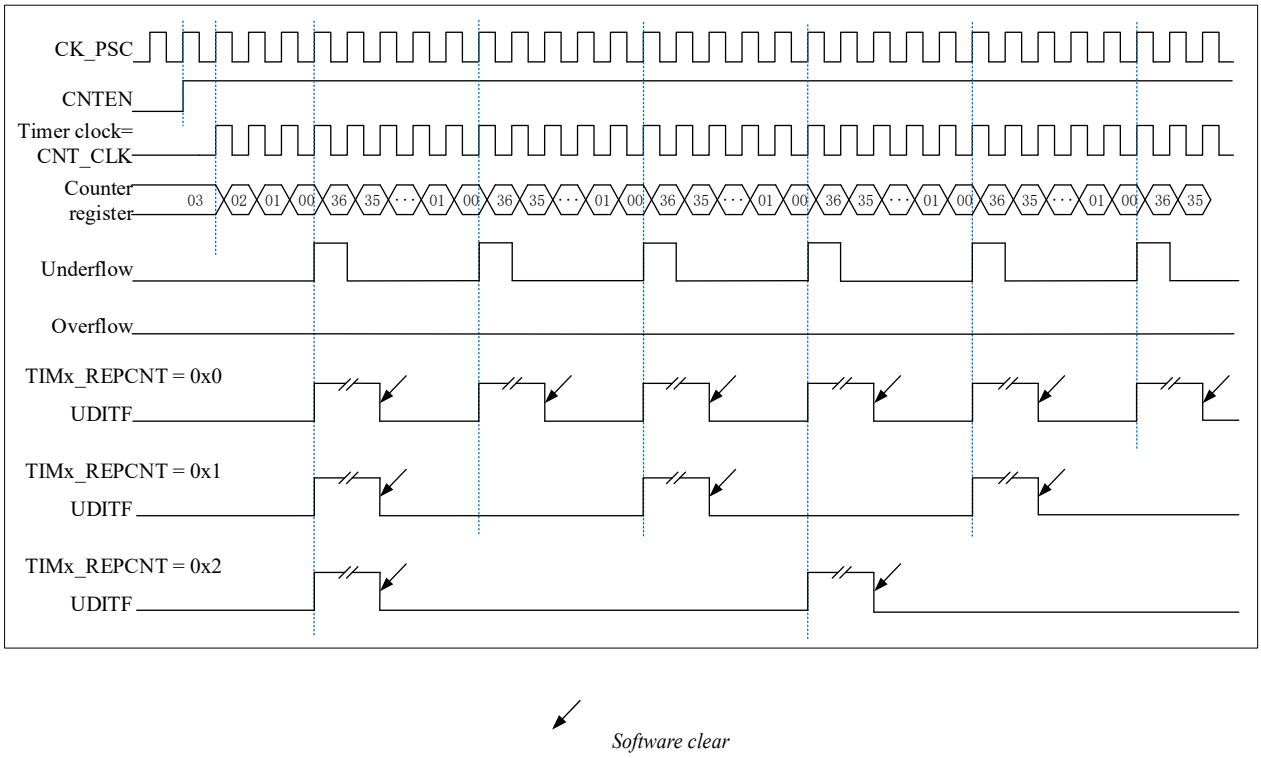

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Figure 11-9 Repeat count sequence diagram in up-counting mode

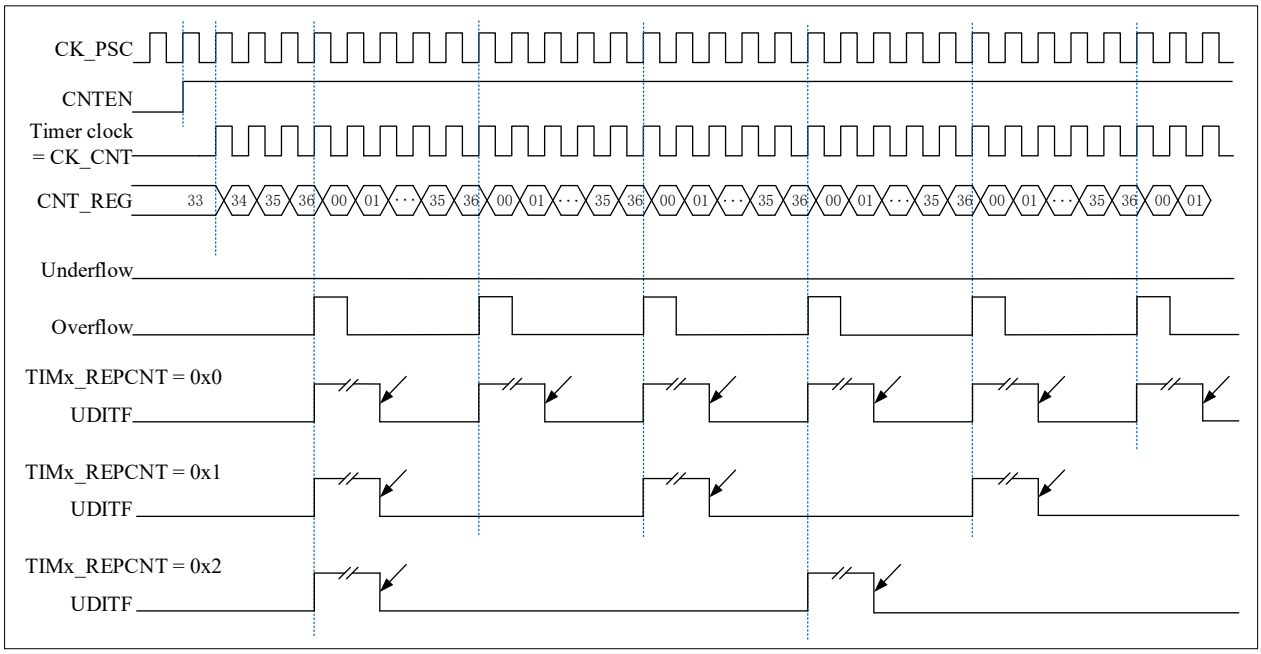
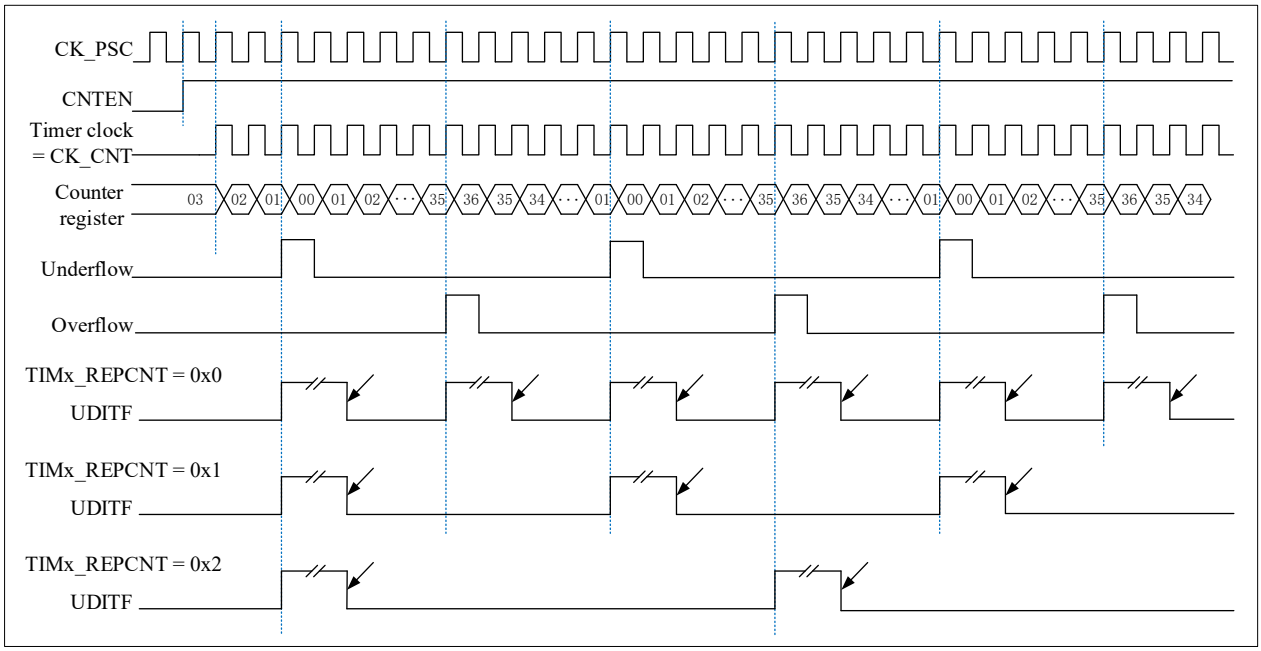


Figure 11-10 Repeat count sequence diagram in center-aligned mode



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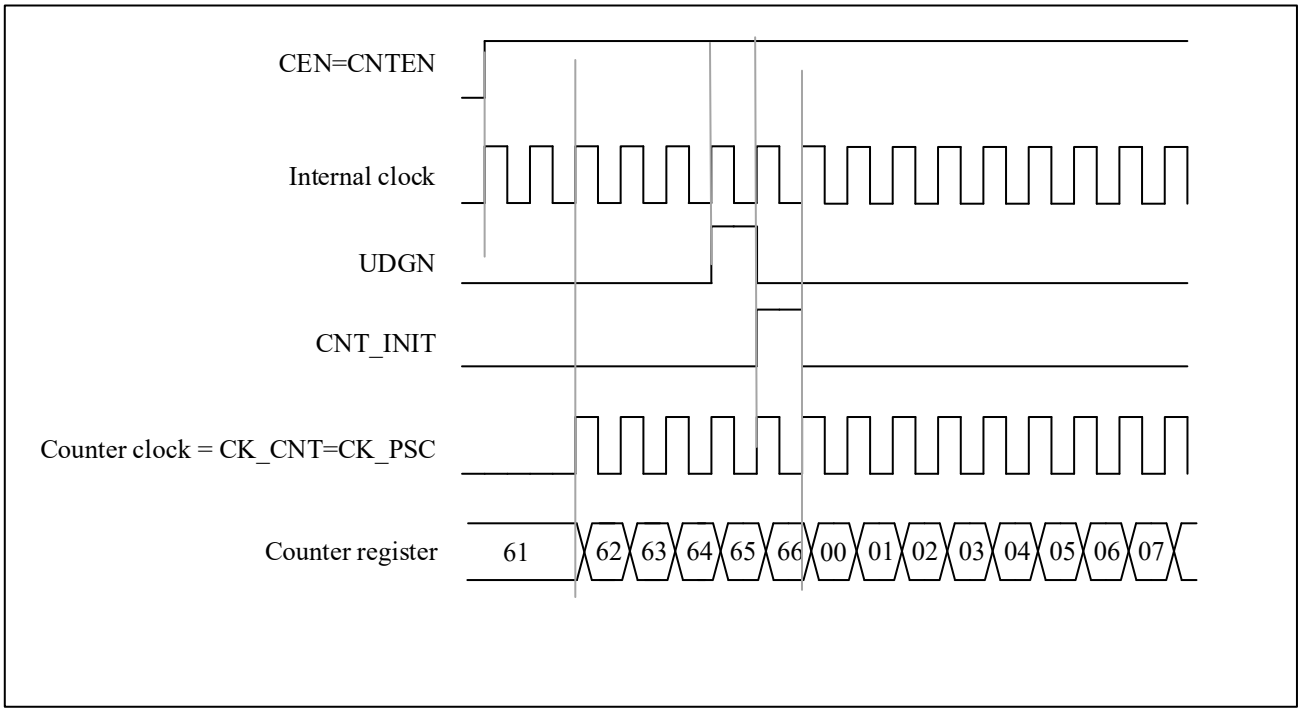
11.3.4 Clock Selection

- The internal clock of Advanced-control timers ： CK_INT
- Two kinds of external clock mode :
  - external input pin
  - external trigger input ETR
- Internal trigger input (ITRx): one timer is used as a prescaler for another timer.

11.3.4.1 Internal clock source (CK_INT)

When the TIMx_SMCTRL.SMSEL is equal to “000”, the slave mode controller is disabled. The three control bits (TIMx_CTRL1.CNTEN、TIMx_CTRL1. DIR、TIMx_EVTGEN. UDGN) can only be changed by software (except TIMx_EVTGEN. UDGN, which remains cleared automatically). It is provided that the TIMx_CTRL1.CNTEN bit is written as' 1 ' by soft, the clock source of the prescaler is provided by the internal clock CK_INT.

Figure 11-11 Control circuit in normal mode, internal clock divided by 1



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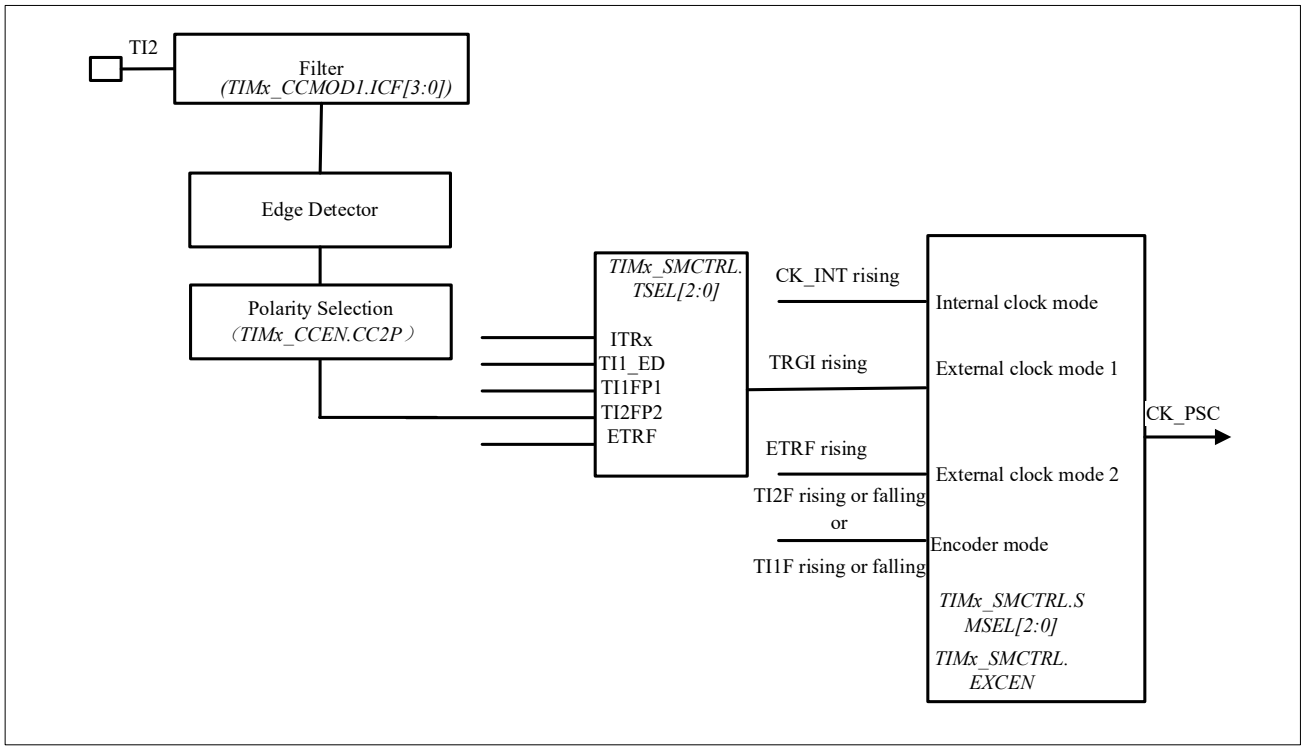
11.3.4.2 External clock source mode 1

Figure 11-12 TI2 external clock connection example



This mode is selected by configuring TIMx_SMCTRL.SMSEL=111. The counter can be configured to count on the rising or falling edge of the clock at the selected input.

For example, to configure up-counting mode to count on the rising edge of the clock at the T12 input, the configuration steps are as follows:

- Configure TIMx_CCMOD1.CC2SEL equal to '01', CC2 channel is configured as input, IC2 is mapped to TI2
- Configure TIMx_CCEN.CC2P equal to '0', select clock rising edge polarity
- To select input filter bandwidth by configuring TIMx_CCMOD1.IC2F[3:0] (if filter is not needed, keep IC2F bit at '0000')
- Configure TIMx_SMCTRL.SMSEL equal to '111', select timer external clock mode 1
- Configure TIMx_SMCTRL.TSEL equal to '110', select TI2 as the trigger input source
- Configure TIMx_CTRL1.CNTEN equal to '1' to start the counter

Note: The capture prescaler is not used for triggering, so it does not need to be configured

When the rising edge of the timer clock occurs at TI2=1, the counter counts once and the TIMx_STS .TITF flag is pulled high.

The delay between the rising edge of TI2 and the actual clock of the counter depends on the resynchronization circuit at the input of TI2.

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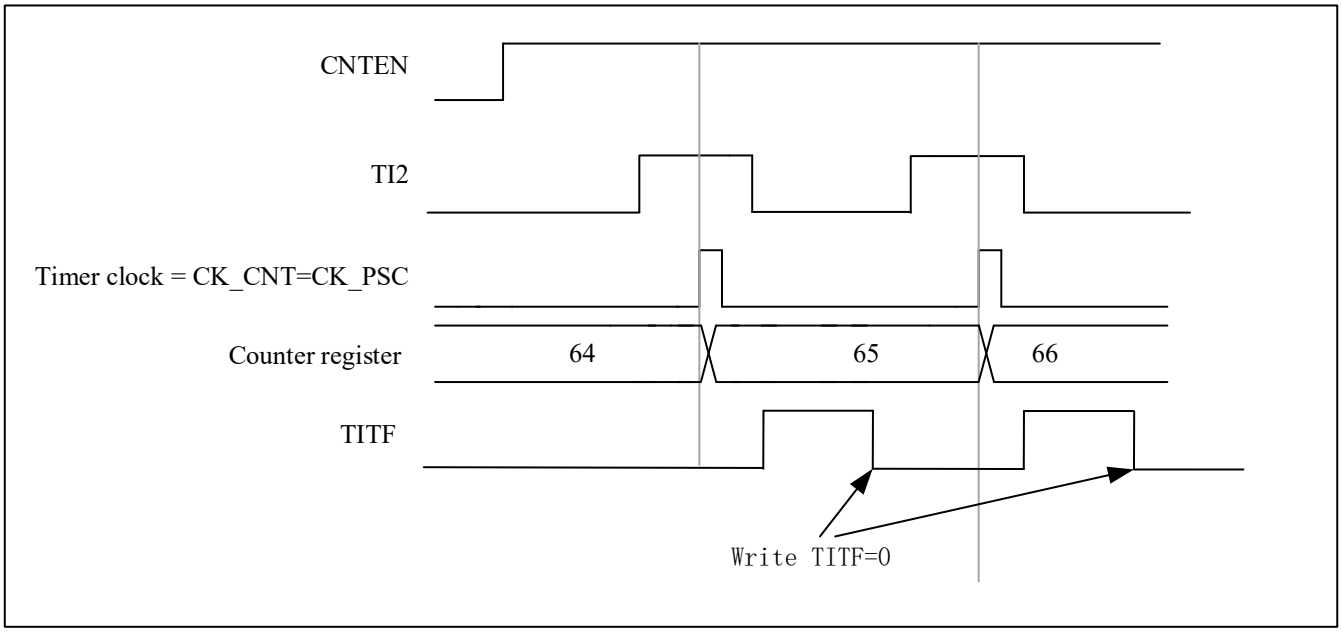
Figure 11-13 Control circuit in external clock mode 1

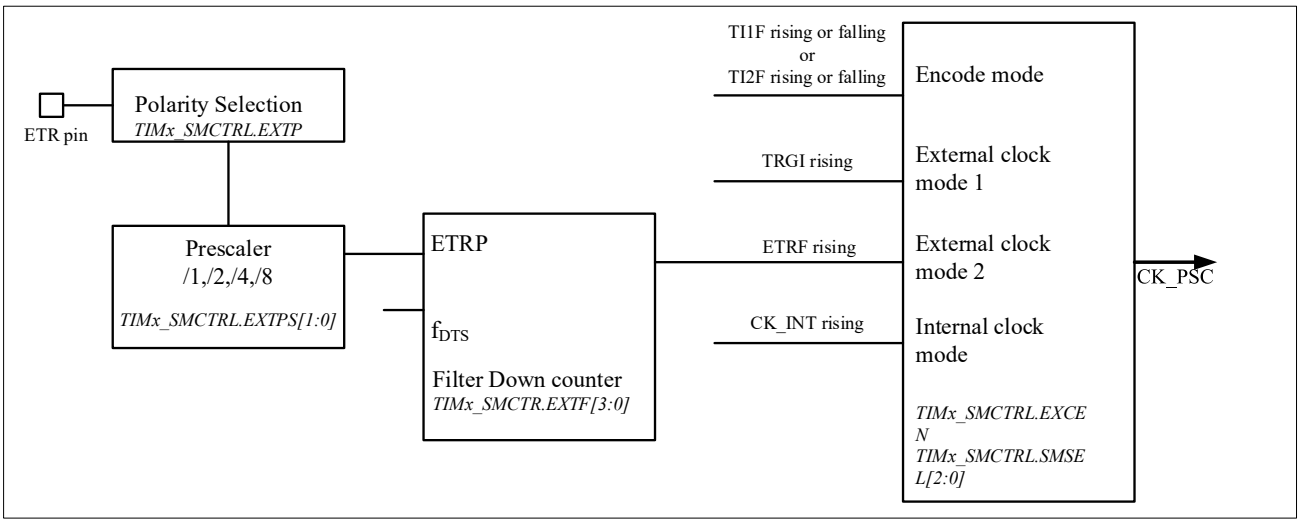


11.3.4.3 External clock source mode 2

This mode is selected by TIMx_SMCTRL .EXCEN equal to 1. The counter can count on every rising or falling edge of the external trigger input ETR.

The following figure is a schematic diagram of the external trigger input module in External clock source mode 2

Figure 11-14 External trigger input block diagram



For example, use the following configuration steps to make the up counter count every 2 rising edges on ETR.

- Since no filter is needed in this case, make TIMx_SMCTRL .EXTF[3:0] equal to ‘0000’
- Configure the prescaler by making TIMx_SMCTRL.EXTPS[1:0] equal to ‘01’
- Select the polarity on ETR pin by setting TIMx_SMCTRL.EXTP equal to ‘0’, The rising edge of ETR is valid

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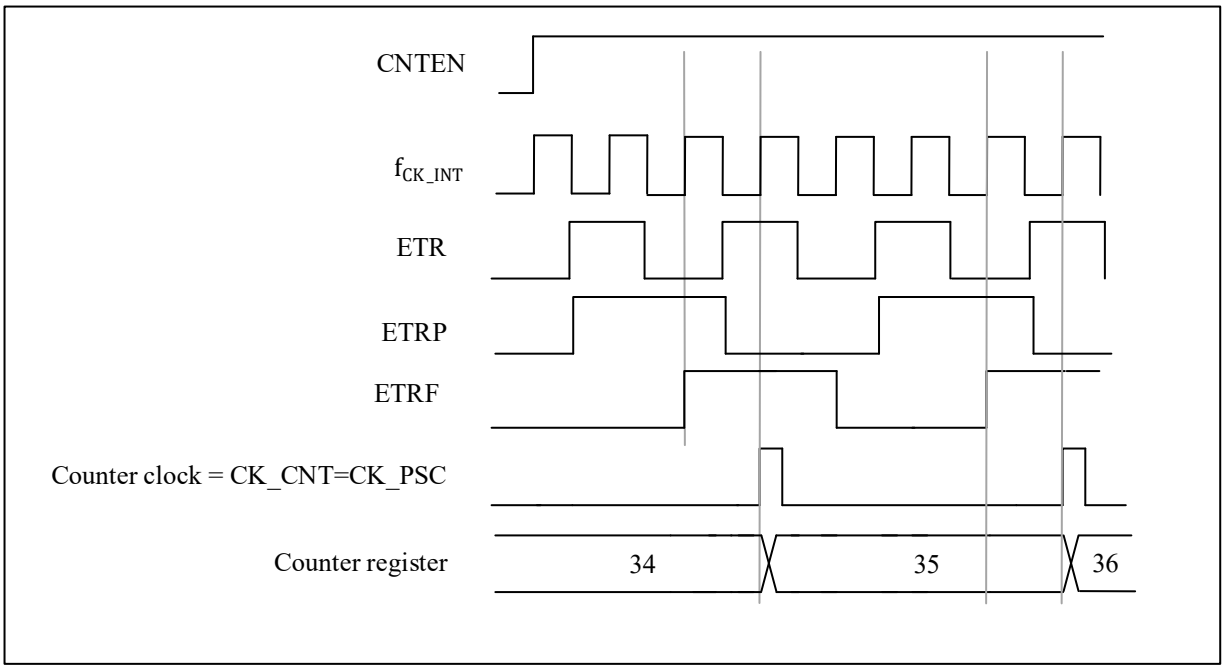
- External clock mode 2 is selected by setting TIMx_SMCTRL .EXCEN equal to '1'
- Turn on the counter by setting TIMx_CTRL1. CNTEN equal to '1'

The counter counts every 2 rising edges of ETR. The delay between the rising edge of ETR and the actual clock to the counter is due to a resynchronization circuit on the ETRP signal.

Figure 11-15 Control circuit in external clock mode 2



11.3.5 Capture/Compare Channels

Capture/compare channels include capture/compare registers and shadow registers. The input section consists of digital filters, multiplexers and prescalers. The output section includes comparators and output controls.

The input signal TIx is sampled and filtered to generate the signal TIxF. A signal (TIxF_rising or TIxF_falling) is then generated by the edge detector of the polarity select function, the polarity of which is selected by the TIMx_CCEN.CCxP bits. This signal can be used as a trigger input for the slave mode controller. At the same time, the signal ICx is sent to the capture register after frequency division. The following figure shows a block diagram of a capture/compare channel.

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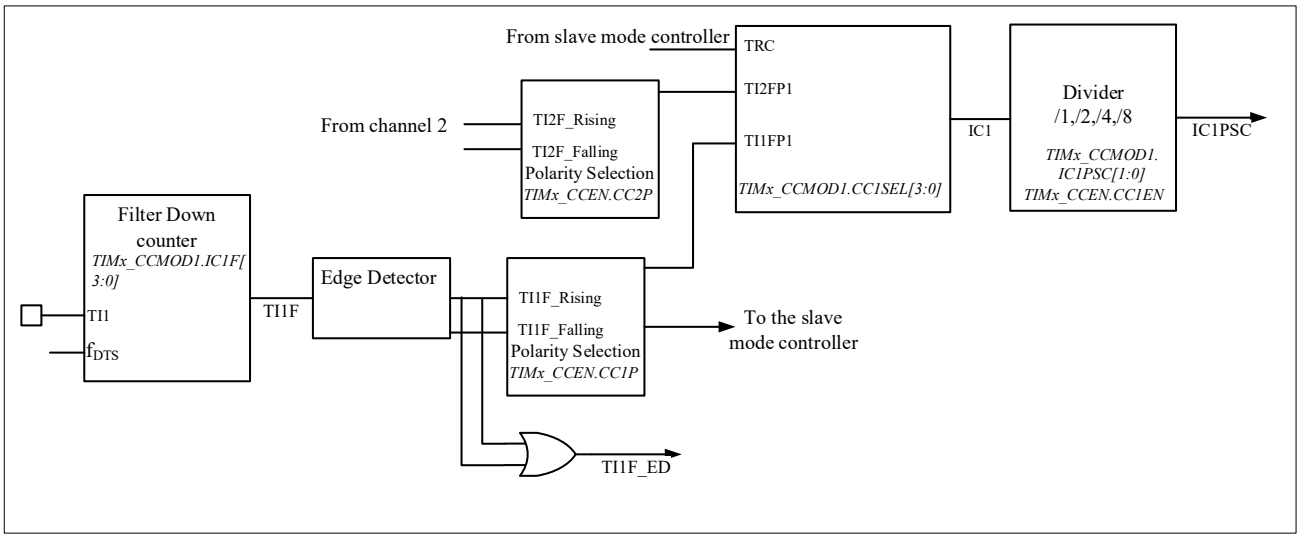
Figure 11-16 Capture/compare channel (example: channel 1 input stage)



The output part generates an intermediate waveform OCxRef (active high) as reference. The polarity acts at the end of the chain.

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Figure 11-17 Capture/compare channel 1 main circuit

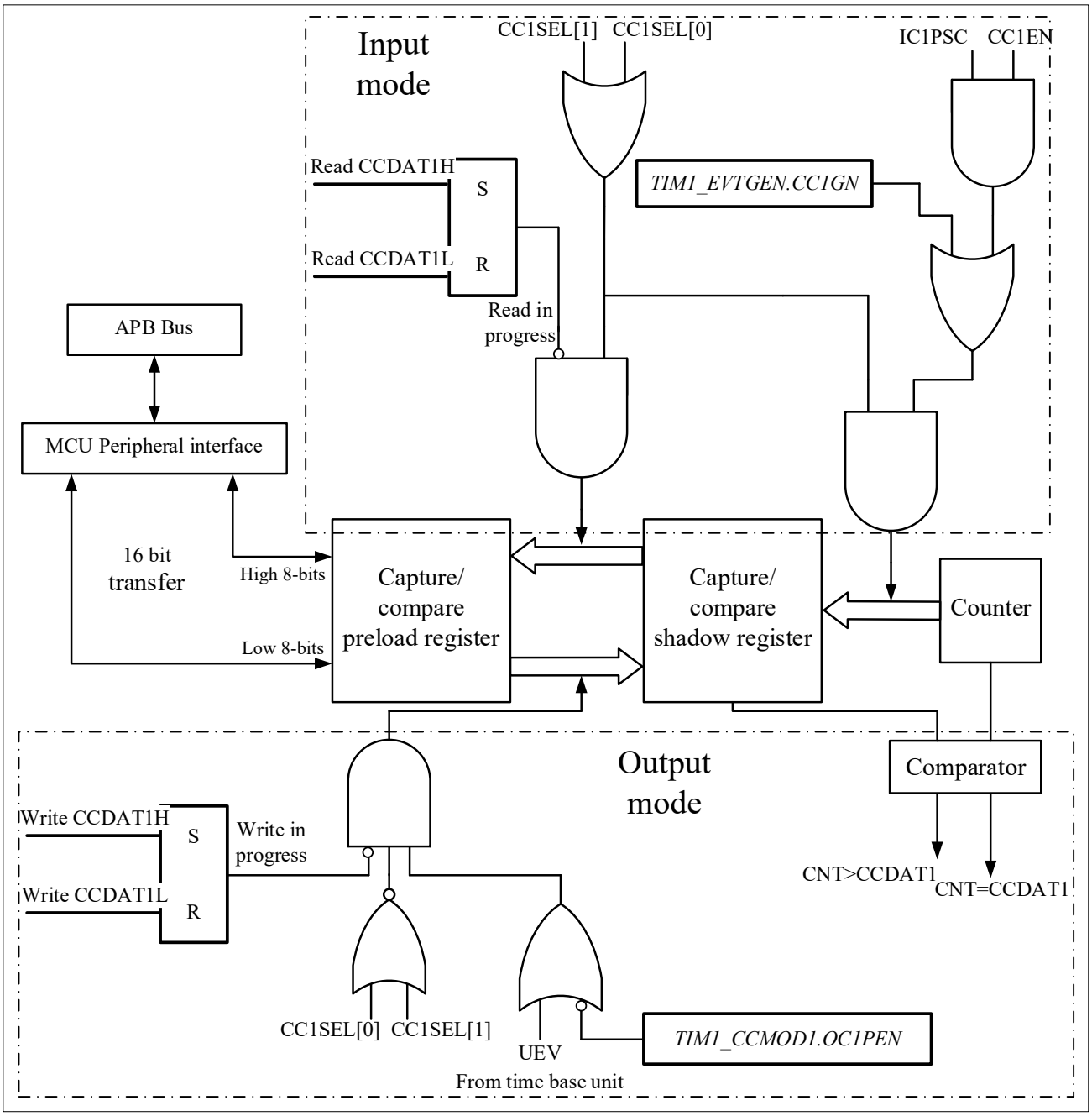

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Figure 11-18 Output part of channelx (x= 1,2,3, take channel 1 as example)

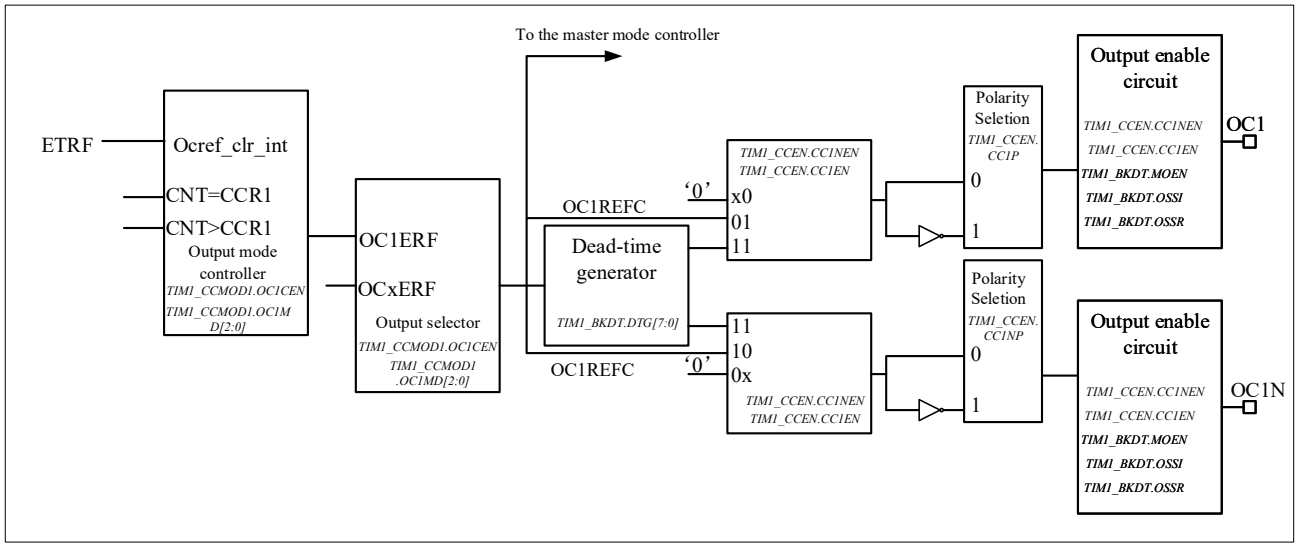
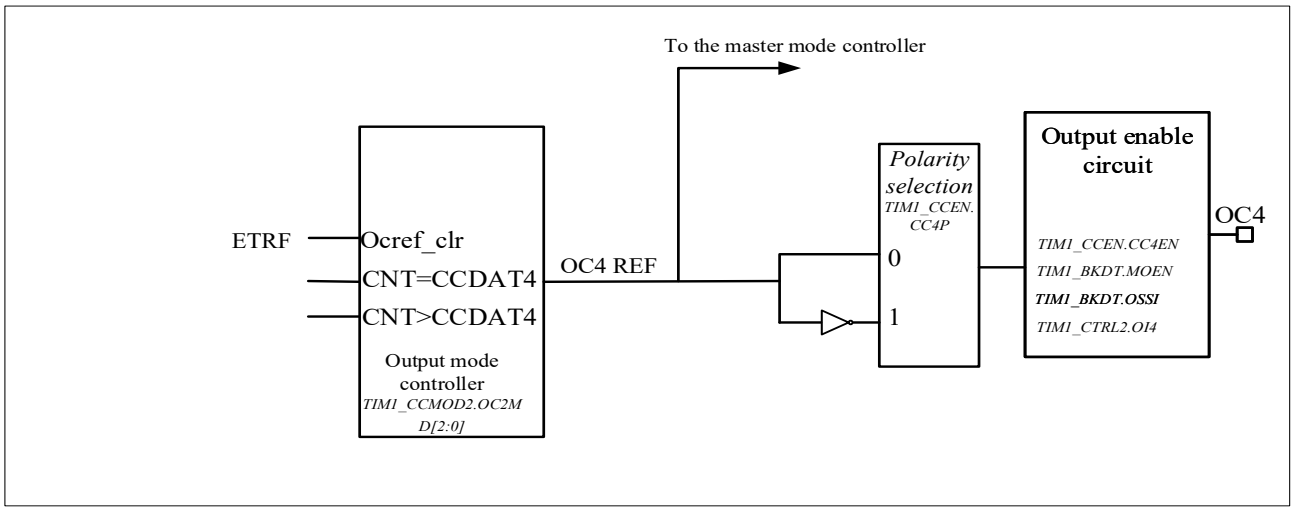


Figure 11-19 Output part of channelx (x= 4)



Reads and writes always access preloaded registers when capturing/comparing. The two specific working processes are as follows:

In capture mode, the capture is actually done in the shadow register, and then the value in the shadow register is copied into the preload register.

In compare mode, as opposed to capture mode, the value of the preload register is copied into the shadow register, which is compared with the counter.

11.3.6 Input Capture Mode

In capture mode, the TIMx_CCDATx registers are used to latch the counter value after the ICx signal detects.

There is a capture interrupt flag TIMx_STS.CCxITF, which can issue an interrupt or DMA request if the corresponding interrupt enable is pulled high.

The TIMx_STS. CCxITF bit is set by hardware when a capture event occurs and is cleared by software or by reading

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the TIMx_CCDATx register.

The overcapture flag TIMx_STS.CCxOCF is set equal to 1 when the counter value is captured in the TIMx_CCDATx register and TIMx_STS.CC1ITF is already pulled high. Unlike the former, TIMx_STS.CCxOCF is cleared by writing 0 to it.

To achieve a rising edge of the TI1 input to capture the counter value into the TIMx_CCDAT1 register, the configuration flow is as follows:

- To select a valid input:

  Configure TIMx_CCMOD1.CC1SEL to '01'. At this time, the input is the CC1 channel, and IC1 is mapped to TI1.

- Program the desired input filter duration:

  Define the sampling frequency of the TI1 input and the length of the digital filter by configuring the TIMx_CCMODx.ICxF bits. Example: If the input signal jitters up to 5 internal clock cycles, we must choose a filter duration longer than these 5 clock cycles. When 8 consecutive samples (sampled at f_{DTS} frequency) with the new level are detected, we can validate the transition on TI1. Then configure TIMx_CCMOD1. IC1F to '0011'.

- By configuring TIMx_CCEN .CC1P=0, select the rising edge as the valid transition polarity on the TI1 channel.
- Configure the input prescaler. In this example, configure TIMx_CCMOD1.IC1PSC= '00' to disable the prescaler because we want to capture every valid transition.
- Enable capture by configuring TIMx_CCEN. CC1EN = '1'.

If you want to enable DMA request, you can configure TIMx_DINTEN.CC1DEN=1.If you want enable related interrupt request, you can configureTIMx_DINTEN.CC1IEN bit=1

11.3.7 PWM Input Mode

There are some differences between PWM input mode and normal input capture mode, including:

- Two ICx signals are mapped to the same TIx input.
- The two ICx signals are active on edges of opposite polarity.
- Select one of two TIxFP signals as trigger input.
- The slave mode controller is configured in reset mode.

For example, the following configuration flow can be used to know the period and duty cycle of the PWM signal on TI1 (It depends on the frequency of CK_INT and the value of the prescaler).

- Configure TIMx_CCMOD1.CC1SEL equal to '01' to select TI1 as valid input for TIMx_CCDAT1.
- Configure TIMx_CCEN.CC1P equal to '0' to select the active polarity of filtered timer input 1(TI1FP1), valid on the rising edge.
- Configure TIMx_CCMOD1.CC2SEL equal to '10' select TI1 as valid input for TIMx_CCDAT2.
- Configure TIMx_CCEN.CC2P equal to 1 to select the valid polarity of filtered timer input 2(TI1FP2), valid on the falling edge.

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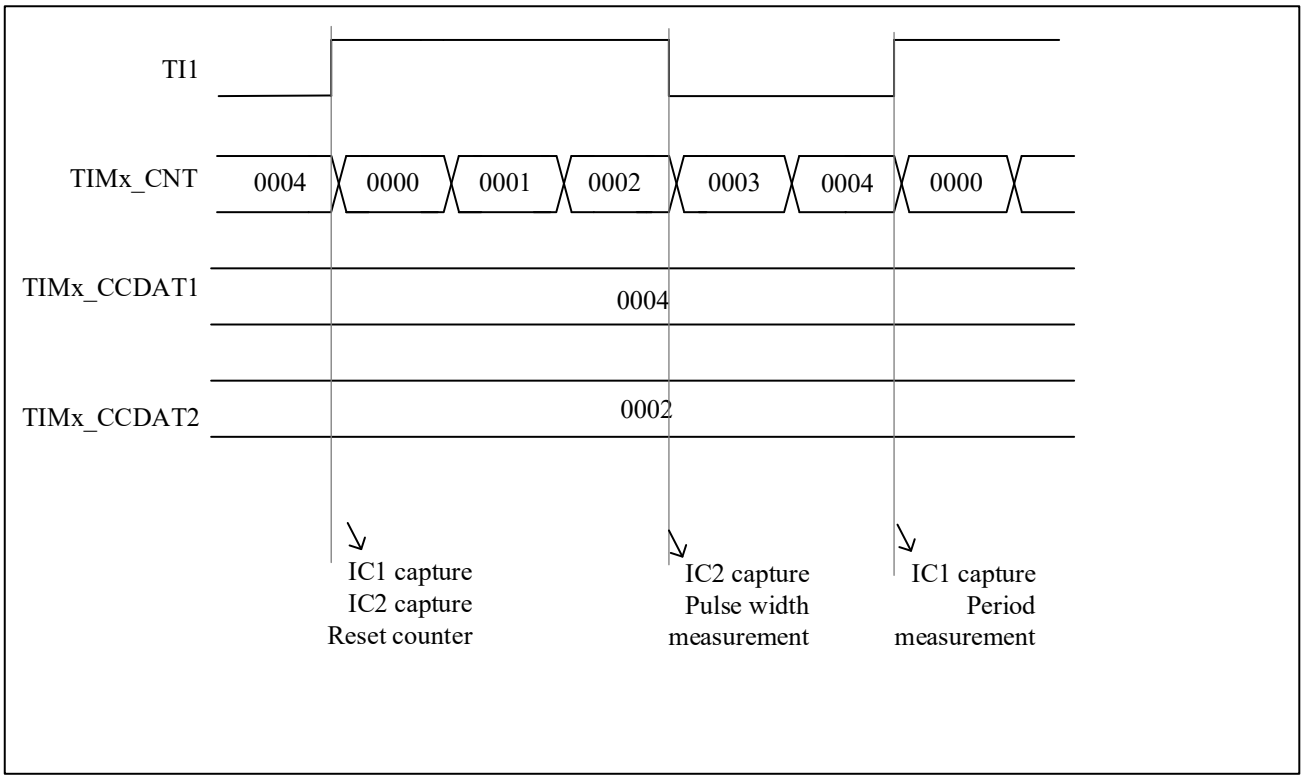
- Configure TIMx_SMCTRL.TSEL=101 to select Filtered timer input 1 (TI1FP1) as valid trigger input.
- Configure TIMx_SMCTRL.SMSEL=100 to configure the slave mode controller to reset mode.
- Configure TIMx_CCEN. CC1EN=1 and TIMx_CCEN.CC2EN=1 to enable capture.

Figure 11-20 PWM input mode timing



Because of only filter timer input 1 (TI1FP1) and filter timer input 2 (TI2FP2) are connected to the slave mode controller, the PWM input mode can only be used with the TIMx_CH1/TIMx_CH2 signals.

11.3.8 Forced Output Mode

Software can force output compare signals to active or inactive level directly, in output mode (TIMx_CCMODx.CCxSEL=00).

User can set TIMx_CCMODx. OCxMD=101 to force the output compare signal to active level. And the OCxREF will be forced high, OCx get opposite value to CCxP polarity bit. On the other hand, user can set TIMx_CCMODx. OCxMD=100 to force the output compare signal to inactive level.

The values of the TIMx_CCDATx shadow register and the counter still comparing with each other in this mode.

The comparison between the output compare register TIMx_CCDATx and the counter TIMx_CNT has no effect on OCxREF. And the flag still can be set. Therefore, the interrupt and DMA requests still can be sent.

11.3.9 Output Compare Mode

User can use this mode to control the output waveform, or to indicate that a period of time has elapsed.

When the capture/compare register and the counter have the same value, the output compare function's operations

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are as follow:

- TIMx_CCMODx.OCxMD is for output compare mode, and TIMx_CCEN.CCxP is for output polarity. When the compare matches, if set TIMx_CCMODx.OCxMD=000, the output pin will keep its level;if set TIMx_CCMODx.OCxMD=001, the output pin will be set active;if set TIMx_CCMODx.OCxMD=010, the output pin will be set inactive;if set TIMx_CCMODx.OCxMD=011, the output pin will be set to toggle.
- Set TIMx_STS.CCxITF.
- If user set TIMx_DINTEN.CCxIEN, a corresponding interrupt will be generated.
- If user set TIMx_DINTEN.CCxDEN and set TIMx_CTRL2.CCDSEL to select DMA request, and DMA request will be sent.

User can set TIMx_CCMODx.OCxPEN to choose capture/compare shawdow regisete using capture/compare preload registers(TIMx_CCDATx) or not.

The time resolution is one count of the counter.

In one-pulse mode, the output compare mode can also be used to output a single pulse.

Here are the configuration steps for output compare mode:

- First of all, user should select the counter clock.
- Secondly, set TIMx_AR and TIMx_CCDATx with desired data.
- If user need to generate an interrupt, set TIMx_DINTEN.CCxIEN.
- Then select the output mode by set TIMx_CCEN.CCxP, TIMx_CCMODx.OCxMD, TIMx_CCEN.CCxEN, etc.
- At last, set TIMx_CTRL1.CNTEN to enable the counter.

User can update the output waveform by setting TIMx_CCDATx at any time, as long as the preload register is not enabled. Otherwise the TIMx_CCDATx shadow register will be updated at the next update event.

Here is an example.

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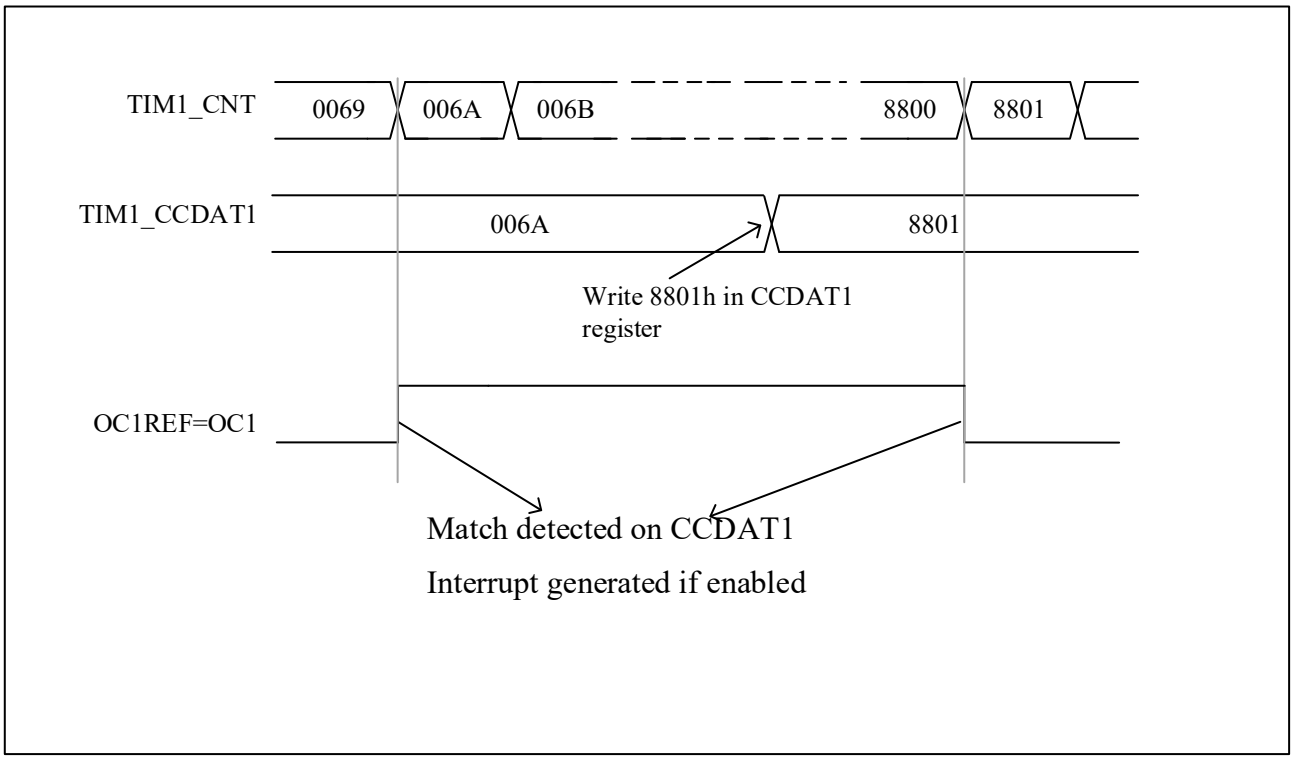
Figure 11-21 Output compare mode, toggle on OC1



11.3.10 PWM Mode

User can use PWM mode to generate a signal whose duty cycle is determined by the value of the TIMx_CCDATx register and whose frequency is determined by the value of the TIMx_AR register. And depends on the value of TIMx_CTRL1.CAMSEL, the TIM can generate PWM signal in edge-aligned mode or center-aligned mode.

User can set PWM mode 1 or PWM mode 2 by setting TIMx_CCMODx. OCxMD=110 or setting TIMx_CCMODx. OCxMD=111. To enable preload register, user must set corresponding TIMx_CCMODx.OCxPEN. And then set TIMx_CTRL1.ARPEN to auto-reload preload register eventually.

User can set polarity of OCx by setting TIMx_CCEN.CCxP. On the other hand, to enable the output of OCx, user need to set the combination of the value of CCxEN, CCxNEN, MOEN, OSSI, and OSSR in TIMx_CCEN and TIMx_BKDT.

The values of TIMx_CNT and TIMx_CCDATx are always compared with each other when the TIM is under PWM mode.

Only if an update event occurs, the preload register will transfer to the shadow register. Therefore user must reset all the registers by setting TIMx_EVTGEN.UDGN before the counter starts counting.

11.3.10.1 PWM center-aligned mode

If user set TIMx_CTRL1.CAMSEL equal 01, 10 or 11, the PWM center-aligned mode will be active. The setting of the compare flag depends on the value of TIMx_CTRL1.CAMSEL. There are three kinds of situation that the compare flag is set, only when the counter counts up, only when the counter counts down, or when the counter counts up and counts down. User should not modified TIMx_CTRL1.DIR by software, it is updated by hardware.

Examples of center-aligned PWM waveforms is as follow, and the setting of the waveform are: TIMx_AR=8, PWM

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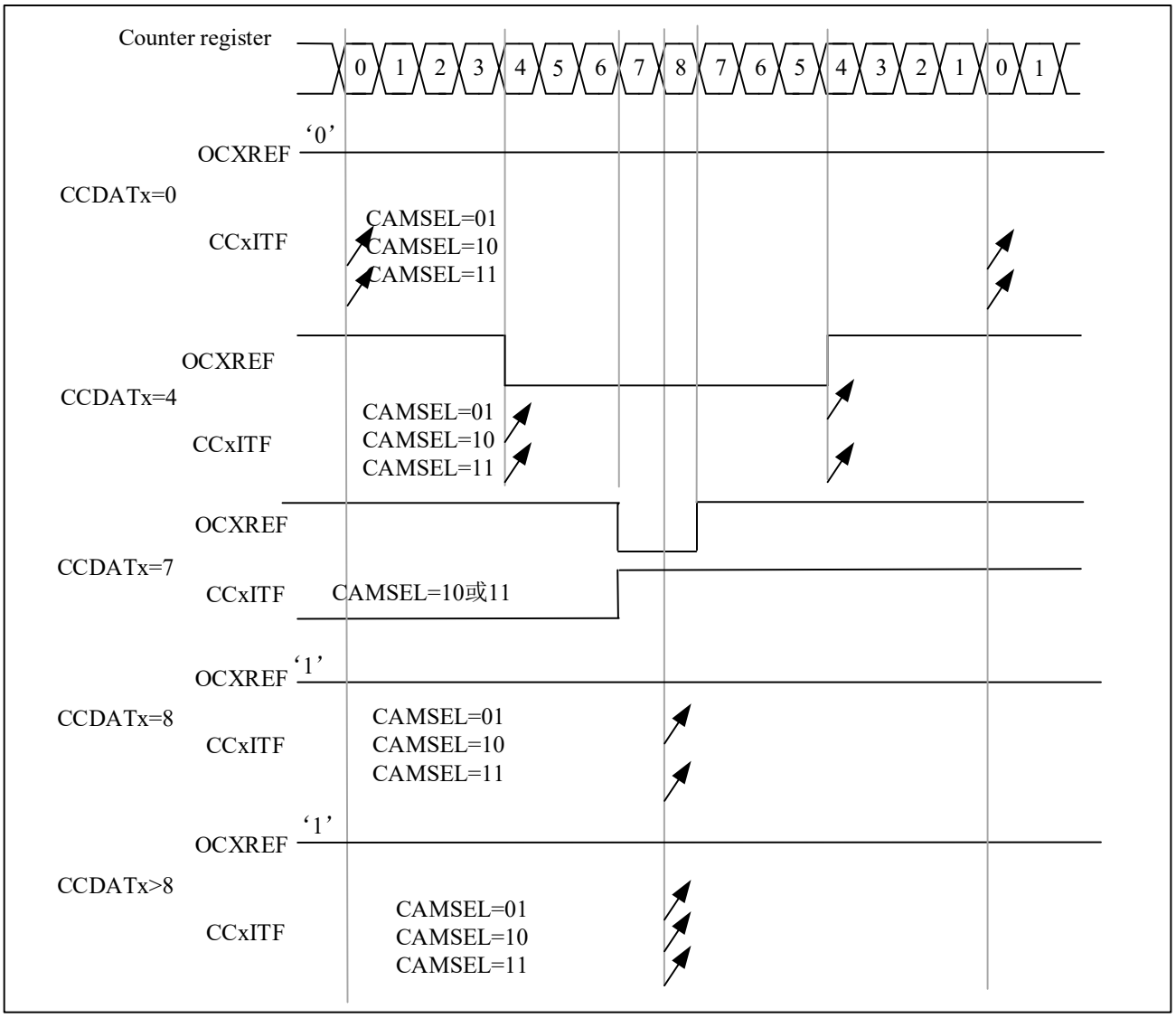
mode 1, the compare flag is set when the counter counts down corresponding to TIMx_CTRL1. CAMSEL=01.

Figure 11-22 Center-aligned PWM waveform (AR=8)



Notes that user should know when using center-aligned mode are as follow:

- It depends on the value of TIMx_CTRL1.DIR that the counter counts up or down. Cautions that the DIR and CAMSEL bits should not be changed at the same time.
- User should not write the counter while running in center-aligned mode, otherwise it will cause unexpected results. Here are some example:
  - If the value written into the counter is 0 or is the value of TIMx_AR, the direction will be updated but the update event will not be generated.
  - If the value written into the counter is greater than the value of auto-reload, the direction will not be updated.
- To be on the safe side, user is suggested setting TIMx_EVTGEN.UDGN to generate an update by software

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before starting the counter, and not writing the counter while it is running.

11.3.10.2 PWM edge-aligned mode

There are two kinds of configuration in edge-aligned mode, up-counting and down-counting.

- **Up-counting**

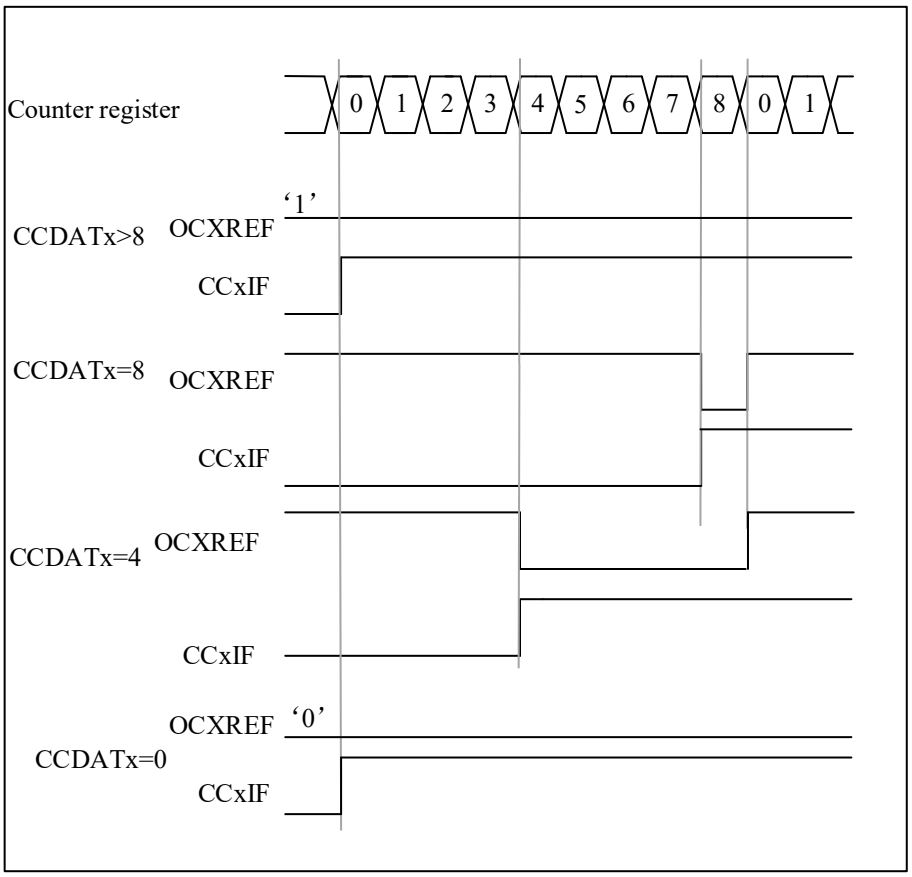
User can set TIMx_CTRL1.DIR=0 to make counter counts up.

Here is an example for PWM mode1.

When TIMx_CNT < TIMx_CCDATx, the reference PWM signal OCxREF is high. Otherwise it will be low. If the compare value in TIMx_CCDATx is greater than the auto-reload value, the OCxREF will remains 1. Conversely, if the compare value is 0, the OCxREF will remains 0.

When TIMx_AR=8, the PWM waveforms are as follow.

Figure 11-23 Edge-aligned PWM waveform (APR=8)



- **Down-counting**

User can set TIMx_CTRL1.DIR=1 to make counter counts down.

Here is an example for PWM mode1.

When TIMx_CNT > TIMx_CCDATx, the reference PWM signal OCxREF is low. Otherwise it will be high. If the compare value in TIMx_CCDATx is greater than the auto-reload value, the OCxREF will remains 1.

Note: If the nth PWM cycle CCDATx shadow register >= AR value, the shadow register value of CCDATx in the (n+1)th PWM cycle is 0. At the moment when the counter is 0 in the (n+1)th PWM cycle, although the value of the

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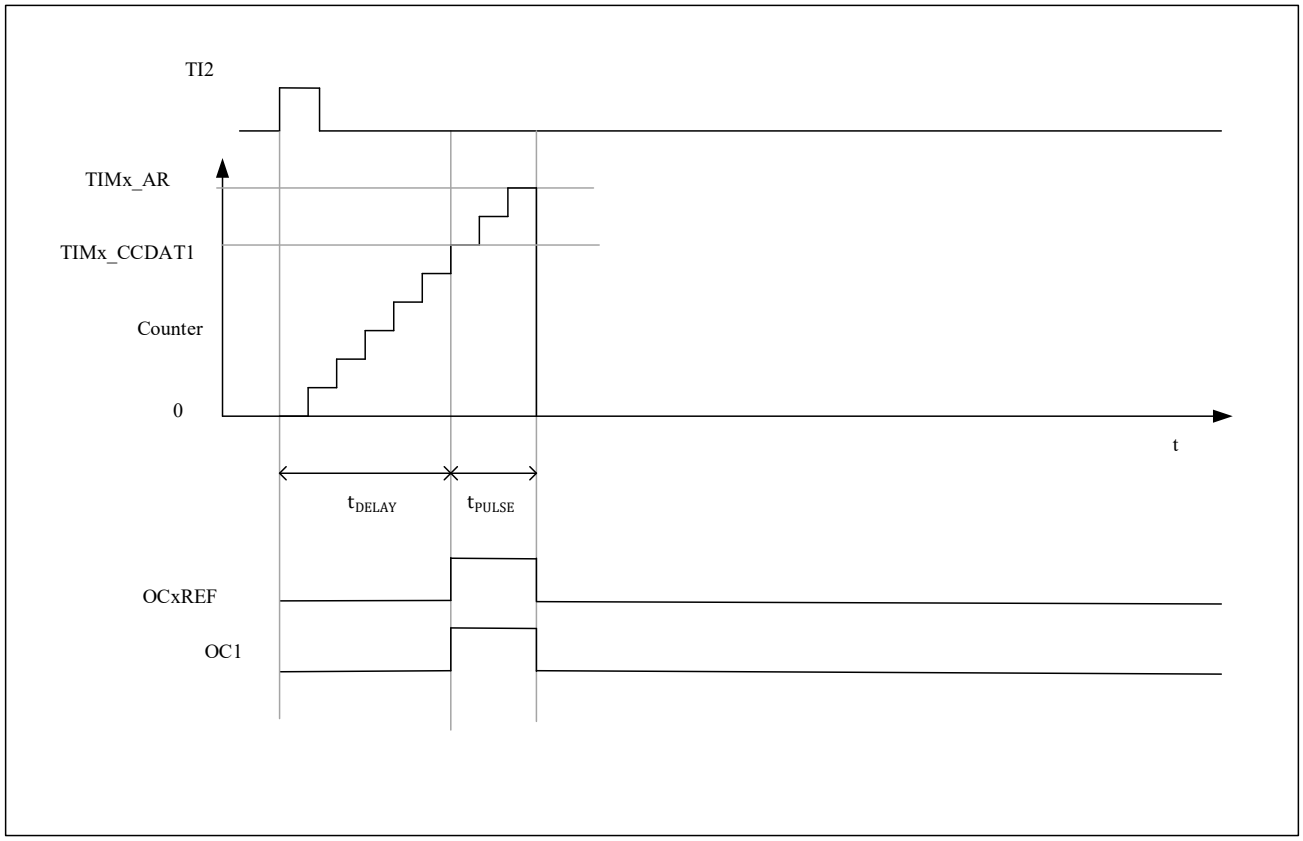
counter = CCDATx shadow register = 0 and OCxREF = '0', no compare event will be generated.

11.3.11 One-pulse Mode

In the one-pulse mode (ONEPM), a trigger signal is received, and a pulse t_{PULSE} with a controllable pulse width is generated after a controllable delay t_{DELAY}. The output mode needs to be configured as output compare mode or PWM mode. After selecting one-pulse mode, the counter will stop counting after the update event UEV is generated.

Figure 9-41 Example of One-pulse mode



The following is an example of a one-pulse mode:

A rising edge trigger is detected from the TI2 input, and a pulse with a width of t_{PULSE} is generated on OC1 after a delay of t_{DELAY}.

1. Counter configuration: count up, counter TIMx_CNT < TIMx_CCDAT1 ≤ TIMx_AR;

2. TI2FP2 is mapped to TI2, TIMx_CCMOD1.CC2SEL= '01'; TI2FP2 is configured for rising edge detection, TIMx_CCEN.CC2P= '0';

3. TI2FP2 acts as the trigger (TRGI) of the slave mode controller and starts the counter, TIMx_SMCTRL.TSEL= '110', TIMx_SMCTRL.SMSEL= '110' (trigger mode);

4. TIMx_CCDAT1 writes the count value to be delayed (t_{DELAY}), TIMx_AR - TIMx_CCDAT1 is the count value of the pulse width t_{PULSE};

5. Configure TIMx_CTRL1.ONEPM=1 to enable single pulse mode, configure TIMx_CCMOD1.OC1MD = '111'to

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select PWM2 mode;

6. Wait for an external trigger event on TI2, and a one pulse waveform will be output on OC1;

11.3.11.1 Special case: OCx fast enable:

In one-pulse mode, an edge is detected through the TIx input, and triggers the start of the counter to count to the comparison value and then output a pulse. These operations limit the minimum delay t_{DELAY} that can be achieved.

You can set TIMx_CCMODx.OCxFEN=1 to turn on OCx fast enable, after triggering the rising edge, the OCxREF signal will be forced to be converted to the same level as the comparison match occurs immediately, regardless of the comparison result. OCxFEN fast enable only takes effect when the channel mode is configured for PWM1 and PWM2 modes.

11.3.12 Clearing the OCxREF Signal on an External Event

If user set TIMx_CCMODx.OCxCEN=1, high level of ETRF input can be used to driven the OCxREF signal to low, and the OCxREF signal will remains low, until the next UEV happens. Only output compare and PWM modes can use this function. This cannot be used when it is in forced mode.

Here is an example for it. To control the current, user can connect the ETR signal to the output of a comparator, and the operation for ETR should be as follow:

- Set TIMx_SMCTRL.EXTPS=00 to disable the external trigger prescaler.
- Set TIMx_SMCTRL.EXCEN=0 to disable the external clock mode 2.
- Set TIMx_SMCTRL.EXTP and TIMx_SMCTRL.EXTF to configure the external trigger polarity and external trigger filter according to the need.

Here is an example for the case that when ETRF input becomes high, the behavior of OCxREF signal for different value of OCxCEN. Timer is set to be in PWM mode in this case.

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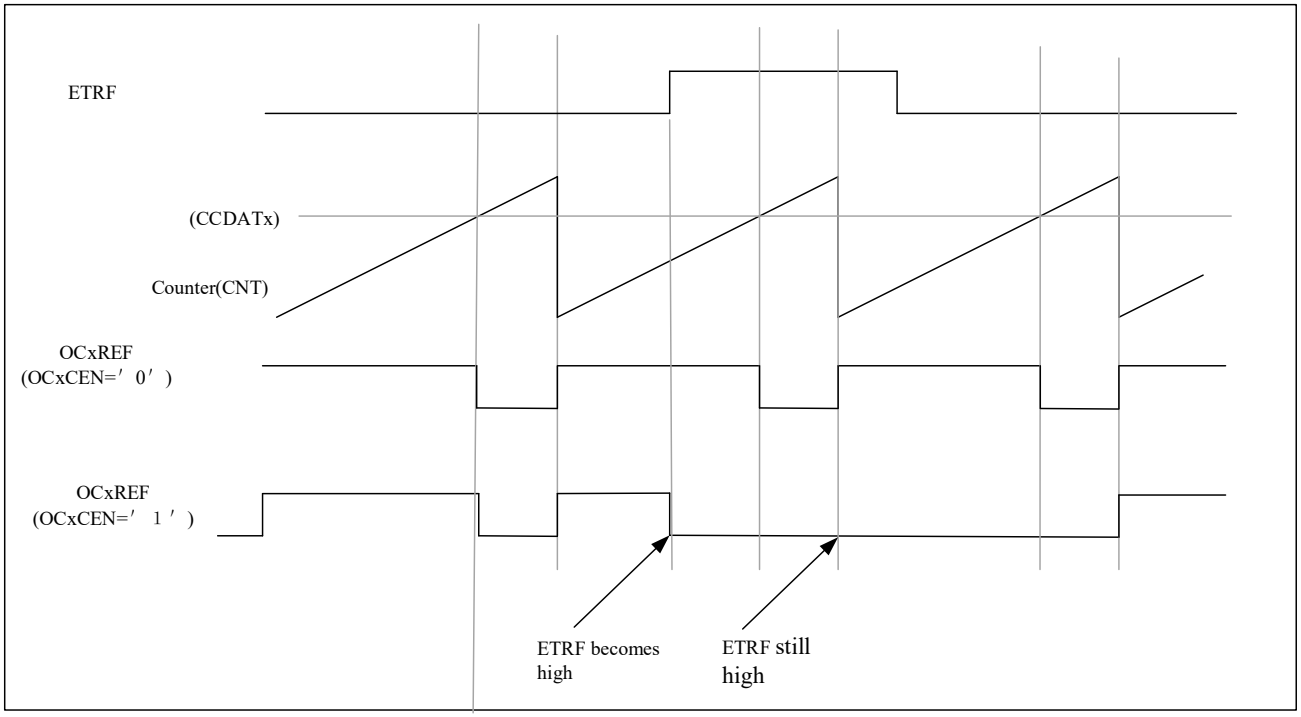
Figure 11-24 Clearing the OCxREF of TIMx



11.3.13 Complementary Outputs with Dead-time Insertion

Advanced-control timer can output two complementary signals, and manage the switching-off and switching-on of outputs. This is called dead-time. User should adjust dead-time depending on the devices connected to the outputs and their characteristics.

User can select the polarity of outputs by setting TIMx_CCEN.CCxP and TIMx_CCEN.CCxNP. And this selection is independently for each output.

User can control the complementary signals OCx and OCxN by setting the combination of several control bits, which are TIMx_CCEN.CCxEN, TIMx_CCEN.CCxNEN, TIMx_BKDT.MOEN, TIMx_CTRL2.OIx, TIMx_CTRL2.OIxN, TIMx_BKDT.OSSI, and TIMx_BKDT.OSSR. When switching to the IDLE state, the dead-time will be activated.

If user set TIMx_CCEN.CCxEN and TIMx_CCEN.CCxNEN at the same time, a dead-time will be insert. If there is a break circuit, the TIMx_BKDT.MOEN should be set too. There are 10-bit dead-time generators for each channel.

Reference waveform OCxREF can generates 2 outputs OCx and OCxN. And if OCx and OCxN are active high, the OCx ouput signal is the same as the reference signal and the OCxN output signal is the opposite of the reference signal. However, OCx output signal will be delayed relative to the reference rising edge and the OCxN output signal will be delayed relative to the reference falling edge. If the delay is greater than the width of the active OCx or OCxN output, the corresponding pulse will not generated.

The relationships between the output signals of the dead-time generator and the reference signal OCxREF are as follow.

Assume that TIMx_CCEN.CCxP=0, TIMx_CCEN.CCxNP=0, TIMx_BKDT.MOEN=1, TIMx_CCEN.CCxEN=1, TIMx_CCEN.CCxNEN=1.

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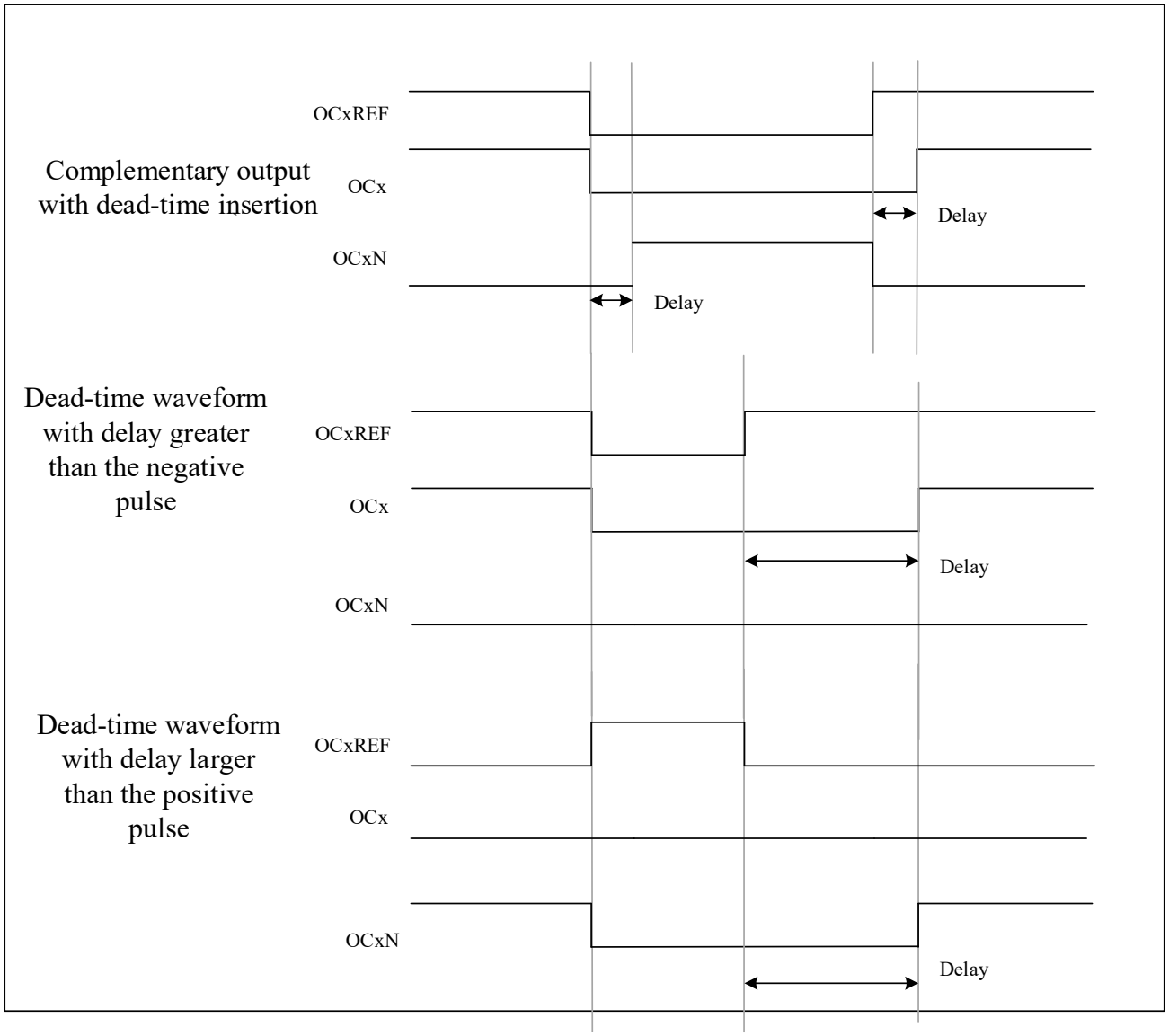
Figure 11-25 Complementary output with dead-time insertion



User can set TIMx_BKDT.DTGN to programme the dead-time delay for each of the channels.

11.3.13.1 Redirecting OCxREF to OCx or OCxN

User can set TIMx_CCEN.CCxEN and TIMx_CCEN.CCxNEN to re-directed OCxREF to the OCx output or to OCxN output, in output mode.

Here are two ways to use this function. When the complementary remains at its inactive level, user can use this function to send a specific waveform, such as PWM or static active level. User can also use this function to set both outputs in their inactive level or both outputs active and complementary with dead-time.

If user set TIMx_CCEN.CCxEN=0 and TIMx_CCEN.CCxNEN=1, it will not complemented, and OCxN will become active when OCxREF is high. On the other hand, if user set TIMx_CCEN.CCxEN=1 and TIMx_CCEN.CCxNEN=1, OCx will become active when OCxREF is high. On the contrary, OCxN will become active when OCxREF is low.

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11.3.14 Break Function

The output enable signals and inactive levels will be modified when setting the corresponding control bits when using the break function. However, the output of OCx and OCxN cannot at the active level at the same time no matter when, that is, (CCxP^OIx) ^(CCxNP^OIxN)!=0.

When multiple break signals are enabled, each break signal constitutes an OR logic. Here are some signal which can be the source of breaking.

- The break input pin
- A clock failure event, generated by the clock security system in the clock controller.
- A PVD failure event.
- Core Hardfault event.
- The output signal of the comparator (configured in the comparator module, high level break).
- By software through the TIMx_EVTGEN.BGN.

The break circuit will be disable after reset. And the MOEN bit will be low. User can set TIMx_BKDT.BKEN to enable the break function. The polarity of break input signal can be selected by setting TIMx_BKDT.BKP. User can modify the TIMx_BKDT.BKEN and TIMx_BKDT.BKP at the same time. After user set the TIMx_BKDT.BKEN and TIMx_BKDT.BKP, there is 1 APB clock cycle delay before the option take effect. Therefore, user need to wait 1 APB clock cycle to read back the value of the written bit.

The falling edge of MOEN can be asynchronous, so between the actual signal and the synchronous control bit, there set a resynchronization circuit. This circuit will cause a delay between the asynchronous and the synchronous signal. When user set TIMx_BKDT.MOEN while it is low, user need to insert a delay before reading the value. Because an asynchronous signal was written but user read the synchronous signal.

The behaviors that after a break occurs are as follow:

- TIMx_BKDT.MOEN will be cleared asynchronously, and then the outputs will be put in inactive state, idle state or reset state. The state of output is selected by setting TIMx_BKDT.OSSI. This will take effect even if the MCU oscillator is off.
- Once TIMx_BKDT.MOEN=0, the output of each output channel will be driven with the level programmed in TIMx_CTRL2.OIx. Timer will release the enable outputs(taken over by GPIO controller) if TIMx_BKDT.OSSI=0, otherwise it will remains high.
- If user choose to use complementary outputs, the behaviors of TIM are as follow
  - Depends on the polarity, the outputs will be set in reset state first. It is an asynchronous option so it still works even if there is no clock provided to the timer.
  - The dead-time generator will reactivated if the timer clock is still provided, and drive the outputs according to the value of TIMx_CTRL2.OIx and TIMx_CTRL2.OIxN after the dead-time when (CCxP ^ OIx) ^ (CCxNP^OIxN)! = 0, that is, the OCx and OCxN still cannot be driven to active level at the same time. Note that the dead-time will be longer than usual because of the resynchronization on MOEN (almost 2 cycles of ck_tim).
  - Timer will release the output control if TIMx_BKDT.OSSI=0. Otherwise, if the enable output was high, it

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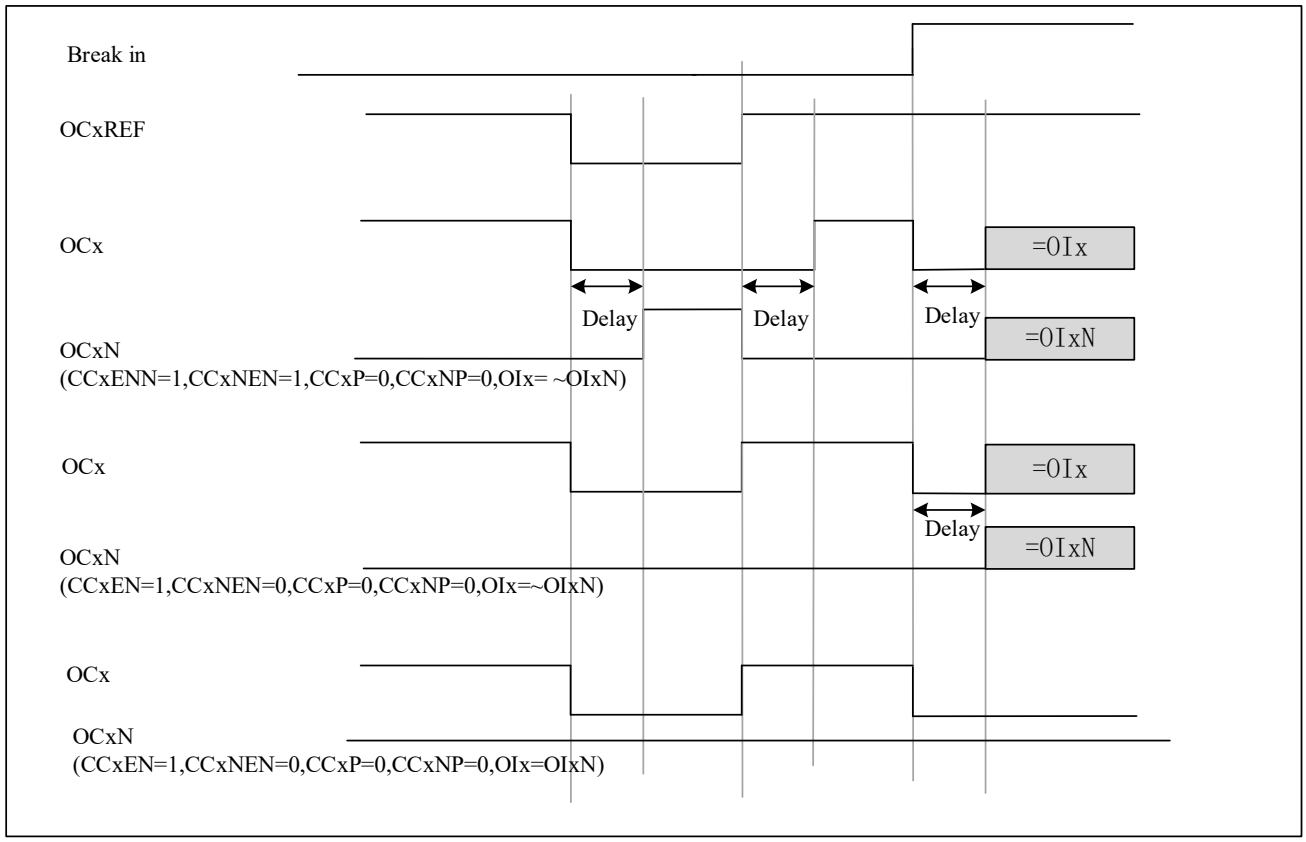
will remain high. If it was low, it will become high when TIMx_CCEN.CCxEN or TIMx_CCEN.CCxNEN is high.

- If TIMx_DINTEN.BIEN=1, when TIMx_STS.BITF=1, an interrupt will be generated.
- If user set TIMx_BKDT.AOEN, the TIMx_BKDT.MOEN will be set automatically when the next UEV happened. User can use this to regulate. If user did not set TIMx_BKDT.AOEN, the TIMx_BKDT.MOEN will remain low until been set 1 again. At this situation, user can use this for security. User can connect the break input to thermal sensors, alarm for power drivers, or other security components.
- When the break input is active, TIMx_BKDT.MOEN cannot be set automatically or by software at the same time, and the TIMx_STS.BITF cannot be cleared. Because the break inputs are active on level.

To insure the security of application, the break circuit has the write protection function, and there is break input and output management too. It allow user to freeze some parameters, such as dead-time duration, OCx/OCxN polarities and state when disabled, OCxMD configurations, break enable and polarity. User can choose one of the 3 levels of protection to use by setting TIMx_BKDT.LCKCFG. However, the TIMx_BKDT.LCKCFG can only be written once after an MCU reset.

An example for output behavior in response to a break is as follow

Figure 11-26 Output behavior in response to a break



11.3.15 Debug Mode

When the microcontroller is in debug mode (the Cortex-M4 core halted), depending on the DBG_CTRL.TIMx_STOP configuration in the DBG module, the TIMx counter can either continue to work normally or stop. For more details,

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see 29.4.3.

11.3.16 TIMx and external Trigger Synchronization

TIMx timers can be synchronized by a trigger in slave modes (reset, trigger and gated).

11.3.16.1 Slave mode: Reset mode

In reset mode, the trigger event can reset the counter and the prescaler updates the preload registers TIMx_AR, TIMx_CCDATx, and generates the update event UEV (TIMx_CTRL1.UPRS=0).

The following is an example of a reset mode:

1. Channel 1 is configured as input to detect the rising edge of TI1 (TIMx_CCMOD1.CC1SEL=01, TIMx_CCEN.CC1P=0);

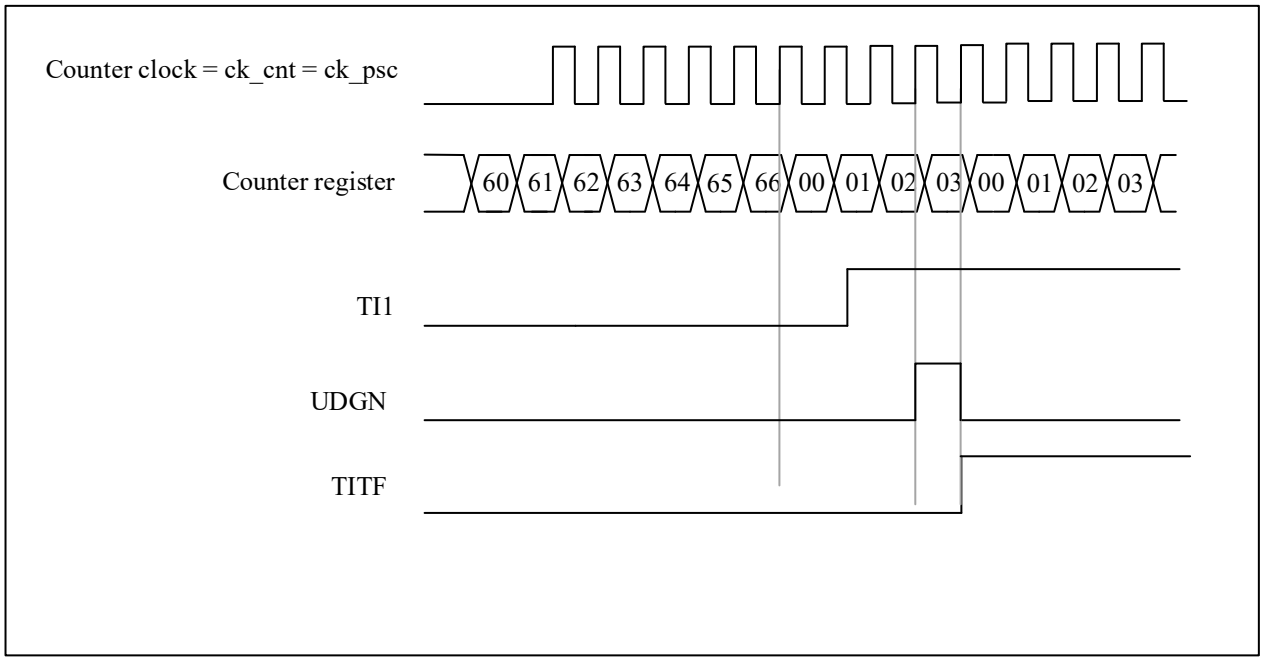
2. The slave mode is selected as reset mode (TIMx_SMCTRL.SMSEL=100), and the trigger input is selected as TI1 (TIMx_SMCTRL.TSEL=101);

3. Start counter (TIMx_CTRL1.CNTEN = 1)

After starting the timer, when TI1 detects a rising edge, the counter resets and restarts counting, and the trigger flag is set (TIMx_STS.TITF=1);

The delay between the rising edge on TI1 and the actual reset of the counter is due to the resynchronization circuit on TI1 input.

Figure 11-27 Control circuit in reset mode



11.3.16.2 Slave mode: Trigger mode

In trigger mode, the trigger event (rising edge/falling edge) of the input port can trigger the counter to start counting.

The following is an example of a trigger pattern:

1. Channel 2 is configured as input to detect the rising edge of TI2 (TIMx_CCMOD1.CC2SEL=01,

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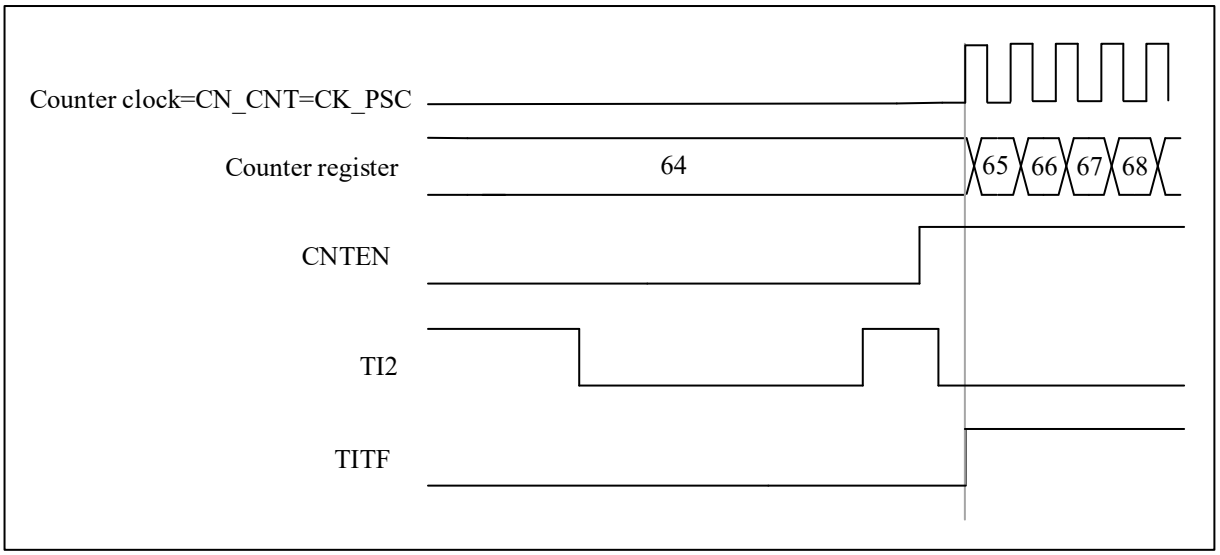
TIMx_CCEN.CC2P=0);

2. Select from mode to trigger mode (TIMx_SMCTRL.SMSEL=110), select TI2 for trigger input (TIMx_SMCTRL.TSEL=110);

When TI2 detects a rising edge, the counter starts counting, and the trigger flag is set (TIMx_STS.TITF=1);

The delay between the rising edge on TI2 and the actual start of the counter is due to the resynchronization circuit on TI2 input.

Figure 11-28 Control circuit in Trigger mode



11.3.16.3 Slave mode: Gated mode

In gate control mode, the level polarity of the input port can control whether the counter counts.

The following is an example of a gated pattern:

1. Channel 1 is configured as input detection active low on TI1 (TIMx_CCMOD1.CC1SEL=01, TIMx_CCEN.CC1P=1);

2. Select the slave mode as the gated mode (TIMx_SMCTRL.SMSEL=101), and select TI1 as the trigger input (TIMx_SMCTRL.TSEL=101);

3. Start counter (TIMx_CTRL1.CNTEN = 1)

When TI1 detects that the level changes from low to high, the counter stops counting, and when TI1 detects that the level changes from high to low, the counter starts counting, and the trigger flag will be set when it starts or stops counting (TIMx_STS.TITF=1);

The delay between the rising edge on TI1 and the actual stop of the counter is due to the resynchronization circuit on TI1 input.

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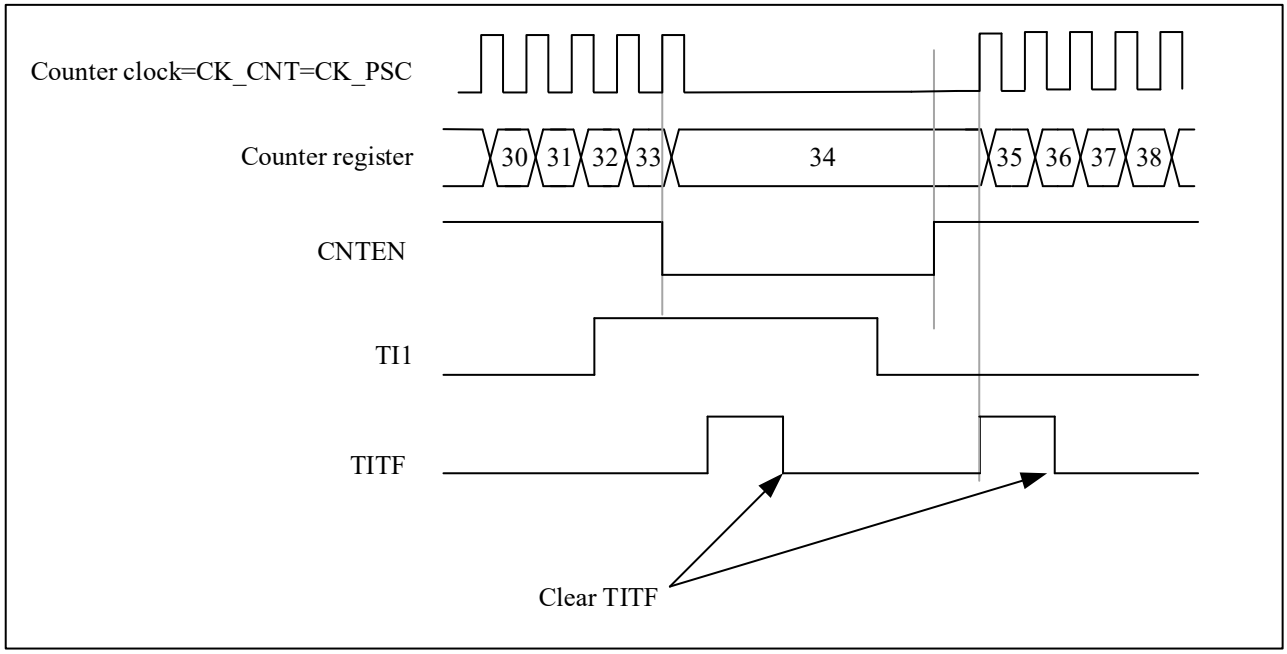
Figure 11-29 Control circuit in Gated mode



11.3.16.4 Slave mode: Trigger Mode + External Clock Mode 2

In reset mode, trigger mode and gate control mode, the counter clock can be selected as external clock mode 2, and the ETR signal is used as the external clock source input. At this time, the trigger selection needs to select non-ETRF (TIMx_SMCTRL.TSEL=111).

Here is an example:

1. Channel 1 is configured as input to detect the rising edge of TI1 (TIMx_CCMOD1.CC1SEL=01, TIMx_CCEN.CC1P=0);

2. Enable external clock mode 2 (TIMx_SMCTRL.EXCEN=1), select rising edge for external trigger polarity (TIMx_SMCTRL.EXTP=0), select slave mode as trigger mode (TIMx_SMCTRL.SMSEL=110), select TI1 for trigger input (TIMx_SMCTRL.TSEL=101);

When TI1 detects a rising edge, the counter starts counting on the rising edge of ETR, and the trigger flag is set (TIMx_STS.TITF=1);

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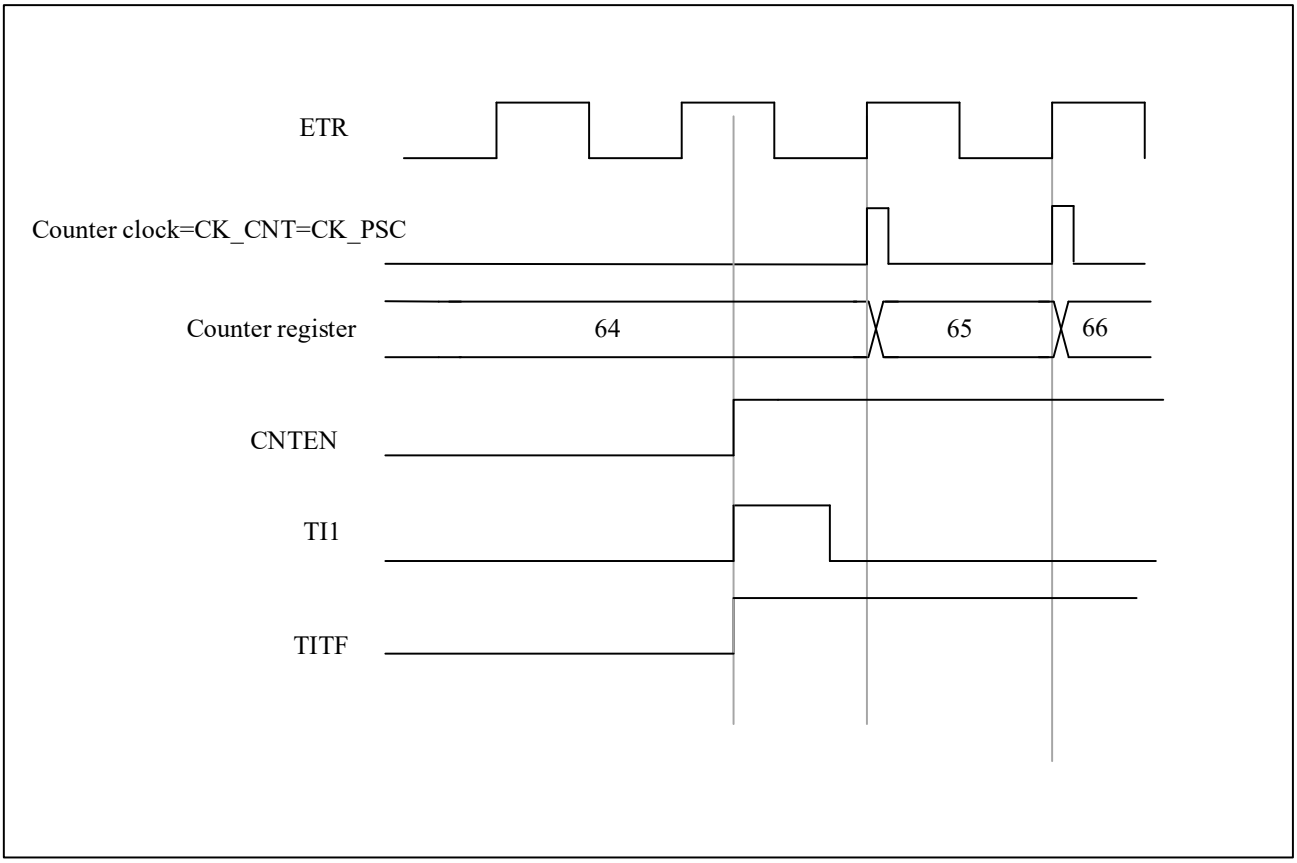
Figure 11-30 Control circuit in Trigger Mode + External Clock Mode2



11.3.17 Timer Synchronization

All TIM timers are internally connected for timer synchronization or chaining. For more details, see 12.3.14.

11.3.18 6-step PWM Generation

In order to modify the configuration of all channels at the same time, the configuration of the next step can be set in advance (the preloaded bits are OCxMD, CCxEN and CCxNEN). When a COM commutation event occurs, the OCxMD, CCxEN, and CCxNEN preload bits are transferred to the shadow register bits.

COM commutation event generation method:

1. The software sets TIMx_EVTGEN.CCUDGN;

2. Generated by hardware on the rising edge of TRGI;

When a COM commutation event occurs, the TIMx_STS.COMITF flag will be set, enabling interrupts (TIMx_DINTEN.COMIEN) will generate interrupts, and enabling DMA requests (TIMx_DINTEN.COMDEN) will generate DMA requests.

The following figure shows the output timing diagram of OCx and OCxN when a COM commutation event occurs in three different configurations:

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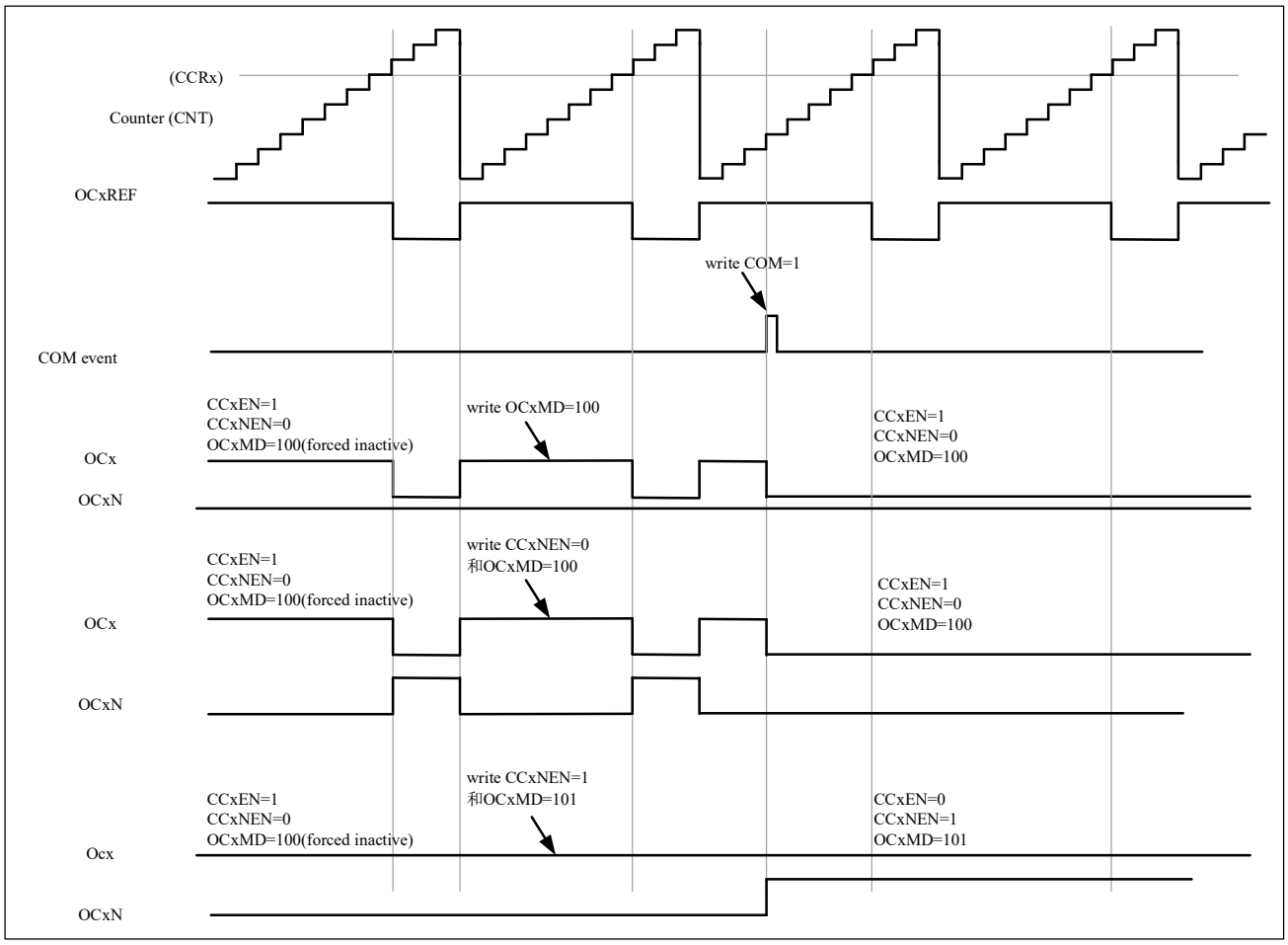
Figure 11-31 6-step PWM generation, COM example (OSSR=1)



11.3.19 Encoder Interface Mode

The encoder uses two inputs TI1 and TI2 as an interface and the counter counts on every edge change on TI1FP1 or TI2FP2. The counting direction is automatically controlled by hardware TIMx_CTRL1.DIR. There are three types of encoder counting modes:

1. The counter only counts on the edge of TI1, TIMx_SMCTRL.SMSEL = ‘001’;

2. The counter only counts on the edge of TI2, TIMx_SMCTRL.SMSEL =’010’;

3. The counter counts on the edges of TI1 and TI2 at the same time, TIMx_SMCTRL.SMSEL = ‘011’;

The encoder interface is equivalent to using an external clock with direction selection, and the counter only counts continuously between 0 and the auto-reload value (TIMx_AR.AR [15:0]). Therefore, it is necessary to configure the auto-reload register TIMx_AR in advance.

Note: Encoder mode and external clock mode 2 are not compatible and must not be selected together.

The relationship between the counting direction and the encoder signal is shown in **Table 11-1 Counting direction versus encoder signals**:

Table 11-1 Counting direction versus encoder signals

	Level on opposite signals	TI1FP1 signal	TI2FP2 signal

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Active edge	(TI1FP1 forTI2, TI2FP2 for TI1)	Rising	Falling	Rising	Falling
Counting only at TI1	High	Counting down	Counting up	Don't count	Don't count
	Low	Counting up	Counting down	Don't count	Don't count
Counting only at TI2	High	Don't count	Don't count	Counting up	Counting down
	Low	Don't count	Don't count	Counting down	Counting up
Counting on TI1 and TI2	High	Counting down	Counting up	Counting up	Counting down
	Low	Counting up	Counting down	Counting down	Counting up

Here is an example of an encoder with dual edge triggering selected to suppress input jitter:

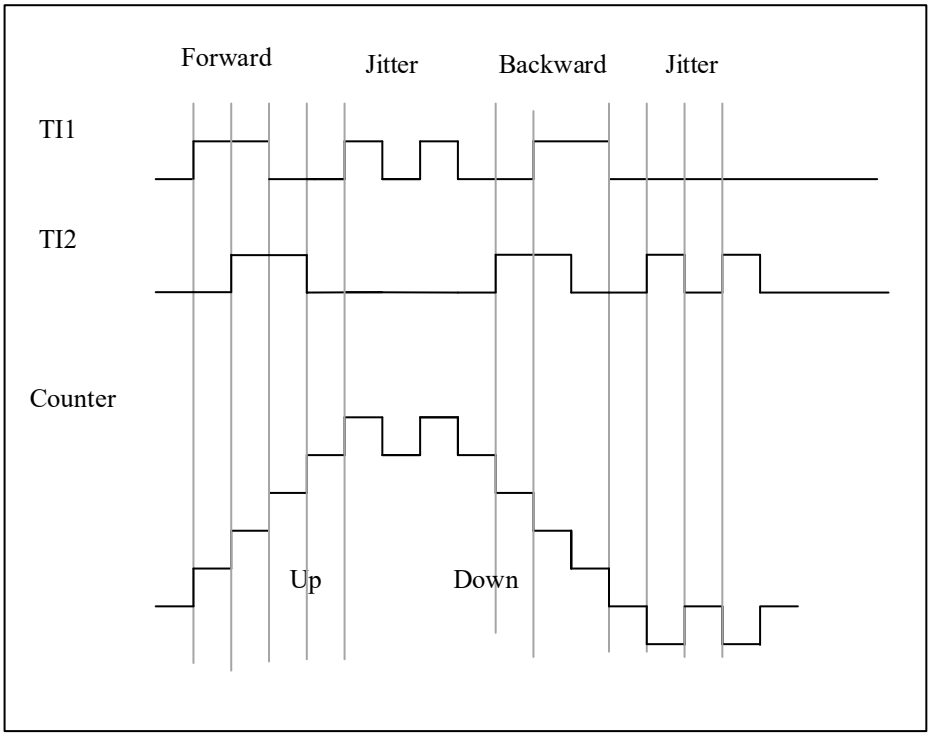
1. IC1FP1 is mapped to TI1 (TIMx_CCMOD1.CC1SEL= '01'), IC1FP1 is not inverted (TIMx_CCEN.CC1P= '0');

2. IC1FP2 is mapped to TI2 (TIMx_CCMOD2.CC2SEL= '01'), IC2FP2 is not inverted (TIMx_CCEN.CC2P= '0');

3. The input is valid on both rising and falling edges (TIMx_SMCTRL.SMSEL = '011');

4. Enable counter TIMx_CTRL1.CNTEN= '1';

Figure 11-32 Example of counter operation in encoder interface mode



The following figure shows the example of counter behavior when IC1FP1 polarity is inverted (CC1P= '1', other configurations are the same as above)

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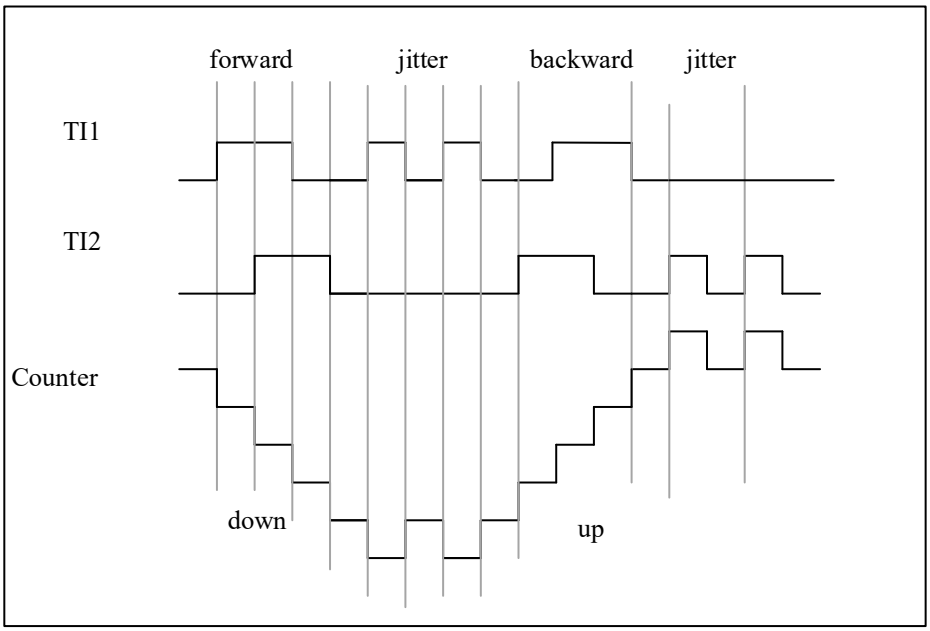
Figure 11-33 Encoder interface mode example with IC1FP1 polarity inverted



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11.3.20 Interfacing with Hall Sensor

Connect the Hall sensor to the three input pins (CC1, CC2 and CC3) of the timer, and then select the XOR function to pass the inputs of TIMx_CH1, TIMx_CH2 and TIMx_CH3 through the XOR gate as the output of TI1 to channel 1 for capture signal.

The timer needs to be configured as the reset mode in slave mode (TIMx_SMCTRL.SMSEL= '100'); the edge of the trigger select TI1 triggers TI1F_ED (TIMx_SMCTRL.TSEL= '100'), any change in the Hall 3 inputs will trigger the counter to recount, so it is used as a time reference; the capture/compare channel 1 is configured to capture the TRC signal in capture mode (TIMx_CCMOD1.CC1SEL= '11'), which is used to calculate the two input time intervals, thereby reflecting the motor speed.

Select timer channel 2 to output pulses to the advanced timer to trigger the COM event of the advanced timer to update the control bits of the output PWM. The trigger selection of the advanced timer needs to select the corresponding internal trigger signal (TIMx_SMCTRL.TSEL="ITRx"), the capture/compare preload control bit needs to be configured to support preload (TIMx_CTRL2.CCPCTL=1) and support the rising edge of TRGI Trigger an update (TIMx_CTRL2.CCUSEL=1).

This example is shown in the following figure.

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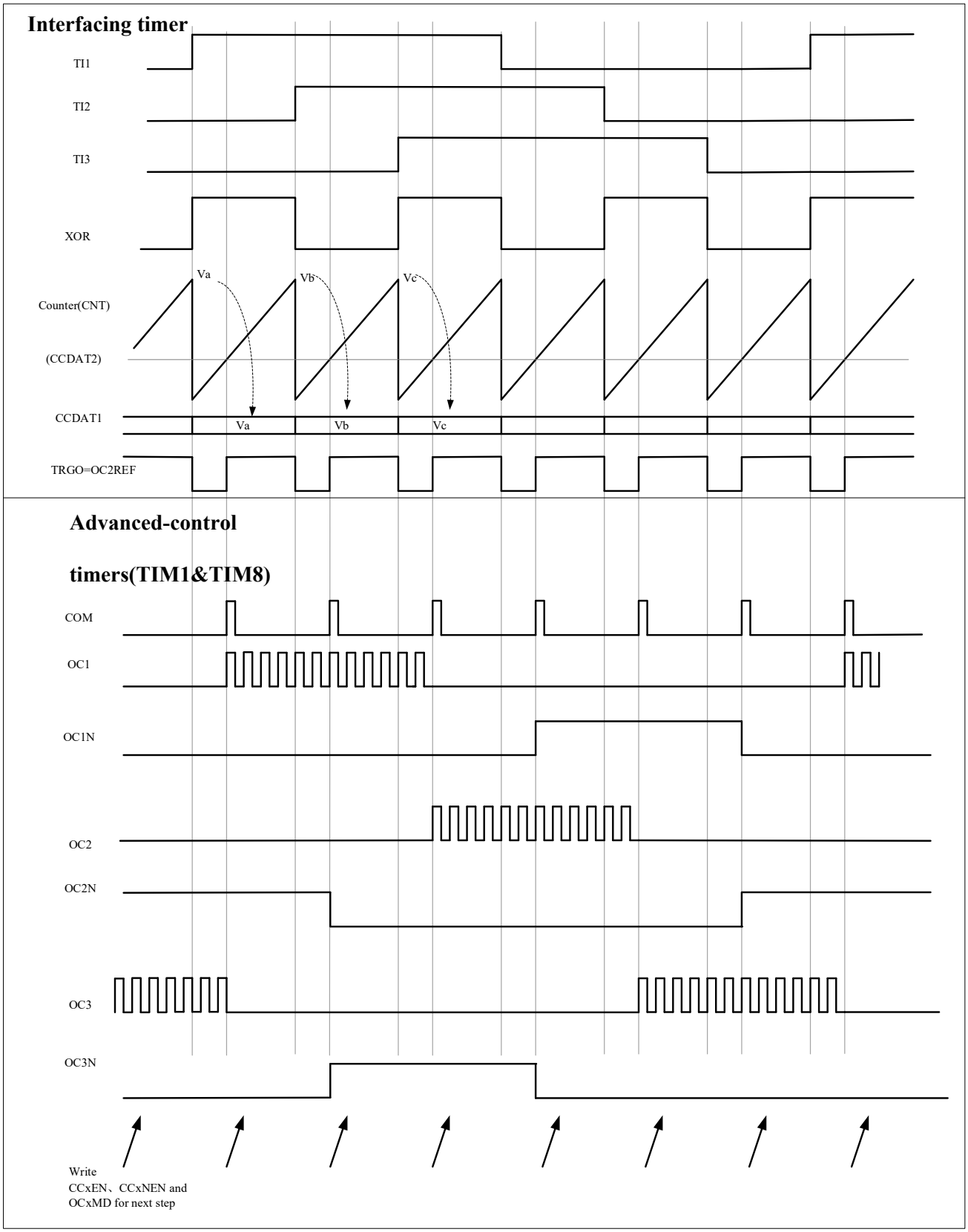
Figure 11-34 Example of Hall sensor interface



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11.4 TIMx register (x=1, 8)

For abbreviations used in registers, see section 1.1.

These peripheral registers can be operated as half word (16-bits) or one word (32-bits).

11.4.1 Register Overview

Table 11-2 Register map and reset value

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
000h	TIMx_CTRL1	Reserved														PBKPEN	LBKPEN	CLRSEL	Reserved	Reserved	Reserved	C1SEL	IOMBKPEN	CLKD[1:0]		ARPEN	CAMSEL[1:0]		DIR	ONEPM	UPRS	UPDIS	CNTEN
	Reset Value															0	0	0				0	0	0	0	0	0	0	0	0	0	0	0
004h	TIMx_CTRL2	Reserved													OI6	Reserved	OI5	Reserved	OI4	OI3N	OI3	OI2N	OI2	OI1N	OI1	TI1SEL	MMSEL[2:0]			CCDSEL	CCUSEL	Reserved	CCPCTL
	Reset Value														0		0		0	0	0	0	0	0	0	0	0	0	0	0	0		0
008h	TIMx_SMCTRL	Reserved																EXTP	EXCEN	EXTPS[1:0]		EXTF[3:0]				MSMD	TSEL[2:0]			Reserved	SMSEL[2:0]		
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0		0	0	0
00Ch	TIMx_DINTEN	Reserved																	TDEN	COMDEN	CC4DEN	CC3DEN	CC2DEN	CC1DEN	UDEN	BIEN	TIEN	COMIEN	CC4IEN	CC3IEN	CC2IEN	CC1IEN	UIEN
	Reset Value																		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
010h	TIMx_STS	Reserved														CC6ITF	CC5ITF	Reserved			CC4OCF	CC3OCF	CC2OCF	CC1OCF	Reserved	BITF	TITF	COMITF	CC4ITF	CC3ITF	CC2ITF	CC1ITF	UDITF
	Reset Value															0	0				0	0	0	0		0	0	0	0	0	0	0	0
014h	TIMx_EVTGEN	Reserved																								BGN	TGN	CCUDGN	CC4GN	CC3GN	CC2GN	CC1GN	UDGN
	Reset Value																									0	0	0	0	0	0	0	0
018h	TIMx_CCMOD1	Reserved																OC2CEN	OC2MD[2:0]			OC2PEN	OC2FEN	CC2SEL[1:0]		OC1CEN	OC1MD[2:0]			OC1PEN	OC1FEN	CC1SEL[1:0]	
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	TIMx_CCMOD1	Reserved																IC2F[3:0]				IC2PSC[1:0]		CC2SEL[1:0]		IC1F[3:0]				IC1PSC[1:0]		CC1SEL[1:0]	
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
01Ch	TIMx_CCMOD2	Reserved																OC4CEN	OC4MD[2:0]			OC4PEN	OC4FEN	CC4SEL[1:0]		OC3CEN	OC3MD[2:0]			OC3PEN	OC3FEN	CC3SEL[1:0]	
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	TIMx_CCMOD2	Reserved																IC4F[3:0]				IC4PSC[1:0]		CC4SEL[1:0]		IC3F[3:0]				IC3PSC[1:0]		CC3SEL[1:0]	
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
020h	TIMx_CCEN	Reserved											CC6P	CC6EN	Reserved	CC5P	CC5EN	Reserved		CC4P	CC4EN	CC3NP	CC3NEN	CC3P	CC3EN	CC2NP	CC2NEN	CC2P	CC2EN	CC1NP	CC1NEN	CC1P	CC1EN
	Reset Value												0	0		0	0			0	0	0	0	0	0	0	0	0	0	0	0	0	0

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024h	TIMx_CNT	Reserved	CNT[15:0]														
	Reset Value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
028h	TIMx_PSC	Reserved	PSC[15:0]														
	Reset Value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
02Ch	TIMx_AR	Reserved	AR[15:0]														
	Reset Value		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
030h	TIMx_REPCNT	Reserved	REPCNT[7:0]														
	Reset Value		0	0	0	0	0	0	0	0							
034h	TIMx_CCDAT1	Reserved	CCDAT1[15:0]														
	Reset Value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
038h	TIMx_CCDAT2	Reserved	CCDAT2[15:0]														
	Reset Value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
03Ch	TIMx_CCDAT3	Reserved	CCDAT3[15:0]														
	Reset Value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
040h	TIMx_CCDAT4	Reserved	CCDAT4[15:0]														
	Reset Value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
044h	TIMx_BKDT	Reserved	MOEN	AOEN	BKP	BKEN	OSSR	OSSI	LCKCFG[1:0]		DTGN[7:0]						
	Reset Value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
048h	TIMx_DCTRL	Reserved	DBLEN[4:0]					Reserved	DBADDR[4:0]								
	Reset Value		0	0	0	0	0		0	0	0	0	0				
04Ch	TIMx_DADDR	Reserved	BURST[15:0]														
	Reset Value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
050h	TIMx_CCMOD3	Reserved	OC6CEN	OC6MD[2:0]			OC6PEN	OC6FEN	Reserved		OC5CEN	OC5MD[2:0]			OC5PEN	OC5FEN	Reserved
	Reset Value		0	0	0	0	0	0			0	0	0	0	0	0	
054h	TIMx_CCDAT5	Reserved	CCDAT5[15:0]														
	Reset Value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
058h	TIMx_CCDAT6	Reserved	CCDAT6[15:0]														
	Reset Value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

11.4.2 Control Register 1 (TIMx_CTRL1)

Offset address: 0x00

Reset value: 0x0000 0000

31																18	17	16
Reserved																	PBKPEN	LOCKUPEN
																	rw	rw
15	14				12	11	10	9	8	7	6	5	4	3	2	1	0	
CLRSEL	Reserved					C1SEL	IOM BKPEN	CLKD[1:0]		ARPEN	CAMSEL[1:0]		DIR	ONEPM	UPRS	UPDIS	CNTEN	
rw						rw	rw	rw		rw	rw		rw	rw	rw	rw	rw	

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Bit field	Name	Description
31:18	Reserved	Reserved, the reset value must be maintained
17	PBKPEN	PVD as BKP enable 0: Disable 1: Enable *Note:Before operating this bit, the extended mode of the chip must be turned on (set PWR_CTRL3.EXMODE)*
16	LBKPEN	LockUp as BKP enable 0: Disable 1: Enable *Note:Before operating this bit, the extended mode of the chip must be turned on (set PWR_CTRL3.EXMODE)*
15	CLRSEL	OCxREF clear selection 0: Select the external OCxREF clear from ETR 1: Select the internal OCxREF clear from comparator *Note:Before operating this bit, the extended mode of the chip must be turned on (set PWR_CTRL3.EXMODE)*
14:12	Reserved	Reserved, the reset value must be maintained
11	C1SEL	Channel 1 selection 0: Select external CH1 signal from IOM 1: Select internal CH1 signal from COMP *Note:Before operating this bit, the extended mode of the chip must be turned on (set PWR_CTRL3.EXMODE)*
10	IOMBKPEN	Enabling IOM as BKP 0: Enable. Select external break (from IOM) signal. 1: Disable. Select internal break (from COMP) signal. *Note:Before operating this bit, the extended mode of the chip must be turned on (set PWR_CTRL3.EXMODE)*
9:8	CLKD[1:0]	Clock division CLKD[1:0] indicates the division ratio between CK_INT (timer clock) and DTS (clock used for dead-time generator and digital filters (ETR, TIx)) 00: $t_{DTS} = t_{CK\_INT}$ 01: $t_{DTS} = 2 \times t_{CK\_INT}$ 10: $t_{DTS} = 4 \times t_{CK\_INT}$ 11: Reserved, do not use this configuration
7	ARPEN	ARPEN: Auto-reload preload enable 0: Shadow register disable for TIMx_AR register 1: Shadow register enable for TIMx_AR register
6:5	CAMSEL[1:0]	Center-aligned mode selection 00: Edge-aligned mode. TIMx_CTRL1.DIR specifies up-counting or down-counting. 01: Center-aligned mode 1. The counter counts in center-aligned mode, and the output compare interrupt flag bit is set to 1 when down-counting. 10: Center-aligned mode 2. The counter counts in center-aligned mode, and the output compare interrupt flag bit is set to 1 when up-counting.

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Bit field	Name	Description
		11: Center-aligned mode 3. The counter counts in center-aligned mode, and the output compare interrupt flag bit is set to 1 when up-counting or down-counting. *Note: Switching from edge-aligned mode to center-aligned mode is not allowed when the counter is still enabled (TIMx_CTRL1.CNTEN = 1).*
4	DIR	Direction 0: Up-counting 1: Down-counting *Note: This bit is read-only when the counter is configured in center-aligned mode or encoder mode.*
3	ONEPM	One-pulse mode 0: Disable one-pulse mode, the counter counts are not affected when an update event occurs. 1: Enable one-pulse mode, the counter stops counting when the next update event occurs (clearing TIMx_CTRL1.CNTEN bit)
2	UPRS	Update request source This bit is used to select the UEV event sources by software. 0: If update interrupt or DMA request is enabled, any of the following events will generate an update interrupt or DMA request: – Counter overflow/underflow – The TIMx_EVTGEN.UDGN bit is set – Update generation from the slave mode controller 1: If update interrupt or DMA request is enabled, only counter overflow/underflow will generate update interrupt or DMA request
1	UPDIS	Update disable This bit is used to enable/disable the Update event (UEV) events generation by software. 0: Enable UEV. UEV will be generated if one of following condition been fulfilled: – Counter overflow/underflow – The TIMx_EVTGEN.UDGN bit is set – Update generation from the slave mode controller Shadow registers will update with preload value. 1: UEV disabled. No update event is generated, and the shadow registers (AR, PSC, and CCDATx) keep their values. If the TIMx_EVTGEN.UDGN bit is set or a hardware reset is issued by the slave mode controller, the counter and prescaler are reinitialized.
0	CNTEN	Counter Enable 0: Disable counter 1: Enable counter *Note: external clock, gating mode and encoder mode can only work after TIMx_CTRL1.CNTEN bit is set in the software. Trigger mode can automatically set TIMx_CTRL1.CNTEN bit by hardware.*

11.4.3 Control Register 2 (TIMx_CTRL2)

Offset address: 0x04

Reset value: 0x0000 0000

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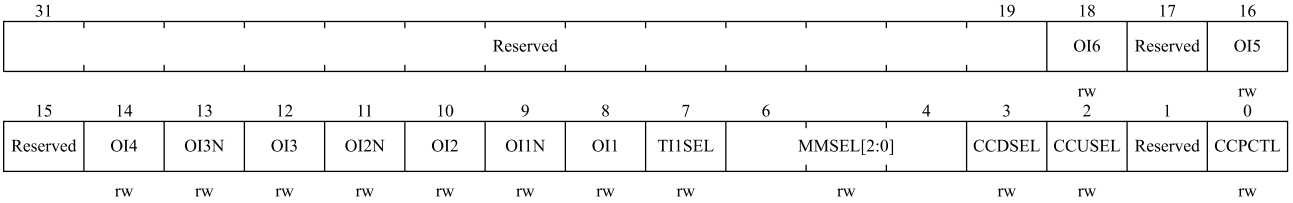

Bit field	Name	Description
31:19	Reserved	Reserved, the reset value must be maintained
18	OI6	Output idle state 6 (OC6 output). See TIMx_CTRL2.OI1 bit.
17	Reserved	Reserved, the reset value must be maintained
16	OI5	Output idle state 5 (OC5 output). See TIMx_CTRL2.OI1 bit.
15	Reserved	Reserved, the reset value must be maintained
14	OI4	Output idle state 4 (OC4 output). See TIMx_CTRL2.OI1 bit.
13	OI3N	Output idle state 3 (OC3N output). See TIMx_CTRL2.OI1N bits.
12	OI3	Output idle state 3 (OC3 output). See TIMx_CTRL2.OI1 bit.
11	OI2N	Output idle state 2 (OC2N output). See TIMx_CTRL2.OI1N bits.
10	OI2	Output idle state 2 (OC2 output). See TIMx_CTRL2.OI1 bit.
9	OI1N	Output Idle state 1 (OC1N Output) 0: When TIMx_BKDT.MOEN = 0, after dead-time OC1N = 0 1: When TIMx_BKDT.MOEN = 0, after dead-time OC1N = 1
8	OI1	Output Idle state 1 0: When TIMx_BKDT.MOEN = 0, if OC1N is implemented, after dead-time OC1 = 0 1: When TIMx_BKDT.MOEN = 0, if OC1N is implemented, after dead-time OC1 = 1
7	TI1SEL	TI1 selection 0: TIMx_CH1 pin connected to TI1 input. 1: TIMx_CH1, TIMx_CH2, and TIMx_CH3 pins are XOR connected to the TI1 input.
6:4	MMSEL[2:0]	Master Mode Selection These 3 bits (TIMx_CTRL2. MMSEL [2:0]) are used to select the synchronization information (TRGO) sent to the slave timer in the master mode. Possible combinations are as follows: 000: Reset –When the TIMx_EVTGEN.UDGN is set or a reset is generated by the slave mode controller, a TRGO pulse occurs. And in the latter case, the signal on TRGO is delayed compared to the actual reset. 001: Enable - The TIMx_CTRL1.CNTEN bit is used as the trigger output (TRGO). Sometimes you need to start multiple timers at the same time or enable slave timer for a period of time. The counter enable signal is set when TIMx_CTRL1.CNTEN bit is set or the trigger input in gated mode is high. When the counter enable signal is controlled by the trigger input, there is a delay on TRGO except if the master/slave mode is selected (see the description of the TIMx_SMCTRL.MSMD bit). 010: Update - The update event is selected as the trigger output (TRGO). For example, a master timer clock can be used as a slave timer prescaler.

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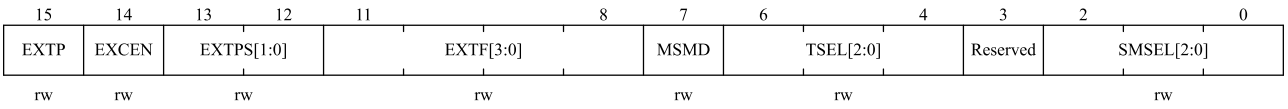
Bit field	Name	Description
		011: Compare pulse - Triggers the output to send a positive pulse (TRGO) when the TIMx_STS.CC1ITF is to be set (even if it is already high), when a capture or a comparison succeeds. 100: Compare - OC1REF signal is used as the trigger output (TRGO). 101: Compare - OC2REF signal is used as the trigger output (TRGO). 110: Compare - OC3REF signal is used as the trigger output (TRGO). 111: Compare - OC4REF signal is used as the trigger output (TRGO).
3	CCDSEL	Capture/compare DMA selection 0: When a CCx event occurs, a DMA request for CCx is sent. 1: When an update event occurs, a DMA request for CCx is sent.
2	CCUSEL	Capture/compare control update selection 0: If TIMx_CTRL2.CCPCTL = 1, they can only be updated by setting CCUDGN bits 1: If TIMx_CTRL2.CCPCTL = 1, they can be updated by setting CCUDGN bits or a rising edge on TRGI. *Note: This bit only applied to channels with complementary outputs.*
1	Reserved	Reserved, the reset value must be maintained
0	CCPCTL	Capture/ Compare preloaded control 0: No preloading of CCxEN, CCxNEN and OCxMD bits occurs. 1: Preloading of CCxEN, CCxNEN and OCxMD bits occurs. they are updated only when a commutation event COM occurs (CCUDGN bit set or rising edge on TRGI depending on CCUSEL bit) *Note: This bit only applied to channels with complementary outputs.*

11.4.4 Slave Mode Control Register (TIMx_SMCTRL)

Offset address: 0x08

Reset value: 0x0000



Bit field	Name	Description
15	EXTP	External trigger polarity This bit is used to select whether the trigger operation is to use ETR or the inversion of ETR. 0: ETR active at high level or rising edge. 1: ETR active at low level or falling edge.
14	EXCEN	External clock enable This bit is used to enable external clock mode 2, and the counter is driven by any active edge on the ETRF signal in this mode. 0: External clock mode 2 disable. 1: External clock mode 2 enable.

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Bit field	Name	Description
		Note 1: When external clock mode 1 and external clock mode 2 are enabled at the same time, the input of the external clock is ETRF. *Note 2: The following slave modes can be used simultaneously with external clock mode 2: reset mode, gated mode and trigger mode; However, TRGI cannot connect to ETRF (TIMx_SMCTRL.TSEL ≠ '111').* *Note 3: Setting the TIMx_SMCTRL.EXCEN bit has the same effect as selecting external clock mode 1 and connecting TRGI to ETRF (TIMx_SMCTRL.SMSEL = 111 and TIMx_SMCTRL.TSEL = 111).*
13:12	EXTPS[1:0]	External trigger prescaler The frequency of the external trigger signal ETRP must be at most 1/4 of TIMxCLK frequency. When a faster external clock is input, a prescaler can be used to reduce the frequency of ETRP. 00: Prescaler disable 01: ETRP frequency divided by 2 10: ETRP frequency divided by 4 11: ETRP frequency divided by 8
11:8	EXTF[3:0]	External trigger filter These bits are used to define the frequency at which the ETRP signal is sampled and the bandwidth of the ETRP digital filtering. In effect, the digital filter is an event counter that generates a validate output after consecutive N events are recorded. 0000: No filter, sampling at f_{DTS} 0001: $f_{SAMPLING} = f_{CK\_INT}$, N = 2 0010: $f_{SAMPLING} = f_{CK\_INT}$, N = 4 0011: $f_{SAMPLING} = f_{CK\_INT}$, N = 8 0100: $f_{SAMPLING} = f_{DTS}/2$, N = 6 0101: $f_{SAMPLING} = f_{DTS}/2$, N = 8 0110: $f_{SAMPLING} = f_{DTS}/4$, N = 6 0111: $f_{SAMPLING} = f_{DTS}/4$, N = 8 1000: $f_{SAMPLING} = f_{DTS}/8$, N = 6 1001: $f_{SAMPLING} = f_{DTS}/8$, N = 8 1010: $f_{SAMPLING} = f_{DTS}/16$, N = 5 1011: $f_{SAMPLING} = f_{DTS}/16$, N = 6 1100: $f_{SAMPLING} = f_{DTS}/16$, N = 8 1101: $f_{SAMPLING} = f_{DTS}/32$, N = 5 1110: $f_{SAMPLING} = f_{DTS}/32$, N = 6 1111: $f_{SAMPLING} = f_{DTS}/32$, N = 8
7	MSMD	Master/ Slave mode 0: No action 1: Events on the trigger input (TRGI) are delayed to allow a perfect synchronization between the current timer (via TRGO) and its slaves. This is useful when several timers are required to be synchronized to a single external event.

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Bit field	Name	Description
6:4	TSEL[2:0]	Trigger selection These 3 bits are used to select the trigger input of the synchronous counter. 000: Internal trigger 0 (ITR0) 100: TI1 edge detector (TI1F_ED) 001: Internal trigger 1 (ITR1) 101: Filtered timer input 1(TI1FP1) 010: Internal trigger 2 (ITR2) 110: Filtered timer input 2 (TI2FP2) 011: Internal trigger 3 (ITR3) 111: External triggered Input (ETRF) For more details on ITRx, see Table 11-3 below. *Note: These bits must be changed only when not in use (e. g. TIMx_SMCTRL.SMSEL=000) to avoid false edge detection at the transition.*
3	Reserved	Reserved, the reset value must be maintained
2:0	SMSEL[2:0]	Slave mode selection When an external signal is selected, the active edge of the trigger signal (TRGI) is linked to the selected external input polarity (see input control register and control register description) 000: Disable slave mode. If TIMx_CTRL1.CNTEN = 1, the prescaler is driven directly by the internal clock. 001: Encoder mode 1. According to the level of TI2FP2, the counter up-counting or down-counting on the edge of TI1FP1. 010: Encoder mode 2. According to the level of TI1FP1, the counter up-counting or down-counting on the edge of TI2FP2. 011: Encoder mode 3. According to the input level of another signal, the counter up-counting or down-counting on the edges of TI2FP1 and TI2FP2. 100: Reset mode. On the rising edge of the selected trigger input (TRGI), the counter is reinitialized and the shadow register is updated. 101: Gated mode. When the trigger input (TRGI) is high, the clock of the counter is enabled. Once the trigger input becomes low, the counter stops counting, but is not reset. In this mode, the start and stop of the counter are controlled. 110: Trigger mode. When a rising edge occurs on the trigger input (TRGI), the counter is started but not reset. In this mode, only the start of the counter is controlled. 111: External clock mode 1. The counter is clocked by the rising edge of the selected trigger input (TRGI). *Note: Do not use gated mode if TI1F_ED is selected as the trigger input (TIMx_SMCTRL.TSEL=100). This is because TI1F_ED outputs a pulse for each TI1F transition, whereas gated mode checks the level of the triggered input.*

Table 11-3 TIMx internal trigger connection

Slave timer	ITR0 (TSEL = 000)	ITR1 (TSEL = 001)	ITR2 (TSEL = 010)	ITR3 (TSEL = 011)
TIM1	TIM5	TIM2	TIM3	TIM4
TIM8	TIM1	TIM2	TIM4	TIM5

11.4.5 DMA/Interrupt Enable Registers (TIMx_DINTEN)

Offset address: 0x0C

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Reset value: 0x0000

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	TDEN	COMDEN	CC4DEN	CC3DEN	CC2DEN	CC1DEN	UDEN	BIEN	TIEN	COMIEN	CC4IEN	CC3IEN	CC2IEN	CC1IEN	UIEN
	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bit field	Name	Description
15	Reserved	Reserved, the reset value must be maintained
14	TDEN	Trigger DMA request enable 0: Disable trigger DMA request 1: Enable trigger DMA request
13	COMDEN	COM DMA request enable 0: Disable COM DMA request 1: Enable COM DMA request
12	CC4DEN	Capture/Compare 4 DMA request enable 0: Disable capture/compare 4 DMA request 1: Enable capture/compare 4 DMA request
11	CC3DEN	Capture/Compare 3 DMA request enable 0: Disable capture/compare 3 DMA request 1: Enable capture/compare 3 DMA request
10	CC2DEN	Capture/Compare 2 DMA request enable 0: Disable capture/compare 2 DMA request 1: Enable capture/compare 2 DMA request
9	CC1DEN	Capture/Compare 1 DMA request enable 0: Disable capture/compare 1 DMA request 1: Enable capture/compare 1 DMA request
8	UDEN	Update DMA request enable 0: Disable update DMA request 1: Enable update DMA request
7	BIEN	Break interrupt enable 0: Disable break interrupt 1: Enable break interrupt
6	TIEN	Trigger interrupt enable 0: Disable trigger interrupt 1: Enable trigger interrupt
5	COMIEN	COM interrupt enable 0: Disable COM interrupt 1: Enable COM interrupt
4	CC4IEN	Capture/Compare 4 interrupt enable 0: Disable capture/compare 4 interrupt 1: Enable capture/compare 4 interrupt
3	CC3IEN	Capture/Compare 3 interrupt enable 0: Disable capture/compare 3 interrupt 1: Enable capture/compare 3 interrupts

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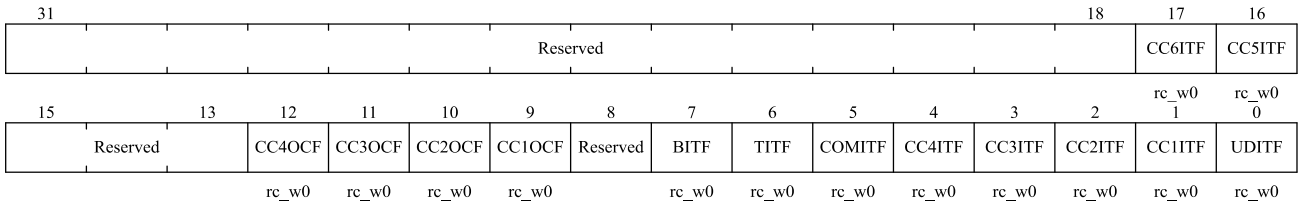
Bit field	Name	Description
2	CC2IEN	Capture/Compare 2 interrupt enable 0: Disable capture/compare 2 interrupt 1: Enables capture/compare 2 interrupts
1	CC1IEN	Capture/Compare 1 interrupt enable 0: Disable capture/compare 1 interrupt 1: Enables capture/comparing 1 interrupt
0	UIEN	Update interrupt enable 0: Disable update interrupt 1: Enables update interrupt

11.4.6 Status Registers (TIMx_STS)

Offset address: 0x10

Reset value: 0x0000 0000



Bit field	Name	Description
31：18	Reserved	Reserved, the reset value must be maintained
17	CC6ITF	Capture/Compare 6 interrupt flag See TIMx_STS.CC1ITF description.
16	CC5ITF	Capture/Compare 5 interrupt flag See TIMx_STS.CC1ITF description.
15：13	Reserved	Reserved, the reset value must be maintained
12	CC4OCF	Capture/Compare 4 overcapture flag See TIMx_STS.CC1OCF description.
11	CC3OCF	Capture/Compare 3 overcapture flag See TIMx_STS.CC1OCF description.
10	CC2OCF	Capture/Compare 2 overcapture flags See TIMx_STS.CC1OCF description.
9	CC1OCF	Capture/Compare 1 overcapture flag This bit is set by hardware only when the corresponding channel is configured in input capture mode. Cleared by software writing 0. 0: No overcapture occurred 1: TIMx_STS.CC1ITF was already set when the value of the counter has been captured in the TIMx_CCDAT1 register.
8	Reserved	Reserved, the reset value must be maintained

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Bit field	Name	Description
7	BITF	Break interrupt flag This bit is set by hardware once the brake input is active. This bit is cleared by software when the brake input becomes inactive. 0: No break event occurred 1: An active level has been detected
6	TITF	Trigger interrupt flag This bit is set by hardware when an active edge is detected on the TRGI input when the slave mode controller is in a mode other than gated. This bit is set by hardware when any edge in gated mode is detected. This bit is cleared by software. 0: No trigger event occurred 1: Trigger interrupt occurred
5	COMITF	COM interrupt flag This bit is set by hardware once a COM event is generated (when TIMx_CCEN.CCxEN, TIMx_CCEN.CCxNEN, TIMx_CCMOD1.OCxMD have been updated). This bit is cleared by software. 0: No COM event occurred 1: COM interrupt pending
4	CC4ITF	Capture/Compare 4 interrupt flag See TIMx_STS.CC1ITF description.
3	CC3ITF	Capture/Compare 3 interrupt flag See TIMx_STS.CC1ITF description.
2	CC2ITF	Capture/Compare 2 interrupt flag See TIMx_STS.CC1ITF description.
1	CC1ITF	Capture/Compare 1 interrupt flag **When the corresponding channel of CC1 is in output mode:** Except in center-aligned mode, this bit is set by hardware when the counter value is the same as the compare value (see TIMx_CTRL1.CAMSEL bit description). This bit is cleared by software. 0: No match occurred. 1: The value of TIMx_CNT is the same as the value of TIMx_CCDAT1. When the value of TIMx_CCDAT1 is greater than the value of TIMx_AR, the TIMx_STS.CC1ITF bit will go high if the counter overflows (in up-counting and up/down-counting modes) and underflows in down-counting mode. **When the corresponding channel of CC1 is in input mode:** This bit is set by hardware when the capture event occurs. This bit is cleared by software or by reading TIMx_CCDAT1. 0: No input capture occurred. 1: Input capture occurred. Counter value has captured in the TIMx_CCDAT1. An edge with the same polarity as selected has been detected on IC1.
0	UDITF	Update interrupt flag This bit is set by hardware when an update event occurs under the following conditions: – When TIMx_CTRL1.UPDIS = 0, and repeat counter value overflow or underflow (An update event is generated when the repeat counter equals 0).

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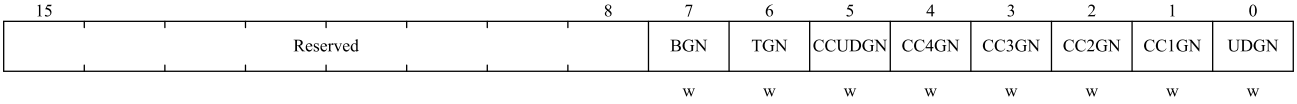
Bit field	Name	Description
		– When TIMx_CTRL1.UPRS = 0, TIMx_CTRL1.UPDIS = 0, and set the TIMx_EVTGEN.UDGN bit by software to reinitialize the CNT. – When TIMx_CTRL1.UPRS = 0, TIMx_CTRL1.UPDIS = 0, and the counter CNT is reinitialized by the trigger event. (See TIMx_SMCTRL Register description) This bit is cleared by software. 0: No update event occurred 1: Update interrupt occurred

11.4.7 Event Generation Registers (TIMx_EVTGEN)

Offset address: 0x14

Reset values: 0x0000



Bit field	Name	Description
15：8	Reserved	Reserved, the reset value must be maintained
7	BGN	Break generation This bit can generate a brake event when set by software. And at this time TIMx_BKDT.MOEN = 0, TIMx_STS.BITF = 1, if the corresponding interrupt and DMA are enabled, the corresponding interrupt and DMA will be generated. This bit is automatically cleared by hardware. 0: No action 1: Generated a break event
6	TGN	Trigger generation This bit can generate a trigger event when set by software. And at this time TIMx_STS.TITF = 1, if the corresponding interrupt and DMA are enabled, the corresponding interrupt and DMA will be generated. This bit is automatically cleared by hardware. 0: No action 1: Generated a trigger event
5	CCUDGN	Capture/Compare control update generation This bit is set by software. And if TIMx_CTRL2.CCPCTL = 1 at this time, the CCxEN, CCxNEN and OCxMD bits are allowed to be updated. This bit is automatically cleared by hardware. 0: No action 1: Generated a COM event *Note: This bit is only valid for channels with complementary outputs.*
4	CC4GN	Capture/Compare 4 generation See TIMx_EVTGEN.CC1GN description.
3	CC3GN	Capture/Compare 3 generation See TIMx_EVTGEN.CC1GN description.
2	CC2GN	Capture/Compare 2 generation See TIMx_EVTGEN.CC1GN description.

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Bit field	Name	Description
1	CC1GN	Capture/Compare 1 generation This bit can generate a capture/compare event when set by software. This bit is automatically cleared by hardware. When the corresponding channel of CC1 is in output mode: The TIMx_STS.CC1ITF flag will be pulled high, if the corresponding interrupt and DMA are enabled, the corresponding interrupt and DMA will be generated. When the corresponding channel of CC1 is in input mode: TIMx_CCDAT1 will capture the current counter value, and the TIMx_STS.CC1ITF flag will be pulled high, if the corresponding interrupt and DMA are enabled, the corresponding interrupt and DMA will be generated. If The TIMx_STS.CC1ITF is already pulled high, pull TIMx_STS.CC1OCF high. 0: No action 1: Generated a CC1 capture/compare event
0	UDGN	Update generation This bit can generate an update event when set by software. And at this time the counter will be reinitialized, the prescaler counter will be cleared, the counter will be cleared in center-aligned or up-counting mode, but take TIMx_AR in down-counting mode the value of the register. This bit is automatically cleared by hardware. 0: No action 1: Generated an update event

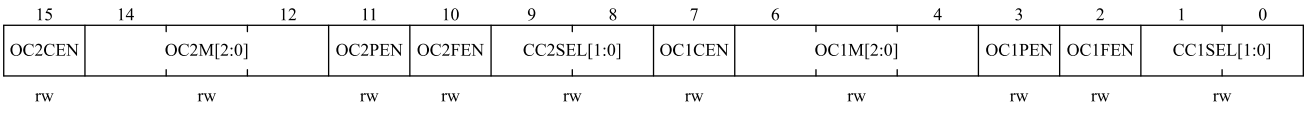
11.4.8 Capture/Compare Mode Register 1 (TIMx_CCMOD1)

Offset address: 0x18

Reset value: 0x0000

Channels can be used for input (capture mode) or output (compare mode), and the direction of the channel is defined by the corresponding CCxSEL bit. The other bits of the register act differently in input and output modes. OCx describes the function of a channel in output mode, ICx describes the function of a channel in input mode. Hence, please note that the same bit can have different meanings for output mode and for input mode.

Output compare mode:



Bit field	Name	Description
15	OC2CEN	Output Compare 2 clear enable
14:12	OC2MD[2:0]	Output Compare 2 mode
11	OC2PEN	Output Compare 2 preload enable
10	OC2FEN	Output Compare 2 fast enable

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Bit field	Name	Description
9:8	CC2SEL[1:0]	Capture/compare 2 selection These bits are used to select the input/output and input mapping of the channel 00: CC2 channel is configured as output 01: CC2 channel is configured as input, IC2 is mapped on TI2 10: CC2 channel is configured as input, IC2 is mapped on TI1 11: CC2 channel is configured as input, IC2 is mapped on TRC. This mode is only active when the internal trigger input is selected by TIMx_SMCTRL.TSEL. *Note: CC2SEL is writable only when the channel is off (TIMx_CCEN.CC2EN = 0).*
7	OC1CEN	Output Compare 1 clear enable 0: OC1REF is not affected by ETRF input level 1: OC1REF is cleared immediately when the ETRF input level is detected as high
6:4	OC1MD[2:0]	Output Compare 1 mode These bits are used to manage the output reference signal OC1REF, which determines the values of OC1 and OC1N, and is valid at high levels, while the active levels of OC1 and OC1N depend on the TIMx_CCEN.CC1P and TIMx_CCEN.CC1NP bits. 000: Frozen. Comparison between TIMx_CCDAT1 register and counter TIMx_CNT has no effect on OC1REF signal. 001: Set channel 1 to the active level on match. When TIMx_CCDAT1 = TIMx_CNT, OC1REF signal will be forced high. 010: Set channel 1 as inactive level on match. When TIMx_CCDAT1 = TIMx_CNT, OC1REF signal will be forced low. 011: Toggle. When TIMx_CCDAT1 = TIMx_CNT, OC1REF signal will be toggled. 100: Force to inactive level. OC1REF signal is forced low. 101: Force to active level. OC1REF signal is forced high. 110: PWM mode 1 - In up-counting mode, if TIMx_CNT < TIMx_CCDAT1, OC1REF signal of channel 1 is high, otherwise it is low. In down-counting mode, if TIMx_CNT > TIMx_CCDAT1, OC1REF signal of channel 1 is low, otherwise it is high. 111: PWM mode 2 - In up-counting mode, if TIMx_CNT < TIMx_CCDAT1, OC1REF signal of channel 1 is low, otherwise it is high. In down-counting mode, if TIMx_CNT > TIMx_CCDAT1, OC1REF signal of channel 1 is high, otherwise it is low. *Note 1: In PWM mode 1 or PWM mode 2, the OC1REF level changes only when the comparison result changes or when the output compare mode is switched from frozen mode to PWM mode.*
3	OC1PEN	Output Compare 1 preload enable 0: Disable preload function of TIMx_CCDAT1 register. Supports write operations to TIMx_CCDAT1 register at any time, and the written value is effective immediately. 1: Enable preload function of TIMx_CCDAT1 register. Only read and write operations to preload registers. When an update event occurs, the value of TIMx_CCDAT1 is loaded into the active register. *Note 1: Only when TIMx_CTRL1.ONEPM = 1(In one-pulse mode), PWM mode can be used without verifying the preload register, otherwise no other behavior can be predicted.*

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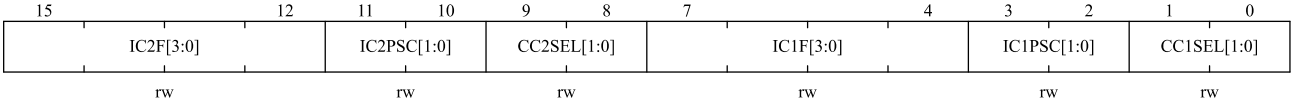
Bit field	Name	Description
2	OC1FEN	Output Compare 1 fast enable This bit is used to speed up the response of the CC output to the trigger input event. 0: CC1 behaves normally depending on the counter and CCDAT1 values, even if the trigger is ON. The minimum delay for activating CC1 output when an edge occurs on the trigger input is 5 clock cycles. 1: An active edge of the trigger input acts like a comparison match on CC1 output. Therefore, OC is set to the comparison level regardless of the comparison result. The delay time for sampling the trigger input and activating the CC1 output is reduced to 3 clock cycles. OCxFEN only works if the channel is configured in PWM1 or PWM2 mode.
1：0	CC1SEL[1:0]	Capture/compare 1 selection These bits are used to select the input/output and input mapping of the channel 00: CC1 channel is configured as output 01: CC1 channel is configured as input, IC1 is mapped on TI1 10: CC1 channel is configured as input, IC1 is mapped on TI2 11: CC1 channels are configured as inputs and IC1 is mapped to TRC. This mode is only active when the internal trigger input is selected by TIMx_SMCTRL.TSEL. *Note: CC1SEL is writable only when the channel is off (TIMx_CCEN.CC1EN = 0).*

Input capture mode:



Bit field	Name	Description
15:12	IC2F[3:0]	Input Capture 2 Filter
11:10	IC2PSC[1:0]	Input Capture 2 Prescaler
9:8	CC2SEL[1:0]	Capture/Compare 2 selection These bits are used to select the input/output and input mapping of the channel 00: CC2 channel is configured as output 01: CC2 channel is configured as input, IC2 is mapped on TI2 10: CC2 channel is configured as input, IC2 is mapped on TI1 11: CC2 channel is configured as input, IC2 is mapped on TRC. This mode is only active when the internal trigger input is selected by TIMx_SMCTRL.TSEL. *Note: CC2SEL is writable only when the channel is off (TIMx_CCEN.CC2EN = 0).*
7:4	IC1F[3:0]	Input Capture 1 filter These bits are used to define sampling frequency of TI1 input and the length of digital filter. The digital filter is an event counter that generates an output transition after N events are recorded. 0000: No filter, sampling at f_{DTS} frequency 0001: $f_{SAMPLING} = f_{CK\_INT}$, N = 2 0010: $f_{SAMPLING} = f_{CK\_INT}$, N = 4 0011: $f_{SAMPLING} = f_{CK\_INT}$, N = 8 0100: $f_{SAMPLING} = f_{DTS}/2$, N = 6

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Bit field	Name	Description
		0101: $f_{SAMPLING} = f_{DTS}/2$, N = 8 0110: $f_{SAMPLING} = f_{DTS}/4$, N = 6 0111: $f_{SAMPLING} = f_{DTS}/4$, N = 8 1000: $f_{SAMPLING} = f_{DTS}/8$, N = 6 1001: $f_{SAMPLING} = f_{DTS}/8$, N = 8 1010: $f_{SAMPLING} = f_{DTS}/16$, N = 5 1011: $f_{SAMPLING} = f_{DTS}/16$, N = 6 1100: $f_{SAMPLING} = f_{DTS}/16$, N = 8 1101: $f_{SAMPLING} = f_{DTS}/32$, N = 5 1110: $f_{SAMPLING} = f_{DTS}/32$, N = 6 1111: $f_{SAMPLING} = f_{DTS}/32$, N = 8
3:2	IC1PSC[1:0]	Input Capture 1 prescaler These bits are used to select the ratio of the prescaler for IC1 (CC1 input). When TIMx_CCEN.CC1EN = 0, the prescaler will be reset. 00: No prescaler, capture is done each time an edge is detected on the capture input 01: Capture is done once every 2 events 10: Capture is done once every 4 events 11: Capture is done once every 8 events
1:0	CC1SEL[1:0]	Capture/Compare 1 selection These bits are used to select the input/output and input mapping of the channel 00: CC1 channel is configured as output 01: CC1 channel is configured as input, IC1 is mapped on TI1 10: CC1 channel is configured as input, IC1 is mapped on TI2 11: CC1 channel is configured as input, IC1 is mapped to TRC. This mode is only active when the internal trigger input is selected by TIMx_SMCTRL.TSEL. *Note: CC1SEL is writable only when the channel is off (TIMx_CCEN.CC1EN = 0).*

11.4.9 Capture/Compare Mode Register 2 (TIMx_CCMOD2)

Offset address: 0x1C

Reset value: 0x0000

See the description of the CCMOD1 register above

Output comparison mode:

15	14:12	11	10	9:8	7	6:4	3	2	1:0
OC4CEN	OC4MD[2:0]	OC4PEN	OC4FEN	CC4SEL[1:0]	OC3CEN	OC3MD[2:0]	OC3PEN	OC3FEN	CC3SEL[1:0]
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bit field	Name	Description
15	OC4CEN	Output compare 4 clear enable
14:12	OC4MD[2:0]	Output compare 4 mode
11	OC4PEN	Output compare 4 preload enable
10	OC4FEN	Output compare 4 fast enable

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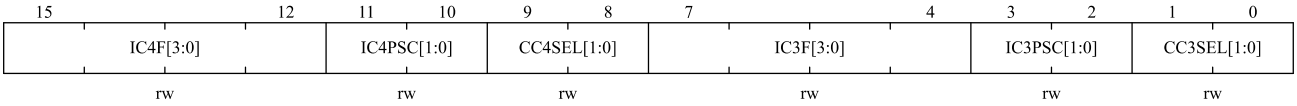
Bit field	Name	Description
9:8	CC4SEL[1:0]	Capture/Compare 4 selection These bits are used to select the input/output and input mapping of the channel 00: CC4 channel is configured as output 01: CC4 channel is configured as input, IC4 is mapped on TI4 10: CC4 channel is configured as input, IC4 is mapped on TI3 11: CC4 channel is configured as input, IC4 is mapped on TRC. This mode is only active when the internal trigger input is selected by TIMx_SMCTRL.TSEL. *Note: CC4SEL is writable only when the channel is off (TIMx_CCEN.CC4EN = 0).*
7	OC3CEN	Output compare 3 clear enable
6:4	OC3MD[2:0]	Output compare 3 mode
3	OC3PEN	Output compare 3 preload enable
2	OC3FEN	Output compare 3 fast enable
1:0	CC3SEL[1:0]	Capture/Compare 3 selection These bits are used to select the input/output and input mapping of the channel 00: CC3 channel is configured as output 01: CC3 channel is configured as input, IC3 is mapped to TI3 10: CC3 channel is configured as input, IC3 is mapped on TI4 11: CC3 channel is configured as input, IC3 is mapped to TRC. This mode is only active when the internal trigger input is selected by TIMx_SMCTRL.TSEL. *Note: CC3SEL is writable only when the channel is off (TIMx_CCEN.CC3EN = 0).*

Input capture mode:



Bit field	Name	Description
15:12	IC4F[3:0]	Input Capture 4 filter
11:10	IC4PSC[1:0]	Input Capture 4 Prescaler
9:8	CC4SEL[1:0]	Capture/Compare 4 selection These bits are used to select the input/output and input mapping of the channel 00: CC4 channel is configured as output 01: CC4 channel is configured as input, IC4 is mapped on TI4 10: CC4 channel is configured as input, IC4 is mapped on TI3 11: CC4 channel is configured as input, IC4 is mapped on TRC. This mode is only active when the internal trigger input is selected by TIMx_SMCTRL.TSEL. *Note: CC4SEL is writable only when the channel is off (TIMx_CCEN.CC4EN = 0).*
7:4	IC3F[3:0]	Input Capture 3 filter
3:2	IC3PSC[1:0]	Input Capture 3 Prescaler

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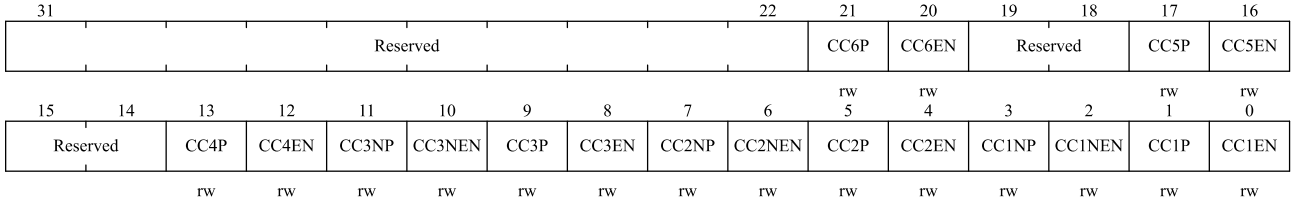
Bit field	Name	Description
1:0	CC3SEL[1:0]	Capture/compare 3 selection These bits are used to select the input/output and input mapping of the channel 00: CC3 channel is configured as output 01: CC3 channel is configured as input, IC3 is mapped to TI3 10: CC3 channel is configured as input, IC3 is mapped on TI4 11: CC3 channel is configured as input, IC3 is mapped to TRC. This mode is only active when the internal trigger input is selected by TIMx_SMCTRL.TSEL. *Note: CC3SEL is writable only when the channel is off (TIMx_CCEN.CC3EN = 0).*

11.4.10 Capture/Compare Enable Registers (TIMx_CCEN)

Offset address: 0x20

Reset value: 0x0000 0000



Bit field	Name	Description
31:22	Reserved	Reserved, the reset value must be maintained
21	CC6P	Capture/Compare 6 output polarity See TIMx_CCEN.CC1P description.
20	CC6EN	Capture/Compare 6 output enable See TIMx_CCEN.CC1EN description.
19：18	Reserved	Reserved, the reset value must be maintained
17	CC5P	Capture/Compare 5 output polarity See TIMx_CCEN.CC1P description.
16	CC5EN	Capture/Compare 5 output enable See TIMx_CCEN.CC1EN description.
15:14	Reserved	Reserved, the reset value must be maintained
13	CC4P	Capture/Compare 4 output polarity See TIMx_CCEN.CC1P description.
12	CC4EN	Capture/Compare 4 output enable See TIMx_CCEN.CC1EN description.
11	CC3NP	Capture/Compare 3 Complementary output polarity See TIMx_CCEN.CC1NP description.
10	CC3NEN	Capture/Compare 3 complementary output enable See TIMx_CCEN.CC1NEN description.
9	CC3P	Capture/Compare 3 output polarity

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Bit field	Name	Description
		See TIMx_CCEN.CC1P description.
8	CC3EN	Capture/Compare 3 output enable See TIMx_CCEN.CC1EN description.
7	CC2NP	Capture/Compare 2 complementary output polarity See TIMx_CCEN.CC1NP description.
6	CC2NEN	Capture/Compare 2 complementary output enable See TIMx_CCEN.CC1NEN description.
5	CC2P	Capture/Compare 2 output polarity See TIMx_CCEN.CC1P description.
4	CC2EN	Capture/Compare 2 output enable See TIMx_CCEN.CC1EN description.
3	CC1NP	Capture/Compare 1 complementary output polarity 0: OC1N active high 1: OC1N active low
2	CC1NEN	Capture/Compare 1 complementary output enable 0: Disable - Disable output OC1N signal. The level of OC1N depends on the value of these bits TIMx_BKDT.MOEN, TIMx_BKDT.OSSI, TIMx_BKDT.OSSR, TIMx_CTRL2.OI1, TIMx_CTRL2.OI1N and TIMx_CCEN.CC1EN. 1: Enable - Enable output OC1N signal. The level of OC1N depends on the value of these bits TIMx_BKDT.MOEN, TIMx_BKDT.OSSI, TIMx_BKDT.OSSR, TIMx_CTRL2.OI1, TIMx_CTRL2.OI1N and TIMx_CCEN.CC1EN.
1	CC1P	Capture/Compare 1 output polarity When the corresponding channel of CC1 is in output mode: 0: OC1 active high 1: OC1 active low When the corresponding channel of CC1 is in input mode: At this time, this bit is used to select whether IC1 or the inverse signal of IC1 is used as the trigger or capture signal. 0: non-inverted: Capture action occurs when IC1 generates a rising edge. When used as external trigger, IC1 is non-inverted. 1: inverted: Capture action occurs when IC1 generates a falling edge. When used as external trigger, IC1 is inverted.
0	CC1EN	Capture/Compare 1 output enable When the corresponding channel of CC1 is in output mode: 0: Disable - Disable output OC1 signal. The level of OC1 depends on the value of these bits TIMx_BKDT.MOEN, TIMx_BKDT.OSSI, TIMx_BKDT.OSSR, TIMx_CTRL2.OI1, TIMx_CTRL2.OI1N and TIMx_CCEN.CC1NEN. 1: Enable - Enable output OC1 signal. The level of OC1N depends on the value of these bits TIMx_BKDT.MOEN, TIMx_BKDT.OSSI, TIMx_BKDT.OSSR, TIMx_CTRL2.OI1, TIMx_CTRL2.OI1N and TIMx_CCEN.CC1NEN. When the corresponding channel of CC1 is in input mode: At this time, this bit is used to disable/enable the capture function.

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Bit field	Name	Description
		0: Disable capture 1: Enable capture

Table 11-4 Output control bits of complementary OCx and OCxN channels with break function

Control bits					Output state[1)]	
MOEN	OSSI	OSSR	CCxEN	CCxNEN	OCx Output state	OCxN Output state
1	X	0	0	0	Output disabled（not driven by timer） OCx=0，OCx_EN=0	Output disabled（not driven by timer） OCxN=0，OCxN_EN=0
		0	0	1	Output disabled（not driven by timer） OCx=0，OCx_EN=0	OCxREF + polarity， OCxN= OCxREF xor CCxNP，OCxN_EN=1
		0	1	0	OCxREF + polarity， OCx= OCxREF xor CCxP，OCx_EN=1	Output disabled（not driven by timer） OCxN=0，OCxN_EN=0
		0	1	1	OCxREF + polarity + dead-time， OCx_EN=1	Complementary to OCxREF + polarity + dead-time，OCxN_EN=1
		1	0	0	Output disabled（not driven by timer） OCx=CCxP，OCx_EN=0	Output disabled（not driven by timer） OCxN=CCxNP，OCxN_EN=0
		1	0	1	Off-state (Output enabled with inactive state) OCx=CCxP，OCx_EN=1	OCxREF + polarity， OCxN= OCxREF xor CCxNP，OCxN_EN=1
		1	1	0	OCxREF + polarity， OCx= OCxREF xor CCxP， OCx_EN=1	Off-state (Output enabled with inactive state) OCxN=CCxNP，OCxN_EN=1
		1	1	1	OCxREF + polarity + dead-time， OCx_EN=1	Complementary to OCxREF + polarity + dead-time， OCxN_EN=1
0	0	X	0	0	Output disabled（not driven by timer） Asynchronously： OCx=CCxP， OCx_EN=0， OCxN=CCxNP，OCxN_EN=0； Then if the clock is present：OCx=OIx and OCxN=OIxN after a dead-time, when (CCxP ^ OIx) ^ (CCxNP^OIxN)! = 0.	
	0		0	1		
	0		1	0		
	0		1	1		
	1		0	0	Off-state (Output enabled with inactive state) Asynchronously： OCx=CCxP， OCx_EN=1， OCxN=CCxNP，OCxN_EN=1； Then if the clock is present：OCx=OIx and OCxN=OIxN after a dead-time, when (CCxP ^ OIx) ^ (CCxNP^OIxN)! = 0	
	1		0	1		
	1		1	0		
	1		1	1		

1. If both outputs of a channel are not used (CCxEN = CCxNEN = 0), OIx, OIxN, CCxP and CCxNP must all be cleared.

Note: The status of external I/O pins connected to complementary OCx and OCxN channels depends on the OCx and OCxN channel states and GPIO and AFIO registers.

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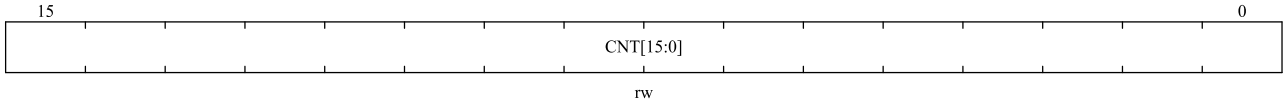
11.4.11 Counters (TIMx_CNT)

Offset address: 0x24

Reset value: 0x0000

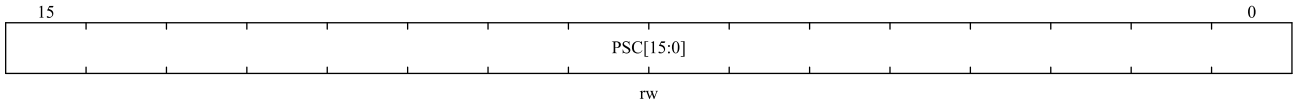


Bit field	Name	Description
15:0	CNT[15:0]	Counter value

11.4.12 Prescaler (TIMx_PSC)

Offset address: 0x28

Reset value: 0x0000

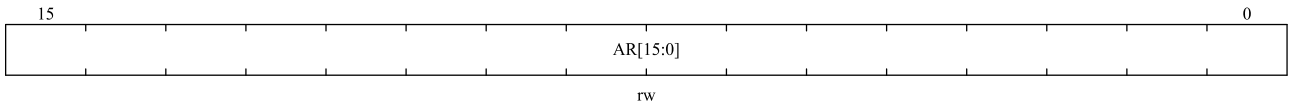


Bit field	Name	Description
15:0	PSC[15:0]	Prescaler value Counter clock $f_{CK\_CNT} = f_{CK\_PSC}/ (PSC [15:0] +1)$. Each time an update event occurs, the PSC value is loaded into the active prescaler register.

11.4.13 Auto-reload Register (TIMx_AR)

Offset address: 0x2C

Reset values: 0xFFFF



Bit field	Name	Description
15:0	AR[15:0]	Auto-reload value These bits define the value that will be loaded into the actual auto-reload register. See Section 11.3.1 for more details. When the TIMx_AR.AR [15:0] value is null, the counter does not work.

11.4.14 Repeat Count Registers (TIMx_REPCNT)

Offset address: 0x30

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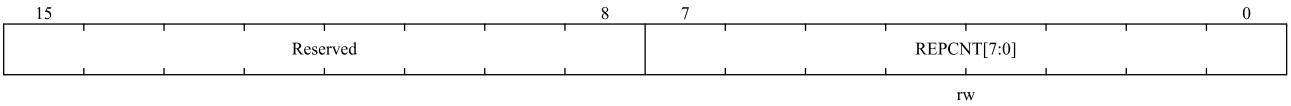
Reset value: 0x0000

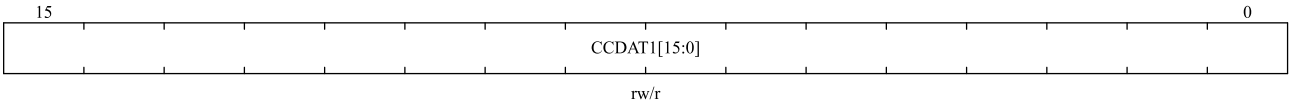


Bit field	Name	Description
15:8	Reserved	Reserved, the reset value must be maintained
7:0	REPCNT[7:0]	Repetition counter value Repetition counter is used to generate the update event or update the timer registers only after a given number (N+1) cycles of the counter, where N is the value of TIMx_REPCNT.REPCNT . The repetition counter is decremented at each counter overflow in up-counting mode, at each counter underflow in down-counting mode or at each counter overflow and at each counter underflow in center-aligned mode. Setting the TIMx_EVTGEN.UDGN bit will reload the content of TIMx_REPCNT.REPCNT and generate an update event.

11.4.15 Capture/Compare Register 1 (TIMx_CCDAT1)

Offset address: 0x34

Reset value: 0x0000



Bit field	Name	Description
15:0	CCDAT1[15:0]	Capture/Compare 1 value • CC1 channel is configured as output: CCDAT1 contains the value to be compared to the counter TIMx_CNT, signaling on the OC1 output. If the preload feature is not selected in TIMx_CCMOD1.OC1PEN bit, the written value is immediately transferred to the active register. Otherwise, this preloaded value is transferred to the active register only when an update event occurs. • CC1 channel is configured as input: CCDAT1 contains the counter value transferred by the last input capture 1 event (IC1). When configured as input mode, register CCDAT1 and CCDDAT1 are only readable. When configured as output mode, register CCDAT1 and CCDDAT1 are readable and writable.

11.4.16 Capture/Compare Register 2 (TIMx_CCDAT2)

Offset address: 0x38

Reset value: 0x0000

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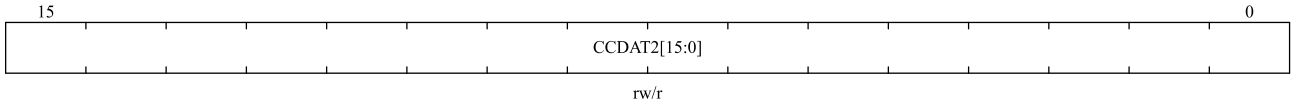
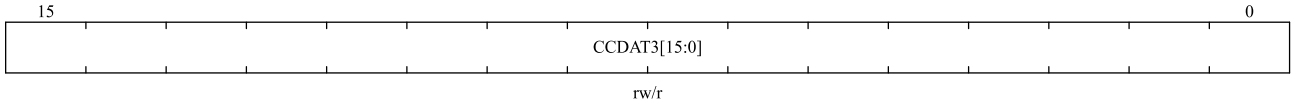


Bit field	Name	Description
15:0	CCDAT2[15:0]	Capture/Compare 2 values • CC2 channel is configured as output: CCDAT2 contains the value to be compared to the counter TIMx_CNT, signaling on the OC2 output. If the preload feature is not selected in TIMx_CCMOD1.OC2PEN bit, the written value is immediately transferred to the active register. Otherwise, this preloaded value is transferred to the active register only when an update event occurs. • CC2 channel is configured as input: CCDAT2 contains the counter value transferred by the last input capture 2 event (IC2). When configured as input mode, register CCDAT2 and CCDDAT2 are only readable. When configured as output mode, register CCDAT2 and CCDDAT2 are readable and writable.

11.4.17 Capture/Compare Register 3 (TIMx_CCDAT3)

Offset address: 0x3C

Reset value: 0x0000



Bit field	Name	Description
15:0	CCDAT3[15:0]	Capture/Compare 3 value • CC3 channel is configured as output: CCDAT3 contains the value to be compared to the counter TIMx_CNT, signaling on the OC3 output. If the preload feature is not selected in TIMx_CCMOD2.OC3PEN bit, the written value is immediately transferred to the active register. Otherwise, this preloaded value is transferred to the active register only when an update event occurs. • CC3 channel is configured as input: CCDAT3 contains the counter value transferred by the last input capture 3 event (IC3). When configured as input mode, register CCDAT3 and CCDDAT3 are only readable. When configured as output mode, register CCDAT3 and CCDDAT3 are readable and writable.

11.4.18 Capture/Compare Register 4 (TIMx_CCDAT4)

Offset address: 0x40

Reset value: 0x0000

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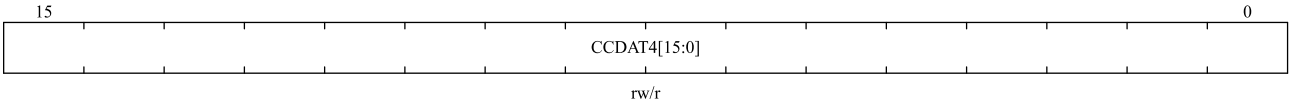
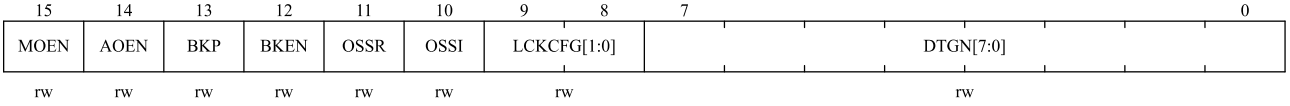


Bit field	Name	Description
15:0	CCDAT4[15:0]	Capture/Compare 4 value • CC4 channel is configured as output: CCDAT4 contains the value to be compared to the counter TIMx_CNT, signaling on the OC4 output. If the preload feature is not selected in TIMx_CCMOD2.OC4PEN bit, the written value is immediately transferred to the active register. Otherwise, this preloaded value is transferred to the active register only when an update event occurs. • CC4 channel is configured as input: CCDAT4 contains the counter value transferred by the last input capture 4 event (IC4). When configured as input mode, register CCDAT4 and CCDDAT4 are only readable. When configured as output mode, register CCDAT4 and CCDDAT4 are readable and writable.

11.4.19 Break and Dead-time Registers (TIMx_BKDT)

Offset address: 0x44

Reset value: 0x0000



Note: AOEN, BKP, BKEN, OSSI, OSSR, and DTGN [7:0] bits can all be write protected depending on the LOCK configuration, and it is necessary to configure all of them on the first write to the TIMx_BKDT register.

Bit field	Name	Description
15	MOEN	Main Output enable This bit can be set by software or hardware depending on the TIMx_BKDT.AOEN bit, and is asynchronously cleared to '0' by hardware once the brake input is active. It is only valid for channels configured as outputs. 0: OC and OCN outputs are disabled or forced to idle state. 1: OC and OCN outputs are enabled if TIMx_CCEN.CCxEN or TIMx_CCEN.CCxNEN bits are set. For more details, see Section 11.4.10 Capture/Compare enable registers (TIMx_CCEN).
14	AOEN	Automatic output enable 0: Only software can set TIMx_BKDT.MOEN; 1: Software sets TIMx_BKDT.MOEN; or if the break input is not active, when the next update event occurs, hardware automatically sets TIMx_BKDT.MOEN.
13	BKP	Break input polarity 0: Low level of the brake input is valid 1: High level of the brake input is valid

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Bit field	Name	Description
		Note: Any write to this bit requires an APB clock delay to take effect.
12	BKEN	Break enable 0: Disable brake input (BRK and CCS clock failure events) 1: Enable brake input (BRK and CCS clock failure events) *Note: Any write to this bit requires an APB clock delay to take effect.*
11	OSSR	Off-state Selection for Run Mode This bit is used when TIMx_BKDT.MOEN=1 and the channel is a complementary output. The OSSR bit does not exist in timer without complementary outputs. 0: When inactive, OCx/OCxN outputs are disabled (OCx/OCxN enable output signal=0). 1: When inactive, OCx/OCxN outputs are enabled with their inactive level as soon as CCxEN=1 or CCxNEN=1. Then, OCx/OCxN enable output signal=1 For more details, See Section 11.4.10, capture/compare enablement registers (TIMx_CCEN).
10	OSSI	Off-state Selection for Idle Mode This bit is used when TIMx_BKDT.MOEN=0 and the channels configured as outputs. 0: When inactive, OCx/OCxN outputs are disabled (OCx/OCxN enable output signal=0). 1: When inactive, OCx/OCxN outputs are enabled with their idle level as soon as CCxEN=1 or CCxNEN=1. Then, OCx/OCxN enable output signal=1 For more details, See Section 11.4.10, capture/compare enablement registers (TIMx_CCEN).
9:8	LCKCFG[1:0]	Lock Configuration These bits offer a write protection against software errors. 00: – No write protected. 01: – LOCK Level 1 TIMx_BKDT.DTGN, TIMx_BKDT.BKEN, TIMx_BKDT.BKP, TIMx_BKDT.AOEN, TIMx_CTRL2.OIx, TIMx_CTRL2.OIxN bits enable write protection. 10: – LOCK Level 2 Except for register write protection in LOCK Level 1 mode, TIMx_CCEN.CCxP and TIMx_CCEN.CCxNP (If the corresponding channel is configured in output mode), TIMx_BKDT.OSSR and TIMx_BKDT.OSSI bits also enable write protection. 11: – LOCK Level 3 Except for register write protection in LOCK Level 2, TIMx_CCMODx.OCxMD and TIMx_CCMODx.OCxPEN bits (If the corresponding channel is configured in output mode) also enable write protection. *Note: After the system reset, the LCKCFG bit can only be written once. Once written to the TIMx_BKDT register, LCKCFG will be protected until the next reset.*

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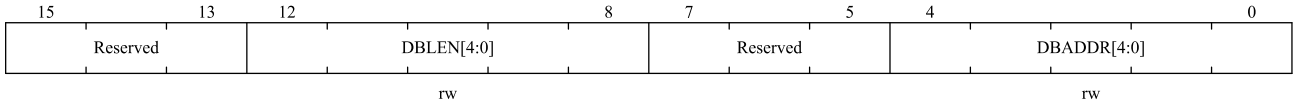
Bit field	Name	Description
7:0	DTGN [7:0]	Dead-time Generator These bits define the dead-time duration between inserted complementary outputs. The relationship between the DTGN value and the dead time is as follows: DTGN[7:5] = 0xx: dead time = DTGN[7:0] × (t_{DTS}) DTGN[7:5] = 10x: dead time =(64+DTGN[5:0]) × (2 × t_{DTS}) DTGN[7:5]=110: dead time =(32+DTGN[4:0]) × (8 × t_{DTS}) DTGN [then] = 111: dead time = (32 + DTGN [4:0]) × (16 × t_{DTS}) t_{DTS} value see TIMx_CTRL1.CLKD [1:0].

11.4.20 DMA Control Register (TIMx_DCTRL)

Offset address: 0x48

Reset value: 0x0000



Bit field	Name	Description
15:9	Reserved	Reserved, the reset value must be maintained, kept at 0.
12:8	DBLEN[4:0]	DMA Burst Length This bit field defines the number DMA will accesses (write/read) TIMx_DADDR register. 00000:1 time transfer 00001: 2 times transfers 00010: 3 times transfers … 10001: 18 times transfers
7:5	Reserved	Reserved, the reset value must be maintained.
4:0	DBADDR[4:0]	DMA Base Address This bit field defines the first address where the DMA accesses the TIMx_DADDR register. When access is done through the TIMx_DADDR first time, this bit-field specifies the address you just access. And then the second access to the TIMx_DADDR, you will access the address of "DMA Base Address + 4" 00000: TIMx_CTRL1, 00001: TIMx_CTRL2, 00010: TIMx_SMCTRL, … 10001: TIMx_BKDT

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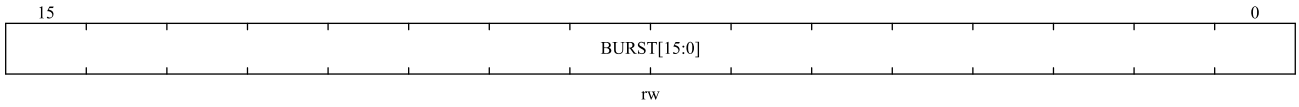
Bit field	Name	Description
		10010：TIMx_DCTRL

11.4.21 DMA Transfer Buffer Register (TIMx_DADDR)

Offset address: 0x4C

Reset value: 0x0000



Bit field	Name	Description
15:0	BURST[15:0]	DMA access buffer. When a read or write operation is assigned to this register, the register located at the address range (DMA base address + DMA burst length × 4) will be accessed. DMA base address = The address of TIM_CTRL1 + TIMx_DCTRL. DBADDR * 4； DMA burst len = TIMx_DCTRL.DBLEN + 1. Example: If TIMx_DCTRL.DBLEN = 0x3(4 transfers), TIMx_DCTRL.DBADDR = 0xD (TIMx_CCDAT1), DMA data length = half word, DMA memory address = buffer address in SRAM, DMA peripheral address = TIMx_DADDR address. When an event occurs, TIMx will send requests to the DMA, and transfer data 4 times. For the first time, DMA access to the TIMx_ DADDR register will be mapped to access TIMx_CCDAT1 register; For the second time, DMA access to the TIMx_ DADDR register will be mapped to access TIMx_CCDAT2 register; … … For the fourth time, DMA access to the TIMx_ DADDR register will be mapped to access TIMx_CCDAT4 register;

11.4.22 Capture/Compare Mode Registers 3(TIMx_CCMOD3)

Offset address: 0x54

Reset value: 0x0000

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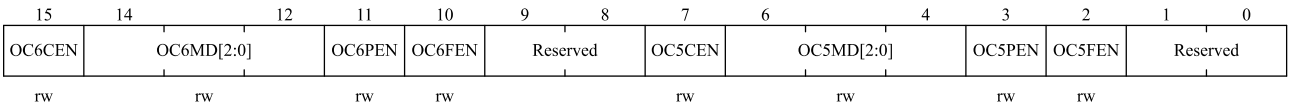
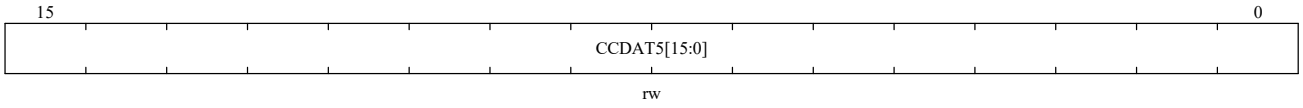


Bit field	Name	Description
15	OC6CEN	Output compare 6 clear enable
14:12	OC6MD[2:0]	Output compare 6 mode
11	OC6PEN	Output compare 6 preload enable
10	OC6FEN	Output compare 6 fast enable
9:8	Reserved	Reserved, the reset value must be maintained
7	OC5CEN	Output compare 5 clear enable
6:4	OC5MD[2:0]	Output compare 5 mode
3	OC5PEN	Output compare 5 Preload enable
2	OC5FEN	Output compare 5 fast enable
1：0	Reserved	Reserved, the reset value must be maintained

11.4.23 Capture/Compare Register 5 (TIMx_CCDAT5)

Offset address: 0x58

Reset value: 0x0000

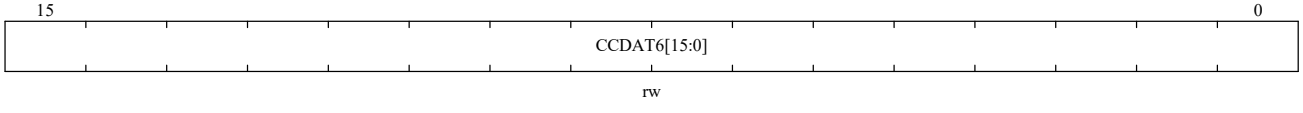


Bit field	Name	Description
15:0	CCDAT5[15:0]	Capture/Compare 5 value • CC5 channel can only configured as output: CCDAT5 contains the value to be compared to the counter TIMx_CNT, signaling on the OC5 output. If the preload feature is not selected in TIMx_CCMOD3.OC5PEN bit, the written value is immediately transferred to the active register. Otherwise, this preloaded value is transferred to the active register only when an update event occurs. TIM1_CC5 and TIM8_CC5 is used for comparator blanking.

11.4.24 Capture/Compare Register 6 (TIMx_CCDAT6)

Offset address: 0x5C

Reset value: 0x0000



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Bit field	Name	Description
15:0	CCDAT6[15:0]	Capture/Compare 6 value • CC6 channel can only configured as output: CCDAT6 contains the value to be compared to the counter TIMx_CNT, signaling on the OC6 output. If the preload feature is not selected in TIMx_CCMOD3.OC6PEN bit, the written value is immediately transferred to the active register. Otherwise, this preloaded value is transferred to the active register only when an update event occurs. TIM1_CC6 is used to switch the input channel of OPAMP1 and OPAMP2; TIM8_CC6 is used to switch the input channel of OPAMP3 and OPAMP4

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12 General-purpose Timers (TIM2, TIM3, TIM4 and TIM5)

12.1 General-purpose Timers Introduction

The general-purpose timers (TIM2, TIM3, TIM4 and TIM5) is mainly used in the following occasions: counting the input signal, measuring the pulse width of the input signal and generating the output waveform, etc.

12.2 Main Features of General-purpose Timers

- 16-bit auto-reload counters. (It can realize up-counting, down-counting, up/down counting)
- 16-bit programmable prescaler. (The frequency division factor can be configured with any value between 1 and 65536)
- TIM2, TIM3, TIM4 and TIM5 up to 4 channels.
- Channel's working modes: PWM output, ouput compare, one-pulse mode output, input capture.
- The events that generate the interrupt/DMA are as follows:
  - Update event
  - Trigger event
  - Input capture
  - Output compare
- Timer can be controlled by external signal
- Timers can be linked together internally for timer synchronization or chaining
- Incremental (quadrature) encoder interface: used for tracking motion and resolving rotation direction and position;
- Hall sensor interface: used to do three-phase motor control;
- Supports capture of internal comparator output signal.

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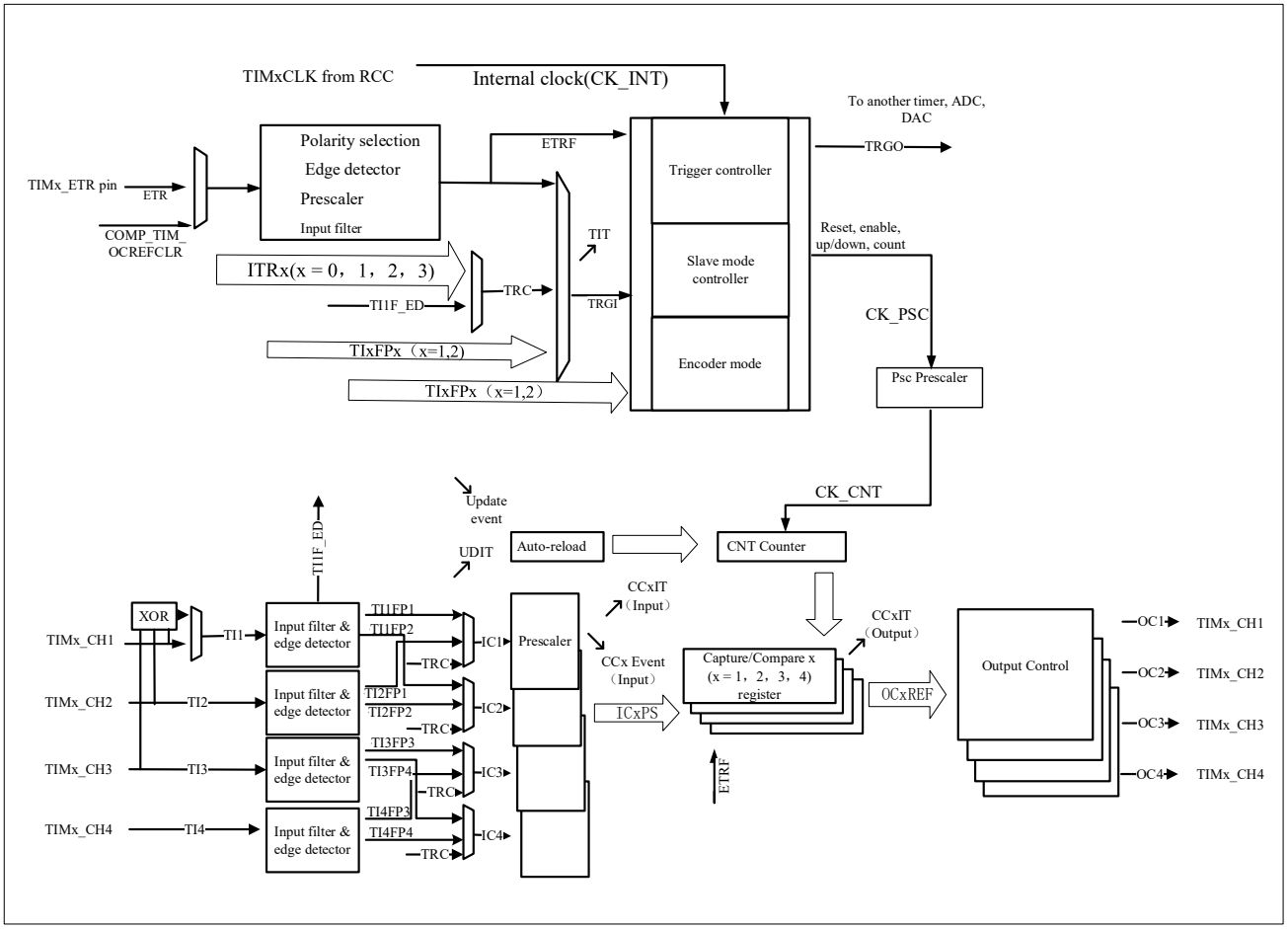
Figure 12-1 Block diagram of TIMx（x=2, 3 ,4 and 5）



The event *Interrupt and DMA output*

The capture channel 1/2/3/4 input can come from IOM or comparator output , except CH4 of TIM5 (Only from IOM)

For the mapping of ETR input to IOM, see 7.2.5.7

12.3 General-purpose Timers Description

12.3.1 Time-base Unit

The time-base unit mainly includes: prescaler, counter and auto-reload. When the time base unit is working, the software can read and write the corresponding registers (TIMx_PSC, TIMx_CNT and TIMx_AR) at any time.

Depending on the setting of the auto-reload preload enable bit (TIMx_CTRL1.ARPEN), the value of the preload register is transferred to the shadow register immediately or at each update event UEV. An update event is generated when the counter reaches the overflow/underflow condition and it can be generated by software when TIMx_CTRL1.UPDIS=0. The counter CK_CNT is valid only when the TIMx_CTRL1.CNTEN bit is set. The counter starts counting one clock cycle after the TIMx_CTRL1.CNTEN bit is set.

12.3.1.1 Prescaler description

The TIMx_PSC register consists of a 16-bit counter that can be used to divide the counter clock frequency by any

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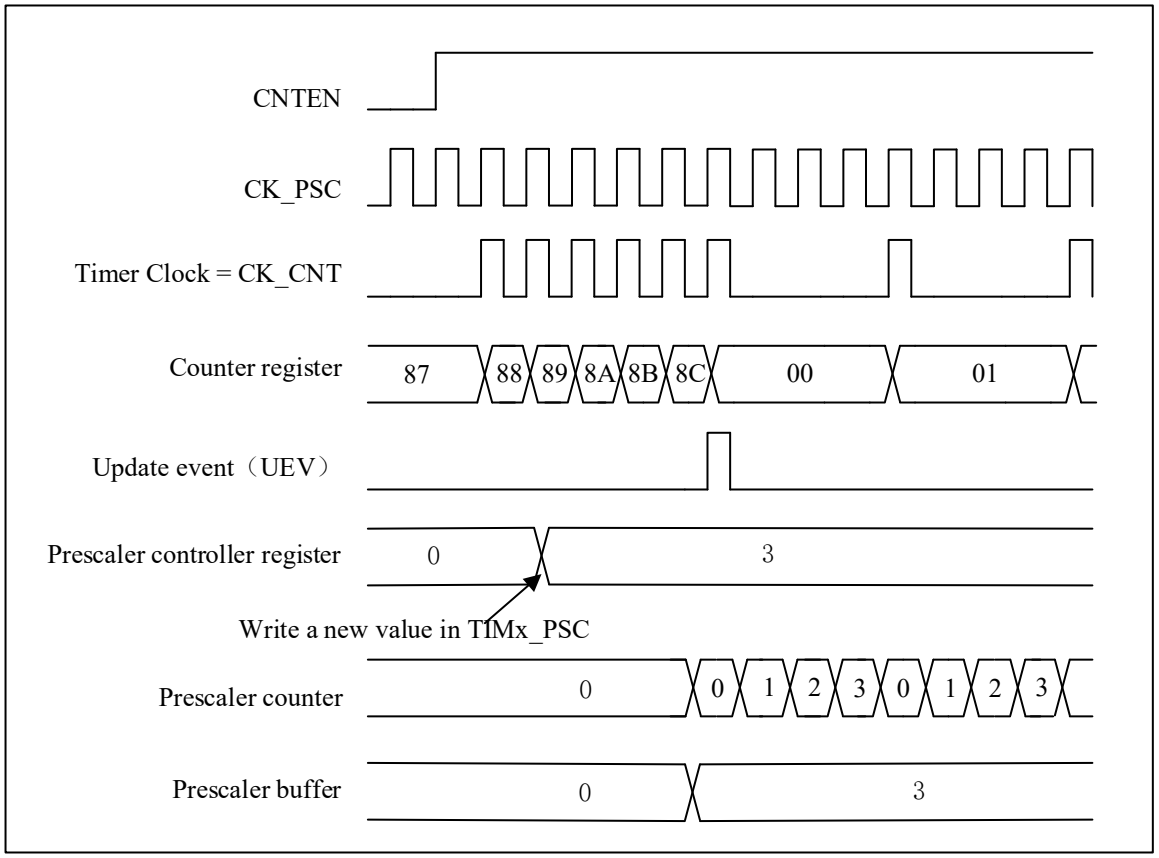
factor between 1 and 65536. It can be changed on the fly as it is buffered. The prescaler value is only taken into account at the next update event.

Figure 12-2 Counter timing diagram with prescaler division change from 1 to 4



12.3.2 Counter Mode

12.3.2.1 Up-counting mode

In up-counting mode, the counter will count from 0 to the value of the register TIMx_AR, then it resets to 0. And a counter overflow event is generated.

If the TIMx_CTRL1.UPRS bit (select update request) and the TIMx_EVTGEN.UDGN bit are set, an update event (UEV) will generate And TIMx_STS.UDITF will not be set by hardware, therefore, no update interrupts or update DMA requests are generated. This setting is used in scenarios where you want to clear the counter but do not want to generate an update interrupt.

Depending on the update request source is configured in the TIMx_CTRL1.UPRS. When an update event occurs, TIMx_STS.UDITF is set, all registers are updated:

• Update auto-reload shadow registers with preload value(TIMx_AR), when TIMx_CTRL1.ARPEN = 1.

• The prescaler shadow register is reloaded with the preload value(TIMx_PSC).

To avoid updating the shadow registers when new values are written to the preload registers, you can disable the update by setting TIMx_CTRL1.UPDIS=1.

When an update event occurs, the counter will still be cleared and the prescaler counter will also be set to 0 (but the

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prescaler value will remain unchanged).

The figure below shows some examples of the counter behavior and the update flags for different division factors in the up-counting mode.

Figure 12-3 Timing diagram of up-counting. The internal clock divider factor = 2/N

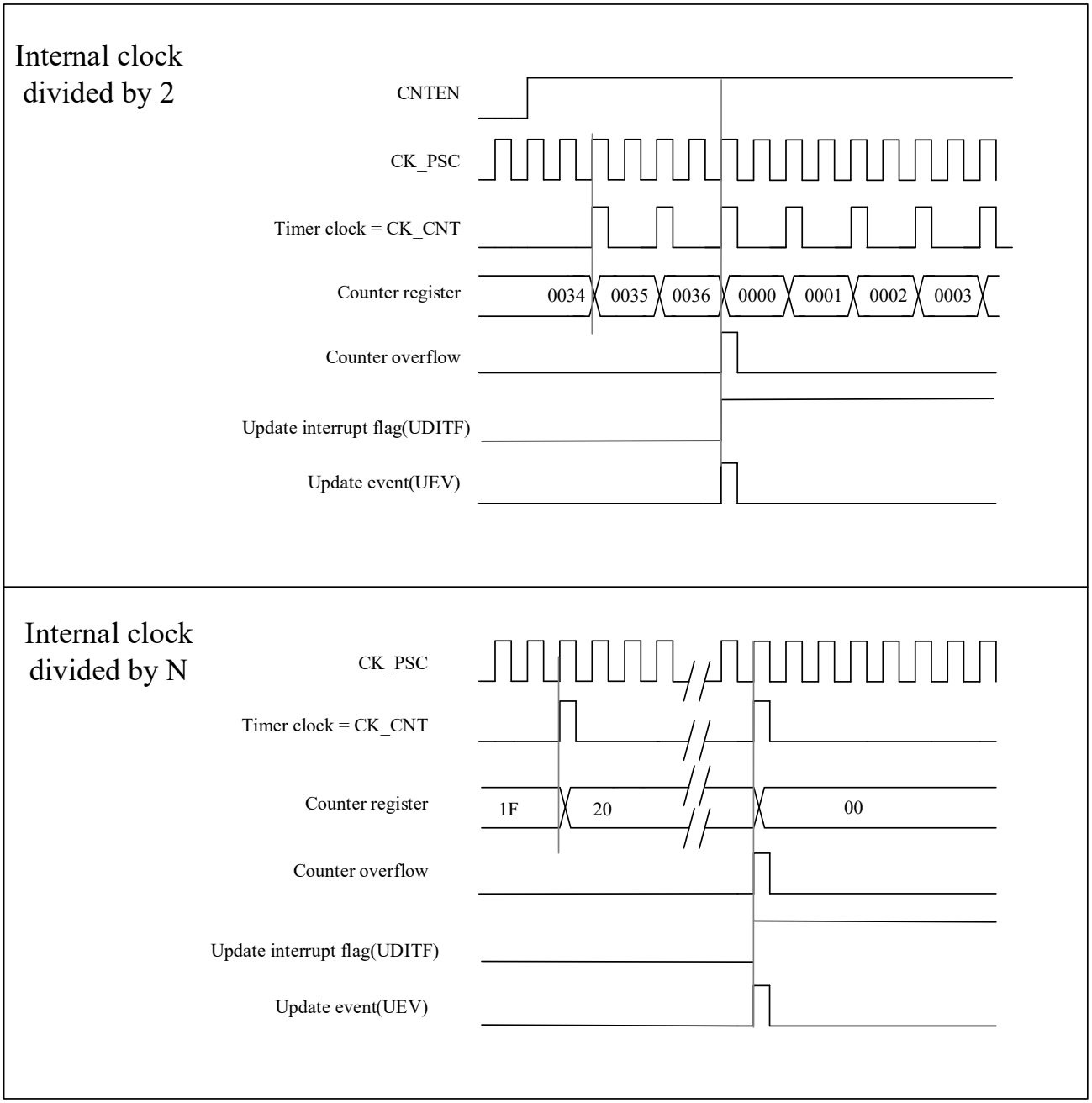

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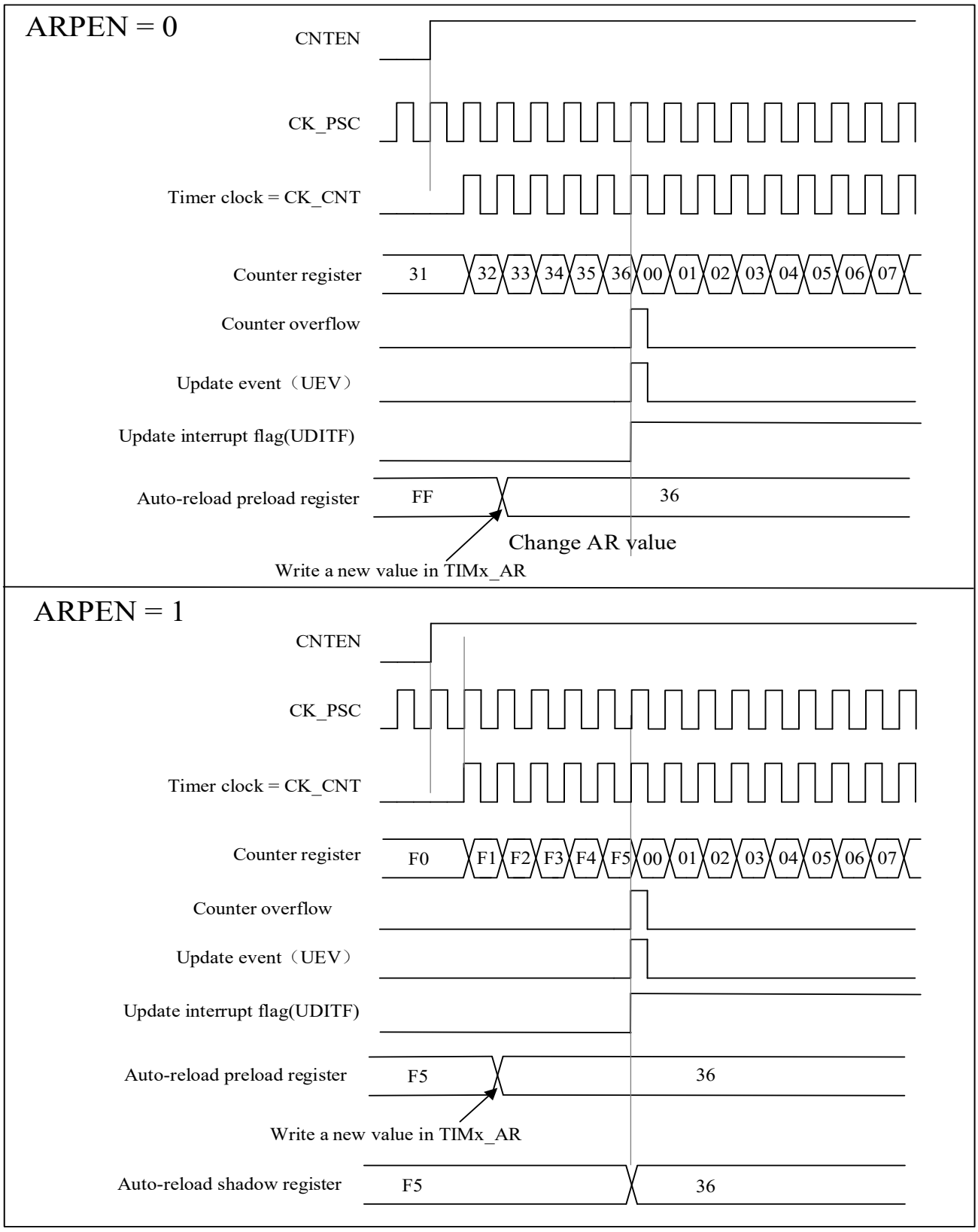
Figure 12-4 Timing diagram of the up-counting, update event when ARPEN=0/1



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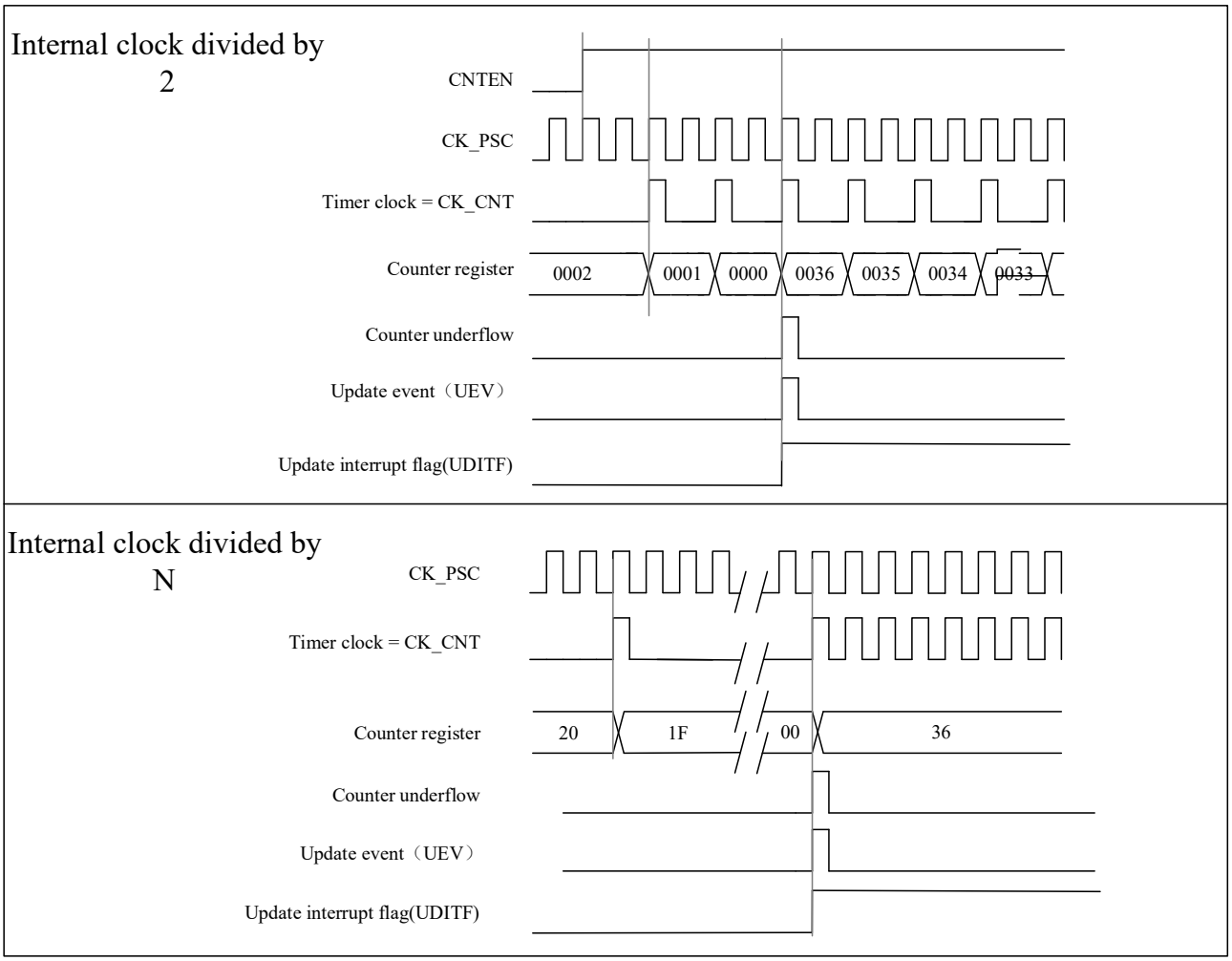
12.3.2.2 Down-counting mode

In down-counting mode, the counter will decrement from the value of the register TIMx_AR to 0, then restart from the auto-reload value and generate a counter underflow event.

The process of configuring update events and updating registers in down-counting mode is the same as in up-counting mode, see 12.3.2.1.

The figure below shows some examples of the counter behavior and the update flags for different division factors in the down-counting mode.

Figure 12-5 Timing diagram of the down-counting, internal clock divided factor = 2/N



12.3.2.3 Center-aligned mode

In center-aligned mode, the counter increments from 0 to the value (TIMx_AR) – 1, a counter overflow event is generated. It then counts down from the auto-reload value (TIMx_AR) to 1 and generates a counter underflow event. Then the counter resets to 0 and starts counting up again.

In this mode, the TIMx_CTRL1.DIR direction bits have no effect and the count direction is updated and specified by hardware. Center-aligned mode is valid when the TIMx_CTRL1. CAMSEL bit is not equal to "00".

The update events can be generated each time the counter overflows and each time the counter underflows. Alternatively, an update event can also be generated by setting the TIMx_EVTGEN. UDGN bit (either by software

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or using a slave mode controller). In this case, the counter restarts from 0, as does the prescaler's counter.

Please note: if the update source is a counter overflow, auto-reload update before reloading the counter.

Figure 12-6 Timing diagram of the Center-aligned, internal clock divided factor =2/N

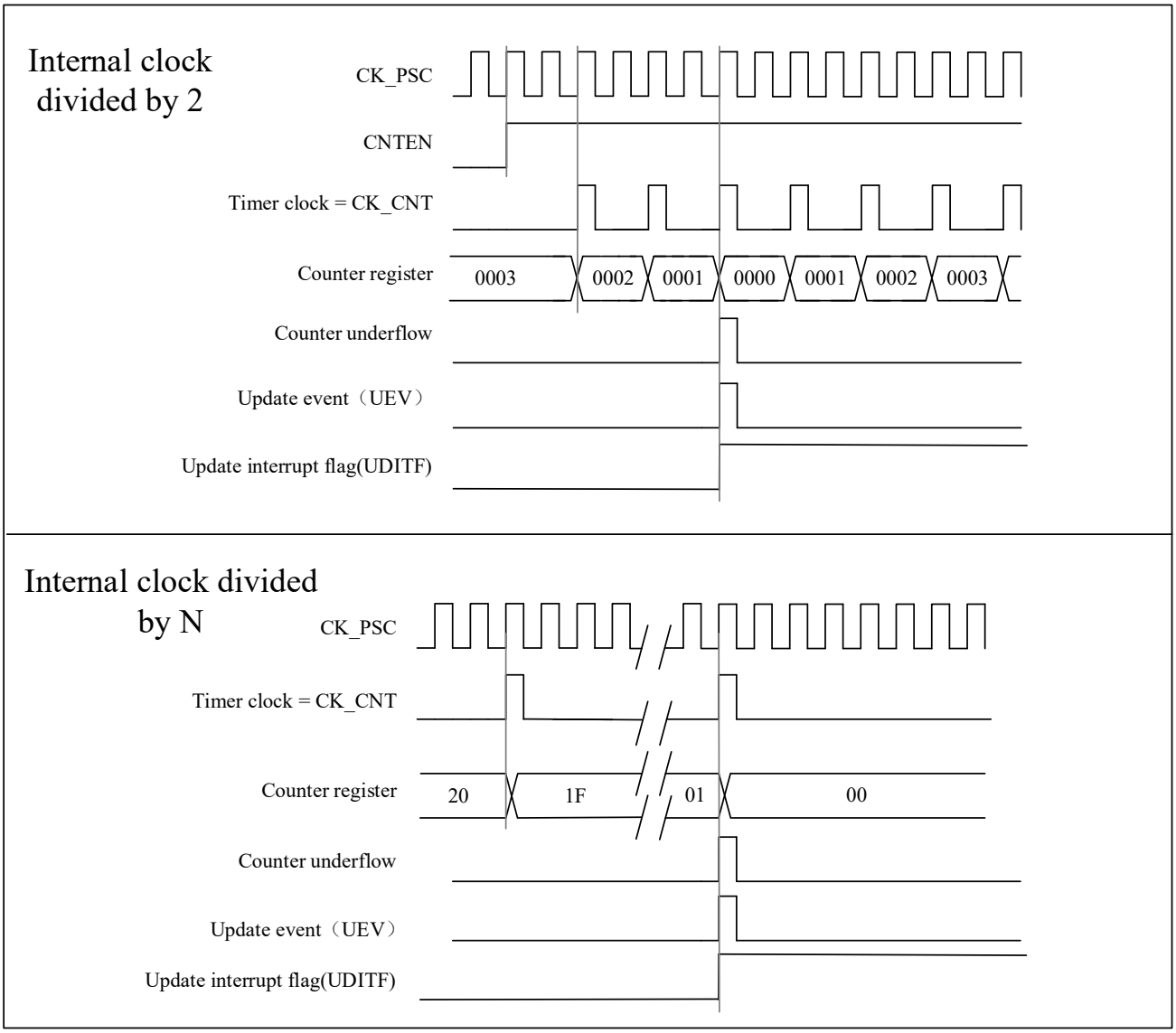

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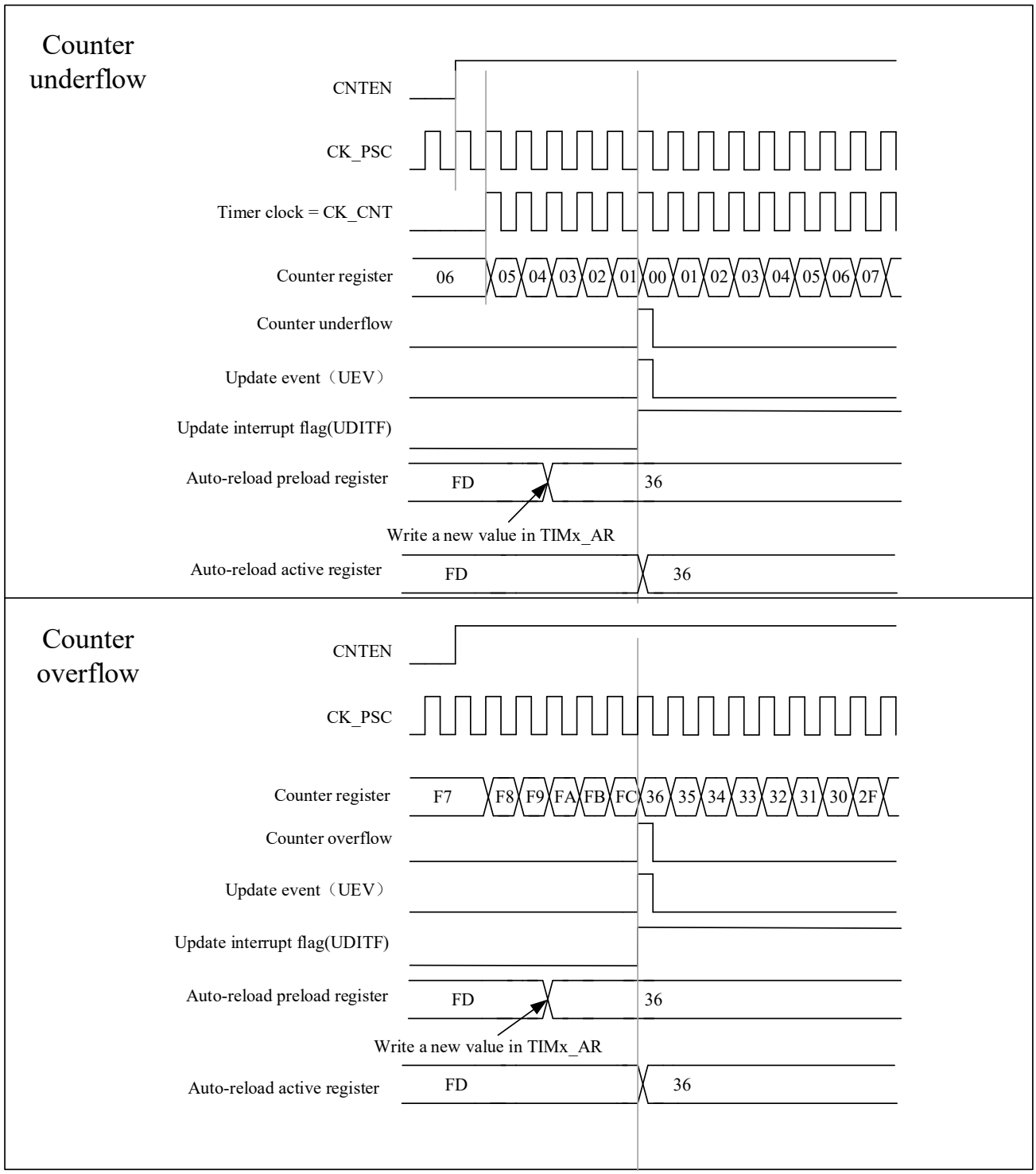
Figure 12-7 A center-aligned sequence diagram that includes counter overflows and underflows (ARPEN = 1)



12.3.3 Clock Selection

- The internal clock of timers ： CK_INT
- Two kinds of external clock mode :
  - external input pin

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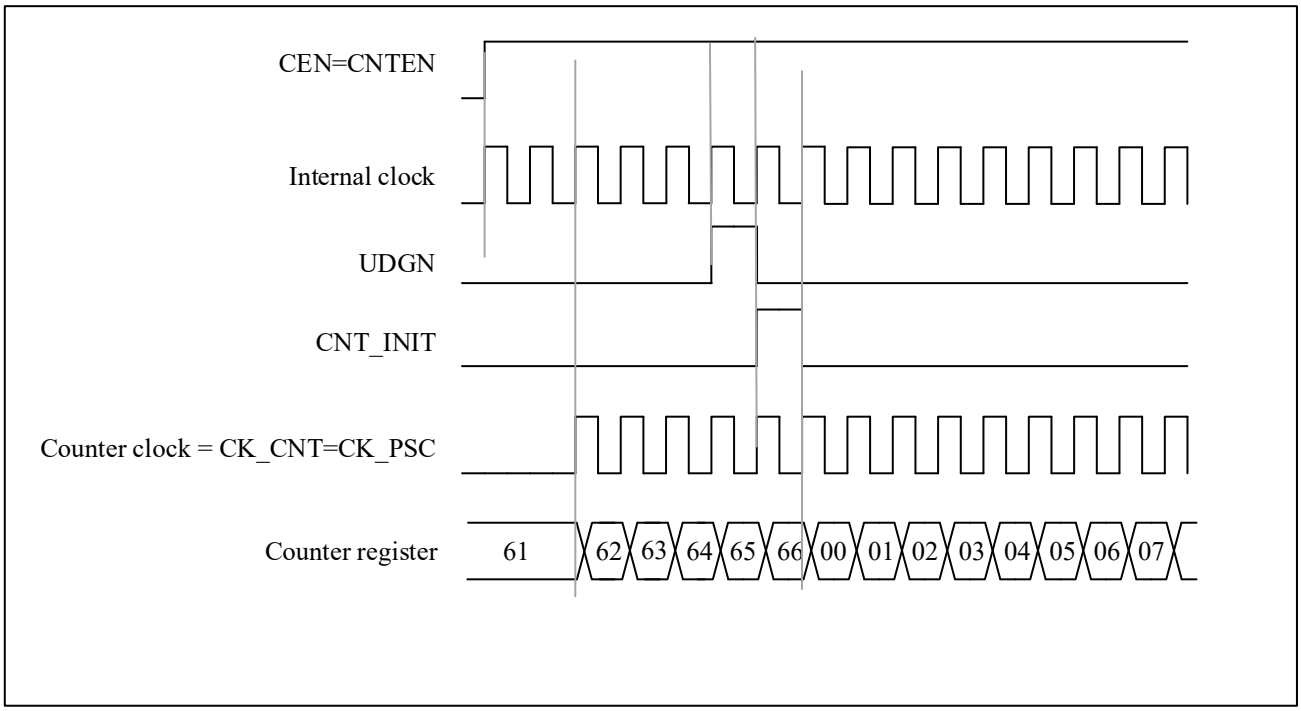
– external trigger input ETR

- Internal trigger input (ITRx): one timer is used as a prescaler for another timer.

12.3.3.1 Internal clock source (CK_INT)

When the TIMx_SMCTRL.SMSEL is equal to “000”, the slave mode controller is disabled. The three control bits (TIMx_CTRL1.CNTEN、TIMx_CTRL1. DIR、TIMx_EVTGEN. UDGN) can only be changed by software (except TIMx_EVTGEN. UDGN, which remains cleared automatically). It is provided that the TIMx_CTRL1.CNTEN bit is written as' 1 ' by soft, the clock source of the prescaler is provided by the internal clock CK_INT.

Figure 12-8 Control circuit in normal mode, internal clock divided by 1



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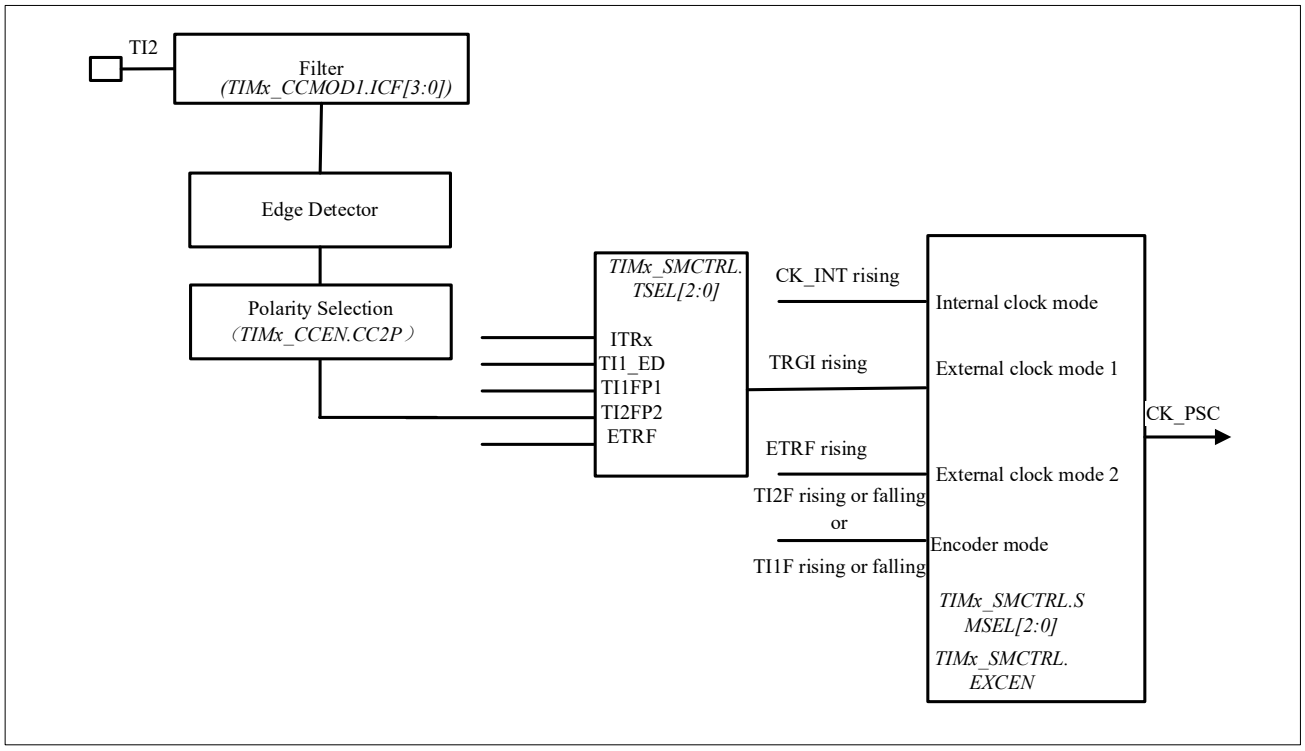
12.3.3.2 External clock source mode 1

Figure 12-9 TI2 external clock connection example



This mode is selected by configuring TIMx_SMCTRL.SMSEL=111. The counter can be configured to count on the rising or falling edge of the clock at the selected input.

For example, to configure up-counting mode to count on the rising edge of the clock at the T12 input, the configuration steps are as follows:

- Configure TIMx_CCMOD1.CC2SEL equal to '01', CC2 channel is configured as input, IC2 is mapped to TI2
- Configure TIMx_CCEN.CC2P equal to '0', select clock rising edge polarity
- To select input filter bandwidth by configuring TIMx_CCMOD1.IC2F[3:0] (if filter is not needed, keep IC2F bit at '0000')
- Configure TIMx_SMCTRL.SMSEL equal to '111', select timer external clock mode 1
- Configure TIMx_SMCTRL.TSEL equal to '110', select TI2 as the trigger input source
- Configure TIMx_CTRL1.CNTEN equal to '1' to start the counter

Note: The capture prescaler is not used for triggering, so it does not need to be configured

When the rising edge of the timer clock occurs at TI2=1, the counter counts once and the TIMx_STS .TITF flag is pulled high.

The delay between the rising edge of TI2 and the actual clock of the counter depends on the resynchronization circuit at the input of TI2.

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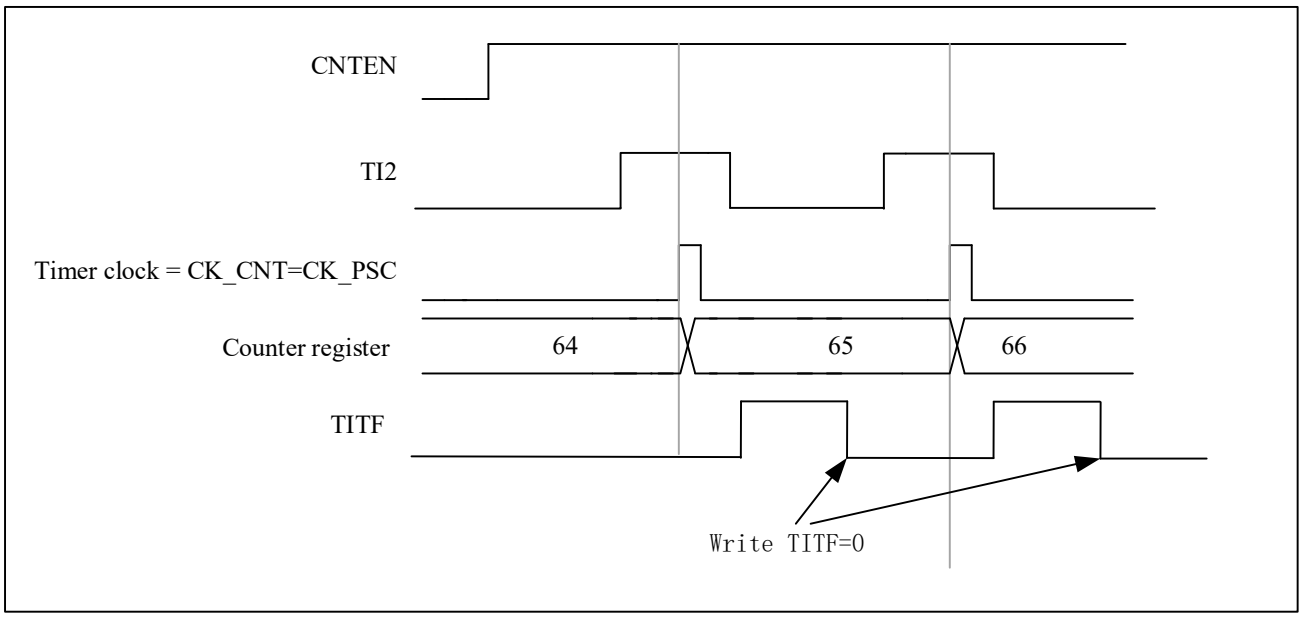
Figure 12-10 Control circuit in external clock mode 1

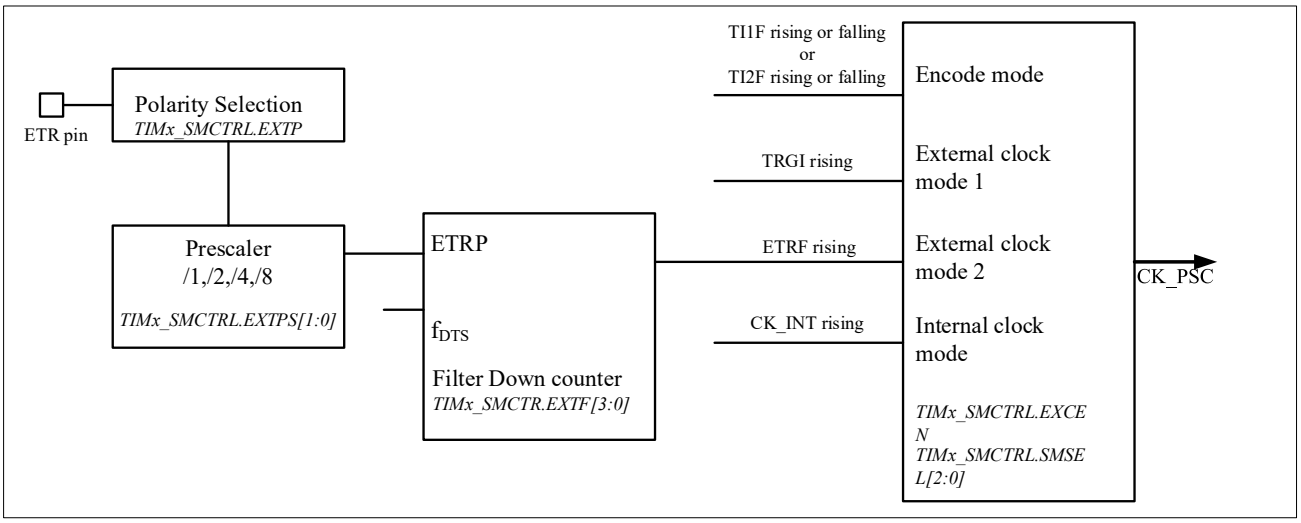


12.3.3.3 External clock source mode 2

This mode is selected by TIMx_SMCTRL .EXCEN equal to 1. The counter can count on every rising or falling edge of the external trigger input ETR.

The following figure is a schematic diagram of the external trigger input module in External clock source mode 2

Figure 12-11 External trigger input block diagram



For example, use the following configuration steps to make the up counter count every 2 rising edges on ETR.

- Since no filter is needed in this case, make TIMx_SMCTRL .EXTF[3:0] equal to '0000'
- Configure the prescaler by making TIMx_SMCTRL.EXTPS[1:0] equal to '01'
- Select the polarity on ETR pin by setting TIMx_SMCTRL.EXTP equal to '0', The rising edge of ETR is valid
- External clock mode 2 is selected by setting TIMx_SMCTRL .EXCEN equal to '1'
- Turn on the counter by setting TIMx_CTRL1. CNTEN equal to '1'

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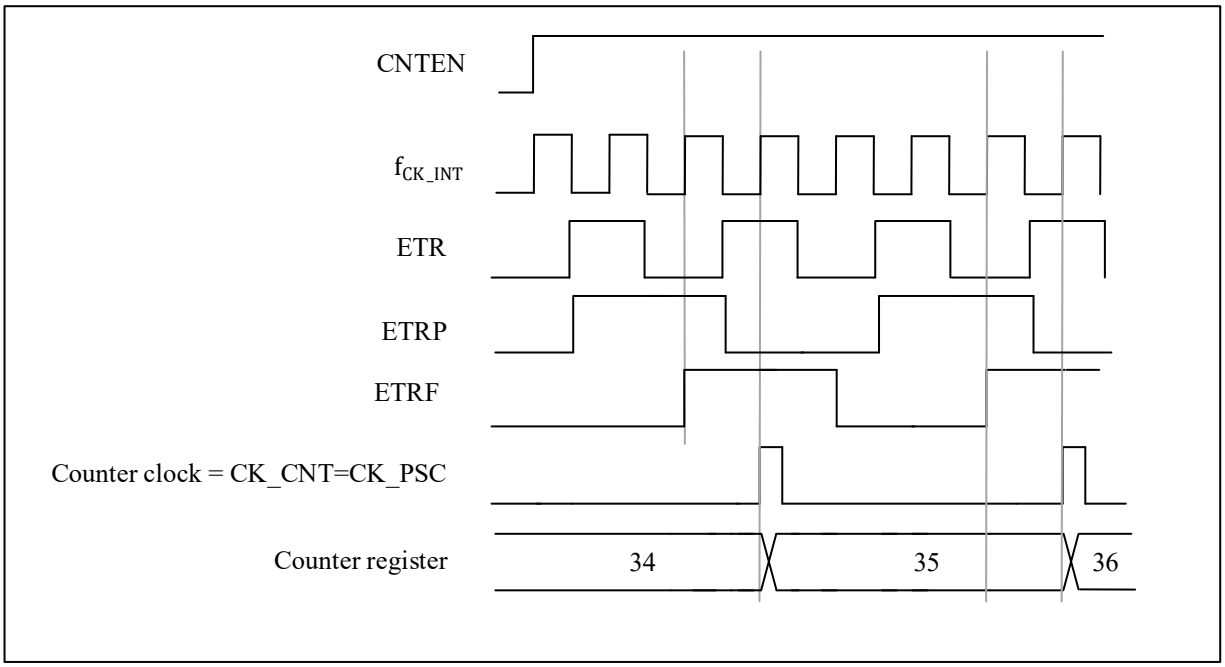
The counter counts every 2 rising edges of ETR. The delay between the rising edge of ETR and the actual clock to the counter is due to a resynchronization circuit on the ETRP signal.

Figure 12-12 Control circuit in external clock mode 2



12.3.4 Capture/Compare Channels

Capture/compare channels include capture/compare registers and shadow registers. The input section consists of digital filters, multiplexers and prescalers. The output section includes comparators and output controls.

The input signal TIx is sampled and filtered to generate the signal TIxF. A signal (TIxF_rising or TIxF_falling) is then generated by the edge detector of the polarity select function, the polarity of which is selected by the TIMx_CCEN.CCxP bits. This signal can be used as a trigger input for the slave mode controller. At the same time, the signal ICx is sent to the capture register after frequency division. The following figure shows a block diagram of a capture/compare channel.

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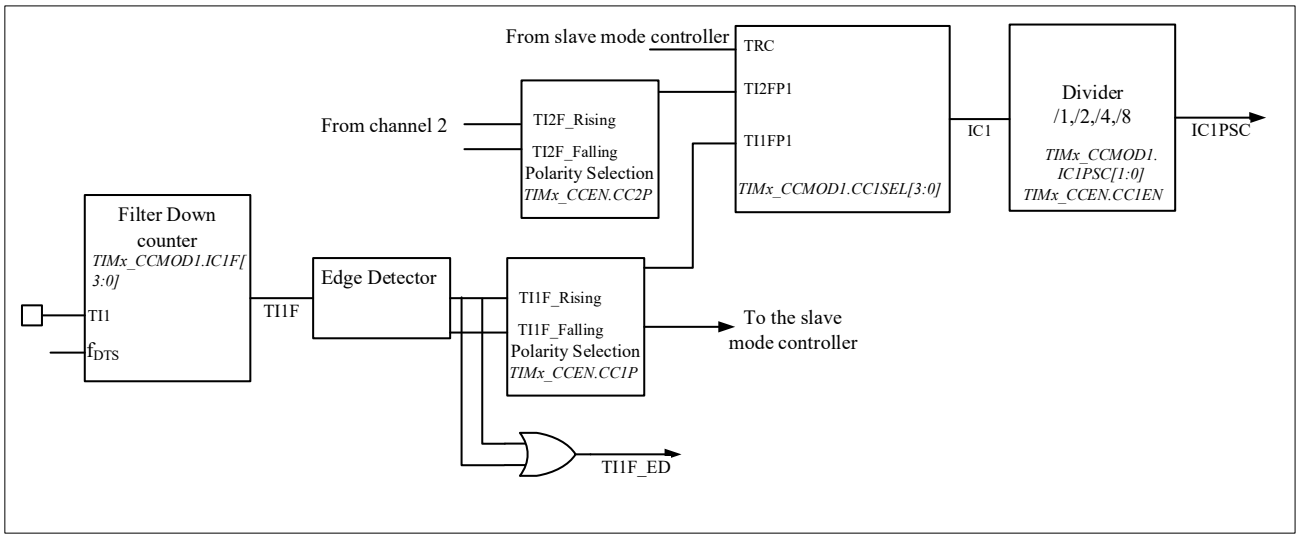
Figure 12-13 Capture/compare channel (example: channel 1 input stage)



The output part generates an intermediate waveform OCxRef (active high) as reference. The polarity acts at the end of the chain.

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Figure 12-14 Capture/compare channel 1 main circuit

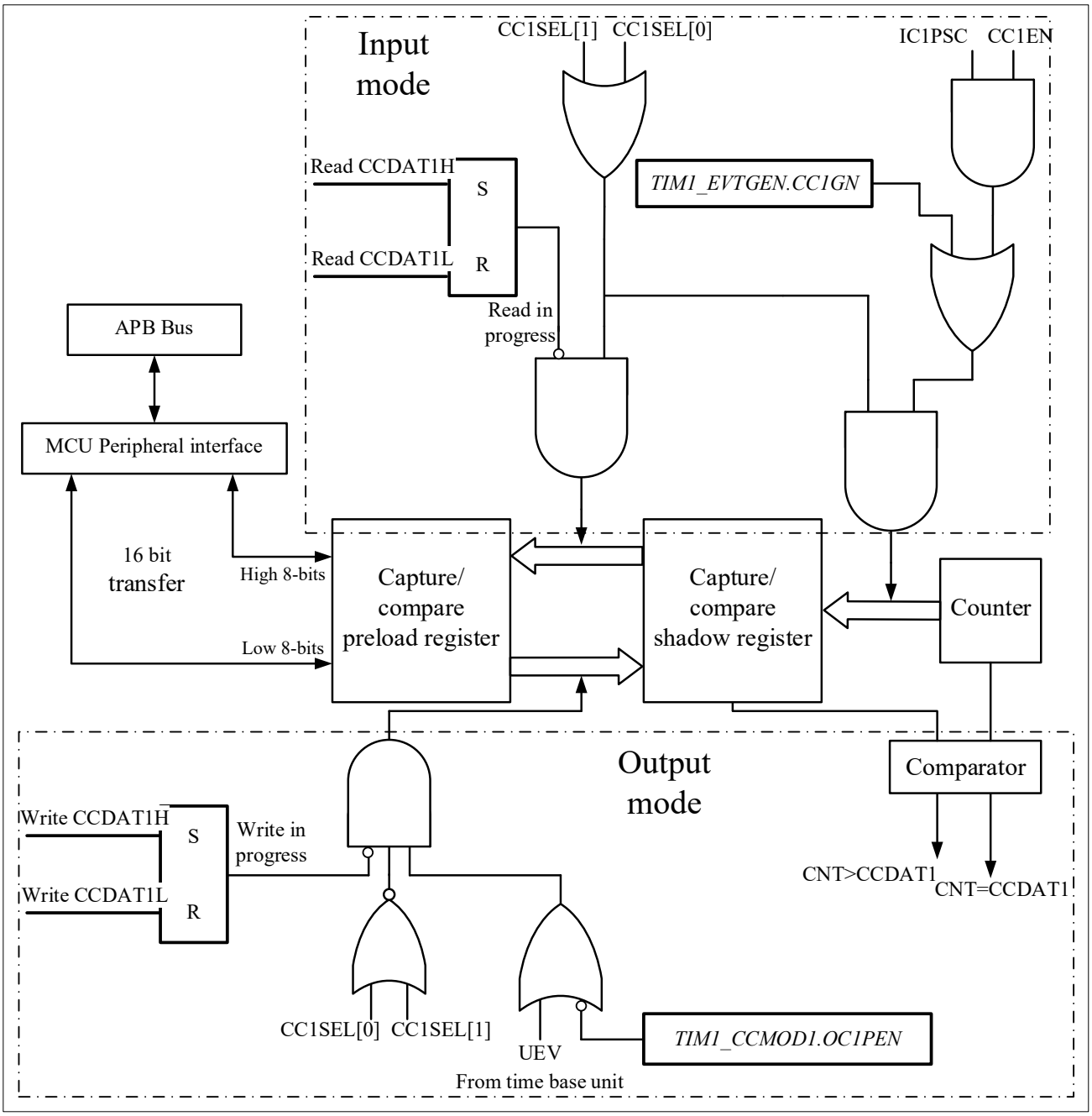

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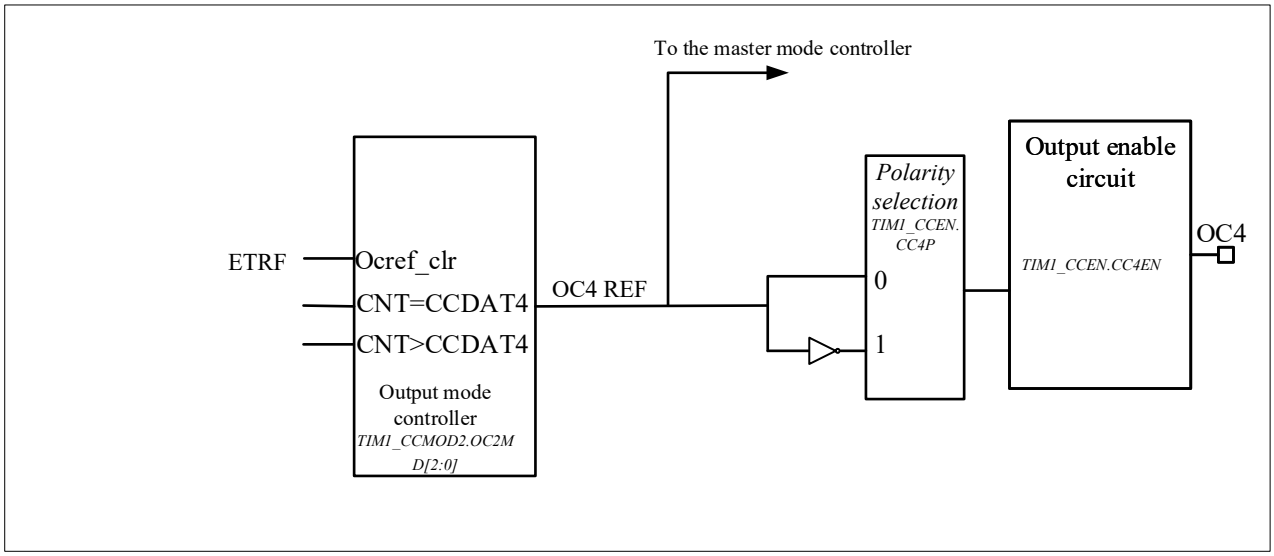
Figure 12-15 Output part of channelx （x = 1,2,3,4;take channel 4 as an example）



Reads and writes always access preloaded registers when capturing/comparing. The two specific working processes are as follows:

In capture mode, the capture is actually done in the shadow register, and then the value in the shadow register is copied into the preload register.

In compare mode, as opposed to capture mode, the value of the preload register is copied into the shadow register, which is compared with the counter.

12.3.5 Input Capture Mode

In capture mode, the TIMx_CCDATx registers are used to latch the counter value after the ICx signal detects.

There is a capture interrupt flag TIMx_STS.CCxITF, which can issue an interrupt or DMA request if the corresponding interrupt enable is pulled high.

The TIMx_STS. CCxITF bit is set by hardware when a capture event occurs and is cleared by software or by reading the TIMx_CCDATx register.

The overcapture flag TIMx_STS.CCxOCF is set equal to 1 when the counter value is captured in the TIMx_CCDATx register and TIMx_STS.CC1ITF is already pulled high. Unlike the former, TIMx_STS.CCxOCF is cleared by writing 0 to it.

To achieve a rising edge of the TI1 input to capture the counter value into the TIMx_CCDAT1 register, the configuration flow is as follows:

- To select a valid input:

  Configure TIMx_CCMOD1.CC1SEL to ‘01’. At this time, the input is the CC1 channel, and IC1 is mapped to TI1.

- Program the desired input filter duration:

  Define the sampling frequency of the TI1 input and the length of the digital filter by configuring the TIMx_CCMODx.ICxF bits. Example: If the input signal jitters up to 5 internal clock cycles, we must choose a

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filter duration longer than these 5 clock cycles. When 8 consecutive samples (sampled at f_{DTS} frequency) with the new level are detected, we can validate the transition on TI1. Then configure TIMx_CCMOD1. IC1F to '0011'.

- By configuring TIMx_CCEN .CC1P=0, select the rising edge as the valid transition polarity on the TI1 channel.
- Configure the input prescaler. In this example, configure TIMx_CCMOD1.IC1PSC= '00' to disable the prescaler because we want to capture every valid transition.
- Enable capture by configuring TIMx_CCEN. CC1EN = '1'.

If you want to enable DMA request, you can configure TIMx_DINTEN.CC1DEN=1.If you want enable related interrupt request, you can configureTIMx_DINTEN.CC1IEN bit=1

12.3.6 PWM Input Mode

There are some differences between PWM input mode and normal input capture mode, including:

- Two ICx signals are mapped to the same TIx input.
- The two ICx signals are active on edges of opposite polarity.
- Select one of two TIxFP signals as trigger input.
- The slave mode controller is configured in reset mode.

For example, the following configuration flow can be used to know the period and duty cycle of the PWM signal on TI1 (It depends on the frequency of CK_INT and the value of the prescaler).

- Configure TIMx_CCMOD1.CC1SEL equal to '01' to select TI1 as valid input for TIMx_CCDAT1.
- Configure TIMx_CCEN.CC1P equal to '0' to select the active polarity of filtered timer input 1(TI1FP1), valid on the rising edge.
- Configure TIMx_CCMOD1.CC2SEL equal to '10' select TI1 as valid input for TIMx_CCDAT2.
- Configure TIMx_CCEN.CC2P equal to 1 to select the valid polarity of filtered timer input 2(TI1FP2), valid on the falling edge.
- Configure TIMx_SMCTRL.TSEL=101 to select Filtered timer input 1 (TI1FP1) as valid trigger input.
- Configure TIMx_SMCTRL.SMSEL=100 to configure the slave mode controller to reset mode.
- Configure TIMx_CCEN. CC1EN=1 and TIMx_CCEN.CC2EN=1 to enable capture.

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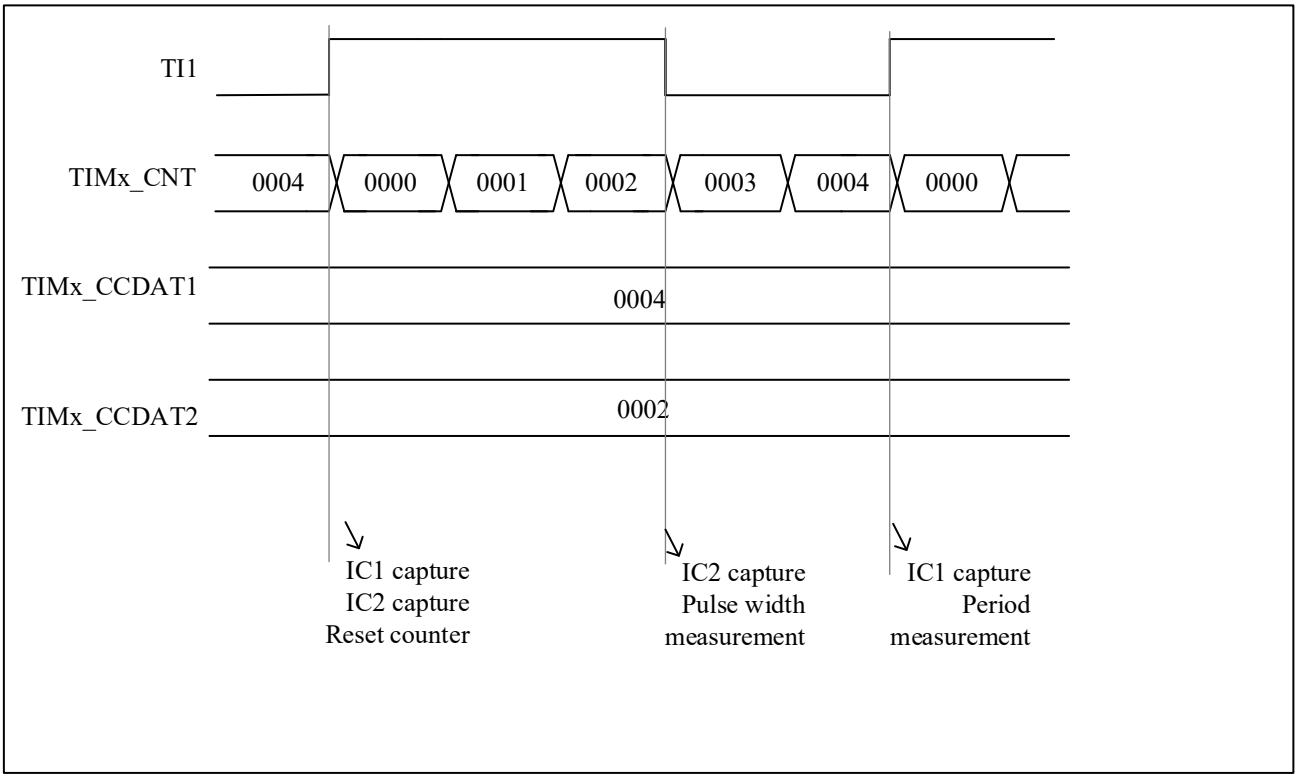
Figure 12-16 PWM input mode timing



Because of only filter timer input 1 (TI1FP1) and filter timer input 2 (TI2FP2) are connected to the slave mode controller, the PWM input mode can only be used with the TIMx_CH1/TIMx_CH2 signals.

12.3.7 Forced Output Mode

Software can force output compare signals to active or inactive level directly, in output mode (TIMx_CCMODx.CCxSEL=00).

User can set TIMx_CCMODx. OCxMD=101 to force the output compare signal to active level. And the OCxREF will be forced high, OCx get opposite value to CCxP polarity bit. On the other hand, user can set TIMx_CCMODx. OCxMD=100 to force the output compare signal to inactive level.

The values of the TIMx_CCDATx shadow register and the counter still comparing with each other in this mode. And the flag still can be set. Therefore, the interrupt and DMA requests still can be sent.

The comparison between the output compare register TIMx_CCDATx and the counter TIMx_CNT has no effect on OCxREF. And the flag still can be set. Therefore, the interrupt and DMA requests still can be sent.

12.3.8 Output Compare Mode

User can use this mode to control the output waveform, or to indicate that a period of time has elapsed.

When the capture/compare register and the counter have the same value, the output compare function's operations are as follow:

- TIMx_CCMODx.OCxMD is for output compare mode, and TIMx_CCEN.CCxP is for output polarity. When the compare matches, if set TIMx_CCMODx.OCxMD=000, the output pin will keep its level;if set

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TIMx_CCMODx.OCxMD=001, the output pin will be set active;if set TIMx_CCMODx.OCxMD=010, the output pin will be set inactive;if set TIMx_CCMODx.OCxMD=011, the output pin will be set to toggle.

- Set TIMx_STS.CCxITF.
- If user set TIMx_DINTEN.CCxIEN, a corresponding interrupt will be generated.
- If user set TIMx_DINTEN.CCxDEN and set TIMx_CTRL2.CCDSEL to select DMA request, and DMA request will be sent.

User can set TIMx_CCMODx.OCxPEN to choose capture/compare shawdow regisete using capture/compare preload registers(TIMx_CCDATx) or not.

The time resolution is one count of the counter.

In one pulse mode, the output compare mode can also be used to output a single pulse.

Here are the configuration steps for output compare mode:

- First of all, user should select the counter clock.
- Secondly, set TIMx_AR and TIMx_CCDATx with desired data.
- If user need to generate an interrupt, set TIMx_DINTEN.CCxIEN.
- Then select the output mode by set TIMx_CCEN.CCxP, TIMx_CCMODx.OCxMD, TIMx_CCEN.CCxEN, etc.
- At last, set TIMx_CTRL1.CNTEN to enable the counter.

User can update the output waveform by setting TIMx_CCDATx at any time, as long as the preload register is not enabled. Otherwise the TIMx_CCDATx shadow register will be updated at the next update event.

Here is an example.

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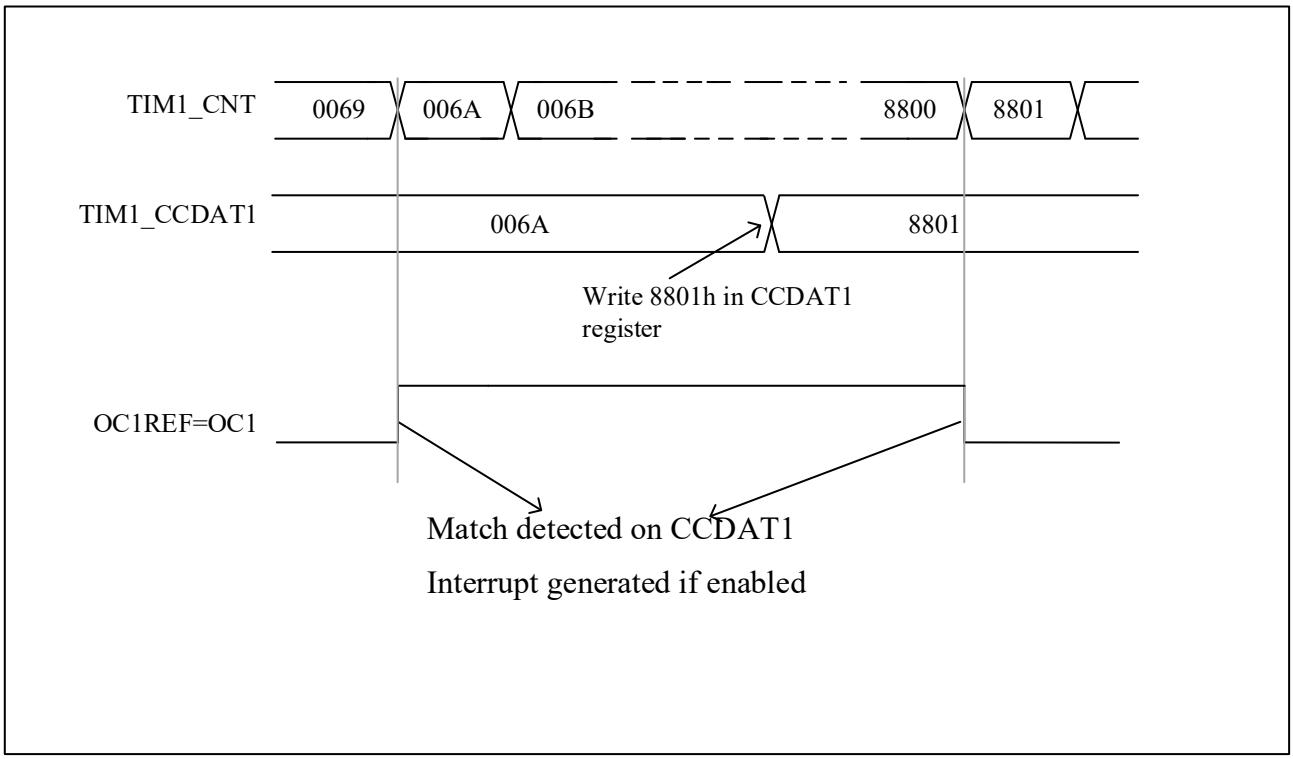
Figure 12-17 Output compare mode, toggle on OC1



12.3.9 PWM Mode

User can use PWM mode to generate a signal whose duty cycle is determined by the value of the TIMx_CCDATx register and whose frequency is determined by the value of the TIMx_AR register. And depends on the value of TIMx_CTRL1.CAMSEL, the TIM can generate PWM signal in edge-aligned mode or center-aligned mode.

User can set PWM mode 1 or PWM mode 2 by setting TIMx_CCMODx. OCxMD=110 or setting TIMx_CCMODx. OCxMD=111. To enable preload register, user must set corresponding TIMx_CCMODx.OCxPEN. And then set TIMx_CTRL1.ARPEN to auto-reload preload register eventually.

User can set polarity of OCx by setting TIMx_CCEN.CCxP. To enable the output of OCx, user need to set the combination of the value of CCxEN.

The values of TIMx_CNT and TIMx_CCDATx are always compared with each other when the TIM is under PWM mode.

Only if an update event occurs, the preload register will transfer to the shadow register. Therefore user must reset all the registers by setting TIMx_EVTGEN.UDGN before the counter starts counting.

12.3.9.1 PWM center-aligned mode

If user set TIMx_CTRL1.CAMSEL equal 01, 10 or 11, the PWM center-aligned mode will be active. The setting of the compare flag depends on the value of TIMx_CTRL1.CAMSEL. There are three kinds of situation that the compare flag is set, only when the counter counts up, only when the counter counts down, or when the counter counts up and counts down. User should not modified TIMx_CTRL1.DIR by software, it is updated by hardware.

Examples of center-aligned PWM waveforms is as follow, and the setting of the waveform are: TIMx_AR=8, PWM mode 1, the compare flag is set when the counter counts down corresponding to TIMx_CTRL1. CAMSEL=01.

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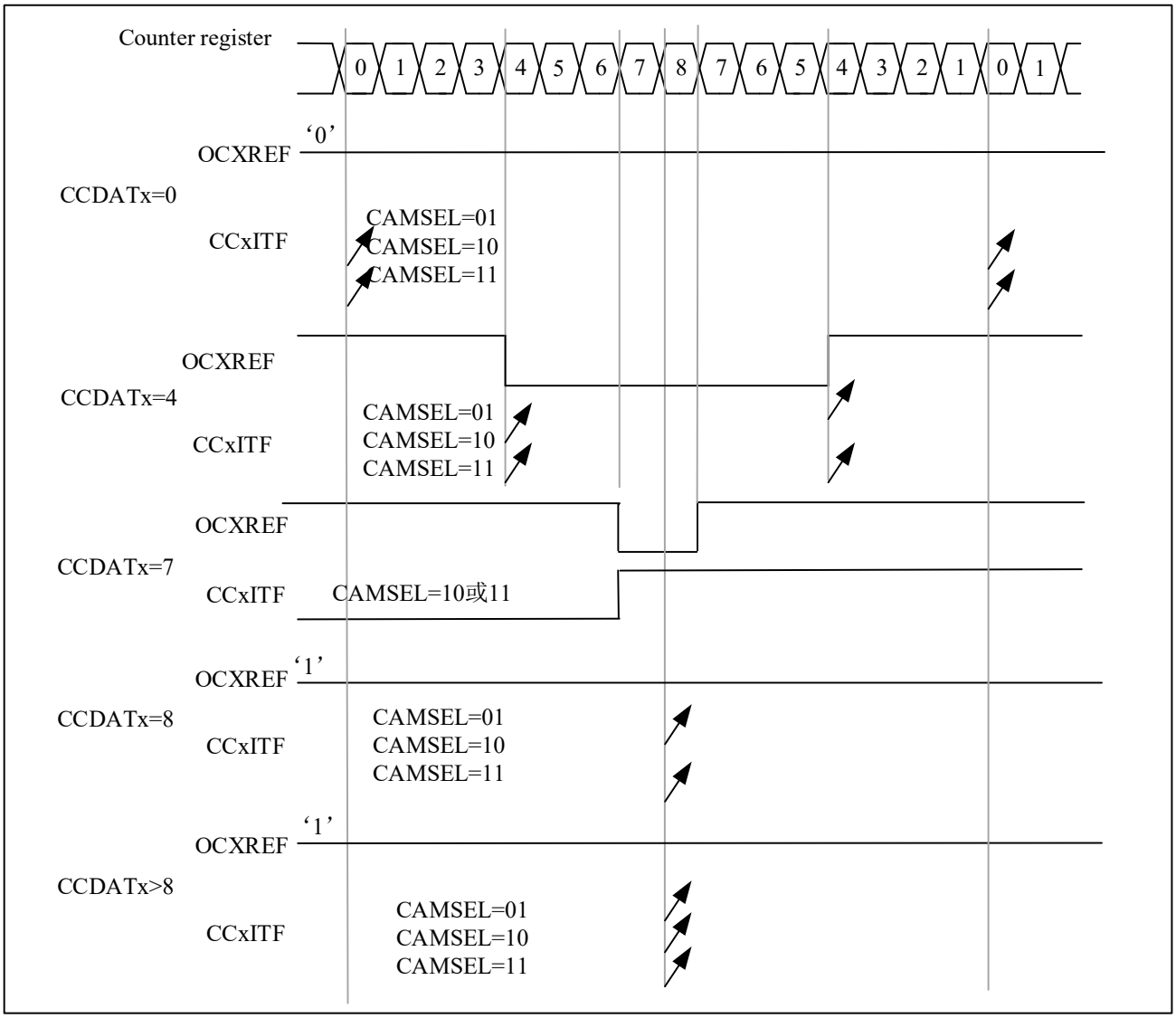
Figure 12-18 Center-aligned PWM waveform (AR=8)



Notes that user should know when using center-aligned mode are as follow:

- It depends on the value of TIMx_CTRL1.DIR that the counter counts up or down. Cautions that the DIR and CAMSEL bits should not be changed at the same time.
- User should not write the counter while running in center-aligned mode, otherwise it will cause unexpected results. Here are some example:
  - If the value written into the counter is 0 or is the value of TIMx_AR, the direction will be updated but the update event will not be generated.
  - If the value written into the counter is greater than the value of auto-reload, the direction will not be updated.
- To be on the safe side, user is suggested setting TIMx_EVTGEN.UDGN to generate an update by software before starting the counter, and not writing the counter while it is running.

12.3.9.2 PWM edge-aligned mode

There are two kinds of configuration in edge-aligned mode, up-counting and down-counting.

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- **Up-counting**

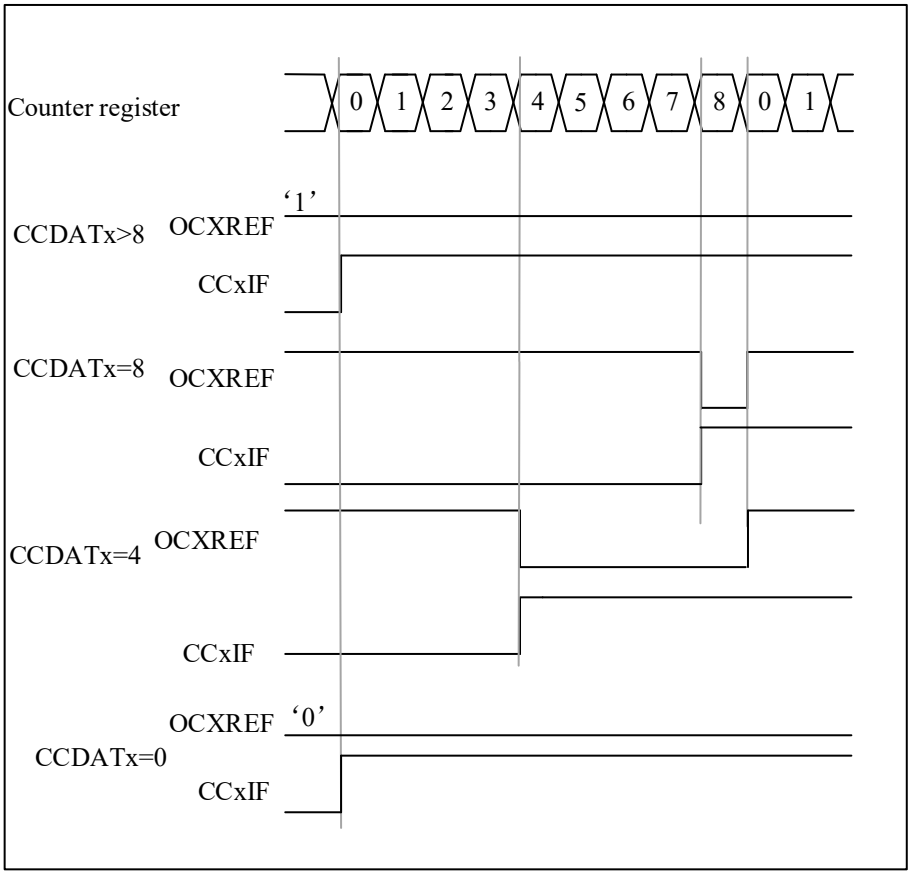
User can set TIMx_CTRL1.DIR=0 to make counter counts up.

Here is an example for PWM mode1.

When TIMx_CNT < TIMx_CCDATx, the reference PWM signal OCxREF is high. Otherwise it will be low. If the compare value in TIMx_CCDATx is greater than the auto-reload value, the OCxREF will remains 1. Conversely, if the compare value is 0, the OCxREF will remains 0.

When TIMx_AR=8, the PWM waveforms are as follow.

Figure 12-19 Edge-aligned PWM waveform (APR=8)



- **Down-counting**

User can set TIMx_CTRL1.DIR=1 to make counter counts down.

Here is an example for PWM mode1.

When TIMx_CNT > TIMx_CCDATx, the reference PWM signal OCxREF is low. Otherwise it will be high. If the compare value in TIMx_CCDATx is greater than the auto-reload value, the OCxREF will remains 1.

Note: If the nth PWM cycle CCDATx shadow register >= AR value, the shadow register value of CCDATx in the (n+1)th PWM cycle is 0. At the moment when the counter is 0 in the (n+1)th PWM cycle, although the value of the counter = CCDATx shadow register = 0 and OCxREF = '0', no compare event will be generated.

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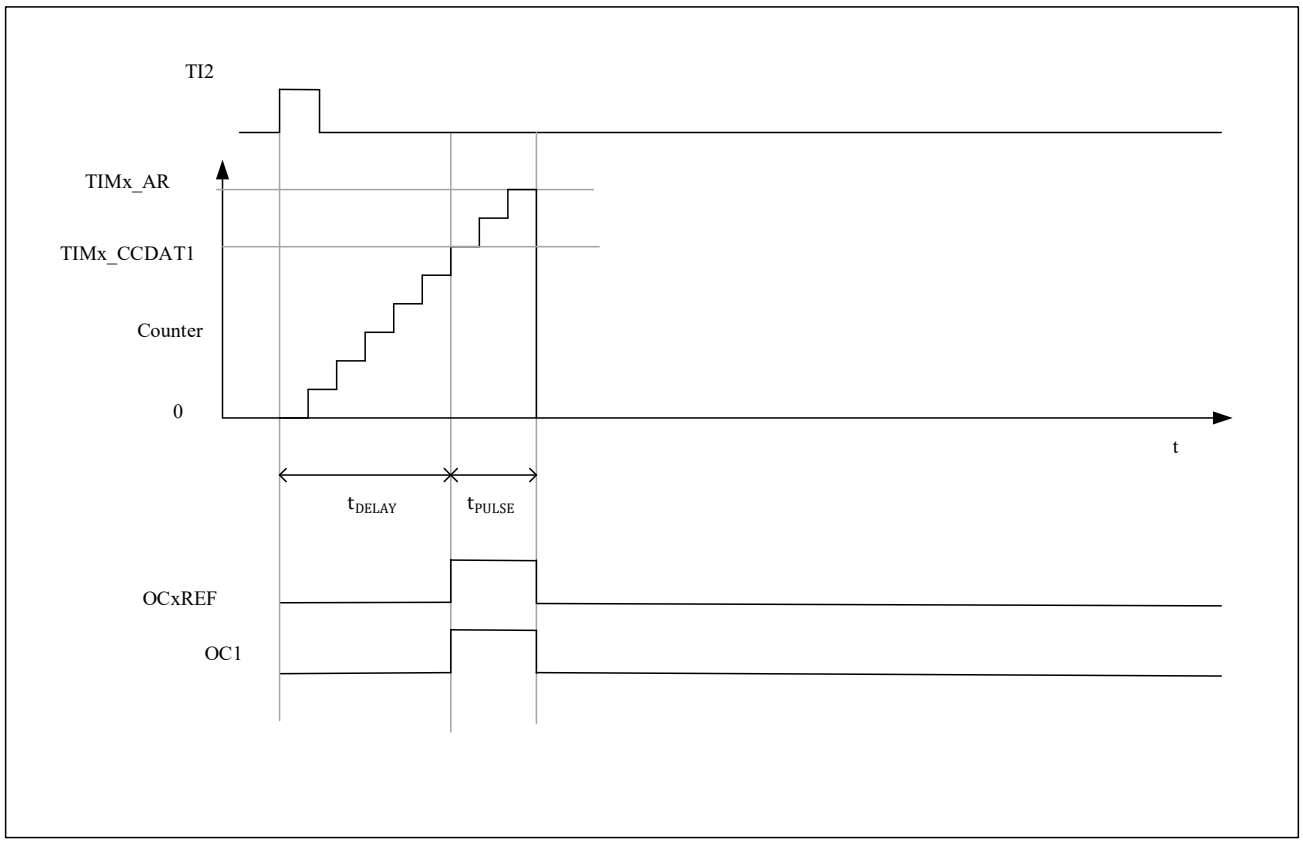
12.3.10 One-pulse Mode

In the one-pulse mode (ONEPM), a trigger signal is received, and a pulse t_{PULSE} with a controllable pulse width is generated after a controllable delay t_{DELAY}. The output mode needs to be configured as output compare mode or PWM mode. After selecting one-pulse mode, the counter will stop counting after the update event UEV is generated.

Figure 12-20 Example of One-pulse mode



The following is an example of a one-pulse mode:

A rising edge trigger is detected from the TI2 input, and a pulse with a width of t_{PULSE} is generated on OC1 after a delay of t_{DELAY}.

1. Counter configuration: count up, counter TIMx_CNT < TIMx_CCDAT1 ≤ TIMx_AR;

2. TI2FP2 is mapped to TI2, TIMx_CCMOD1.CC2SEL= '01'; TI2FP2 is configured for rising edge detection, TIMx_CCEN.CC2P= '0';

3. TI2FP2 acts as the trigger (TRGI) of the slave mode controller and starts the counter, TIMx_SMCTRL.TSEL= '110', TIMx_SMCTRL.SMSEL= '110' (trigger mode);

4. TIMx_CCDAT1 writes the count value to be delayed (t_{DELAY}), TIMx_AR - TIMx_CCDAT1 is the count value of the pulse width t_{PULSE};

5. Configure TIMx_CTRL1.ONEPM=1 to enable single pulse mode, configure TIMx_CCMOD1.OC1MD = '111' to select PWM2 mode;

6. Wait for an external trigger event on TI2, and a one pulse waveform will be output on OC1;

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12.3.10.1 Special case: OCx fast enable:

In one-pulse mode, an edge is detected through the TIx input, and triggers the start of the counter to count to the comparison value and then output a pulse. These operations limit the minimum delay t_{DELAY} that can be achieved.

You can set TIMx_CCMODx.OCxFEN=1 to turn on OCx fast enable, after triggering the rising edge, the OCxREF signal will be forced to be converted to the same level as the comparison match occurs immediately, regardless of the comparison result. OCxFEN fast enable only takes effect when the channel mode is configured for PWM1 and PWM2 modes.

12.3.11 Clearing the OCxREF Signal on an External Event

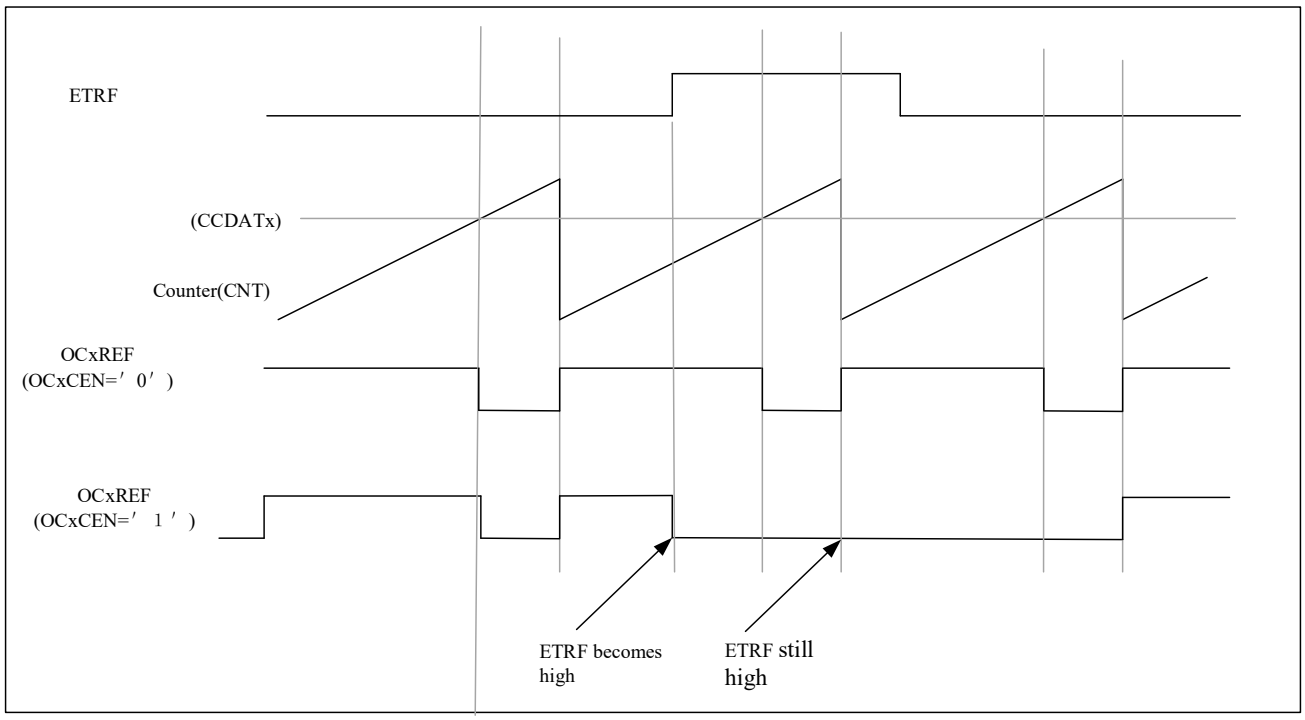
If user set TIMx_CCMODx.OCxCEN=1, high level of ETRF input can be used to driven the OCxREF signal to low, and the OCxREF signal will remains low, until the next UEV happens. Only output compare and PWM modes can use this function. This cannot be used when it is in forced mode.

Here is an example for it. To control the current, user can connect the ETR signal to the output of a comparator, and the operation for ETR should be as follow:

- Set TIMx_SMCTRL.EXTPS=00 to disable the external trigger prescaler.
- Set TIMx_SMCTRL.EXCEN=0 to disable the external clock mode 2.
- Set TIMx_SMCTRL.EXTP and TIMx_SMCTRL.EXTF to configure the external trigger polarity and external trigger filter according to the need.

Here is an example for the case that when ETRF input becomes high, the behavior of OCxREF signal for different value of OCxCEN. Timer is set to be in PWM mode in this case.

Figure 12-21 Control circuit in reset mode



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12.3.12 Debug Mode

When the microcontroller is in debug mode (the Cortex-M4 core halted), depending on the DBG_CTRL.TIMx_STOP configuration in the DBG module, the TIMx counter can either continue to work normally or stop. For more details, see 29.4.3.

12.3.13 TIMx and External Trigger Synchronization

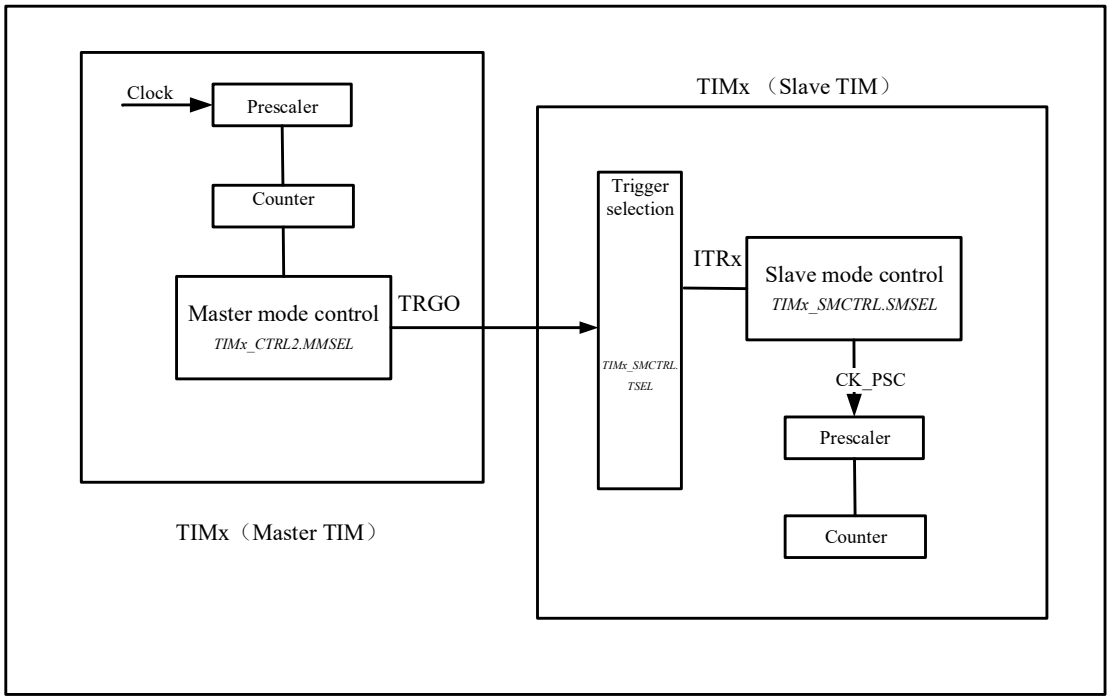
Same as advanced timer. See 11.3.16.

12.3.14 Timer Synchronization

All TIMx timers are internally connected to each other. This implementation allows any master timer to provide trigger to reset, start, stop or provide a clock for the other slave timers. The master clock is used for internal counter and can be prescaled. Below figure shows a Block diagram of timer interconnection.

The synchronization function does not support dynamic change of the connection. User should configure and enable the slave timer before enable the master timer's trigger or clock.

Figure 12-22 Block diagram of timer interconnection



12.3.14.1 Master timer as a prescaler for another timer

TIM1 as a prescaler for TIM2. TIM1 is maser, TIM2 is slave.

User need to do the following steps for this configuration.

- Setting TIM1_CTRL2.MMSEL=' 010' to use the update event of TIM1 as trigger output.
- Configure TIM2_SMCTRL. TSEL= '000' , connect the TRGO of TIM1 to TIM2.

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- Configure TIM2_SMCTRL.SMSEL = ‘111’, the slave mode controller will be configured in external clock mode 1.
- Start TIM2 by setting TIM2_CTRL1. CNTEN = ‘1’.
- Start TIM1 by setting TIM1_CTRL1. CNTEN = ‘1’.

Note: If user select OCx as the trigger output of TIM1 by configuring MMSEL = ‘1xx’, OCx rising edge will be used to drive timer2.

12.3.14.2 Master timer to enable another timer

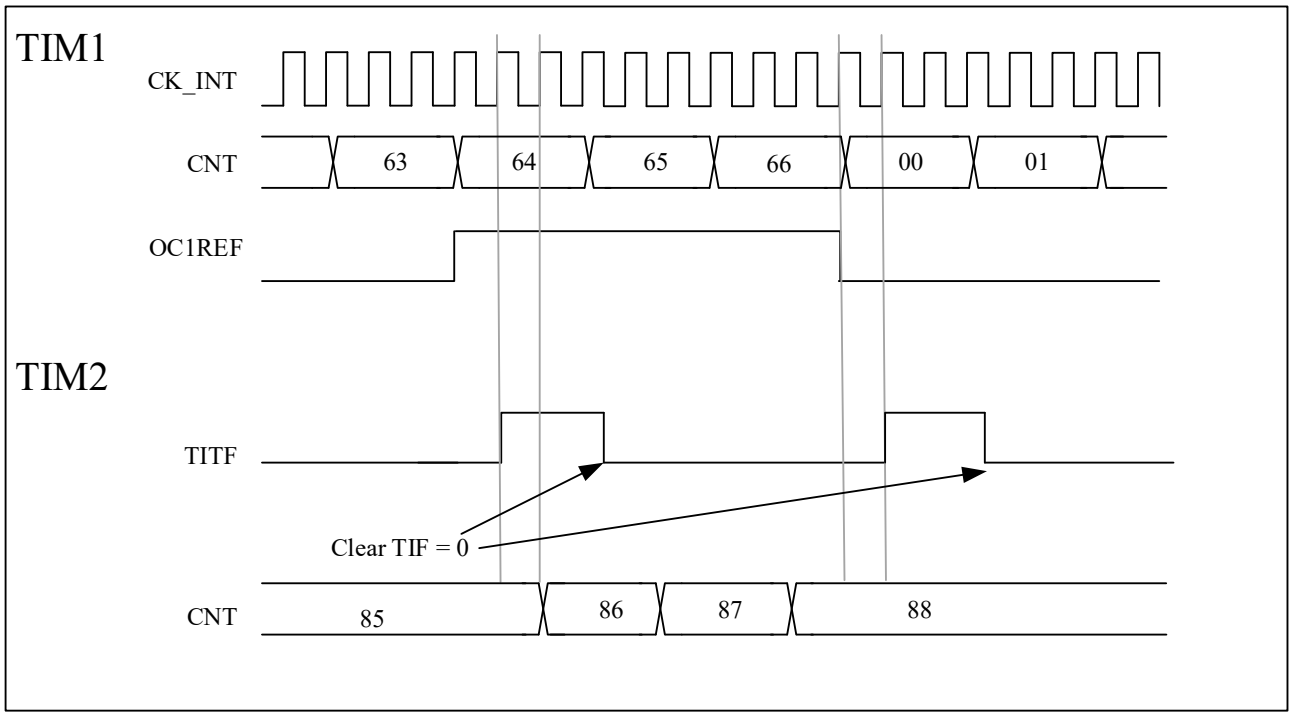
In this example, TIM2 is enabled by the output compare of TIM1. TIM2 counter will start to count after the OC1REF output from TIM1 is high. Both counters are clocked based on CK_INT via a prescaler divide by 3 is performed ($f_{CK\_CNT} = f_{CK\_INT}/3$).

The configuration steps are shown as below.

- Setting TIM1_CTRL2.MMSEL=’100’ to use the OC1REF of TIM1 as trigger output.
- Configure TIM1_CCMOD1 register to configure the OC1REF output waveform.
- Setting TIM2_SMCTRL.TSEL = ‘000’ to connect TIM1 trigger output to TIM2.
- Setting TIM2_SMCTRL.SMSEL= ‘101’ to set TIM2 to gated mode.
- Setting TIM2_CTRL1.CNTEN= ‘1’ to start TIM2.
- Setting TIM1_CTRL1.CNTEN= ‘1’ to start TIM1.

Note: The TIM2 clock is not synchronized with the TIM1 clock, this mode only affects the TIM2 counter enable signal.

Figure 12-23 TIM2 gated by OC1REF of TIM1



In the next example, Gated TIM2 with enable signal of TIM1, Setting TIM1.CTRL1.CNTEN = ‘0’ to stop TIM1. TIM2

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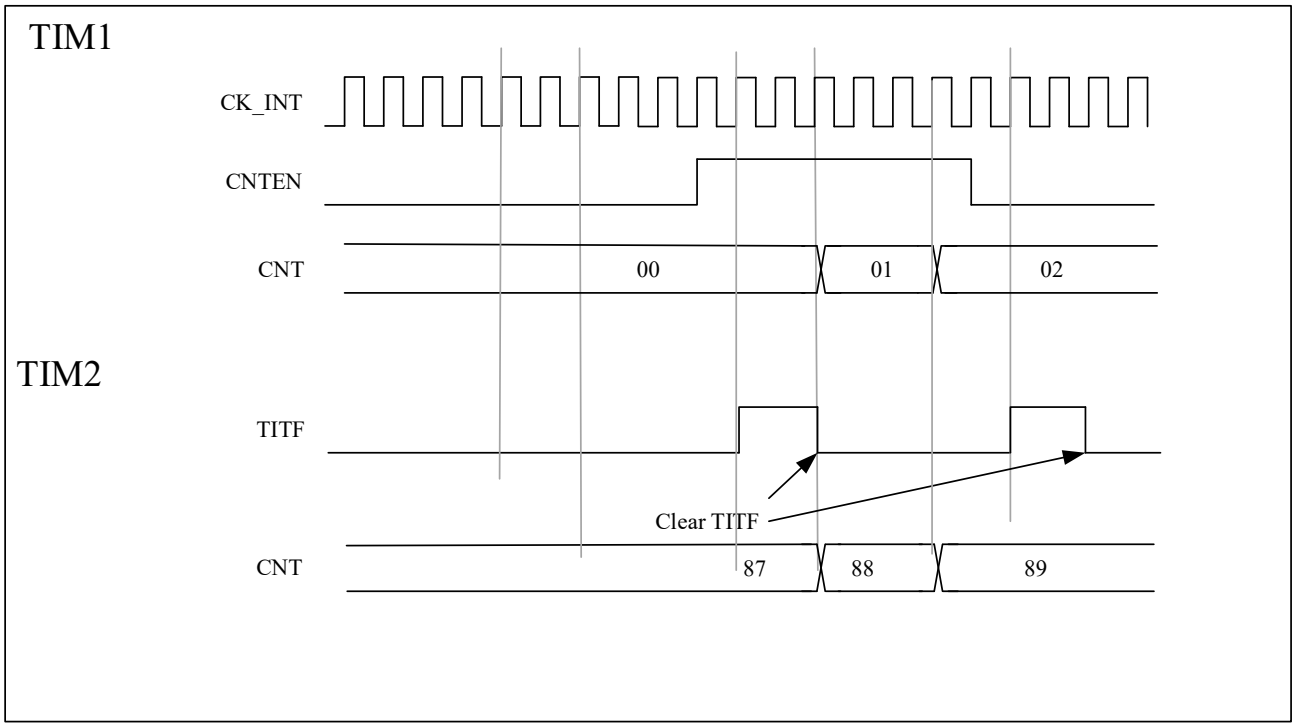
counts on the divided internal clock only when TIM1 is enable. Both counters are clocked based on CK_INT via a prescaler divide by 3 is performed ($f_{CK\_CNT} = f_{CK\_INT}/3$).

The configuration steps are shown as below

- Setting TIM1_CTRL2.MMSEL=' 001' to use the enable signal of TIM1 as trigger output
- Setting TIM2_SMCTRL.TSEL = '000' to configure TIM2 to get the trigger input from TIM1
- Setting TIM2_SMCTRL.SMSEL = '101' to configure TIM2 in gated mode.
- Setting TIM2_CTRL1.CNTEN= '1' to start TIM2.
- Setting TIM1_CTRL1.CNTEN= '1' to start TIM1.
- Setting TIM1_CTRL1.CNTEN= '0' to stop TIM1.

Figure 12-24 TIM2 gated by enable signal of TIM1



12.3.14.3 Master timer to start another timer

In this example, we can use update event as trigger source.TIM1 is master, TIM2 is slave.

The configuration steps are shown as below:

- Setting TIM1_CTRL2.MMSEL=' 010' to use the update event of TIM1 as trigger output
- Configure TIM1_AR register to set the output period.
- Setting TIM2_SMCTRL .TSEL= '000' to connect TIM1 trigger output to TIM2.
- Setting TIM2_SMCTRL. SMSEL = '110' to set TIM2 to trigger mode.
- Setting TIM1_CTRL1.CNTEN=1 to start TIM1.

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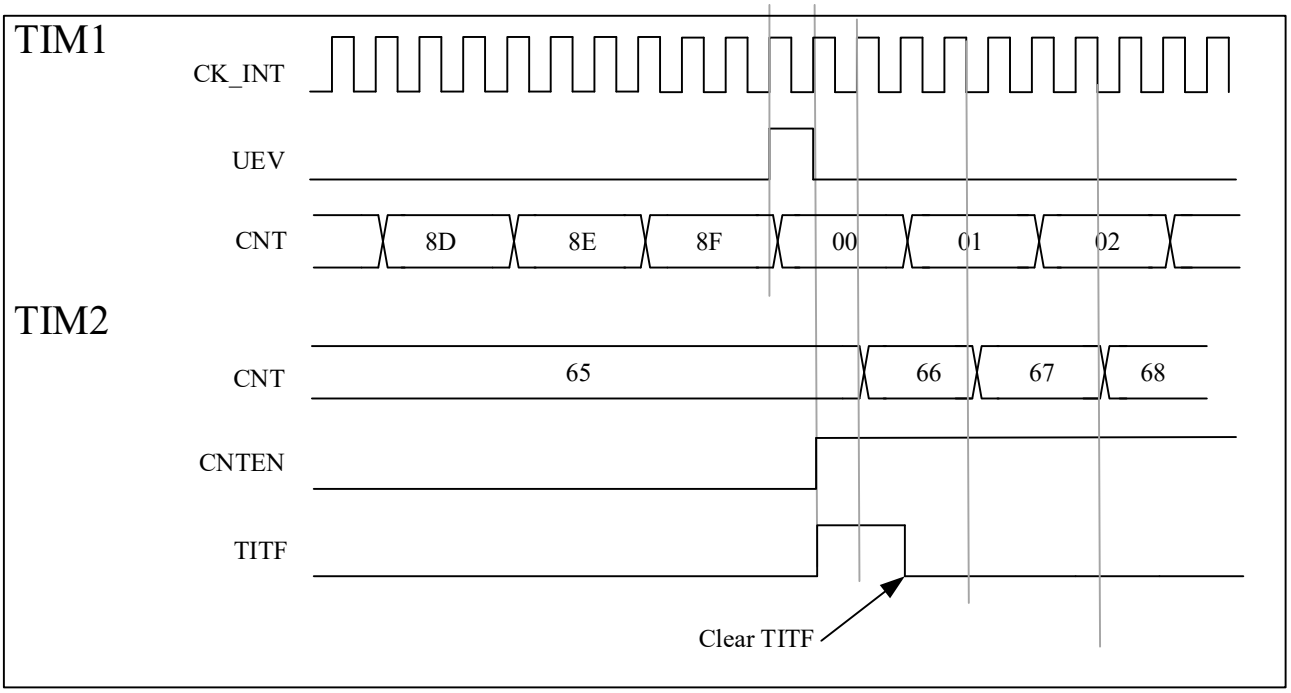
Figure 12-25 Trigger TIM2 with an update of TIM1



12.3.14.4 Start 2 timers synchronously using an external trigger

In this example, TIM1 is enabled when TIM1's TI1 input rises, and TIM2 is enabled when TIM1 is enabled. To ensure the alignment of counters, TIM1 must be configured in master/slave mode. For TI1, TIM1 is the slave; for TIM2, TIM1 is the master.

The configuration steps are shown as below:

- Setting TIM1.MMSEL = '001' to use the enable signal as trigger output
- Setting TIM1_SMCTRL.TSEL = '100' to configure the TIM1 to slave mode and receive the trigger input of TI1.
- Setting TIM1_SMCTRL .SMSEL = '110' to configure TIM1 to trigger mode.
- Setting TIM1_SMCTRL .MSMD = '1' to configure TIM1 to master/slave mode.
- Setting TIM2_SMCTRL .TSEL = '000' to connect TIM1 trigger output to TIM2.
- Setting TIM2_SMCTRL.SMSEL = '110' to configure TIM2 to trigger mode.

When TI1 rising edge arrives, both timers start counting synchronously according to the internal clock, and both TITF flags are set simultaneously.

The following figure shows a delay between CNTEN and CK_PSC of TIM1 in master/slave mode.

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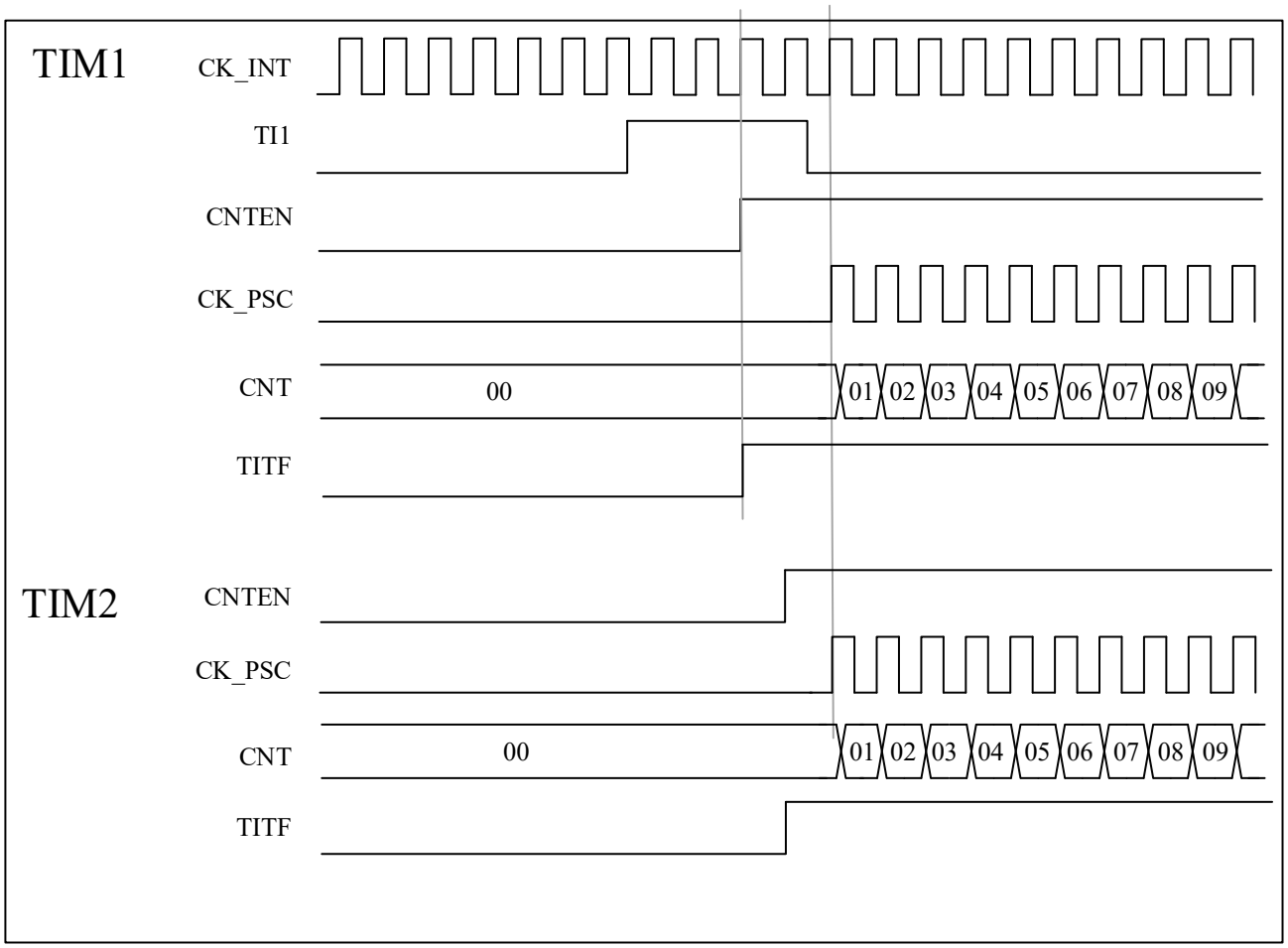
Figure 12-26 Triggers timers 1 and 2 using the TI1 input of TIM1



12.3.15 Encoder Interface Mode

The encoder uses two inputs TI1 and TI2 as an interface and the counter counts on every edge change on TI1FP1 or TI2FP2. The counting direction is automatically controlled by hardware TIMx_CTRL1.DIR. There are three types of encoder counting modes:

1. The counter only counts on the edge of TI1, TIMx_SMCTRL.SMSEL = ‘001’;

2. The counter only counts on the edge of TI2, TIMx_SMCTRL.SMSEL =’010’;

3. The counter counts on the edges of TI1 and TI2 at the same time, TIMx_SMCTRL.SMSEL = ‘011’;

The encoder interface is equivalent to using an external clock with direction selection, and the counter only counts continuously between 0 and the auto-reload value (TIMx_AR.AR [15:0]). Therefore, it is necessary to configure the auto-reload register TIMx_AR in advance.

Note: Encoder mode and external clock mode 2 are not compatible and must not be selected together.

The relationship between the counting direction and the encoder signal is shown in **Table 12-1**:

Table 12-1 Counting direction versus encoder signals

	Level on opposite signals	**TI1FP1 signal**	**TI2FP2 signal**

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Active edge	(TI1FP1 forTI2, TI2FP2 for TI1)	Rising	Falling	Rising	Falling
Counting only at TI1	High	Counting down	Counting up	Don't count	Don't count
	Low	Counting up	Counting down	Don't count	Don't count
Counting only at TI2	High	Don't count	Don't count	Counting up	Counting down
	Low	Don't count	Don't count	Counting down	Counting up
Counting on TI1 and TI2	High	Counting down	Counting up	Counting up	Counting down
	Low	Counting up	Counting down	Counting down	Counting up

Here is an example of an encoder with dual edge triggering selected to suppress input jitter:

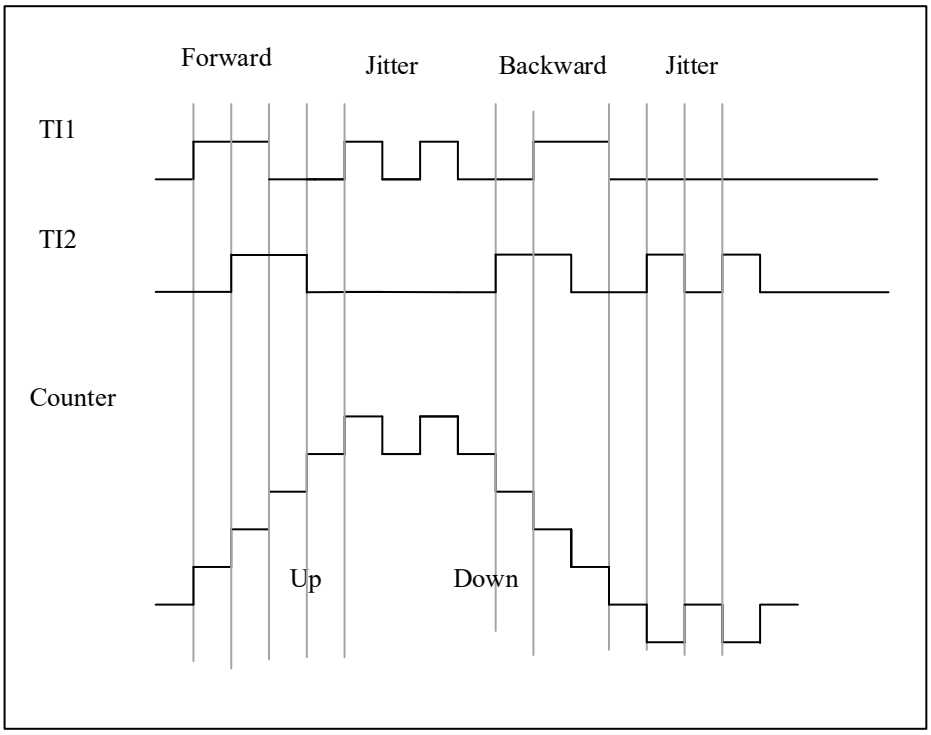
1. IC1FP1 is mapped to TI1 (TIMx_CCMOD1.CC1SEL= ‘01’), IC1FP1 is not inverted (TIMx_CCEN.CC1P= ‘0’);

2. IC1FP2 is mapped to TI2 (TIMx_CCMOD2.CC2SEL= ‘01’), IC2FP2 is not inverted (TIMx_CCEN.CC2P= ‘0’);

3. The input is valid on both rising and falling edges (TIMx_SMCTRL.SMSEL = ‘011’);

4. Enable counter TIMx_CTRL1.CNTEN= ‘1’;

Figure 12-27 Example of counter operation in encoder interface mode



The following figure shows the example of counter behavior when IC1FP1 polarity is inverted (CC1P= '1', other configurations are the same as above)

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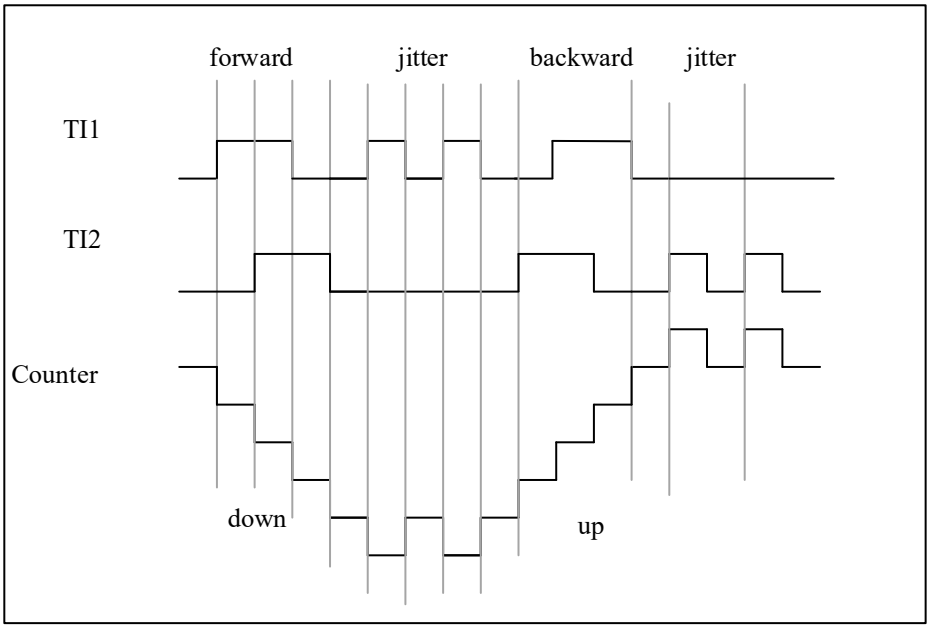
Figure 12-28 Encoder interface mode example with IC1FP1 polarity inverted



12.3.16 Interfacing with Hall Sensor

Please refer to 11.3.20

12.4 TIMx Register Description(x=2, 3 ,4 and 5)

For abbreviations used in registers, see section 1.1.

These peripheral registers can be operated as half word (16-bits) or one word (32-bits).

12.4.1 Register Overview

Table 12-2 Register map and reset value

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
000h	TIMx_CTRL1	Reserved																CLRSEL	C4SEL	C3SEL	C2SEL	C1SEL	Reserved	CLKD[1:0]		ARPEN	CAMSEL[1:0]		DIR	ONEPM	UPRS	UPDIS	CNTEN
	Reset Value																	0	0	0	0	0		0	0	0	0	0	0	0	0	0	0
004h	TIMx_CTRL2	Reserved																							ETRSEL	TI1SEL	MMSEL[2:0]			CCDSEL	Reserved		
	Reset Value																								0	0	0	0	0	0			
008h	TIMx_SMCTRL	Reserved																EXTP	EXCEN	EXTPS[1:0]		EXTF[3:0]				MSMD	TSEL[2:0]			Reserved	SMSELEL[2:0]		
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0		0	0	0
00Ch	TIMx_DINTEN	Reserved																	TDEN	Reserved	CC4DEN	CC3DEN	CC2DEN	CC1DEN	UDEN	Reserved	TIEN	Reserved	CC4IEN	CC3IEN	CC2IEN	CC1IEN	UIEN

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Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reset Value																		0		0	0	0	0	0		0		0	0	0	0	0	0
010h	TIMx_STS	Reserved																			CC4OCF	CC3OCF	CC2OCF	CC1OCF	Reserved		TITF	Reserved	CC4ITF	CC3ITF	CC2ITF	CC1ITF	UDITF
	Reset Value																				0	0	0	0			0		0	0	0	0	0
014h	TIMx_EVTGEN	Reserved																									TGN	Reserved	CC4GN	CC3GN	CC2GN	CC1GN	UDGN
	Reset Value																										0		0	0	0	0	0
018h	TIMx_CCMOD1	Reserved																OC2CEN	OC2MD[2:0]			OC2PEN	OC2FEN	CC2SEL[1:0]		OC1CEN	OC1MD[2:0]			OC1PEN	OC1FEN	CC1SEL[1:0]	
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	TIMx_CCMOD1	Reserved																IC2F[3:0]				IC2PSC[1:0]		CC2SEL[1:0]			IC1F[3:0]			IC1PSC[1:0]		CC1SEL[1:0]	
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
01Ch	TIMx_CCMOD2	Reserved																OC4CEN	OC4MD[2:0]			OC4PEN	OC4FEN	CC4SEL[1:0]		OC3CEN	OC3MD[2:0]			OC3PEN	OC3FEN	CC3SEL[1:0]	
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
01Ch	TIMx_CCMOD2	Reserved																IC4F[3:0]				IC4PSC[1:0]		CC4SEL[1:0]			IC3F[3:0]			IC3PSC[1:0]		CC3SEL[1:0]	
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
020h	TIMx_CCEN	Reserved																		CC4P	CC4EN	Reserved		CC3P	CC3EN	Reserved		CC2P	CC2EN	Reserved		CC1P	CC1EN
	Reset Value																			0	0			0	0			0	0			0	0
024h	TIMx_CNT	Reserved																CNT[15:0]															
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
028h	TIMx_PSC	Reserved																PSC[15:0]															
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
02Ch	TIMx_AR	Reserved																AR[15:0]															
	Reset Value																	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
030h	Reserved																																
034h	TIMx_CCDAT1	Reserved																CCDAT1[15:0]															
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
038h	TIMx_CCDAT2	Reserved																CCDAT2[15:0]															
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
03Ch	TIMx_CCDAT3	Reserved																CCDAT3[15:0]															
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
040h	TIMx_CCDAT4	Reserved																CCDAT4[15:0]															
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
044h	Reserved																																
048h	TIMx_DCTRL	Reserved																			DBLEN[4:0]					Reserved		DBADDR[4:0]				
	Reset Value																				0	0	0	0	0			0	0	0	0	0
04Ch	TIMx_DADDR	Reserved																BURST[15:0]															
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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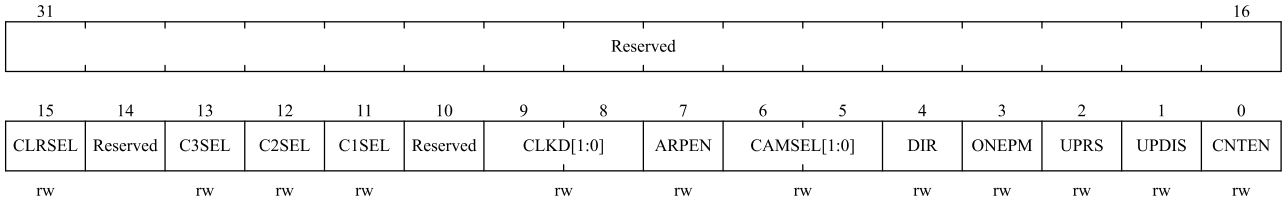
12.4.2 Control Register 1 (TIMx_CTRL1)

Offset address: 0x00

Reset value: 0x0000 0000



Bit field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained
15	CLRSEL	OCxREF clear selection 0: Select the external OCxREF clear from ETR 1: Select the internal OCxREF clear from comparator *Note: For TIM5, setting to 1 is invalid* *Before operating this bit, the extended mode of the chip must be turned on (set PWR_CTRL3.EXMODE)*
14	C4SEL	Channel 4 Selection 0: Select external CH4 (from IOM) signal 1: Select internal CH4 (from COMP) signal *Note: For TIM5, setting to 1 is invalid* *Before operating this bit, the extended mode of the chip must be turned on (set PWR_CTRL3.EXMODE)*
13	C3SEL	Channel 3 Selection 0: Select external CH3 (from IOM) signal 1: Seleect internal CH3 (from COMP) signal *Note:Before operating this bit, the extended mode of the chip must be turned on (set PWR_CTRL3.EXMODE)*
12	C2SEL	Channel 2 Selection 0: Select external CH2 (from IOM) signal 1: Seleect internal CH2 (from COMP) signal *Note:Before operating this bit, the extended mode of the chip must be turned on (set PWR_CTRL3.EXMODE)*
11	C1SEL	Channel 1 selection 0: Select external CH1 (from IOM) signal 1: Select internal CH1 (from COMP) signal *Note:Before operating this bit, the extended mode of the chip must be turned on (set PWR_CTRL3.EXMODE)*
10	Reserved	Reserved, the reset value must be maintained

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Bit field	Name	Description
9:8	CLKD[1:0]	Clock division CLKD[1:0] indicates the division ratio between CK_INT (timer clock) and t_{DTS} (clock used for dead-time generator and digital filters (ETR, TIx)) 00: $t_{DTS} = t_{CK\_INT}$ 01: $t_{DTS} = 2 \times t_{CK\_INT}$ 10: $t_{DTS} = 4 \times t_{CK\_INT}$ 11: Reserved, do not use this configuration
7	ARPEN	ARPEN: Auto-reload preload enable 0: Shadow register disable for TIMx_AR register 1: Shadow register enable for TIMx_AR register
6:5	CAMSEL[1:0]	Center-aligned mode selection 00: Edge-aligned mode. TIMx_CTRL1.DIR specifies up-counting or down-counting. 01: Center-aligned mode 1. The counter counts in center-aligned mode, and the output compare interrupt flag bit is set to 1 when down-counting. 10: Center-aligned mode 2. The counter counts in center-aligned mode, and the output compare interrupt flag bit is set to 1 when up-counting. 11: Center-aligned mode 3. The counter counts in center-aligned mode, and the output compare interrupt flag bit is set to 1 when up-counting or down-counting. *Note: Switching from edge-aligned mode to center-aligned mode is not allowed when the counter is still enabled (TIMx_CTRL1.CNTEN = 1).*
4	DIR	Direction 0: Up-counting 1: Down-counting *Note: This bit is read-only when the counter is configured in center-aligned mode or encoder mode.*
3	ONEPM	One-pulse mode 0: Disable one-pulse mode, the counter counts are not affected when an update event occurs. 1: Enable one-pulse mode, the counter stops counting when the next update event occurs (clearing TIMx_CTRL1.CNTEN bit)
2	UPRS	Update request source This bit is used to select the UEV event sources by software. 0: If update interrupt or DMA request is enabled, any of the following events will generate an update interrupt or DMA request: – Counter overflow/underflow – The TIMx_EVTGEN.UDGN bit is set – Update generation from the slave mode controller 1: If update interrupt or DMA request is enabled, only counter overflow/underflow will generate update interrupt or DMA request

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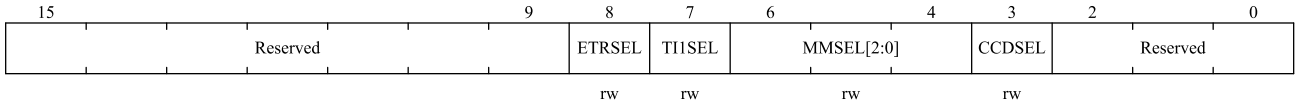
Bit field	Name	Description
1	UPDIS	Update disable This bit is used to enable/disable the Update event (UEV) events generation by software. 0: Enable UEV. And UEV will be generated if one of following condition been fulfilled: – Counter overflow/underflow – The TIMx_EVTGEN.UDGN bit is set – Update generation from the slave mode controller Shadow registers will update with preload value. 1: UEV disabled. No update event is generated, and the shadow registers (AR, PSC, and CCDATx) keep their values. If the TIMx_EVTGEN.UDGN bit is set or a hardware reset is issued by the slave mode controller, the counter and prescaler are reinitialized.
0	CNTEN	Counter Enable 0: Disable counter 1: Enable counter *Note: external clock, gating mode and encoder mode can only work after TIMx_CTRL1.CNTEN bit is set in the software. Trigger mode can automatically set TIMx_CTRL1.CNTEN bit by hardware.*

12.4.3 Control Register 2 (TIMx_CTRL2)

Offset address: 0x04

Reset value: 0x0000



Bit field	Name	Description
15:9	Reserved	Reserved, the reset value must be maintained
8	ETRSEL	External Triggered Selection storage (ETR Selection) 0: Select external ETR (from IOM) signal; 1: Reserved *Note:For the mapping of ETR input to IOM, see 7.2.5.7* *Before operating this bit, the extended mode of the chip must be turned on (set PWR_CTRL3.EXMODE)*
7	TI1SEL	TI1 selection 0: TIMx_CH1 pin connected to TI1 input. 1: TIMx_CH1, TIMx_CH2, and TIMx_CH3 pins are XOR connected to the TI1 input.

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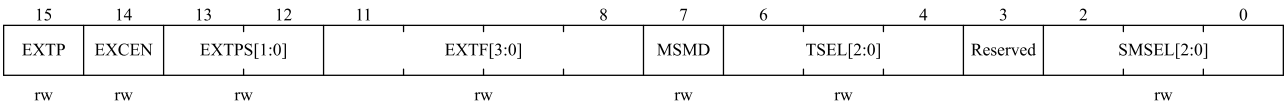
Bit field	Name	Description
6:4	MMSEL[2:0]	Master Mode Selection These 3 bits (TIMx_CTRL2. MMSEL [2:0]) are used to select the synchronization information (TRGO) sent to the slave timer in the master mode. Possible combinations are as follows: 000: Reset –When the TIMx_EVTGEN.UDGN is set or a reset is generated by the slave mode controller, a TRGO pulse occurs. And in the latter case, the signal on TRGO is delayed compared to the actual reset. 001: Enable - The TIMx_CTRL1.CNTEN bit is used as the trigger output (TRGO). Sometimes you need to start multiple timers at the same time or enable slave timer for a period of time. The counter enable signal is set when TIMx_CTRL1.CNTEN bit is set or the trigger input in gated mode is high. When the counter enable signal is controlled by the trigger input, there is a delay on TRGO except if the master/slave mode is selected (see the description of the TIMx_SMCTRL.MSMD bit). 010: Update - The update event is selected as the trigger output (TRGO). For example, a master timer clock can be used as a slave timer prescaler. 011: Compare pulse - Triggers the output to send a positive pulse (TRGO) when the TIMx_STS.CC1ITF is to be set (even if it is already high), when a capture or a comparison succeeds. 100: Compare - OC1REF signal is used as the trigger output (TRGO). 101: Compare - OC2REF signal is used as the trigger output (TRGO). 110: Compare - OC3REF signal is used as the trigger output (TRGO). 111: Compare - OC4REF signal is used as the trigger output (TRGO).
3	CCDSEL	Capture/compare DMA selection 0: When a CCx event occurs, a DMA request for CCx is sent. 1: When an update event occurs, a DMA request for CCx is sent.
2:0	Reserved	Reserved, the reset value must be maintained

12.4.4 Slave Mode Control Register (TIMx_SMCTRL)

Offset address: 0x08

Reset value: 0x0000



Bit field	Name	Description
15	EXTP	External trigger polarity This bit is used to select whether the trigger operation is to use ETR or the inversion of ETR. 0: ETR active at high level or rising edge. 1: ETR active at low level or falling edge.
14	EXCEN	External clock enable This bit is used to enable external clock mode 2, and the counter is driven by any active edge on the ETRF signal in this mode.

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Bit field	Name	Description
		0: External clock mode 2 disable. 1: External clock mode 2 enable. *Note 1: When external clock mode 1 and external clock mode 2 are enabled at the same time, the input of the external clock is ETRF.* *Note 2: The following slave modes can be used simultaneously with external clock mode 2: reset mode, gated mode and trigger mode; However, TRGI cannot connect to ETRF (TIMx_SMCTRL.TSEL ≠ '111').* *Note 3: Setting the TIMx_SMCTRL.EXCEN bit has the same effect as selecting external clock mode 1 and connecting TRGI to ETRF (TIMx_SMCTRL.SMSEL = 111 and TIMx_SMCTRL.TSEL = 111).*
13:12	EXTPS[1:0]	External trigger prescaler The frequency of the external trigger signal ETRP must be at most 1/4 of TIMxCLK frequency. When a faster external clock is input, a prescaler can be used to reduce the frequency of ETRP. 00: Prescaler disable 01: ETRP frequency divided by 2 10: ETRP frequency divided by 4 11: ETRP frequency divided by 8
11:8	EXTF[3:0]	External trigger filter These bits are used to define the frequency at which the ETRP signal is sampled and the bandwidth of the ETRP digital filtering. In effect, the digital filter is an event counter that generates a validate output after consecutive N events are recorded. 0000: No filter, sampling at f_{DTS} 0001: $f_{SAMPLING} = f_{CK\_INT}$, N = 2 0010: $f_{SAMPLING} = f_{CK\_INT}$, N = 4 0011: $f_{SAMPLING} = f_{CK\_INT}$, N = 8 0100: $f_{SAMPLING} = f_{DTS}/2$, N = 6 0101: $f_{SAMPLING} = f_{DTS}/2$, N = 8 0110: $f_{SAMPLING} = f_{DTS}/4$, N = 6 0111: $f_{SAMPLING} = f_{DTS}/4$, N = 8 1000: $f_{SAMPLING} = f_{DTS}/8$, N = 6 1001: $f_{SAMPLING} = f_{DTS}/8$, N = 8 1010: $f_{SAMPLING} = f_{DTS}/16$, N = 5 1011: $f_{SAMPLING} = f_{DTS}/16$, N = 6 1100: $f_{SAMPLING} = f_{DTS}/16$, N = 8 1101: $f_{SAMPLING} = f_{DTS}/32$, N = 5 1110: $f_{SAMPLING} = f_{DTS}/32$, N = 6 1111: $f_{SAMPLING} = f_{DTS}/32$, N = 8
7	MSMD	Master/ Slave mode 0: No action 1: Events on the trigger input (TRGI) are delayed to allow a perfect synchronization between the current timer (via TRGO) and its slaves. This is useful when several timers are required to be synchronized to a single external event.

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Bit field	Name	Description
6:4	TSEL[2:0]	Trigger selection These 3 bits are used to select the trigger input of the synchronous counter. 000: Internal trigger 0 (ITR0) 100: TI1 edge detector (TI1F_ED) 001: Internal trigger 1 (ITR1) 101: Filtered timer input 1 (TI1FP1) 010: Internal trigger 2 (ITR2) 110: Filtered timer input 2 (TI2FP2) 011: Internal trigger 3 (ITR3) 111: External triggered Input (ETRF) For more details on ITRx, see Table 12-3 below. *Note: These bits must be changed only when not in use (e. g. TIMx_SMCTRL.SMSEL=000) to avoid false edge detection at the transition.*
3	Reserved	Reserved, the reset value must be maintained
2:0	SMSEL[2:0]	Slave mode selection When an external signal is selected, the active edge of the trigger signal (TRGI) is linked to the selected external input polarity (see input control register and control register description) 000: Disable slave mode. If TIMx_CTRL1.CNTEN = 1, the prescaler is driven directly by the internal clock. 001: Encoder mode 1. According to the level of TI2FP2, the counter up-counting or down-counting on the edge of TI1FP1. 010: Encoder mode 2. According to the level of TI1FP1, the counter up-counting or down-counting on the edge of TI2FP2. 011: Encoder mode 3. According to the input level of another signal, the counter up-counting or down-counting on the edges of TI2FP1 and TI2FP2. 100: Reset mode. On the rising edge of the selected trigger input (TRGI), the counter is reinitialized and the shadow register is updated. 101: Gated mode. When the trigger input (TRGI) is high, the clock of the counter is enabled. Once the trigger input becomes low, the counter stops counting, but is not reset. In this mode, the start and stop of the counter are controlled. 110: Trigger mode. When a rising edge occurs on the trigger input (TRGI), the counter is started but not reset. In this mode, only the start of the counter is controlled. 111: External clock mode 1. The counter is clocked by the rising edge of the selected trigger input (TRGI). *Note: Do not use gated mode if TI1F_ED is selected as the trigger input (TIMx_SMCTRL.TSEL=100). This is because TI1F_ED outputs a pulse for each TI1F transition, whereas gated mode checks the level of the triggered input.*

Table 12-3 TIMx internal trigger connection

Slave timer	ITR0 (TSEL = 000)	ITR1 (TSEL = 001)	ITR2 (TSEL = 010)	ITR3 (TSEL = 011)
TIM2	TIM1	TIM8	TIM3	TIM4
TIM3	TIM1	TIM2	TIM5	TIM4
TIM4	TIM1	TIM2	TIM3	TIM8
TIM5	TIM2	TIM3	TIM4	TIM8

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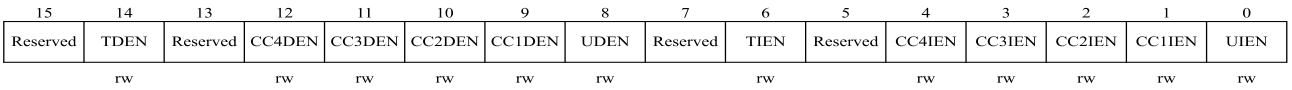
12.4.5 DMA/Interrupt Enable Registers (TIMx_DINTEN)

Offset address: 0x0C

Reset value: 0x0000



15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	TDEN	Reserved	CC4DEN	CC3DEN	CC2DEN	CC1DEN	UDEN	Reserved	TIEN	Reserved	CC4IEN	CC3IEN	CC2IEN	CC1IEN	UIEN
	rw		rw	rw	rw	rw	rw		rw		rw	rw	rw	rw	rw

Bit field	Name	Description
15	Reserved	Reserved, the reset value must be maintained
14	TDEN	Trigger DMA request enable 0: Disable trigger DMA request 1: Enable trigger DMA request
13	Reserved	Reserved, the reset value must be maintained
12	CC4DEN	Capture/Compare 4 DMA request enable 0: Disable capture/compare 4 DMA request 1: Enable capture/compare 4 DMA request
11	CC3DEN	Capture/Compare 3 DMA request enable 0: Disable capture/compare 3 DMA request 1: Enable capture/compare 3 DMA request
10	CC2DEN	Capture/Compare 2 DMA request enable 0: Disable capture/compare 2 DMA request 1: Enable capture/compare 2 DMA request
9	CC1DEN	Capture/Compare 1 DMA request enable 0: Disable capture/compare 1 DMA request 1: Enable capture/compare 1 DMA request
8	UDEN	Update DMA request enable 0: Disable update DMA request 1: Enable update DMA request
7	Reserved	Reserved, the reset value must be maintained
6	TIEN	Trigger interrupt enable 0: Disable trigger interrupt 1: Enable trigger interrupt
5	Reserved	Reserved, the reset value must be maintained
4	CC4IEN	Capture/Compare 4 interrupt enable 0: Disable capture/compare 4 interrupt 1: Enable capture/compare 4 interrupt
3	CC3IEN	Capture/Compare 3 interrupt enable 0: Disable capture/compare 3 interrupt 1: Enable capture/compare 3 interrupts
2	CC2IEN	Capture/Compare 2 interrupt enable 0: Disable capture/compare 2 interrupt

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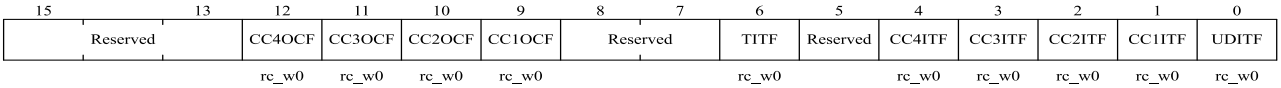
Bit field	Name	Description
		1: Enables capture/compare 2 interrupts
1	CC1IEN	Capture/Compare 1 interrupt enable 0: Disable capture/compare 1 interrupt 1: Enables capture/comparing 1 interrupt
0	UIEN	Update interrupt enable 0: Disable update interrupt 1: Enables update interrupt

12.4.6 Status Registers (TIMx_STS)

Offset address: 0x10

Reset value: 0x0000



Bit field	Name	Description
15:13	Reserved	Reserved, the reset value must be maintained
12	CC4OCF	Capture/Compare 4 overcapture flag See TIMx_STS.CC1OCF description.
11	CC3OCF	Capture/Compare 3 overcapture flag See TIMx_STS.CC1OCF description.
10	CC2OCF	Capture/Compare 2 overcapture flags See TIMx_STS.CC1OCF description.
9	CC1OCF	Capture/Compare 1 overcapture flag This bit is set by hardware only when the corresponding channel is configured in input capture mode. Cleared by software writing 0. 0: No overcapture occurred 1: TIMx_STS.CC1ITF was already set when the value of the counter has been captured in the TIMx_CCDAT1 register.
8:7	Reserved	Reserved, the reset value must be maintained
6	TITF	Trigger interrupt flag This bit is set by hardware when an active edge is detected on the TRGI input when the slave mode controller is in a mode other than gated. This bit is set by hardware when any edge in gated mode is detected. This bit is cleared by software. 0: No trigger event occurred 1: Trigger interrupt occurred
5	Reserved	Reserved, the reset value must be maintained
4	CC4ITF	Capture/Compare 4 interrupt flag See TIMx_STS.CC1ITF description.

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Bit field	Name	Description
3	CC3ITF	Capture/Compare 3 interrupt flag See TIMx_STS.CC1ITF description.
2	CC2ITF	Capture/Compare 2 interrupt flag See TIMx_STS.CC1ITF description.
1	CC1ITF	Capture/Compare 1 interrupt flag **When the corresponding channel of CC1 is in output mode:** Except in center-aligned mode, this bit is set by hardware when the counter value is the same as the compare value (see TIMx_CTRL1.CAMSEL bit description). This bit is cleared by software. 0: No match occurred. 1: The value of TIMx_CNT is the same as the value of TIMx_CCDAT1. When the value of TIMx_CCDAT1 is greater than the value of TIMx_AR, the TIMx_STS.CC1ITF bit will go high if the counter overflows (in up-counting and up/down-counting modes) and underflows in down-counting mode. **When the corresponding channel of CC1 is in input mode:** This bit is set by hardware when the capture event occurs. This bit is cleared by software or by reading TIMx_CCDAT1. 0: No input capture occurred. 1: Input capture occurred. Counter value has captured in the TIMx_CCDAT1. An edge with the same polarity as selected has been detected on IC1.
0	UDITF	Update interrupt flag This bit is set by hardware when an update event occurs under the following conditions: – When TIMx_CTRL1.UPDIS = 0, overflow or underflow (An update event is generated). – When TIMx_CTRL1.UPRS = 0, TIMx_CTRL1.UPDIS = 0, and set the TIMx_EVTGEN.UDGN bit by software to reinitialize the CNT. – When TIMx_CTRL1.UPRS = 0, TIMx_CTRL1.UPDIS = 0, and the counter CNT is reinitialized by the trigger event. (See TIMx_SMCTRL Register description) This bit is cleared by software. 0: No update event occurred 1: Update interrupt occurred

12.4.7 Event Generation Registers (TIMx_EVTGEN)

Offset address: 0x14

Reset values: 0 x0000

Bit field	Name	Description
15：7	Reserved	Reserved, the reset value must be maintained.

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Bit field	Name	Description
6	TGN	Trigger generation This bit can generate a trigger event when set by software. And at this time TIMx_STS.TITF = 1, if the corresponding interrupt and DMA are enabled, the corresponding interrupt and DMA will be generated. This bit is automatically cleared by hardware. 0: No action 1: Generated a trigger event
5	Reserved	Reserved, the reset value must be maintained
4	CC4GN	Capture/Compare 4 generation See TIMx_EVTGEN.CC1GN description.
3	CC3GN	Capture/Compare 3 generation See TIMx_EVTGEN.CC1GN description.
2	CC2GN	Capture/Compare 2 generation See TIMx_EVTGEN.CC1GN description.
1	CC1GN	Capture/Compare 1 generation This bit can generate a capture/compare event when set by software. This bit is automatically cleared by hardware. When the corresponding channel of CC1 is in output mode: The TIMx_STS.CC1ITF flag will be pulled high, if the corresponding interrupt and DMA are enabled, the corresponding interrupt and DMA will be generated. When the corresponding channel of CC1 is in input mode: TIMx_CCDAT1 will capture the current counter value, and the TIMx_STS.CC1ITF flag will be pulled high, if the corresponding interrupt and DMA are enabled, the corresponding interrupt and DMA will be generated. If The IMx_STS.CC1ITF is already pulled high, pull TIMx_STS.CC1OCF high. 0: No action 1: Generated a CC1 capture/compare event
0	UDGN	Update generation This bit can generate an update event when set by software. And at this time the counter will be reinitialized, the prescaler counter will be cleared, the counter will be cleared in center-aligned or up-counting mode, but take TIMx_AR in down-counting mode the value of the register. This bit is automatically cleared by hardware. 0: No action 1: Generated an update event

12.4.8 Capture/Compare Mode Register 1 (TIMx_CCMOD1)

Offset address: 0x18

Reset value: 0x0000

Channels can be used for input (capture mode) or output (compare mode), and the direction of the channel is defined by the corresponding CCxSEL bit. The other bits of the register act differently in input and output modes. OCx describes the function of a channel in output mode, ICx describes the function of a channel in input mode. Hence, please note that the same bit can have different meanings for output mode and for input mode.

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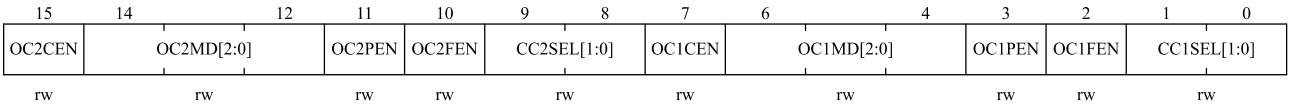
Output compare mode:



Bit field	Name	Description
15	OC2CEN	Output Compare 2 clear enable
14:12	OC2MD[2:0]	Output Compare 2 mode
11	OC2PEN	Output Compare 2 preload enable
10	OC2FEN	Output Compare 2 fast enable
9:8	CC2SEL[1:0]	Capture/compare 2 selection These bits are used to select the input/output and input mapping of the channel 00: CC2 channel is configured as output 01: CC2 channel is configured as input, IC2 is mapped on TI2 10: CC2 channel is configured as input, IC2 is mapped on TI1 11: CC2 channel is configured as input, IC2 is mapped on TRC. This mode is only active when the internal trigger input is selected by TIMx_SMCTRL.TSEL. *Note: CC2SEL is writable only when the channel is off (TIMx_CCEN.CC2EN = 0).*
7	OC1CEN	Output Compare 1 clear enable 0: OC1REF is not affected by ETRF input level 1: OC1REF is cleared immediately when the ETRF input level is detected as high
6:4	OC1MD[2:0]	Output Compare 1 mode These bits are used to manage the output reference signal OC1REF, which determines the values of OC1 and OC1N, and is valid at high levels, while the active levels of OC1 and OC1N depend on the TIMx_CCEN.CC1P and TIMx_CCEN.CC1NP bits. 000: Frozen. Comparison between TIMx_CCDAT1 register and counter TIMx_CNT has no effect on OC1REF signal. 001: Set channel 1 to the active level on match. When TIMx_CCDAT1 = TIMx_CNT, OC1REF signal will be forced high. 010: Set channel 1 as inactive level on match. When TIMx_CCDAT1 = TIMx_CNT, OC1REF signal will be forced low. 011: Toggle. When TIMx_CCDAT1 = TIMx_CNT, OC1REF signal will be toggled. 100: Force to inactive level. OC1REF signal is forced low. 101: Force to active level. OC1REF signal is forced high. 110: PWM mode 1 - In up-counting mode, if TIMx_CNT < TIMx_CCDAT1, OC1REF signal of channel 1 is high, otherwise it is low. In down-counting mode, if TIMx_CNT > TIMx_CCDAT1, OC1REF signal of channel 1 is low, otherwise it is high. 111: PWM mode 2 - In up-counting mode, if TIMx_CNT < TIMx_CCDAT1, OC1REF signal of channel 1 is low, otherwise it is high. In down-counting mode, if TIMx_CNT > TIMx_CCDAT1, OC1REF signal of channel 1 is high, otherwise it is low. *Note 1: In PWM mode 1 or PWM mode 2, the OC1REF level changes only when the comparison result changes or when the output compare mode is switched from frozen mode to PWM mode.*

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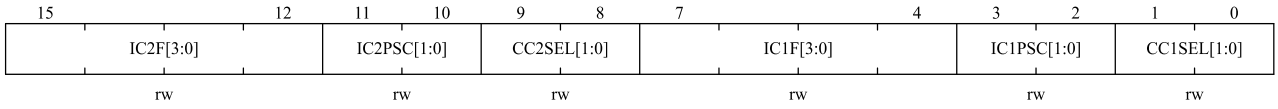
Bit field	Name	Description
3	OC1PEN	Output Compare 1 preload enable 0: Disable preload function of TIMx_CCDAT1 register. Supports write operations to TIMx_CCDAT1 register at any time, and the written value is effective immediately. 1: Enable preload function of TIMx_CCDAT1 register. Only read and write operations to preload registers. When an update event occurs, the value of TIMx_CCDAT1 is loaded into the active register. *Note 1: Only when TIMx_CTRL1.ONEPM = 1(In one-pulse mode), PWM mode can be used without verifying the preload register, otherwise no other behavior can be predicted.*
2	OC1FEN	Output Compare 1 fast enable This bit is used to speed up the response of the CC output to the trigger input event. 0: CC1 behaves normally depending on the counter and CCDAT1 values, even if the trigger is ON. The minimum delay for activating CC1 output when an edge occurs on the trigger input is 5 clock cycles. 1: An active edge of the trigger input acts like a comparison match on CC1 output. Therefore, OC is set to the comparison level regardless of the comparison result. The delay time for sampling the trigger input and activating the CC1 output is reduced to 3 clock cycles. OCxFEN only works if the channel is configured in PWM1 or PWM2 mode.
1：0	CC1SEL[1:0]	Capture/compare 1 selection These bits are used to select the input/output and input mapping of the channel 00: CC1 channel is configured as output 01: CC1 channel is configured as input, IC1 is mapped on TI1 10: CC1 channel is configured as input, IC1 is mapped on TI2 11: CC1 channels are configured as inputs and IC1 is mapped to TRC. This mode is only active when the internal trigger input is selected by TIMx_SMCTRL.TSEL. *Note: CC1SEL is writable only when the channel is off (TIMx_CCEN.CC1EN = 0).*

Input capture mode:



Bit field	Name	Description
15:12	IC2F[3:0]	Input Capture 2 Filter
11:10	IC2PSC[1:0]	Input Capture 2 Prescaler
9:8	CC2SEL[1:0]	Capture/Compare 2 selection These bits are used to select the input/output and input mapping of the channel 00: CC2 channel is configured as output 01: CC2 channel is configured as input, IC2 is mapped on TI2 10: CC2 channel is configured as input, IC2 is mapped on TI1 11: CC2 channel is configured as input, IC2 is mapped on TRC. This mode is only active when the internal trigger input is selected by TIMx_SMCTRL.TSEL. *Note: CC2SEL is writable only when the channel is off (TIMx_CCEN.CC2EN = 0).*

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Bit field	Name	Description
7:4	IC1F[3:0]	Input Capture 1 filter These bits are used to define sampling frequency of TI1 input and the length of digital filter. The digital filter is an event counter that generates an output transition after N events are recorded. 0000: No filter, sampling at f_{DTS} frequency 0001: $f_{SAMPLING} = f_{CK\_INT}$, N = 2 0010: $f_{SAMPLING} = f_{CK\_INT}$, N = 4 0011: $f_{SAMPLING} = f_{CK\_INT}$, N = 8 0100: $f_{SAMPLING} = f_{DTS}/2$, N = 6 0101: $f_{SAMPLING} = f_{DTS}/2$, N = 8 0110: $f_{SAMPLING} = f_{DTS}/4$, N = 6 0111: $f_{SAMPLING} = f_{DTS}/4$, N = 8 1000: $f_{SAMPLING} = f_{DTS}/8$, N = 6 1001: $f_{SAMPLING} = f_{DTS}/8$, N = 8 1010: $f_{SAMPLING} = f_{DTS}/16$, N = 5 1011: $f_{SAMPLING} = f_{DTS}/16$, N = 6 1100: $f_{SAMPLING} = f_{DTS}/16$, N = 8 1101: $f_{SAMPLING} = f_{DTS}/32$, N = 5 1110: $f_{SAMPLING} = f_{DTS}/32$, N = 6 1111: $f_{SAMPLING} = f_{DTS}/32$, N = 8
3:2	IC1PSC[1:0]	Input Capture 1 prescaler These bits are used to select the ratio of the prescaler for IC1 (CC1 input). When TIMx_CCEN.CC1EN = 0, the prescaler will be reset. 00: No prescaler, capture is done each time an edge is detected on the capture input 01: Capture is done once every 2 events 10: Capture is done once every 4 events 11: Capture is done once every 8 events
1:0	CC1SEL[1:0]	Capture/Compare 1 selection These bits are used to select the input/output and input mapping of the channel 00: CC1 channel is configured as output 01: CC1 channel is configured as input, IC1 is mapped on TI1 10: CC1 channel is configured as input, IC1 is mapped on TI2 11: CC1 channel is configured as input, IC1 is mapped to TRC. This mode is only active when the internal trigger input is selected by TIMx_SMCTRL.TSEL. *Note: CC1SEL is writable only when the channel is off (TIMx_CCEN.CC1EN = 0).*

12.4.9 Capture/Compare Mode Register 2 (TIMx_CCMOD2)

Offset address: 0x1C

Reset value: 0x0000

See the description of the CCMOD1 register above

Output comparison mode:

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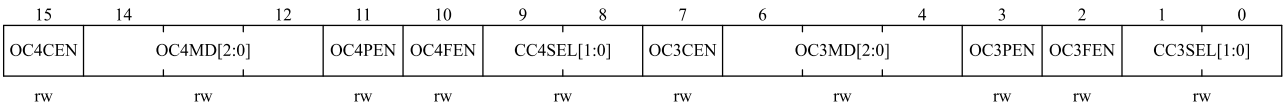
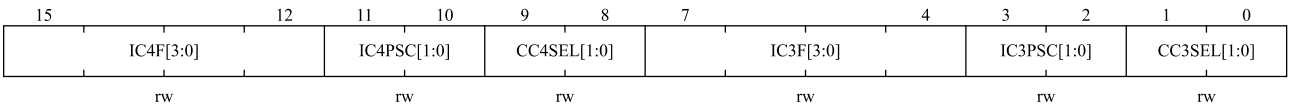


Bit field	Name	Description
15	OC4CEN	Output compare 4 clear enable
14:12	OC4MD[2:0]	Output compare 4 mode
11	OC4PEN	Output compare 4 preload enable
10	OC4FEN	Output compare 4 fast enable
9:8	CC4SEL[1:0]	Capture/Compare 4 selection These bits are used to select the input/output and input mapping of the channel 00: CC4 channel is configured as output 01: CC4 channel is configured as input, IC4 is mapped on TI4 10: CC4 channel is configured as input, IC4 is mapped on TI3 11: CC4 channel is configured as input, IC4 is mapped on TRC. This mode is only active when the internal trigger input is selected by TIMx_SMCTRL.TSEL. *Note: CC4SEL is writable only when the channel is off (TIMx_CCEN.CC4EN = 0).*
7	OC3CEN	Output compare 3 clear enable
6:4	OC3MD[2:0]	Output compare 3 mode
3	OC3PEN	Output compare 3 preload enable
2	OC3FEN	Output compare 3 fast enable
1:0	CC3SEL[1:0]	Capture/Compare 3 selection These bits are used to select the input/output and input mapping of the channel 00: CC3 channel is configured as output 01: CC3 channel is configured as input, IC3 is mapped to TI3 10: CC3 channel is configured as input, IC3 is mapped on TI4 11: CC3 channel is configured as input, IC3 is mapped to TRC. This mode is only active when the internal trigger input is selected by TIMx_SMCTRL.TSEL. *Note: CC3SEL is writable only when the channel is off (TIMx_CCEN.CC3EN = 0).*

Input capture mode:



Bit field	Name	Description
15:12	IC4F[3:0]	Input Capture 4 filter
11:10	IC4PSC[1:0]	Input Capture 4 Prescaler

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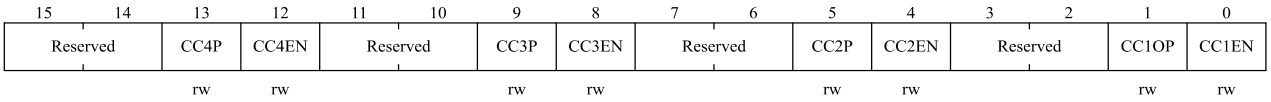
Bit field	Name	Description
9:8	CC4SEL[1:0]	Capture/Compare 4 selection These bits are used to select the input/output and input mapping of the channel 00: CC4 channel is configured as output 01: CC4 channel is configured as input, IC4 is mapped on TI4 10: CC4 channel is configured as input, IC4 is mapped on TI3 11: CC4 channel is configured as input, IC4 is mapped on TRC. This mode is only active when the internal trigger input is selected by TIMx_SMCTRL.TSEL. *Note: CC4SEL is writable only when the channel is off (TIMx_CCEN.CC4EN = 0).*
7:4	IC3F[3:0]	Input Capture 3 filter
3:2	IC3PSC[1:0]	Input Capture 3 Prescaler
1:0	CC3SEL[1:0]	Capture/compare 3 selection These bits are used to select the input/output and input mapping of the channel 00: CC3 channel is configured as output 01: CC3 channel is configured as input, IC3 is mapped to TI3 10: CC3 channel is configured as input, IC3 is mapped on TI4 11: CC3 channel is configured as input, IC3 is mapped to TRC. This mode is only active when the internal trigger input is selected by TIMx_SMCTRL.TSEL. *Note: CC3SEL is writable only when the channel is off (TIMx_CCEN.CC3EN = 0).*

12.4.10 Capture/Compare Enable Registers (TIMx_CCEN)

Offset address: 0x20

Reset value: 0x0000



Bit field	Name	Description
15:14	Reserved	Reserved, the reset value must be maintained.
13	CC4P	Capture/Compare 4 output polarity See TIMx_CCEN.CC1P description.
12	CC4EN	Capture/Compare 4 output enable See TIMx_CCEN.CC1EN description.
11:10	Reserved	Reserved, the reset value must be maintained
9	CC3P	Capture/Compare 3 output polarity See TIMx_CCEN.CC1P description.
8	CC3EN	Capture/Compare 3 output enable See TIMx_CCEN.CC1EN description.
7:6	Reserved	Reserved, the reset value must be maintained

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Bit field	Name	Description
5	CC2P	Capture/Compare 2 output polarity See TIMx_CCEN.CC1P description.
4	CC2EN	Capture/Compare 2 output enable See TIMx_CCEN.CC1EN description.
3:2	Reserved	Reserved, the reset value must be maintained
1	CC1P	Capture/Compare 1 output polarity When the corresponding channel of CC1 is in output mode: 0: OC1 active high 1: OC1 active low When the corresponding channel of CC1 is in input mode: At this time, this bit is used to select whether IC1 or the inverse signal of IC1 is used as the trigger or capture signal. 0: non-inverted: Capture action occurs when IC1 generates a rising edge. When used as external trigger, IC1 is non-inverted. 1: inverted: Capture action occurs when IC1 generates a falling edge. When used as external trigger, IC1 is inverted. *Note: If TIMx_BKDT.LCKCFG = 3 or 2, these bits cannot be modified.*
0	CC1EN	Capture/Compare 1 output enable When the corresponding channel of CC1 is in output mode: 0: Disable - Disable output OC1 signal. 1: Enable - Enable output OC1 signal. When the corresponding channel of CC1 is in input mode: At this time, this bit is used to disable/enable the capture function. 0: Disable capture 1: Enable capture

Table 12-4 Output control bits of standard OCx channel

CCxEN	OCx output status
0	Disable output (OCx=0)
1	OCx = OCxREF + polarity

Note: The state of external I/O pins connected to standard OCx channels depends on the OCx channel state and GPIO and AFIO registers.

12.4.11 Counters (TIMx_CNT)

Offset address: 0x24

Reset value: 0x0000

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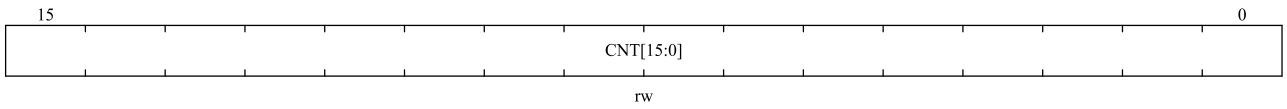
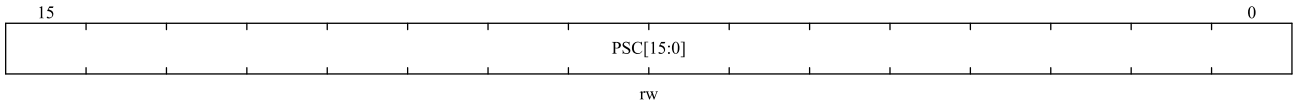


Bit field	Name	Description
15:0	CNT[15:0]	Counter value

12.4.12 Prescaler (TIMx_PSC)

Offset address: 0x28

Reset value: 0x0000

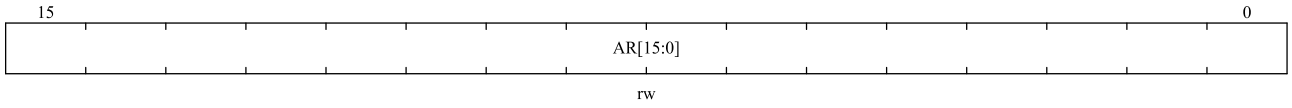


Bit field	Name	Description
15:0	PSC[15:0]	Prescaler value Counter clock $f_{CK\_CNT} = f_{CK\_PSC}/$ (PSC [15:0] +1). Each time an update event occurs, the PSC value is loaded into the active prescaler register.

12.4.13 Auto-reload Register (TIMx_AR)

Offset address: 0x2C

Reset values: 0xFFFF

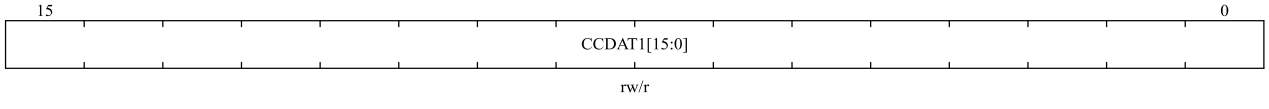


Bit field	Name	Description
15:0	AR[15:0]	Auto-reload value These bits define the value that will be loaded into the actual auto-reload register. See Section 12.3.1 for more details. When the TIMx_AR.AR [15:0] value is null, the counter does not work.

12.4.14 Capture/Compare Register 1 (TIMx_CCDAT1)

Offset address: 0x34

Reset value: 0x0000



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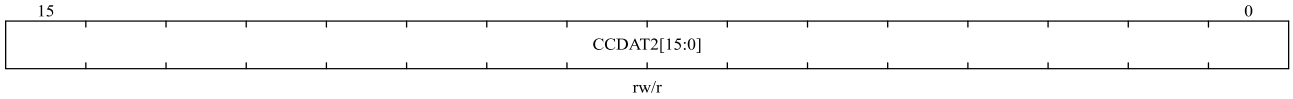
Bit field	Name	Description
15:0	CCDAT1[15:0]	Capture/Compare 1 value • CC1 channel is configured as output: CCDAT1 contains the value to be compared to the counter TIMx_CNT, signaling on the OC1 output. If the preload feature is not selected in TIMx_CCMOD1.OC1PEN bit, the written value is immediately transferred to the active register. Otherwise, this preloaded value is transferred to the active register only when an update event occurs. • CC1 channel is configured as input: CCDAT1 contains the counter value transferred by the last input capture 1 event (IC1). When configured as input mode, register CCDAT1 is only readable. When configured as output mode, register CCDAT1 is readable and writable.

12.4.15 Capture/Compare Register 2 (TIMx_CCDAT2)

Offset address: 0x38

Reset value: 0x0000

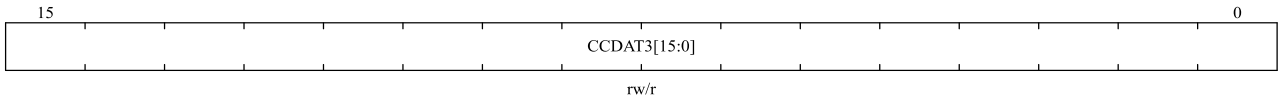


Bit field	Name	Description
15:0	CCDAT2[15:0]	Capture/Compare 2 values • CC2 channel is configured as output: CCDAT2 contains the value to be compared to the counter TIMx_CNT, signaling on the OC2 output. If the preload feature is not selected in TIMx_CCMOD1.OC2PEN bit, the written value is immediately transferred to the active register. Otherwise, this preloaded value is transferred to the active register only when an update event occurs. • CC2 channel is configured as input: CCDAT2 contains the counter value transferred by the last input capture 2 event (IC2). When configured as input mode, register CCDAT2 is only readable. When configured as output mode, register CCDAT2 is readable and writable.

12.4.16 Capture/Compare Register 3 (TIMx_CCDAT3)

Offset address: 0x3C

Reset value: 0x0000



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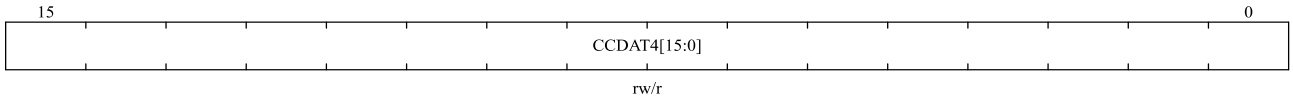
Bit field	Name	Description
15:0	CCDAT3[15:0]	Capture/Compare 3 value • CC3 channel is configured as output: CCDAT3 contains the value to be compared to the counter TIMx_CNT, signaling on the OC3 output. If the preload feature is not selected in TIMx_CCMOD2.OC3PEN bit, the written value is immediately transferred to the active register. Otherwise, this preloaded value is transferred to the active register only when an update event occurs. • CC3 channel is configured as input: CCDAT3 contains the counter value transferred by the last input capture 3 event (IC3). When configured as input mode, register CCDAT3 is only readable. When configured as output mode, register CCDAT3 is readable and writable.

12.4.17 Capture/Compare Register 4 (TIMx_CCDAT4)

Offset address: 0x40

Reset value: 0x0000

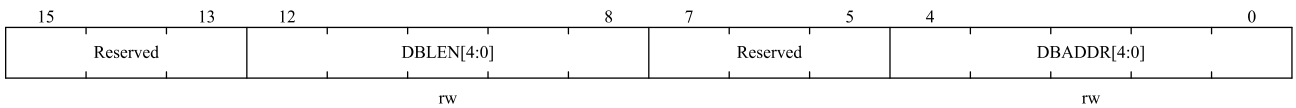


Bit field	Name	Description
15:0	CCDAT4[15:0]	Capture/Compare 4 value • CC4 channel is configured as output: CCDAT4 contains the value to be compared to the counter TIMx_CNT, signaling on the OC4 output. If the preload feature is not selected in TIMx_CCMOD2.OC4PEN bit, the written value is immediately transferred to the active register. Otherwise, this preloaded value is transferred to the active register only when an update event occurs. • CC4 channel is configured as input: CCDAT4 contains the counter value transferred by the last input capture 4 event (IC4). When configured as input mode, register CCDAT4 is only readable. When configured as output mode, register CCDAT4 is readable and writable.

12.4.18 DMA Control Register (TIMx_DCTRL)

Offset address: 0x48

Reset value: 0x0000



Bit field	Name	Description
15:13	Reserved	Reserved, the reset value must be maintained

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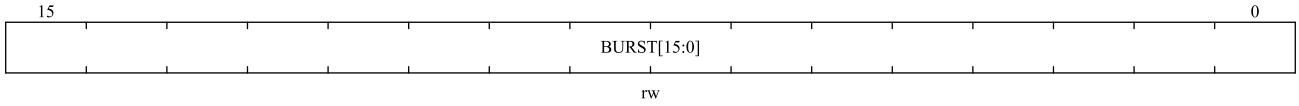
Bit field	Name	Description
12:8	DBLEN[4:0]	DMA Burst Length This bit field defines the number DMA will accesses (write/read) TIMx_DADDR register. 00000:1 time transfer 00001: 2 times transfers 00010: 3 times transfers … 10001: 18 times transfers
7:5	Reserved	Reserved, the reset value must be maintained.
4:0	DBADDR[4:0]	DMA Base Address This bit field defines the first address where the DMA accesses the TIMx_DADDR register. When access is done through the TIMx_DADDR first time, this bit-field specifies the address you just access. And then the second access to the TIMx_DADDR, you will access the address of "DMA Base Address + 4" 00000: TIMx_CTRL1, 00001: TIMx_CTRL2, 00010: TIMx_SMCTRL, … 01011: TIMx_AR， 01100: Reserved， 01101: TIMx_ CCDAT1， ..... 10000: TIMx_CCDAT4 10010：TIMx_DCTRL

12.4.19 DMA Transfer Buffer Register (TIMx_DADDR)

Offset address: 0x4C

Reset value: 0x0000



Bit field	Name	Description
15:0	BURST[15:0]	DMA access buffer. When a read or write operation is assigned to this register, the register located at the address range (DMA base address + DMA burst length × 4) will be accessed. DMA base address = The address of TIM_CTRL1 + TIMx_DCTRL. DBADDR * 4； DMA burst len = TIMx_DCTRL.DBLEN + 1.

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Bit field	Name	Description
		Example: If TIMx_DCTRL.DBLEN = 0x3(4 transfers), TIMx_DCTRL.DBADDR = 0xD (TIMx_CCDAT1), DMA data length = half word, DMA memory address = buffer address in SRAM, DMA peripheral address = TIMx_DADDR address. When an event occurs, TIMx will send requests to the DMA, and transfer data 4 times. For the first time, DMA access to the TIMx_ DADDR register will be mapped to access TIMx_CCDAT1 register; For the second time, DMA access to the TIMx_ DADDR register will be mapped to access TIMx_CCDAT2 register; … … For the fourth time, DMA access to the TIMx_ DADDR register will be mapped to access TIMx_CCDAT4 register;

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13 Basic Timers (TIM6 and TIM7)

13.1 Introduction

Basic timers TIM6 and TIM7 each contain a 16-bit auto-reload counter.

These two timers are independent of each other and do not share any resources.

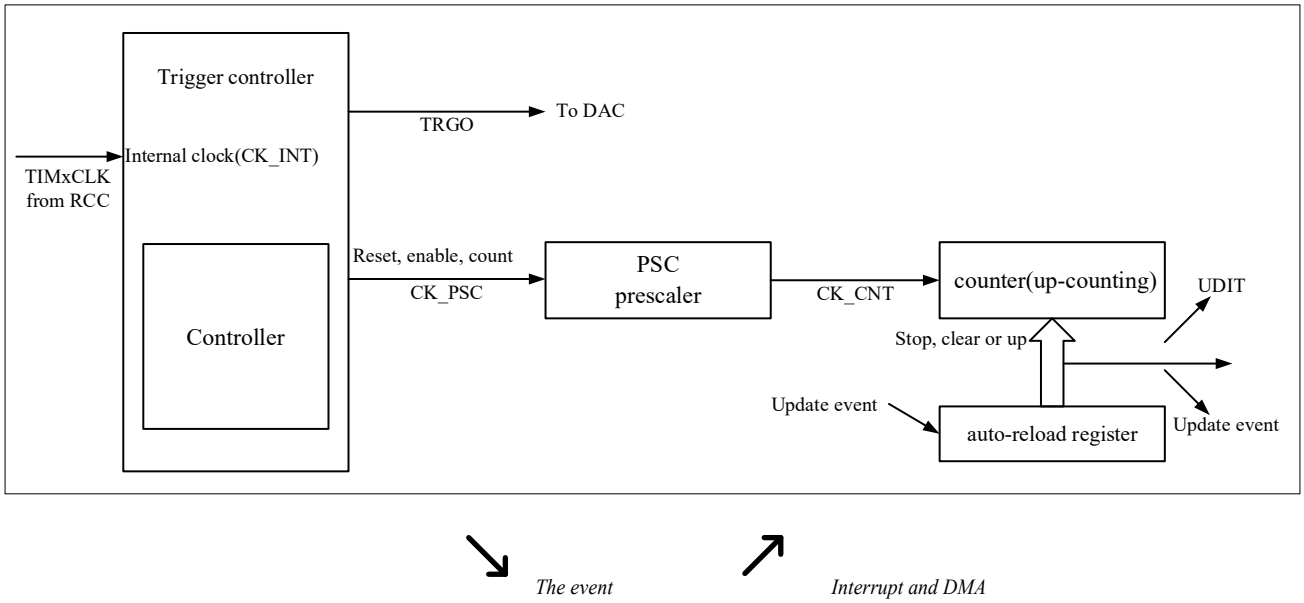
The basic timer can provide a time reference for general purpose timers.

The basic timer is directly connected to the DAC inside the chip and drives the DAC directly through the trigger output.

13.2 Main Features

- 16-bit auto-reload up-counting counters.
- 16-bit programmable prescaler. (The frequency division factor can be configured with any value between 1 and 65536)
- Synchronization circuit for triggering DAC
- The events that generate the interrupt/DMA are as follows:
  - Update event

Figure 13-1 Block diagram of TIMx（x = 6 and 7）



13.3 Basic Timers Description

13.3.1 Time-base Unit

The time-base unit mainly includes: prescaler, counter and auto-reload. When the time base unit is working, the software can read and write the corresponding registers (TIMx_PSC, TIMx_CNT and TIMx_AR) at any time.

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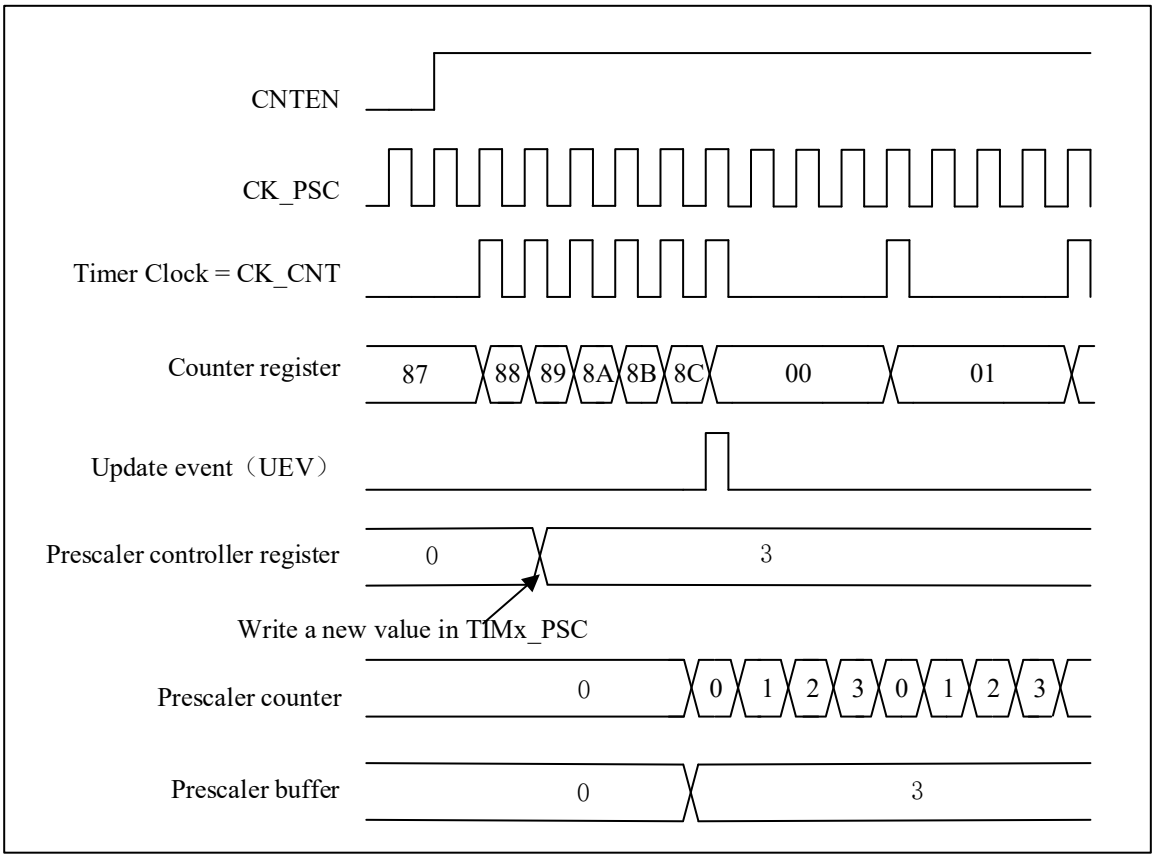
Depending on the setting of the auto-reload preload enable bit (TIMx_CTRL1.ARPEN), the value of the preload register is transferred to the shadow register immediately or at each update event UEV. An update event is generated when the counter reaches the overflow condition and it can be generated by software when TIMx_CTRL1.UPDIS=0. The counter CK_CNT is valid only when the TIMx_CTRL1.CNTEN bit is set. The counter starts counting one clock cycle after the TIMx_CTRL1.CNTEN bit is set.

13.3.1.1 Prescaler description

The TIMx_PSC register consists of a 16-bit counter that can be used to divide the counter clock frequency by any factor between 1 and 65536. It can be changed on the fly as it is buffered. The prescaler value is only taken into account at the next update event.

Figure 13-2 Counter timing diagram with prescaler division change from 1 to 4



13.3.2 Counter Mode

13.3.2.1 Up-counting mode

In up-counting mode, the counter will count from 0 to the value of the register TIMx_AR, then it resets to 0. And a counter overflow event is generated.

If the TIMx_CTRL1.UPRS bit (select update request) and the TIMx_EVTGEN.UDGN bit are set, an update event (UEV) will generate, and TIMx_STS.UDITF will not be set by hardware. Therefore, no update interrupts or update DMA requests are generated. This setting is used in scenarios where you want to clear the counter but do not want to generate an update interrupt.

Depending on the update request source is configured in TIMx_CTRL1.UPRS, When an update event occurs,

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TIMx_STS.UDITF is set, all registers are updated:

- Update auto-reload shadow registers with preload value(TIMx_AR), when TIMx_CTRL1.ARPEN = 1.
- The prescaler shadow register is reloaded with the preload value(TIMx_PSC)

To avoid updating the shadow registers when new values are written to the preload registers, you can disable the update by setting TIMx_CTRL1.UPDIS=1.

When an update event occurs, the counter will still be cleared and the prescaler counter will also be set to 0 (but the prescaler value will remain unchanged).

The figure below shows some examples of the counter behavior and the update flags for different division factors in the up-counting mode.

Figure 13-3 Timing diagram of up-counting. The internal clock divider factor = 2/N

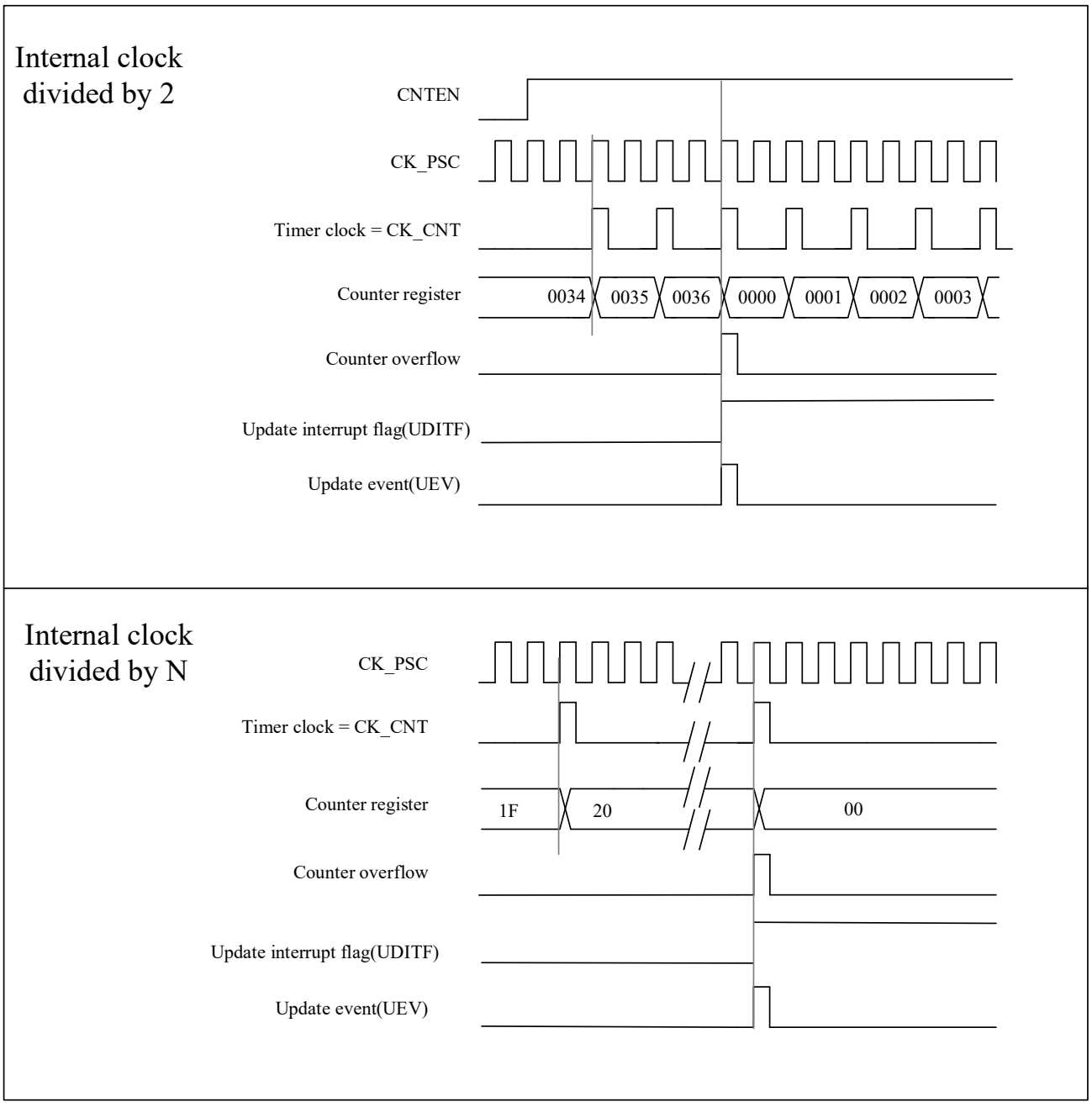

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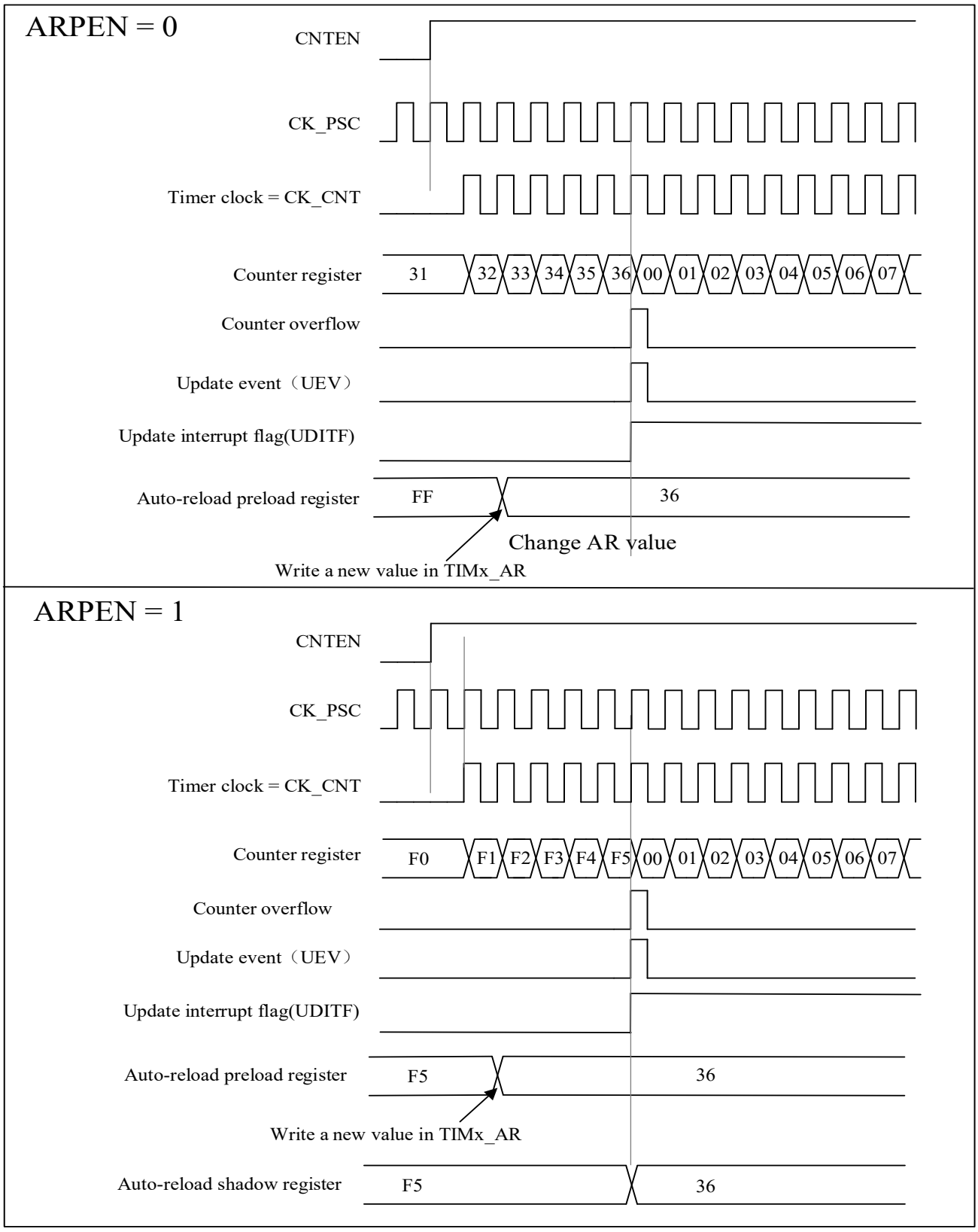
Figure 13-4 Timing diagram of the up-counting, update event when ARPEN=0/1



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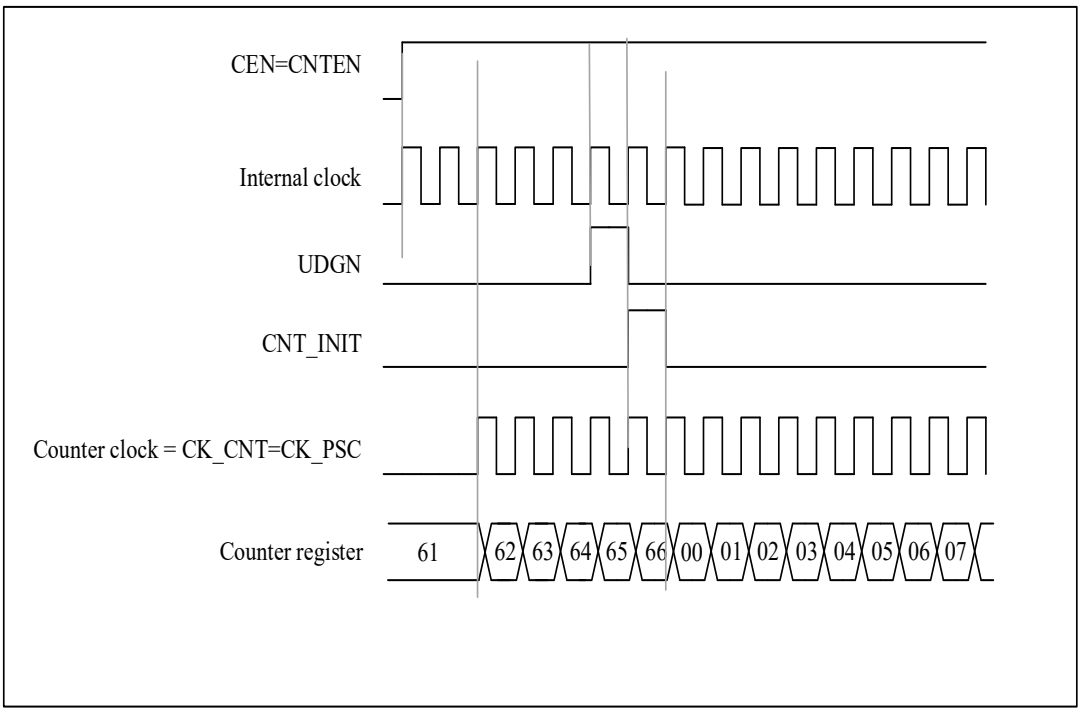
13.3.3 Clock Selection

- The internal clock of timers ： CK_INT

13.3.3.1 Internal clock source (CK_INT)

It is provided that the TIMx_CTRL1.CNTEN bit is written as' 1 ' by software, the clock source of the prescaler is provided by the internal clock CK_INT.

Figure 13-5 Control circuit in normal mode, internal clock divided by 1



13.3.4 Debug Mode

When the microcontroller is in debug mode (the Cortex-M4 core halted), depending on the DBG_CTRL.TIMx_STOP configuration in the DBG module, the TIMx counter can either continue to work normally or stop. For more details, see 29.4.3

13.4 TIMx Register Description(x = 6 and 7)

For abbreviations used in registers, see section 1.1.

These peripheral registers can be operated as half word (16-bits) or one word (32-bits).

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13.4.1 Register Overview

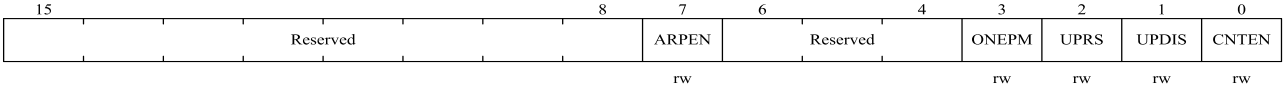
Table 13-1 Register overview

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
000h	TIMx_CTRL1	Reserved																								ARPEN	Reserved			ONEPM	UPRS	UPDIS	CNTEN
	Reset Value																									0				0	0	0	0
004h	TIMx_CTRL2	Reserved																									MMSEL[2:0]			Reserved				
	Reset Value																										0	0	0				
008h	Reserved																																
00Ch	TIMx_DINTEN	Reserved																							UDEN	Reserved							UIEN
	Reset Value																								0								0
010h	TIMx_STS	Reserved																															UDITF
	Reset Value																																0
014h	TIMx_EVTGEN	Reserved																															UDGN
	Reset Value																																0
018h	Reserved																																
01Ch	Reserved																																
020h	Reserved																																
024h	TIMx_CNT	Reserved																CNT[15:0]															
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
028h	TIMx_PSC	Reserved																PSC[15:0]															
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
02Ch	TIMx_AR	Reserved																AR[15:0]															
	Reset Value																	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

13.4.2 Control Register 1 (TIMx_CTRL1)

Offset address: 0x00

Reset value: 0x0000



Bit field	Name	Description
15:8	Reserved	Reserved, the reset value must be maintained

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Bit field	Name	Description
7	ARPEN	ARPEN: Auto-reload preload enable 0: Shadow register disable for TIMx_AR register 1: Shadow register enable for TIMx_AR register
6:4	Reserved	Reserved, the reset value must be maintained
3	ONEPM	One-pulse mode 0: Disable one-pulse mode, the counter counts are not affected when an update event occurs. 1: Enable one-pulse mode, the counter stops counting when the next update event occurs (clearing TIMx_CTRL1.CNTEN bit)
2	UPRS	Update request source This bit is used to select the UEV event sources by software. 0: If update interrupt or DMA request is enabled, any of the following events will generate an update interrupt or DMA request: – Counter overflow – The TIMx_EVTGEN.UDGN bit is set 1: If update interrupt or DMA request is enabled, only counter overflow will generate update interrupt or DMA request
1	UPDIS	Update disable This bit is used to enable/disable the Update event (UEV) events generation by software. 0: Enable UEV. UEV will be generated if one of following condition been fulfilled: – Counter overflow – The TIMx_EVTGEN.UDGN bit is set Shadow registers will update with preload value. 1: UEV disabled. No update event is generated, and the shadow registers (AR, PSC) keep their values. If the TIMx_EVTGEN.UDGN bit is set, the counter and prescaler are reinitialized.
0	CNTEN	Counter Enable 0: Disable counter 1: Enable counter

13.4.3 Control Register 2 (TIMx_CTRL2)

Offset address：0x04

Reset value：0x0000

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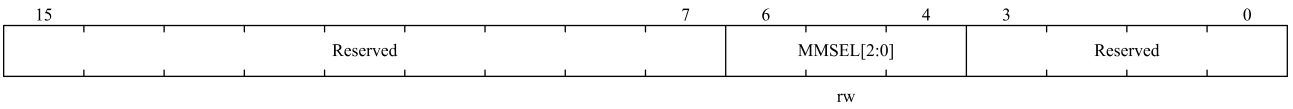
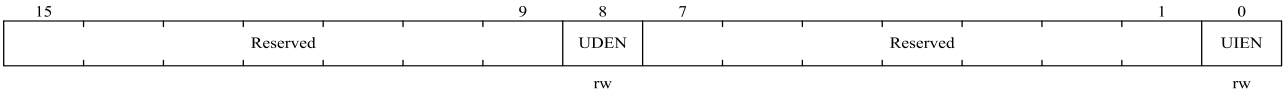


Bit field	Name	Description
15:7	Reserved	Reserved, the reset value must be maintained
6:4	MMSEL[2:0]	Master Mode Selection These 3 bits (TIMx_CTRL2. MMSEL [2:0]) are used to select the synchronization information (TRGO) sent to the slave timer in the master mode. Possible combinations are as follows: 000: Reset –When the TIMx_EVTGEN.UDGN is set or a reset is generated by the slave mode controller, a TRGO pulse occurs. And in the latter case, the signal on TRGO is delayed compared to the actual reset. 001: Enable - The TIMx_CTRL1.CNTEN bit is used as the trigger output (TRGO). Sometimes you need to start multiple timers at the same time or enable slave timer for a period of time. The counter enable signal is set when TIMx_CTRL1.CNTEN bit is set or the trigger input in gated mode is high. 010: Update - The update event is selected as the trigger output (TRGO). For example, a master timer clock can be used as a slave timer prescaler. 011: Compare pulse - Triggers the output to send a positive pulse (TRGO) when the TIMx_STS.CC1ITF is to be set (even if it is already high), when a capture or a comparison succeeds.
15：1	Reserved	Reserved, the reset value must be maintained.

13.4.4 DMA/Interrupt Enable Registers (TIMx_DINTEN)

Offset address: 0x0C

Reset value: 0x0000



Bit field	Name	Description
15:9	Reserved	Reserved, the reset value must be maintained
8	UDEN	Update DMA Request enable 0: Disable update DMA request 1: Enable update DMA request
7:1	Reserved	Reserved, the reset value must be maintained

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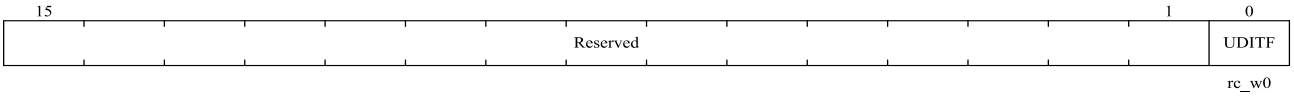
Bit field	Name	Description
0	UIEN	Update interrupt enable 0: Disable update interrupt 1: Enable update interrupt

13.4.5 Status Registers (TIMx_STS)

Offset address: 0x10

Reset value: 0x0000

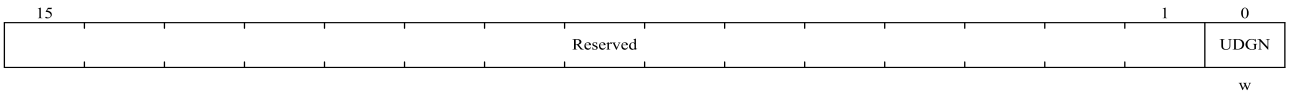


Bit field	Name	Description
15:1	Reserved	Reserved, the reset value must be maintained
0	UDITF	Update interrupt flag This bit is set by hardware when an update event occurs under the following conditions: – When TIMx_CTRL1.UPDIS = 0, and counter value overflow. – When TIMx_CTRL1.UPRS = 0, TIMx_CTRL1.UPDIS = 0, and set the TIMx_EVTGEN.UDGN bit by software to reinitialize the CNT. This bit is cleared by software. 0: No update event occurred 1: Update interrupt occurred

13.4.6 Event Generation Registers (TIMx_EVTGEN)

Offset address: 0x14

Reset values: 0 x0000



Bit field	Name	Description
15：1	Reserved	Reserved, the reset value must be maintained.
0	UDGN	UDGN: Update generation

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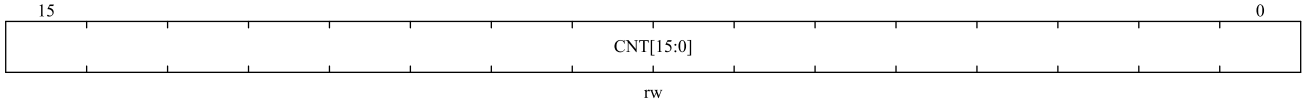
Bit field	Name	Description
		Software can set this bit to update configuration register value and hardware will clear it automatically. 0: No effect. 1: Timer counter will restart and all shadow register will be updated. It will restart prescaler counter also.

13.4.7 Counter (TIMx_CNT)

Offset address: 0x24

Reset value: 0x0000

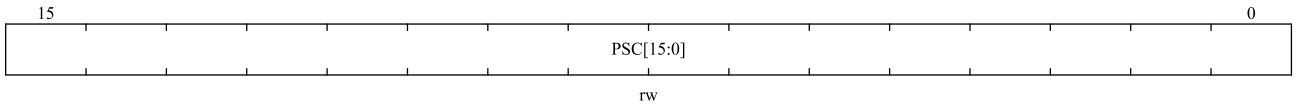


Bit field	Name	Description
15:0	CNT[15:0]	Counter value

13.4.8 Prescaler (TIMx_PSC)

Offset address: 0x28

Reset value: 0x0000

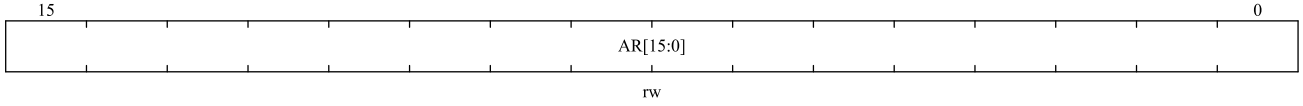


Bit field	Name	Description
15:0	PSC[15:0]	Prescaler value PSC register value will be updated to prescaler register at update event. Counter clock frequency is input clock frequency divide PSC + 1.

13.4.9 Automatic reload register (TIMx_AR)

Offset address: 0x2C

Reset values: 0xFFFF



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Bit field	Name	Description
15:0	AR[15:0]	Auto-reload value These bits define the value that will be loaded into the actual auto-reload register. See 13.3.1 for more details. When the TIMx_AR.AR [15:0] value is null, the counter does not work.

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14 Real-time Clock (RTC)

14.1 Description

- The real-time clock (RTC) is an independent BCD timer/counter.
- Daylight saving time compensation supported by software.
- A periodic automatic programmable wakeup timer.
- Two 32-bit registers contain the seconds, minutes, hours, day (day of week), date (day of month), month, and year.
- Independent 32-bit register contain sub-seconds value.
- Two programmable alarms.
- Two 32-bit registers contain two programmable alarms seconds, minutes, hours, day (day of week), and date (day of month).
- Two 32-bit registers contain two programmable alarms sub-seconds.
- Digital calibration function.
- Time-Stamp function.
- After Backup domain reset, all RTC registers are protected against possible parasitic write accesses.
- Multiple Wakeup sources of Interrupt/Event. These include Alarm A, Alarm B, Wakeup Timer, Time-Stamp.
- After RTC is enabled by the RCC register and voltage remains in the operating range, RTC will not stop timing in any mode (include RUN mode, SLEEP mode, STOP0 mode, STOP2 mode and STANDBY mode).
- RTC provides a variety of ways to wakeup from all low-power modes (SLEEP mode, STOP0 mode, STOP2 mode and STANDBY mode .

14.1.1 Specification

Table 14-1 RTC feature support

Main function	Description
Clock	RTC clock can be selected from LSI, LSE and HSE, which are 40KHz, 32.768KHz and HSE / 128 respectively
Reset	The APB interface is reset by the system. Some register reset from RTC module is synchronized with APB reset. RTC core is reset by backup domain reset.
Calendar	Calendar consists of sub second, second, minute, hour (12 or 24 format), day (day of the week), date, month and year. These data are stored in the shadow register of APB module.
Wakeup Timer	Output “RTC_OUT” can be configured to send wakeup events to GPIO. At the same time, it also can be configured as an interrupt/event to wake up the system from SLEEP, STOP0 ,STOP2 modes.

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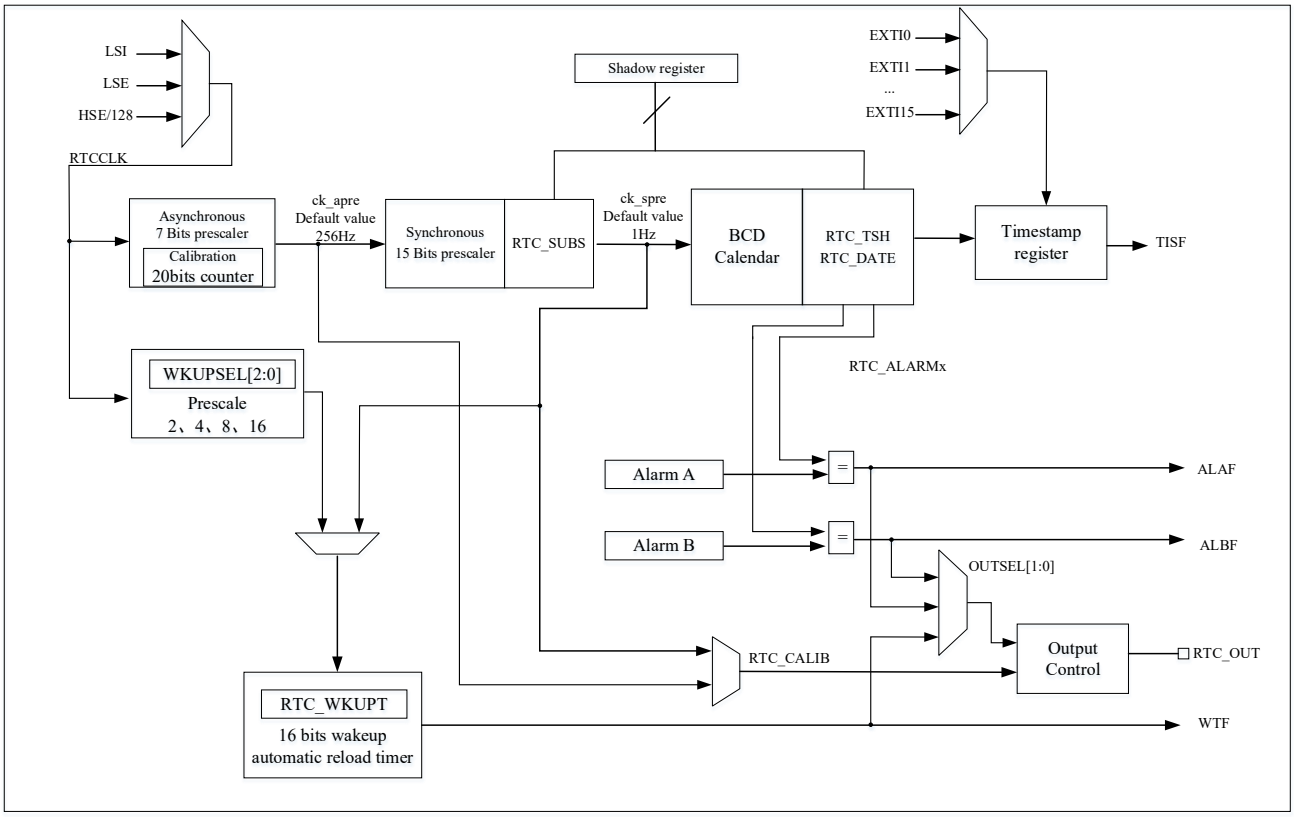
Main function	Description
Alarm	Programmable alarm clock and interrupt function. The alarm can be triggered by any combination of the calendar fields. When the alarm event occurs the alarm flag can be sent to GPIO through "RTC_OUT", and it also can be used to wake up the CPU or exit from the low power status such as SLEEP, STOP0, STOP2 and STANDBY modes.
Timestamp	Time-stamp function for GPIO event saving.
Interrupts/events	Alarm A/Alarm B interrupt/event Wakeup interrupt/event Timestamp interrupt/event

14.2 RTC function description

14.2.1 RTC block diagram

Figure 14-1 RTC Block Diagram



RTC includes the following functions:

- Alarm A and Alarm B event/interrupt
- Timestamp event/interrupt
- RTC output functions
  - 256 Hz or 1Hz clock output (LSE frequency is 32.768 kHz).
  - Alarm clock output (polarity configurable), Alarm A and Alarm B are optional.

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  - Auto wakeup output (polarity configurable).
- RTC input functions:
  - Timestamp event detection
- Control PC13 by configuring output register:
  - Set RTC_OPT.TYPE bit to configure open-drain/push-pull output of PC13

14.2.2 GPIOs of RTC

Timestamp input come from IOM (mapped to PC13) or EXTI module, if EXTI module is needed to start, please refer to the timestamp trigger source selection register (EXTI_TS_SEL) for details.

RTC_OUT (Alarm, Wakeup event or calibration output (256Hz or 1Hz)) is mapped to PC13. Regardless of the PC13 GPIO configuration, the PC13 pin configuration is controlled by the RTC as an output.

14.2.3 RTC register write protection

PWR_CTRL.DBKP bit (see the Power Control section) is cleared in default, so the PWR_CTRL.DBKP bit must set to "1" to enable write access to the RTC register. Once the backup domain is reset, all write protection RTC registers are write protected. All write protection RTC registers require the following steps to unlock write protection:

- Write "0xCA" into RTC_WRP register.
- Write "0x53" into RTC_WRP register.

The unlocking mechanism only checks the write operation to the RTC_WRP register. During or before and after the unlocking process, the write operation to other registers does not affect the unlocking result.

14.2.4 RTC clock and prescaler

RTC clock source:

- LSE clock
- LSI clock
- HSE/128 clock

For the purpose of reduction of power consumption, the prescaler is divided into 2 programmable prescalers, they are asynchronous prescaler and synchronous prescaler. If both prescaler are used, it is recommended that the value of the asynchronous divider be as large as possible.

- A 7-bit asynchronous prescaler which is given by RTC_PRE.DIVA[6:0] bits
- A 15-bit synchronous prescaler which is given by RTC_PRE.DIVS[14:0] bits

The formula for f_{ck_apre} and f_{ck_spre} are given below:

$$f_{ck\_apre} = \frac{f_{RTCCLK}}{RTC\_PRE.DIVA[6:0]+1}$$

$$f_{ck\_spre} = \frac{f_{RTCCLK}}{(RTC\_PRE.DIVS[14:0]+1)*(RTC\_PRE.DIVA[6:0]+1)}$$

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The ck_apre clock is used to driven RTC_SUBS sub-second down counter. When it reaches 0, reload RTC_SUBS with the value of RTC_PRE.DIVS[14:0].

14.2.5 RTC calendar

There are three shadow registers, they are RTC_DATE, RTC_TSH and RTC_SUBS. The RTC time and date registers can be accessed through the shadow registers. It is also possible to access them directly to avoid the synchronization waiting time. The three shadow registers are as follow:

- RTC_DATE: set and read date
- RTC_TSH: set and read time
- RTC_SUBS: read sub-second

After every two RTCCLK cycles, the current calendar value is copied to the shadow register, and RTC_INITSTS.RSYF bit is set to 1. This process is not performed in low power (stop & standby) modes. While exiting these modes, the shadow register updates the values after 2 RTCCLK cycles.

By default, when user try to access the calendar register, it accesses the contents of the shadow register instead. User can access the calendar register directly by setting the RTC_CTRL.BYPS bit.

When RTC_CTRL.BYPS=0, calendar values are from shadow registers, when reading RTC_SUBS, RTC_TSH or RTC_DATE register, it is necessary to make ensure the frequency of APB1 clock (f_{APB1}) is at least 7 times the frequency of RTC clock (f_{RTCCLK}), and APB1 clock frequency lower than RTC clock frequency is not allowed in any case. System reset will reset shadow registers.

14.2.6 Calendar initialization and configuration

The value of prescaler and calendar can be initialized by the following steps:

- Enter initialization mode by setting “1” to RTC_INITSTS.INITM bit, then wait for RTC_INITSTS.INITF flag to be set 1.
- Set RTC_PRE.DIVS[14:0] and RTC_PRE.DIVA[6:0] value.
- Write the initial calendar values include time and date into the shadow registers (RTC_TSH and RTC_DATE) and configure the time format (12 or 24 hours) by the RTC_CTRL.HFMT bit.
- Exit initialization mode by clearing the RTC_INITSTS.INITM bit.

The values of calendar counter will automatically loaded from shadow registers after 4 RTCCLK clock cycles, then the calendar counter restarts.

14.2.7 Calendar reading

1. Reading calendar value when RTC_CTRL.BYPS=0

Calendar value is read from shadow registers if RTC_CTRL.BYPS=0. In order to read RTC calendar registers (RTC_SUBS, RTC_TSH and RTC_DATE) correctly, APB1 clock frequency must be set equal to or greater than 7 times of RTC clock frequency. In any case, APB1 clock frequency must not be less than RTC clock frequency.

If APB1 clock frequency is not equal to or greater than 7 times of RTC clock frequency, refer to the following process

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to read calendar value.

- Read the data of RTC_SUBS, RTC_TSH and RTC_DATE twice.
- Compare the data read twice, if they are equal, the read data can be considered correct; if they are not equal, read the data for the third time.
- The third time read data can be considered correct.

Shadow registers (RTC_SUBS, RTC_TSH and RTC_DATE) are updated every two RTCCLK cycles. If user want to read calendar value in a short time(less than two RTCCLK cycles), RTC_INITSTS.RSYF bit must be cleared by software after the first time read.

In some cases, it is necessary to wait until RTC_INITSTS.RSYF bit is set 1 before read calendar value.

- After waking up from the low power modes (STOP mode, STANDBY mode), clear RTC_INITSTS.RSYF bit, then wait RTC_INITSTS.RSYF bit is set again.
- System reset.
- Calendar complete initialization.
- Calendar complete synchronization.

2. Reading calendar value when RTC_CTRL.BYPS=1

Reading the calendar value directly from the calendar counter if RTC_CTRL.BYPS=1. The advantage of this configuration is that read calendar value without delay after wakeup from the low power mode, the disadvantage is that these data of RTC_SUBS, RTC_TSH and RTC_DATE may not be at a time.

To ensure the correctness of read calendar value, it is necessary to read RTC_SUBS, RTC_TSH and RTC_DATE twice, then compare the data read twice, if they are equal, the read data can be considered correct;

14.2.8 Calibration clock output

When RTC_CTRL.COEN set to 1, PC13 pin will output calibration clock. If RTC_CTRL.CALOSEL=0 and RTC_PRE.DIVA[6:0] = 0x7F, the RTC_CALIB frequency results is f_{RTCCLK}/RTC_PRE.DIVA[6:0]. This is equivalent to a calibration output of 256 Hz when the RTCCLK frequency is 32.768 kHz. The rising edge is recommended for there is slight jitter on the falling edge.

When RTC_CTRL.CALOSEL=1 and "RTC_PRE.DIVS[14:0]+1" is a non-zero integer multiple of 256, the RTC_CALIB frequency is given by the formula f_{RTCCLK}/(256 * (DIVA+1)). This is equivalent to 1Hz calibration output when the RTCCLK frequency is 32.768 kHz and RTC_PRE.DIVA[6:0] = 0x7F.

Note: When the RTC_CALIB or RTC_ALARM output is selected, the RTC_OUT pin (PC13) is automatically configured as output.

14.2.9 Programmable alarms

RTC has 2 programmable alarms: Alarm A and Alarm B.

RTC alarm can be enabled or disabled by RTC_CTRL.ALxEN bit. If the alarm value match the calendar values, the RTC_INITSTS.ALxF flag will be set 1. Each calendar field can be selected to trigger alarm interrupt if RTC_CTRL.ALxIEN bit is enabled.

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Alarm output: Alarm A or Alarm B can be mapped to RTC_ALxRM output when RTC_CTRL.OUTSEL[1:0] is selected, and output polarity can be configured by RTC_CTRL.OPOL bit.

Note: If the seconds field is selected (RTC_ALARMx.MASK1 bit reset), RTC_PRE.DIVS[14:0] must be larger than 3 to ensure correct operation.

14.2.10 Alarm configuration

Alarm A and Alarm B should be configured in the following below:

- Disable Alarm A/Alarm B by clearing RTC_CTRL.ALAEN/RTC_CTRL.ALBEN bit.
- Configure the Alarm x registers (RTC_ALRMxSS/RTC_ALARMx)
- Enable Alarm A/Alarm B interrupt by set RTC_CTRL.ALAIEN/RTC_CTRL.ALBIEN bit(this step can be selected as needed)
- Enable Alarm A/Alarm B by setting RTC_CTRL.ALAEN/RTC_CTRL.ALBEN bit.

14.2.11 Alarm output

When RTC_CTRL.OUTSEL[1:0] !=0, RTC_ALARM alternate function output is enable. There are Alarm A output, Alarm B output and Wakeup output to choose by the value of RTC_CTRL.OUTSEL[1:0] bits.

RTC_CTRL.OPOL bit control the polarity of the Alarm A, Alarm B or Wakeup output.

RTC_OPT.TYPE bit control the RTC_ALARM pin to output open drain or output pull-up.

When RTC_CALIB or RTC_ALARM output is selected, the RTC_OUT pin (PC13) is automatically configured as output.

14.2.12 Periodic automatic wakeup

A 16-bit programmable auto-load down counter can generate periodic wakeup flag if reaches 0. It is also can be extend the range of wakeup timer to 17 bits. Periodic automatic wakeup can be enabled by setting RTC_CTRL.WTEN.

There are two wake-up input clock sources can be selected:

- RTC clock (RTCCLK) divided by 2/ 4/8/16.

  Assume RTCCLK comes from LSE (32.768KHz), wake-up interrupt period can be configured range from 122us to 32s under the resolution down to 61us.

- Internal clock ck_spre.
  - Assume ck_spre frequency is 1Hz, the available wake-up time range from 2s to 18h, and the resolution is 1 second.
  - When RTC_CTRL.WKUPSEL [2:0] = 10x, the period is range from 2s to 18h.

After RTC_CTRL.WTEN bit is set to 1, the down counter is running and when it reaches 0, RTC_INITSTS.WTF will be set and the device can exit from low power mode(except Standby mode) when the periodic wakeup interrupt is enabled by setting the RTC_CTRL.WTIEN bit.

Periodic wakeup output: periodic wakeup can be mapped to RTC_ALxRM output when RTC_CTRL.OUTSEL[1:0]

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is selected, the RTC_OUT pin(PC13) is automatically configured as output, and output polarity can be configured by RTC_CTRL.OPOL bit.

14.2.13 Wakeup timer configuration

The wakeup timer automatic reload value should be configured in the following below:

- Disable wakeup timer by clearing RTC_CTRL.WTEN bit, then wait for RTC_INITSTS.WTWF flag to be set 1.
- Select wake up timer clock by set RTC_CTRL.WKUPSEL[2:0] bits.
- Configure the wake-up automatic reload value by set RTC_WKUPT.WKUPT[15:0] bits.
- Enable Wakeup interrupt by set RTC_CTRL.WTIEN bit(this step can be selected as needed)
- Enable wakeup timer by setting RTC_CTRL.WTEN bit

14.2.14 Timestamp function

Timestamp can be enabled by setting RTC_CTRL.TSEN bit to 1. When a timestamp event is detected on the RTC_TS pin, the calendar values of the event will be stored in the timestamp register (RTC_TSSS, RTC_TST, RTC_TSD), and RTC_INITSTS.TISF is set to 1. If a new timestamp event is detected when RTC_INITSTS.TISF has been set to 1 already, the hardware sets RTC_INITSTS.TISOVF flag to 1, and the timestamp registers (RTC_TST and RTC_TSD) will continue to hold the value of the previous event, which means timestamp registers(RTC_TST and RTC_TSD) data will not change when RTC_INITSTS.TISF=1.

After the timestamp event caused by the synchronization process occurs again, RTC_INITSTS.TISF is set to 1 in 2 RTC_CLK cycles. There is no delay in the generation of RTC_INITSTS.TISOVF. This means that if two timestamp events are very close, this can cause RTC_INITSTS.TISOVF to be "1" and RTC_INITSTS.TISF to be "0". Therefore, after detecting that RTC_INITSTS.TISF is "1", then detect RTC_INITSTS.TISOVF bit.

If timestamp events are enabled, the timestamp will capture the calendar read in the timestamp register. Timestamp events can be generated on any of the 16 GPIO ports selected by EXTI. The GPIO pins in each port are selected by setting the corresponding EXTI_TS_SEL.TSSEL[3:0] bits.

14.2.15 Daylight saving time configuration

Daylight saving time function can be controlled by RTC_CTRL.SU1H, RTC_CTRL.AD1H, and RTC_CTRL.BAKP bits. Calendar will subtract one hour when set RTC_CTRL.SU1H bit to 1, and add one hour when set RTC_CTRL.AD1H to 1. RTC_CTRL.BAKP can be used to remember this adjustment or not.

14.2.16 RTC sub-second register shift

When the value of calendar has a sub-second deviation compared to the external precision clock, the shift function can be used to improve the precision of calendar.

Calendar can use RTC_SCTRL.SUB1S and RTC_SCTRL.ADFS[14:0] bits to control maximum delay or advance 1s. The resolution of the adjustment is 1/(RTC_PRE.DIVS[14:0]+1) second, it means the higher value of RTC_PRE.DIVS[14:0] , the higher of the resolution. However, to keep the synchronous prescaler output at 1Hz, the higher RTC_PRE.DIVS[14:0] means the lower RTC_PRE.DIVA[6:0], then more power consuming.

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Note: Before starting a shift operation, user must check RTC_SUBS.SS[15] bit is 0.

Whenever write RTC_SCTRL register, the RTC_INITSTS.SHOPF flag will be set by hardware, which indicate a shift operation is pending. Once this shift operation is complete, the bit is cleared by hardware.

14.2.17 RTC digital clock precision calibration

Digital precision calibration is achieved by adjusting the number of RTC clock pulses in the calibration period. Digital precision calibration resolution is 0.954 PPM with the range from -487.1 PPM to +488.5 PPM.

When the input frequency is 32768 Hz, calibration period can be configured as 2^{20} RTCCLK cycles or 32 seconds. The precision calibration register (RTC_CALIB) indicates that there has RTC_CALIB.CM[8:0] RTCCLK clock cycles will be reduced during the specified period.

The value of RTC_CALIB.CM[8:0] represents the number of RTCCLK pulses to be reduced during specified period. While RTC_CALIB.CP can be used to increase 488.5 PPM, every 2^{11} RTCCLK cycles will inserts a RTCCLK pulse.

When using RTC_CALIB.CM[8:0] and RTC_CALIB.CP in combination, it can increase cycles range from -511 to +512 RTCCLK cycles, and the calibration range from -487.1 ppm to +488.5 ppm, with the resolution is about 0.954 ppm.

The effective calibrated frequency (f_{CAL}) can be calculated by using the formula given below:

$$f_{CAL} = f_{RTCCLK} * (1 + \frac{RTC\_CALIB.CP*512 - RTC\_CALIB.CM[8:0]}{2^{20} + RTC\_CALIB.CM[8:0] - RTC\_CALIB.CP * 512})$$

Calibrated when RTC_PRE .DIVA[6:0]<3

When the asynchronous prescaler value (RTC_PRE.DIVA[6:0]) is less than 3, the RTC_CALIB.CP cannot be programmed to 1, and RTC_CALIB.CP value will be ignored if the it has been set to 1.

When RTC_PRE .DIVA[6:0]<3, the value of RTC_PRE.DIVS[14:0] should be decrease. Assume RTCCLK frequency is 32768Hz:

- When RTC_PRE .DIVA[6:0] =2, RTC_PRE.DIVS[14:0]=8189.
- When RTC_PRE .DIVA[6:0] =1, RTC_PRE.DIVS[14:0]=16379.
- When RTC_PRE .DIVA[6:0] =0, RTC_PRE.DIVS[14:0]=32759.

The effective calibrated frequency (f_{CAL}) can be calculated by using the formula given below:

$$f_{CAL} = f_{RTCCLK} * \left(1 + \frac{256 - RTC\_CALIB.CM[8:0]}{2^{20} + RTC\_CALIB.CM[8:0] - 265}\right)$$

Verify RTC calibration

RTC output 1Hz waveform for measuring and verifying RTC precision.

Up to 2 RTCCLK cycles measurement error may occur when measure the RTC frequency in a limit measurement period. If the measurement period is the same as calibration period, the error can be eliminated.

- The calibration period is 32 seconds (default).

  Using an accurate 32-second period to measure the 1Hz calibration output can ensure that the measurement error is within 0.447ppm (0.5 RTCCLK cycles within 32 seconds).

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- The calibration period is 16 seconds.

  Using an accurate 16-second period to measure the 1Hz calibration output can ensure that the measurement error is within 0.954ppm (0.5 RTCCLK cycles within 16 seconds).

- The calibration period is 8 seconds.

  Using an accurate 8-second period to measure the 1Hz calibration output can ensure that the measurement error is within 1.907ppm (0.5 RTCCLK cycles within 8 seconds).

Dynamic recalibration

When RTC_INITSTS.INITF=0, RTC_CALIB register can update by using following steps:

- Wait RTC_INITSTS.RECPF=0.
- A new value is written to the RTC_CALIB, then RTC_INITSTS.RECPF is automatically set to 1.
- The new calibration settings will take effect within 3 ck_apre cycles after a data write to the RTC_CALIB.

14.2.18 RTC low power mode

The working state of RTC in low power mode.

Lower Power Mode	RTC Working State	Exit Low Power Mode
SLEEP	Normal work	RTC interrupt
STOP0	Normal work when the clock source of RTC is LSE or LSI	Alarm A, Alarm B, Periodic Wakeup and Timestamp event
STOP2	Normal work when the clock source of RTC is LSE or LSI	Alarm A, Alarm B, Periodic Wakeup and Timestamp event
STANDBY	Normal work when the clock source of RTC is LSE or LSI	Alarm A, Alarm B and Timestamp event

14.3 RTC Registers

14.3.1 RTC Register overview

Table 14-2 RTC register overview

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
000h	RTC_TSH	Reserved									APM	HOT[1:0]		HOU[3:0]				Reserved	MIT[2:0]			MIU[3:0]				Reserved	SCT[2:0]			SCU[3:0]			
	Reset Value										0	0	0	0	0	0	0		0	0	0	0	0	0	0		0	0	0	0	0	0	0
004h	RTC_DATE	Reserved								YRT[3:0]				YRU[3:0]				WDU[2:0]			MOT	MOU[3:0]				Reserved	DAT[1:0]		DAU[3:0]				
	Reset Value									0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1		0	0	0	0	0	0	1
008h	RTC_CTRL	Reserved								COEN	OUTSEL[1:0]		OPOL	CALOSEL	BAKP	SU1H	AD1H	Reserved	WTIEN	ALBIEN	ALAIEN	TSEN	WTEN	ALBEN	ALAEN	Reserved	HFMT	BYPS	Reserved	TSPOL	WKUPSEL[2:0]		
	Reset Value									0	0	0	0	0	0	0	0		0	0	0	0	0	0	0		0	0		0	0	0	0

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Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
00Ch	RTC_INITSTS	Reserved															RECPF	Reserved			TISOVF	TISF	WTF	ALBF	ALAF	INITM	INITF	RSYF	INITSF	SHOPF	WTWF	ALBWF	ALAWF
	Reset Value																0				0	0	0	0	0	0	0	0	0	0	1	1	1
010h	RTC_PRE	Reserved									DIVA[6:0]							Reserved	DIVS[14:0]														
	Reset Value										1	1	1	1	1	1	1		0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
014h	RTC_WKUPT	Reserved																WKUPT[15:0]															
	Reset Value																	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
01Ch	RTC_ALARMA	MASK4	WKDSEL	DTT[1:0]		DTU[3:0]				MASK3	APM	HOT[1:0]		HOU[3:0]				MASK2	MIT[2:0]			MIU[3:0]				MASK1	SET[2:0]			SEU[3:0]			
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
020h	RTC_ALARMB	MASK4	WKDSEL	DTT[1:0]		DTU[3:0]				MASK3	APM	HOT[1:0]		HOU[3:0]				MASK2	MIT[2:0]			MIU[3:0]				MASK1	SET[2:0]			SEU[3:0]			
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
024h	RTC_WRP	Reserved																PKEY[7:0]															
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
028h	RTC_SUBS	Reserved																SS[15:0]															
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
02Ch	RTC_SCTRL	SUB1S	Reserved															ADFS[14:0]															
	Reset Value	0																0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
030h	RTC_TST	Reserved									APM	HOT[1:0]		HOU[3:0]				Reserved	MIT[2:0]			MIU[3:0]				Reserved	SET[2:0]			SEU[3:0]			
	Reset Value										0	0	0	0	0	0	0		0	0	0	0	0	0	0		0	0	0	0	0	0	0	0
034h	RTC_TSD	Reserved								YRT[3:0]				YRU[3:0]				WDU[2:0]			MOT	MOU[3:0]				Reserved	DAT[1:0]			DAU[3:0]			
	Reset Value									0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		0	0	0	0	0	0	0	0
038h	RTC_TSSS	Reserved																SSE[15:0]															
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
03Ch	RTC_CALIB	Reserved																CP	CW8	CW16	Reserved				CM[8:0]								
	Reset Value																	0	0	0					0	0	0	0	0	0	0	0	0
044h	RTC_ALRMASS	Reserved				MASKSSA[3:0]				Reserved								SSV[14:0]															
	Reset Value					0	0	0	0									0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
048h	RTC_ALRMBSS	Reserved				MASKSSB[3:0]				Reserved								SSV[14:0]															
	Reset Value					0	0	0	0									0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
04Ch	RTC_OPT	Reserved																															TYPE
	Reset Value																																0

14.3.2 RTC Calendar Time Register (RTC_TSH)

Address offset: 0x00

Reset value: 0x0000 0000

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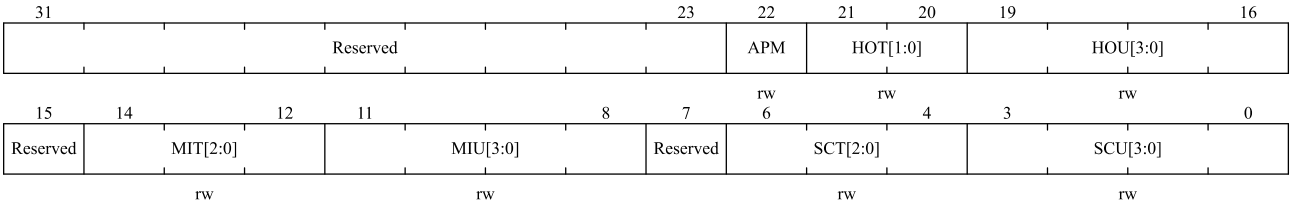
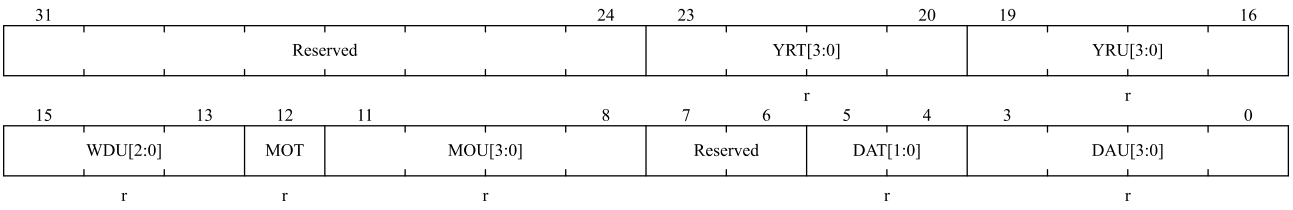


Bit field	Name	Description
31:23	Reserved	Reserved, the reset value must be maintained
22	APM	AM/PM format. 0:AM format or 24-hour format 1:PM format
21:20	HOT[1:0]	Describes the hour tens value in BCD format
19:16	HOU[3:0]	Describes the hour units value in BCD format
15	Reserved	Reserved, the reset value must be maintained
14:12	MIT [2: 0]	Describes the minute tens value in BCD format
11:8	MIU[3:0]	Describes the minute units value in BCD format
7	Reserved	Reserved, the reset value must be maintained
6:4	SCT[2:0]	Describes the second tens value in BCD format
3:0	SCU[3:0]	Describes the second units value in BCD format

14.3.3 RTC Calendar Date Register (RTC_DATE)

Address offset: 0x04

Reset value: 0x0000 2101



Bit field	Name	Description
31:24	Reserved	Reserved, the reset value must be maintained
23:20	YRT[3:0]	Describes the year tens value in BCD format
19:16	YRU[3:0]	Describes the year units value in BCD format
15:13	WDU[2:0]	Describes which Week day 000: Forbidden 001: Monday ... 111: Sunday
12	MOT	Describes the month tens value in BCD format
11:8	MOU[3:0]	Describes the month units value in BCD format
7:6	Reserved	Reserved, the reset value must be maintained

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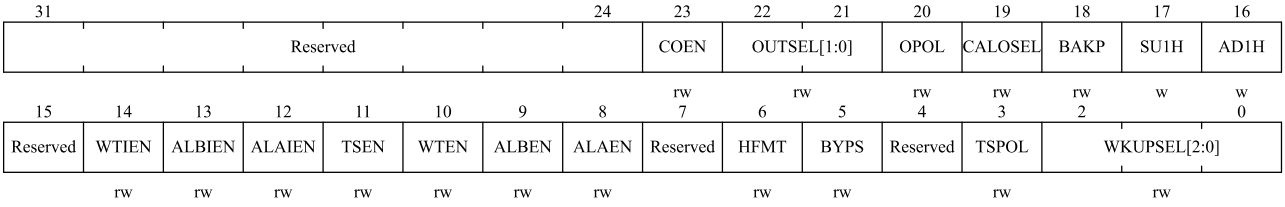
Bit field	Name	Description
5:4	DAT[1:0]	Describes the date tens value in BCD format
3:0	DAU[3:0]	Describes the date units value in BCD format

14.3.4 RTC Control Register (RTC_CTRL)

Address offset: 0x08

Reset value: 0x0000 0000



Bit field	Name	Description
31:24	Reserved	Reserved, the reset value must be maintained
23	COEN	Calibration output enable This bit controls RTC_CALIB output 0: Disable calibration output 1: Enable calibration output
22:21	OUTSEL[1:0]	Output selection These bits are used to select the alarm/wakeup output 00: Disable output 01: Enable Alarm A output 10: Enable Alarm B output 11: Enable Wakeup output
20	OPOL	Output polarity bit This bit is used to configure the polarity of output. 0: Outputs high level when the selected output triggers(see OUTSEL[1:0]) 1: Outputs low level when the selected output triggers(see OUTSEL[1:0])
19	CALOSEL	Calibration output selection When RTC_CTRL.COEN=1, RTCCLK = 32.768KHz and prescale at their default value (RTC_PRE.DIVA[6:0]=127 and RTC_PRE.DIVS[14:0]=255). 0: Calibration output is 256 Hz 1: Calibration output is 1 Hz
18	BAKP	Daylight saving time record This bit is written by the user 0: Not record daylight saving time 1: Record daylight saving time
17	SU1H	Subtract 1 hour (winter time change) 1 hour will be subtracted to the calendar time when the current hour value is not 0. This bit is always read as 0. 0: No effect.

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Bit field	Name	Description
		1: Subtracts 1 hour to the current time.
16	AD1H	Add 1 hour (summer time change) When this bit is set, 1 hour can be added to the calendar time. This bit is always read as. 0: No effect. 1: Adds 1 hour to the current time.
15	Reserved	Reserved, the reset value must be maintained
14	WTIEN	Wakeup timer interrupt enable 0: Disable wakeup timer interrupt. 1: Enable wakeup timer interrupt.
13	ALBIEN	Alarm B interrupt enable 0: Disable Alarm B interrupt 1: Enable Alarm B Interrupt
12	ALAIEN	Alarm A interrupt enable 0: Disable Alarm A interrupt 1: Enable Alarm A interrupt
11	TSEN	Timestamp enable 0: Disable timestamp 1: Enable timestamp
10	WTEN	Wakeup timer enable 0: Disable wakeup timer 1: Enable wakeup timer
9	ALBEN	Alarm B enable 0: Disable Alarm B 1: Enable Alarm B
8	ALAEN	Alarm A enable 0: Disable Alarm A 1: Enable Alarm A
7	Reserved	Reserved, the reset value must be maintained
6	HFMT	Hour format bit 0: 24 hour format 1: Am/PM format
5	BYPS	Bypass values from the shadow registers 0: Calendar values are copied from the shadow registers, which are refreshed every two RTCCLK cycles. 1: Calendar values are copied directly from the calendar counters. *Note: If the frequency of the APB1 clock falls below seven times the frequency of RTCCLK, RTC_CTRL.BYPS bit must be set to '1'*
4	Reserved	Reserved, the reset value must be maintained
3	TSPOL	Time-stamp event active edge 0: Input rising edge creates a timestamp event 1: Input falling edge creates a timestamp event TSE need to be reset when TSPOL is changed to avoid unwanted RTC_INITSTS.TISF setting.

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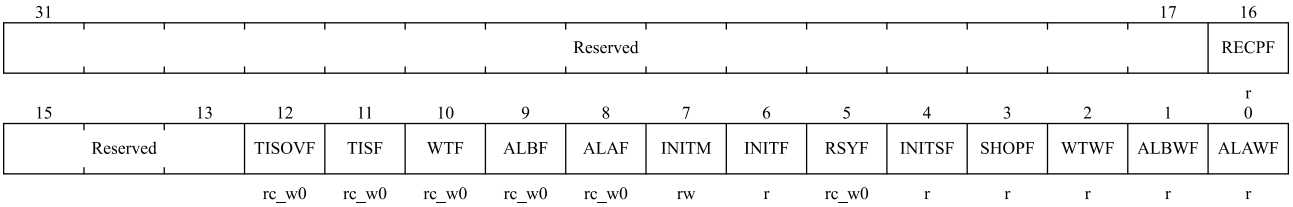
Bit field	Name	Description
2:0	WKUPSEL[2:0]	Wakeup clock selection 000: RTC clock is divided by 16 001: RTC clock is divided by 8 010: RTC clock is divided by 4 011: RTC clock is divided by 2 10x: ck_spre (usually 1Hz) clock is selected

14.3.5 RTC Initial Status Register (RTC_INITSTS)

Address offset: 0x0C

Reset value: 0x0000 0007



Bit field	Name	Description
31:17	Reserved	Reserved, the reset value must be maintained
16	RECPF	Recalibration pending flag The RECPF status flag is automatically set to '1' when software writes to the RTC_CALIB register, indicating that the RTC_CALIB register is blocked. After the new calibration settings are processed, this bit returns to '0'.
15:13	Reserved	Reserved, the reset value must be maintained
12	TISOVF	The time-stamp overflow flag This flag is set to '1'by hardware when a time-stamp event happens when TISF bit is set. This flag can be cleared by software writing 0. It is advised to check and clear TISOVF only after clearing the TISF bit. Otherwise, an overflow might not be noticed if a timestamp event occurs immediately before the TISF bit is being cleared.
11	TISF	Time-stamp flag This flag is set to '1' by hardware when a time-stamp event happens. This flag can be cleared by software writing 0
10	WTF	Wake up timer flag This flag is set by hardware when the value of wakeup auto-reload counter reaches 0. This flag is cleared by software by writing 0. This flag must be cleared by software at least 1.5 RTCCLK periods before WTF is set again.
9	ALBF	Alarm B flag This flag is set to '1' by hardware when the time/date registers value match the Alarm B register values. This flag can be cleared by software writing 0

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Bit field	Name	Description
8	ALAF	Alarm A flag This flag is set to '1' by hardware when the time/date registers value match the Alarm A register values. This flag can be cleared by software writing 0
7	INITM	Enter Initialization mode 0: Free running mode 1: Enter initialization mode and set calendar time value, date value, and prescale value.
6	INITF	Initialization flag RTC is in initialization state when this bit is '1', and calendar time, date and prescale value can be updated. 0: Calendar time, date and prescale value can not be updated 1: Calendar time, date and prescale value can be updated
5	RSYF	Register synchronization flag This flag is set to '1' by hardware when the calendar value are copied into the shadow registers. This bit is cleared by hardware when in initialization mode, while a shift operation is pending (SHOPF = 1), or when in bypass shadow register mode (RTC_CTRL.BYPS = 1). This bit can also be cleared by software. It is cleared either by software or by hardware in initialization mode. 0: Calendar shadow register not yet synchronized 1: Calendar shadow register synchronized
4	INITSF	Initialization status flag This flag is set to '1' by hardware when the calendar year field is different from 0 (which is the RTC domain reset state). 0: Calendar has not been initialized 1: Calendar has been initialized
3	SHOPF	Shift operation pending flag This flag is set to '1' by hardware as soon as a shift operation is initiated by a write to the RTC_SCTRL register. It is cleared by hardware when the corresponding shift operation has been completed, note that writing to the SHOPF bit has no effect. 0: No shift operation is pending 1: A shift operation is pending
2	WTWF	Wakeup timer write flag 0: Wakeup timer configuration update is not allowed 1: Wakeup timer configuration update is allowed
1	ALBWF	Alarm B write flag This flag is set to '1' by hardware when Alarm B values can be changed, after the RTC_CTRL.ALBEN bit has been set to 0. 0: Alarm B update is not allowed 1: Alarm B update is allowed
0	ALAWF	Alarm A write flag. This flag is set to '1' by hardware when Alarm A values can be changed, after the RTC_CTRL.ALAEN bit has been set to 0.

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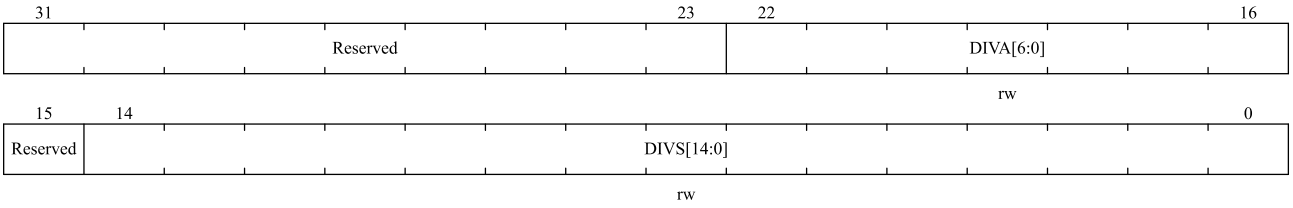
Bit field	Name	Description
		0: Alarm A update is not allowed 1: Alarm A update is allowed

14.3.6 RTC Prescaler Register (RTC_PRE)

Address offset: 0x10

Reset value: 0x007F 00FF

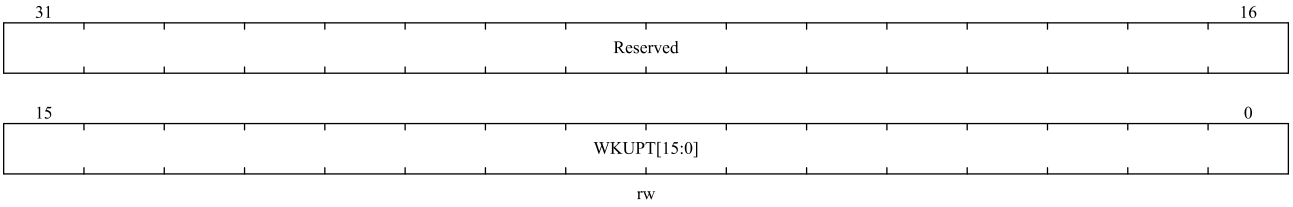


Bit field	Name	Description
31:23	Reserved	Reserved, the reset value must be maintained
22:16	DIVA[6:0]	Asynchronous prescaler factor f_{ck_apre} = RTCCLK/(DIVA[6:0]+1)
15	Reserved	Reserved, the reset value must be maintained
14:0	DIVS[14:0]	Synchronous prescaler factor $f_{ck\_spre} = f_{ck\_apre}$/(DIVS[14:0]+1)

14.3.7 RTC Wakeup Timer Register (RTC_WKUPT)

Address offset: 0x14

Reset value: 0x0000 FFFF



Bit field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained
15:0	WKUPT[15:0]	Wake up auto-reload value bits The RTC_INITSTS.WTF flag is set every (WKUPT[15:0] + 1) ck_wut cycles when the RTC_CTRL.WTEN=1. The wakeup timer becomes 17-bits When RTC_CTRL.WKUPSEL[2]=1. *Note:* *This register change (such as the second setting or later Settings) needs to be changed in the wakeup interrupt, otherwise the changed settings will not take effect immediately, but will take effect after the next wakeup;*

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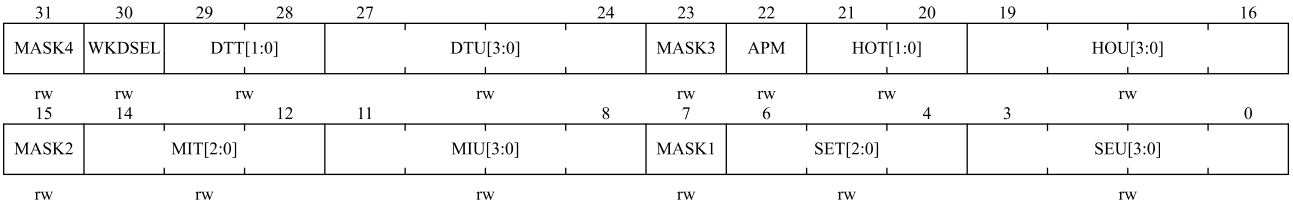
Bit field	Name	Description
		In particular, when RTC_CTRL.WKUPSEL[2:0] is set to 010, the modified setting does not take effect immediately, but will take effect after wake up in the next cycle.

14.3.8 RTC Alarm A Register (RTC_ALARMA)

Address offset: 0x1C

Reset value: 0x0000 0000



Bit field	Name	Description
31	MASK4	Alarm date mask 0: Date/day match 1: Date/day not match
30	WKDSEL	Week day selection 0: DTU[3:0] represents the date units 1: DTU[3:0] represents week day only. DTT[1:0] is not considered
29:28	DTT[1:0]	Describes the date tens value in BCD format
27:24	DTU[3:0]	Describes the date units value in BCD format
23	MASK3	Alarm hours mask 0: Hours match 1: Hours not match
22	APM	AM/PM notation 0: AM or 24 hours format 1: PM format
21:20	HOT[1:0]	Describes the hour tens value in BCD format
19:16	HOU[3:0]	Describes the hour units value in BCD format
15	MASK2	Alarm minutes mask 0: Minutes match 1: Minutes not match
14:12	MIT[2:0]	Describes the minute tens value in BCD format
11:8	MIU[3:0]	Describes the minute units value in BCD format
7	MASK1	Alarm seconds mask 0: Seconds match 1: Seconds not match
6:4	SET[2:0]	Describes the second tens value in BCD format
3:0	SEU[3:0]	Describes the second units value in BCD format

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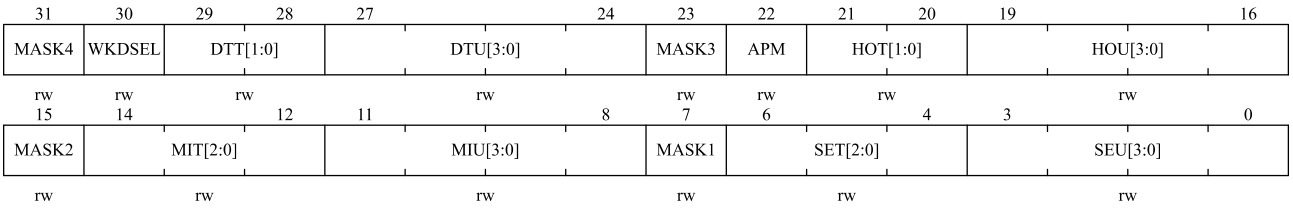
14.3.9 RTC Alarm B Register (RTC_ ALARMB)

Address offset: 0x20

Reset value: 0x0000 0000



Bit field	Name	Description
31	MASK4	Alarm date mask 0: Date/day match 1: Date/day not match
30	WKDSEL	Week day selection 0: DTU[3:0] represents the date units 1: DTU[3:0] represents week day only. DTT[1:0] is not considered
29:28	DTT[1:0]	Describes the date tens value in BCD format
27:24	DTU[3:0]	Describes the date units value in BCD format
23	MASK3	Alarm hours mask 0: Hours match 1: Hours not match
22	APM	AM/PM notation 0: AM or 24 hours format 1: PM format
21:20	HOT[1:0]	Describes the hour tens value in BCD format
19:16	HOU[3:0]	Describes the hour units value in BCD format
15	MASK2	Alarm minutes mask 0: Minutes match 1: Minutes not match
14:12	MIT[2:0]	Describes the minute tens value in BCD format
11:8	MIU[3:0]	Describes the minute units value in BCD format
7	MASK1	Alarm seconds mask 0: Seconds match 1: Seconds not match
6:4	SET[2:0]	Describes the second tens value in BCD format
3:0	SEU[3:0]	Describes the second units value in BCD format

14.3.10 RTC Write Protection register (RTC_WRP)

Address offset: 0x24

Reset value: 0x0000 0000

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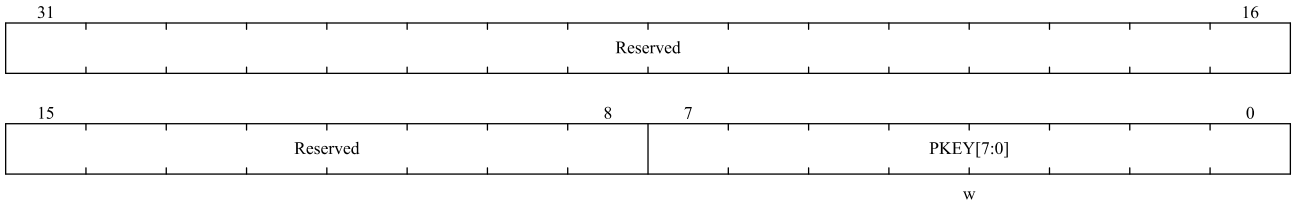
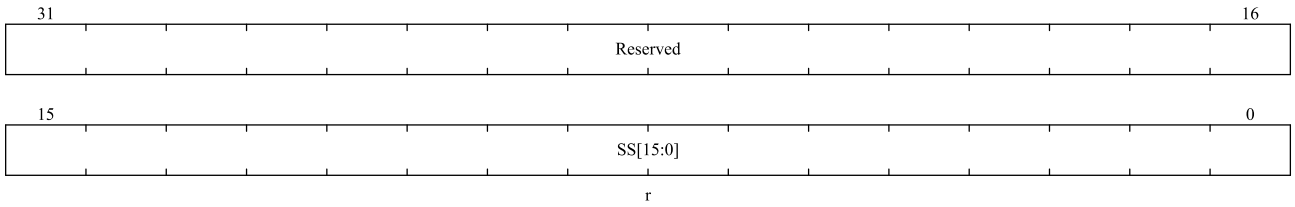


Bit field	Name	Description
31:8	Reserved	Reserved, the reset value must be maintained
7:0	PKEY[7:0]	Write protection key Reading this byte always returns 0x00. For detail on how to unlock RTC register write protection, see chapter RTC write protection register.

14.3.11 RTC Sub-second Register (RTC_SUBS)

Address offset: 0x28

Reset value: 0x0000 0000



Bit field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained
15:0	SS[15:0]	Sub-second value. The value is the counter value of synchronous prescaler. This sub-second value is calculated by the below formula: Sub-second value = (RTC_PRE.DIVS[14:0]-SS)/(RTC_PRE.DIVS[14:0]+1) *Note: SS[15:0] can be larger than RTC_PRE.DIVS[14:0] only after the shift operation is finished. In this case, the correct time/date is one second slower than the time/date indicated by RTC_TSH/RTC_DATE.*

14.3.12 RTC Shift Control Register (RTC_ SCTRL)

Address offset: 0x2C

Reset value: 0x0000 0000

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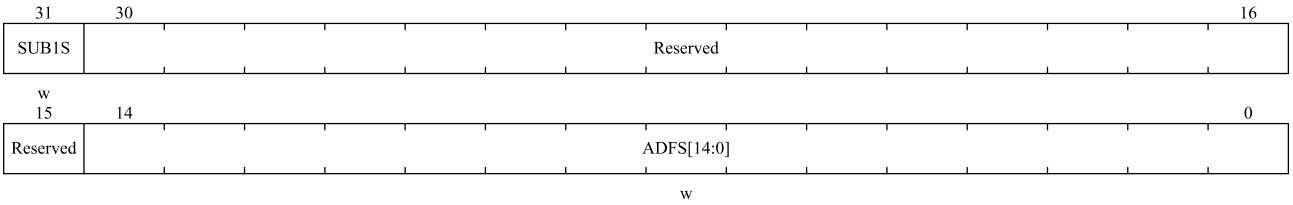
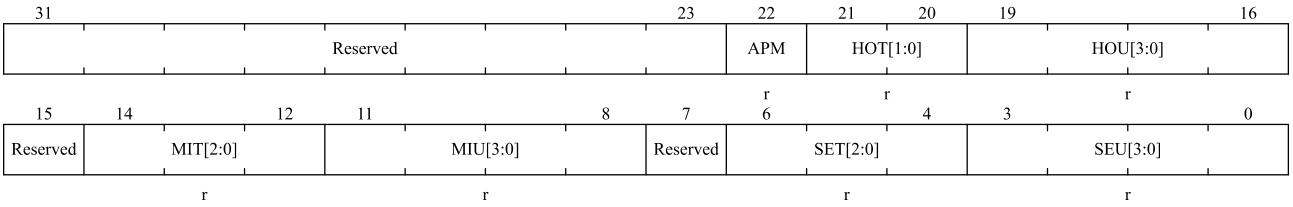


Bit field	Name	Description
31	SUB1S	Add one second 0: No impact. 1: Subtract one second to the clock/calendar This bit can only be written and read as zero. Writing to this bit does not have an impact when RTC_INITSTS.SHOPF=1.
30:15	Reserved	Reserved, the reset value must be maintained
14:0	ADFS[14:0]	Add a fraction of a second This bit is a write-only bit and is always read as 0. The value written to ADFS[14:0] will be subtracted by the synchronous prescaler counter. As the counter counts down, this operation can effectively speed up the following time from the clock: Acceleration (seconds) = ADFS [14:0]/ (DIVS[14:0] + 1) SUB1S bit can be used together with the ADFS[14:0]bits: Delay (seconds) = 1-(ADFS[14:0] / (DIVS[14:0] + 1)). *Note: Before writing ADFS[14:0], need to read the RTC_SUBS register to ensure that ADFS[14:0] < RTC_SUBS.SS[15:0];*

14.3.13 RTC Timestamp Time Register (RTC_TST)

Address offset: 0x30

Reset value: 0x0000 0000



Bit field	Name	Description
31:23	Reserved	Reserved, the reset value must be maintained
22	APM	AM/PM notation 0: AM or 24-hour clock 1: PM
21:20	HOT[1:0]	Describes the hour tens value in BCD format
19:16	HOU[3:0]	Describes the hour units value in BCD format
15	Reserved	Reserved, the reset value must be maintained
14:12	MIT[2:0]	Describes the minute tens value in BCD format

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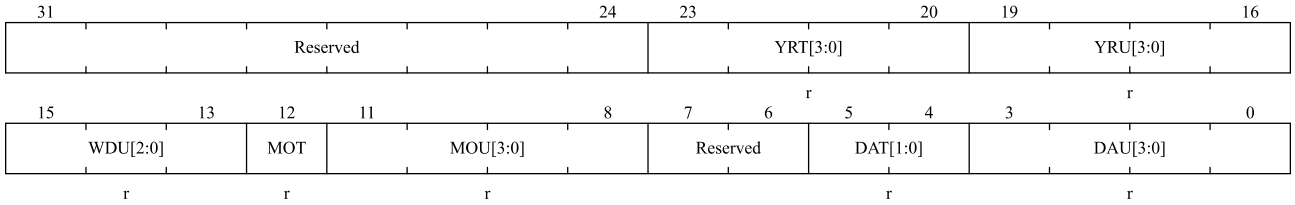
Bit field	Name	Description
11:8	MIU[3:0]	Describes the minute units value in BCD format
7	Reserved	Reserved, the reset value must be maintained
6:4	SET[2:0]	Describes the second tens value in BCD format
3:0	SEU[3:0]	Describes the second units value in BCD format

14.3.14 RTC Timestamp Date Register (RTC_TSD)

Address offset: 0x34

Reset value: 0x0000 0000

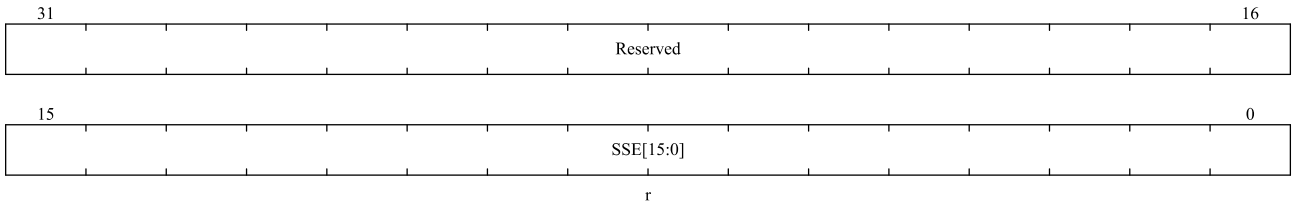


Bit field	Name	Description
31:24	Reserved	Reserved, the reset value must be maintained
23:20	YRT[3:0]	Describes the year tens value in BCD format
19:16	YRU[3:0]	Describes the year units value in BCD format
15:13	WDU[2:0]	Describes which Week day 000: Forbidden 001: Monday ... 111: Sunday
12	MOT	Describes the month tens value in BCD format
11:8	MOU[3:0]	Describes the month units value in BCD format
7:6	Reserved	Reserved, the reset value must be maintained
5:4	DAT[1:0]	Describes the date tens value in BCD format
3:0	DAU[3:0]	Describes the date units value in BCD format

14.3.15 RTC Timestamp Sub-second Register (RTC_TSSS)

Address offset: 0x38

Reset value: 0x0000 0000



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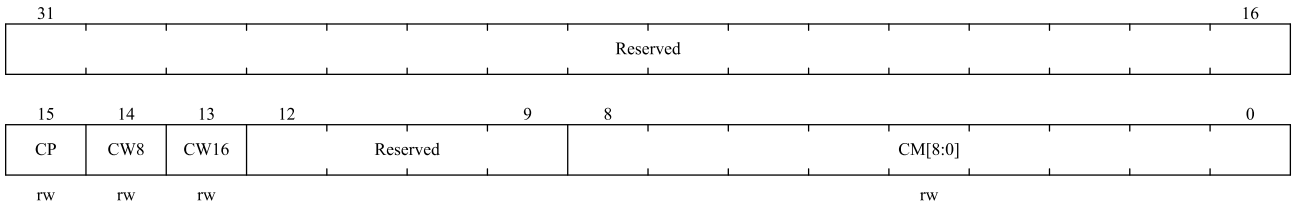
Bit field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained
15:0	SSE[15:0]	Sub second value SSE[15:0] is the value in the synchronous prescaler counter. The fraction of a second is provided by the formula below: Second fraction = (RTC_PRE.DIVS[14:0] – SSE[15:0]) / (RTC_PRE.DIVS[14:0] + 1) *Note: SSE[15:0] can be larger than RTC_PRE.DIVS[14:0] only after a shift operation. In that case, the correct time/date is one second less than as indicated by RTC_TSH/RTC_DATE.*

14.3.16 RTC Calibration Register (RTC_CALIB)

Address offset: 0x3C

Reset value: 0x0000 0000



Bit field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained
15	CP	Increase frequency of RTC by 488.5 ppm This feature is intended to be used along with CM[8:0]. When RTCCLK frequency is 32768 Hz, the number of RTCCLK pulses added during a 32-second window is ((512 * CP) – CM[8:0]). 0: No add pulse. 1: One RTCCLK pulse is inserted every 2^{11} pulses.
14	CW8	Select an 8-second calibration cycle period 0: Not effect. 1: Select an 8-second calibration period. When CW8 is set to ‘1’, the 8-second calibration cycle period is selected. *Note: when CW8 = 1, CM[1:0] will always be' 00'*
13	CW16	To select a 16-second calibration cycle period 0: Not effect. 1: Select a calibration period of 16 seconds. If CW8 = 1, this bit cannot be set to 1. *Note: when CW16 = 1, CM[0] will always be '0'*
12:9	Reserved	Reserved, the reset value must be maintained
8:0	CM[8:0]	Negative calibration bits The number of mask pulse out of 2^{20} RTCCLK pulses. This effectively decreases the frequency of the calendar with a resolution of 0.9537 ppm.

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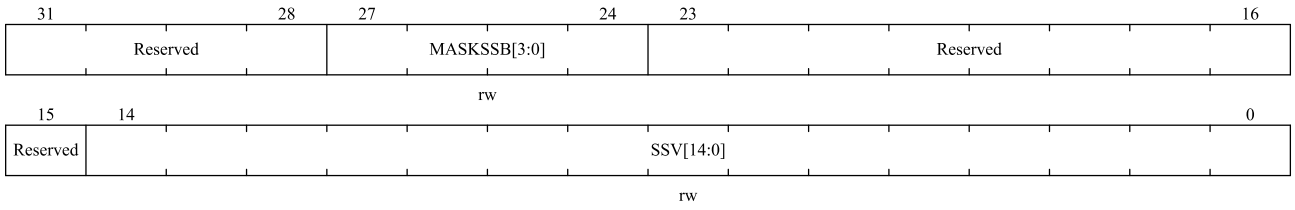
14.3.17 RTC Alarm A sub-second register (RTC_ ALRMASS)

Address offset: 0x44

Reset value: 0x0000 0000

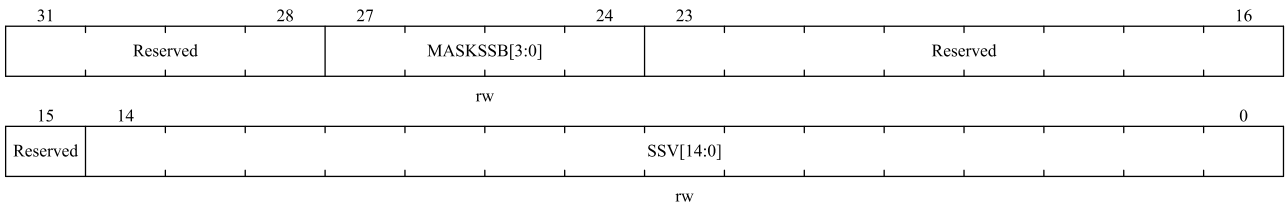


Bit field	Name	Description
31:28	Reserved	Reserved, the reset value must be maintained
27:24	MASKSSB[3:0]	Mask the most significant bit from this bits. 0x0: No comparison on sub seconds for Alarm. The alarm is set when the seconds unit is incremented (assuming that the rest of the fields match). 0x1: Only SSV[0] is compared and other bits are not compared. 0x2: Only SSV[1:0] are compared and other bits are not compared. 0x3: Only SSV[2:0] are compared and other bits are not compared. ... 0xC: Only SSV[11:0] are compared and other bits are not compared. 0xD: Only SSV[12:0] are compared and other bits are not compared. 0xE: Only SSV[13:0] are compared and other bits are not compared. 0xF: SSV[14:0] are compared Synchronization counter RTC_SUBS.SS[15] bit is never compared.
23:15	Reserved	Reserved, the reset value must be maintained
14:0	SSV[14:0]	Sub seconds value This value is compared with the synchronous prescaler counter RTC_SUBS.SS[14:0], and bit number of compared is controlled by MASKSSB[3:0].

14.3.18 RTC Alarm B sub-second register (RTC_ ALRMBSS)

Address offset: 0x48

Reset value: 0x0000 0000



Bit field	Name	Description
31:28	Reserved	Reserved, the reset value must be maintained

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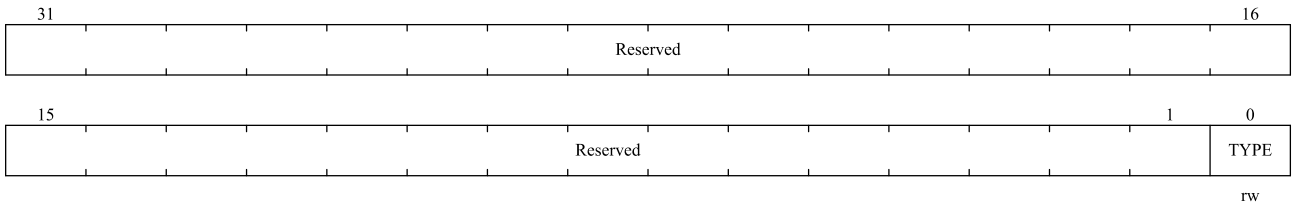
Bit field	Name	Description
27:24	MASKSSB[3:0]	Mask the most significant bit from this bits. 0x0: No comparison on sub seconds for Alarm. The alarm is set when the seconds unit is incremented (assuming that the rest of the fields match). 0x1: Only SSV[0] is compared and other bits are not compared. 0x2: Only SSV[1:0] are compared and other bits are not compared. 0x3: Only SSV[2:0] are compared and other bits are not compared. ... 0xC: Only SSV[11:0] are compared and other bits are not compared. 0xD: Only SSV[12:0] are compared and other bits are not compared. 0xE: Only SSV[13:0] are compared and other bits are not compared. 0xF: SSV[14:0] are compared Synchronization counter RTC_SUBS.SS[15] bit is never compared.
23:15	Reserved	Reserved, the reset value must be maintained
14:0	SSV[14:0]	Sub seconds value This value is compared with the synchronous prescaler counter RTC_SUBS.SS[14:0], and bit number of compared is controlled by MASKSSB[3:0].

14.3.19 RTC Option Register (RTC_ OPT)

Address offset: 0x4C

Reset value: 0x0000 0000



Bit field	Name	Description
31:1	Reserved	Reserved, the reset value must be maintained
0	TYPE	RTC_ALARM output type on PC13 0: Open-drain output 1: Push-pull output

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15 CRC Calculation Unit

15.1 Introduction

This module integrates the functions of CRC32 and CRC16, and the cyclic redundancy check (CRC) calculation unit obtains any CRC calculation result according to a fixed generator polynomial. In other applications, CRC technology is mainly used to verify the correctness and integrity of data transmission or data storage. EN/IEC 60335-1 provides a method to verify the integrity of flash memory. CRC calculation unit can calculate the identifier of the software when the program is running, then compare it with the reference identifier generated during connection, and then store it in the specified memory space.

15.2 Main Features

15.2.1 CRC32

- CRC32($X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$)
- 32 bits of data to be checked and 32 bits of output check code.
- CRC calculation time: 1 AHB clock cycles (HCLK)
- General-purpose 8-bit register (can be used to store temporary data)

15.2.2 CRC16

- CRC16($X^{16} + X^{15} + X^2 + 1$)
- There are 8 bits of data to be checked and 16 bits of output check code.
- CRC calculation time: 1 AHB clock cycle (HCLK)
- The verification initial value can be configured, and the size end of the data to be verified can be configured.
- Support 8bit LRC check value generation

The following figure is the block diagram of CRC unit.

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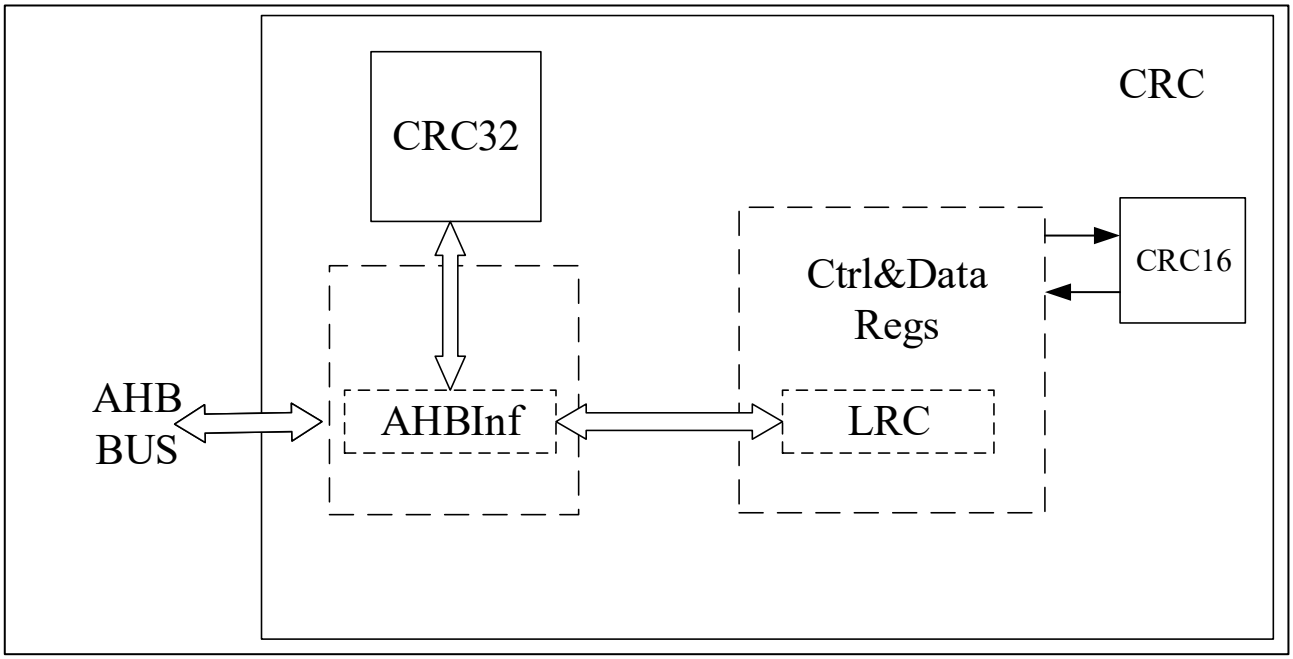
Figure 15-1 CRC calculation unit block diagram



15.3 Function Description

15.3.1 CRC32

CRC unit contains one 32-bit data register:

- Writing this register to input CRC data.
- Reading this register to get the calculated CRC result.

Every writing operation of this data register triggers the calculation of this new data with the previous calculation result (CRC calculation is performed on the whole 32-bit word rather than byte by byte).

Supports back-to-back writes or sequential write-read operations.

CRC_CRC32DAT can be re-initialized to 0xFFFFFFFF by setting CRC_CRC32CTRL.RESET. This operation does not affect the data in register CRC_CRC32IDAT.

15.3.2 CRC16

The LSB or MSB of the check data is controlled by the CRC_CRC16CTRL.ENDHL bit.

To clear the result of the last CRC operation, set CRC_CRC16CTRL.CLR to 1 or CRC_CRC16D to 0.

The initial value of CRC calculation can be configured by writing the CRC_CRC16D register. By default, the initial value is the result of the last calculation.

LRC calculation is the same as CRC calculation. Both are carried out at the same time. CRC or LRC can be read out depending on needs. If the initial value needs to be set, the LRC register should be configured first.

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15.4 CRC registers

15.4.1 CRC register overview

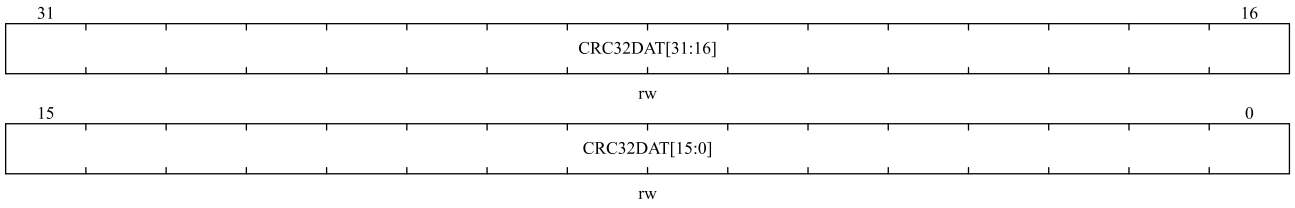
Table 15-1 CRC register overview

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
000h	CRC32DAT	CRC32DAT[31:0]																															
	Reset Value	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
004h	CRC32IDAT	Reserved																								CRC32IDAT[7:0]							
	Reset Value																									0	0	0	0	0	0	0	0
008h	CRC32CTRL	Reserved																															RESET
	Reset Value																																0
00Ch	CRC16CTRL	Reserved																													CLR	ENDHL	Reserved
	Reset Value																														0	0	0
010h	CRC16DAT	Reserved																								CRC16DAT[7:0]							
	Reset Value																									0	0	0	0	0	0	0	0
014h	CRC16D	Reserved																CRC16D[15:0]															
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
018h	LRC	Reserved																								LRCDAT[7:0]							
	Reset Value																									0	0	0	0	0	0	0	0

15.4.2 CRC32 data register (CRC_CRC32DAT)

Address offset: 0x00

Reset value: 0xFFFF FFFF



Bit field	Name	Description
31:0	CRC32DAT[31:0]	The written data is the CRC value to be checked. The read data is the CRC calculation result. Only 32-bit operations are supported.

15.4.3 CRC32 independent data register (CRC_CRC32IDAT)

Address offset: 0x04

Reset value: 0x0000 0000

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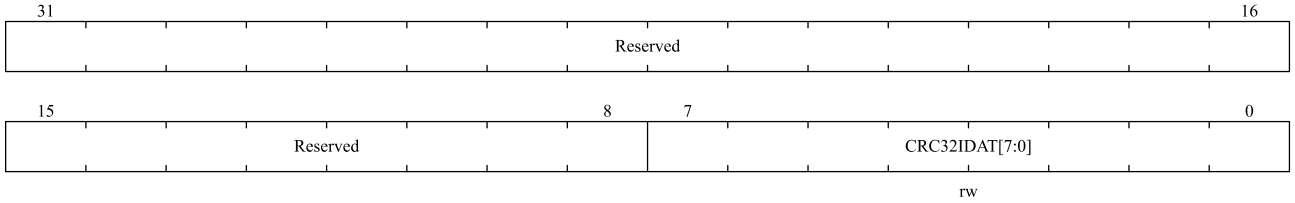


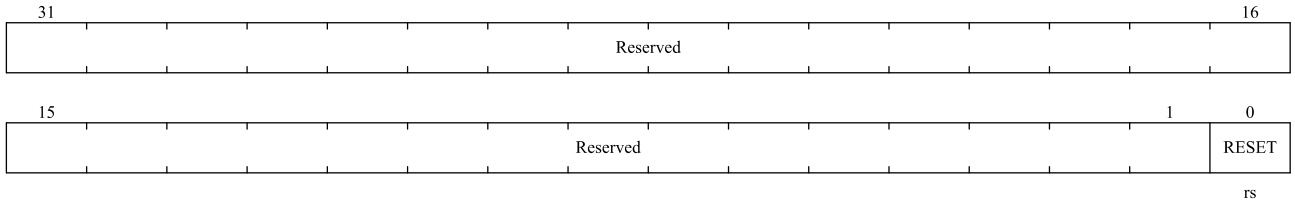
Bit field	Name	Description
31:8	Reserved	Reserved, the reset value must be maintained.
7:0	CRC32IDAT[7:0]	Independent 8-bit data register. General 8 bits data register. It is for temporary stored 1-byte data. CRC_CRC32CTRL.RESET reset signal will not impact this register.

Note: This register is not a part of CRC calculation and can be used to store any data.

15.4.4 CRC32 control register (CRC_CRC32CTRL)

Address offset: 0x08

Reset value: 0x0000 0000

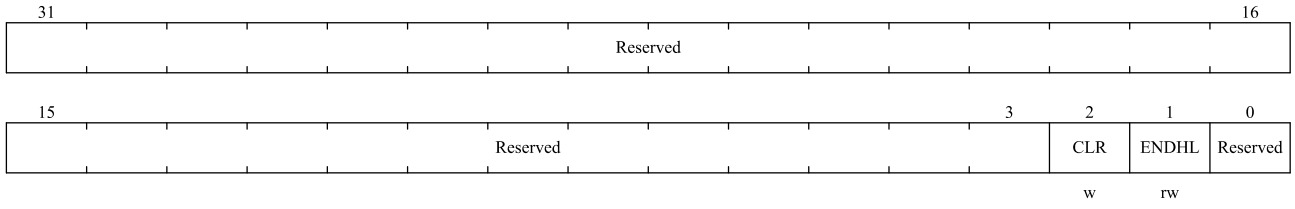


Bit field	Name	Description
31:1	Reserved	Reserved, the reset value must be maintained.
0	RESET	RESET signal. It can reset CRC32 module and set data register to be 0xFFFF_FFFF. This reset can only write 1, and hardware will clear to 0 automatically.

15.4.5 CRC16 control register (CRC_CRC16CTRL)

Address offset: 0x0C

Reset value: 0x0000 0000



Bit field	Name	Description
31:3	Reserved	Reserved, the reset value must be maintained.

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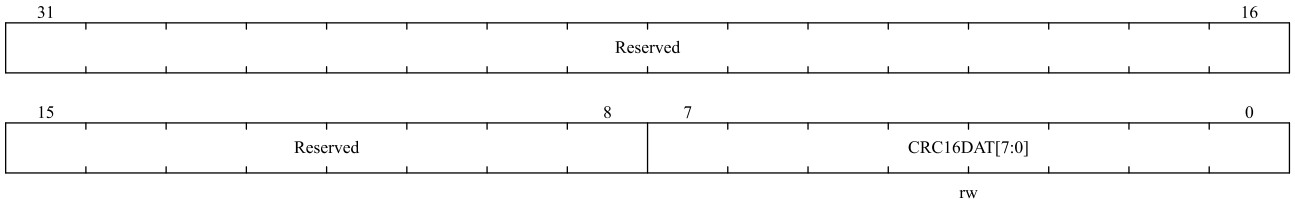
Bit field	Name	Description
2	CLR	Clear CRC16 results. 0: Not clear. 1: Clear to default value 0x0000. Set this bit to 1 will only maintain 1 clock cycle, hardware will clear automatically. (Software read always 0).
1	ENDHL	Data to be verified start to calculate from MSB or LSB(configured endian). 0: From MSB to LSB 1: From LSB to MSB This bit is only for data to be verified.
0	Reserved	Reserved, the reset value must be maintained.

Note: 8-bits, 16-bits and 32-bits operations are supported.

15.4.6 CRC16 input data register (CRC_CRC16DAT)

Address offset: 0x10

Reset value: 0x0000 0000



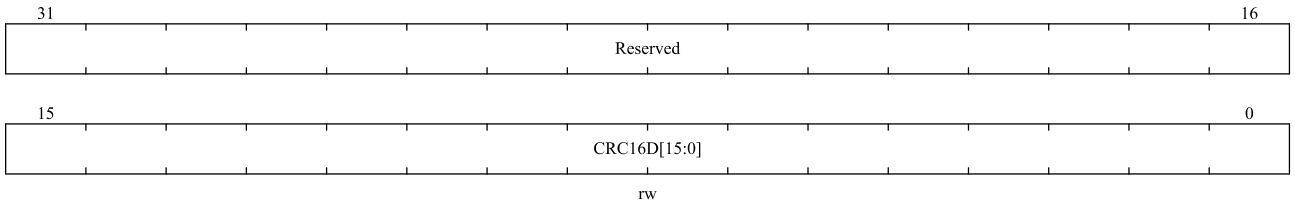
Bit field	Name	Description
31:8	Reserved	Reserved, the reset value must be maintained.
7:0	CRC16DAT[7:0]	Data to be verified.

Note: 8-bits, 16-bits and 32-bits operations are supported.

15.4.7 CRC cyclic redundancy check code register (CRC_CRC16D)

Address offset: 0x14

Reset value: 0x0000 0000



Bit field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained.
15:0	CRC16D[15:0]	16-bit value of cyclic redundancy result data. Every time the software writes the CRC16DAT register, the 16-bit calculated data from

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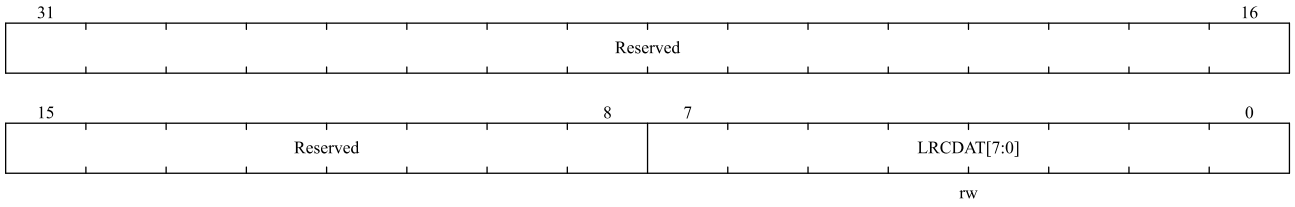
Bit field	Name	Description
		CRC16 is updated in this register.

Note: 8-bits, 16-bits and 32-bits operations are supported (8-bit operations must be performed twice in a row to ensure that 16-bit initial values are configured properly)

15.4.8 LRC result register (CRC_LRC)

Address offset: 0x18

Reset value: 0x0000 0000



Bit field	Name	Description
31:8	Reserved	Reserved, the reset value must be maintained.
7:0	LRCDAT[7:0]	LRC check value register. Software need to write initial value before use. And then each writing data to CRC_CRC16DAT will be XOR with CRC_LCR register value. The result will be stored in CRC_LRC. Software read the result. It should be cleared before next use.

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16 Independent Watchdog (IWDG)

16.1 Introduction

The N32G45x has built-in independent watchdog (IWDG) and window watchdog (WWDG) timers to solve the problems caused by software errors. Watchdog timer is very flexible to use, which improves the security of the system and the accuracy of timing control.

Independent Watchdog (IWDG) is driving by Low-speed internal clock (LSI clock) running at 40 KHz, which will still running event dead loop or MCU stuck is happening. This can provide higher safety level, timing accuracy and flexibility of watchdog. It can reset and resolve system malfunctions due to software failure. The IWDG is best suited for applications that require the watchdog to run as a totally independent process outside the main application, but have lower timing accuracy constraints.

When the power control register PWR_CTRL2.IWDGRSTEN bit is '1' and the IWDG counter reaches 0, a system reset will be generated (if this bit is '0', the IWDG will count but not reset). When the PWR_CTRL2.IWDGRSTEN bit is '1' and the IWDG counter reaches 0, it can wake up low power consumption (if this bit is '0', IWDG will count and reset but can only wake up SLEEP/STOP0, not STOP2/STANDBY).

Note: This chapter is based on the system default IWDGRSTEN=1, IWDGWPEN=1 discussion..

16.2 Main Features

- Independent 12-bit down-counter
- RC oscillator provides independent clock source, which can also operate in SLEEP, STOP0, STOP2 and STANDBY mode.
- Reset and low-power wake-up can be matched.
- A system reset occurs when the down counter reaches 0x0000 (if watchdog activated).

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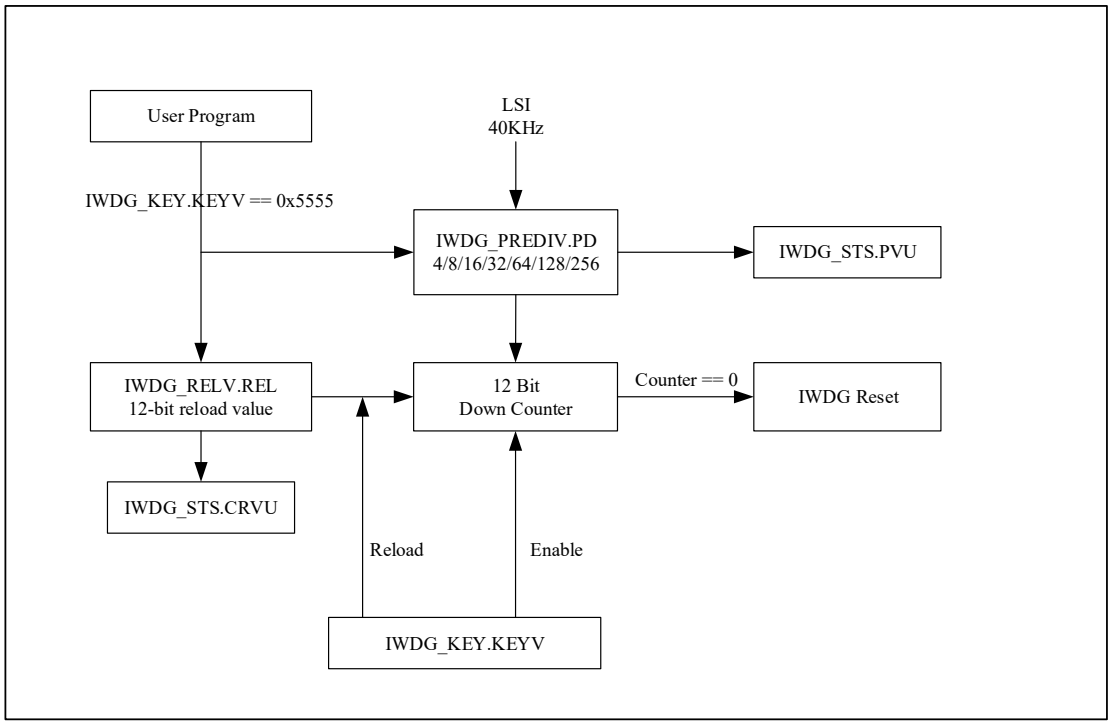
16.3 Functional description

Figure 16-1 Functional block diagram of the independent watchdog module



Note: Watchdog function is in V_{DD} power supply area, and it can still work normally in SLEEP, STOP0, STOP2 and STANDBY modes.

To enable IWDG, we need to write 0xCCCC to IWDG_KEY.KEYV[15:0] bits. Counter starts counting down from reset value (0xFFF). When counter count to 0x000, it generates a reset signal (IWDG_RESET) to MCU. Other than that, as long as 0xAAAA (reload request) is write to IWDG_KEY.KEYV[15:0] bits before reset, the counter value is set to the reload value in the IWDG_RELV.REL[11:0] bits and prevents the watchdog from resetting the entire device.

If the "hardware watchdog timer" function is enabled through the selection byte, the watchdog will automatically start running after the system is powered on and will generate a system reset, unless the software reloads the counter before it reaches ‘0’.

16.3.1 Register access protection

IWDG_PREDIV and IWDG_RELV register are write protected. To modify the value of those two register, user needs to write 0x5555 to IWDG_KEY.KEYV[15:0] bits. Writing other value enables write protections again. IWDG_STS.PVU indicates whether the pre-scaler value update is on going. IWDG_STS.CRVU indicates whether the IWDG is updating the reload value. The hardware sets the IWDG_STS.PVU bit and/or IWDG_STS.CRVU bit when the pre-scaler value and/or reload value is updating. After the pre-scaler value and/or reload value update is complete, the hardware clears the IWDG_STS.PVU bit and/or IWDG_STS.CRVU bit.

The reload operation (IWDG_KEY.KEYV[15:0] configured with value of 0xAAAA) will also cause the registers to become write protected again.

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16.3.2 Debug mode

In debug mode (Cortex-M4 core stops), IWDG counter will either continue to work normally or stops, depending on DBG_CTRL.IWDG_STOP bit in debug module. If this bit is set to '1', the counter stops. The counter works normally when the bit is '0'. See the chapter on debugging module for details 29.3.2.

16.4 User interface

IWDG module user interface contains 4 registers: Key Register (IWDG_KEY), Pre-scale Register (IWDG_PREDIV), Reload Register (IWDG_RELV) and Status Register (IWDG_STS).

16.4.1 Operate flow

When IWDG is enable from reset from software (write 0xAAAA to IWDG_KEY.KEYV[15:0] bits) or hardware (clear WDG_SW bit). It starts counting down from 0xFFF. Down counting gap is determined by pre-scale LSI clock. Once the counter is reloaded, each new round will start from the value in IWDG_RELV.REL[11:0] instead of 0xFFF.

When program is running normally, software needs to feed IWDG before counter reaches 0 and start a new round of down counting. When counter reach 0, this indicates program malfunction. IWDG generates reset signal under this circumstance.

If user wants to configure IWDG pre-scale and reload value register, it needs to write 0x5555 to IWDG_KEY.KEYV[15:0] first. Then confirm IWDG_STS.CRVU bit and IWDG_STS.PVU bit. IWDG_STS.CRVU bit indicates reload value update is ongoing, IWDG_STS.PVU indicates Pre-scale divider ratio is updating. Only when those two bit are 0 then user can update corresponding value. When update is on-going, hardware sets corresponding bit to 1. At this time, reading IWDG_PREDIV.PD[2:0] or IWDG_RELV.REL[11:0] is invalid since data needs sync to LSI clock domain. The value read from IWDG_PREDIV.PD[2:0] or IWDG_RELV.REL[11:0] will be valid after hardware clears the IWDG_STS.PVU bit or IWDG_STS.CRVU bit.

If the application uses more than one reload value or pre-scaler value, it must wait until the IWDG_STS.CRVU bit is reset before changing the reload value, the same as changing the pre-scaler value. However, after updating the pre-scale and/or the reload value, it is not necessary to wait until IWDG_STS.CRVU bit or IWDG_STS.PVU bit are reset before continuing code execution (even in case of low-power mode entry, the write operation is taken into account and will complete).

Pre-scale register and reload register controls the time that generates reset, as shown in Table 16-1.

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Table 16-1 IWDG counting maximum and minimum reset time

Pre-scale factor	PD[2:0]	Minimum（ms） RL[11:0]=0	Maximum（ms） RL[11:0]=0xFFF
/4	000	0.1	409.6
/8	001	0.2	819.2
/16	010	0.4	1638.4
/32	011	0.8	3276.8
/64	100	1.6	6553.6
/128	101	3.2	13107.2
/256	11x	6.4	26214.4

16.4.2 IWDG configuration flow

Software flow:

1. Write 0x5555 to IWDG_KEY.KEYV[15:0] bits to enable write access of IWDG_PREDIV and IWDG_RELV registers.
2. Check IWDG_STS.PVU bit or IWDG_STS.CRVU bit, if they are 0, continue next step.
3. Configure IWDG_PREDIV.PD[2:0] bits to select pre-scale value.
4. Configure IWDG_RELV.REL[11:0] bits reload value.
5. Writing 0xAAAA to IWDG_KEY.KEYV[15:0] bits to upload counter with reload value.
6. Enable watchdog by software or hardware writing 0xCCCC to IWDG_KEY.KEYV[15:0] bits.

If user wants change pre-scale and reload value, repeat step 1~5. If not, just feed the dog with step 5.

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16.5 IWDG registers

16.5.1 IWDG register overview

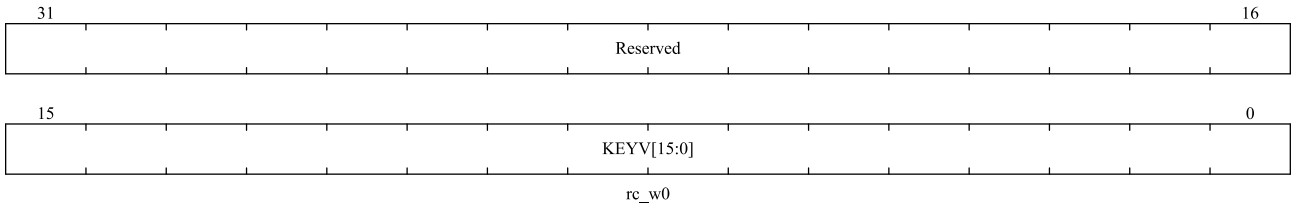
Table 16-2 IWDG register overview

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x00	IWDG_KEY	Reserved																KEYV[15:0]															
	Reset value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x04	IWDG_PREDIV	Reserved																													PD[2:0]		
	Reset value																														0	0	0
0x08	IWDG_RELV	Reserved																REL[11:0]															
	Reset value																	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
0x0C	IWDG_STS	Reserved																														CRVU	PVU
	Reset value																															0	0

16.5.2 IWDG key register (IWDG_KEY)

Address offset: 0x00

Reset value: 0x00000000



Bit field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained.
15:0	KEYV[15:0]	Key value register: only certain value will serve particular function 0xCCCC: Start watch dog counter, does not have any effect if hardware watchdog is enable, (if hardware watchdog is selected, it is not limited by this command word) 0xAAAA: Reload counter with REL value in IWDG_RELV register to prevent reset. 0x5555: Disable write protection of IWDG_PREDIV and IWDG_RELV register

16.5.3 IWDG pre-scaler register (IWDG_PREDIV)

Address offset: 0x04

Reset value: 0x00000000

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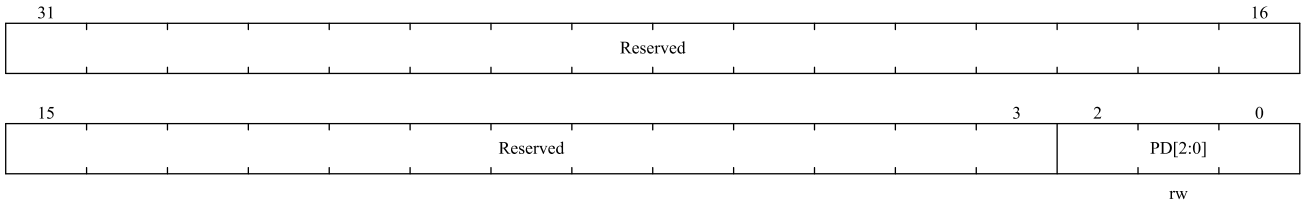
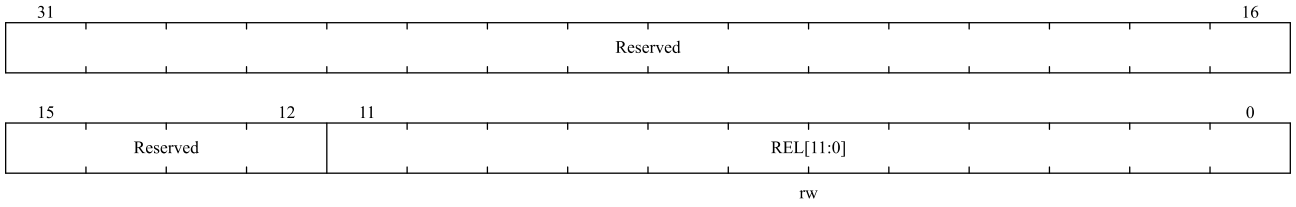


Bit field	Name	Description
31:3	Reserved	Reserved, the reset value must be maintained.
2:0	PD[2:0]	Pre-frequency division factor Pre-scaler divider: with write access protection when IWDG_KEY.KEYV[15:0] is not 0x5555. The IWDG_STS.PVU bit must be 0 otherwise PD [2:0] value cannot be changed. Divide number is as follow: 000: divider /4 001: divider /8 010: divider /16 011: divider /32 100: divider /64 101: divider /128 Other : divider /256 *Note: Reading this register will return the pre-divided value from the VDD voltage domain. If a write operation is in progress, the read-back value may be invalid. Therefore, the read value is valid only when the IWDG_STS.PVU bit is '0'.*

16.5.4 IWDG reload register (IWDG_RELV)

Address offset: 0x08

Reset value: 0x00000FFF



Bit field	Name	Description
31:12	Reserved	Reserved, the reset value must be maintained.

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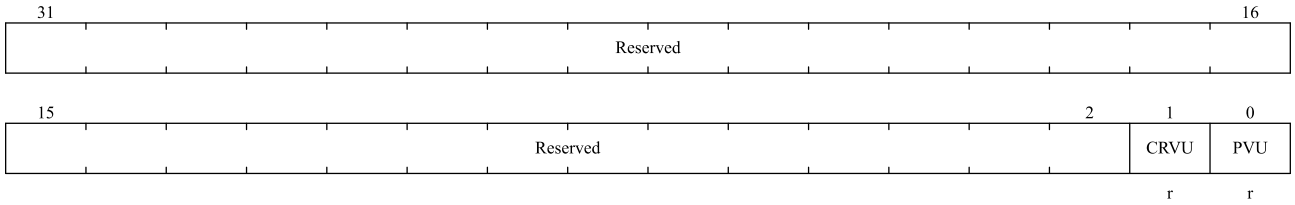
Bit field	Name	Description
11:0	REL[11:0]	Watchdog counter reload value. With write protection. Defines the reload value of the watchdog counter, which is loaded to the counter every time 0xAAAA is written to IWDG_KEY.KEYV[15:0] bits. The counter then starts to count down from this value. The watchdog timeout period can be calculated from this reloading value and the clock pre-scaler value, refer to Table 16-1。 This register can only be modified when the IWDG_STS.CRVU bit is '0'. *Note: Reading this register will return the reload value from the VDD voltage domain. If a write operation is in progress, the read-back value may be invalid. Therefore, the read value is valid only when the IWDG_STS.CRVU bit is '0'.*

16.5.5 IWDG status register (IWDG_STS)

Address offset: 0x0C

Reset value: 0x00000000



Bit field	Name	Description
31:2	Reserved	Reserved, the reset value must be maintained.
1	CRVU	Watchdog reload value update Reload Value Update: this bit indicates an update of reload value is ongoing. Set by hardware and clear by hardware. Software can only try to change IWDG_RELV.REL[11:0] value when IWDG_KEY.KEYV[15:0] bits' value is 0x5555 and this bit is 0.
0	PVU	Watchdog pre-scaler value update Pre-scaler Value Update: this bit indicates an update of pre-scaler value is ongoing. Set by hardware and clear by hardware. Software can only try to change IWDG_PREDIV.PD[2:0] value when IWDG_KEY.KEYV[15:0] bits' value is 0x5555 and this bit is 0.

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17 Window Watchdog (WWDG)

17.1 Introduction

The clock of the window watchdog (WWDG) is obtained by dividing the APB1 clock frequency by 4096, and whether the program operation is abnormal is detected through the configuration of the time window. Therefore, WWDG is suitable for precise timing, and is often used to monitor software failures caused by external disturbances or unforeseen logic conditions that cause an application to deviate from its normal operating sequence. A system reset occurs when the WWDG down counter is refreshed before reaching the window register value or after the WWDG_CTRL.T6 bit becomes 0.

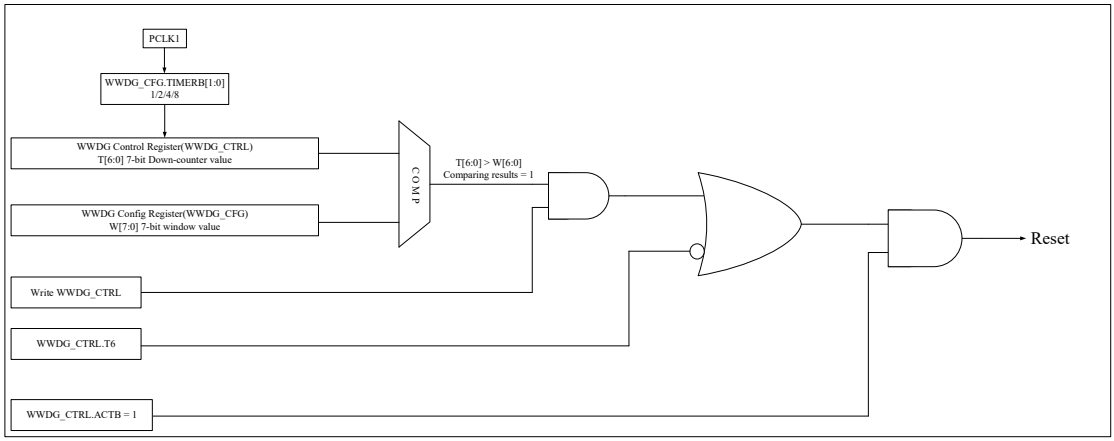
17.2 Main Features

- 7-bit independent running down counter programmable
- After WWDG is enabled, a reset occurs under the following conditions
  - The value of the decremented counter is less than 0x40.
  - When the decremented counter value is greater than the value of the window register, it is reloaded.
- Early wake-up interrupt: If the watchdog is started and the interrupt is enabled, wake-up interrupt (WWDG_CFG.EWINT) will be generated when the count value reaches 0x40.

17.3 Function Description

If the watchdog is activated (the WWDG_CTRL.ACTB bit), when the 7-bit (WWDG_CTRL.T[6:0]) down-counter reaches 0x3F(WWDG_CTRL.T6 bit is cleared), or the software reloads the counter when the counter value is greater than the value of the window register, a system reset will be generated. In order to avoid system reset, the software must periodically refresh the counter value in the window during normal operation.

Figure 17-1 Watchdog block diagram



Set the WWDG_CTRL.ACTB bit to enable the watchdog, and thereafter, the WWDG will remain on until reset occurs. The 7-bit down-counter runs independently, and the counter keeps counting down whether WWDG is enabled or not. Therefore, before enabling the watchdog, you need to set WWDG_CTRL.T [6] bit to 1, preventing reset right after enable. The pre-scaler value set by the clock APB1 and WWDG_CFG.TIMERB[1:0] bits determine the decrement speed of the counter. WWDG_CFG.W[6:0] bits set the upper limit of the window.

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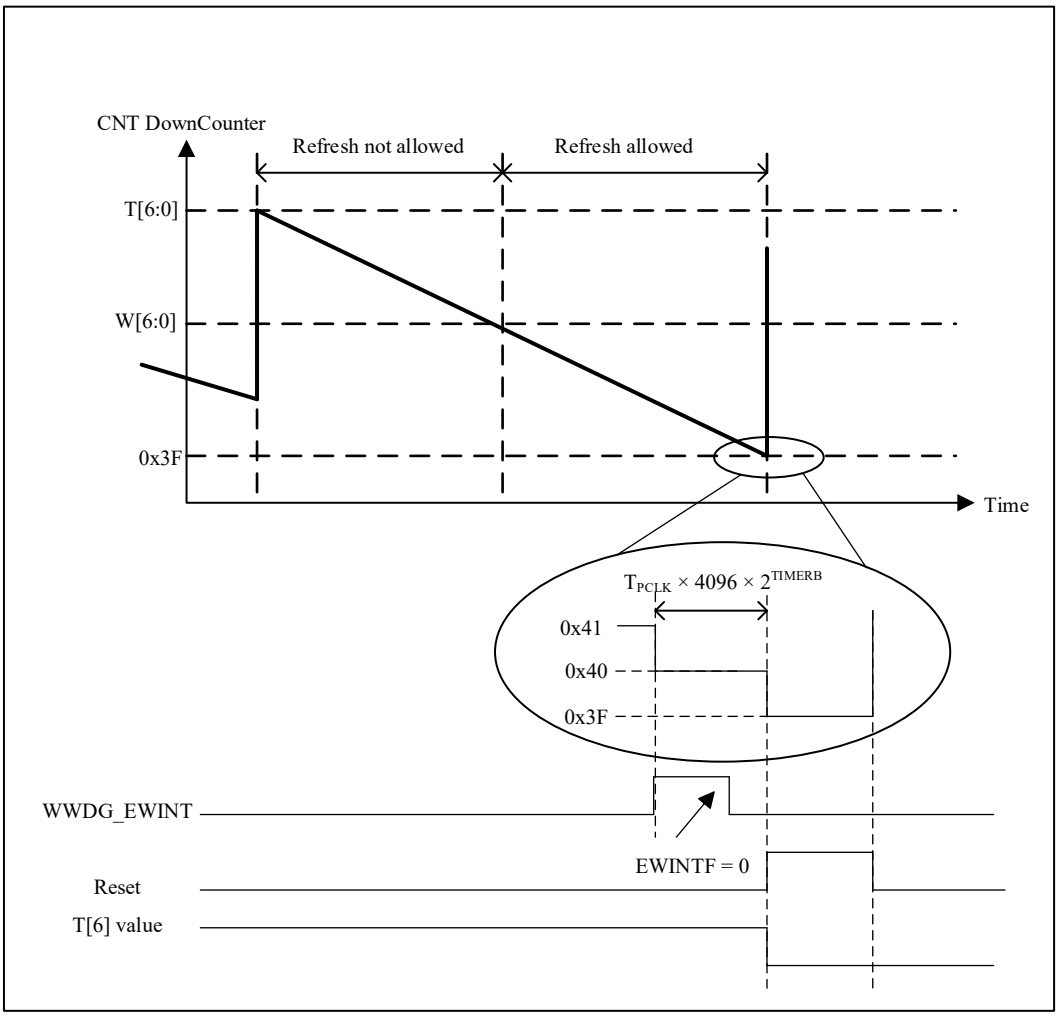
When the down-counter is refreshed before reaching the window register value or after WWDG_CTRL.T6 bit becomes 0, a system reset will be generated. Figure 17-2 describes the working process of the window register.

Set the WWDG_CFG.EWINT bit to enable early wake-up interrupt. When the count-down counter reaches 0x40, an interrupt will be generated. You can analyze the cause of software failure or save important data in the corresponding interrupt service routine (ISR), and reload the counter to prevent WWDG from resetting. Write '0' to the WWDG_STS.EWINTF bit to clear the interrupt.

17.4 Timing for refresh watchdog and interrupt generation

Figure 17-2 Refresh window and interrupt timing of WWDG



Watchdog refreshing window is between WWDG_CFG.W[6:0] value (maximum value 0x7F) and 0x3F, refresh outside this window will generates reset request to MCU. Counter count down from 0x7F to 0x3F using scaled APB1 clock, the maximum counting time and minimum counting time is shown in Table 17-1 (assuming APB1 clock 36 MHz) with calculate equation:

$$T_{WWDG} = T_{PCLK1} \times 4096 \times 2^{TIMERB} \times (T[5:0] + 1)$$

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In which:

T_{WWDG}: WWDG timeout

T_{PCLK1}:APB1 clock interval in ms

Minimum-maximum timeout value at PCLK1 = 36MHz

Table 17-1 Maximum and minimum counting time of WWDG

TIMERB	Maximum counting (ms)	Minimum counting (ms)
0	7.28	0.113
1	14.56	0.227
2	29.12	0.455
3	58.25	0.910

17.5 Debug mode

In debug mode (Cortex-M4 core stops), WWDG counter will either continue to work normally or stops, depending on DBG_CTRL.WWDG_STOP bit in debug module. If this bit is set to '1', the counter stops. The counter works normally when the bit is '0'. See the chapter on debugging module for details 29.3.2.

17.6 User interface

17.6.1 WWDG configuration flow

1) Configure RCC_APB1PCLKEN.WWDGEN[11] bit to enable the clock of WWDG module;
2) Software setting WWDG_CFG.TIMERB[8:7] bits to configure pre-scale factor for WWDG.
3) Software configure WWDG_CTRL.T[6:0] bits, setting starting value of counter. Need to set WWDG_CTRL.T[6] bit to 1, preventing reset right after enable.
4) Configure WWDG_CFG.W[6:0] bits to configure upper boundary window value;
5) Setting WWDG_CTRL.ACTB[7] bit to enable WWDG;
6) Software operates WWDG_STS.EWINTF[0] bit to clear wake-up interrupt flag;
7) Configure WWDG_CFG.EWINT[9] bit to enable early wake-up interrupt.

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17.7 WWDG registers

17.7.1 WWDG register overview

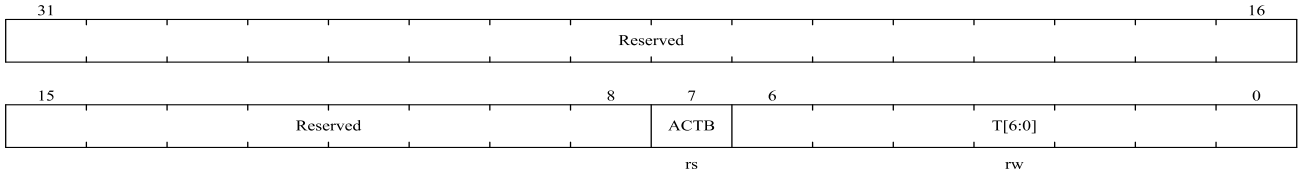
Table 17-2 WWDG register overview

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
000h	WWDG_CTRL	Reserved																								ACTB	T[6:0]						
	Reset Value																									0	1	1	1	1	1	1	1
004h	WWDG_CFG	Reserved																						EWINT	TIMERB [1:0]		W[6:0]						
	Reset Value																							0	0	0	1	1	1	1	1	1	1
008h	WWDG_STS	Reserved																															EWINTF
	Reset Value																																0

17.7.2 WWDG control register (WWDG_CTRL)

Address offset : 0x00

Reset value : 0x0000007F



Bit field	Name	Description
31:8	Reserved	Reserved, the reset value must be maintained.
7	ACTB	Activation bit When ACTB=1, the watchdog can generate a reset. This bit is set by software and only cleared by hardware after a reset. When ACTB = 1, the watchdog can generate a reset. 0: Disable watchdog 1: Enable watchdog
6:0	T[13:0]	These bits contain the value of the watchdog counter. It is decremented every (4096x2^{TIMERB}) PCLK1 cycles. A reset is produced when it rolls over from 0x40 to 0x3F (T6 becomes cleared).

17.7.3 WWDG config register (WWDG_CFG)

Address offset: 0x04

Reset value : 0x0000007F

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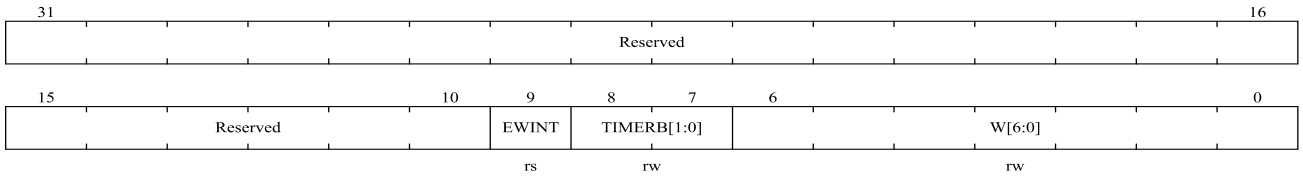
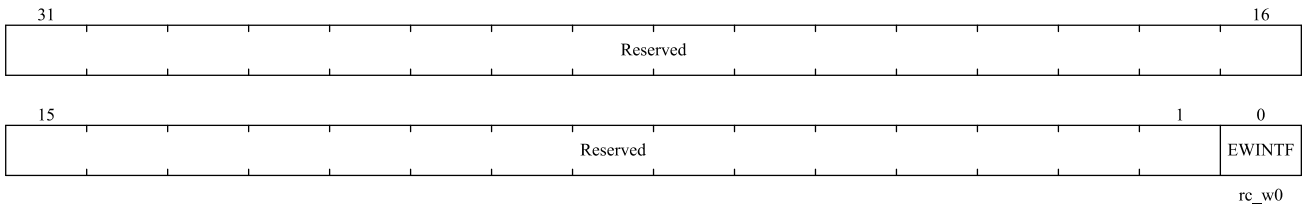


Bit field	Name	Description
31:10	Reserved	Reserved, the reset value must be maintained.
9	EWINT	Early wake-up interrupt When set, an interrupt occurs whenever the counter reaches the value 0x40. This interrupt is only cleared by hardware after a reset.
8:7	TIMERB[1:0]	Timer base. The time base of the pre-scaler can be modified as follows: 00: CK Counter Clock (PCLK1 div 4096) div 1 01: CK Counter Clock (PCLK1 div 4096) div 2 10: CK Counter Clock (PCLK1 div 4096) div 4 11: CK Counter Clock (PCLK1 div 4096) div 8
6:0	W[6:0]	7-bit window value These bits contain the window value to be compared to the down counter.

17.7.4 WWDG status register (WWDG_STS)

Address offset: 0x08

Reset value : 0x0000



Bit field	Name	Description
31:1	Reserved	Reserved, the reset value must be maintained.
0	EWINTF	Early wake-up interrupt flag This bit is set by hardware when the counter has reached the value 0x40. It must be cleared by software by writing ‘0’. A write of ‘1’ has no effect. This bit is also set if the interrupt is not enabled.

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18 SDIO Interface（SDIO）

18.1 Main Features of SDIO

SDIO interface defines SD card, SD I/O card, Multimedia Card (MMC) host interface. It provides data transfer between AHB peripheral bus and SD memory card, SDIO card, Multimedia Card (MMC) and CE-ATA devices. Among them, the supported multimedia card system specifications are published by the MMCA technical committee and can be obtained on the website of the Multimedia Card Association (www.mmca.org), and the supported CE-ATA system specifications can be found in the CE-ATA working group. Available on the website (www.ce-ata.org), supported SD memory cards and SD I/O card system specifications are available through the SD Card Association website (www.sdcard.org).

Main features of SDIO are as follows:

- SD card: fully compatible with SD memory card specification version 2.0.
- SD I/O: Fully compatible with SD I/O card specification version 2.0, there are two different data bus modes: 1-bit (default) and 4-bit.
- MMC: Fully compatible with Multimedia Card System Specification Version 4.2 and earlier versions. There are three different data bus modes: 1-bit (default), 4-bit and 8-bit.
- CE-ATA: fully compatible with CE-ATA digital protocol version 1.1, fully supports CE-ATA function.
- Up to 48MHz data transfer rate in 8-bit data bus mode.
- Support interrupt and DMA request.
- Supports data and command output enable signals for controlling external bidirectional drivers.

Notices:

1. SDIO has no SPI compatible communication mode.

2. In version 2.11 of the Multimedia Card System Specification, it is defined that the SD memory card protocol only supports the I/O part of the SD card or composite card in I/O mode, and does not support many required commands in the SD storage device, such as erasing etc. some commands don't work in SDI/O devices, so SDIO doesn't support these commands either. In addition, some commands are different in SD memory card and SD I/O card, and SDIO does not support these commands.

SDIO supports only one SD/SDIO/MMC 4.2 card or CE-ATA device at a time, but can support multiple MMC version 4.1 or earlier cards.

18.2 SDIO bus topology

Communication on the SDIO bus is achieved by transferring commands and data. After power-on reset, the host must

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initialize the card through a special message-based bus protocol. Each message is a command/response structure, additionally, some messages have data tokens. Each part of the message is described in detail as follows:

- Command: The command is serially transmitted on the CMD line and is a token to initiate an operation, sent from the host to the card
- Response: A response is serially transmitted on the CMD line, sent from the card to the host in response to a previously received command.
- Data: Data is transmitted through the data line. Data can be transferred from the card to the host or from the host to the card. The number of data lines used for data transfer can be 1 (SDIO_DAT0), 4 (SDIO_DAT[3:0]) or 8 (SDIO_DAT[7:0]).

The structure of commands, responses and data blocks is described in the card functional description chapter. A data transfer is a bus operation. A normal operation always consists of a command and response. Additionally, some operations have a data token. There are other operations that include their information directly in the command or response structure. In this case, the operation has no data token.

There are two types of data transfer commands: block and stream. Data transmitted on SD/SDIO memory cards and CE-ATA devices is transmitted in the form of data blocks; data transmitted on MMC is transmitted in the form of data blocks or data streams;

Data streams and data block transfers are defined as follows:

- Data flow: The command initiates a continuous data flow, and the data transmission is terminated only when a stop command appears on the CMD signal line. This mode minimizes command overhead (only MMC is supported).
- Data block: The command successfully sends a data block followed by a CRC check. Read and write operations allow single or multiple block transfers. As with continuous read, a multi-block transfer is terminated when a stop command appears on the CMD signal line.

The basic operations on the SDIO bus are command/response operations, and this type of bus transaction passes their information directly in a command or response structure. In addition, some operations have data tokens. Data transfer between the card and the device is done through blocks. Each transmission type is shown in the following figure:

Figure 18-1 SDIO "No Response" and "No Data" operations

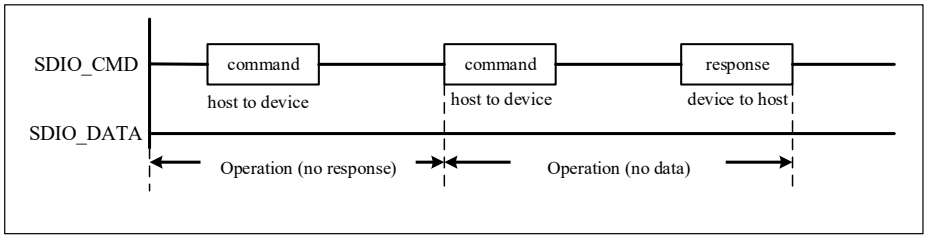

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Figure 18-2 SDIO (multi) data block read operation

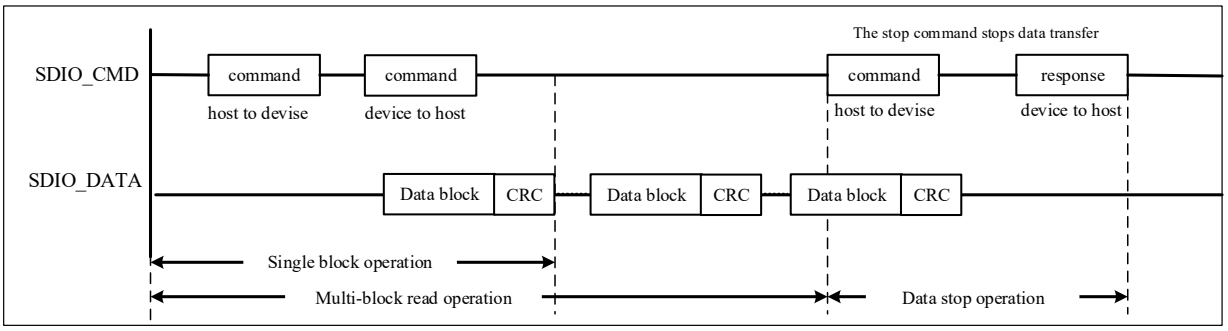
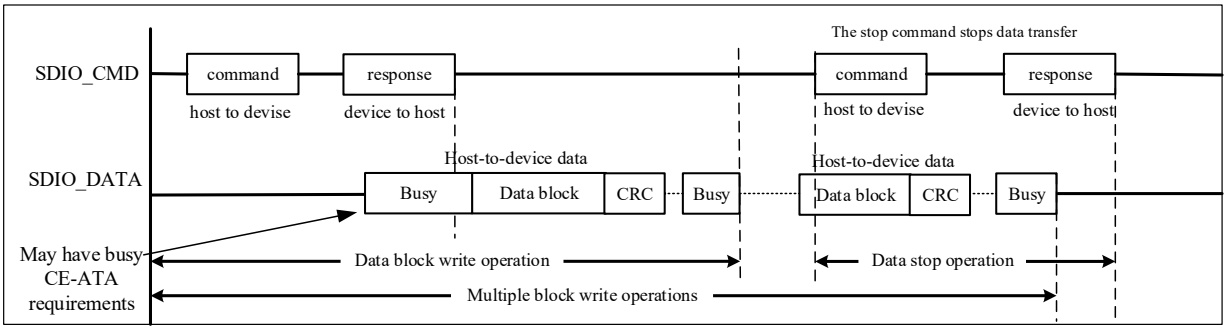


Figure 18-3 SDIO (multiple) data block write operation



Note: When there is a Busy signal, SDIO (SDIO_DAT0 is pulled low) will not send any data.

Figure 18-4 SDIO continuous read operation

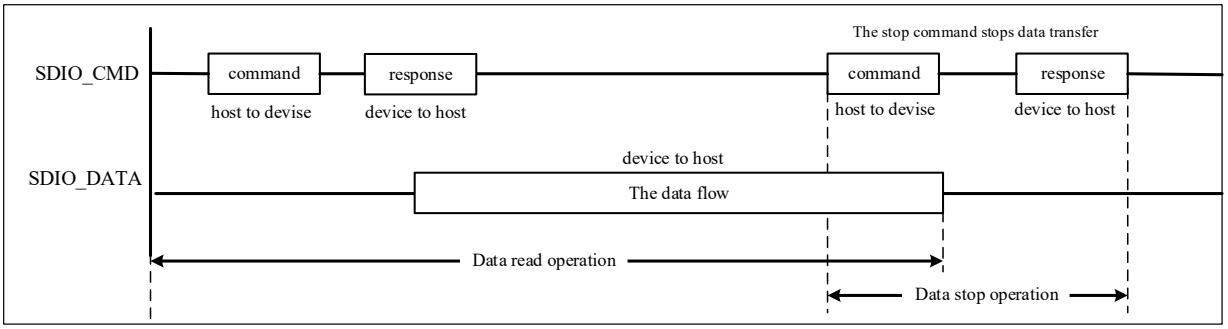
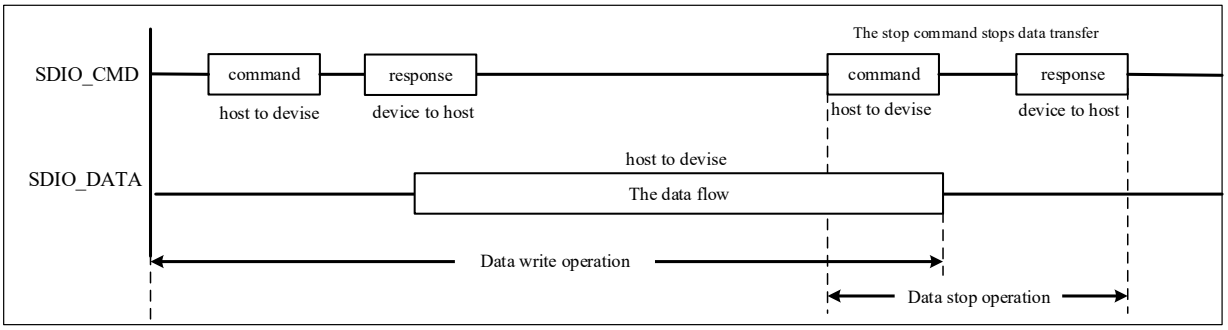


Figure 18-5 SDIO continuous write operation



18.3 SDIO function description

Figure 18-6 is a block diagram of SDIO structure:

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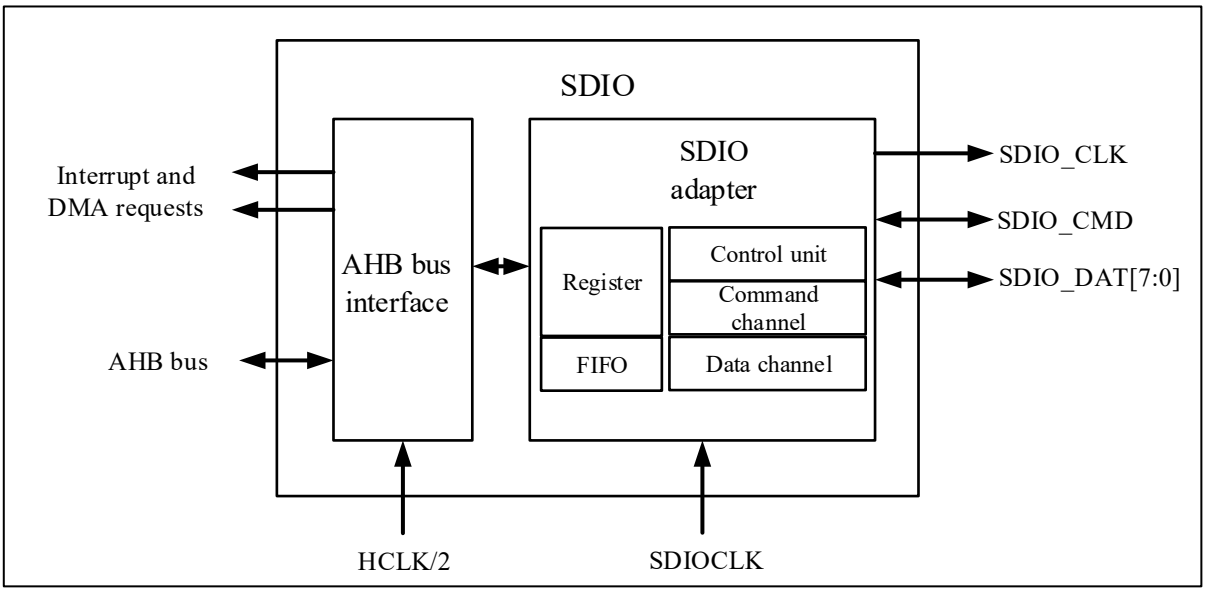
- SDIO adapter: It consists of control unit, command unit and data unit. The control unit generates a clock signal, and the command unit and data unit manage the transmission of commands and data respectively, thereby realizing the related functions of the MMC/SD/SD I/O card. .
- AHB bus interface: used to operate the FIFO unit of the register control data transmission in the SDIO adapter module, and generate interrupt and DMA request signals.

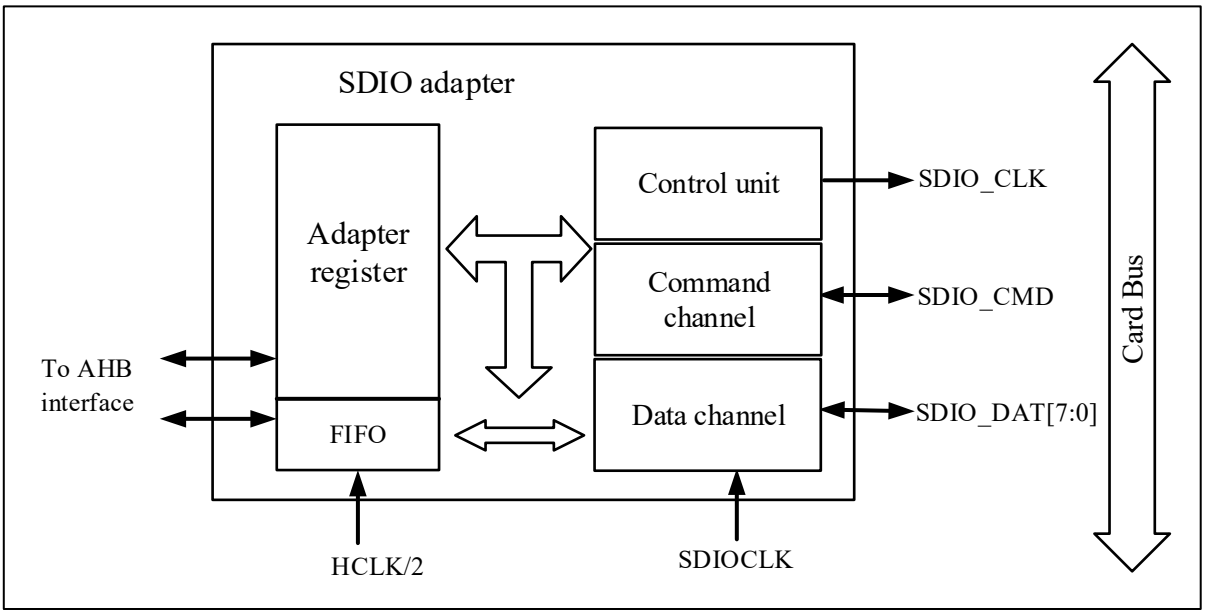
Figure 18-6 SDIO block diagram



18.3.1 SDIO adapter

The following figure is a simplified block diagram of the SDIO adapter:

Figure 18-7 SDIO adapter



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The HCLK/2 of the AHB bus is used as the clock of the adapter register and FIFO, and the SDIOCLK(equal to HCLK) is used as the clock of the control unit, command channel and data channel.

The SDIO adapter includes five parts: control unit, adapter register module, command unit, data unit and data FIFO. The signals output to the card bus are as follows:

- SDIO_DAT[7:0]: The data signal line uses push-pull mode. By default, only SDIO_DAT0 is used for data transfer after power-on or reset. The SDIO adapter can configure a wider data bus for data transfer after initializing the host, using DAT0-DAT3 or DAT0-DAT7 (only for MMC V4.2). Note that the protocol of MMC version V3.31 and previous versions only supports 1-bit data line (only SDIO_DAT0 can be used). When an SD or SD I/O card is connected to the bus, SDIO_DAT0 or SDIO_DAT[3:0] can be used by the host to configure data transfers.
- SDIO_CMD, two operating modes:
  - Open-drain mode for initialization (only for MMC version V3.31 or earlier)
  - Push-pull mode for command transfer (SD/SD I/O cards and MMC V4.2 also use push-pull drive during initialization)
- SDIO_CLK: The clock provided to the card by the SDIO controller. One bit of command or data is sent directly on the command line (SDIO_CMD) and all data lines per clock cycle. The variation range of the clock frequency of different cards is different, as follows:
  - MMC V3.31 protocol, optional clock frequency between 0MHz and 20MHz;
  - MMC V4.0/4.2 protocol, optional clock frequency between 0MHz and 48MHz;
  - SD or SD I/O card, optional clock frequency between 0MHz and 25MHz.

The following table is the MMC/SD/SD I/O card bus pin definition:

Table 18-1 MMC/SD/SD I/O Card bus pin definition

Pin	Direction	Description
SDIO_CLK	Output	MMC/SD/SDIO card clock, clock line from host to card
SDIO_CMD	Bidirectional	MMC/SD/SDIO card command, bidirectional command/response signal line
SDIO_DAT[7:0]	Bidirectional	MMC/SD/SDIO card data, bidirectional data bus

18.3.1.1 Adapter register block

The adapter register block contains all SDIO related registers.

18.3.1.2 Control unit

The control unit contains power management functions and clock management functions,which are used for the memory card identifcation, initialization,clock control etc.

Power management is controlled by the SDIO_PWRCTRL register to achieve power down and power up. There are three power phases: power off, power up, and power on.

Configure the power saving mode by setting SDIO_CLKCTRL.PWRCFG bit to turn off SDIO_CLK when the bus is idle.When SDIO_CLKCTRL.CLKBYP bit is 0, SDIO_CLK is obtained by dividing the frequency of SDIOCLK; when SDIO_CLKCTRL.CLKBYP bit is 1, SDIO_CLK is directly SDIOCLK.

Hardware clock control is enabled by setting the HWCLKEN bit in the SDIO_CLKCTRL register. This function is

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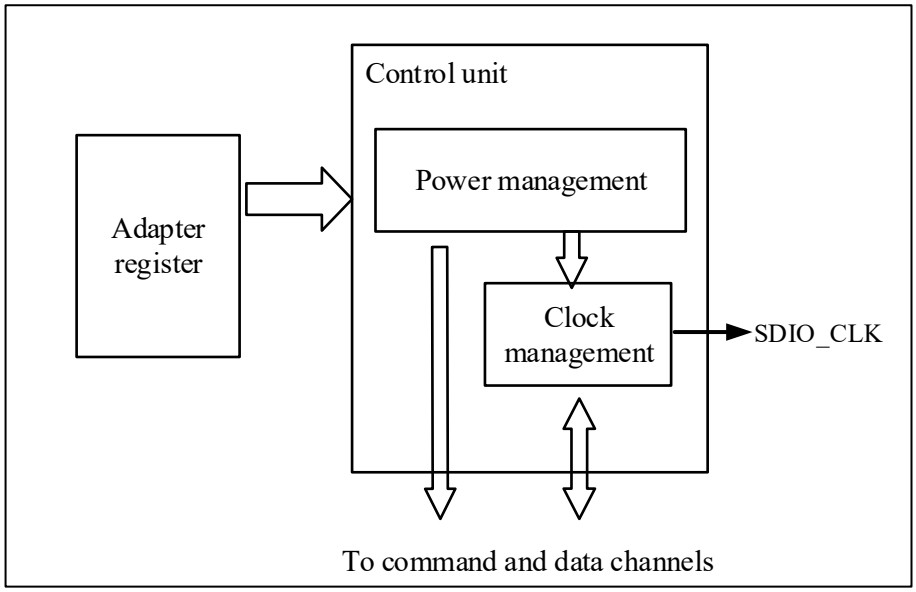
used to avoid FIFO underflow and overflow errors. The hardware controls the switch of SDIO_CLK according to whether the system bus is busy. When the FIFO cannot receive or transmit data, the host will turn off SDIO_CLK and freeze the SDIO state machine to avoid related errors. Only the state machine can be frozen, but the AHB interface is still working. Therefore, the FIFO can be accessed through the AHB bus.

The clock management subunit generates and controls the SDIO_CLK signal. SDIO_CLK output supports: clock divider or clock bypass mode.

SDIO_CLK clock not output in these three cases after reset, during power-off and power-on phases, or when power-saving mode is enabled and the card bus is idle (8 clock cycles after the command channel and data channel subunits enter the idle phase).

Figure 18-8 Control unit



18.3.1.3 Command unit

The command unit and the card send and receive commands. The data transfer flow of the command channel is controlled by the command state machine (CPSM). The command transfer begins after setting SDIO_CMDCTRL.CPSMEN bit to 1 and writing it once. First send a 48-bit command to the card through the SDIO_CMD line, one bit of data per SDIO_CLK. The 48-bit command contains 1 start bit, 1 transmit bit, 6-bit command index (defined SDIO_CMDCTRL.CMDIDX bits), 32-bit parameters (defined by SDIO_CMDARG), 7-bit CRC, and 1-bit stop bit. Then receive the response from the card when SDIO_CMDCTRL.CMDIDX bits is not 0b00 or 0b10. The response is divided into a 48-bit short response and a 136-bit long response, and the responses are stored in the SDIO_RESPONSE0~SDIO_RESPONSE 3 registers. The command unit can also generate command status flags, which are defined in the SDIO_STS register.

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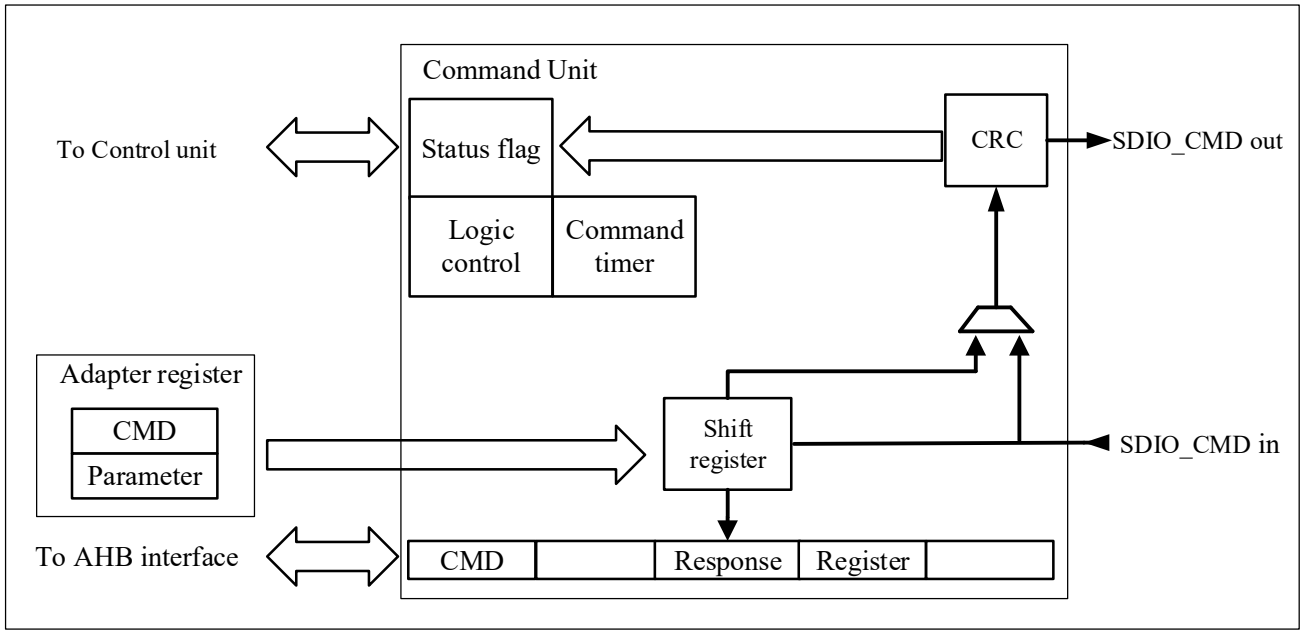
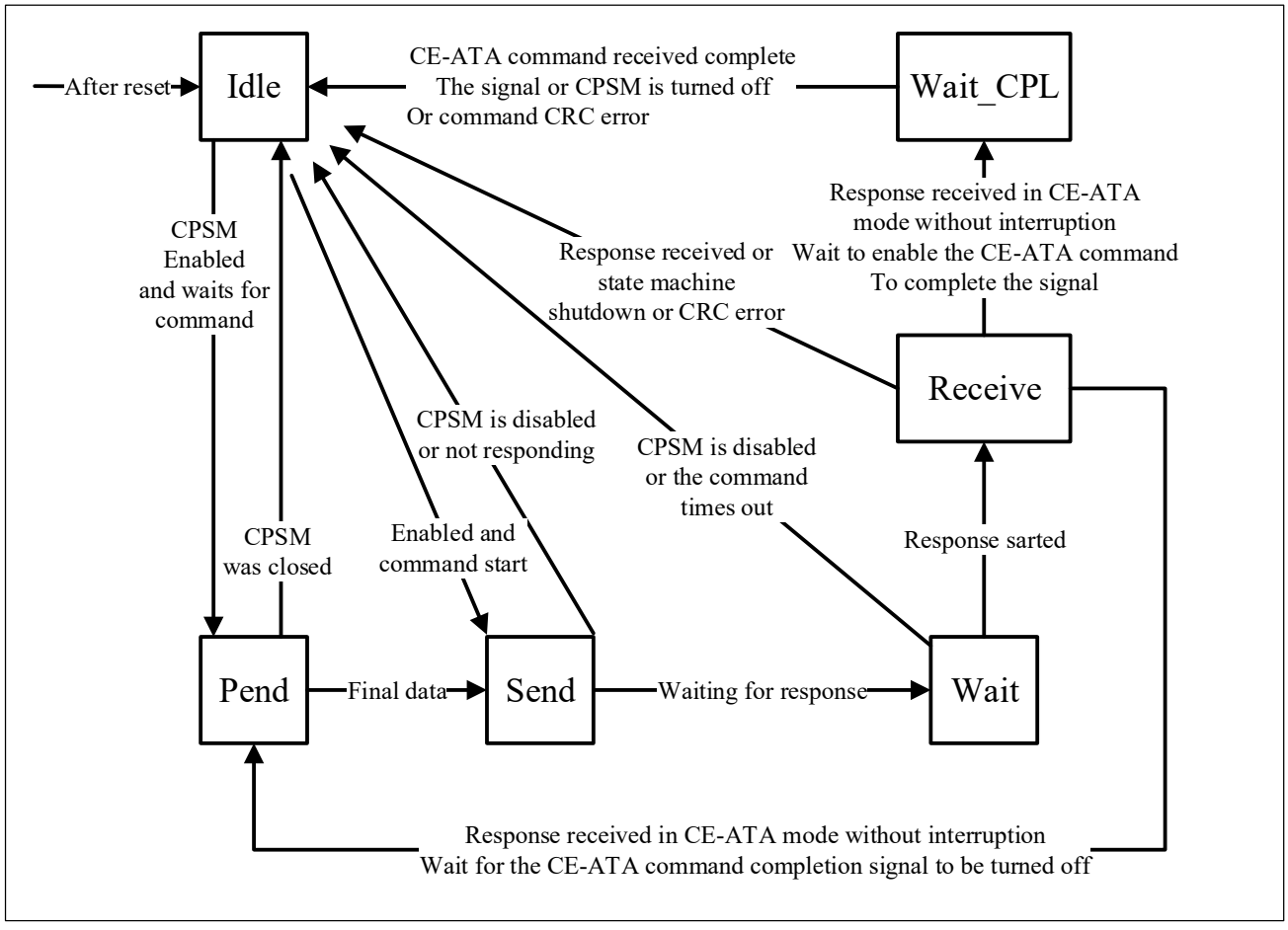
Figure 18-9 SDIO adapter command unit



- Command Path State Machine (CPSM)

Figure 18-10 Command Path State Machine (CPSM)



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- Idle

This state is an idle state. After the system is reset, the state is ready to send a command or the command state machine (CPSM) is turned off. All belong to the Idle state. When the command state machine (CPSM) is enabled, wait for the end of data transmission bit (SDIO_CMDCTRL.WDATEND) Enable or disable can enter the Pend state.

Note: The command state machine remains idle for at least 8 SDIO_CLK cycles to meet NCC and NRC timing constraints. NCC is the minimum time interval between two host commands, and NRC is the minimum time interval between a host command and a card response.

- Pend

This state is a pending state, waiting for the end of data transfer. When the data transmission is completed, the command state machine enters the Send state from the Pend state; when the command state machine (CPSM) is turned off, the CPSM enters the Idle state.

- Send

This state is the sending state, indicating that the command is being sent. If there is a response after the command is sent, the command state machine enters the Wait state, and if there is no response after the command is sent, the command state machine enters the Idle state.

- Wait

This state is a wait state, waiting for the response start bit. When entering the wait (Wait) state, the command timer starts to run; if a response is received, that is, the start bit is detected, the command state machine (CPSM) enters the Receive state, and when the command state machine (CPSM) enters the receiving (Receive) state Before a timeout occurred, set the timeout flag and enter the Idle state.

Note: The command timeout period is fixed at 64 SDIO_CLK clock cycles.

- Receive

This state is the receiving state, the response is received and the CRC is checked.

Receive a response in CE-ATA mode, disable the CE-ATA interrupt and wait for the CE-ATA device command completion signal to be enabled and then enter the Wait_CPL state.

Receive a response in CE-ATA mode, disable the CE-ATA interrupt and wait for the CE-ATA device command completion signal to be disable and then enter the Pend state.

The Idle state is entered when the CPSM is closed, a response is received, or the command CRC detection fails.

- Wait_CPL

In this state, wait for the CE-ATA device command completion signal, and enter the Idle state after receiving the CE-ATA command completion signal. It will also enter the Idle state when the CPSM is turned off or the command CRC check fails.

If the interrupt bit is set in the command register, the timer is turned off and the CPSM waits for an interrupt request from a certain card. If the pending bit is set in the command register, the CPSM enters the pending (Pend) state and waits for the CmdPend signal sent by the data channel subunit. When the CmdPend signal is detected, the CPSM enters the sending (Send) state, which will trigger the data counter to stop sending function of the command.

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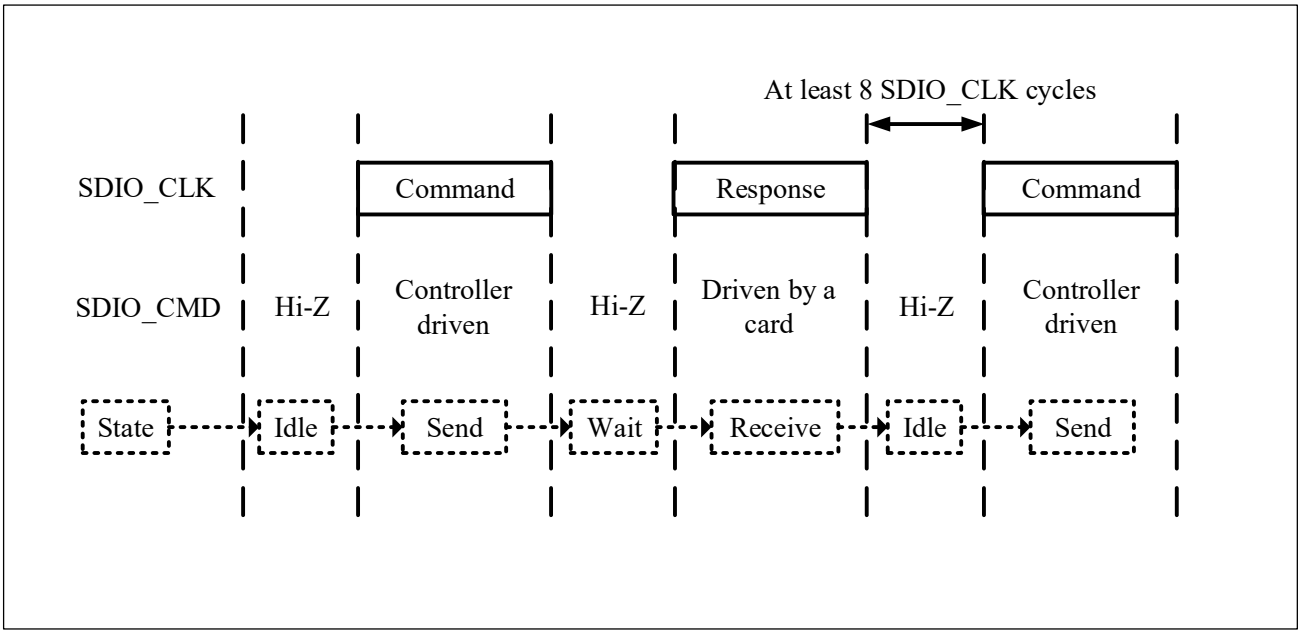
Figure 18-11 SDIO command transmission



- Command register

The 6-bit command index and command type sent to the card are stored in the command register; the command type (see Section 18.7.4) determines whether and what type of response (48-bit or 136-bit).

Table 18-2 Command Channel Status Flags

Flag	Description
SDIO_STS.CMDRESPRECV	CRC correct response
SDIO_STS.CCRCERR	CRC error response
SDIO_STS.CMDSEND	Command (command that does not require a response) has been sent
SDIO_STS.CMDTIMEOUT	Response timeout
SDIO_STS.CMDRUN	Command transfer in progress

The CRC generator calculates the CRC checksum of all bits preceding the CRC code, including start bits, transmit bits, command index, and command parameters (or card status). For the long response format, the CRC checksum is calculated from the first 120 bits of the CID or CSD; note that the start bit, transmission bits and 6 reserved bits in the long response format do not participate in the CRC calculation.

The CRC checksum is a 7-bit value:

CRC[6:0] = remainder [(M(x) * x7) / G(x)]

G(x) = x7 + x3 + 1

M(x) = (start bit) * x39 + ... + (last bit before CRC) * x0, or

M(x) = (start bit) * x119 + ... + (last bit before CRC) * x0.

18.3.1.4 Data channel

The data between the host and the card is transmitted through the data channel.

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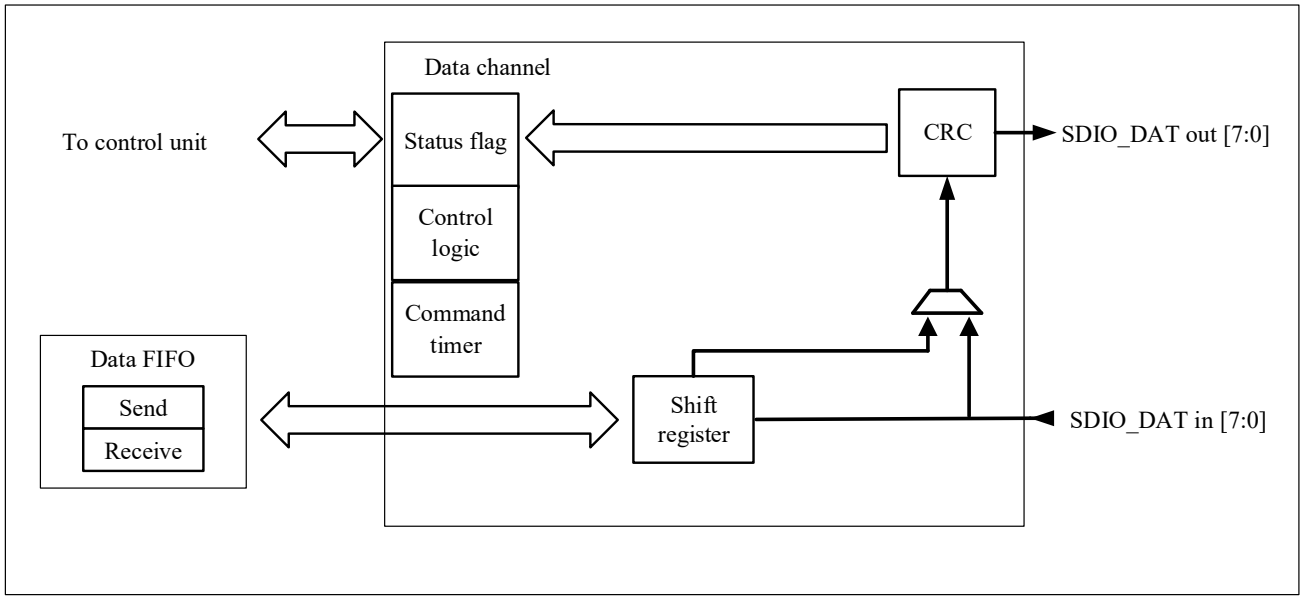
Figure 18-12 Data Channel



The data bus width of the card can be configured in the clock control register (SDIO_CLKCTRL). When the data width is 4 bits (SDIO_ CLKCTRL.BUSMODE bit is 0b01), 4 bits of data will be transmitted on the four data signal lines SDIO_DAT[3:0] in each clock cycle; when the data width is 8 bits (SDIO_ CLKCTRL.BUSMODE bit is 0b10), 8-bit data will be transmitted on the eight data signal lines SDIO_DAT[7:0] per clock cycle; when the data width is 1 bit (SDIO_CLKCTRL.BUSMODE bit is 0b00) or the bus mode is not selected , only 1 bit of data is transmitted on SDIO_DAT0 per clock cycle.

The data transmission flow is controlled by the Data Channel State Machine (DPSM). Data transfer begins after a write to the SDIO_DATCTRL register and setting the SDIO_DATCTRL.DATEN bit to 1. When the SDIO_DATCTRL.DATDIR bit is 0, the data is from the controller to the card, and the DPSM enters the Wait_S state. If there is data in the transmit FIFO, the DPSM enters the transmit state, and the data channel subunit starts to send data to the card; when the DATDIR bit is When 1, the data is from the card to the controller, the DPSM enters the Wait_R state, when the start bit is received, the DPSM enters the receiving state and waits for the start bit, and the data channel subunit starts to receive data from the card. Data units can also generate data status flags (defined in the SDIO_STS register).

18.3.1.5 Data path state machine (DPSM)

The data channel state machine (DPSM) operates at the SDIO_CLK frequency, and the card bus signal is synchronized with the rising edge of SDIO_CLK. DPSM has 6 states, as shown in the following figure:

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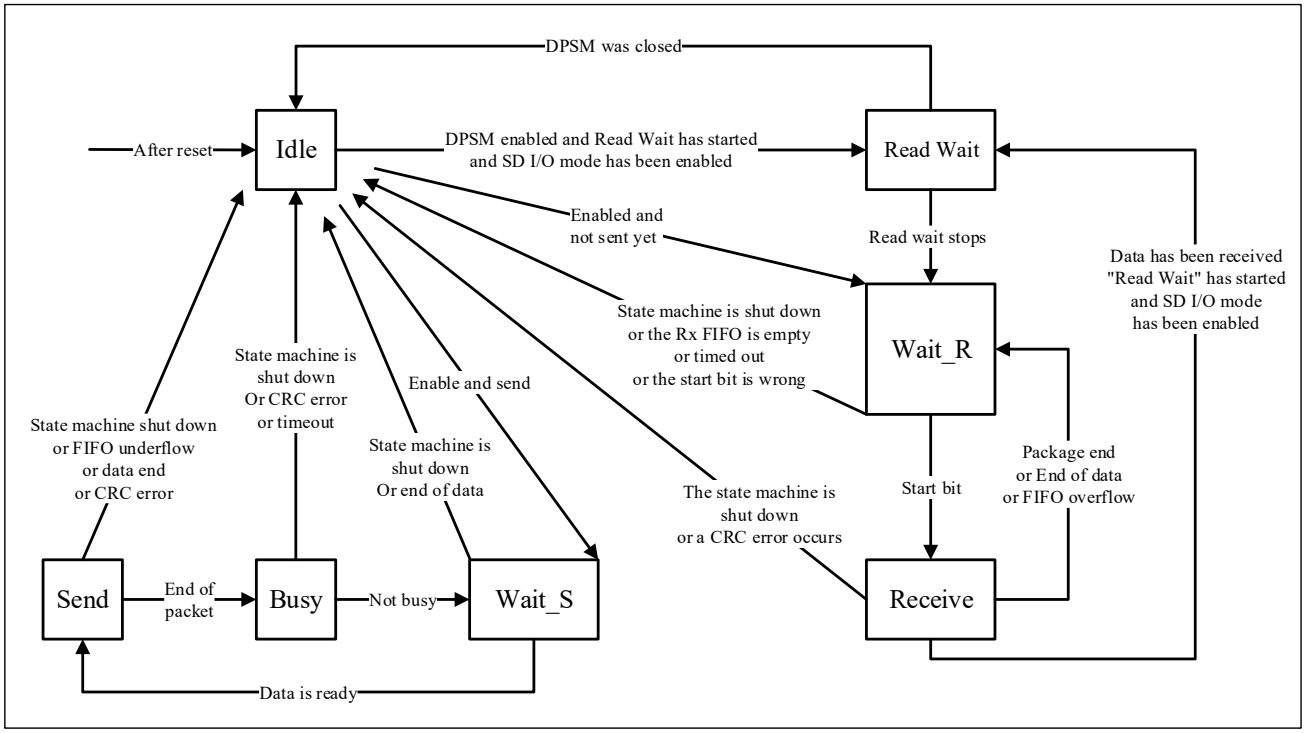
Figure 18-13 Data Path State Machine (DPSM)



- Idle:

  In this state, the data channel does not work, waiting to transmit and receive data, and the SDIO_DAT[7:0] output is in a high-impedance state. When the data control register is written and the enable bit is set, the DPSM loads a new value for the data counter, enters the Wait_S state when the data transfer direction is from the host to the card, and enters the Wait_R state when the data transfer direction is from the card to the host. The Read Wait state is entered when DPSM is enabled and a read wait has started and SD I/O mode is enabled.

- Wait_R:

  In this state, the DPSM waits for the start bit of the received data. If the data times out (counter equals 0, when the receive FIFO is empty) the DPSM enters the Idle state. If the data counter is not equal to 0, the DPSM waits for a start bit on SDIO_DAT; if the DPSM receives a start bit before the timeout, it enters the Receive state and loads the data block counter. If the DPSM times out before detecting a start bit, or if a start bit error occurs, the DPSM will go into the idle state and set the time-out status flag.

- Receive:

  In this state the DPSM receives the card's data and writes it to the data FIFO. Depending on the setting of the transfer mode bits in the data control register, the data transfer mode can be block transfer or stream transfer.

  – In block mode, when the data block counter reaches 0, the DPSM waits to receive the CRC code, if the received code matches the internally generated CRC code, the DPSM enters the Wait_R state, otherwise the CRC failure state flag is set and the DPSM enters the idle state state.

  – In streaming mode, when the data counter is not 0, the DPSM receives data; when the counter is 0, the remaining data in the shift register is written into the data FIFO, and the DPSM enters the Wait_R state. If a FIFO overflow error occurs, the DPSM sets the FIFO error flag and enters the idle state.

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- Wait_S:

  In this state, the DPSM waits for the data FIFO empty flag to be invalid or the end of the data transfer. If the data counter is 0, the DPSM enters the idle state; otherwise, the DPSM waits for the data FIFO empty flag to disappear before entering the sending state.

  Note: DPSM will remain in Wait_S state for at least 2 clock cycles to meet the timing requirements of NWR. NWR is the interval from receiving the response from the card to when the host starts data transmission.

- Send:

  In this state, the DPSM starts sending data to the card device. Depending on the setting of the transfer mode bits in the data control register, the data transfer mode can be block transfer or stream transfer:

  – In block mode, when the data block counter reaches 0, the DPSM sends the internally generated CRC code, followed by the end bit, and enters the busy state.

  – In streaming mode, when the enable bit is high and the data counter is not 0, the DPSM sends data to the card device, and then enters the idle state.

  – If a FIFO underflow error occurs, the DPSM sets the FIFO error flag and enters the idle state.

- Busy:

  In this state, the DPSM waits for the CRC status flag:

  – If the correct CRC status is not received, the DPSM enters the idle state and sets the CRC failure status flag.

  – If the correct CRC status is received, and the card is not busy (SDIO_DAT0 is not low), the DPSM enters the Wait_S state.

  – If the correct CRC status is not received, the DPSM enters the idle state and sets the CRC failure status flag.

  – If the data timeout DPSM sets the data timeout flag and enters the idle state.

  – When the DPSM is in Wait_R or busy state, the data timer is enabled and can generate a data timeout error:

  – When sending data, if the DPSM is in a busy state and exceeds the timeout interval set by the program, a timeout will occur.

  – When receiving data, if all data is not received and DPSM is in Wait_R state for more than the timeout interval set by the program, a timeout will occur

18.3.1.6 Data

Data can be transferred from the host to the card and vice versa.

Data is transmitted over the data line. Data is stored in a 32-word depth FIFO, each word is 32 bits wide.

Table 18-3 Data Token Format

Description	Start bit	Data	CRC16	End bit
Block Data	0	-	Yes	1
Stream Data	0	-	No	1

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18.3.1.7 Data FIFO

The data FIFO unit has a data buffer for sending and receiving data buffers. The FIFO contains a data buffer and transmit and receive circuits, where the buffer size is 32 bits wide per word, 32 words in total (32 words deep). The data FIFO operates in the AHB clock region (HCLK/2), and all signals connected to the SDIO clock region (SDIOCLK) are resynchronized.

Depending on the SDIO_STS.TXRUN and SDIO_STS.RXRUN flags, the FIFO can be turned off, transmit enabled, or receive enabled. SDIO_STS.TXRUN and SDIO_STS.RXRUN are set by the data channel subunit and are mutually exclusive:

- When SDIO_STS.TXRUN is valid, the transmit FIFO represents the transmit circuit and data buffer
- When SDIO_STS.RXRUN is valid, the receive FIFO represents the receive circuit and data buffer

Transmit FIFO: When the SDIO transmit function is enabled, data can be written to the transmit FIFO through the AHB interface. The transmit FIFO has 32 consecutive addresses. There is a data output register in the transmit FIFO that contains the data word pointed to by the read pointer. When the data channel subunit fills the shift register, it moves the read pointer to the next data and transfers the data out. If the transmit FIFO is not enabled, all status flags are inactive. When sending data, the data channel subunit sets SDIO_STS.TXRUN to be valid.

Table 18-4 Transmit FIFO Status Flags

Flag	Description
SDIO_STS.TFIFOF	This flag is set high when all 32 transmit FIFO words have valid data.
SDIO_STS.TFIFOE	This flag is set high when all 32 transmit FIFO words have no valid data.
SDIO_STS.TFIFOHE	This flag is set high when 8 or more transmit FIFO words are empty. This flag can be used as a DMA request.
SDIO_STS.TDATVALID	This flag is set high when the transmit FIFO contains valid data. The meaning of this flag is just the opposite of TFIFOE.
SDIO_STS.TXURERR	This flag is set high when an underflow error occurs. This flag is cleared when writing to the SDIO clear register.

Receive FIFO: When the data channel subunit receives a data word, it will write the data into the FIFO. After the write operation is completed, the write pointer will automatically increase by one; at the other end, there is a read pointer that always points to the current data in the FIFO. If the receive FIFO is closed, all status flags are cleared and the read and write pointers are reset. The data channel subunit sets SDIO_STS.RXRUN when data is received. The following table lists the status flags of the receive FIFO. The receive FIFO can be accessed through 32 consecutive addresses.

Table 18-5 Receive FIFO Status Flags

Flag	Description
SDIO_STS.RFIFOF	This flag is set high when all 32 transmit FIFO words have valid data.
SDIO_STS.RFIFOE	This flag is set high when all 32 transmit FIFO words have no valid data.
SDIO_STS.RFIFOHF	This flag is set high when 8 or more transmit FIFO words are empty. This flag can be used as a DMA request.
SDIO_STS.RDATVALID	This flag is set high when the transmit FIFO contains valid data. The meaning of this flag is just the opposite of TFIFOE.
SDIO_STS.RXORERR	This flag is set high when an underflow error occurs. This flag is cleared when writing to the SDIO

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Flag	Description
	clear register.

18.3.2 SDIO AHB Interface

The AHB interface implements access to SDIO registers, data FIFOs, and generation of interrupts and DMA requests. Includes data channel, register decoder, and interrupt/DMA control logic.

18.3.2.1 SDIO interrupt

When at least one of the selected status flags is high, the interrupt control logic generates an interrupt request. The interrupt enable register allows the interrupt logic to generate the corresponding interrupt.

18.3.2.2 SDIO/DMA Interface

The DMA interface provides a way to quickly transfer data directly between the SDIO data FIFO and memory.

The following example details how to implement this method. The host controller uses CMD24 (WRITE_BLOCK) to transfer 512 bytes from the host to the MMC card, and the DMA controller is used to fill the SDIO FIFO with data from the memory.

1. Complete the card identification process
2. Increase SDIO_CLK clock frequency
3. Send CMD7 command to select card and configure bus width
4. The configuration process of DMA1 is as follows:
   a) Enable DMA1 controller and clear all interrupt flags
   b) Use the base address of the memory buffer to set the source address register of DMA1 channel 3, and use the address of the SDIO_FIFO register to configure the destination address register of DMA1 channel 3.
   c) Set the control register of DMA1 channel 3 (the memory address pointer is incremented, the peripheral address pointer is fixed, and the data width of memory and peripherals is word width)
   d) Enable DMA1 channel 3
5. The process of writing a data block (CMD24) is as follows:
   a) Set the SDIO data length register, write the data size in bytes into the SDIO_DATLEN register, write the block size in bytes into the SDIO_DATCTRL register, and then the host sends data in each block size (BLKSIZE).
   b) Write the address of the data to the SDIO parameter register SDIO_CMDARG, which is the address of the card that needs to transmit data
   c) Set the SDIO command control register (SDIO_CMDCTRL): SDIO_CMDCTRL.CMDIDX is set to 24 (WRITE_BLOCK); SDIO_CMDCTRL.CMDRESP[1:0] is set to 1 (SDIO card host waits for a response); SDIO_CMDCTRL.CMDRESP is set to 1 (SDIO card host waits for a short response); SDIO_CMDCTRL.CPSMEN is set to 1 (enable SDIO card host sends commands), other fields are their reset values.
   d) Wait for SDIO_STS.CMDRESPRECV bit is set, and then configure the SDIO data control register: SDIO_DATCTRL.DATEN is set to 1 (the SDIO card host is enabled to send data);

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SDIO_DATCTRL.DATDIR is set to 0 (the transmission direction is from the controller to the card); SDIO_DATCTRL.TRANSMOD is set to 0 (block data transfer); SDIO_DATCTRL.DMAEN is set to 1 (DMA enabled); SDIO_DATCTRL.BLKSIZE is set to 9 (512 bytes); other fields do not need to be set.

e) Bit10 DATBLKEND flag bit of wait status register SDIO_STS is set.

6. Query the enable status register of the DMA channel to confirm that no channel is still enabled.

18.4 Card function description

18.4.1 Confirmation of working voltage range

All cards can use any voltage within the specified range to communicate with the SDIO card host, the minimum and maximum voltage VDD values that can be supported are defined by the operating condition register (OCR) on the card. When communication between the host and the card is initiated, the host may not know the voltages supported by the card, and the card may not know whether the host can provide the voltages it supports. In order to verify the voltage, a series of special commands are required, which are defined in the relevant specifications.

The commands defined in the protocol specification include: CMD1 (SEND_OP_COND, for MMC), ACMD41 (SD_APP_OP_COND, for SD memory cards) and CMD5 (IO_SEND_OP_COND, for SD I/O cards). These commands provide a mechanism for the host to identify and reject cards that do not match the VDD range required by the host. This is because a card whose internal memory stores the Card Identification Number (CID) and Card Specific Data (CSD) can only transmit these information under the condition of data transfer VDD. When the SDIO card host module is inconsistent with the VDD range of the card, the card will not be able to complete the identification cycle and cannot send CSD data; therefore, when the VDD range does not match, the SDIO card host can use these special commands to identify and reject the card. The SDIO card host will generate the required VDD voltage when executing these commands. Cards that cannot transmit data within the specified voltage range are disconnected from the bus and become inactive.

If the card cannot operate at the supplied voltage, it does not return a response and remains in an idle state. It is mandatory to send CMD8 before ACMD41 command when initializing SD card. Receiving CMD8 is to let the card know that the host supports the physical layer 2.00 protocol and the card supports higher version functions. If the card can operate at the supplied voltage, the response will return the supply voltage and the check mode set in the command parameter.

18.4.2 Card reset

The CMD0 command (GO_IDLE_STATE) is a software reset command, which sets the multimedia card (MMC) and SD memory card into the idle state (Idle State). Regardless of the current card state. The reset command (CMD0) is only used for the memory part of the memory or combination card. The CMD52 command (IO_RW_DIRECT) resets the SD I/O card. Cards in the Inactive State are not affected by this command.

After the host is powered on, all cards are in the idle state (Idle State), including the cards that were previously in the inactive state (Inactive State). After power-on or after executing CMD0, the outputs of all cards are in a high-impedance state. The CMD lines of all cards are in input mode, waiting for the start bit of the next command, while all cards are initialized to a default relative card address (RCA=0x0001) and driven with a default clock frequency of 400kHz (lowest speed, maximum current drive capability).

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18.4.3 Card identification mode

After the host resets, it enters the card identification mode to search for a new card on the bus. In card identification mode, the host resets all cards, verifies the operating voltage range, identifies the cards and asks each card for the relative card address (RCA). This operation is done separately on each card's own command signal line CMD. All data communication in card identification mode uses only the command line (CMD). During card identification, the card should operate at clock rate F_{OD} (400 kHz).

18.4.4 Card identification process

The identification process of different cards is different; for multimedia cards, the card identification process starts with the clock frequency F_{od}, and all SDIO_CMD outputs are driven open, allowing parallel connection of cards during this process.

The identification process of the multimedia card is as follows:

1. The bus is enabled
2. The SDIO card host broadcasts the CMD1 (SEND_OP_COND) command, receives the operating conditions, and obtains the "wire AND" of the contents of the operating condition registers of all cards
3. If the card is not compatible, it will be placed in an inactive state
4. The SDIO card host broadcasts a CMD2 command (ALL_SEND_CID) to all active cards. All active cards simultaneously send their CID numbers serially. Those cards that detect that the output CID bits do not match the data on the command line must Stop sending and wait for the next recognition cycle. In the end, only one card can successfully transmit the complete CID to the SDIO card host and enter the identification state.
5. The SDIO card host sends a CMD3 command (SET_RELATIVE_ADDR) to the card. This new address is called the relative card address (RCA), which is shorter than the CID and is used to address the card. At this point, the card goes into a standby state and no longer responds to the new identification process, and at the same time its output drive changes from open circuit to push-pull mode.
6. The SDIO card host repeats steps 4 and 5 above until a timeout condition is received.

The SD card identification process starts with the clock frequency F_{od}, and all SDIO_CMD outputs are push-pull drivers instead of open-circuit drivers. The identification process is as follows:

1. The bus is enabled
2. The SDIO card host broadcasts the ACMD41 (SEND_APP_OP_COND) command to get the contents of the operating condition registers of all cards
3. If the card is not compatible, it will be placed in an inactive state
4. The SDIO card host broadcasts CMD2 (ALL_SEND_CID) to all activated cards, and all activated cards return their unique card identification number (CID) and enter the identification state.
5. The SDIO card host sends a CMD3 (SET_RELATIVE_ADDR) command and an address to an activated card, this new address is called relative card address (RCA), which is shorter than CID and is used to address the card. At this point, the card goes into the standby state. The host of the SDIO card can send this command again to change the RCA, and the RCA of the card will be the last assignment.

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6. The SDIO card host repeats steps 4 and 5 above for all activated cards until a timeout condition is received.

The SD I/O card identification process is as follows:

1. The bus is enabled
2. The SDIO card host sends the CMD5 (IO_SEND_OP_COND) command to get the contents of the card's operating condition register
3. If the card is not compatible, it will be placed in an inactive state
4. The SDIO card host sends a CMD3 (SET_RELATIVE_ADDR) command and an address to an activated card, this new address is called relative card address (RCA), which is shorter than CID and is used to address the card. At this point, the card goes into the standby state. The host of the SDIO card can send this command again to change the RCA, and the RCA of the card will be the last assignment.

18.4.5 Write data block

When the write data block command (CMD24-27) is executed, one or more data blocks are transferred from the host to the card(1-bit or 4-bit high level). If the CRC check is wrong, the card indicates a transfer failure via the SDIO_DAT signal line, the transferred data is discarded without being written, and all subsequent (in multi-block write mode) transferred data blocks will be ignored.

If the host transmits partial data and the accumulated data length is not aligned with the data block, and block misalignment is not allowed (parameter WRITE_BLK_MISALIGN for CSD is not set), the card will detect block misalignment errors before the start of the first unaligned block (set the ADDRESS_ERROR error bit in the status register) and ignore subsequent data transfers at the same time. The write operation is also aborted when the host attempts to write to a write-protected area, in which case the card will set the WP_VIOLATION bit in the status register.

Setting the CID and CSD registers does not require setting the block length in advance, and the transmitted data is also protected by CRC. If part of the CSD or CID register is stored in ROM, then this unchangeable part must match the corresponding part of the receive buffer. If there is an inconsistency, the card will report an error without modifying the contents of any register.

Some cards may take a long or unpredictable time to complete the writing of a data block. After receiving a data block and completing the CRC check, the card will start the write operation. If the write buffer is full and cannot be re-issued with a new WRITE_BLOCK command When receiving new data, it will pull the SDIO_DAT signal line low. The host can use SEND_STATUS (CMD13) to query the status of the card at any time, and the card will return the current status. The status bit READY_FOR_DATA indicates whether the card can accept new data or whether a write operation is still in progress. The host can unselect the card (select another card) by sending the CMD7 command, and put the card in the disconnected state, which can release the SDIO_DAT signal line without interrupting the outstanding write operation; when a card is reselected, if The write operation is still in progress and the write buffer is still unavailable, it will again indicate the busy state by pulling the SDIO_DAT signal line low.

18.4.6 Read data block

The read data block is a block-based data transfer. The basic unit of data transfer is a data block. The size of the block is defined in CSD (READ_BL_LEN). If READ_BL_PARTIAL is set, smaller blocks of data can also be transferred, whose start and end addresses are fully contained within the 512-byte boundary, and READ_BL_LEN defines the

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size of the physical block.

CMD17 (READ_SINGLE_BLOCK) means to start reading a data block, and the card returns to the sending state after the transmission is over. CMD18 (READ_MULTIPLE_BLOCK) starts to read multiple consecutive data blocks. In order to ensure the integrity of data transmission, there is a CRC check code after each data block.

The block length is set by CMD16 and can be set to 512 bytes regardless of the setting of READ_BL_LEN.

The host can abort a multi-block read operation at any time, regardless of the type of operation. Send a stop transfer command (CMD12) to abort the operation. The stop command has a delay in execution due to serial command transmission. Data transfer is stopped after the end bit of the stop command.

When using CMD18 to read the last block of userland, the host should ignore possible OUT_OF_RANGE errors, even if the sequence is correct.

If the card detects an error (for example: out-of-bounds, address misplacement, or internal error) during a multi-block read operation (of either type), it stops the data transfer and remains in the data state; at this point the host must send a stop transfer command to abort operate. Read errors are reported in response to the stop transfer command. If the host sends the stop transmission command, the card has already transmitted the last data block in a certain number of multiple data block operations, because the card is no longer in the data state at this time, the host will get an illegal command response. If the cumulative length of the partial blocks transferred by the host is not block aligned and block misalignment is not allowed, the card will detect block misalignment at the beginning of the first unaligned block, set the ADDRESS_ERROR error flag in the status register, interrupt the transfer and wait for the data Status of the stop command.

18.4.7 Data Streaming Operation (Only for Multimedia Card)

Data stream operations include data stream write and data stream read. In streaming mode, data is transferred in bytes without CRC after each data block.

18.4.7.1 Data stream write

Data stream writing to CMD20 (WRITE_DAT_UNTIL_STOP) starts to transmit data from the host to the card, starting from the starting address and continuing to transmit until the host issues a stop command. If partial data block transfers are allowed (CSD parameter WRITE_BL_PARTIAL is set), data flow can be started and stopped at any address in the card's address space, otherwise data flow should only be started and stopped at data block boundaries. Since the amount of data to be transmitted is not predetermined, the CRC check cannot be used. If the maximum memory address is reached when sending data, subsequent data transfers will be discarded even if the SDIO card host does not send a stop command.

If the host provides an out-of-range address as a parameter to CMD20, the card will reject the command, stay in the transmit state, and set ADDRESS_OUT_OF_RANGE; it should be noted that the data stream write command is only applicable to 1-bit bus configuration (SDIO_DAT0 signal on-line). It is considered an illegal command if CMD20 is issued in other bus configuration.

The maximum clock frequency for streaming write operations is calculated by the formula given below:

$$Max\_Write\_Frequence = Min(TRAN\_SPEED, \frac{8 \times 2^{WRITE\_BL\_LEN} - 100 \times NSAC}{TAAC \times R2W\_FACTOR})$$

- Max_Write_Frequence: maximum write frequency

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- TRAN_SPEED: Maximum bus clock frequency
- WRITE_BL_LEN: maximum write block length
- NSAC: Data read operation time in CLK cycles 2
- TAAC: Data read operation time 1
- R2W_FACTOR: Write speed factor

All parameters are defined in CSD registers. If the host attempts to use a higher frequency, the card may not be able to process the data and stop programming while setting the error bit SDIO_STS.RXORERR in the status register and ignoring all subsequent data transfers, waiting (in the receive data state) for a stop command . If the host attempts to write a value in the write-protected area, the write operation will be aborted and the card will set the WP_VIOLATION bit.

18.4.7.2 Data stream read

Data Streaming Data transfer is controlled by the READ_DAT_UNTIL_STOP (CMD11) command.

This command requires the card to read data from the specified address until the SDIO card host sends a STOP_TRANSMISSION (CMD12) command. Due to the delay of serial command transmission, the execution of the stop command will have a certain delay, so the data transfer will not stop until the end bit of the stop command. If the host provides an out-of-range address as a parameter to pass to CMD11, the card will reject the command and stay in the transfer state, the SDIO card host does not send a stop command, and the subsequently transferred data is also considered invalid data.

Another point to note is that the data stream read command only works in 1-bit bus mode (SDIO_DAT0 signal line). If CMD11 is issued in other bus configurations, the command is considered illegal.

The maximum clock frequency for stream read operations can be calculated as:

$$Max\_Read\_Frequence = Min(TRAN\_SPEED, \frac{8 \times 2^{READ\_BL\_LEN} - 100 \times NSAC}{TAAC \times R2W\_FACTOR})$$

- Max_Read_Frequence: maximum read frequency
- TRAN_SPEED: maximum data transfer rate
- READ_BL_LEN: maximum read data block length
- NSAC: Data read operation time in CLK cycles2
- TAAC: Data read operation time 1
- R2W_FACTOR: Write speed factor

If the host tries to use a higher frequency, the card will not be able to process the data transfer, at this time the card sets the SDIO_STS.TXURERR error bit in the status register, aborts the data transfer and waits for a stop command in the data state.

18.4.8 Erase

Erase includes block erase and sector erase. The erasing unit of the multimedia card is the erasing group, the basic writing unit of the card is the writing data block, and the erasing group is calculated by the writing data block. The size of the erase group is a card specific parameter and is defined in the CSD.

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The host can erase a contiguous range of erase groups. There are three steps involved in starting the erase operation. First, the host uses the ERASE_GROUP_START (CMD35) command to define the start address in the contiguous range, then uses the ERASE_GROUP_END (CMD36) command to define the end address of the contiguous range, and finally sends the erase command ERASE (CMD38) to start the erase operation. In the erase command, the address field is the erase group address in bytes. The card discards the portion that is not aligned with the size of the erase group and aligns the address boundary to the boundary of the erase group.

If an erase command (CMD35, CMD36, CMD38) is not received as described above, the card should set the ERASE_SEQ_ERROR bit in the card status register and restart the erase operation (waiting for the first step).

If a command other than SEND_STATUS and erase command is received, the card should set ERASE_RESET in the status register, reset the erase sequence and execute the new command.

If the erase range includes write-protected data blocks, the write-protected area will not be erased, only non-protected blocks can be erased, and the card should set the WP_ERASE_SKIP status bit in the status register.

If the host supplies an out-of-range address as an argument to CMD35 or CMD36, the card will reject the command, set the ADDRESS_OUT_OF_RANGE bit in the status register, and reset the entire erase sequence.

During the entire erasing process, Kara low SDIO_DAT signal. The actual erase time may be long, and the host can send a CMD7 command to deselect the card.

18.4.9 Wide bus selection and de-selection

The default bus width is 1 bit after the card is powered on or after the GO_IDLE_STATE (CMD0) command. The bus width can be changed after the host has verified the functional pins on the bus and the card is initialized.

The wide bus (4-bit bus width) operation mode can be selected by the SET_BUS_WIDTH (ACMD6) command, it should be noted that the SET_BUS_WIDTH (ACMD6) command is only valid in the transfer state, which means that only after the card is selected using the SELECT/DESELECT_CARD (CMD7) command to change the bus width.

18.4.10 Protection management

The host supports three card protection methods to protect data from being erased or rewritten:

1. Internal write protection of the card
2. Physical write protection switch
3. Card lock operation for password management

18.4.10.1 Write protection of internal cards

By permanently or temporarily setting the write-protect bit in the CSD, the user can permanently write-protect the entire card to prevent the card's data from being overwritten or erased. Some cards set the write protection of a group of sectors by setting the WP_GRP_ENABLE bit of the CSD, so that only part of the data can be selected to be protected. Write protection can be changed by program. The basic unit of write protection is the CSD parameter WP_GRP_SIZE sectors. Users can customize the size of the write protection area by configuring the value of WP_GRP_SIZE. The SET_WRITE_PROT command sets the write protection of the specified write protection group, and the CLR_WRITE_PROT command clears the write protection of the specified write protection group. The SEND_WRITE_PROT command requests the device to send the status of the write protection bit. This command is

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similar to the single data block read command. A data block of write protection bits, which represents 32 write protection groups starting from the specified address, followed by a 16-bit CRC code at the end. The address field of the write protect command is a group address in bytes, the card will truncate all addresses outside the group size.

18.4.10.2 Physical write protection switch

There is a mechanical slide switch on the side of the card, which provides the user with setting whether to write-protect the card. When the sliding switch is placed in the open position of the small window, the card is in write-protected state, and when the sliding switch is placed in the closed position of the small window, the card is not write-protected, and the user can modify the content in the card. There is also a switch on the corresponding part of the slot of the card to indicate whether the card is in the write-protected state. It should be noted that this instruction is for the SDIO card host module, and the internal circuit of the card does not know the position of the write-protect switch.

18.4.10.3 Password protection

Password protection means that the host module can lock or unlock the card with a password. The password is stored in the 128-bit PWD register, and the length of the password is stored in the 8-bit register of PWDS_LEN. These registers are non-volatile, so their contents are not lost after a power loss. The locked card supports all basic commands, such as reset, initialization, and status query commands sent by the SDIO card host module. If the card has previously set a password (that is, the value of PWDS_LEN is not 0), the card will be automatically locked after each power-on.

The same as the CSD and CID register write commands, the lock/unlock command is only valid in the transmission state, which also means that the card must be selected before using the lock/unlock command, and there is no address parameter in this command. of.

The structure and bus operation type of the lock/unlock command of the card are the same as the single data block write command of the card. The data block transmitted by the command contains the information required by the command, such as password setting mode, PWD content and lock/unlock instructions. Before sending the lock/unlock command of the card, the SDIO card host module has defined the length of the command data block. The structure of the command is shown in Table 18-6.

Table 18-6 Lock/Unlock Data Structure

Byte	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0	Reserved (Remains at 0)				ERASE	LOCK_UNLOCK	CLR_PWD	SET_PWD
1	PWDS_LEN							
2	Password Data (PWD)							
……								
PWDS_LEN-1								

- ERASE: Setting this bit to 1 will perform a forced erase, all other bits must be 0. In this case only the command byte is sent, all other bytes of the command will be ignored by the card.
- LOCK_UNLOCK: When this bit is 1, it means the card is locked, and when it is 0, it means it is unlocked. This bit can be set at the same time as SET_PWD, but not at the same time as CLR_PWD.
- CLR_PWD: Set this bit to 1 clear password data.
- SET_PWD: This bit is 1 to save the password data to the memory.
- PWDS_LEN: This parameter defines the length of the password, in bytes.

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- PWD: password data, according to different commands, the password data is different. For example, in the case of setting a new password, it contains the new password, and when changing the password, it contains the old password and the new password set.

The following sections list the command sequences to set/clear password, lock/unlock, and force wipe.

18.4.10.4 Set password

1. If the card has not been selected before, use the CMD7 (SELECT/DESELECT_CARD) command to select a card.
2. Use CMD16 (SET_BLOCKLEN) to define the length of the data block, the 8-bit card lock/unlock mode, the 8-bit PWDS_LEN (in bytes), and the number of bytes of the new password. When the password replacement is completed, the size of the data block in which the command is sent must take into account the lengths of both the old and new passwords.
3. On the data line, send the CMD42 (LOCK/UNLOCK) command with a suitable data block length and include a 16-bit CRC code. The data block contains the operation mode (SET_PWD=1), the password length (PWDS_LEN) and the password data itself (PWD). When the password replacement is completed, the password length value (PWDS_LEN) should be the sum of the lengths of the old and new passwords. The password data field (PWD) is preceded by the old password (in use) and followed by the new password.
4. When the old password sent is incorrect (size or content does not match the expected value), LOCK_UNLOCK_FAILED in the status register will be set and the old password will not be changed. If the old password matches, the new password data and length are stored in PWD and PWDS_LEN respectively.

The password length field (PWDS_LEN) can indicate whether a password is currently set. If the field is zero, it means that the password is not used. Only when the field is not zero, the card will be automatically locked when powered on. If a password is set, and you want to lock the card immediately without power failure, you can set the LOCK_UNLOCK bit or send an additional lock command.

18.4.10.5 Clear password

1. If the card has not been selected before, use the CMD7 (SELECT/DESELECT_CARD) command to select a card.
2. Use CMD16 (SET_BLOCKLEN) to define the data block length, 8-bit card lock/unlock mode, 8-bit PWDS_LEN (in bytes), and the number of bytes of the currently used password.
3. On the data line, send the CMD42 (LOCK/UNLOCK) command with a suitable data block length and include a 16-bit CRC code. The data block contains the operating mode (CLR_PWD), the password length (PWDS_LEN) and the password data itself (PWD). If the passwords match, the contents of PWD will be cleared and PWDS_LEN will be set to 0. If the contents of PWD and PWDS_LEN do not match the transmitted password and its size, the LOCK_UNLOCK_FAILED error bit in the status register is set and the password is unchanged.

18.4.10.6 Card lock

1. If the card has not been selected before, use the CMD7 (SELECT/DESELECT_CARD) command to select a card.
2. Use CMD16 (SET_BLOCKLEN) to define the data block length, 8-bit card lock/unlock mode, 8-bit PWDS_LEN indicates the number of bytes of the currently used password.
3. On the data line, send the CMD42 (LOCK/UNLOCK) command with a suitable data block length and include

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a 16-bit CRC code. The data block contains the operation mode (LOCK_UNLOCK=1), the password length (PWDS_LEN) and the password data itself (PWD).

4. If the PWD content is equal to the sent password, the card will be locked and the CARD_IS_LOCKED status bit in the status register will be set. If the sent password does not match the expected password (length or content), the LOCK_UNLOCK_FAILED error bit in the status register is set and the lock operation fails.

Setting the password and locking the card can be performed simultaneously in the same sequence of operations. In this case, the card host module first sets the password according to the above steps. It should be noted that the LOCK_UNLOCK bit should be set in the third step of sending the new password command.

Only the card that has previously set a password (PWDS_LEN is not 0) will be automatically locked when it is powered on and reset. Locking a card that is already locked or a card without a password will fail and set the LOCK_UNLOCK_FAILED error bit in the status register.

18.4.10.7 Card unlock

1. If the card has not been selected before, use the CMD7 (SELECT/DESELECT_CARD) command to select a card.
2. Use CMD16 (SET_BLOCKLEN) to define the data block length, 8-bit card lock/unlock mode, 8-bit PWDS_LEN (in bytes), and the number of bytes of the currently used password.
3. On the data line, send the CMD42 (LOCK/UNLOCK) command with a suitable data block length and include a 16-bit CRC code. The data block contains the operation mode (LOCK_UNLOCK=0), the password length (PWDS_LEN) and the password data itself (PWD).
4. If the sent password does not match the expected password (length or content), set the LOCK_UNLOCK_FAILED error bit in the status register to 1, while the card remains locked. When the password is matched, the card lock is released, and the CARD_IS_LOCKED bit in the status register is cleared at the same time.

If the unlocked state is only valid during the current power supply process, as long as the PWD is not cleared, the card will still be automatically locked after the next power-on.

Attempting to unlock an already unlocked card will cause the operation to fail and set the LOCK_UNLOCK_FAILED error bit in the status register.

18.4.10.8 Force erase

A forced erase operation can erase all data and passwords in the card. If the user forgets the password, the card can be made available again through a forced wipe operation.

1. If the card has not been selected before, use the CMD7 (SELECT/DESELECT_CARD) command to select a card.
2. Use CMD16 (SET_BLOCKLEN) to define the data block length, 8-bit card lock/unlock mode, 8-bit PWDS_LEN indicates the number of bytes of the currently used password.
3. Send a CMD42 (LOCK/UNLOCK) command with a suitable data block length on the data line and include a 16-bit CRC code. The data block contains the operating mode (ERASE=1) all other bits are 0.
4. If and only if the ERASE bit in the data field is 1, all contents of the card will be erased, including the PWD and PWDS_LEN fields. The card is no longer locked after erasing. If any other bit is not 0, set the

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LOCK_UNLOCK_FAILED error bit in the status register, the data in the card remains unchanged, and the card remains locked.

NOTE: Attempting to perform an erase operation on an already unlocked card will cause the operation to fail and set the LOCK_UNLOCK_FAILED error bit in the status register.

18.4.11 Card status register

18.4.11.1 Card status register

Card status refers to the error and status information of the executed command, indicated in the response.

Generally, after receiving a command, the card will return the status information related to the command to the card host. These status information may be stored in the local status register. This status information is called the card's status field, and the response format R1 contains a 32-bit field called the card status.

Table 18-7 defines the different status messages.

Table 18-7 Card Status

Bits	Identifier	Type	Value	Description	Clear condition
31	ADDRESS_OUT_OF_RANGE	EXR	'0'=no error '1'=error	The address parameter in the command is out of the allowed range for the card. A multi-block or stream read/write operation (even from a valid address) attempts to read or write beyond the capacity of the card.	C
30	ADDRESS_MISALIGN		'0'=no error '1'=error	The first data block defined by the address parameter in the command (contrasted with the current data block length) is not aligned with the card's physical block. A multi-block or stream read/write operation (even if starting at a legal address) attempts to read or write a block of data that is not aligned with the physical block.	C
29	BLOCK_LEN_ERROR		'0'=no error '1'=error	The parameter of the SET_BLOCKLEN command exceeds the maximum allowable range of the card, or the previously defined data block length is illegal for the current command (for example: the host issues a write command, the current block length is less than the minimum length allowed by the card, and at the same time Partial data block writing is not allowed).	C
28	ERASE_SEQ_ERROR		'0'=no error '1'=error	Erase commands were sent in the wrong order.	C
27	ERASE_PARAM	EX	'0'=no error '1'=error	An illegal erase group was selected while erasing.	C
26	WP_VIOLATION	EX	'0'=no error	An attempt was made to program a write-protected	C

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Bits	Identifier	Type	Value	Description	Clear condition
			‘1’=error	block of data.	
25	CARD_IS_LOCKED	SR	‘0’=card unlocked ‘1’=card locked	When this bit is set, it means the card has been locked.	A
24	LOCK_UNLOCK_FAILED	EX	‘0’=no error ‘1’=error	Wrong sequence of commands in lock/unlock or wrong password detected.	C
23	COM_CRC_ERROR	ER	‘0’=no error ‘1’=error	CRC check error in previous command.	B
22	ILLEGAL_COMMAND	ER	‘0’=no error ‘1’=error	The command is illegal for the current card state.	B
21	CARD_ECC_FAILED	EX	‘0’=success ‘1’=failure	The ECC check is implemented inside the card, but it fails to correct the data.	C
20	CC_ERROR	ER	‘0’=no error ‘1’=error	(Not defined in the standard) An error occurred inside the card, independent of a command from the host.	C
19	ERROR	EX	‘0’=no error ‘1’=error	An internal card error (eg: read or write error) related to the execution of the last host command (not defined in the standard) has occurred.	C
18	Reserved				
17	Reserved				
16	CID/CSD_OVERWRITE	EX	‘0’=no error ‘1’=error	Can be any of the following errors: The CID register has been written and cannot be overwritten; The read-only portion of the CSD does not match the contents of the card; An attempt was made to reverse the copy or permanent write protection, i.e. restore or release write protection.	C
15	WP_ERASE_SKIP	EX	‘0’= not protected ‘1’= protected	Encountering an existing write-protected data block, only part of the address space is erased.	C
14	CARD_ECC_DISABLED	SX	‘0’=enabled ‘1’=disabled	No internal ECC is used when executing the command.	A
13	ERASE_RESET		‘0’=clear ‘1’=set	The sequence into the erase process was aborted because a command outside the erase sequence was received (not a CMD35, CMD36, CMD38, or CMD13 command).	C
12:9	CURRENT_STATE	SR	‘0’= Idle ‘1’= Ready ‘2’= Ident ‘3’= Standby ‘4’= Send ‘5’= Data ‘6’= Receive	The state of the state machine in the card when the command is received. If the execution of a command results in a change of state, this change will be reflected in the response of the next command. These four bits are interpreted as decimal numbers 0 to 15.	B

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Bits	Identifier	Type	Value	Description	Clear condition
			'7'= Program '8'= Disconnect '9'= Busy test '10~15'= Reserved		
8	READY_FOR_DATA	SR	'0'= no ready '1'= ready	Corresponds to a buffer empty signal on the bus.	
7	SWITCH_ERROR	ER	'0'=no error '1'=error	The card did not switch to the desired mode as required by the SWITCH command.	B
6	Reserved				
5	APP_CMD	SR	'0'=enabled '1'=disabled	Card expects ACMD, or indicates that the command has been interpreted as an ACMD command.	C
4	Reserved for SD I/O Card				
3	AKE_SEQ_ERROR	ER	'0'=no error '1'=error	The order of validation is wrong.	C
2	Reserved for application specific commands				
1,0	Reserved for manufacturer test mode				

The abbreviations in the table for types and clearing condition fields are defined as follows:

Type:

- E: Error bit. Send an error condition to the host. These bits are cleared once a response (reporting an error) is issued.
- S: Status bit. These bits serve only as information fields and do not change in response to commands. These bits are persistent, they are set or cleared depending on the card state.
- R/X: Both R and X are detection bits, the difference is that R means that the card detects an anomaly in the command interpretation and verification phase (response mode), while X means that the card detects an anomaly in the command execution phase (execution mode).

SDIO card host can read these bits by sending a status command to query the status of the card.

Clear condition:

- A: According to the current state of the card
- B: Always relative to the previous command. Cleared when the correct command is received, this method has a delay of one command.
- C: Read clear

18.4.11.2 SD status register

The SD status contains not only status bits related to specific functions of the SD memory card, but also some status bits related to future applications. The length of the SD state is a 512-bit data block. After receiving the ACMD13 command (CMD55, then CMD13), the content of the SD status register is transferred to the SDIO card host. But it

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should be noted that ACMD13 commands can only be sent when the card is in the transmitting state (the card has been selected).

Table 18-8 defines the different SD status register information.

Table 18-8 SD Status

Bits	Identifier	Type	Value	Description	Clear condition
511:510	DAT_BUS_WIDTH	SR	‘00’= 1 (Default) ‘01’= Reserved ‘10’= 4 Bit width ‘11’= Reserved	The current data bus width as defined by the SET_BUS_WIDTH command.	A
509	SECURED_MODE	SR	‘0’= Not in privacy mode ‘1’= In privacy mode	The card is in secure operation mode (see "SD Security Specification" for details).	A
508:496	Reserved				
495:480	SD_CARD_TYPE	SR	‘00xxh’= SD memory card in physical specification version 1.01~2.00 ('x' means any value). The defined cards are: '0000'= Regular SD RD/WR Card '0001'= SD ROM Card	The lower 8 bits of this field can define different variants of SD memory cards in the future (each bit can be used to define a different SD type). The upper 8 bits can be used to define SD cards that do not adhere to the current SD physical layer specification.	A
479:448	SIZE_OF_PROTECTED_AREA	SR	Protected area size (See below)	(See below)	A
447:440	SPEED_CLASS	SR	The speed type of the card (See below)	(See below)	A
439:432	PERFORMANCE_MOVE	SR	Transfer performance in units of 1MB/sec (See below)	(See below)	A
431:428	AU_SIZE	SR	Size of AU (see below)	(See below)	A
427:424	Reserved				
423:408	ERASE_SIZE	SR	Number of AUs that can be erased at one time	(See below)	A
407:402	ERASE_TIMEOUT	SR	Timeout value for the range specified by the ERASE_AU	(See below)	A

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Bits	Identifier	Type	Value	Description	Clear condition
			unit		
401:400	ERASE_OFFSET	SR	Fixed offset value to increase when erasing	(See below)	A
399:312	Reserved				
311:0	Reserved for Manufacturer				

The abbreviations in the table for types and clearing condition fields are defined as follows:

Type:

- E: Error bit. Send an error condition to the host. These bits are cleared once a response (reporting an error) is issued.
- S: Status bit. These bits serve only as information fields and do not change in response to commands. These bits are persistent, they are set or cleared depending on the card state.
- R/X: R and X are both detection bits, the difference is that R indicates that the card detects an abnormality in the command interpretation and verification stage (response mode), while X indicates that the card detects an anomaly in the command execution stage (execution mode).

The SDIO card host queries the status of the card by sending status commands to read these bits.

Clear condition:

- A: According to the current state of the card
- B: Always relative to the previous command. Cleared when the correct command is received, this method has a delay of one command.
- C: Read clear

SIZE_OF_PROTECTED_AREA

This bit is set differently for standard-capacity and high-capacity cards.

The capacity of the protected area of a standard capacity card is calculated as follows:

Protected Area=SIZE_OF_PROTECTED_AREA * MULT * BLOCK_LEN

SIZE_OF_PROTECTED_AREA is in units of MULT * BLOCK_LEN.

The capacity of the protected area of the high-capacity card is calculated as follows:

Protected Area = SIZE_OF_PROTECTED_AREA

SIZE_OF_PROTECTED_AREA is in bytes.

SPEED_CLASS

These 8 bits indicate the type of speed and a value that can be calculated by calculating $P_W/2$ (P_W is the write performance).

Table 18-9 Speed Type Codes

SPEED_CLASS	Value definition

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00h	Class 0
01h	Class 2
02h	Class 4
03h	Class 6
04h~FFh	Reserved

PERFORMANCE_MOVE

These 8 bits indicate the mobile performance (Pm) in units of 1MB/sec. If the card does not move data in RU (unit of record), Pm should be considered to be infinity. When this field is FFh, it means Pm is infinite.

Table 18-10 Mobility Performance Codes

PERFORMANCE_MOVE	Value definition
00h	Undefined
01h	1MB/sec
02h	2MB/sec
……	……
FEh	254MB/sec
FFh	Infinity

AU_SIZE

These 4 bits indicate the length of the AU, value is (16K bytes) × $2^{(AU\_SIZE-1)}$.

Table 18-11 AU_SIZE Codes

AU_SIZE	Value definition
00h	Undefined
01h	16KB
02h	32KB
03h	64KB
04h	128KB
05h	256KB
06h	512KB
07h	1MB
08h	2MB
09h	4MB
Ah~Fh	Reserved

The maximum AU length is determined by the capacity of the card. The card can set any AU length between the RU length and the maximum AU length.

Table 18-12 Maximum AU Size

Capacity	16MB~64MB	128MB~256MB	512MB	1GB~32GB
Maximum AU Size	512KB	1MB	2MB	4MB

ERASE_SIZE

This 16-bit field represents NERASE. When NERASE AUs are erased, the timeout period is defined by

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ERASE_TIMEOUT. The host should determine the appropriate number of AUs to be erased in one operation so that the host can display the progress of the erase operation. If this field is 0, the timeout calculation for erasure is not supported.

Table 18-13 ERASE_SIZE Codes

ERASE_SIZE	Value definition
0000h	Erase timeout calculation is not supported.
0001h	1 AU
0002h	2 AU
0003h	3 AU
……	……
FFFFh	65535 AU

ERASE_TIMEOUT

These 6 bits represent TERASE. When multiple AUs indicated by ERASE_SIZE are erased, this value gives the erase timeout time from the offset. The range of ERASE_TIMEOUT can be defined up to 63 seconds. The manufacturer of the card can choose any combination of ERASE_SIZE and ERASE_TIMEOUT according to the specific implementation. Once ERASE_TIMEOUT is determined, then ERASE_SIZE is also determined. If the ERASE_SIZE field is set to 0, then ERASE_TIMEOUT should also be set is 0.

Table 18-14 Erase Timeout Code

ERASE_TIMEOUT	Value definition
00	Erase timeout calculation is not supported.
01	1 sec
02	2 sec
03	3 sec
……	……
63	63 sec

ERASE_OFFSET

These 2 bits give TOFFSET, which can select one of the four values shown in the table below. When ERASE_SIZE and ERASE_TIMEOUT are both 0, this value has no meaning.

Table 18-15 Erase Offset Codes

ERASE_OFFSET	Value definition
0	0 sec
1	1 sec
2	2 sec
3	3 sec

18.4.12 SD I/O mode

18.4.12.1 I/O interrupts

There is a pin (pin 8) with interrupt function on the SD interface, which enables the SD I/O card to interrupt the multi-media card/SD module. In 4-bit SD mode, this pin is SDIO_DAT1, through which the card sends the multi-

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media card to the multi-media card. The /SD module makes an interrupt request. For each card or function within the card, the interrupt function is optional.

The interrupt of SD I/O is level-effective, that is, the interrupt signal line must maintain the active level (low) before it can be recognized and responded by the multimedia card/SD module, and remains inactive level (high) after the interrupt process ends. After the interrupt request has been serviced by the MultiMediaCard/SD module, the interrupt status bits can be cleared by writing the appropriate bits to the SD I/O card's internal registers through an I/O write operation.

The interrupt outputs of the SD I/O card are all active low, and the multimedia card/SD module provides pull-up resistors on all data lines (SDIO/D[3:0]). The multimedia card/SD module samples the 8th pin (SDIO_DAT/IRQ) and performs interrupt detection only in the interrupt stage, and ignores the value on the signal line at other times.

Both I/O operations and memory operations have interrupt stages, and the definition of the interrupt stage for single data block operations and multiple data block transfer operations is different.

18.4.12.2 I/O suspend and resume

In a multifunction SD I/O card, or in a card with both I/O and memory functions, multiple devices (I/O and memory) share the MMC/SD bus. In order to enable multiple devices to share the bus in the MMC/SD module, SD I/O cards and composite cards can selectively implement the concept of suspend/resume; in cards that support suspend/resume, the MMC/SD module can suspend a A data transfer operation of a function or memory to give up the bus to another function or memory with a higher priority, and resume the previously suspended transfer after the transfer of the function or memory with a higher priority is completed.

Whether to support suspend/resume operations is optional. Following are the steps to perform a suspend/resume operation on the MMC/SD bus:

1. Determine the current function of the data line (SDIO_DAT[3:0])
2. Request to suspend low-priority or slow operations
3. Wait for the pause operation to complete and confirm that the device has been paused
4. Start the transfer of the high-priority device
5. Wait for the high-priority device to complete the transfer
6. Resume from a suspend operation

18.4.12.3 I/O ReadWait

The Read Wait operation is optional and only works in 1-bit or 4-bit mode of the SD card. The read wait operation means that when a card is reading multiple registers (IO_RW_EXTENDED, CMD53), the MMC/SD module can ask it to temporarily stop data transmission, and at the same time allow the MMC/SD module to send commands to other functions in the SD I/O device. The MMC/SD module can judge whether a card supports the read waiting protocol by detecting the internal registers of the card. The read wait time is related to the interrupt phase.

18.5 Commands and responses

18.5.1 Application related commands and general commands

The SD card host module system is a standard interface, which is suitable for a variety of application types, while

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taking into account specific users and applications, so two types of general commands are defined in the standard: application-related commands (ACMD) and general commands (GEN_CMD) .

When the card receives the APP_CMD (CMD55) command, the card expects the next command to be an application related command. Application Dependent Commands (ACMD) and normal multimedia card commands have the same format structure, and they can also use the same CMD number. Because it appears after APP_CMD (CMD55), the card recognizes it as an ACMD command. If the APP_CMD(CMD55) command is not followed by a defined application-related command, it is recognized as a standard command; for example: if CMD13 (SD_STATUS(ACMD13) is defined in the application) is received immediately after APP_CMD(CMD55), it will Interpreted as SD_STATUS (ACMD13); but if the card receives CMD7 immediately after APP_CMD (CMD55), and the card does not define ACMD7, it will be interpreted as a standard CMD7 (SELECT/DESELECT_CARD) command.

If you want to use the manufacturer-defined ACMD, the SD card host needs to do the following:

1. Send APP_CMD (CMD55) command
2. The card returns a response to the multimedia/SD card module, indicating that the APP_CMD bit is set and waiting for the ACMD command.
3. Send the specified ACMD
4. The card returns a response to the multimedia/SD card module, the response indicates that the APP_CMD bit is set, and the received command has been correctly parsed according to the ACMD command; if the received command is not an ACMD command, the card will be processed according to the ordinary multimedia card command, At the same time, clear the APP_CMD bit of the status register.

If an illegal command is sent, error handling will be performed according to standard illegal multimedia card commands. The bus operation process of the GEN_CMD command is the same as the single data block read and write command (WRITE_BLOCK, CMD24 or READ_SINGLE_BLOCK, CMD17); at this time, the parameter of the command indicates the direction of data transmission instead of the address, and the data block has a user-defined format and meaning.

Before sending the GEN_CMD (CMD56) command, the state machine must be in the transmission state, that is, the card must be selected, and the length of the data block is defined by SET_BLOCKLEN (CMD16). The response to the GEN_CMD (CMD56) command is in R1b format.

18.5.2 Commands of Multimedia Card/SD Card module

Table 18-16 Write commands for block-based transfers

CMD Index	Type	Parameter	Response Format	Abbreviation	Description
CMD23	ac	[31:16]=0 [15:0]= Number of blocks	R1	SET_BLOCK_COUNT	Defines the number of blocks that need to be transferred in a subsequent multi-block read or write command.
CMD24	adtc	[31:0]= Data Address	R1	WRITE_BLOCK	Writes a block of the length selected by the SET_BLOCKLEN command.
CMD25	adtc	[31:0]= Data Address	R1	WRITE_MULTIPLE_BLOCK	Continuously write data blocks until a STOP_TRANSMISSION command is

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CMD Index	Type	Parameter	Response Format	Abbreviation	Description
					received or the specified number of blocks is reached.
CMD26	adtc	[31:0]= Stuff bits	R1	PROGRAM_CID	Program the identification register of the card. This command can only be sent once per card. There are hardware mechanisms in the card to prevent multiple programming operations. Usually this order is reserved for the manufacturer.
CMD27	adtc	[31:0]= Stuff bits	R1	PROGRAM_CSD	Program the programmable bits in the CSD of the card.
CMD28	ac	[31:0]= Data Address	R1b	SET_WRITE_PROT	If the card is write-protected, this command sets the write-protect bit of the specified group. The write protection feature is set in the special data area of the card (WP_GRP_SIZE).
CMD29	ac	[31:0]= Data Address	R1b	CLR_WRITE_PROT	If the card is write-protected, this command clears the write-protect bit of the specified group.
CMD30	adtc	[31:0]= Write Protect Data Addresses	R1	SEND_WRITE_PROT	If the card is write-protected, this command requires the card to send the status of the write-protect bit.
CMD31	Reserved				

Table 18-17 Block-based write-protect commands

CMD Index	Type	Parameter	Response Format	Abbreviation	Description
CMD28	ac	[31:0]= Data Address	R1b	SET_WRITE_PROT	If the card is write-protected, this command sets the write-protect bit of the specified group. The write protection feature is set in the special data area of the card (WP_GRP_SIZE).
CMD29	ac	[31:0]= Data Address	R1b	CLR_WRITE_PROT	If the card is write-protected, this command clears the write-protect bit of the specified group.
CMD30	adtc	[31:0]= Write Protect Data Addresses	R1	SEND_WRITE_PROT	If the card is write-protected, this command requires the card to send the status of the write-protect bit.
CMD31	Reserved				

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Table 18-18 Erase command

CMD Index	Type	Parameter	Response Format	Abbreviation	Description
CMD32 …… CMD34	Reserve. For backward compatibility with older versions of the media card protocol, these command codes cannot be used.				
CMD35	ac	[31:0]= Data Address	R1	ERASE_GROUP_START	Within the selected erase range, set the address of the first erase group.
CMD36	ac	[31:0]= Data Address	R1	ERASE_GROUP_END	Sets the address of the last erase group within the selected contiguous erase range.
CMD37	Reserve. For backward compatibility with older versions of the media card protocol, these command codes cannot be used.				
CMD38	ac	31:0]= Stuff bits	R1	ERASE	Erase the previously selected block of data.

Table 18-19 I/O mode command

CMD Index	Type	Parameter	Response Format	Abbreviation	Description
CMD39	ac	[31:16] =RCA [15]= Register Write Flag [14:8]= Register Address [7:0]= Register Data	R4	FAST_IO	Used to write and read 8-bit (register) data fields. This command specifies a card and register and also provides written data if the write flag is set. The R4 response contains the data read from the specified register. This command accesses application-related registers not defined in the multimedia card standard.
CMD40	bcr	[31:0]= Data Address	R5	GO_IRQ_STATE	Put the system in interrupt mode.
CMD41	Reserved				

Table 18-20 Lock command

CMD Index	Type	Parameter	Response Format	Abbreviation	Description
CMD42	adtc	[31:0]= Stuff bits	R1b	LOCK_UNLOCK	Set/clear password or lock/unlock card. The length of the data block is set by the SET_BLOCKLEN command.
CMD43 …… CMD54	Reserved				

Table 18-21 Application related commands

CMD Index	Type	Parameter	Response Format	Abbreviation	Description
CMD55	ac	[31:16]=RCA	R1	APP_CMD	Indicates that the next command to the card is an

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CMD Index	Type	Parameter	Response Format	Abbreviation	Description
		[15:0]= Stuff bits			application-related command rather than a standard command.
CMD56	adtc	[31:1]= Stuff bits [0]=RD/WR			In general or application-related commands, either to transfer a block of data to the card, or to read a block of data from the card. The length of the data block is set by the SET_BLOCKLEN command.
CMD57 …… CMD59	Reserved				
CMD60 …… CMD63	Reserved for manufacturer.				

18.5.3 Command type

ACMD and GEN_CMD contain four different types:

1. Broadcast Command (BC): Sent to all cards, no response.
2. Broadcast Command with Response (BCR): sent to all cards and received responses from all cards at the same time;
3. Command (AC) with addressing (point-to-point): sent to the addressed card, there is no data transmission on the SDIO_DAT signal line.

Data transfer command (AC) with addressing (point-to-point): sent to the addressed card, SDIO_DAT signal line for data transfer.

18.5.4 Command format

The command format consists of command and response.

Command: A command is used to start an operation. The host sends a command with an address or a broadcast command to a specified card or all cards (the broadcast command is only applicable to MMC V3.31 or earlier versions). All commands have a fixed length of 48 bits and are transmitted serially on the CMD line. The following table gives the general command format on Multimedia Cards, SD Memory Cards and SDIO Cards

The CE-ATA command is an extension of the MMC V4.2 command, so it has the same format.

The command channel operates in half-duplex mode, so that commands and responses can be sent and received separately. If the CPSM is not in the transmit state, the SDIO_CMD output is in a high-impedance state, as shown in Figure 20-11 Bit sequence. Data on SDIO_CMD is synchronized with the rising edge of SDIO_CLK.

Table 18-22 Command format

Bit	Width	Value	Description
47	1	0	Start bit
46	1	1	Transmission bit

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[45:40]	6	-	Command index
[39:8]	32	-	Parameter
[7:1]	7	-	CRC7
0	1	1	End bit

Response: The response is a response to the previously received command, which is sent to the host by a card with a specified address. For all cards of MMC V3.31 or earlier, the response is sent simultaneously; the response is serially transmitted on the SDIO_CMD line.

SDIO supports two response types: 48-bit short response and 136-bit long response. Both types have CRC error detection:

Note: If the response does not contain a CRC (such as the response to CMD1), the device driver SHOULD ignore the CRC failure status.

Table 18-23 Short response format

Bit	Width	Value	Description
47	1	0	Start bit
46	1	0	Transmission bit
[45:40]	6	-	Command index
[39:8]	32	-	Parameter
[7:1]	7	-	CRC7 (or 1111111b)
0	1	1	End bit

Table 18-24 Long response format

Bit	Width	Value	Description
135	1	0	Start bit
134	1	0	Transmission bit
[133:128]	6	111111	Reserved
[127:1]	127	-	CID or CSD (including internal CRC7)
0	1	1	End bit

18.5.5 Response format

All responses are sent over the CMD signal line. Response transfers always start with the MSB bit of the corresponding response string. The length of the response string depends on the response type.

Each response contains a start bit (always 0) followed by the direction bit of the transfer (card=0). The x in the table below represents a variable part. All responses are CRC protected except for the R3 response type. Each command codeword has an end bit (always 1).

There are 5 response types, and their formats are defined as follows:

R1 (normal response command)

The code length of the R1 response is 48 bits. Where bits 45:40 indicate the command index to respond to and its value is between 0 and 63. The state of the card is encoded by 32 bits.

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Table 18-25 R1 response

Bit	Width	Value	Description
47	1	0	Start bit
46	1	0	Transmission bit
[45:40]	6	X	Command index
[39:8]	32	X	Card status
[7:1]	7	X	CRC7
0	1	1	End bit

R1b

R1b has the same format as R1, the difference is that R1b can choose to send a busy signal on the data line. After receiving these commands, depending on the state before receiving the command, the card may become busy and the host should check the busy state in the response.

R2 (CID, CSD register)

The R2 code length is 136 bits. The responses of CMD2 and CMD10 are saved in the CID register and sent. The response of CMD9 is saved in the CSD register and sent. The card only responds and transmits bits [127...1] of CID and CSD, on the receiving side, these two register reserved bits [0] are replaced with the end bit of the response. The actual erase operation may take a long time, and the host can send a CMD7 command to deselect the card.

Table 18-26 R2 response

Bit	Width	Value	Description
135	1	0	Start bit
134	1	0	Transmission bit
[133:128]	6	'111111'	Command index
[127:1]	127	X	Card status
0	1	1	End bit

R3 (OCR register)

The R3 code length is 48 bits. The response of CMD1 is saved in the OCR register and sent. The definition of the level code is: the limited voltage window is low and the card is busy.

Table 18-27 R3 response

Bit	Width	Value	Description
47	1	0	Start bit
46	1	0	Transmission bit
[45:40]	6	'111111'	Reserved
[39:8]	32	X	OCR register
[7:1]	7	'1111111'	Reserved
0	1	1	End bit

R4 (Fast I/O)

The R4 code is 48 bits long and is only applicable to MMC cards. The parameter field includes the RCA of the specified card, the address of the register that needs to be read or written, and its content.

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Table 18-28 R4 response

Bit		Width	Value	Description
47		1	0	Start bit
46		1	0	Transmission bit
[45:40]		6	'111111'	Reserved
[39:8]Argument field	[31:16]	16	x	RCA
	[15:8]	8	x	Register address
	[7:0]	8	x	Read register contents
[7:1]		7	'1111111'	CRC7
0		1		End bit

R4b

R4b is only available for SD I/O cards, and the code length is 48 bits. The SDIO card will return a unique SDIO response R4 after receiving the CMD5 command.

Table 18-29 R4b response

Bit		Width	Value	Description
47		1	0	Start bit
46		1	0	Transmission bit
[45:40]		6	x	Reserved
[39:8]Argument field	39	1	x	Card is ready
	[38:36]	3	x	Number of I/O functions
	35	1	x	Present memory
	[34:32]	3	x	Stuff bits
	[31:8]	24	x	I/O ORC
[7:1]		7	x'	Reserved
0		1	1	End bit

When the SD I/O card receives the command CMD5, the I/O part of the card is enabled and can respond to all subsequent commands normally. The enabled state of the I/O card will remain until the next reset, power off, or CMD52 command for I/O reset. Note that the correct response for a memory-only SD card would be 1 for the current memory and 0 for the number of I/O functions. A memory-only SD card designed according to the SD Memory Card Specification Version 1.0 treats the detected CMD5 command as an illegal command and does not respond to it. The host that can handle the I/O card will send a CMD5 command, and if the card returns a response R4, the host will determine the configuration of the card based on the data in the R4 response.

R5 (Interrupt Request)

R5 only works with multimedia cards. The code length is 48 bits. The RCA field in the parameter is 0x0 when this response is generated by the host.

Table 18-30 R5 response

Bit	Width	Value	Description
47	1	0	Start bit
46	1	0	Transmission bit
[45:40]	6	'111111'	CMD40

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Bit		Width	Value	Description
[39:8]Argument field	[31:16]	16	x	RCA[31:16] of a successful card or host
	[15:0]	16	x	Undefined. Can be used as interrupt data.
[7:1]		7	x	CRC7
0		1	1	End bit

R6 (Interrupt Request)

R6 only works with SD I/O cards. The code length is 48 bits. Bits[45:40] represent the command index to the CMD3 response. The 16 most significant bits of the parameter field are used for the published RCA number. This is the normal response of the memory device to a CMD3 command.

Table 18-31 R6 response

Bit		Width	Value	Description
47		1	0	Start bit
46		1	0	Transmission bit
[45:40]		6	'101000'	CMD40
[39:8]Argument field	[31:16]	16	x	RCA[31:16] of a successful card or host
	[15:0]	16	x	Undefined. Can be used as interrupt data.
[7:1]		7	x	CRC7
0		1	1	End bit

When sending a CMD3 command to an I/O-only card, the card's status bits[23:8] will change, and bit 16 in the response is the value in the I/O-only SD card, bit 15 is COM_CRC_ERROR, Bit 14 is ILLEGAL_COMMAND, Bit 13 is ERROR, Bits[12:0] are reserved.

18.6 Hardware flow control

Using the hardware flow control function can avoid FIFO underflow (transmit mode) and overflow (receive mode) errors.

The operation process of hardware flow control is to stop SDIO_CLK and freeze the SDIO state machine. When the FIFO cannot send and receive data, the data transmission is suspended. It should be noted that only the state machine driven by SDIO_CLK is frozen, the AHB interface is still working. Even when flow control is in effect, the FIFO can still be read from or written to.

The SDIO_CLKCTRL.HWCLKEN bit must be set to '1' to enable hardware flow control. After reset, the hardware flow control function is automatically turned off.

18.7 SDIO register

Devices communicate with the system through control registers. The width of the control registers is 32 bits wide, and these registers can be manipulated on the AHB bus. Note that these peripheral registers must be manipulated in word (32 bits).

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18.7.1 SDIO register overview

Table 18-32 SDIO register overview

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
000h	SDIO_PWRCTRL	Reserved																														PWR CTRL	
	Reset Value																															0	0
004h	SDIO_CLKCTRL	Reserved																DIV[8]	HWCLKEN	CLKEDGE	BUS MODE [1:0]		CLKBYP	PWRCFG	CLOCKEN	DIV[7:0]							
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
008h	SDIO_CMDARG	CMDARG																															
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
00Ch	SDIO_CMDCTRL	Reserved																	CEATAEN	INTDIS	ENCMDF	SUSPEND	CPSMEN	WDATEND	WINTREQ	CMD RESP [1:0]		CMDIDX[5:0]					
	Reset Value																		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
010h	SDIO_CMDRESP	Reserved																										RESPCMDIDX[5:0]					
	Reset Value																											0	0	0	0	0	0
014h	SDIO_RESPONSE1	CARDSTS1[31:0]																															
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
018h	SDIO_RESPONSE2	CARDSTS2[31:0]																															
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
01Ch	SDIO_RESPONSE3	CARDSTS3[31:0]																															
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
020h	SDIO_RESPONSE4	CARDSTS4[31:0]																															
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
024h	SDIO_DTIMER	DATTIMEOUT[31:0]																															
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
028h	SDIO_DATLEN	Reserved							DATLEN[24:0]																								
	Reset Value								0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
02Ch	SDIO_DATCTRL	Reserved																DMADIR	SDIOEN	RWAITMOD	RWAITSTOP	RWAITEN	BLKSIZE[3:0]				DMAEN	TRANSMOD	DATDIR	DATEN		
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
030h	SDIO_DATCOUNT	Reserved							DATCOUNT[24:0]																								
	Reset Value								0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
034h	SDIO_STS	Reserved								CEATAF	SDIOINT	RDATVALID	TDATVALID	RFIFOE	TFIFOE	RFIFOF	TFIFOF	RFIFOHF	TFIFOHE	RXRUN	TXRUN	CMDRUN	DATBLKEND	SBERR	DATEND	CMDSEND	CMDRESPRECV	RXORERR	TXURERR	DATTIMEOUT	CMDTIMEOUT	DCRCERR	CCRCERR
	Reset Value									0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
038h	SDIO_INTCLR	Reserved								CEATAFC	SDIOINTC	Reserved											DATBLKENDC	SBERRC	DATENDC	CMDSENDC	CMDRESPRECVC	RXORERRC	TXURERRC	DATTIMEOUTC	CMDTIMEOUTC	DCRCERRC	CCRCERRC
	Reset Value									0	0												0	0	0	0	0	0	0	0	0	0	0
03Ch	SDIO_INTEN	Reserved								CEATAFEN	SDIOINTEN	RDATVALIDEN	TDATVALIDEN	RFIFOEEN	TFIFOEEN	RFIFOFEN	TFIFOFEN	RFIFOHFEN	TFIFOHEEN	RXRUNEN	TXRUNEN	CMDRUNEN	DATBLKENDEN	SBERREN	DATENDEN	CMDSENDEN	CMDRESPRECVEN	RXORERREN	TXURERREN	DATTIMEOUTEN	CMDTIMEOUTEN	DCRCERREN	CCRCERREN
	Reset Value									0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
048h	SDIO_FIFOCOUNT	Reserved								FIFOCOUNT[23:0]																							
	Reset Value									0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
080h	SDIO_DATFIFO	FIFIDAT[31:0]																															
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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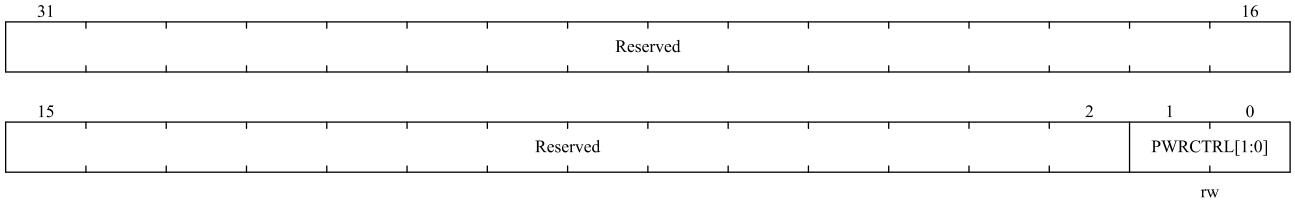
18.7.2 SDIO power control register (SDIO_PWRCTRL)

Address offset: 0x00

Reset value: 0x0000 0000



Bit Field	Name	Description
31:2	Reserved	Reserved, the reset value must be maintained.
1:0	PWRCTRL	Power supply control bits. Defines the current functional state of the card clock: 00: The power is turned off and the clock of the card is stopped. 01: Reserved. 10: Reserved, power-on state. 11: Power-on state, the clock of the card is turned on.

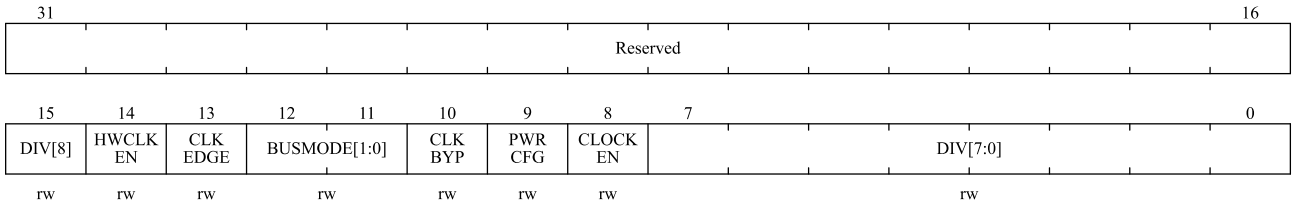
Note: This register cannot be written within 7 HCLK clock cycles after writing data.

18.7.3 SDIO clock control register (SDIO_CLKCTRL)

Address offset: 0x04

Reset value: 0x0000 0000

SDIO_CLKCTRL register controls the SDIO_CLK output clock.



Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained.
15	DIV[8]	The highest bit of the clock frequency division factor, used in extended mode.
14	HWCLKEN	HW Flow Control enable. 0: Disable hardware flow control 1: Enable hardware flow control After hardware flow control is enabled, please refer to the definition of SDIO status register in Section 0 for the meaning of SDIO_STS.TFIFOE and SDIO_STS.RFIFOF interrupt signals.
13	CLKEDGE	SDIO_CLK dephasing selection bit. 0: SDIO_CLK is generated on the rising edge of the master clock SDIOCLK.

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Bit Field	Name	Description
		1: SDIO_CLK is generated on the falling edge of the master clock SDIOCLK.
12:11	BUSMODE	Wide bus mode enable bit. 00: Default bus mode, use SDIO_DAT0. 01: 4-bit bus mode, use SDIO_DAT[3:0]. 10: 8-bit bus mode, use SDIO_DAT[7:0].
10	CLKBYP	Clock divider bypass enable bit. 0: Bypass off: SDIOCLK is divided according to the DIV value before driving the SDIO_CLK output signal. 1: Bypass enabled: SDIOCLK directly drives the SDIO_CLK output signal.
9	PWRCFG	Power saving configuration bit. To save power, the SDIO_CLK clock output can be turned off by setting the PWRCFG bit when the bus is idle. 0: SDIO_CLK is always output. 1: SDIO_CLK is only output when there is bus activity.
8	CLOCKEN	Clock enable bit. 0: SDIO_CLK is off. 1: SDIO_CLK is enabled.
7:1	DIV	Clock divide factor. This field defines the division factor between the input clock (SDIOCLK) and the output clock (SDIO_CLK): SDIO_CLK frequency = SDIOCLK/[DIV + 2].

Notes::

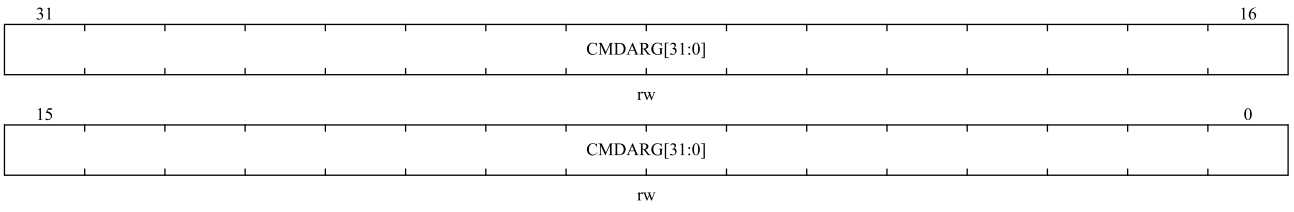
1. *When SD/SDIO card or multimedia card is in identification mode, the frequency of SDIO_CLK must be lower than 400kHz.*
2. *When all cards are assigned corresponding addresses, the clock frequency can be changed to the maximum frequency allowed by the card bus.*
3. *This register cannot be written within 7 HCLK clock cycles after writing data. For SD I/O cards, SDIO_CLK can be stopped during the read wait period, when SDIO_CLKCTRL register does not control SDIO_CLK.*

18.7.4 SDIO command argument register (SDIO_CMDARG)

Address offset: 0x08

Reset value: 0x0000 0000

SDIO_CMDARG register contains the 32-bit command parameter, which will be sent to the card as part of the command.



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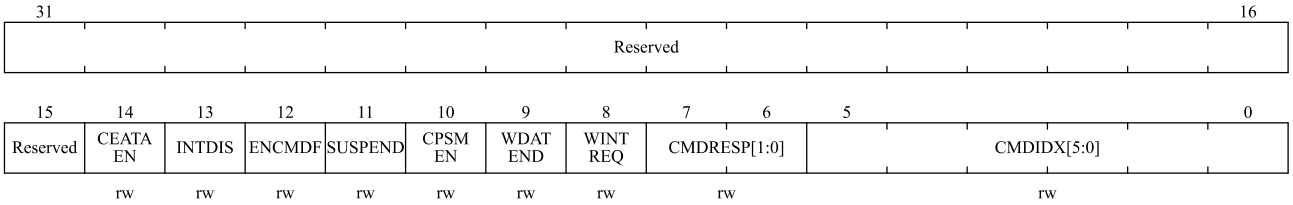
Bit Field	Name	Description
31:0	CMDARG	Command argument. Command parameters are part of the command sent to the card. If a command contains a parameter, this register must be loaded before writing the command to the command register.

18.7.5 SDIO command register (SDIO_CMDCTRL)

Address offset: 0x0C

Reset value: 0x0000 0000

SDIO_CMDCTRL register contains the command index and command type bits. The command index is sent to the card as part of the command. The Command Type bit controls the Command Channel State Machine (CPSM).



Bit Field	Name	Description
31:15	Reserved	Reserved, the reset value must be maintained.
14	CEATAEN	CE-ATA command. If this bit is set, CPSM will transmit CMD61.
13	INTDIS	Not interrupt enable. If this bit is not set, interrupts are enabled for CE-ATA devices.
12	ENCMDF	Enable CMD completion. If this bit is set, the command complete signal is enabled.
11	SUSPEND	SD I/O suspend command. If this bit is set, the command to be sent is a suspend command (for SDIO cards only).
10	CPSMEN	Command path state machine (CPSM) Enable bit. If this bit is set, CPSM is enabled.
9	WDATEND	CPSM Waits for ends of data transfer (CmdPend internal signal). If this bit is set, the CPSM waits for the end of the data transfer before starting to send a command.
8	WINTREQ	CPSM waits for interrupt request. If this bit is set, the CPSM turns off the command timeout control and waits for an interrupt request.
7:6	CMDRESP	Wait for response bits. These 2 bits indicate whether the CPSM needs to wait for a response, and if it needs to wait for a response, the response type. 00: No response, expect SDIO_STS.CMDSEND flag 01: Short response, expect SDIO_STS.CMDRESPRECV or SDIO_STS.CCRCERR flag 10: No response, expect SDIO_STS.CMDSEND flag 11: long response, expect SDIO_STS.CMDRESPRECV or C SDIO_STS.CRCERR flag
5:0	CMDIDX	Command index.

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Bit Field	Name	Description
		The command index is sent to the card as part of the command.

Notes::

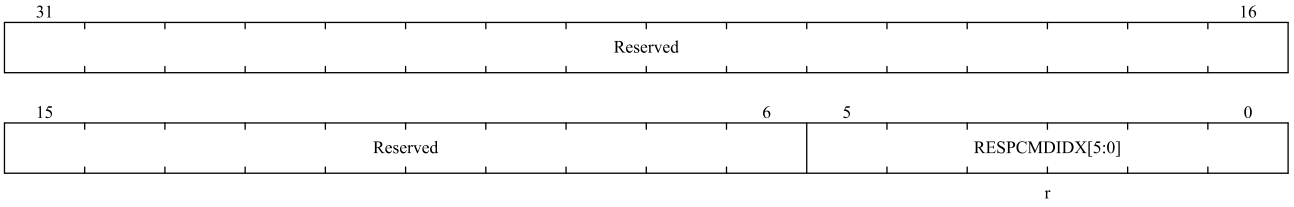
1. *This register cannot be written within 7 HCLK clock cycles after writing data.*
2. *The multimedia card can send 2 kinds of responses: 48-bit short response, or 136-bit long response. SD cards and SD I/O cards can only send short responses, the parameters can be changed according to the type of response, and the software will distinguish the type of response according to the command sent. CE-ATA devices only send short responses.*

18.7.6 SDIO command response register(SDIO_CMDRESP)

Address offset: 0x10

Reset value: 0x0000 0000

SDIO_CMDRESP register contains the command index in the last received command response. If the transmitted command response does not contain a command index (long response or OCR response), although it should contain 111111b (reserved field value in the response), the content of the RESPCMDIDX field is unknown.



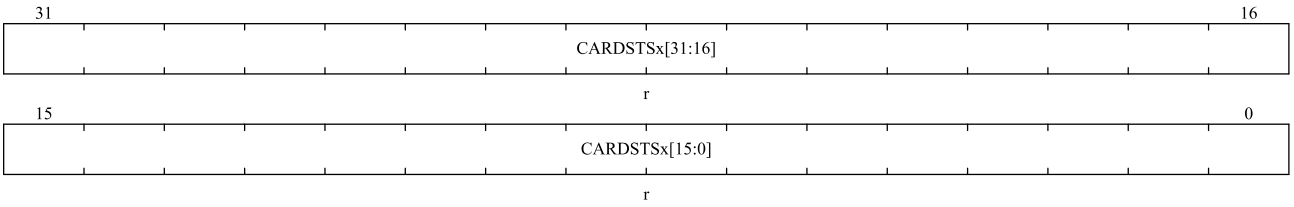
Bit Field	Name	Description
31:6	Reserved	Reserved, the reset value must be maintained.
5:0	RESPCMDIDX	Response command index. Read-only bit that contains the command index in the last command response received.

18.7.7 SDIO response 1..4 register (SDIO_RESPONSEx)

Address offset: 0x14 + 4*(x-1), x = 1..4

Reset value: 0x0000 0000

SDIO_ RESPONSE1/2/3/4 registers contain the status of the card, i.e. the part of the response received.



Bit Field	Name	Description

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31:0	CARDSTSx：	See table below.

Depending on the response status, the card's status length is either 32 bits or 127 bits.

Table 18-33 Response Type and SDIO_RESPONSEx Register

Register	Short response	Long response
SDIO_ RESPONSE1	Card Status[31:0]	Card Status[127:96]
SDIO_ RESPONSE2	Unused	Card Status[95:64]
SDIO_ RESPONSE3	Unused	Card Status[63:32]
SDIO_ RESPONSE4	Unused	Card Status[31:1]

The highest bit of the card status is always received first, and the lowest bit of the SDIO_RESPONSE3 register is always 0.

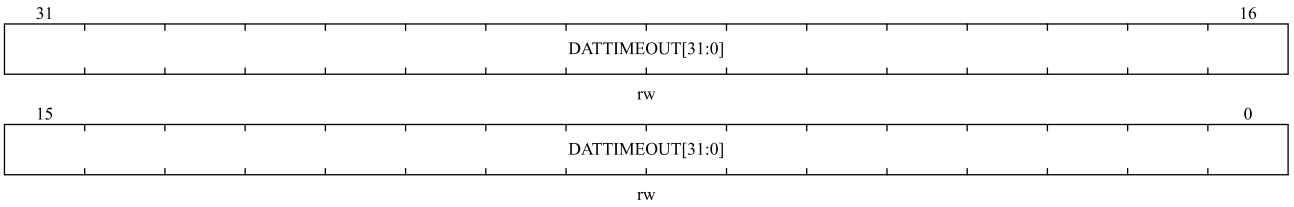
18.7.8 SDIO data timer register (SDIO_DTIMER)

Address offset: 0x24

Reset value: 0x0000 0000

SDIO_DTIMER register contains the data timeout in card bus clock cycles.

A counter loads the value from the SDIO_DTIMER register and counts down when the data path state machine (DPSM) enters the Wait_R or busy state, and sets the timeout flag if the counter decrements to 0 while the DPSM is in these states.



Bit Field	Name	Description
31:0	DATTIMEOUT	Data timeout period. Data timeout in card bus clock cycles.

Note: Before writing to the data control register for data transfer, the data timer register and data length register must be written first.

18.7.9 SDIO data length register (SDIO_DATLEN)

Address offset: 0x28

Reset value: 0x0000 0000

SDIO_DATLEN register contains the length of data bytes to be transferred. When data transfer starts, this value is loaded into the data counter.

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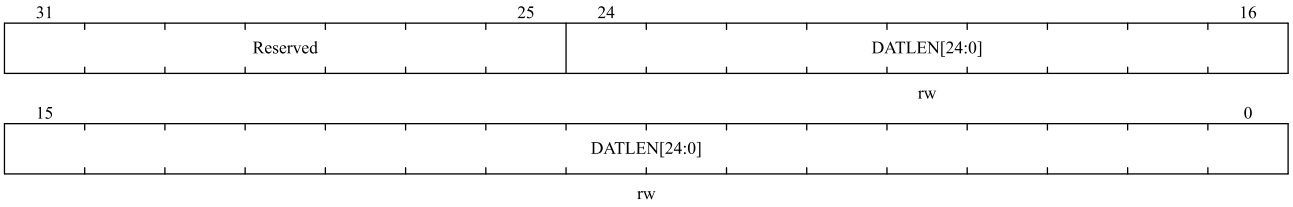


Bit Field	Name	Description
31:25	Reserved	Reserved, the reset value must be maintained.
24:0	DATLEN	Data length value. Number of data bytes to transfer.

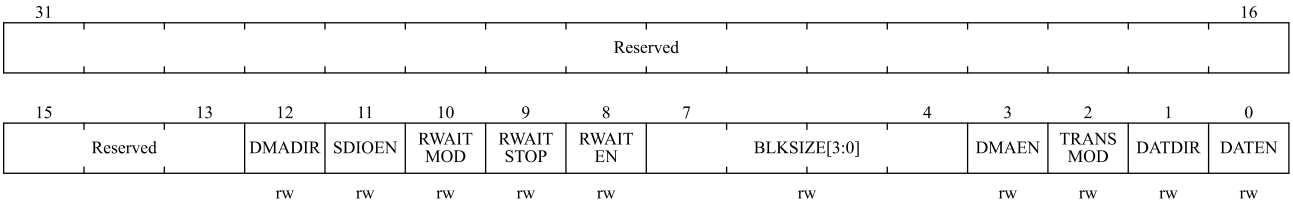
Note: For block data transfers, the value in the data length register must be a multiple of the data block length (see SDIO_DATCTRL). Before writing to the data control register for data transfer, the data timer register and data length register must be written first.

18.7.10 SDIO data control register (SDIO_DATCTRL)

Address offset: 0x2C

Reset value: 0x0000 0000

SDIO_DATCTRL register controls the Data Path State Machine (DPSM).



Bit Field	Name	Description
31:13	Reserved	Reserved, the reset value must be maintained.
12	DMADIR	In DMA mode, it is configured as 1 when data output is transferred to an external device, and configured as 0 when external device data is input.
11	SDIOEN	SD I/O enable functions. If this bit is set, the DPSM performs SD I/O card specific operations.
10	RWAITMOD	Read wait mode. 0: Stop SDIO_CLK control read wait; 1: Use SDIO_DAT2 to control read wait.
9	RWAITSTOP	Read wait stop. 0: If RWAITEN is set, execute read wait; 1: Stop read wait if RWAITEN is set.
8	RWAITEN	Read wait start. Setting this bit starts a read wait operation.
7:4	BLKSIZE[3:0]	Data block size. When block data transfer mode is selected, this field defines the data block length: 0000: block length = 2^0 = 1 byte;

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Bit Field	Name	Description
		0001: block length = 2^1 = 2 bytes; 0010: block length = 2^2 = 4 bytes; 0011: block length = 2^3 = 8 bytes; 0100: (decimal 4) block length=2^4=16 bytes; 0101: (decimal 5) block length=2^5=32 bytes; 0110: (decimal 6) block length = 2^6 = 64 bytes; 0111: block length = 2^7 = 128 bytes; 1000: block length = 2^8 = 256 bytes; 1001: block length = 2^9 = 512 bytes; 1010: block length = 2^{10} = 1024 bytes; 1011: block length = 2^{11} = 2048 bytes; 1100: block length=2^{12}=4096 bytes; 1101: block length=2^{13}=8192 bytes; 1110: block length = 2^{14} = 16384 bytes; 1111: reserved.
3	DMAEN	DMA enable bit. 0: Turn off DMA; 1: Enable DMA.
2	TRANSMOD	Data transfer mode selection. 0: block data transfer; 1: Streaming data transmission.
1	DATDIR	Data transfer direction selection. 0: controller to card; 1: Card to the controller.
0	DATEN	Data transfer enabled bit. If this bit is set to 1, data transfer starts. Depending on the DATDIR direction bit, the DPSM enters the Wait_S or Wait_R state, and if the RWAITEN bit is set at the very beginning of the transfer, the DPSM enters the read wait state. The enable bit does not need to be cleared after a data transfer, but SDIO_DATCTRL must be changed to allow a new data transfer.

Note: This register cannot be written within 7 HCLK clock cycles after writing data.

18.7.11 SDIO data counter register (SDIO_DATCOUNT)

Address offset: 0x30

Reset value: 0x0000 0000

When the DPSM enters the Wait_R or Wait_S state from the idle state, the SDIO_DATCOUNT register loads the value from the data length register (see SDIO_DATLEN). During the data transfer, the value of this counter is decremented until it is reduced to 0, then the SDIO_STS.DPSM enters the idle state and sets the data state End mark DATEND.

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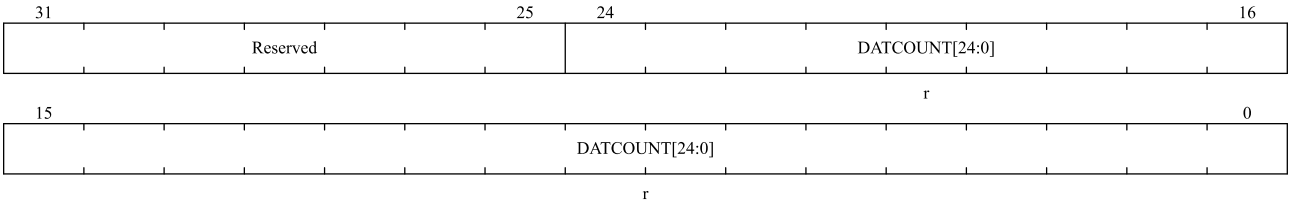


Bit Field	Name	Description
31:25	Reserved	Reserved, the reset value must be maintained.
24:0	DATCOUNT	Data count value. When reading this register, it returns the number of data bytes to be transmitted. Writing this register has no effect.

Note: This register can only be read at the end of a data transfer.

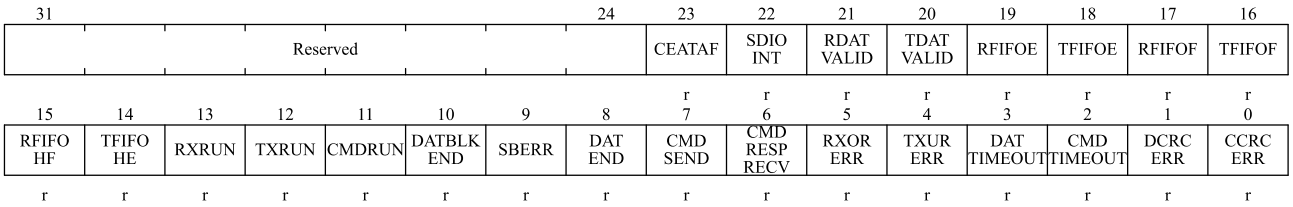
18.7.12 SDIO status register (SDIO_STS)

Address offset: 0x34

Reset value: 0x0000 0000

SDIO_STS is a read-only register that contains two types of flags:

- Static flags (bits[23:22, 10:0]): These bits can be cleared by writing to the SDIO Interrupt Clear Register (see SDIO_ INTCLR).
- Dynamic flags (bits[21:11]): The state of these bits changes according to the part of the logic they correspond to (eg: FIFO full and empty flags go high or low with data writes to the FIFO).



Bit Field	Name	Description
31:24	Reserved	Reserved, the reset value must be maintained.
23	CEATAF	CE-ATA command completion signal received for CMD61.
22	SDIOINT	SDIO interrupt received.
21	RDATVALID	Data available in receive FIFO.
20	TDATVALID	Data available in transmit FIFO.
19	RFIFOE	Receive FIFO empty.
18	TFIFOE	Transmit FIFO empty. If hardware flow control is used, the TFIFOE signal becomes active when the FIFO contains 2 words.
17	RFIFOF	Receive FIFO full. If hardware flow control is used, the RFIFOF signal becomes active when the FIFO is still 2 words full.

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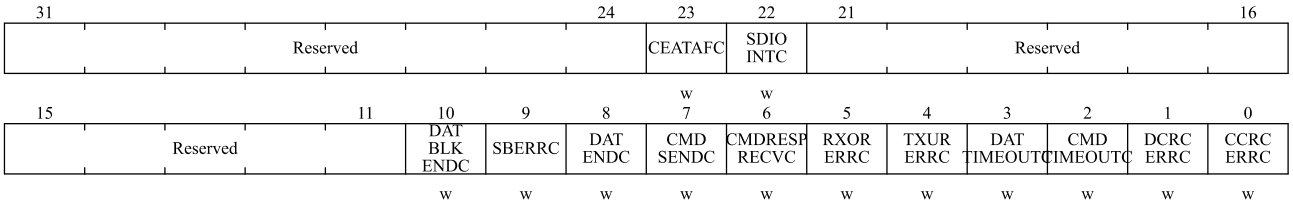
Bit Field	Name	Description
16	TFIFOF	Transmit FIFO full.
15	RFIFOHF	Receive FIFO half full: There are at least 8 words left in the FIFO.
14	TFIFOHE	Transmit FIFO half empty: At least 8 more words can be written to the FIFO.
13	RXRUN	Data receive in progress.
12	TXRUN	Data transmit in progress.
11	CMDRUN	Command transfer in progress.
10	DATBLKEND	Data block sent/received (CRC check passed).
9	SBERR	Start bit not detected on all data signals in wide bus mode.
8	DATEND	Data end (Data counter, SDIDCOUNT, is zero).
7	CMDSEND	Command sent (no response required).
6	CMDRESPRECV	Command response (CRC check passed).
5	RXORERR	Received FIFO overrun error.
4	TXURERR	Transmit FIFO underrun error.
3	DATTIMEOUT	Data timeout.
2	CMDTIMEOUT	Command response timeout. The command timeout is a fixed value of 64 SDIO_CLK clock cycles.
1	DCRCERR	Data block sent/received (CRC check failed).
0	CCRCERR	Command response received (CRC check failed).

18.7.13 SDIO interrupt clear register (SDIO_INTCLR)

Address offset: 0x38

Reset value: 0x0000 0000

SDIO_INTCLR is a write-only register, writing '1' in the corresponding register bit will clear the corresponding bit in the SDIO_STS status register.



Bit Field	Name	Description
31:24	Reserved	Reserved, the reset value must be maintained.
23	CEATAFC	CEATAF flag clear bit. Software sets this bit to clear the SDIO_STS.CEATAF flag.
22	SDIOINTC	SDIOINT flag clear bit. Software sets this bit to clear the SDIO_STS.SDIOINT flag.
21:11	Reserved	Reserved, the reset value must be maintained.
10	DATBLKENDC	DATBLKEND flag clear bit.

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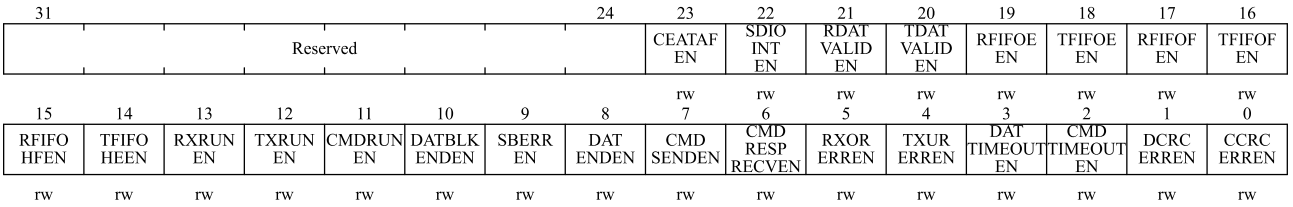
Bit Field	Name	Description
		Software sets this bit to clear the SDIO_STS.DATBLKEND flag.
9	SBERRC	SBERR flag clear bit. Software sets this bit to clear the SDIO_STS.SBERR flag.
8	DATENDC	DATEND flag clear bit. Software sets this bit to clear the SDIO_STS.DATEND flag.
7	CMDSENDC	CMDSEND flag clear bit. Software sets this bit to clear the SDIO_STS.CMDSEND flag.
6	CMDRESPRECVC	CMDRESPRECV flag clear bit. Software sets this bit to clear the SDIO_STS.CMDRESPRECV flag.
5	RXORERRC	RXORERR flag clear bit. Software sets this bit to clear the SDIO_STS.RXORERR flag.
4	TXURERRC	TXURERR flag clear bit. Software sets this bit to clear the SDIO_STS.TXURERR flag.
3	DATTIMEOUTC	DATTIMEOUT flag clear bit. Software sets this bit to clear the SDIO_STS.DATTIMEOUT flag.
2	CMDTIMEOUTC	CMDTIMEOUT flag clear bit. Software sets this bit to clear the SDIO_STS.CMDTIMEOUT flag.
1	DCRCERRC	DCRCERR flag clear bit. Software sets this bit to clear the SDIO_STS.DCRCERR flag.
0	CCRCERRC	CCRCERR clear bit. Software sets this bit to clear the SDIO_STS.CCRCERR flag.

18.7.14 SDIO interrupt enable register (SDIO_INTEN)

Address offset: 0x3C

Reset value: 0x0000 0000

In the corresponding bit '1', the SDIO_INTEN interrupt enable register determines which status bit generates the interrupt.



Bit Field	Name	Description
31:24	Reserved	Reserved, the reset value must be maintained.
23	CEATAFEN	CE-ATA command completion signal received interrupt enable. Setting/clearing this bit by software to enable/disable interrupt generation upon receipt of CE-ATA command completion signal. 0: No interrupt is generated when the CE-ATA command completion signal is received 1: An interrupt is generated when the CE-ATA command completion signal is received

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Bit Field	Name	Description
22	SDIOINTEN	SDIO mode interrupt received interrupt enable Setting/clearing this bit by software to enable/disable the SDIO mode interrupt received interrupt function. 1: SDIO mode interrupt has been received and no interrupt will be generated 0: SDIO mode interrupt has been received and an interrupt is generated
21	RDATVALIDEN	Data available in Rx FIFO interrupt enable. Setting/clearing this bit by software to enable/disable the data valid interrupt in the receive FIFO. 0: The data in the receiving FIFO is valid and no interrupt is generated 1: The data in the receiving FIFO is valid to generate an interrupt
20	TDATVALIDEN	Data available in Rx FIFO interrupt enable. Setting/clearing this bit by software to enable/disable the data valid interrupt in the transmit FIFO. 0: The data in the transmit FIFO is valid and no interrupt is generated 1: The data in the transmit FIFO is valid to generate an interrupt
19	RFIFOEEN	Rx FIFO empty interrupt enable. Setting/clearing this bit by software to enable/disable the data valid interrupt in the transmit FIFO. 0: The data in the transmit FIFO is valid and no interrupt is generated 1: The data in the transmit FIFO is valid to generate an interrupt
18	TFIFOEEN	Tx FIFO empty interrupt enable. Setting/clearing this bit by software to enable/disable the transmit FIFO empty interrupt. 0: No interrupt will be generated when the transmit FIFO is empty 1: Transmit FIFO empty and generate interrupt
17	RFIFOFEN	Rx FIFO full interrupt enable. Setting/clearing this bit by software enables/disables the receive FIFO full interrupt. 0: No interrupt will be generated when the receive FIFO is full 1: Receive FIFO full and generate an interrupt
16	TFIFOFEN	Tx FIFO full interrupt enable. Setting/clearing this bit by software to enable/disable the transmit FIFO full interrupt. 0: No interrupt will be generated when the transmit FIFO is full 1: Transmit FIFO full generates an interrupt
15	RFIFOHFEN	Rx FIFO half full interrupt enable. Setting/clearing this bit by software enables/disables the receive FIFO half-full interrupt. 0: No interrupt is generated when the receive FIFO is half full 1: Interrupt generated when the receive FIFO is half full
14	TFIFOHEEN	Tx FIFO half empty interrupt enable. Setting/clearing this bit by software to enable/disable the transmit FIFO half-empty interrupt. 0: No interrupt is generated when the transmit FIFO is half-empty 1: Transmit FIFO half empty to generate interrupt
13	RXRUNEN	Data receive acting interrupt enable. Setting/clearing this bit by software to enable/disable the receiving data interrupt. 0: Data is being received without generating an interrupt 1: Interrupt when data is being received
12	TXRUNEN	Data transmit acting interrupt enable. Setting/clearing this bit by software to enable/disable the Transmitting Data interrupt.

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Bit Field	Name	Description
		0: Data is being sent without generating an interrupt 1: Interrupt when data is being sent
11	CMDRUNEN	Command acting interrupt enable. Setting/clearing this bit by software to enable/disable the command-in-transit interrupt. 0: Transmitting command without interrupt 1: Interrupt when command is being transmitted
10	DATBLKENDEN	Data block end interrupt enable. Setting/clearing this bit by software enables/disables the end of block transfer interrupt. 0: No interrupt is generated at the end of data block transfer 1: Interrupt generated at the end of data block transfer
9	SBERREN	Start bit error interrupt enable. Setting/clearing this bit by software to enable/disable start bit error interrupt. 0: Start bit error does not generate an interrupt 1: Start bit error generates an interrupt
8	DATENDEN	Data end interrupt enable. Set/clear this bit by software to enable/disable end of data transfer interrupt. 0: No interrupt will be generated at the end of data transfer 1: Interrupt generated at the end of data transfer
7	CMDSENDEN	Command sent interrupt enable. Setting/clearing this bit by software to enable/disable the command sent interrupt. 0: The command has been sent without generating an interrupt 1: The command has been sent to generate an interrupt
6	CMDRESPRECVEN	Command response received interrupt enable. Setting/clearing this bit by software to enable/disable the receive acknowledge interrupt. 0: No interrupt is generated when a response is received 1: Receive a response and generate an interrupt
5	RXORERREN	Rx FIFO overrun error interrupt enable. Setting/clearing this bit by software to enable/disable the receive FIFO overflow error interrupt. 0: Receive FIFO overflow error does not generate an interrupt 1: Receive FIFO overflow error generates interrupt
4	TXURERREN	Tx FIFO underrun error interrupt enable. Setting/clearing this bit by software to enable/disable the transmit FIFO underflow error interrupt. 0: Transmit FIFO underflow error does not generate an interrupt 1: Transmit FIFO underflow error generates an interrupt
3	DATTIMEOUTEN	Data timeout interrupt enable. Setting/clearing this bit by software to enable/disable the data timeout interrupt. 0: Data timeout does not generate an interrupt 1: Data timeout generates an interrupt
2	CMDTIMEOUTEN	Command timeout interrupt enable. Setting/clearing this bit by software to enable/disable the command timeout interrupt. 0: Command timeout does not generate an interrupt 1: Command timeout generates an interrupt
1	DCRCERREN	Data CRC fail interrupt enable.

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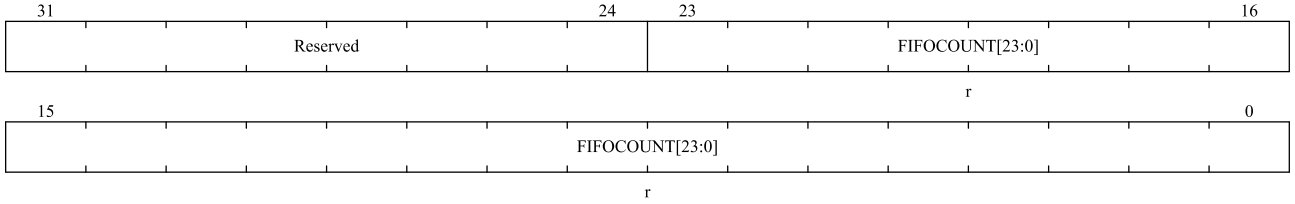
Bit Field	Name	Description
		Setting/clearing this bit by software to enable/disable the interrupt for block CRC detection failure. 0: Data block CRC detection failure does not generate an interrupt 1: Data block CRC detection failure generates an interrupt
0	CCRCERREN	Command CRC fail interrupt enable. Setting/clearing this bit by software to enable/disable the command CRC detection failure interrupt. 0: Command CRC detection failure does not generate an interrupt 1: Command CRC detection failure generates an interrupt

18.7.15 SDIO FIFO counter register (SDIO_FIFOCOUNT)

Address offset: 0x48

Reset value: 0x0000 0000

The SDIO_FIFOCOUNT register contains the number of data words that have not been written to or read from the FIFO. When the data transfer enable bit SDIO_DATCTRL.DATEN is set and the DPSM is idle, the FIFO counter is loaded with the value from the data length register (see SDIO_DATLEN). If the data length is not word-aligned (a multiple of 4), the last remaining 1~3 bytes are treated as a word.



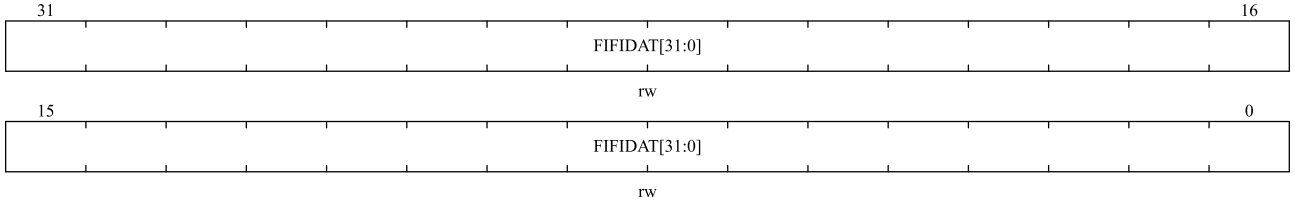
Bit Field	Name	Description
31:24	Reserved	Reserved, the reset value must be maintained.
23:0	FIFOCOUNT	The number of data words to be written to or read from the FIFO.

18.7.16 SDIO data FIFO register (SDIO_DATFIFO)

Address offset: 0x80

Reset value: 0x0000 0000

The receive and transmit FIFO is a 32-bit wide read or write set of registers, it contains 32 registers on consecutive 32 addresses, the CPU can use the FIFO to read and write multiple operands.



Bit Field	Name	Description
31:0	FIFIDAT	Receive and transmit FIFO data.

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		The FIFO data occupies 32 entries of 32-bit words at the address: (SDIO base address + 0x80) to (SDIO base address + 0xFC)

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19 Universal Serial Bus Full-speed Device Interface (USB_FS_Device)

19.1 Introduction

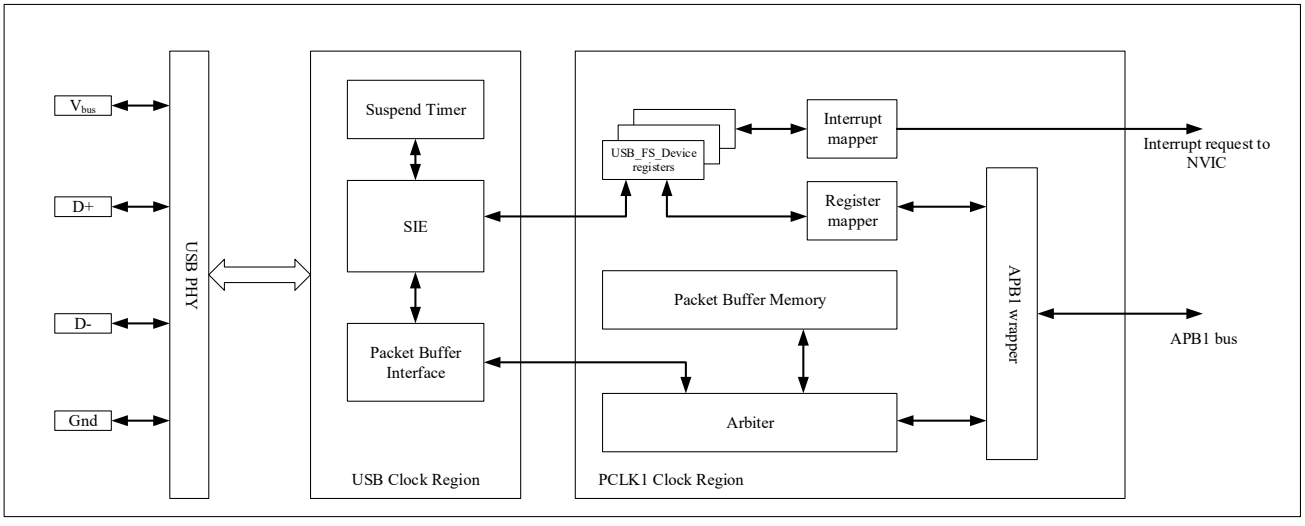
Universal serial bus full-speed device interface (USB_FS_Device) module is a peripheral that conforms to the USB2.0 full-speed protocol. It contains the USB PHY of the physical layer and does not require an additional PHY chip. USB_FS_Device supports four transfer types defined in USB2.0 protocol: control transfer, bulk transfer, interrupt transfer and isochronous transfer.

19.2 Main features

- Comply with USB2.0 full-speed device specification
- Supports up to 8 configurable USB endpoints
- Each endpoint supports four transfer types in the USB2.0 protocol:
  - Control transfer
  - Bulk transfer
  - Interrupt transfer
  - Isochronous transfer
- Bulk endpoint/isochronous endpoint supports double buffering mechanism
- Cyclic redundancy check (CRC) generation/checking, non-return-to-zero inverted (NRZI) encoding/decoding and bit-stuffing
- Support USB suspend/resume operation
- Frame lock clock pulse generation

Figure 19-1 is a functional block diagram of a USB peripheral.

Figure 19-1 USB device block diagram



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19.3 Clock configuration

The USB 2.0 protocol specification stipulates that the USB full-speed module uses a fixed 48MHz clock. In order to provide an accurate 48MHz clock to USB_FS_Device, a two-stage clock configuration is required, as follows:

- In the first stage, the 48MHz working clock is obtained by accurate frequency division of PLLCLK, so when using USB_FS_Device, it is necessary to ensure that the PLLCLK clock is 48MHz/72MHz/96MHz/144MHz, otherwise USB_FS_Device cannot work normally;
- In the second stage, enable the USB peripheral clock mounted on the APB1 bus, that is, the APB1 bus clock. Its frequency does not have to be equal to 48MHz, but can be greater or less than 48MHz.

Note: The frequency of the APB1 bus clock must be greater than 8MHz, otherwise the data buffer may overflow/underflow.

19.4 Functional description

Based on this module, data exchange can be realized between the microcontroller and the PC host through a USB connection. The data transfer between the microcontroller and the PC host is based on a 512-byte dedicated SRAM, which is the Packet Buffer Memory in Figure 19-1. USB peripherals can directly access this SRAM. The actual usage size of this dedicated SRAM is determined by the number of endpoints used and the endpoint packet buffer size of each endpoint. Each endpoint has a buffer description table entry, which describes the buffer address, size and the number of bytes that need to be transferred. For details, please refer to 19.4.2 Buffer Description Table. The SRAM is mapped to the APB1 peripheral memory area, its address is from 0x4000 6000 to 0x4000 63FF, the total capacity is 1KB, but only 512 bytes are used due to the bus width, and the buffer description table of each endpoint is also stored in this SRAM, so the maximum endpoint packet buffer that can be used by each endpoint is less than 512 bytes.

Note: USB and CAN1 share this SRAM, so USB and CAN1 cannot be used at the same time.

19.4.1 Access Packet Buffer Memory

As shown in Figure 19-1, the microcontroller communicates with the USB module through the APB1 bus, and the microcontroller accesses the Packet Buffer Memory through the APB1 wrapper. When the microcontroller and the USB module both access the Packet Buffer Memory, the Arbiter decides who can access, the arbitration logic is that half of the APB1 bus cycle is used for the microcontroller to access the Packet Buffer Memory, and the other half of the cycle is used for the USB module to access the Packet Buffer Memory, in this way, the access conflicts caused by the continuous access of the microcontroller to the Packet Buffer Memory can be avoided.

Note: APB1 bus and USB module access Packet Buffer Memory in different ways.

19.4.1.1 USB module access Packet Buffer Memory

The USB module accesses the Packet Buffer Memory in 16-bit mode, refer to Figure 19-2. When the USB module accesses the Packet Buffer Memory, first find the location of the buffer description table in the Packet Buffer Memory through the USB_BUFTAB register. The value of the USB_BUFTAB register indicates the starting address of the buffer description table, which must be within the memory range of the Packet Buffer Memory and be 8-byte aligned. If only endpoint 0 and endpoint 1 are used, the buffer description table only needs 16 bytes. If only endpoint 0 and endpoint 7 are used, the buffer description table needs 64 bytes. Although endpoint 1 to endpoint 6 are not used, but

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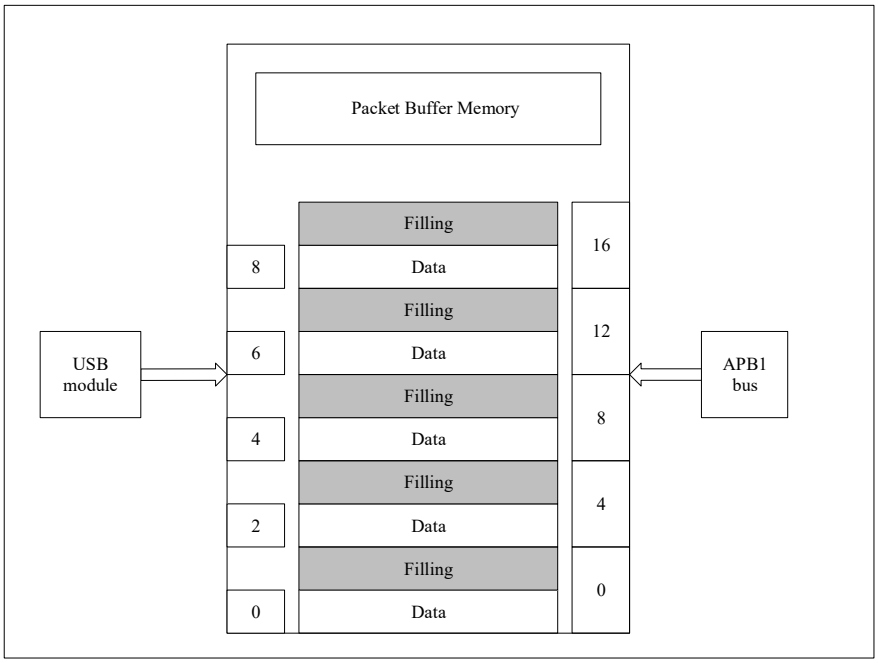
The description table of endpoint 7 starts from 56 bytes, so it will occupy 64 bytes of space.

19.4.1.2 User application access Packet Buffer Memory

The user application program on the microcontroller needs to access the Packet Buffer Memory from the APB1 bus according to 32-bit alignment and 16-bit read and write access, that is, the address of the operation data must be 32-bit aligned, and only 16-bit data can be read or written at a time, can't be 8-bit nor 32-bit. Figure 19-2 shows the way in which the user application program on the microcontroller and the USB module accesses the Packet Buffer Memory.

Figure 19-2 The user applications on the microcontrollers and the USB modules access Packet Buffer Memory



19.4.2 Buffer description table

The buffer description table defines the buffer address, size and the number of bytes to be transmitted for the endpoint used in the communication process. Each endpoint corresponds to two endpoint data packet buffers, one for sending and one for receiving. These endpoint packet buffers can be stored anywhere in the entire Packet Buffer Memory, and the buffer description table is also located in the Packet Buffer Memory, whose starting address is determined by the USB_BUFTAB register.

The buffer description table has a total of 8 entries, each entry corresponds to an endpoint register, each register has two directions of sending and receiving, and each direction requires two 16-bit word buffer description tables, so each table items consist of four 16-bit words, so the start address of the buffer description table must be 8-byte aligned. Endpoint packet buffers for unused endpoints or in the unused direction of a used endpoint may be used for other purposes. The relationship between the buffer description table and the endpoint packet buffer is shown in Figure 19-3 below.

Whether the endpoint is used for receiving or sending, the buffer description table starts with the first entry, which is the very bottom of the buffer description table. The USB module cannot access/modify the data of other endpoint packet buffers other than the currently allocated endpoint packet buffer area, For example: when the endpoint 0 packet receive buffer receives a data larger than the current endpoint 0 packet receive buffer from the PC host, the endpoint

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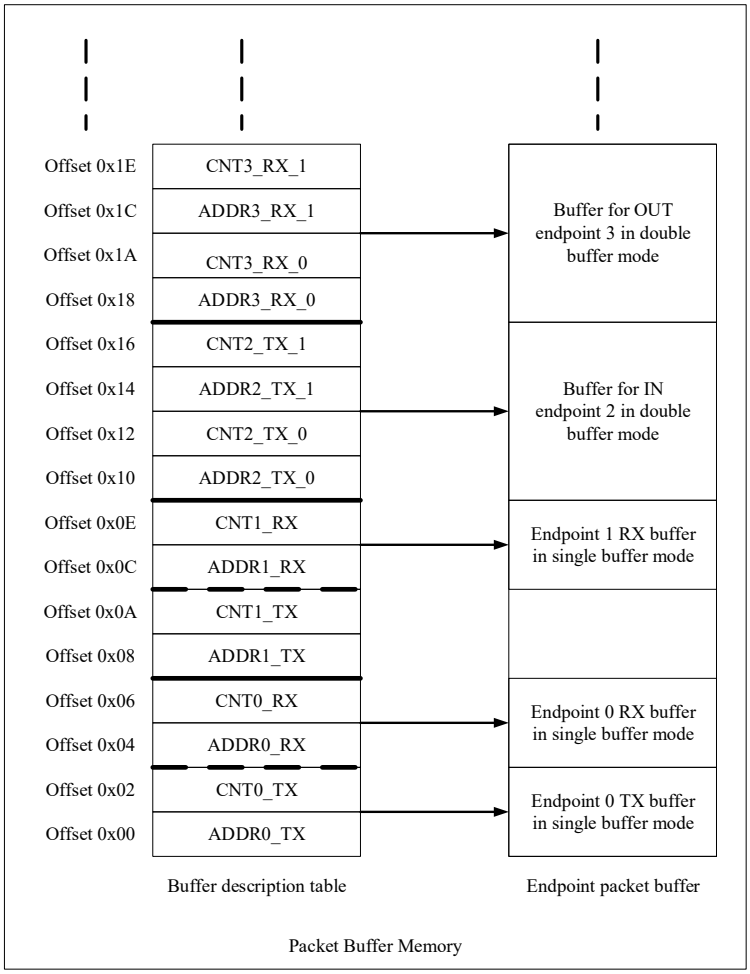
0 only receives data up to the endpoint 0 packet receive buffer size, other redundant data is discarded and a buffer overflow exception occurs.

Figure 19-3 The relationship between the buffer description table and the endpoint packet buffer



19.4.3 Double-buffered endpoints

19.4.3.1 Double buffer endpoint function introduction

When a large amount of data needs to be transmitted between the PC host and the USB device, the use of bulk transmission allows the PC host to transmit data with maximum efficiency within one frame. However, when the transmission speed is too fast, the USB device will receive a new data packet when the USB device is processing the previous data transmission. In order to correctly complete the previous data transmission, the USB can only reply the NAK handshake signal to the PC host. Due to the retransmission mechanism of bulk transfer, the PC host will continue to retransmit the same data packet until the USB device can process the data packet and reply to the PC host with an ACK handshake signal, the PC host will stop retransmitting the data packet. Such retransmission will occupy a lot of bandwidth, thereby reducing the rate of bulk transfer. In order to solve this problem, a double buffering mechanism is introduced to improve the efficiency of bulk transfer, and flow control is implemented.

When the unidirectional endpoint uses the double buffer mechanism, both the receive buffer and the transmit buffer on the endpoint will be used, one of the buffers is used by the USB module, and the other buffer is used by the microcontroller, use the data toggle bit in the endpoint register to select which buffer is currently used, and introduce

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two flags for this: DATTOG and SW_BUF. DATTOG indicates the buffer currently being used by the USB module, and SW_BUF indicates the buffer currently being used by the application on the microcontroller. The definitions of DATTOG and SW_BUF are shown in Table 19-1 shown. A unidirectional endpoint using the double buffer mechanism only needs to use one USB_EPn register.

Table 19-1 DATTOG and SW_BUF definitions

Buffer flag	Sending endpoint	Receiving endpoint
DATTOG	DATTOG_TX (Bit 6 of the USB_EPn register)	DATTOG_RX (Bit 14 of the USB_EPn register)
SW_BUF	Bit 14 of the USB_EPn register	Bit 6 of the USB_EPn register

As shown in Figure 19-3, when an endpoint uses the double buffer mechanism, all four buffer description table entries of the endpoint will be used. DATTOG and SW_BUF are responsible for flow control. When a transfer is complete, the USB hardware toggles the DATTOG bit; when the application on the microcontroller has finished processing the data, the software toggles SW_BUF bit. After the first transfer starts, in the subsequent transfer process, if the values of DATTOG and SW_BUF are equal, a buffer access conflict occurs between the USB module and the application, the transfer is paused, and a NAK handshake packet is sent to the host; when the values of DATTOG and SW_BUF are not equal, normal USB communication can be performed.

Table 19-2 How to use double buffering

Endpoint type	DATTOG	SW_BUF	Buffer used by the USB module	Buffers used by the application
IN Endpoint	0	1	ADDRn_TX_0/CNTn_TX_0	ADDRn_TX_1/CNTn_TX_1
	1	0	ADDRn_TX_1/CNTn_TX_1	ADDRn_TX_0/CNTn_TX_0
	0	0	Endpoint is in NAK state	ADDRn_TX_0/CNTn_TX_0
	1	1	Endpoint is in NAK state	ADDRn_TX_1/CNTn_TX_1
OUT Endpoint	0	1	ADDRn_RX_0/CNTn_RX_0	ADDRn_RX_1/CNTn_RX_1
	1	0	ADDRn_RX_1/CNTn_RX_1	ADDRn_RX_0/CNTn_RX_0
	0	0	Endpoint is in NAK state	ADDRn_RX_0/CNTn_RX_0
	1	1	Endpoint is in NAK state	ADDRn_RX_1/CNTn_RX_1

Note: The double-buffered bulk endpoint will only set the endpoint to the NAK state when there is a buffer access conflict, and will not set the endpoint to the NAK state after each correct transmission is completed.

19.4.3.2 Double-buffered endpoint usage

If you want to use double-buffered bulk endpoints, you can set them up as follows:

- Set USB_EPn.EP_TYPE = 00, define the endpoint as a bulk endpoint
- Set USB_EPn.EP_KIND = 1, define endpoint as double buffer endpoint

As shown in Figure 19-3, when double-buffered bulk endpoint 3 performs data transmission in the OUT direction, assuming DATTOG = 1 and SW_BUF = 0, it means that the application can process the data in buffer0 corresponding to ADDR3_RX_0/CNT3_RX_0, after receiving the data from the USB bus, the USB module fills the data into the buffer1 corresponding to ADDR3_RX_1/CNT3_RX_1. When a transaction transfer on the USB bus is completed, the hardware will toggle DATTOG = 0. If the application has not finished processing the data in buffer0 corresponding to ADDR3_RX_0/CNT3_RX_0, the software will not toggle SW_BUF (SW_BUF = 0). If there is another OUT data packet transmission on the USB bus at this time, the USB device will automatically reply the NAK handshake signal to indicate flow control until the application finishes processing the data in buffer0 corresponding

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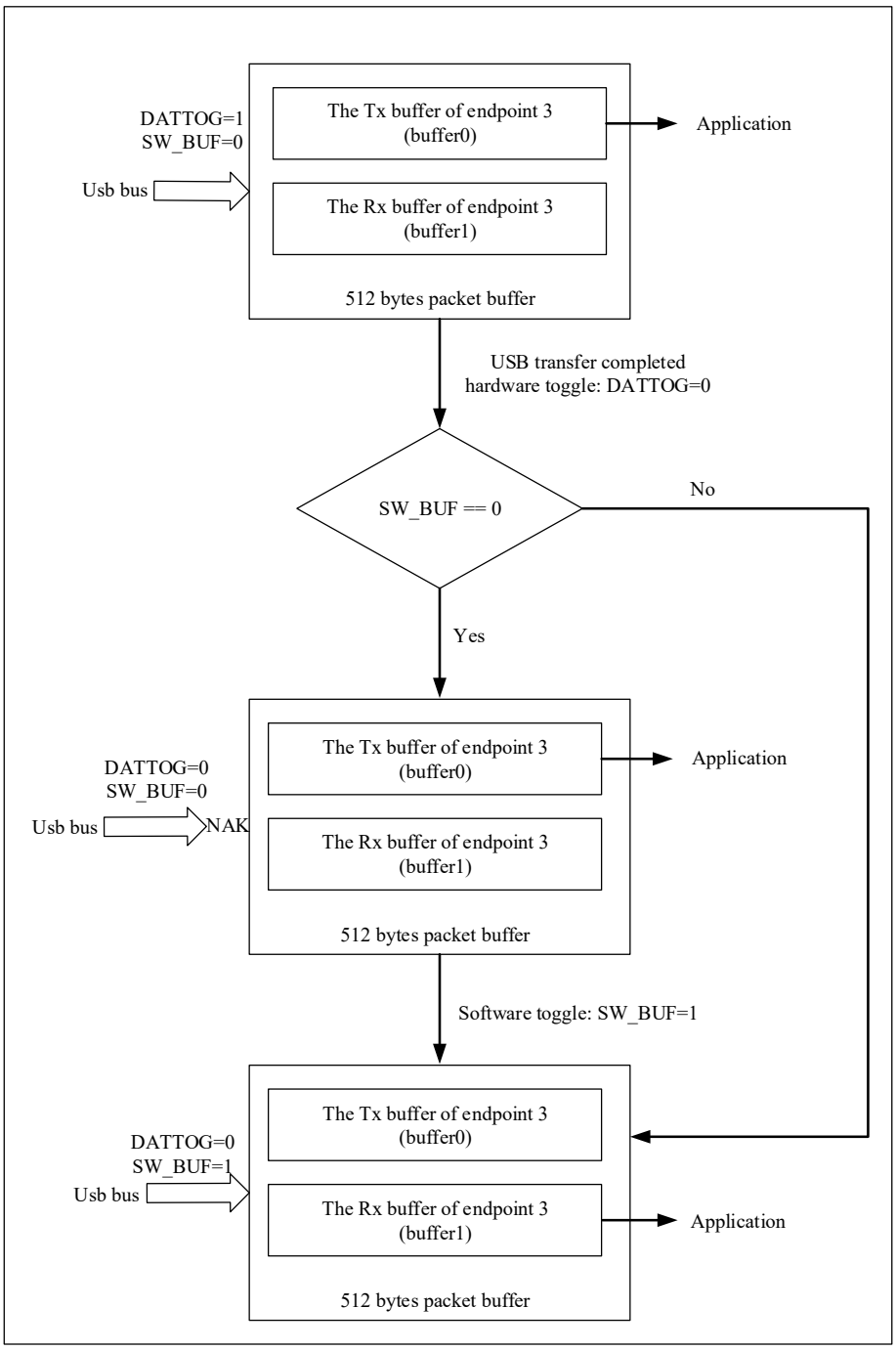
to ADDR3_RX_0/CNT3_RX_0, and the software toggle SW_BUF = 1. In this case, the DATTOG and SW_BUF values are different. If there is another OUT data packet transmission on the USB bus, the USB device can receive data normally, and fill the received data into buffer0 corresponding to ADDR3_RX_0/CNT3_RX_0, and the application can process the buffer1 corresponding to ADDR3_RX_1/CNT3_RX_1. As shown in Figure 19-4 below.

Figure 19-4 Double buffered bulk endpoint example



19.4.4 USB transfer

19.4.4.1 Overview of USB transfer

A USB transfer consists of multiple transactions, and a transaction consists of multiple packets.

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A packet is the basic unit of USB transmission. All data must be packaged before being transmitted on the USB bus. The process of one time receiving or sending data on the USB is called a transaction, and there are three types of transactions: Setup transaction, Data IN transaction, and Data OUT transaction.

19.4.4.2 IN transaction

When the host wants to read the data of the USB device, the host sends a PID IN token packet to the USB device. After the USB device receives the IN token packet correctly, if the address matches a configured endpoint address, the USB module will access the corresponding USB_ADDRn_TX and USB_CNTn_TX registers according to the buffer description table entry of the endpoint, and store the values in these two registers to the internal 16-bit ADDR register and CNT register that cannot be accessed by the application. The ADDR register is used as a pointer to the endpoint's corresponding endpoint packet send buffer, and the CNT register is used to record the number of remaining untransferred bytes. The USB bus uses the low byte first method to read data from the endpoint data packet sending buffer. The data starts to read data from the endpoint data packet sending buffer pointed to by USB_ADDRn_TX, and the length is USB_CNTn_TX/2 words. If the data packet sent is an odd number of bytes, only the lower 8 bits of the last word are used.

After the USB device receives the PID IN token packet sent by the host, the USB processing flow for the IN transaction is as follows:

- If the device address information and endpoint information in this IN token packet are valid, and the status of the endpoint specified in the token packet is VALID, the USB device sends a PID DATA0 or DATA1 packet according to the USB_EPn.DATTOG_TX bit, send the prepared data to the host, when the last data byte is sent, the calculated data CRC will also be sent to the host. After the USB device receives the PID ACK handshake packet returned by the host. The hardware toggles the USB_EPn.DATTOG_TX bit, the hardware sets the endpoint's sending state to NAK state (USB_EPn.STS_TX = 10), and the hardware sets USB_EPn.CTRS_TX bit to generate a correct sending interrupt. The software responds to the CTRS_TX interrupt, identifies which endpoint the communication is on by checking the USB_STS.EP_ID bit, identifies the communication direction through USB_STS.DIR, clears the interrupt flag, and prepares the next data to be sent, and then the software sets the endpoint sending status to VALID status (USB_EPn.STS_TX = 11).
- If the endpoint specified in this IN token packet is invalid, the USB device does not send data packets, but sends PID NAK or STALL handshake packets according to USB_EPn.STS_TX.

19.4.4.3 OUT and SETUP transaction

When the host wants to send data or commands to the USB device, the host will send the PID OUT or SETUP token packet to the USB device. After the USB device receives the OUT or SETUP token correctly, if the address matches a configured endpoint address, the USB module will access the corresponding USB_ADDRn_RX and USB_CNTn_RX registers according to the buffer description table entry of the endpoint. Store the value of the USB_ADDRn_RX register into the internal ADDR register, and reset the internal CNT register at the same time. The ADDR register is used as a pointer to the endpoint data packet receiving buffer corresponding to the endpoint, and the CNT register is used to record the number of received data bytes, and initialize the internal 16-bit BUF_COUNT register that cannot be accessed by the application program with the BL_SIZE and NUM_BLK values in the USB_CNTn_RX register, which is used for buffer overflow detection. When the USB module receives data from the USB bus, the USB module organizes the received data in words (the first received is the low byte), and store it in the endpoint data packet receiving buffer pointed to by ADDR, at the same time, the CNT value is automatically incremented, and the BUF_COUNT value is automatically decremented.

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After the USB device receives the PID OUT or SETUP token packet sent by the host, the USB processing flow for OUT or SETUP is as follows:

- If the device address information and endpoint information in the OUT or SETUP token packet are valid, and the status of the endpoint specified in the token packet is VALID, USB device moves data from the hardware buffer that cannot be accessed by the application to the endpoint data packet receiving buffer that can be accessed by the application. Then the USB device checks the received CRC. If the CRC is correct, the USB device replies to the host with a PID ACK handshake packet; If there is an error in the CRC or other error types (bit stuffing, frame error, etc.), the USB device will not reply to the host with an ACK handshake packet, and USB_STS.ERROR is set, at this time, the application does not need to do any processing, the USB device will automatically recover to be ready to receive the next transfer. If the received data size exceeds the data packet buffer size of the receiving endpoint, the USB device will stop receiving data, and the hardware will reply to the STALL handshake packet and set the buffer overflow error, but no interrupt will be generated. After the USB device replies the PID ACK handshake packet to the host, the USB device toggles the USB_EPn.DATTOG_RX bit by the hardware, the hardware sets the endpoint receiving state to NAK state (USB_EPn.STS_RX = 10), and the hardware sets USB_EPn.CTRS_RX to generate a correct receive interrupt. The software responds to the CTRS_RX interrupt, identifies the communication on which endpoint by checking the USB_STS.EP_ID bit, identifies the communication direction through USB_STS.DIR, clears the interrupt flag, processes the data received from the host, and after processing the received data, the software then sets the receiving state of the endpoint to the VALID state (USB_EPn.STS_RX = 11) to enable the next transmission.
- If the endpoint specified in this OUT or SETUP token packet is invalid, the USB device sends a PID NAK or STALL handshake packet according to USB_EPn.STS_RX.

Note: When the USB device receives data from the host, if the size of the received data exceeds the size of the data packet buffer of the receiving endpoint, the hardware will automatically stop writing, that is, the data in the data packet buffer of other endpoints will never be overwritten.

19.4.4.4 Control transfer

Control transfer consists of 3 stages, 1 Setup stage + 0/multiple Data stages in the same direction + 1 Status stage. SETUP transaction can only be completed by the control endpoint, and the process of SETUP transaction and OUT transaction is similar. When a Setup transaction is completed correctly, the hardware generates a USB_EPn.CTRS_RX interrupt. In the interrupt, the software first changes the Tx and Rx direction states of the USB device endpoint to NAK, and then checks the USB_EPn.SETUP bit to determine whether it is a SETUP transaction or an OUT transaction. And according to the corresponding fields in the SETUP token packet, it is judged whether there is a data stage in the future, and if there is a data stage, whether the data stage is IN transmission or OUT transmission. As shown in Figure 19-5, take control write transfer as an example. Before enabling subsequent data stages, determine whether the Data stage is the last Data stage:

- If it is not the last Data stage, that is, it is not the last data packet, before enabling the reception of OUT transactions, set the unused direction Tx status to STALL to prevent the host from prematurely ending the Data stage and entering the Status stage, the USB device can return a PID STALL handshake packet, and the Rx state of the direction to be used is set to VALID. When the first OUT transaction is completed correctly, the hardware generates the USB_EPn.CTRS_RX interrupt, and changes the Rx direction state of the USB device endpoint to NAK, the Tx direction state remains unchanged, the software judges whether the next OUT transaction to be enabled is the last Data stage in the interrupt. If it is not the last Data stage, before enabling the receiving OUT transaction, the software then sets the Rx direction status of the USB device endpoint to VALID, and the Tx

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direction status remains unchanged;

- If it is the last Data stage, before enabling the reception of the last OUT transaction, the software sets the Tx direction status that was not used in the previous Data stage to NAK, so that even if the host starts the Status stage immediately after the last Data stage, the USB device can still remain in the state of waiting for the end of the control transfer, and the Rx direction state is set to VALID, ready to receive the last packet of data;

After the last OUT transaction is completed correctly, the hardware generates the USB_EPn.CTRS_RX interrupt, and sets the Rx direction state of the USB device endpoint to NAK, and the TX direction state remains unchanged. When the software prepares the 0-length data packet that needs to be sent in the Status stage in the interrupt, the software changes the Tx direction status of the USB device endpoint to VALID.

Control read transfers are similar to control write transfers with the following differences:

- To control read transfer, after the last IN transaction in the Data stage is completed correctly, before enabling the Status stage in the OUT direction, in addition to setting the Rx direction status of the USB device endpoint to VALID, you also need to set STATUS_OUT (USB_EPn.EP_KIND) to 1, indicates that the next stage will be the Status stage in the OUT direction, and the subsequent OUT transaction must be a 0-length data packet, otherwise an error will be generated.
- After the Status stage is over, the software clears the STATUS_OUT (USB_EPn.EP_KIND) bit, the Rx direction status of the USB device endpoint is set to VALID, ready to receive a new command request, and the Tx direction status is set to NAK, indicating that before the next SETUP packet transmission is completed, the request for data transfer is not accepted.

Notes:

1、 Bidirectional endpoint 0 is used as the default control endpoint to handle control transfers.

2、 As defined in the USB2.0 specification, after the USB device receives the PID SETUP token packet, it cannot reply with the PID NAK or STALL handshake packet, but only with the PID ACK handshake packet. If the transmission of the SETUP packet fails, the next SETUP packet will be raised. If the Rx state of endpoint 0 is set to STALL or NAK, the USB module can still receive the SETUP token packet.

3、 When USB_EP0.CTRS_RX = 1, the USB module receives the SETUP token packet again, the USB module will discard the SETUP token packet, and will not reply any handshake packet to the host, forcing the host to send the SETUP token packet again.

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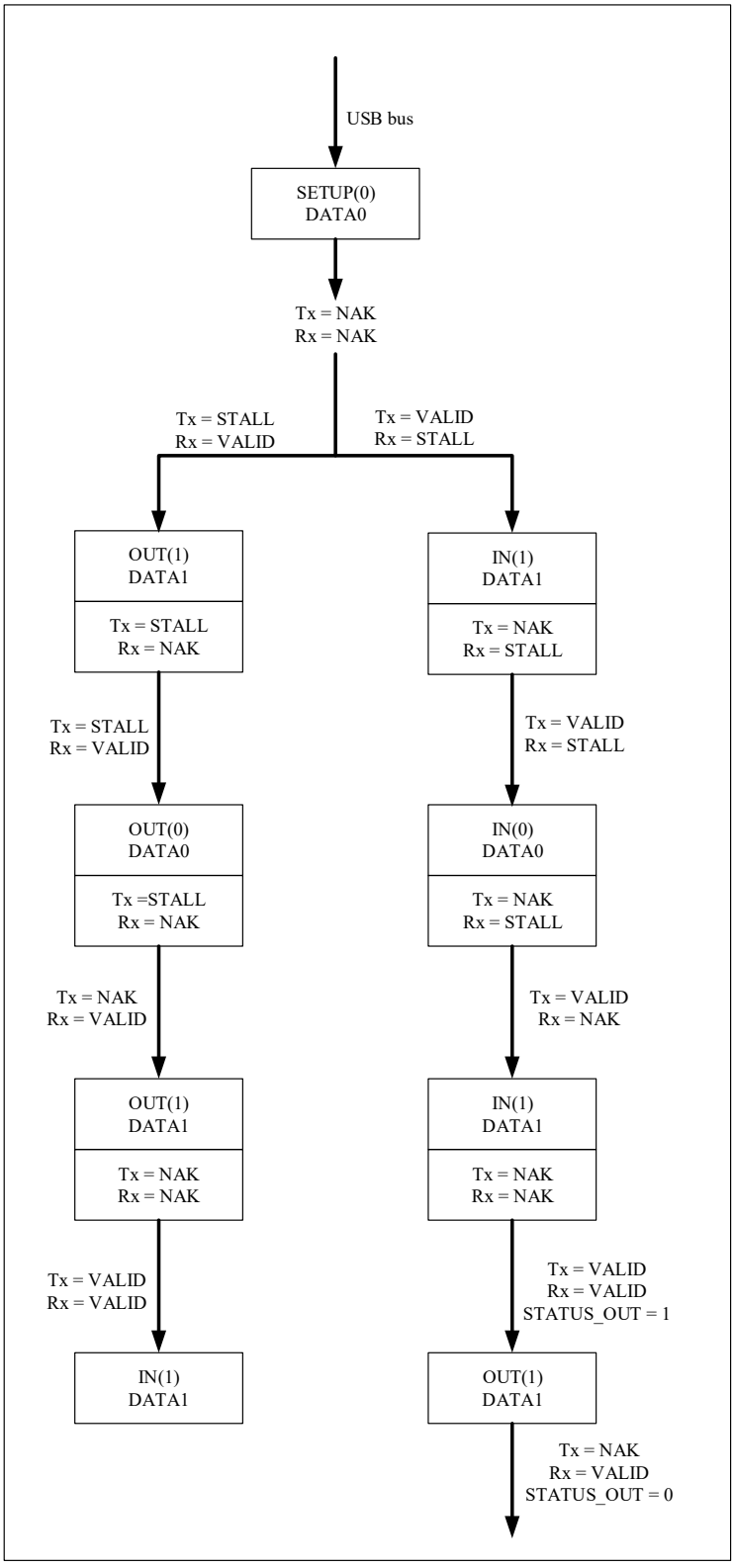
Figure 19-5 Control transfer



19.4.4.5 Isochronous transfer

Transmissions that require a fixed and precise data rate are defined as isochronous transfer. If an endpoint is defined as a isochronous endpoint during enumeration, the USB host will allocate the required bandwidth for the endpoint in each frame of transmission, but in order to save bandwidth, isochronous transfer does not have a retransmission

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mechanism, that is, there is no handshake stage, there is no handshake packet after the data packet, so there is no need to use the data toggle mechanism, and the isochronous transfer only transmits the PID DATA0 data packet.

The isochronous endpoint uses a double buffer mechanism to reduce the processing pressure of the application. The buffer used by the USB module is identified by the DATTOG bit. In the same register, the USB_EPn.DATTOG_RX bit identifies the receiving isochronous endpoint, and the USB_EPn.DATTOG_TX bit identifies the sending isochronous endpoint. Compared with the bulk double buffering mechanism, the isochronous double buffering mechanism has no SW_BUF, because the buffer that the application can access is the one not indicated by DATTOG, so to achieve bidirectional isochronous transmission, two USB_EPn registers need to be used. The use of double-buffered isochronous endpoints is shown in Table 19-3.

Table 19-3 How to use isochronous double buffering

Endpoint type	DATTOG	Buffer used by the USB module	Buffers used by the application
IN Endpoint	0	ADDRn_TX_0/CNTn_TX_0	ADDRn_TX_1/CNTn_TX_1
	1	ADDRn_TX_1/CNTn_TX_1	ADDRn_TX_0/CNTn_TX_0
OUT Endpoint	0	ADDRn_RX_0/CNTn_RX_0	ADDRn_RX_1/CNTn_RX_1
	1	ADDRn_RX_1/CNTn_RX_1	ADDRn_RX_0/CNTn_RX_0

The application initializes the DATTOG bits based on the buffer to be used the first time. Each time the transfer is completed, USB_EPn.CTRS_RX or USB_EPn.CTRS_TX is set according to the direction in which the transmission is enabled, and a corresponding interrupt is generated. If a CRC error or buffer overflow error occurs, the USB_EPn.CTRS_RX or USB_EPn.CTRS_TX interrupt event can still be triggered, but if it is a CRC error, the hardware will set the USB_STS.ERROR bit, indicating that the data may be corrupted. At the same time, the hardware toggles the DATTOG bit, but the USB_EPn.STS_RX or USB_EPn.STS_TX bits are not affected.

Isochronous endpoint definition: set USB_EPn.EP_TYPE = 10. Since the isochronous endpoint has no handshake mechanism, the status of the isochronous endpoint can only be set to VALID or DISABLED, and it is illegal to set it to STALL or NAK.

Note: Compared with bulk double buffering, since isochronous *double buffering has no handshake mechanism,* isochronous *double buffering has no flow control mechanism.*

19.4.5 USB events and interrupts

Every USB behavior is initiated by the application and driven by USB interrupts or events. After a system reset, the application needs to wait for a series of USB interrupts and events.

19.4.5.1 Reset events

19.4.5.1.1 System reset and power-on reset

After a system reset or power-on reset occurs, the software first needs to enable the clock signal of the USB module, then clear the reset signal to access the registers of the USB module, and finally open the analog part connected to the USB transceiver. The software operation process is as follows:

- Enable the clock signal of the USB module
- Clear the USB_CTRL.PD bit
- Wait for the internal reference voltage to stabilize, because it takes a start-up time to turn on the internal voltage, during which the USB transceiver is in an indeterminate state

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- Clear the USB_CTRL.FRST bit
- Clear the USB_STS register, remove pending interrupts, and enable other units

Note: Every time the USB module is enabled after system reset or power-on reset, the pull-up resistor on the DP signal line needs to be configured. This control bit is located in bit28 of the base address 0x4000 1820 register. Set bit28 to 1 to enable the pull-up resistor on the DP signal line, otherwise disable the pull-up resistor. Modification of other bits of this register is not allowed.

19.4.5.1.2 USB reset (reset interrupt)

When a USB reset occurs, the state of the USB module is the same as after a system reset: all endpoints are disabled for communication. The software needs to do the following:

- After the reset interrupt is generated, the software must enable the transmission of endpoint 0 within 10ms
- Set the USB_ADDR.EFUC bit
- Initialize the USB_EP0 register and its associated endpoint packet buffer

19.4.5.2 Suspend and resume events

19.4.5.2.1 Suspend events

When full-speed USB is communicating normally, the host will send a PID SOF token packet every millisecond. If the USB module detects that 3 consecutive SOF packets are lost, that is, the USB bus is in an idle state within 3ms, the hardware sets the USB_STS.SUSPD bit, triggers a suspend interrupt, and the USB device enters the suspend state. The USB2.0 standard stipulates that in the suspend state, the average current consumption on the USB bus does not exceed 2.5mA, but self-powered devices do not need to strictly abide by this regulation.

Note: After the USB device enters the suspend state, it must still have the function of detecting the RESET signal.

19.4.5.2.2 Resume events

After the USB device enters the suspend state, to resume normal USB communication, the USB host can initiate a resume sequence or a reset sequence, or the USB device itself can trigger the resume sequence, but the resume sequence can only be ended by the USB host. If the reset sequence initiated by the USB host resumes the USB device, according to the regulations in the USB2.0 standard, it must be ensured that the resume process does not exceed 10ms.

Table 19-4 lists the USB_FN.RXDP_STS bit and the USB_FN.RXDM_STS bit to identify what triggers the resume event and the corresponding software action.

Table 19-4 Resume event detection

[USB_FN.RXDP_STS, USB_FN.RXDM_STS]	Wake-up event	Software operation
00	Root reset	None
01	Root resume	None
10	None (noise on bus)	Go back in Suspend mode
11	Not allowed (noise on bus)	Go back in Suspend mode

Note: The USB_CTRL.RESUM bit can only be set when USB_CTRL.FSUSPD = 1, i.e. the USB module is in suspend state.

19.4.5.3 USB interrupt

The USB controller has 3 interrupt lines, which are as follows:

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- USB low priority interrupt (channel 20): can be triggered by all USB events;
- USB high-priority interrupt (channel 19): can only be triggered by correct transfer events for isochronous and double-buffered bulk transfers;
- USB resume interrupt (channel 42): triggered by a resume event from USB suspend mode.

19.4.6 Endpoint initialization

1. Initialize the USB_ADDRn_TX or USB_ADDRn_RX register, configure the endpoint Tx or Rx packet buffer start address;
2. According to the actual usage scenario of the endpoint, configure the USB_EPn.EP_TYPE bit and the USB_EPn.EP_KIND bit to set the endpoint type and buffer type;
3. Perform different operations based on the endpoint direction:
   - If it is a sending endpoint
   1) Set the USB_EPn.STS_TX bit to enable the sending function of the endpoint
   2) Configure the USB_CNTn_TX.CNTn_TX bit, set the endpoint data packet send buffer size
   - If it is a receiving endpoint
   1) Set the USB_EPn.STS_RX bit to enable the receiving function of the endpoint
   2) Configure the USB_CNTn_RX.BL_SIZE bit and the USB_CNTn_RX.NUM_BLK bit to set the endpoint packet receive buffer size

19.5 USB registers

The peripheral registers can be accessed by half-words (16-bit) or words (32-bit).

USB base address: 0x4000 5C00

19.5.1 USB register overview

Table 19-5 USB register overview

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
000h	USB_EP0	Reserved																CTRS_RX	DATTOG_RX	STS_RX[1:0]		SETUP	EP_TYPE[1:0]		EP_KIND	CTRS_TX	DATTOG_TX	STS_TX[1:0]		EPADDR[3:0]			
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
004h	USB_EP1	Reserved																CTRS_RX	DATTOG_RX	STS_RX[1:0]		SETUP	EP_TYPE[1:0]		EP_KIND	CTRS_TX	DATTOG_TX	STS_TX[1:0]		EPADDR[3:0]			
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
008h	USB_EP2	Reserved																CTRS_RX	DATTOG_RX	STS_RX[1:0]		SETUP	EP_TYPE[1:0]		EP_KIND	CTRS_TX	DATTOG_TX	STS_TX[1:0]		EPADDR[3:0]			
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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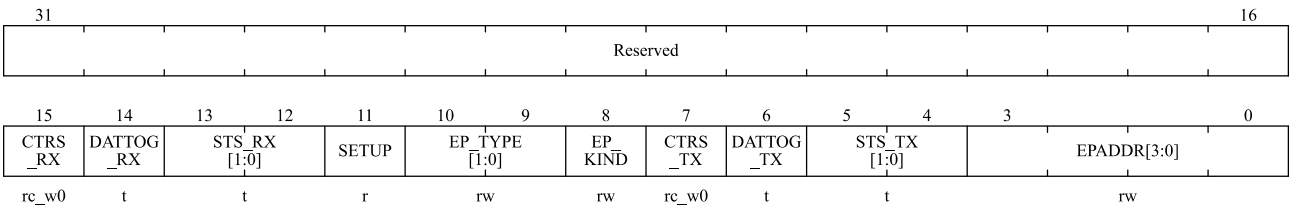
Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
00Ch	USB_EP3	Reserved																CTRS_RX	DATTOG_RX	STS_RX[1:0]		SETUP	EP_TYPE[1:0]		EP_KIND	CTRS_TX	DATTOG_TX	STS_TX[1:0]		EPADDR[3:0]			
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
010h	USB_EP4	Reserved																CTRS_RX	DATTOG_RX	STS_RX[1:0]		SETUP	EP_TYPE[1:0]		EP_KIND	CTRS_TX	DATTOG_TX	STS_TX[1:0]		EPADDR[3:0]			
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
014h	USB_EP5	Reserved																CTRS_RX	DATTOG_RX	STS_RX[1:0]		SETUP	EP_TYPE[1:0]		EP_KIND	CTRS_TX	DATTOG_TX	STS_TX[1:0]		EPADDR[3:0]			
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
018h	USB_EP6	Reserved																CTRS_RX	DATTOG_RX	STS_RX[1:0]		SETUP	EP_TYPE[1:0]		EP_KIND	CTRS_TX	DATTOG_TX	STS_TX[1:0]		EPADDR[3:0]			
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
01Ch	USB_EP7	Reserved																CTRS_RX	DATTOG_RX	STS_RX[1:0]		SETUP	EP_TYPE[1:0]		EP_KIND	CTRS_TX	DATTOG_TX	STS_TX[1:0]		EPADDR[3:0]			
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
040h	USB_CTRL	Reserved																CTRSM	PMAOM	ERRORM	WKUPM	SUSPDM	RSTM	SOFM	ESOFM	Reserved				RESUM	FSUSPD	LP_MODE	PD	FRST
	Reset Value																	0	0	0	0	0	0	0	0					0	0	0	1	1
044h	USB_STS	Reserved																CTRS	PMAO	ERROR	WKUP	SUSPD	RST	SOF	ESOF	Reserved				DIR	EP_ID[3:0]			
	Reset Value																	0	0	0	0	0	0	0	0					0	0	0	0	0
048h	USB_FN	Reserved																RXDP_STS	RXDM_STS	LOCK	LSTSOF [1:0]		FN[10:0]											
	Reset Value																	0	0	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X
04Ch	USB_ADDR	Reserved																Reserved									ADDR[6:0]							
	Reset Value																										0	0	0	0	0	0	0	0
050h	USB_BUFTAB	Reserved																BUFTAB[15:3]															Reserved	
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0				

19.5.2 USB endpoint n register (USB_EPn), n=[0..7]

Address offset: 0x00 to 0X1C

Reset value: 0x0000 0000



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Bit Field	Name	Description
31：16	Reserved	Reserved, the reset value must be maintained.
15	CTRS_RX	Correct receive flag This bit is set by hardware when an OUT or SETUP transaction on this endpoint completes successfully. If USB_CTRL.CTRSM = 1, the corresponding interrupt will be generated. *Note:* *1、 Software can read and write this bit, but only writing 0 is valid, and writing 1 is invalid.*
14	DATTOG_RX	Receive data PID toggle bit If the endpoint is not isochronous, this bit represents the toggle data bit (0 = DATA0, 1 = DATA1). Double-buffered endpoint, this bit is used to implement the flow control mechanism for double-buffered endpoints. Isochronous endpoint, this bit is used for double buffer exchange. *Note:* *1、 Software can read and write this bit, but writing 0 is invalid, and writing 1 toggles this bit.* *2、 Control endpoint, the hardware clears this bit after the USB module correctly receives the PID SETUP token packet.* *3、 In isochronous transfer, hardware toggles this bit just after the end of data packet reception.*
13：12	STS_RX[1:0]	Receive status This bit indicates the current state of the endpoint, Table 19-6 lists the available states of the endpoint. Hardware sets this bit to the NAK state when a correct OUT or SETUP transaction completes. *Note:* *1、 Software can read and write this bit, but writing 0 is invalid, and writing 1 toggles this bit.* *2、 Double-buffered bulk endpoint, which controls the transmission status according to the buffer status used, refer to section 19.4.3.* *3、 Isochronous endpoint, the hardware will not change the state of the endpoint after the transaction is successfully completed*
11	SETUP	SETUP transfer completion flag This bit is set by hardware when the USB module correctly receives the PID SETUP token packet. *Note:* *1、 Software can only read this bit, not write this bit.* *2、 This bit USB_EPn.SETUP is only valid for control endpoints.*
10：9	EP_TYPE[1:0]	Endpoint type

EP_TYPE[1:0]	Description
00	BULK: bulk endpoint
01	CONTROL: control endpoint
10	ISO: isochronous endpoint

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<table>
<tr><th>Bit Field</th><th>Name</th><th>Description</th></tr>
<tr><td></td><td></td><td><table><tr><td colspan="2">11</td><td>INTERRUPT: interrupt endpoint</td></tr></table></td></tr>
<tr><td>8</td><td>EP_KIND</td><td>Endpoint special type<table><tr><td colspan="2">EP_TYPE[1:0]</td><td>EP_KIND meaning</td></tr><tr><td>00</td><td>BULK</td><td>DBL_BUF: double buffered endpoint</td></tr><tr><td>01</td><td>CONTROL</td><td>STATUS_OUT</td></tr><tr><td>10</td><td>ISO</td><td>Undefined</td></tr><tr><td>11</td><td>INTERRUPT</td><td>Undefined</td></tr></table></td></tr>
<tr><td>7</td><td>CTRS_TX</td><td>Correct send flag
This bit is set by hardware when an IN transaction on this endpoint completes successfully. If USB_CTRL.CTRSM = 1, the corresponding interrupt will be generated.
Note:
1、 Software can read and write this bit, but only writing 0 is valid, and writing 1 is invalid.</td></tr>
<tr><td>6</td><td>DATTOG_TX</td><td>Send data PID toggle bit
If the endpoint is not isochronous, this bit represents the toggle data bit (0 = DATA0, 1 = DATA1).
Double-buffered endpoint, this bit is used to implement the flow control mechanism for double-buffered endpoints.
Isochronous endpoint, this bit is used for double buffer exchange.
Note:
1、 Software can read and write this bit, but writing 0 is invalid, and writing 1 toggles this bit.
2、 Control endpoint, the hardware will set this bit after the USB module correctly receives the PID SETUP token packet.
3、 In isochronous transfer, hardware toggles this bit just after the end of data packet transmission.</td></tr>
<tr><td>5：4</td><td>STS_TX[1:0]</td><td>Send status
This bit indicates the current state of the endpoint, Table 19-7 lists the available states of the endpoint. When a correct IN transaction completes, the hardware sets this bit to the NAK state.
Note:
1、 Software can read and write this bit, but writing 0 is invalid, and writing 1 toggles this bit.
2、 Double-buffered bulk endpoint, which controls the transmission status according to the buffer status used, refer to section 19.4.3.
3、 Isochronous endpoint, the hardware will not change the state of the endpoint after the transaction is successfully completed.</td></tr>
<tr><td>3：0</td><td>EPADDR[3:0]</td><td>Endpoint address
This bit indicates the destination endpoint of the communication and must be written before enabling the corresponding endpoint.</td></tr>
</table>

Note:

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1、When the USB module receives the USB bus reset signal, or USB_CTRL.FRST = 1, the USB module will be reset. Except for the CTRS_RX and CTRS_TX bits that remain unchanged to process the following USB transfer, all other bits are reset.

Table 19-6 Receive status code

STS_RX[1:0]	Description
00	DISABLED: ignore all receive requests for this endpoint
01	STALL: the status of the handshake packet is STALL
10	NAK: the status of the handshake packet is NAK
11	VALID: endpoints can be used to receive

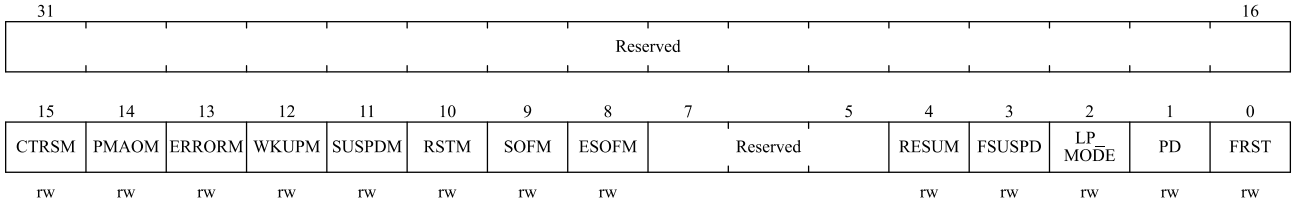
Table 19-7 Send status code

STS_TX[1:0]	Description
00	DISABLED: ignore all send requests for this endpoint
01	STALL: the status of the handshake packet is STALL
10	NAK: the status of the handshake packet is NAK
11	VALID: endpoints can be used to send

19.5.3 USB control register (USB_CTRL)

Address offset: 0x40

Reset value: 0x0000 0003



Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained.
15	CTRSM	Correct transfer interrupt enable 0: Disable correct transfer interrupt 1: Enable correct transfer interrupt, when USB_STS.CTRS = 1, an interrupt is generated.
14	PMAOM	Packet buffer overflow/underflow interrupt enable 0: Disable packet buffer overflow/underflow interrupt 1: Enable packet buffer overflow/underflow interrupt, when USB_STS.PMAO = 1, an interrupt is generated.
13	ERRORM	Error interrupt enable 0: Disable error interrupt 1: Enable error interrupt, when USB_STS.ERROR = 1, an interrupt will be generated.
12	WKUPM	Wake-up interrupt enable 0: Disable wake-up interrupt

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Bit Field	Name	Description
		1: Enable wake-up interrupt, when USB_STS.WKUP = 1, an interrupt will be generated.
11	SUSPDM	Suspend mode interrupt enable 0: Disable suspend mode interrupt 1: Enable suspend mode interrupt, when USB_STS.SUSPD = 1, an interrupt will be generated.
10	RSTM	USB reset interrupt enable 0: Disable USB reset interrupt 1: Enable USB reset interrupt, when USB_STS.RST = 1, an interrupt will be generated.
9	SOFM	Start of frame interrupt enable 0: Disable start of frame interrupt 1: Enable start of frame interrupt, when USB_STS.SOF = 1, an interrupt will be generated.
8	ESOFM	Expected start of frame interrupt enable 0: Disable the expected start of frame interrupt 1: Enable the expected start of frame interrupt, when USB_STS.ESOF = 1, generate an interrupt.
7：5	Reserved	Reserved, the reset value must be maintained.
4	RESUM	Resume request 0: No resume request 1: Send a resume request to the PC host *Note:* *1、 If USB_CTRL.RESUM = 1 remains active for 1ms to 15ms, the PC host will implement a resume operation for the USB module.*
3	FSUSPD	Force suspend Software must set this bit when the USB_STS.SUSPD interrupt is triggered. 0: Suspend mode not entered 1: Enter suspend mode, but the clock and static power consumption of the USB analog transceiver are still present *Note:* *1、 To enter the low power consumption mode (bus powered device), the software must first set USB_CTRL.FSUSPD, and then set USB_CTRL.LP_MODE.*
2	LP_MODE	Low power mode 0: No effect 1: Enter low power mode in suspend mode. Activity on the USB bus (wake event) resets this bit (software can also reset this bit) *Note:* *1、 In low power mode, only the external pull-up resistor is used for power supply, and the system clock will also be stopped or reduced to a certain frequency to reduce power consumption.*
1	PD	Power-down mode 0: Exit power-down mode

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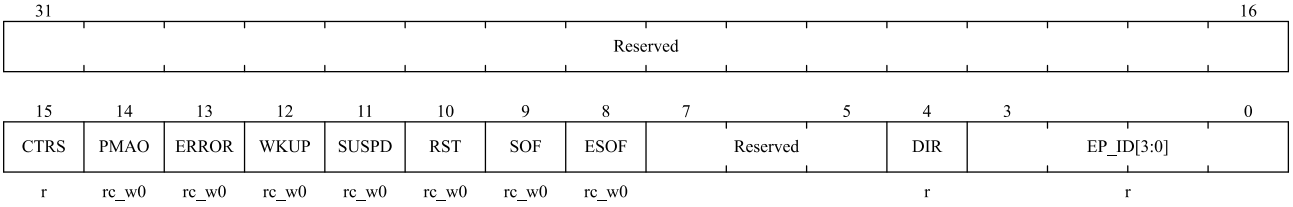
Bit Field	Name	Description
		1: Enter power-down mode *Note:* *1、 When USB_CTRL.PD = 1, the USB module is completely shut down, disconnected from the host, and the USB module will not work.*
0	FRST	Force USB reset 0: No effect 1: Reset the USB module, if USB_CTRL.RSTM = 1, a reset interrupt will be generated *Note:* *1、 When USB_CTRL.FRST = 1, the USB module will remain in reset state until software clears this bit.*

19.5.4 USB interrupt status register (USB_STS)

Address offset: 0x44

Reset value: 0x0000 0000



Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained.
15	CTRS	Correct transmission interrupt flag Set by hardware when the endpoint has completed a data transfer correctly. *Note:* *1、 Software can only read this bit, not write this bit.*
14	PMAO	Packet buffer overflow/underflow interrupt flag This bit is set by hardware when the packet buffer cannot hold all the transmitted data. *Note:* *1、 Software can read and write this bit, but only writing 0 is valid, and writing 1 is invalid.* *2、 This interrupt will not be generated during isochronous transfer.*
13	ERROR	Error interrupt flag Hardware sets this bit when the following errors occur: 1) No response, the host response timed out 2) CRC error, CRC check error in data or token packet 3) Bit stuffing error, bit stuffing error detected in PID, data or CRC 4) Frame format error, non-standard frame received *Note:*

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Bit Field	Name	Description
		1、 Software can read and write this bit, but only writing 0 is valid, writing 1 is invalid.
12	WKUP	Wake-up interrupt flag In the suspend state, when the wake-up signal is detected, the hardware sets this bit, and the hardware resets the USB_CTRL.LP_MODE bit at the same time. *Note:* 1、 *Software can read and write this bit, but only writing 0 is valid, writing 1 is invalid.*
11	SUSPD	Suspend mode interrupt flag This bit is set by hardware when there is no activity on the USB bus for more than 3ms, indicating a suspend request. *Note:* *1、 Software can read and write this bit, but only writing 0 is valid, and writing 1 is invalid.* *2、 In suspend mode, the USB hardware will not detect the suspend signal until the wake-up is over.* *3、 After the USB is reset, the hardware will immediately enable the detection of the suspend signal.*
10	RST	USB reset interrupt flag This bit is set by hardware when a USB reset signal is detected. *Note:* *1、 Software can read and write this bit, but only writing 0 is valid, and writing 1 is invalid.* *2、 When the USB reset interrupt is generated, the address and endpoint registers of the device will be reset, but the configuration registers will not be reset unless cleared by software.*
9	SOF	Start of frame interrupt flag This bit is set by hardware when a PID SOF token packet is detected on the USB bus. *Note:* *1、 Software can read and write this bit, but only writing 0 is valid, and writing 1 is invalid.*
8	ESOF	Expected start of frame interrupt flag This bit is set by hardware when the USB module does not receive the expected PID SOF token packet. *Note:* *1、 Software can read and write this bit, but only writing 0 is valid, and writing 1 is invalid.* *2、 When the USB module does not receive the PID SOF token packet for 3ms in a row, that is, 3 ESOF interrupts occur in a row, and a SUSPD interrupt will be generated.*
7：5	Reserved	Reserved, the reset value must be maintained.
4	DIR	Transmission direction 0: IN packet transfer is completed, and USB_EPn.CTRS_TX is set by hardware

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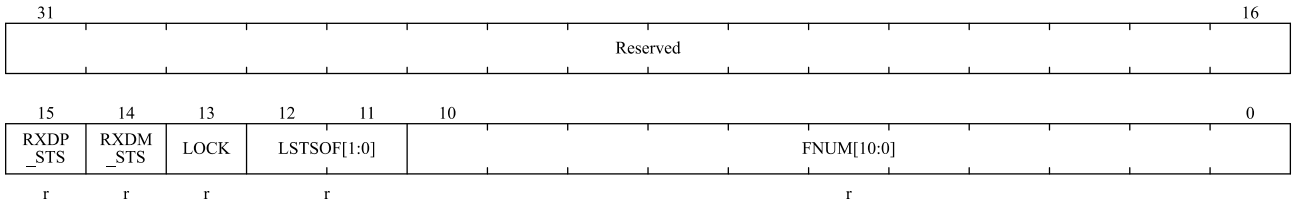
Bit Field	Name	Description
		1: OUT packet transfer is complete, and USB_EPn.CTRS_RX is set by hardware *Note:* *1、 Software can only read this bit, not write this bit.* *2、 When USB_EPn.CTRS_TX and USB_EPn.CTRS_RX are set at the same time, it indicates that there are OUT group and IN group at the same time.*
3：0	EP_ID[3:0]	Endpoint number After the USB module completes the data transmission and generates an interrupt, it is written by the hardware according to the endpoint number of the interrupt request. *Note:* *1、 Software can only read this bit, not write this bit.* *2、 When multiple endpoint requests are interrupted at the same time, the hardware writes the endpoint number with the highest priority. Isochronous endpoints and double-buffered bulk endpoints have high priority, other endpoints have low priority (the lower the endpoint number, the higher the priority).*

19.5.5 USB frame number register (USB_FN)

Address offset: 0x48

Reset value: 0x0000 0XXX, X stands for undefined value



Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained.
15	RXDP_STS	D+ status Represents the state of the USB D+ line, and can detect the occurrence of a resume condition in the suspend state.
14	RXDM_STS	D- status Represents the state of the USB D- line, and can detect the occurrence of a resume condition in the suspend state.
13	LOCK	Lock USB This bit is set by hardware if at least 2 PID SOF token packets are detected continuously after the end of an USB reset condition or after the end of an USB resume sequence. *Note:* *1、 When USB_FN.LOCK = 1, the frame counter will stop counting before the USB module is reset or the USB bus is suspended.*
12:11	LSTSOF[1:0]	Lost SOF flag The hardware increments this bit every time the USB_STS.ESOF event occurs, and

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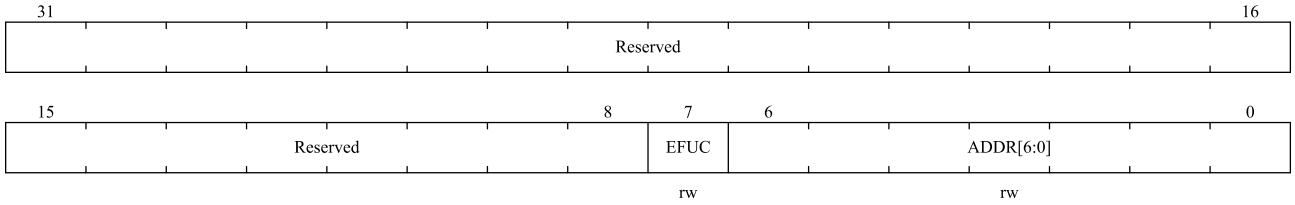
Bit Field	Name	Description
		once the PID SOF token packet is received, the hardware clears this bit.
10:0	FNUM[10:0]	Number of frames Hardware increments this bit every time the USB module receives a PID SOF token packet.

19.5.6 USB device address register (USB_ADDR)

Address offset: 0x4C

Reset value: 0x0000 0000

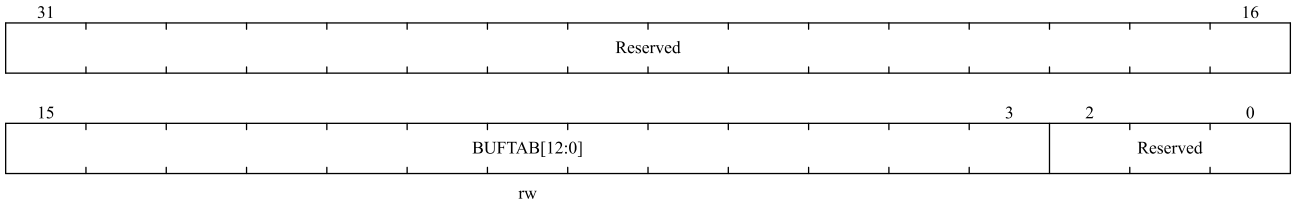


Bit Field	Name	Description
31:8	Reserved	Reserved, the reset value must be maintained.
7	EFUC	USB module enable 0: The USB module stops working and does not respond to any USB communication 1: Enable USB module
6：0	ADDR[6:0]	USB device address This bit holds the address value assigned to the USB device by the USB host during enumeration. After a USB bus reset, this bit is reset to 0x00.

19.5.7 USB packet buffer description table address register (USB_BUFTAB)

Address offset: 0x50

Reset value: 0x0000 0000



Bit Field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained.
15:3	BUFTAB[12:0]	Buffer table This bit holds the starting address of the buffer description table. The buffer description table is used to indicate the address and size of the endpoint packet buffer of each endpoint, aligned by 8 bytes (the lowest 3 bits are 000).
2:0	Reserved	Reserved, the reset value must be maintained.

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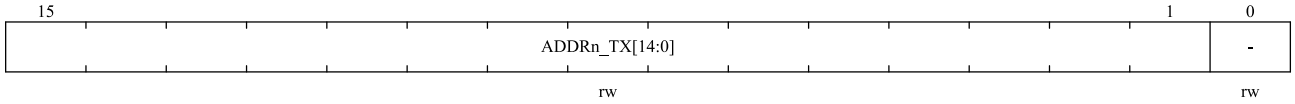
19.6 Buffer description table

The buffer description table is located in the packet buffer memory and is used to configure the address and size of the endpoint packet buffer shared by the USB module and the microcontroller core. Since the APB1 bus is addressed by 32 bits, the data packet buffer memory addresses use 32-bit aligned addresses, not the addresses used by the USB_BUFTAB register and the buffer description table.

19.6.1 Send buffer address register n (USB_ADDRn_TX)

Address offset: [USB_BUFTAB] + n×16

USB local address: [USB_ BUFTAB] + n×8

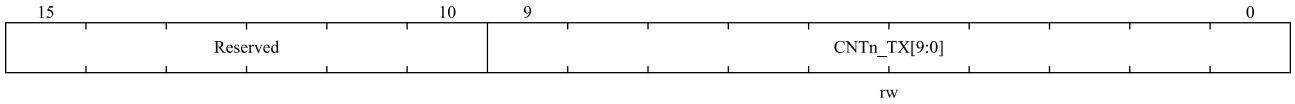


Bit Field	Name	Description
15：1	ADDRn_TX[14:0]	Send buffer address The starting address of the endpoint packet buffer of the endpoint that needs to send data when the next PID IN token packet is received
0	-	Since packet buffer memory addresses are word (32-bit) aligned, this bit must be 0

19.6.2 Send data byte number register n (USB_CNTn_TX)

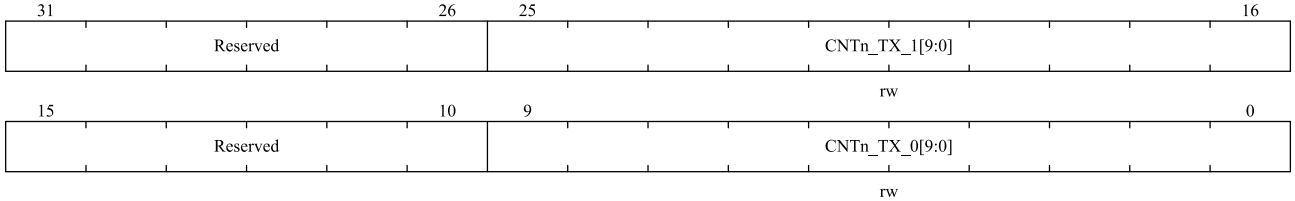
Address offset: [USB_ BUFTAB] + n×16 + 4

USB local address: [USB_ BUFTAB] + n×8 + 2



Bit Field	Name	Description
15:10	Reserved	Reserved, the reset value must be maintained.
9：0	CNTn_TX[9:0]	Number of bytes sent The number of data bytes to send on the next PID IN token packet

Note: As shown in Table 19-2 and Table 19-3, the double-buffered IN endpoint and the isochronous IN endpoint require two USB_CNTn_TX registers: USB_CNTn_TX_0 and USB_CNTn_TX_1.



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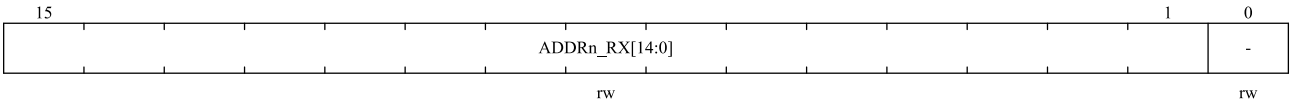
19.6.3 Receive buffer address register n (USB_ADDRn_RX)

Address offset: [USB_ BUFTAB] + n×16 + 8

USB local address: [USB_ BUFTAB] + n×8 + 4



Bit Field	Name	Description
15:1	ADDRn_RX[14:0]	Receive buffer address Endpoint packet buffer start address for the endpoint to hold data when the next PID SETUP or OUT token packet is received
0	-	Since packet buffer memory addresses are word (32-bit) aligned, this bit must be 0

19.6.4 Receive data byte number register n (USB_CNTn_RX)

Address offset: [USB_ BUFTAB] + n×16 + 12

USB local address: [USB_ BUFTAB] + n×8 + 6

Bit Field	Name	Description
15	BLSIZE	Memory block size 0: The memory block size is 2 bytes 1: The memory block size is 32 bytes
14:10	NUM_BLK[4:0]	Number of memory blocks Records the number of memory blocks allocated to the endpoint packet receive buffer and determines the size of the endpoint packet receive buffer that is ultimately used. For details, please refer to the following Table 19-8.
9:0	CNTn_RX[9:0]	Number of bytes received Written by the USB module to record the actual number of bytes of the latest PID SETUP or OUT token packet received by the endpoint.

Note: As shown in Table 19-2 and Table 19-3 double buffered OUT endpoints and isochronous OUT endpoints require two USB_CNTn_RX registers: USB_CNTn_RX_0 and USB_CNTn_RX_1.

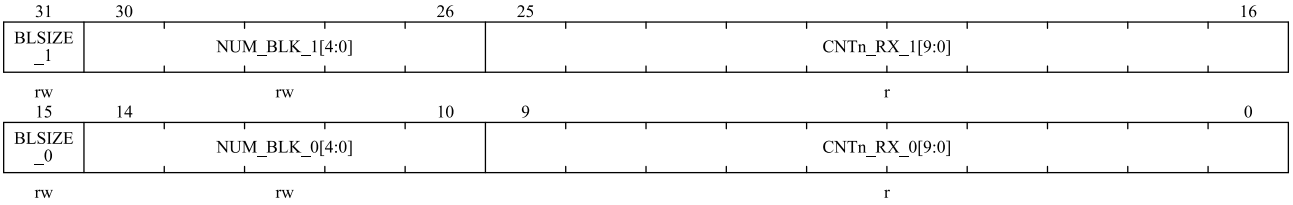


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Table 19-8 Endpoint packet receive buffer size definition

NUM_BLK[4:0]	BLSIZE = 0	BLSIZE = 1
00000	Not allowed	32 bytes
00001	2 bytes	64 bytes
00010	4 bytes	96 bytes
00011	6 bytes	128 bytes
…	…	…
01111	30 bytes	512 bytes
10000	32 bytes	Reserved
10001	34 bytes	Reserved
10010	36 bytes	Reserved
…	…	…
11110	60 bytes	Reserved
11111	62 bytes	Reserved

Note: The size of the endpoint packet receive buffer is defined during the device enumeration process and is defined by the wMaxPacketSize field of the standard endpoint descriptor in the USB 2.0 protocol specification.

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20 Controller Area Network (CAN)

20.1 Introduction to CAN

As CAN network interface, basic extended CAN supports CAN protocols 2.0A and 2.0B. It can efficiently process a large number of received messages and greatly reduce the consumption of CPU resources. The priority characteristics of message sending can be configured by software, and the hardware function of CAN can support time-triggered communication mode for some applications with high security requirements.

20.2 Main Features of CAN

- Baud rate supports up to 1Mbit/s
- CAN protocol 2.0A/B are supported.
- Support time-triggered communication function
- Support individual interrupt control.
- CAN Core Manages the communication between the CAN and the 512 bytes SRAM memory (see Figure 20-3)
- Dual CAN: CAN1 and CAN2 each with 512 bytes of SRAM

Note: USB and CAN1 share a single 512-byte SRAM. Since this SRAM is used to transmit and receive data, USB and CAN1 cannot be used at the same time. USB and CAN1 can be time-shared using in an application, but not simultaneously.

Time triggered communication mode

- 16-bit free-running timer
- Automatic retransmission mode is prohibited.
- The last 2 data bytes of a message can be configured as the timestamp.

Send

- There are 3 sending mailboxes.
- Time stamp function for recording the time of sending SOF
- Software can configure the priority characteristics of sending messages.

Receive

- Filter groups support identifier list mode.
- Each CAN has two receiving FIFOs, each with a depth of 3 levels
- A total of 14 filter groups(each CAN module has its own)
- Configurable FIFO overrun handling method
- Time stamp function for recording the time of receiving SOF

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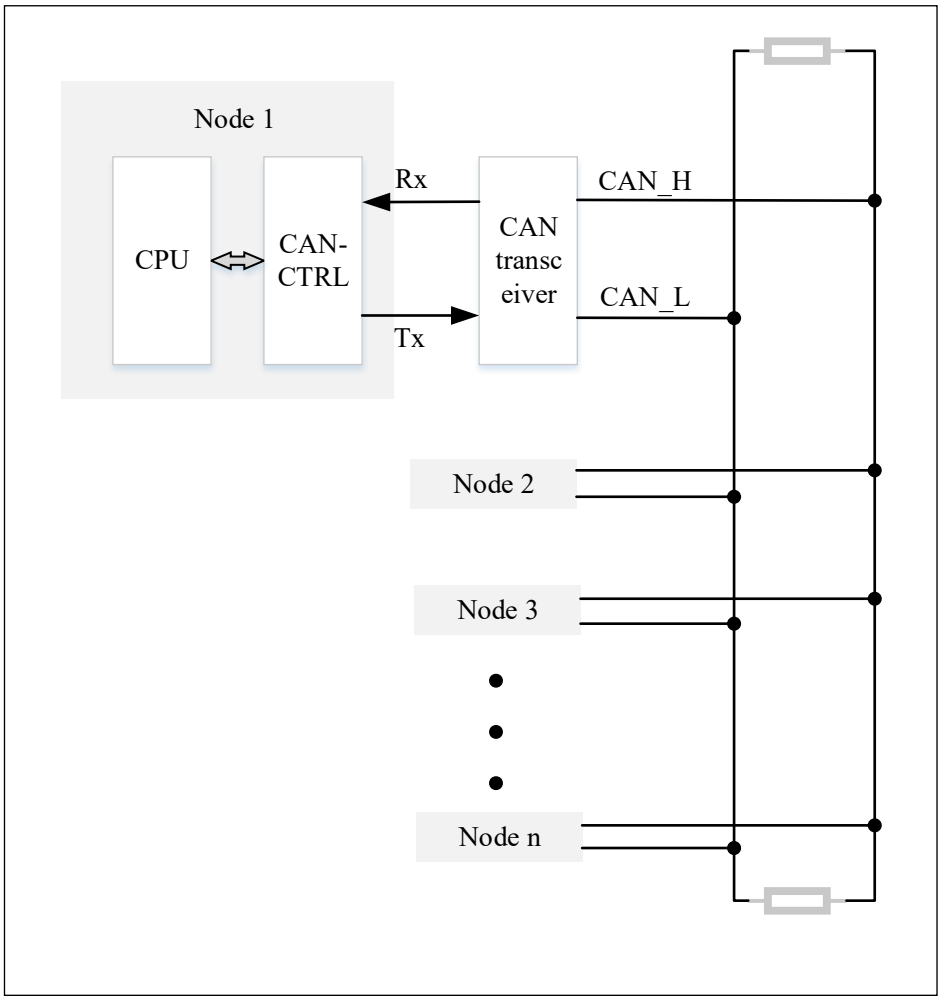
20.3 CAN overall introduction

With the wide application of CAN, the nodes of CAN network are growing rapidly. Multiple CAN nodes are connected through CAN network. With increase number of CAN nodes, messages in CAN network also increase dramatically which will occupides lots of CPU resource. In this CAN controller, receive FIFOs and filter mechanism are added as hardware support for CPU message processing and reduce real-time response requirement of CAN message.

Figure 20-1 Topology of CAN network



20.3.1 CAN module

CAN module can automatically receive and send CAN messages, and supports standard identifiers (11 bits) and extended identifiers (29 bits).

20.3.2 CAN working mode

Initialization, normal and sleep mode are three main working modes of CAN. The internal pull-up resistor of CANTX pin is activated after hardware reset, and CAN works in sleep mode to reduce power consumption.

The software can set CAN_MCTRL.INIRQ and CAN_MCTRL.SLPRQ bit to configure CAN to enter **initialization**

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or **sleep** mode. The software reads values of the CAN_MSTS.INIAK or CAN_MSTS.SLPAK bit to confirm whether the **initialization** or **sleep** mode is entered, at this time the internal pull-up resistor of the CANTX pin is disabled.

CAN is in **normal** mode when CAN_MSTS.INIAK and CAN_MSTS.SLPAK bits are both '0', and it must **synchronize** with CAN bus to enter **normal** mode. When 11 consecutive recessive bits are monitored on the CANRX pin, the CAN bus is idle and synchronization is completed.

20.3.2.1 Normal mode

After the initialization is completed, the software configures CAN to enter normal mode. Clear the CAN_MCTRL.INIRQ and wait for the hardware to clear the CAN_MSTS.INIRQ bit to confirm that CAN enters normal mode. Only after the synchronization with CAN bus is completed, CAN can receive and send messages normally.

Setting the bit width and mode of the filter group must be completed when the filter is in the initialization mode (the CAN_FMC.FINITM bit is 1). Setting the initial value of the filter must be completed when it is inactive (the corresponding CAN_FA1.FAC bit is 0).

20.3.2.2 Initialization mode

The software can perform initialization configuration only when CAN is in initialization mode. Set the CAN_MCTRL.INIRQ bit and clear CAN_MCTRL.SLPRQ bit, and wait for the hardware to set the CAN_MSTS.INIAK bit to confirm that CAN enters the initialization mode. When entering the initialization mode, the register configuration will not be affected. When CAN is in initialization mode, message receiving and sending are prohibited, and the CANTX pin outputs a recessive bit (high level). To exit initialization mode, clear the CAN_MCTRL.INIRQ bit, and wait for the hardware to clear the CAN_MSTS.INIAK bit to confirm that CAN exits the initialization mode.

To perform initialization configuration for CAN by software, at least the bit time characteristic register (CAN_BTIM) and the control register (CAN_MCTRL) need to be configured. The software needs to set the CAN_FMC.FINITM bit to initialize the filter group (mode, bit width, FIFO association, activation and filter value) that configures CAN. Configuring the filter group of CAN does not necessarily need to be in initialization mode.

Specially,when CAN_FMC.FINITM=1, it is forbidden to receive messages. If you want to modify the value of the corresponding filter, you need to first clear the filter activation bit (in CAN_FA1). It is necessary to keep the unused filter group inactive (keep its CAN_FA1.FAC bit to '0').

20.3.2.3 Sleep mode (low power)

To enters sleep mode, set the CAN_MCTRL.SLPRQ bit, and wait for the hardware to set the CAN_MSTS.SLPAK bit to confirm that CAN enters sleep mode. CAN can configure to sleep modeto reduce power consumption when unused. In sleep mode, the clock of CAN stops working, but the software can still access the sending/receiving mailbox register. When CAN is in sleep mode, the CAN_MCTRL.INIRQ bit must be set and the CAN_MCTRL.SLPRQ bit must be clear at the same time so as to enter the initialization mode.

There are two situation to wake up CAN(CAN exits sleep mode):

- When the CAN_MCTRL.AWKUM bit is set(enable hardware wake up automatically), once the activity of the CAN bus is detected, the hardware will automatically clear the CAN_MSTS.SLPRQ bit to wake up CAN.
- When the CAN_MCTRL.AWKUM bit is clear(enable software wake up), and wake-up interrupt occurred ,then

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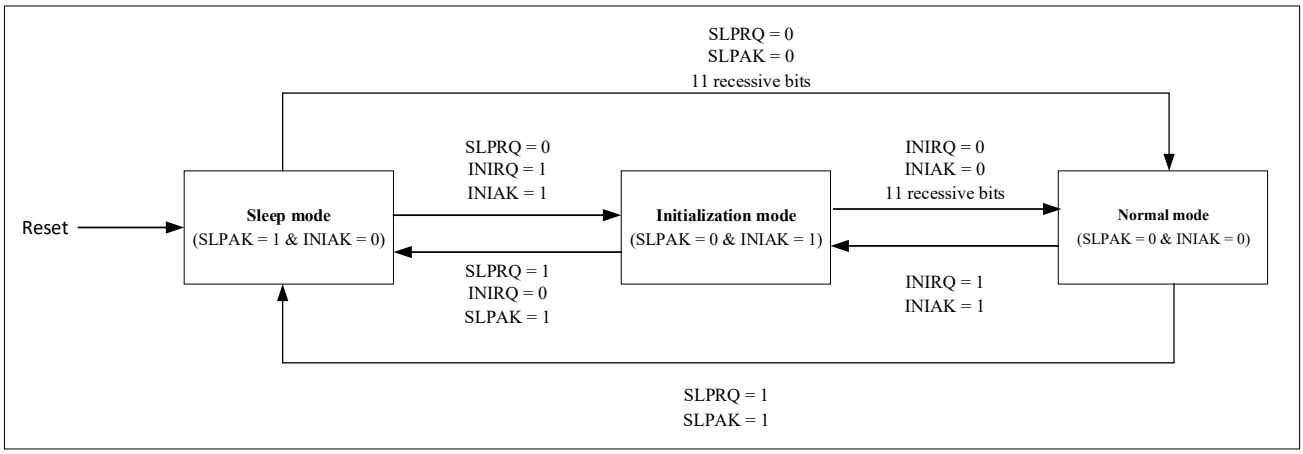
the software must clear the CAN_MCTRL.SLPRQ bit to exit the sleep state.

If the wake-up interrupt (set the CAN_INTE.WKUITE bit) is enabled, the wake-up interrupt will be generated once the CAN bus activity is detected, regardless of whether the hardware is enabled to automatically wake up CAN.

The CAN must be synchronized with the CAN bus before entering Normal mode Wait until the CAN_MSTS.SLPAK bit cleared to confirm the sleep mode has exited.Please refer to Figure 20-2.

Figure 20-2 CAN working mode



Notes: the state that the hardware sets the CAN_MSTS.INIAK or CAN_MSTS.SLPAK bit in response to a sleep or initialization request.

20.3.3 Send mailbox

Applications can send messages through three sending mailboxes. The order of sending three mailbox messages is determined by the sending scheduler according to the priority of the messages, and the priority can be determined by the identifier of the messages or by the order of sending requests.

20.3.4 Receiving filter

Each CAN has 14 configurable identifier filter groups. After the application configures the identifier filter group, the receiving mailbox will automatically receive the required messages and discard other messages.

20.3.5 Receive FIFO

Each CAN has two receiving FIFOs, each of which can store three complete messages. No application program is needed to manage it, and it is managed by hardware.

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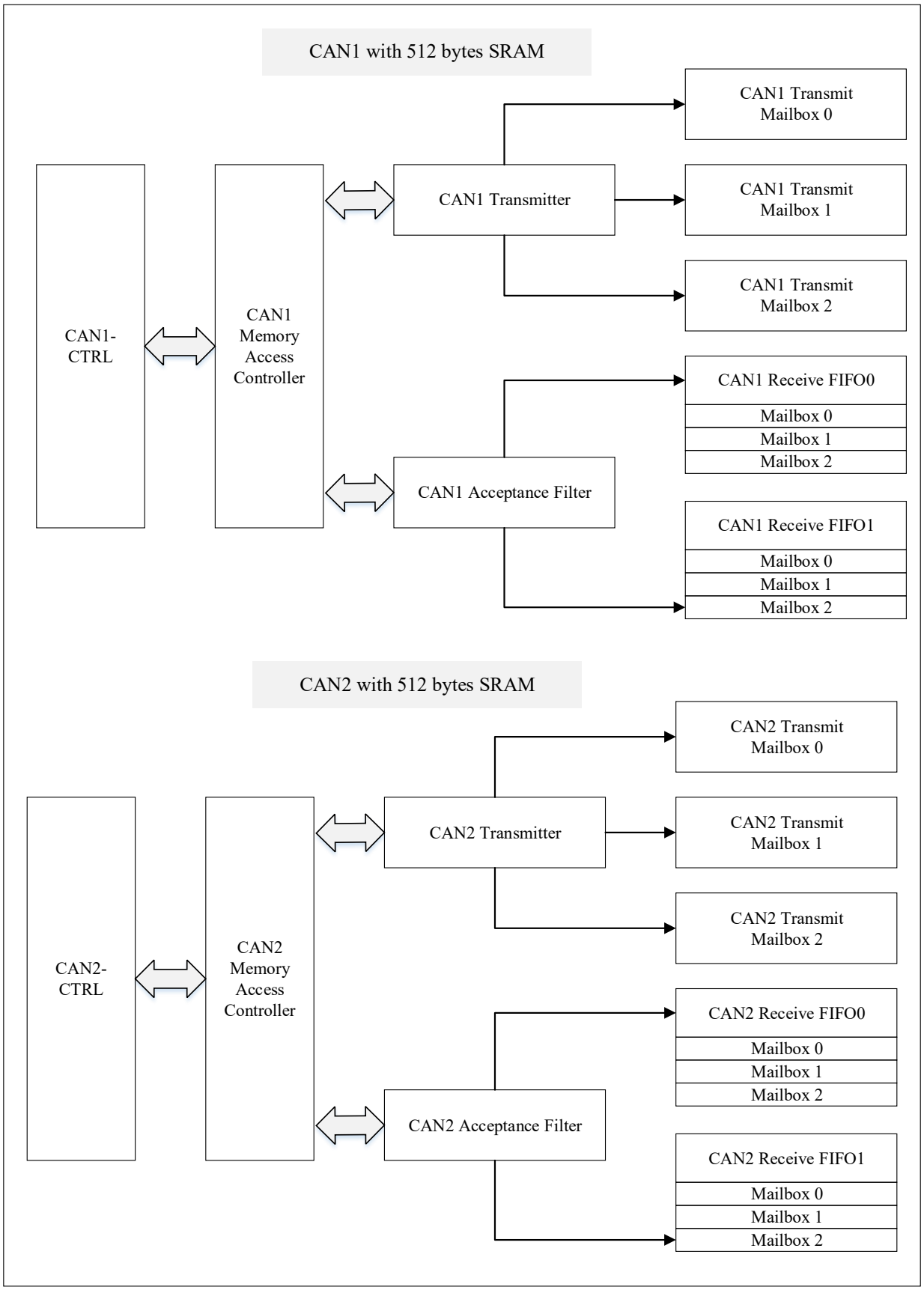
Figure 20-3 Dual CAN block diagram



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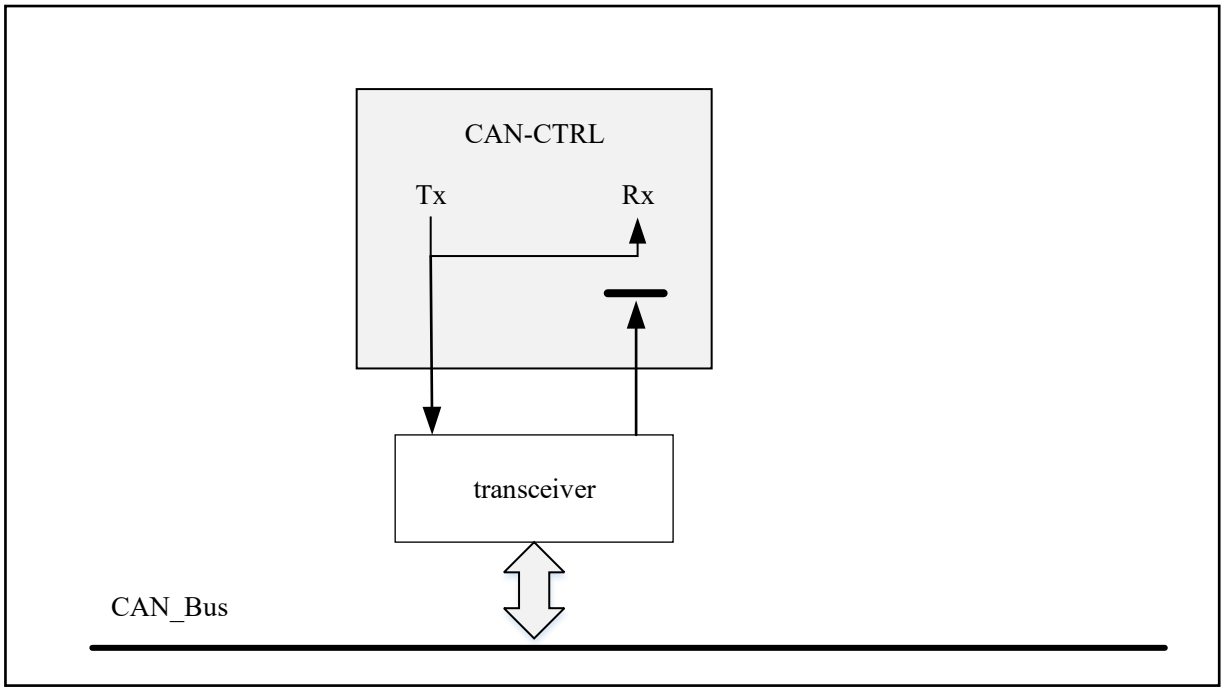
20.3.6 CAN Test mode

In the initialization mode, a test mode must be selected by combining the CAN_BTIM.SLM bit and CAN_BTIM.LBM bit. After selecting a test mode, the software needs to clear the CAN_MCTRL.INIRQ bit to exit the initialization mode and enter the test mode.

20.3.6.1 Loopback mode

Loopback mode can be used for self-test. In loopback mode, CAN saves the sent message in the receiving mailbox as received message (if it can be filtered by reception). In loopback mode, CAN internally feeds back the Tx output to the Rx input, completely ignoring the actual state of the CANRX pin. The message sent can be detected on the CANTX pin. In order to avoid external influence, the CAN kernel ignores the acknowledgement error(at the moment of acknowledgement bit of data/remote frame, it does not detect whether there is an dominant bit). To enter loopback mode, the CAN_BTIM.SLM bit should be cleared and the CAN_BTIM.LBM bit should be set.

Figure 20-4 loopback mode



20.3.6.2 Silent mode

In silent mode , CAN can normally receive data frames and remote frames, but can only send recessive bits, and can't really send messages. If CAN needs to send overload flag, active error flag or ACK bit(these are dominant bits), such dominant bits are internally connected back so as to be detected by the CAN core. At the same time, the CAN bus will not be affected and still remain in the recessive bit state. Therefore, the silent mode is usually used to analyze the activity of the CAN bus, without affecting the bus because dominant bits is not actually sent to the bus.

To enter silent mode, the CAN_BTIM.SLM bit should be set and the CAN_BTIM.LBM bit should be cleared.

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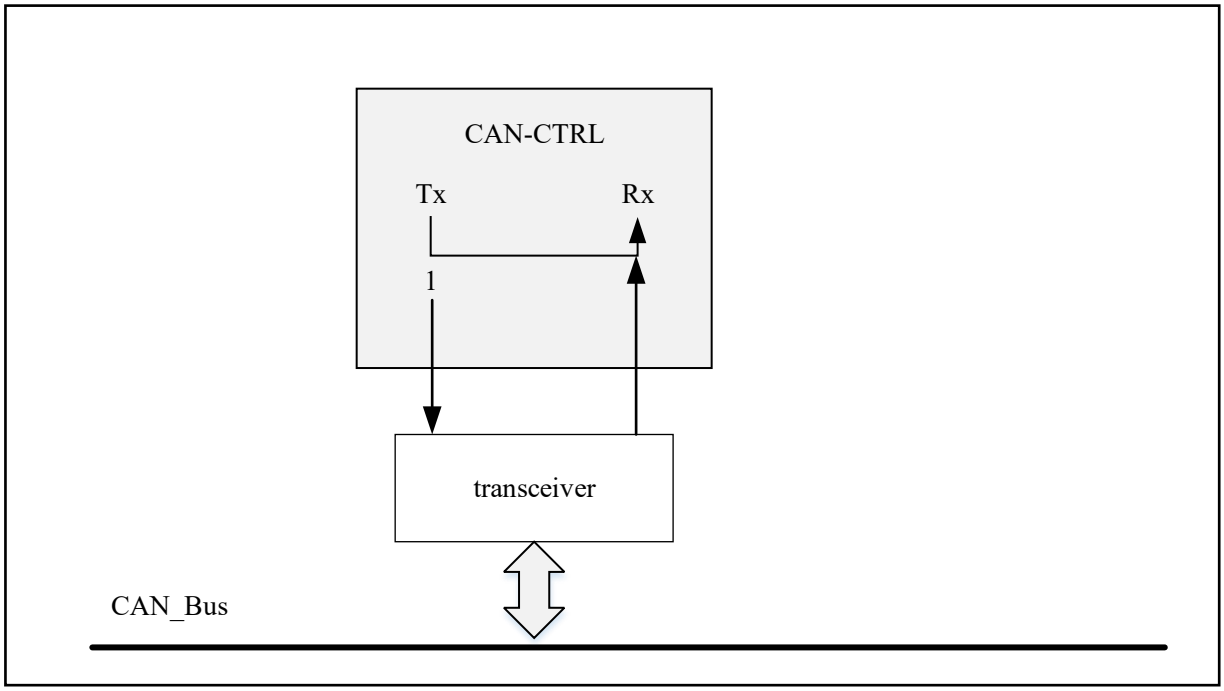
Figure 20-5 silent mode

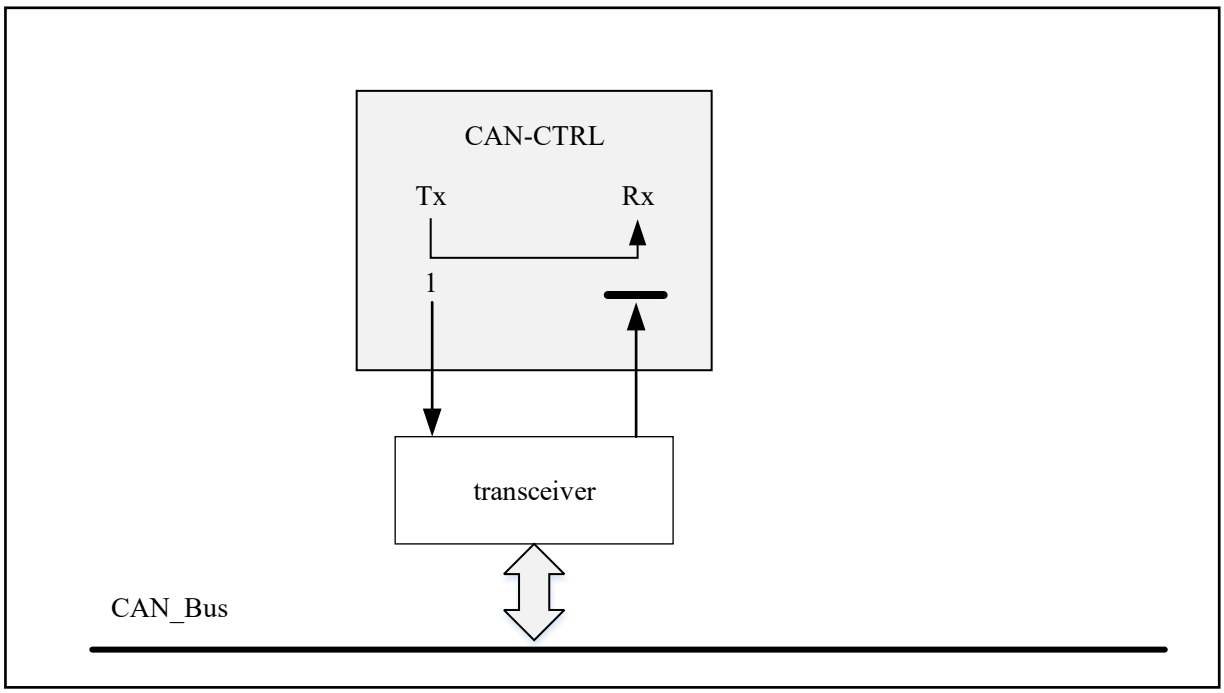


20.3.6.3 Loopback silence mode

In loopback silent mode, the CANRX pin is disconnected from the CAN bus, while the CANTX pin is driven to the recessive bit state. It can be used for "Run-time self diagnose" just like CAN can be tested in loop-back mode, but not affect the whole CAN system connected by CANTX and CANRX.

To enter loopback silence mode, both the CAN_BTIM.SLM bit and the CAN_BTIM.LBM bit should be set.

Figure 20-6 loopback silent mode



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20.3.7 CAN Debugging mode

CAN can continue to work normally or stop working according to the state of the following configuration bits:

- DBG_CTRL.CAN1_STOP bit of CAN1 and DBG_CTRL.CAN2_STOP bit of CAN2 in the debug support(DBG) module.See paragraph 29.3.2 Section: Peripheral debugging support.
- CAN_MCTRL.DBGF bit see paragraph 20.7.3.1 Section: CAN_MCTRL.

When the microcontroller is in debug mode, Cortex-M4F core is in a suspended state.

20.4 CAN function description

20.4.1 Send processing

The process of sending messages is as follows:

- The application program selects an **empty** sending mailbox;
- Writes the identifier, data length and data to be sent in the sending mailbox register;
- Set the CAN_TMIx.TXRQ bit to request transmission(after CAN_TMIx.TXRQ is set the mailbox is no longer an empty mailbox and the software has no permission to write to the mailbox register);
- The mailbox enter the **pending** state and wait to be the highest priority, see 20.4.1.1 Send priority;
- Changing to the **Ready** status once the mailbox becomes the highest priority mailbox;
- The messages in the ready mailbox is sent as soon as the CAN bus enters the idle state, then enter the sending state.
- Become an **empty** mailbox when the message in the mailbox is successfully sent;
- Hardware set the RQCPM and TXOKM bits of the corresponding mailbox in CAN_TSTS register to indicate a successful transmission.

However, if the transmission fails, the CAN_TSTS.ALSTM bit will be set to indicate that the failure is caused by arbitration or the CAN_TSTS.TERRM bit will be set to indicates that it is caused by the transmission error (for specific errors, please check the CAN_ESTS.LEC[2:0] error code bits of the error status).

20.4.1.1 Send priority

Determined by the order of sending requests.

Set the CAN_MCTRL.TXFP bit, and the sending mailbox can be configured as a sending FIFO. At this time, the priority of sending is determined by the order of sending requests. This mode is useful for segmented transmission.

Determined by the identifier.

According to CAN protocol, the message with the lowest identifier has the highest priority. If the values of identifiers are equal, the message with small mailbox number is sent first. When more than one sending mailbox is registered, the sending order is determined by the identifier of the message in the mailbox.

20.4.1.2 Cancel sending

Set the CAN_TSTS.ABRQM bit can abort sending the request. If the mailbox is ready or pending, the sending request

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will be aborted immediately. If the mailbox is in the transmitting state, the request to abort may lead to two kinds of results:

- if the message in the mailbox fails to be sent, the mailbox becomes ready state, then the sending request is aborted, the mailbox becomes an empty mailbox and the CAN_TSTS.TXOKM bit is cleared;
- if the message in the mailbox is successfully sent, the mailbox becomes an empty mailbox, and the CAN_TSTS.TXOKM bit will be set by hardware.

Therefore, when the sending mailbox is in the sending state, regardless of the sending result, the mailbox will become an empty mailbox after the sending operation is finished.

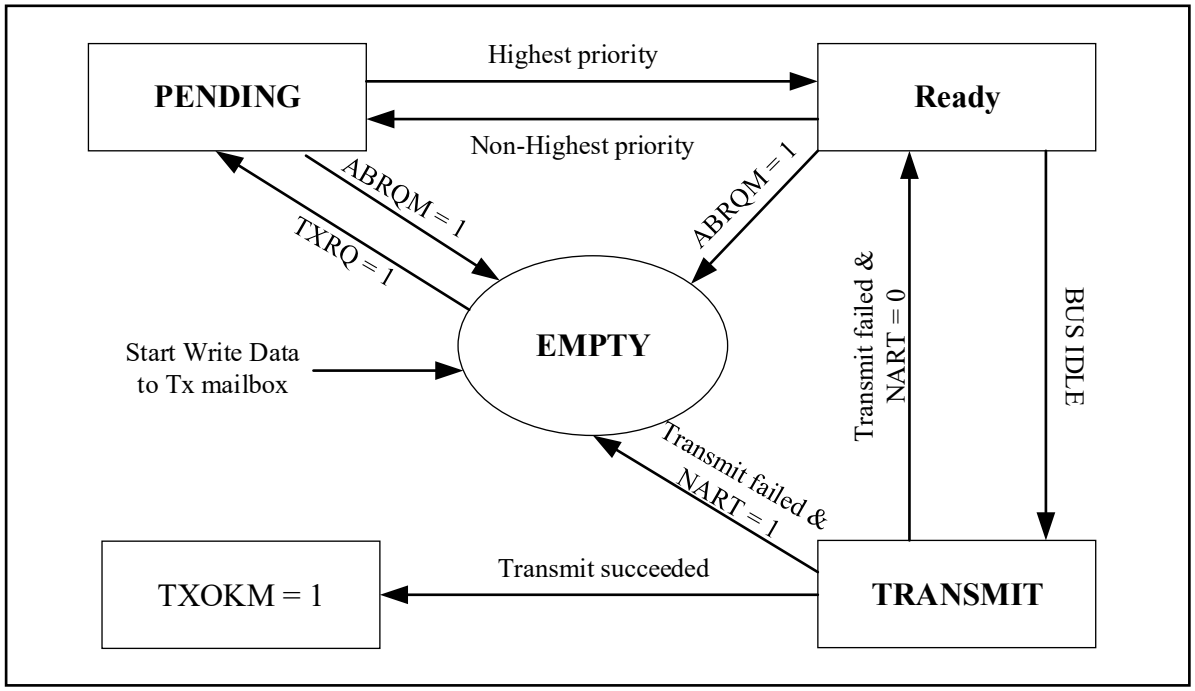
20.4.2 Time triggered communication mode

The internal timer of CAN is activated in time triggered communication mode. It is incremented at each CAN bit time (see 20.4.7 Section). CAN samples the value of the internal timer at the sampling point position of the received and sent frame start bits, and the sampled value is the time stamp of the sending and receiving mailboxes. Timestamps generate form the internal timer will be stored in the CAN_RMDTx/CAN_TMDTx registers respectively.

20.4.3 Non-automatic retransmission mode

To enable non-automatic retransmission mode the CAN_MCTRL.NART bit should be set. This mode corresponds to the function of time-triggered communication option in CAN standard.In non-automatic retransmission mode , the sending operation will only be executed once. If the sending operation fails, whether due to arbitration loss or error, the hardware will not automatically send the message again.At the end of a transmission operation, the hardware judge that the transmission request has been completed, and the hardware sets the CAN_TSTS.RQCPM bit. At the same time, the transmission result can query the CAN_TSTS.TXOKM, CAN_TSTS.ALSTM and CAN_TSTS.TERRM bits.

Figure 20-7 Send mailbox status



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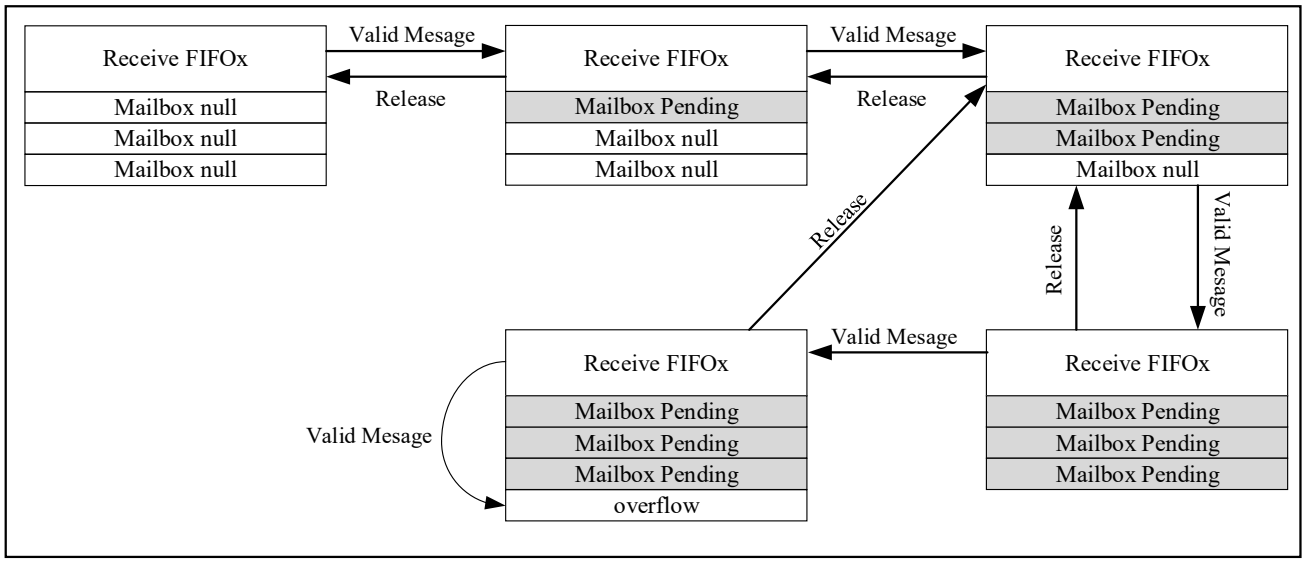
20.4.4 Receiving management

FIFOs with 3 levels depth are used to store received messages. When the application reads the FIFO output mailbox, it reads the first received message in the FIFO. FIFO is completely managed by hardware, which can simplify the application program, ensure the consistency of data and reduce the processing time of CPU.

20.4.4.1 Valid message

According to CAN protocol, when the message is correctly received (no errors are sent up to the last bit of the EOF field) and passes the identifier filtering, then the message is token as a valid message. Please refer to 20.4.5 Section: identifier filtering.

Figure 20-8 Receive FIFO status



20.4.4.2 FIFO receive

A FIFO includes mailboxes with three levels of depth, and the initial state is empty. After receiving the first valid message, one of the mailboxes will be suspended, and the hardware will set the CAN_RFF.FFMP[1:0] bits to 1 to indicate the receipt of a valid message. A valid message is received again before the mailbox is released. At this time, two mailboxes will be suspended at the same time, and the hardware will set the CAN_RFF.FFMP[1:0] bits to 2 to indicate that two valid messages are pending. As above, the third valid message will suspend all three mailboxes and set the CAN_RFF.FFMP[1:0] bits to 3.

When the three-level mailboxes of the FIFO are all suspended, receiving a valid message again will cause the mailbox to overflow and lose a message, and the hardware will set the CAN_RFF.FFOVR bit to 1 to indicate the occurrence of the event. The rules for lost messages depend on the configuration of the FIFO. If the FIFO lock function is disabled (clear the CAN_MCTRL.RFLM bit), then the last message received in the FIFO will be overwritten by the new message. In this way, the latest received message will not be discarded;If the FIFO lock function is enabled (set the CAN_MCTRL.RFLM bit), then the newly received messages will be discarded, and the software can read the first three messages in the FIFO.

20.4.4.3 FIFO release

The message stored in the FIFO will be read through the corresponding receive mailbox. The software reads the mailbox message and releases the mailbox by setting the CAN_RFR.RFOM bit to 1 , and he CAN_RFF.FFMP[1:0]

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bit is decremented by 1 until it is 0.

20.4.4.4 Receive related interrupts

The hardware will update the CAN_RFF.FFMP[1:0] bits when a message is stored in the receiving FIFO. If the FIFO message pending interrupt is currently enabled (the CAN_INTE.FMPITE bit is set), then the FIFO message pending interrupt request will be generated.

When the third message is stored ,the FIFO becomes full, then the CAN_RFF.FFULL bit will be set, and if the FIFO full interrupt is currently enabled (the CAN_INTE.FFITE bit is set), a FIFO full interrupt request will be generated.

When the FIFO overrun, the FFOVR bit will be set. If the FIFO overrun interrupt is currently enabled (the CAN_INTE.FOVITE bit is set), a FIFO overrun interrupt request will be generated.

20.4.5 Identifier filtering

In the CAN network, when basic CAN is in the transmitter state, it broadcasts a message to each node by sending a message to the bus; when basic CAN is in the receiver state, it determines whether the node needs the message according to the identifier of the message after receiving the message. If message is vaild, CAN core copies the message to SRAM(CAN's own SRAM); If it is not needed, the message will be discarded. This process does not require software intervention. Compared with software filtering, hardware filtering reduces the CPU usage. CAN controller provides 14 configurable filter banks (0~13) with variable bit width for application programs to meet this demand. These filter banks are used to receive only those messages needed by software. Each filter bank x contains two 32-bit registers, namely CAN_FxR0 and CAN_FxR1.

20.4.5.1 Setting of filter bit width and mode

Each filter in a filter bank is numbered (filter number, from 0 to a certain maximum value) depending on the mode and bit width setting of the filter bank. See the figure below for the filter configuration.The filter group can be configured through the corresponding CAN_FMC register. Filter banks that are not used by the application should be kept disabled. Before configuring a filter bank, it must be set to the disabled state by clearing the CAN_FA1.FAC bit.

By setting the corresponding CAN_FS1.FSCx bit you can configure the bit width of a filter bank, see Figure 20-9.

By means of the CAN_FM1.FBx bit, the corresponding mask/identifier register can be configured to be the **identifier list** or **identifier mask** mode.The filter group should be set to work in the mask mode in order to filter out a group of identifiers. And the filter group should be set to work in identifier list mode in order to filter out an identifier.

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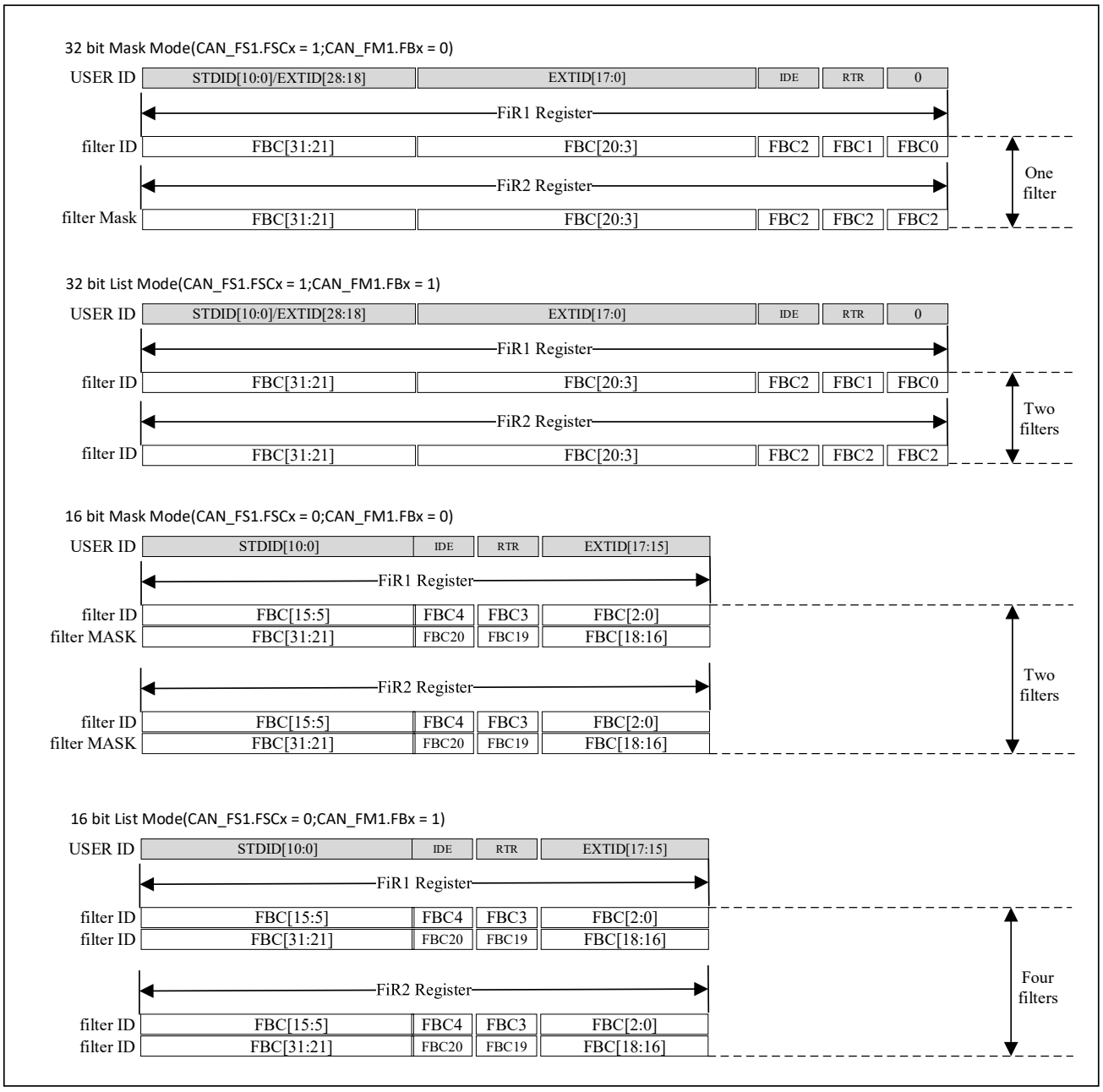
Figure 20-9 Filter bit width setting-register organization



20.4.5.2 Variable bit width

The bit width of each filter bank can be independently configured. Each filter bank can be configured to be one 32-bit filter: including STDID[10:0], EXTID[17:0], IDE and RTRQ bits; or two 16-bit filters,:including STDID[10:0], IDE, RTRQ and EXTID[17:15] bits, see Figure 20-9. In addition, the filter can be configured in two different modes, namely, the mask mode and the identifier list mode.

Mask mode

The filter ID is used to store the identifier format, and the filter MASK is used to indicate which bits must be checked and which bits can be ignored.

Identifier list mode

The filter ID is used to store the identifier format. At this time, there is no mask for comparison, and the mask bit can

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be used to store one more filter ID. However, at this time, the identifier of the message needs to be exactly the same as the filter ID format, otherwise it will fail to pass the filter.

20.4.5.3 Filter matching sequence number

After CAN core received an valid message it will matching the message ID with filters one by one until there is one filter pass or all filters failed. If this message failed to pass any enabled filter then it will be discarded. Otherwise when CAN core finds the first filter that the ID can pass, it pack filter index with the CAN message and stores inside receive FIFO in SRAM according to filter setting (CAN_FFA1 decides store in which FIFO). User can find filter index in FMI [7:0] bits of CAN_RMDTx register. This filter matching index can help to identify which types of message it is in this receive FIFO.

The filter matching sequence number can be used two ways. The first one is comparing the filter matching sequence number with a series of expected values. The another is using the filter matching sequence number as an index to access the target address. When numbering filters, whether the filter group is active or not is not considered. In addition, each FIFO numbers its associated filter. Please refer to the example below.

For the filter in mask mode, the software only needs to compare the mask bits that are needed (bits that must be matched). For the filter in identifier list mode (non-screening filter), the software does not need to directly compare with the identifier.

Table 20-1 Examples of filter numbers

Point to FIFOx	Filter group	Filter mode	FIFO0 filter number
FIFO	0	32 bit mask mode	0
	2	16 bit mask mode	1/2
	5	32 bit list mode	3/4
	7	16 bit list mode	5/6/7/8
	9	32 bit list mode	9/10
	11	16 bit list mode	11/12/13/14
	13	32 bit mask mode	15
Point to FIFOx	Filter group	Filter mode	FIFO1 filter number
FIFO1	1	32 bit list mode	0/1
	3	16 bit list mode	2/3/4/5
	4	32 bit mask mode	6
	6	16 bit mask mode	7/8
	8	32 bit mask mode	9

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	10	16 bit mask mode	10/11
	12	32 bit list mode	12/13

20.4.5.4 Filter priority rule

According to different configurations of filters, it is possible that a message identifier can be filtered by multiple filters; In this case, the filter matching serial number stored in the receiving mailbox is first determined according to bit width,32-bit-wide filters have higher priority than 16-bit-wide filters. For filters with the same bit width, then the identifier list mode takes precedence over the mask mode. If filters have the same bit width and mode, the priority is determined by the filter group number, and the filter group with lower number has the higher priority.Within a filter group,the lower the filter number,the higher the priority.

Figure 20-10 Examples of filter mechanisms

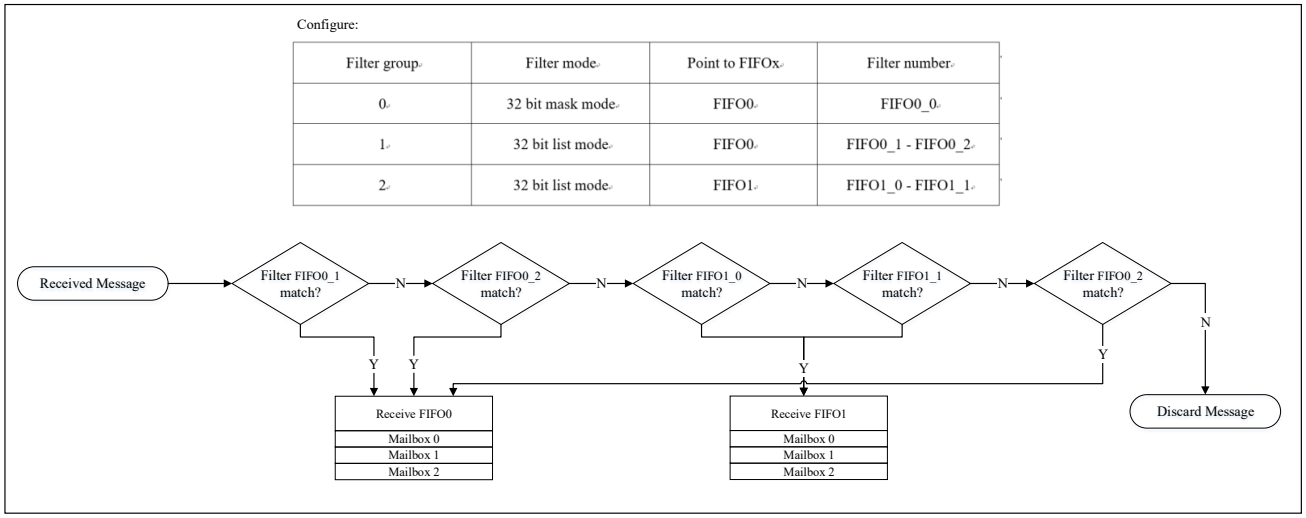

Figure 20-10 illustrates the filter rules of CAN. When receiving a message, its identifier is first compared with the filter configured in identifier list mode. If there is a match, the message will be stored in the associated FIFO, and the serial number of the matched filter will be stored in the filter matching serial number.

If there is no match, the message identifier is then compared with the filter configured in the mask mode. And the hardware will automatically discard the message without software intervention if the message identifier does not match any identifier in the filter.

20.4.6 Message storage

A mailbox contains all information related to a message: identifier, data, control, status and time stamp information. Mailbox is the interface between software and hardware to transfer messages.

20.4.6.1 Send mailbox

Message should be written into an empty sending mailbox by software before enable the sending request. You can query the sending status through the CAN_TSTS register.

Table 20-2 Send mailbox register list

Offset from the base address of the sending mailbox	Register name

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0	CAN_TMIx
4	CAN_TMDTx
8	CAN_TMDLx
12	CAN_TMDHx

20.4.6.2 Receiving mailbox (FIFO)

CAN_RMDTx.FMI[7:0] field can store the filter matching serial number and CAN_RMDTx.MTIM[15:0] field can store the 16-bit timestamp.The software can access the output mailbox of the receiving FIFO to read the received message. Once the software has processed the message, such as reading it out, the software should set the CAN_RFFx.RFFOM bit to release the corresponding, so as to reserve storage space for later messages.

Table 20-3 Receive mailbox register list

Offset from the base address of the receiving mailbox	Register name
0	CAN_RMIx
4	CAN_RMDTx
8	CAN_RMDLx
12	CAN_RMDHx

20.4.7 Bit time characteristic

The bit time characteristic logic monitors the serial CAN bus by sampling, and adjusts its sampling point by synchronizing with the edge of the frame start bit and resynchronizing with the following edge. To avoid programming errors in software, setting the bit time characteristic register (CAN_BTIM) can only be done when CAN is initialized.

Its operation can be simply understood as dividing each nominal time into three segments: Synchronization segment (SYNC_SEG), Time period 1(BS1) and Time period 2(BS2).

Usually, it is expected that the change of bits will occur in SYNC_SEG. Its value is fixed to 1 time unit ($1 \times t_{CAN}$).

BS1 defines the position of the sampling point. It includes PROP_SEG and PHASE_SEG1 in CAN standard. Its value can be programmed into 1 to 16 time units, but in order to compensate the forward drift of phase caused by the frequency difference of different nodes in the network, it can also be automatically extended.

In BS2, it defines the location of the sending point. It stands for PHASE_SEG2 in CAN standard. Its value can be programmed into 1 to 8 time units, but it can also be automatically shortened to compensate for the negative drift of phase.

If a valid transition is detected in BS1 but not in SYNC_SEG, then the time of BS1 is extended by at most RSJW to delay the sampling point. On the contrary, if a valid transition is detected in BS2 but not in SYNC_SEG, then the time of BS2 is shortened at most RSJW to advance the sampling point.

In the above description, RSJW(the resynchronization hop width) defines the upper limit of how many time units can be extended or shortened in each bit. Its value can be programmed into 1 to 4 time units. The effective transition is defined as the first transition from the dominant bit to the recessive bit when CAN itself does not send the recessive bit.

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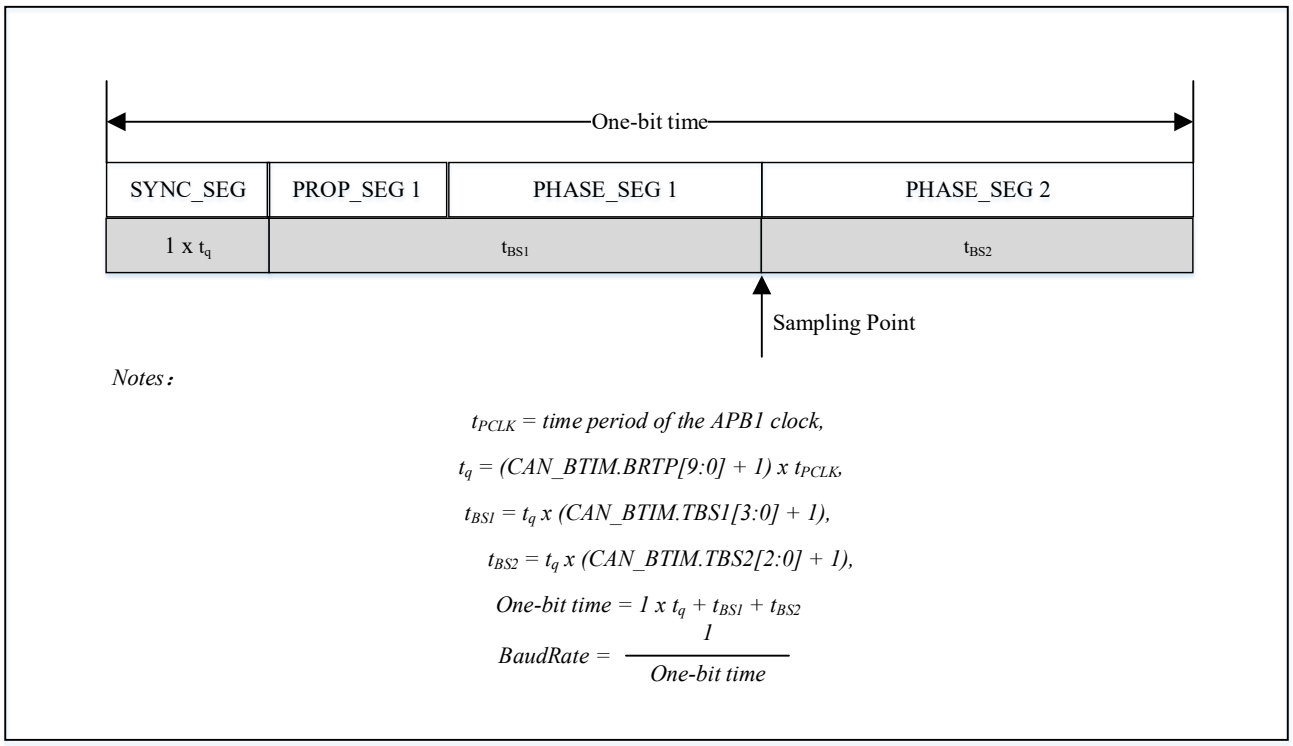
Note: 1. The time characteristics and resynchronization mechanism of CAN bits are detailed in the ISO11898 standard.

2. In order to improve the CAN bit time accuracy, it is not recommended to use HSI as the clock source.

Figure 20-11 Bit sequence



Notes:

t_{PCLK} = *time period of the APB1 clock,*

$t_q = (CAN\_BTIM.BRTP[9:0] + 1) \times t_{PCLK}$,

$t_{BS1} = t_q \times (CAN\_BTIM.TBS1[3:0] + 1)$,

$t_{BS2} = t_q \times (CAN\_BTIM.TBS2[2:0] + 1)$,

$One\text{-}bit\ time = 1 \times t_q + t_{BS1} + t_{BS2}$

$$BaudRate = \frac{1}{One\text{-}bit\ time}$$

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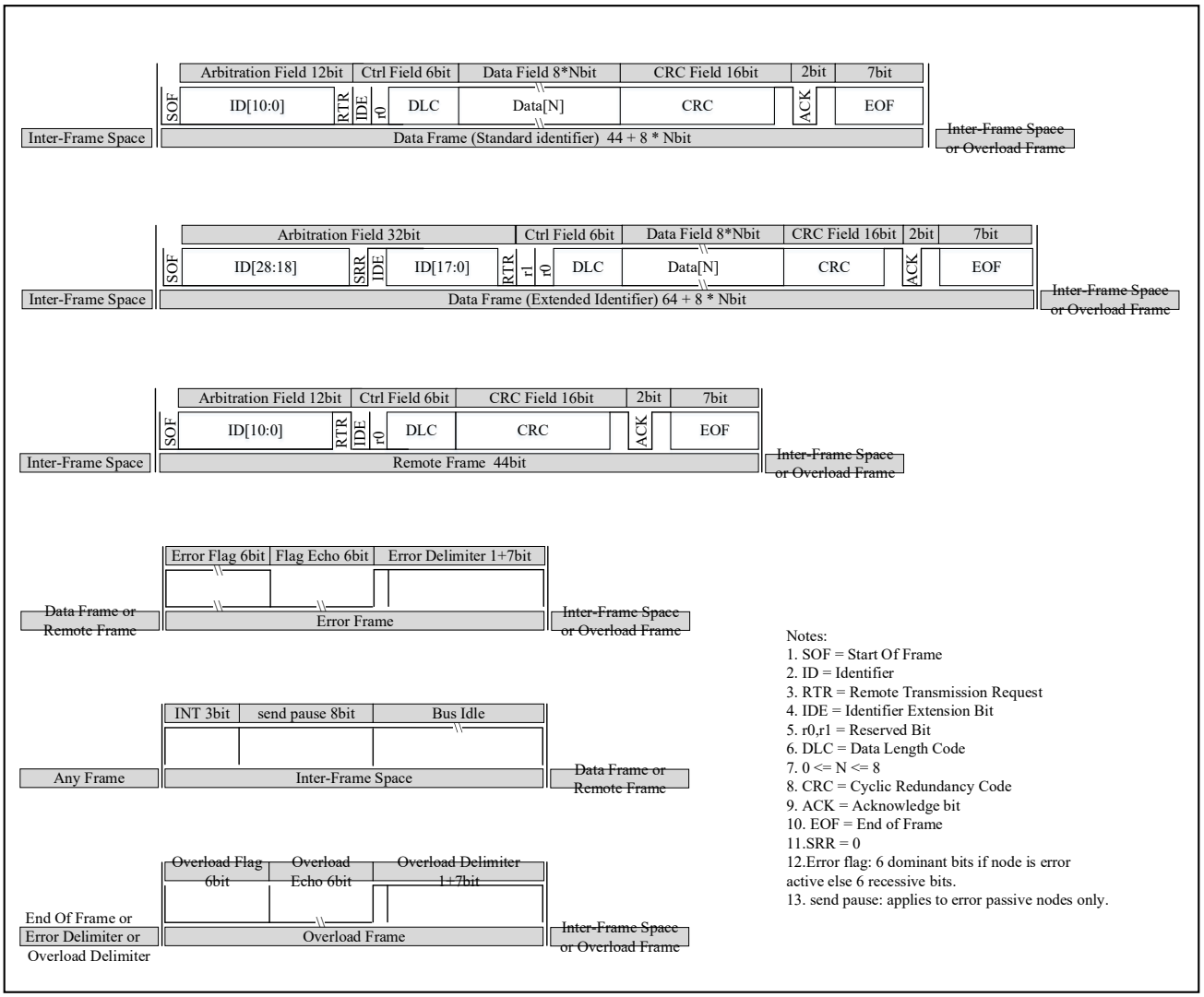
Figure 20-12 Various CAN frames



Notes:
1. SOF = Start Of Frame
2. ID = Identifier
3. RTR = Remote Transmission Request
4. IDE = Identifier Extension Bit
5. r0,r1 = Reserved Bit
6. DLC = Data Length Code
7. 0 <= N <= 8
8. CRC = Cyclic Redundancy Code
9. ACK = Acknowledge bit
10. EOF = End of Frame
11.SRR = 0
12.Error flag: 6 dominant bits if node is error active else 6 recessive bits.
13. send pause: applies to error passive nodes only.

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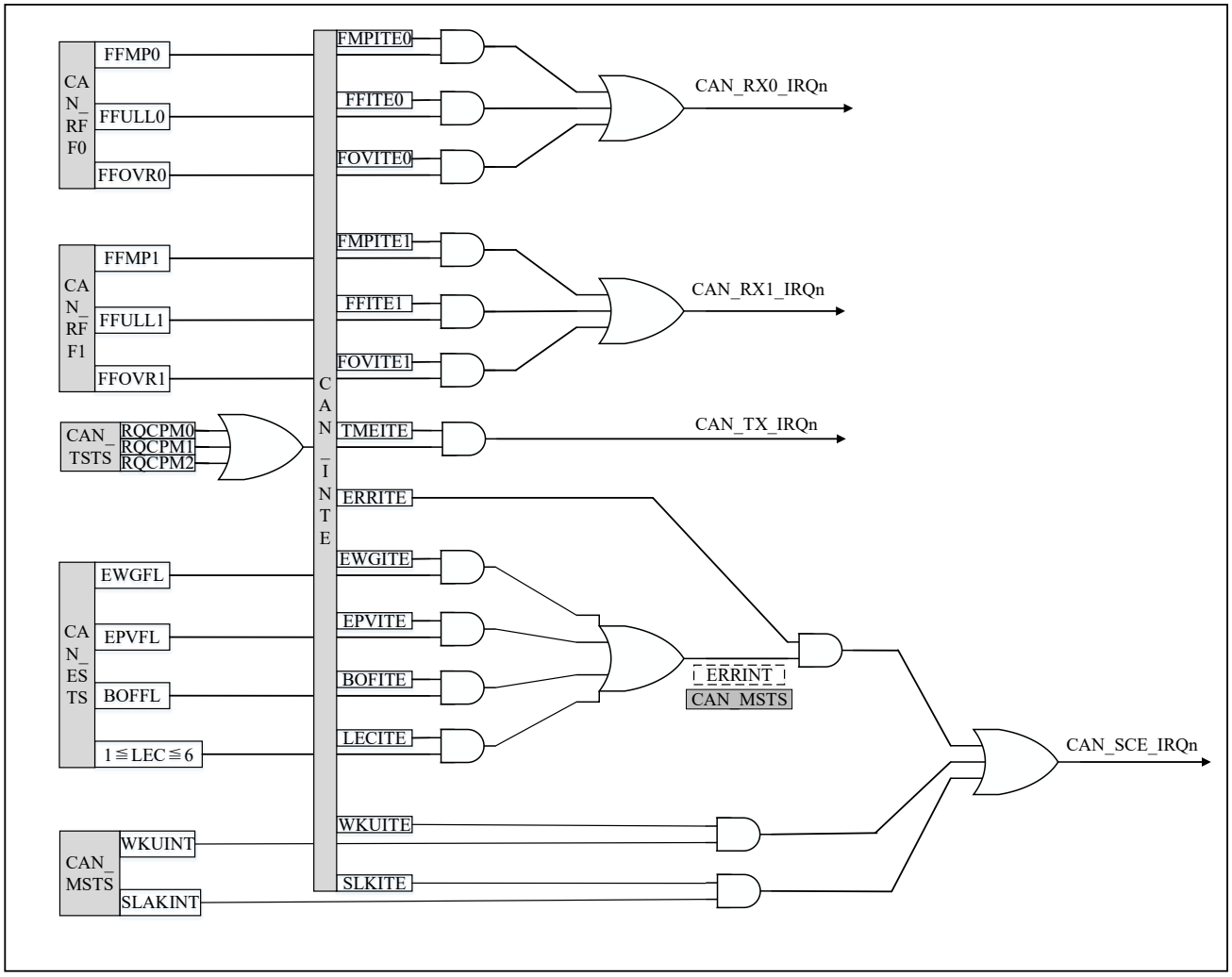
20.5 CAN interrupt

Figure 20-13 Event flag and interrupt generation



CAN has four interrupt vectors. By setting the CAN interrupt enable register (CAN_INTE), you can individually enable or disable each interrupt source. The following are the events that can generate each interrupt.

- FIFO0 interrupt(CAN_RX0_IRQn):

  FIFO0 receives a new message, and the CAN_RFF0.FFMP0 bit is not '00' ;

  When FIFO0 becomes full, and the CAN_ RFF0.FFULL0 bit is set;

  When FIFO0 overruns, and the CAN_ RFF0.FFOVR0 bit is set.

- FIFO1 interrupt(CAN_RX1_IRQn):

  FIFO1 receive a new message, and the CAN_RFF1.FFMP1 bit is not '00'.

  When FIFO1 becomes full, and the CAN_RFF1.FFULL1 bit is set.

  When FIFO1 overruns, and the CAN_ RFF1.FFOVR1 bit is set.

- Send interrupts(CAN_TX_IRQn):

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Send mailbox x becomes empty, and the corresponding CAN_TSTS.RQCPMx bit is set(x=1/2/3).

- **Error and status change interrupt**(CAN_SCE_IRQn):

  CAN enters sleep mode;

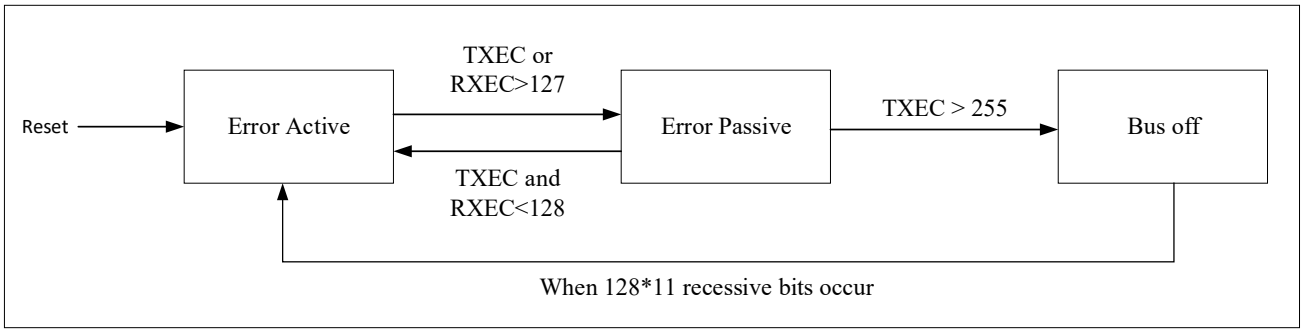
  Wake-up condition, the start of frame bit (SOF) is monitored on the CAN receiving pin.

  Error condition, please refer to the CAN error status register (CAN_ESTS) for details of the error.

20.5.1 Error management

As described in CAN protocol, the error management is completely realized by hardware through sending error counter (CAN_ESTS.TXEC field) and receiving error counter (CAN_ESTS.RXEC field). The counter value will increase or decrease according to the error situation. Please refer to CAN standard if you want to know more detailed information about CAN_ESTS.TXEC and CAN_ESTS.RXEC management.

Figure 20-14 CAN error state diagram



Software can read out the value of the sending/receiving error counter to judge the stability of CAN network, and CAN_ESTS.LEC[2:0] bits can be read to get the detailed information of the current error status. What's more, by setting the CAN_INTE register (such as CAN_INTE. LECITE bit), the software can flexibly control the generation of interrupts when an error is detected.

20.5.2 Bus-Off recovery

When TXEC is greater than 255, the CAN_ESTS.BOFFL bit is set indicating that CAN goes bus-off. at this time, CAN can't receive and send messages.

In normal mode, according to the CAN_MCTRL.ABOM bit, CAN can automatically or at the request of software, recover from bus-off state, and change to error active state. If the CAN_MCTRL.ABOM bit is set, the recovery process will be started automatically after it has entered bus-off state. Otherwise, the recovery process will be started after software must request CAN to enter and then exit initialization mode. In both cases, CAN must wait for a recovery process described in CAN standard, that is 128*11 consecutive recessive bits are detected on CAN RX pin.

In initialization mode, CAN will not monitor the status of CAN RX pin, so the recovery process cannot be completed.

20.6 CAN Configuration Flow

This chapter will introduce common configuration procedure of CAN while other details like functions of each mode and register bits are revealed in other part of this manual. CAN configuration flow can divided into serval phases. Some of the configurations can be changed anytime as long as prior requirements are satisfyied (e.g., filter value).

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- **Preparation Stage:**

1. Configure RCC to enable CAN clock
2. Configure RCC to enable AFIO and GPIO clock
3. Write into GPIO registers to map CAN TX and CAN RX signals to desired GPIO pins.

- **Basic Configuration Stage:**

1. After reset CAN device starts with Sleep mode.
2. Exit Sleep mode by clearing CAN_MCTRL.SLPRQ bit.
3. Enter Initialization mode by setting CAN_MCTRL.INIRQ bit.
4. Wait for CAN_MSTS.INIAK bit become 1 (enter Initilization mode).
5. Configure bit timing for CAN by writing value to CAN_BTIM.BSJW, CAN_BTIM.TBS2, CAN_BTIM.TBS1 and CAN_BTIM.BRTP bits. Baud rate of CAN bus is defined by the formula below:

$$BaudRate = \frac{1}{\big(1 + (TBS1 + 1) + (TBS2 + 1)\big) * (BRTP * t_{pclk})}$$

6. Configure work mode options for CAN by writing to CAN_BTIM.SLM (silent) or CAN_BTIM.LBM in register.
7. Configure CAN behavior(TTCM,ABOM,AWKUM,NART,RFLM,TXFP) through CAN_MCTRL. Most of the configuration in this register can be changed on the fly but its advised not to do so. Otherwise during few cycles, CAN behavior will become unpredictable.
8. Exit Initialization mode by clearing CAN_MCTRL.INIRQ bit.
9. Wait for CAN_MSTS.INIAK bit become 0 (exit Initilization mode).
10. User can use filters to filter the messages they want to receive. To configure filter, user needs to write '1' to CAN_FMC.FINITM bit to request the filters to enter initialization mode. When filter is in initialization mode, CAN stops reception.
11. Configure each filter for working mode (CAN_FM1), filter scale (CAN_FS1) and filter assignment (CAN_FFA1). User can also change filter value (CAN_FiRx) during this time. After completing filter configuration, clear CAN_FMC.FINITM bit to exit initialization for filters.

- **For transmission:**

1. Enable the necessary transmit related interrupt CAN_INTE.TMEITE bit.
2. Check status bits of each mailbox in CAN_TSTS. If any mailbox with TMEMx (x = 0~2) is '1', user can write the message, which is waiting for transmission, to the corresponding mailbox address. CAN_TMIx.TXRQ(x = 0~2) bit must be written to '1' after this mailbox is programed.
3. After some time or after waiting for transmit interrupts, come back to check transmit status in CAN_TSTS. Repeat step 2~3 for new message transmission.

- **For Reception:**

1. User can also change a filter value (**CAN_FiRx**) when the corresponding filter is deactivated. To deactivate certain filter, user needs to write '0' to the corresponding bit in **CAN_FA1** register.
2. Configure reception related interrupts in CAN_INTE register.

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3. Once CAN has received message and stored them inside reception FIFO, user needs to read the corresponding FIFO on time and release reception mailbox by writing '1' to RFFOMx in register CAN_RFFx (x = 0,1).

20.7 CAN Register File

These peripheral registers must be operated as words (32 bits).

20.7.1 Register Description

20.7.1.1 Register access protection

When a CAN node is working normally, incorrect access/modification of some configuration registers may cause hardware errors in the node and temporarily interfere with the entire CAN network. Therefore, modification of the CAN_BTIM register is only allowed when the CAN core is in initialization mode.

Only when the send mailbox status bit CAN_TSTS.TMEM = 1 then the user can modify data to the send mailbox.

20.7.1.2 Control and status registers

By configuring these registers, user can: configure CAN parameters, such as working mode and baud rate; start message sending; handling message reception; interrupt setting; read diagnostic information.

20.7.1.3 Mailbox Register Description

The sending and receiving mailboxes are basically the same except that the receiving mailbox is read-only and contains the CAN_RMDTx.FMI field. The sending mailbox is writable when it is empty.

***Notes**: the corresponding CAN_TSTS.TMEM bit is set, which means that the sending mailbox is empty.*

There are 3 sending mailboxes and 2 receiving FIFO. Each receiving FIFO has three mailboxes, and only the first received message in the FIFO can be accessed.

Each mailbox contains 4 registers:

FIFO0 contains CAN_RMI0, CAN_RMDT0, CAN_RMDL0, CAN_RMDH0;

FIFO1 contains CAN_RMI1, CAN_RMDT1, CAN_RMDL1, CAN_RMDH1;

Send mailbox (x) contains CAN_TMIx, CAN_TMDTx, CAN_TMDLx, CAN_TMDHx; x = 0,1,2.

20.7.1.4 Filter Register Description

The value of the filter can only be modified when the corresponding filter group is closed or the CAN_FMC.FINITM bit is set. In addition, only when the whole filter is set to the initialization mode (that is, CAN_FMC.FINITM=1), the settings of the filter can be modified, that is, the CAN_FM1,CAN_FS1 and CAN_FFA1 registers can be modified.

20.7.2 CAN register address overview

Table 20-4 CAN register overview

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
000h	CAN_MCTRL	Reserved															DBGF	MRST	Reserved							TTCM	ABOM	AWKUM	NART	RFLM	TXFP	SLPRQ	INIRQ
	Reset Value																1	0								0	0	0	0	0	0	1	0

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Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
004h	CAN_MSTS	Reserved																				RXS	LSMP	RXMD	TXMD	Reserved			SLAKINT	WKUINT	ERRINT	SLPAK	INIAK
	Reset Value																					1	1	0	0				0	0	0	1	0
008h	CAN_TSTS	LOWM[2:0]			TMEM[2:0]			CODE[1:0]		ABRQM2	Reserved			TERRM2	ALSTM2	TXOKM2	RQCPM2	ABRQM1	Reserved			TERRM1	ALSTM1	TXOKM1	RQCPM1	ABRQM0	Reserved			TERRM0	ALSTM0	TXOKM0	RQCPM0
	Reset Value	0	0	0	1	1	1	0	0	0				0	0	0	0	0				0	0	0	0	0				0	0	0	0
00Ch	CAN_RFF0	Reserved																										RFFOM0	FFOVR0	FFULL0	Reserved	FFMP0[1:0]	
	Reset Value																											0	0	0		0	0
010h	CAN_RFF1	Reserved																										RFFOM1	FFOVR1	FFULL1	Reserved	FFMP1[1:0]	
	Reset Value																											0	0	0		0	0
014h	CAN_INTE	Reserved														SLKITE	WKUITE	ERRITE	Reserved			LECITE	BOFITE	EPVITE	EWGITE	Reserved		FOVITE1	FFITE1	FMPITE1	FOVITE0	FFITE0	FMPITE0	TMEITE
	Reset Value															0	0	0				0	0	0	0			0	0	0	0	0	0	0
018h	CAN_ESTS	RXEC[7:0]								TXEC[7:0]								Reserved										LEC[2:0]			Reserved	BOFFL	EPVFL	EWGFL
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0											0	0	0		0	0	0
01Ch	CAN_BTIM	SLM	LBM	Reserved				RSJW[1:0]		Reserved	TBS2[2:0]			TBS1[3:0]				Reserved				BRTP[9:0]											
	Reset Value	0	0					0	1		0	1	0	0	0	1	1					0	0	0	0	0	0	0	0	0	0	0	0
020h - 17Fh	Reserved																																
180h	CAN_TMI0	STDID[10:0]/EXTID[28:18]											EXTID[17:0]																		IDE	RTRQ	TXRQ
	Reset Value	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	0
184h	CAN_TMDT0	MTIM[15:0]																Reserved				TGT	Reserved							DLC[3:0]			
	Reset Value	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x					x								x	x	x	x
188h	CAN_TMDL0	DATA3[7:0]								DATA2[7:0]								DATA1[7:0]								DATA0[7:0]							
	Reset Value	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
18Ch	CAN_TMDH0	DATA7[7:0]								DATA6[7:0]								DATA5[7:0]								DATA4[7:0]							
	Reset Value	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
190h	CAN_TMI1	STDID[10:0]/EXTID[28:18]											EXTID[17:0]																		IDE	RTRQ	TXRQ
	Reset Value	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	0
194h	CAN_TMDT1	MTIM[15:0]																Reserved				TGT	Reserved							DLC[3:0]			
	Reset Value	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x					x								x	x	x	x
198h	CAN_TMDL1	DATA3[7:0]								DATA2[7:0]								DATA1[7:0]								DATA0[7:0]							
	Reset Value	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

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19Ch	CAN_TMDH1	DATA7[7:0]								DATA6[7:0]								DATA5[7:0]								DATA4[7:0]							
	Reset Value	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
1A0h	CAN_TMI2	STDID[10:0]/EXTID[28:18]								EXTID[17:0]																					IDE	RTRQ	TXRQ
	Reset Value	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	0
1A4h	CAN_TMDT2	MTIM[15:0]																Reserved							TGT	Reserved					DLC[3:0]			
	Reset Value	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x								x					x	x	x	x
1A8h	CAN_TMDL2	DATA3[7:0]								DATA2[7:0]								DATA1[7:0]								DATA0[7:0]							
	Reset Value	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
1ACh	CAN_TMDH2	DATA7[7:0]								DATA6[7:0]								DATA5[7:0]								DATA4[7:0]							
	Reset Value	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
1B0h	CAN_RMI0	STDID[10:0]/EXTID[28:18]								EXTID[17:0]																					IDE	RTRQ	Reserved
	Reset Value	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	
1B4h	CAN_RMDT0	MTIM[15:0]																FMI[7:0]								Reserved					DLC[3:0]		
	Reset Value	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x					x	x	x	x
1B8h	CAN_RMDL0	DATA3[7;0]								DATA2[7:0]								DATA1[7:0]								DATA0[7:0]							
	Reset Value	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
1BCh	CAN_RMDH0	DATA7[7:0]								DATA6[7:0]								DATA5[7:0]								DATA4[7:0]							
	Reset Value	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
1C0h	CAN_RMI1	STDID[10:0]/EXTID[28:18]								EXTID[17:0]																					IDE	RTRQ	Reserved
	Reset Value	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	
1C4h	CAN_RMDT1	MTIM[15:0]																FMI[7:0]								Reserved					DLC[3:0]		
	Reset Value	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x					x	x	x	x
1C8h	CAN_RMDL1	DATA3[7:0]								DATA2[7:0]								DATA1[7:0]								DATA0[7:0]							
	Reset Value	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
1CCh	CAN_RMDH1	DATA7[7:0]								DATA6[7:0]								DATA5[7:0]								DATA4[7:0]							
	Reset Value	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
1D0h - 1FFh	Reserved																																
200h	CAN_FMC	Reserved																															FINITM
	Reset Value																																1

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204h	CAN_FM1	Reserved																		FB[13:0]													
	Reset Value																			0	0	0	0	0	0	0	0	0	0	0	0	0	0
208h	Reserved																																
20Ch	CAN_FS1	Reserved																		FSC[13:0]													
	Reset Value																			0	0	0	0	0	0	0	0	0	0	0	0	0	0
210h	Reserved																																
214h	CAN_FFA1	Reserved																		FAF[13:0]													
	Reset Value																			0	0	0	0	0	0	0	0	0	0	0	0	0	0
218h	Reserved																																
21Ch	CAN_FA1	Reserved																		FAC[13:0]													
	Reset Value																			0	0	0	0	0	0	0	0	0	0	0	0	0	0
220h	Reserved																																
224h - 23Fh	Reserved																																
240h	CAN_F0B1	FBC[31:0]																															
	Reset Value	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
244h	CAN_F0B2	FBC[31:0]																															
	Reset Value	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
248h	CAN_F1B1	FBC[31:0]																															
	Reset Value	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
24Ch	CAN_F1B2	FBC[31:0]																															
	Reset Value	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
. . .	. . .	Reserved																															
2A8h	CAN_F13B1	FBC[31:0]																															
	Reset Value	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
2ACh	CAN_F13B2	FBC[31:0]																															
	Reset Value	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

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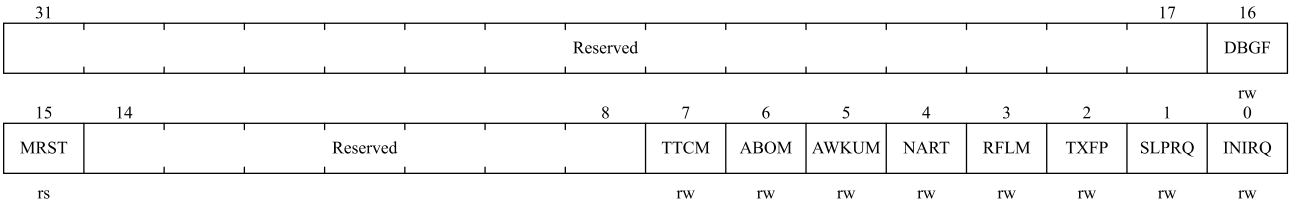
20.7.3 CAN control and status register

Abbreviations used in register descriptions, please refer to 1.1 section.

20.7.3.1 CAN master control register (CAN_MCTRL)

Address offset: 0x00

Reset value: 0x0001 0002



Bit Field	Name	Description
31:17	Reserved	Reserved, the reset value must be maintained.
16	DBGF	Debug freeze 0: During debugging, CAN works as usual. 1: Freeze the reception/transmission of CAN during debugging. The receiving FIFO can still be read, written and controlled normally. ***Notes**: DBG_CTRL.CAN_STOP bit must be set when CAN is frozen, please refer to 20.3.7: Debugging mode.*
15	MRST	CAN software master reset 0: This peripheral works normally; 1: enforce reset CAN, after which CAN enters sleep mode and CAN_RFFx.FFMP bit and CAN_MCTRL register are initialized to their reset values. After that, the hardware automatically clears this bit.
14:8	Reserved	Reserved, the reset value must be maintained.
7	TTCM	Time triggered communication mode 0: disable time triggered communication mode; 1: enable time trigger communication mode. ***Notes**: For more information about time-triggered communication mode, please refer to 20.4.2: Time-triggered communication mode.*
6	ABOM	Automatic bus-off management This bit determines the conditions under which the CAN hardware can exit the bus-off state. 0: The process of exiting the bus-off state is that after the software sets the CAN_MCTRL.INIRQ bit and then clears it, once the hardware detects 128 consecutive 11-bit recessive bits, it exits the bus-off state; 1: Once the hardware detects 128 consecutive 11-bit recessive bits, it will automatically exit the bus-off state. ***Notes**: For more information about bus-off status, please refer to 20.5.1: Error management.*
5	AWKUM	Automatic wake up mode

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Bit Field	Name	Description
		This bit determines whether CAN is awakened by hardware or software when it is in sleep mode. 0: The sleep mode is awakened by the software by clearing the CAN_MCTRL.SLPRQ bit; 1: Sleep mode is automatically awakened by hardware by detecting CAN messages. At the same time of wake-up, the hardware automatically clears the CAN_MSTS.SLPRQ and CAN_MSTS.SLPAK bits.
4	NART	No automatic retransmission 0: According to the CAN standard, when the CAN hardware fails to send a message, it will automatically retransmit it until it is successfully sent; 1: CAN message is only sent once, regardless of the sending result (success, error or arbitration loss).
3	RFLM	Receive FIFO locked mode. 0: the FIFO is not locked when receiving overflows, and when the message of the receiving FIFO is not read out, the next received message will overwrite the last message; 1: FIFO is locked when receiving overflow. When the message of receiving FIFO is not read out, the next received message will be discarded.
2	TXFP	Transmit FIFO priority When there are multiple messages waiting to be sent at the same time, this bit determines the sending order of these messages. 0: Priority is determined by the identifier of the message; 1: Priority is determined by the order in which requests are sent.
1	SLPRQ	Sleep mode request The software can request the CAN to enter the sleep mode by setting this bit, and once the current CAN activity (sending or receiving messages) ends, the CAN will enter the sleep mode. Clear by software to make CAN exit sleep mode. When the CAN_MCTRL.AWKUM bit is set and the SOF bit is detected in the CAN Rx signal, the hardware clears this bit. This bit is set after reset, that is, CAN is in sleep mode after reset.
0	INIRQ	Initialization request clear this bit by software can make CAN exit from initialization mode: when CAN leaves Initialization mode and entering normal mode, it needs to detect 11 consecutive recessive bits at the receiving pin, CAN will be synchronized and ready for receiving and sending data. To this end, the hardware correspondingly the CAN_MSTS.INIAK bit is cleared. Setting this bit by software enables CAN to enter initialization mode from normal operation mode: once the current CAN activity (sending or receiving) is over, the hardware sets the CAN_MSTS.INIAK bit and CAN enters initialization mode.

20.7.3.2 CAN master status register (CAN_MSTS)

Address offset: 0x04

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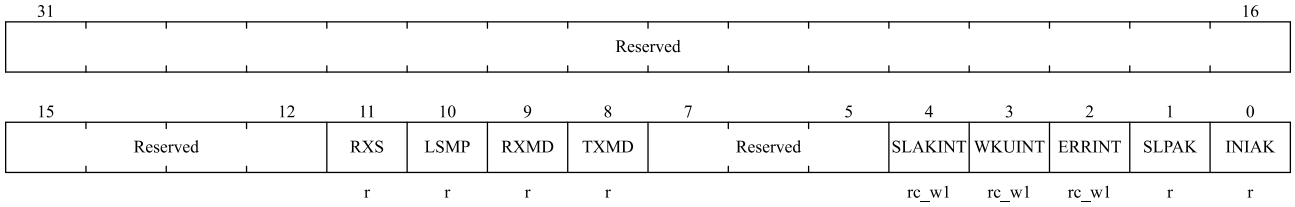
Reset value: 0x0000c02



Bit Field	Name	Description
31:12	Reserved	Reserved, the reset value must be maintained.
11	RXS	CAN Rx signal This bit reflects the actual level of the CAN receive pin (CAN_RX).
10	LSMP	Last sample point The last sampled value of the CAN receive pin (corresponding to the value of the current receive bit).
9	RXMD	Receive mode if this bit equals to 1 indicates CAN is currently the receiver.
8	TXMD	Transmit mode if this bit equals to 1 indicates CAN is currently the transmitter.
7:5	Reserved	Reserved, the reset value must be maintained.
4	SLAKINT	Sleep acknowledge interrupt When CAN_INTE.SLKITE=1, once CAN enters sleep mode, hardware will set this bit, and then the corresponding interrupt will be triggered. When this bit is set, if the CAN_INTE.SLKITE bit is set, a state change interrupt will be generated. Software can clear this bit, and hardware also clears this bit when CAN_MSTS.SLPAK bit is cleared. ***Notes**: When CAN_INTE.SLKITE=0, this bit should not be queried, but the CAN_MSTS.SLPAK bit should be queried to know the sleep state.*
3	WKUINT	Wakeup interrupt When CAN is in sleep state, once the start of frame bit (SOF) is detected, the hardware will set this bit; And if the CAN_INTE.WKUITE bit is set, a state change interrupt is generated. This bit is cleared by software.
2	ERRINT	Error interrupt When an error is detected, a bit of the CAN_ESTS register will be set, and if the corresponding interrupt enable bit of the CAN_INTE register is also set, the hardware will set this bit; If the CAN_INTE.ERRITE bit is set, a state change interrupt is generated. This bit is cleared by software.
1	SLPAK	Sleep acknowledge This bit is set by hardware, indicating that the software CAN module is in sleep mode. This bit is the confirmation of the software request to enter sleep mode (the CAN_MCTRL.SLPRQ bit is set). Hardware clears this bit when CAN exits sleep mode (CAN leaves Sleep mode

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Bit Field	Name	Description
		and entering normal mode,it needs to be synchronized with CAN bus). Synchronization with CAN bus here means that the hardware needs to detect 11 consecutive recessive bits on the RX pin of CAN. ***Notes**: clearing CAN_MCTRL.SLPRQ bit by software or hardware will start the process of exiting sleep mode. See the description of CAN_MCTRL.AWKUM bit for details of clearing CAN_MCTRL.SLPRQ bit.*
0	INIAK	Initialization acknowledge This bit is set by hardware, indicating that the software CAN module is in initialization mode. This bit is the confirmation of the software request to enter the initialization mode (the CAN_MCTRL.INIRQ bit is set). Hardware clears this bit when CAN exits initialization mode (CAN leaves Initialization mode and entering normal mode,it needs to be synchronized with CAN bus). Synchronization with CAN bus here means that the hardware needs to detect 11 consecutive recessive bits on the RX pin of CAN.

20.7.3.3 CAN transmit status register (CAN_TSTS)

Address offset: 0x08

Reset value: 0x1C00 0000

31	30	29	28	27	26	25	24	23	22	20	19	18	17	16
LOWM2	LOWM1	LOWM0	TMEM2	TMEM1	TMEM0	CODE		ABRQM2	Reserved		TERRM2	ALSTM2	TXOKM2	RQCPM2
r	r	r	r	r	r	r		rs			rc_w1	rc_w1	rc_w1	rc_w1

15	14	12	11	10	9	8	7	6	4	3	2	1	0
ABRQM1	Reserved		TERRM1	ALSTM1	TXOKM1	RQCPM1	ABRQM0	Reserved		TERRM0	ALSTM0	TXOKM0	RQCPM0
rs			rc_w1	rc_w1	rc_w1	rc_w1	rs			rc_w1	rc_w1	rc_w1	rc_w1

Bit Field	Name	Description
31	LOWM2	Lowest priority flag for mailbox 2 When multiple mailboxes are waiting to send messages, and the priority of mailbox 2 is the lowest, hardware sets this bit.
30	LOWM1	Lowest priority flag for mailbox 1 When multiple mailboxes are waiting to send messages, and the priority of mailbox 1 is the lowest, hardware sets this bit.
29	LOWM0	Lowest priority flag for mailbox 0 When multiple mailboxes are waiting to send messages, and the priority of mailbox 0 is the lowest, hardware sets this bit. ***Notes**: If there is only one mailbox waiting, CAN_TSTS.LOWM[2:0] is cleared*
28	TMEM2	Transmit mailbox 2 empty When there is no message waiting to be sent in mailbox 2, hardware sets this bit.
27	TMEM1	Transmit mailbox 1 empty When there is no message waiting to be sent in mailbox 1, hardware sets this bit.
26	TMEM0	Transmit mailbox 0 empty When there is no message waiting to be sent in mailbox 0, hardware sets this bit .
25:24	CODE[1:0]	Mailbox code

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Bit Field	Name	Description
		When at least one sending mailbox is empty, these two bits represent the next empty sending mailbox number. When all sending mailboxes are empty, these two bits represent the sending mailbox number with the lowest priority.
23	ABRQM2	Abort request for mailbox 2 Set this bit, software can stop the sending request of mailbox 2, and hardware clears this bit when the sending message of mailbox 2 is idle. If there is no message waiting to be sent in mailbox 2, it will have no effect to set this bit.
22:20	Reserved	Reserved, hardware force is 0.
19	TERRM2	Transmission error of mailbox 2 failed. When the mailbox 2 fails to send due to an error, set this bit.
18	ALSTM2	Arbitration lost for mailbox 2 When the mailbox 2 fails to send due to the loss of arbitration, set this bit.
17	TXOKM2	Transmission OK of mailbox 2 The hardware updates this bit after each sending attempt of mailbox 2: 0: The last sending attempt is not yet successful; 1: The last sending attempt was successful. When the sending request of mailbox 2 is successfully completed, hardware sets this bit. See Figure 20-7.
16	RQCPM2	Request completed mailbox 2 When the last request (send or abort) for mailbox 2 is completed, the hardware will set this bit. Writing '1' to this bit by software can clear it; When the hardware receives the send request, it can also clear this bit (the CAN_TMI2.TXRQ bit is set). When this bit is cleared, other sending status bits (CAN_TSTS.TXOKM2, CAN_TSTS.ALSTM2 and CAN_TSTS.TERRM2 bits) of mailbox 2 are also cleared.
15	ABRQM1	Abort request for mailbox 1 Set this bit, the software can stop the sending request of mailbox 1, and the hardware clears this bit when the sending message of mailbox 1 is idle. If there is no message waiting to be sent in mailbox 1, it will have no effect to set this bit.
14:12	Reserved	Reserved, the reset value must be maintained.
11	TERRM1	Transmission error of mailbox 1 When the mailbox 1 fails to send due to an error, set this bit.
10	ALSTM1	Arbitration lost for mailbox 1 When the mailbox 1 fails to send due to the loss of arbitration, set this bit
9	TXOKM1	Transmission OK of mailbox 1 The hardware updates this bit after each sending attempt of mailbox 1: 0: The last sending attempt is not yet successful; 1: The last sending attempt was successful. When the sending request of mailbox 1 is successfully completed, the hardware sets this bit. See Figure 20-7.
8	RQCPM1	Request completed mailbox 1

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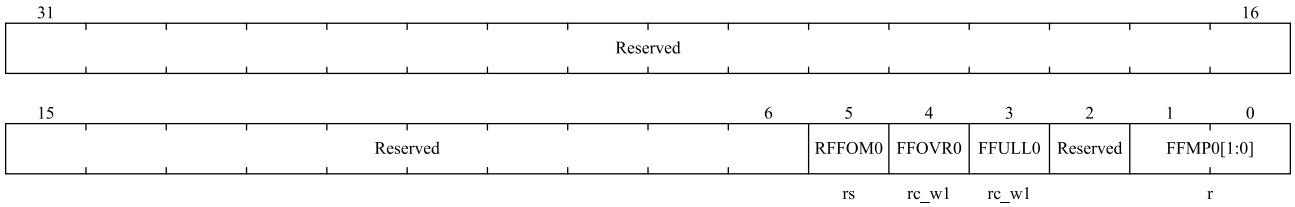
Bit Field	Name	Description
		When the last request (send or abort) for mailbox 1 is completed, the hardware sets this bit. Writing '1' to this bit by software can clear it; When the hardware receives the send request, it can also clears this bit (the CAN_TMI1.TXRQ bit is set). When this bit is cleared, other sending status bits (CAN_TSTS.TXOKM1, CAN_TSTS.ALSTM1 and CAN_TSTS.TERRM1 bits) of mailbox 1 are also cleared.
7	ABRQM0	Abort request for mailbox 0 The software can stop the sending request of mailbox 0 by setting this bit , and the hardware clears this bit when the sending message of mailbox 0 is idle. If there is no message waiting to be sent in mailbox 0, it will have no effect to set this bit.
6:4	Reserved	Reserved, the reset value must be maintained.
3	TERRM0	Transmission error of mailbox 0 When the mailbox 0 fails to send due to an error, set this bit.
2	ALSTM0	Arbitration lost for mailbox 0 When the mailbox 0 fails to send due to the loss of arbitration, set this bit
1	TXOKM0	Transmission OK of mailbox 0 The hardware updates this bit after each attempt to send mailbox 0: 0: The last send attempt is not yet successful; 1: The last sending attempt was successful. When the sending request of mailbox 0 is successfully completed, the hardware sets this bit. See Figure 20-7.
0	RQCPM0	Request completed mailbox 0 When the last request (send or abort) for mailbox 0 was completed, the hardware sets this bit. Writing '1' to this bit by software can clear it; When the hardware receives the send request, it can also clears this bit (the CAN_TMI0.TXRQ bit is set). When this bit is cleared, other sending status bits (CAN_TSTS.TXOKM0, CAN_TSTS.ALSTM0 and CAN_TSTS.TERRM0 bits) of mailbox 0 are also cleared.

20.7.3.4 CAN receive FIFO 0 register (CAN_RFF0)

Address offset: 0x0c

Reset value: 0x0000 0000



Bit Field	Name	Description
31:6	Reserved	Reserved, the reset value must be maintained.

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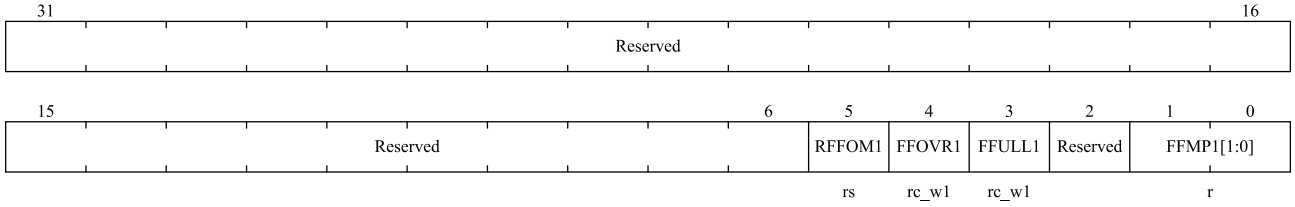
Bit Field	Name	Description
5	RFFOM0	Release FIFO 0 output mailbox. The software releases the output mailbox of the receive FIFO by setting this bit. If the receiving FIFO is empty, it will have no effect on setting this bit, that is, it will be meaningful to set this bit only when there is a message in the FIFO. If there are more than two messages in FIFO, because of the characteristics of FIFO, the software needs to release the output mailbox to access the second message. When the output mailbox is released, the hardware clears this bit.
4	FFOVR0	FIFO 0 overrun When FIFO 0 is full, a new message is received and the message meets the filtering conditions, the hardware sets this bit. This bit is cleared by software.
3	FFULL0	FIFO 0 full When there are 3 messages in FIFO 0, the hardware sets this bit'. This bit is cleared by software.
2	Reserved	Reserved, the reset value must be maintained.
1:0	FFMP0[1:0]	FIFO 0 message pending Number of FIFO messages 0 These two bits reflect the number of messages currently stored in the receiving FIFO 0. Every time a new message is stored in the receiving FIFO 0, the hardware adds 1 to the CAN_RFF0.FFMP0. Every time the software writes '1' to the CAN_RFF0.RFFOM0 bit to release the output mailbox, CAN_RFF0.FFMP0 is decremented by 1 until it is 0.

20.7.3.5 CAN receive FIFO 1 register (CAN_RFF1)

Address offset: 0x10

Reset value: 0x0000 0000



Bit Field	Name	Description
31:6	Reserved	Reserved, the reset value must be maintained.
5	RFFOM1	Release FIFO 1 output mailbox. The software releases the output mailbox of the receive FIFO by setting this bit. If the receiving FIFO is empty, it will have no effect on setting this bit, that is, it will be meaningful to set this bit only when there is a message in the FIFO. If there are more than two messages in FIFO, because of the characteristics of FIFO, the software needs to release the output mailbox to access the second message. When the output mailbox is released, the hardware clears this bit.
4	FFOVR1	FIFO 1 overrun When FIFO 1 is full, a new message is received and the message meets the filtering conditions, the hardware sets this bit. This bit is cleared by software.

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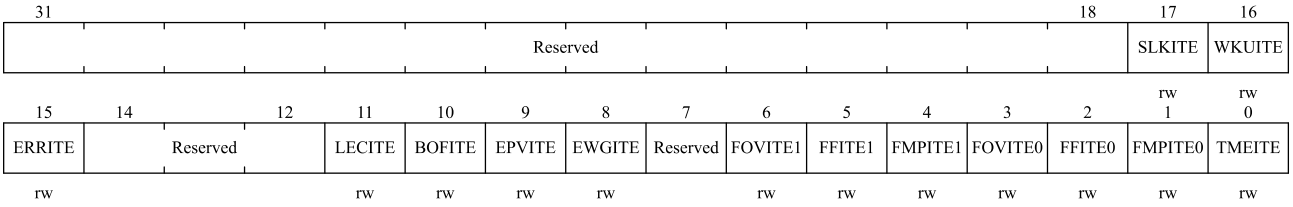
Bit Field	Name	Description
3	FFULL1	FIFO 1 full When there are 3 messages in FIFO 1, the hardware sets this bit. This bit is cleared by software.
2	Reserved	Reserved, the reset value must be maintained.
1:0	FFMP1[1:0]	FIFO 1 message pending Number of messages in FIFO 1 These two bits reflect the number of messages stored in the current receiving FIFO 1. Every time a new message is stored in receiving FIFO 1, the hardware adds 1 to CAN_RFF1.FFMP1. Every time the software releases the output mailbox by writing '1' to CAN_RFF1.RFFOM1 bit, CAN_RFF1.FFMP1 is decremented by 1 until it is 0.

20.7.3.6 CAN interrupt enable register (CAN_INTE)

Address offset: 0x14

Reset value: 0x0000 0000



Bit Field	Name	Description
31:18	Reserved	Reserved, the reset value must be maintained.
17	SLKITE	Sleep interrupt enable 0: when the CAN_MSTS.SLAKINT bit is set, no interrupt is generated; 1: when the CAN_MSTS.SLAKINT bit is set, an interrupt is generated.
16	WKUITE	Wakeup interrupt enable 0: when CAN_MSTS.WKUINT bit is set, no interrupt is generated; 1: when CAN_MSTS.WKUINT bit is set, an interrupt is generated.
15	ERRITE	Error interrupt enable 0: When there is an error registration in the CAN_ESTS register, no interrupt is generated; 1: When there is an error registration in the CAN_ESTS register, an interrupt is generated.
14:12	Reserved	Reserved, the reset value must be maintained.
11	LECITE	Last error code interrupt enable 0: When an error is detected, when the hardware sets CAN_ESTS.LEC[2:0], the CAN_MSTS.ERRINT bit is not set; 1: When an error is detected, when the hardware sets CAN_ESTS.LEC[2:0], the CAN_MSTS.ERRINT bit is set.
10	BOFITE	Bus-off interrupt enable 0: When CAN_ESTS.BOFFL bit is set, CAN_MSTS.ERRINT bit is not set; 1: When the CAN_ESTS.BOFFL bit is set, set the CAN_MSTS.ERRINT bit.

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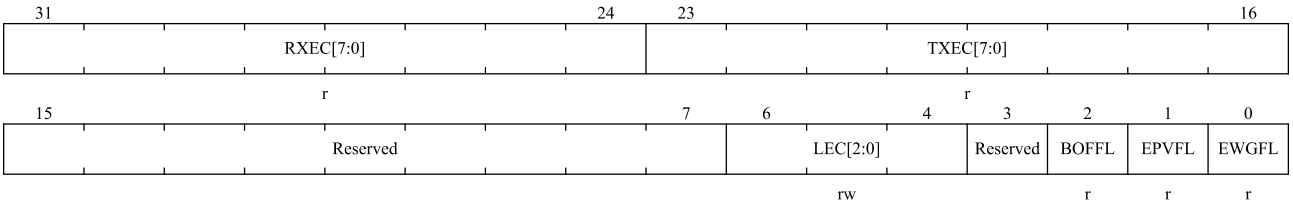
Bit Field	Name	Description
9	EPVITE	Error passive interrupt enable 0: when CAN_ESTS.EPVFL bit is set, CAN_MSTS.ERRINT bit is not set; 1: when CAN_ESTS.EPVFL bit is set, set the CAN_MSTS.ERRINT bit.
8	EWGITE	Error warning interrupt enable 0: When CAN_ESTS.EWGFL bit is set, CAN_MSTS.ERRINT bit is not set; 1: when the CAN_ESTS.EWGFL bit is set, set the CAN_MSTS.ERRINT bit.
7	Reserved	Reserved, the reset value must be maintained.
6	FOVITE1	FIFO 1 overflow interrupt enable 0: When CAN_RFF1.FFOVR bit is set, no interrupt is generated; 1: When CAN_RFF1.FFOVR bit is set, an interrupt is generated.
5	FFITE1	FIFO 1 full interrupt enable 0: When CAN_RFF1.FFULL bit is set, no interrupt is generated; 1: When CAN_RFF1.FFULL bit is set, an interrupt is generated.
4	FMPITE1	FIFO 1 message pending interrupt enable 0: When CAN_RFF1.FFMP[1:0] bits are non-0, no interrupt is generated; 1: When CAN_RFF1.FFMP[1:0] bits are not 0, an interrupt is generated.
3	FOVITE0	FIFO 0 overflow interrupt enable 0: When CAN_RFF0.FFOVR bit is set, no interrupt is generated; 1: When CAN_RFF0.FFOVR bit is set, an interrupt is generated.
2	FFITE0	FIFO 0 full interrupt enable 0: When CAN_RFF0.FFULL bit is set, no interrupt is generated; 1: When CAN_RFF0.FFULL bit is set, an interrupt is generated.
1	FMPITE0	FIFO 0 message pending interrupt enable 0: When CAN_RFF0.FFMP[1:0] bits are non-0, no interrupt is generated; 1: When CAN_RFF0.FFMP[1:0] bits are not 0, an interrupt is generated.
0	TMEITE	Transmit mailbox empty interrupt enable. 0: When CAN_TSTS.RQCPMx bit is set, no interrupt is generated; 1: When CAN_TSTS.RQCPMx bit is set, an interrupt is generated. ***Notes**: Please refer to 20.5 Section CAN interrupt.*

20.7.3.7 CAN error status register (CAN_ESTS)

Address offset: 0x18

Reset value: 0x0000 0000



Bit Field	Name	Description
31:24	RXEC[7:0]	Receive error counter This counter is implemented according to the receiving part of the fault definition

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Bit Field	Name	Description
		mechanism of CAN protocol. According to the standard of CAN, when receiving error, the counter is incremented by 1 or incremented by 8 according to the error condition; After each successful reception, the counter is decremented by 1, or when the value of the counter is greater than 127, its value is set to 120. When the value of this counter exceeds 127, CAN enters the error passive state.
23:16	TXEC[7:0]	Least significant byte of the 9-bit transmit error counter Similar to the above, this counter is implemented according to the sending part of the fault definition mechanism of CAN protocol.
15:7	Reserved	Reserved, the reset value must be maintained.
6:4	LEC[2:0]	The Last error code. When an error is detected on the CAN bus, the hardware is set according to the error situation. When the message is sent or received correctly, the hardware clears its value to '0'. The hardware does not use error code 7, and the software can set this value, so that the code update can be detected. 000: there is no error; 001: Bit padding error; 010: wrong Format (form); 011: Acknowledgment (ack) error; 100: recessive dislocation（CAN transmits recessive but detect dominant on the bus）; 101: dominant dislocation(CAN transmits dominant but detect recessive on the bus); 110: CRC error; 111: Set by software.
3	Reserved	Reserved, the reset value must be maintained.
2	BOFFL	Bus-off flag When going bus-off, hardware sets this bit. When the transmission error counter CAN_TSTS.TXEC overflows, that is, it is greater than 255, CAN goes bus-off. Please refer to 20.5.1 section.
1	EPVFL	Error passive flag When the number of errors reaches the threshold of error passivity, the hardware sets the bit. (The value of the receiving error counter or the sending error counter is > 127).
0	EWGFL	Error warning flag When the number of errors reaches the warning threshold, the hardware sets the bit. (The value of the receiving error counter or the sending error counter is ≥96).

20.7.3.8 CAN bit timing register (CAN_BTIM)

Address offset: 0x1C

Reset value: 0x0123 0000

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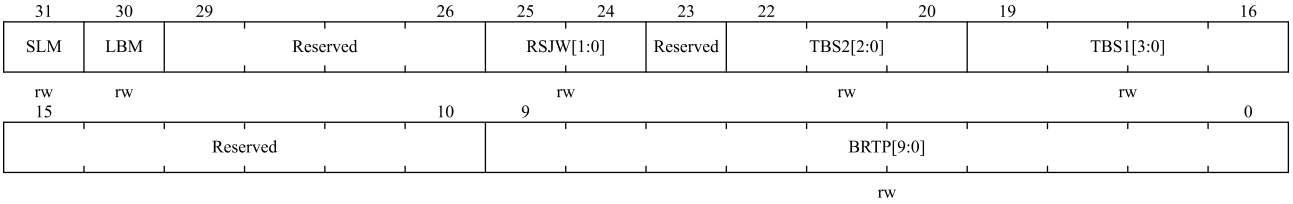
***Notes**: This register CAN only be accessed by software when CAN is in initialization mode.*



Bit Field	Name	Description
31	SLM	Silent mode（debug） 0: Normal state; 1: Silent mode.
30	LBM	Loop back mode（debug） 0: Loopback mode is prohibited; 1: Loopback mode is allowed.
29:26	Reserved	Reserved, the reset value must be maintained.
25:24	RSJW[1:0]	Resynchronization jump width For resynchronization, this bit field defines the upper limit of how many time units CAN be extended or shortened by CAN hardware in each bit. $t_{RJW} = t_{CAN}$ x (RSJW[1:0] + 1).
23	Reserved	Reserved, the reset value must be maintained.
22:20	TBS2[2:0]	Time segment 2 This bit field defines how many time units time period 2 occupies. $t_{BS2} = t_{CAN}$ x (TBS2[2:0] + 1).
19:16	TBS1[3:0]	Time segment 1 This bit field defines how many time units time period 1 occupies. $t_{BS1} = t_{CAN}$ x (TBS1[3:0] + 1) For details of bit time characteristics, please refer to section 20.4.7 secton: bit time characteristics.
15:10	Reserved	Reserved, the reset value must be maintained.
9:0	BRTP[9:0]	Baud rate prescaler This bit field defines the time length of the time unit (tq) t_q =(BRTP[9:0]+1) x t_{PCLK}

20.7.4 CAN mailbox register

This section describes the sending and receiving mailbox registers. For more information about register mapping, refer to 20.4.6 section: message storage.

20.7.4.1 Tx mailbox identifier register(CAN_TMIx)(x=0..2)

Address offset: 0x180, 0x190, 0x1A0

Reset value: 0xXXXX XXXX,X= undefined bit (except bit 0, TXRQ=0 at reset)

***Notes**: 1.This register is write-protected when the mailbox to which it belongs is waiting to be sent;*

2.This register implements the send request control function (bit 0)-the reset value is 0.

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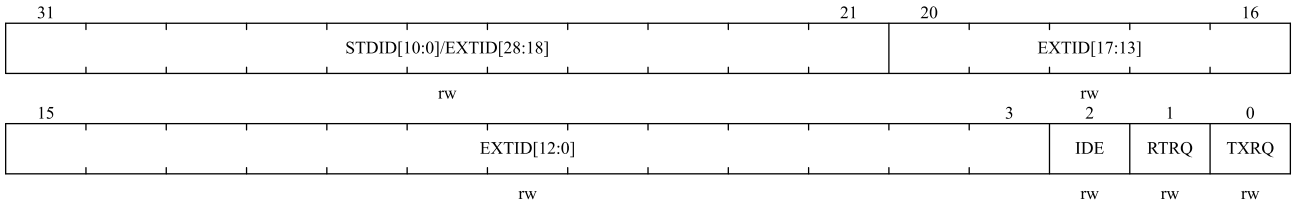


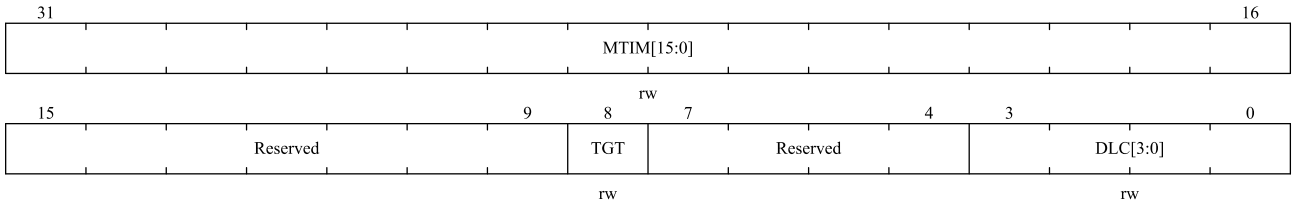
Bit Field	Name	Description
31:21	STDID[10:0]/EXTID[28:18]	Standard identifier or extended identifier Depending on the content of CAN_TMIx.IDE bits, these bits are either standard identifiers or high bytes of extended identity.
20:3	EXTID[17:0]	Extended identifier Low byte of extended identity.
2	IDE	Identifier extension. This bit determines the type of identifier used for sending messages in the mailbox. 0: Use standard identifier; 1: Use extended identifiers.
1	RTRQ	The Remote transmission request 0: data frame; 1: Remote frame.
0	TXRQ	Transmit mailbox request It is set by the software to request to send the data of the mailbox. When the data transmission is completed and the mailbox is empty, hardware clears it.

20.7.4.2 Tx mailbox data length and time stamp register (CAN_TMDTx)(x=0..2)

When the mailbox is not empty, all bits in this register are write-protected.

Address offset: 0x184, 0x194, 0x1A4

Reset value: undefined



Bit Field	Name	Description
31:16	MTIM[15:0]	Message time stamp This field contains the value of the 16-bit timer at the time of sending the message SOF.
15:9	Reserved	Reserved, the reset value must be maintained.
8	TGT	Transmit global time This bit is valid only when the CAN is in time-triggered communication mode, that is, the CAN_MCTRL.TTCM bit is set.

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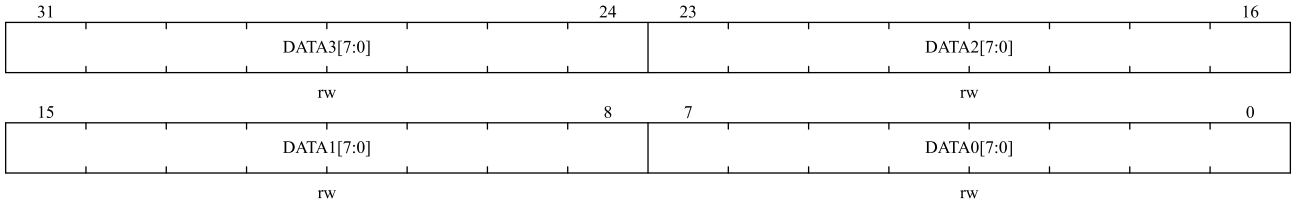
Bit Field	Name	Description
		0: Do not send the time stamp CAN_TMDTx.MTIM[15:0]; 1: send the time stamp CAN_TMDTx.MTIM[15:0]. In a message of length 8, the time stamp CAN_TMDTx.MTIM[15:0] is the last two bytes sent: CAN_TMDTx.MTIM[7:0] is the seventh byte and CAN_TMDTx.MTIM[15:8] is the eighth byte. They replace the data written in CAN_TMDHx[31:16] (CAN_TMDLx.DATA6[7:0] and CAN_TMDLx.DATA7[7:0]). In order to send the 2 bytes of the timestamp, DLC must be programmed to 8.
7:4	Reserved	Reserved, the reset value must be maintained.
3:0	DLC[3:0]	Data length code This field specifies the data length of the data message or the data length requested by the remote frame. One message contains 0 to 8 bytes of data, which is determined by DLC.

20.7.4.3 Tx mailbox low byte data register(CAN_TMDLx) (x=0..2)

When the mailbox is not empty, all bits in this register are write-protected.

Address offset: 0x188, 0x198, 0x1A8

Reset value: undefined



Bit Field	Name	Description
31:24	DATA3[7:0]	Data byte 3 Data byte 3 of the message.
23:16	DATA2[7:0]	Data byte 2 Data byte 2 of the message.
15:8	DATA1[7:0]	Data byte 1 Data byte 1 of the message.
7:0	DATA0[7:0]	Data byte 0 Data byte 0 of the message. *Notes:the message contains 0 to 8 bytes of data, starting from byte 0.*

20.7.4.4 Tx mailbox high byte data register(CAN_TMDHx) (x=0..2)

When the mailbox is not empty, all bits in this register are write protected.

Address offset: 0x18c, 0x19c, 0x1ac

Reset value: undefined

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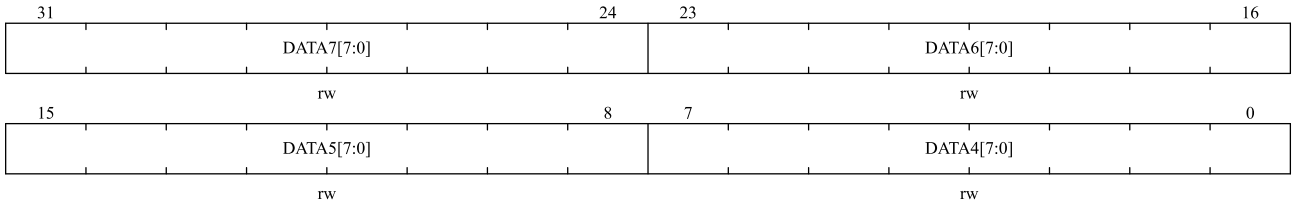


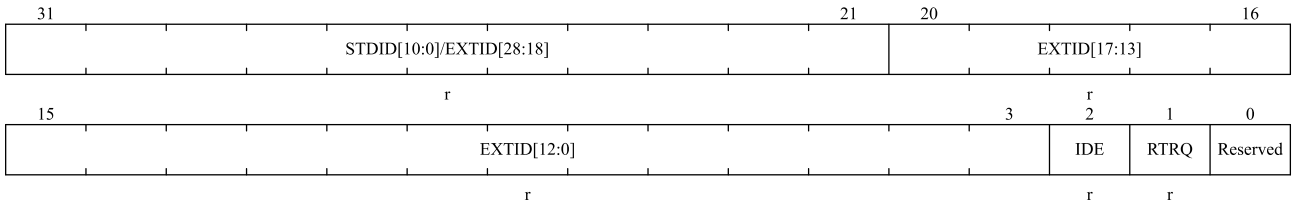
Bit Field	Name	Description
31:24	DATA7[7:0]	Data byte 7 Data byte 7 of the message. *Notes: If the CAN_MCTRL.TTCM bit is '1' and the CAN_TMDTx.TGT bit of this mailbox is also '1', then DATA7 and DATA6 will be replaced by TIME stamps.*
23:16	DATA6[7:0]	Data byte 6 Data byte 6 of the message.
15:8	DATA5[7:0]	Data byte 5 Data byte 5 of the message.
7:0	DATA4[7:0]	Data byte 4 Data byte 4 of the message.

20.7.4.5 Receive FIFO mailbox identifier register (CAN_RMIx) (x=0..1)

Address offset: 0x1B0, 0x1C0

Reset value: undefined

Notes: All receiving mailbox registers are read-only.



Bit Field	Name	Description
31:21	STDID[10:0]/EXTID[28:18]	Standard identifier or extended identifier Depending on the content of CAN_RMIx.IDE bits, these bits are either standard identifiers or high bytes of extended identity.
20:3	EXTID[17:0]	Extended identifier Low byte of extended identity.
2	IDE	Identifier extension. This bit determines the type of identifier used for sending messages in the mailbox. 0: Use standard identifier; 1: Use extended identifiers.
1	RTRQ	Remote transmission request 0: data frame; 1: Remote frame.

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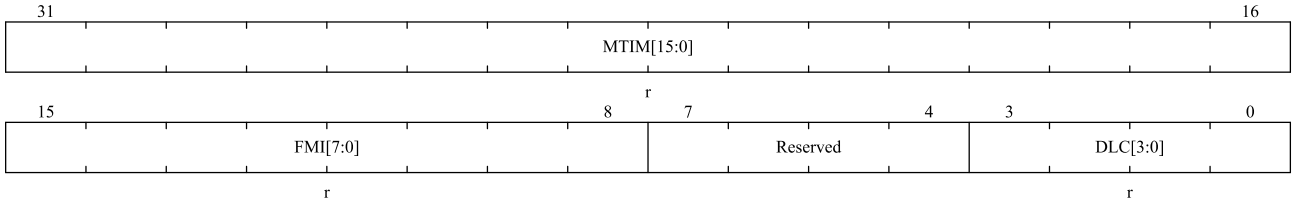
Bit Field	Name	Description
0	Reserved	Reserved, the reset value must be maintained.

20.7.4.6 Receive FIFO mailbox data length and time stamp register(CAN_RMDTx)(x=0..1)

Address offset: 0x1B4, 0x1C4

Reset value: undefined

***Notes**: All receiving mailbox registers are read-only.*



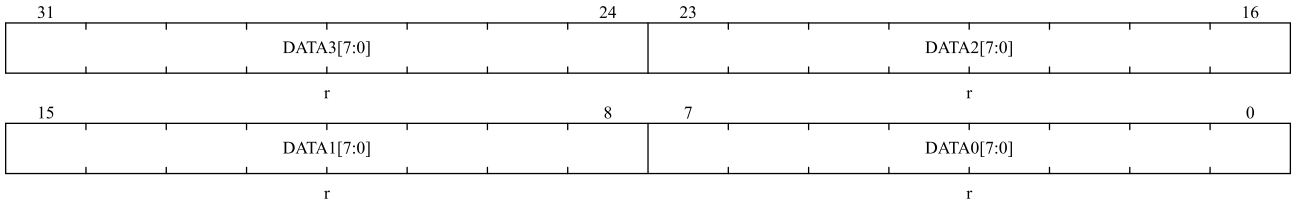
Bit Field	Name	Description
31:16	MTIM[15:0]	Message time stamp This field contains the value of the 16-bit timer at the time of sending the message SOF.
15:8	FMI[7:0]	Filter match index Here is the filter serial number of the information transfer stored in the mailbox. For details of identifier filtering, please refer to 20.4.5 section: Identifier filtering.
7:4	Reserved	Reserved, the reset value must be maintained.
3:0	DLC[3:0]	Data length code This field indicates the data length (0~8) of the received data frame. For remote frame requests, the data length DLC is always 0.

20.7.4.7 Receive FIFO mailbox low byte data register(CAN_RMDLx)(x=0..1)

Address offset: 0x1B8, 0x1C8

Reset value: undefined

***Notes**: All receiving mailbox registers are read-only.*



Bit Field	Name	Description
31:24	DATA3[7:0]	Data byte 3 Data byte 3 of the message.
23:16	DATA2[7:0]	Data byte 2 Data byte 2 of the message.
15:8	DATA1[7:0]	Data byte 1

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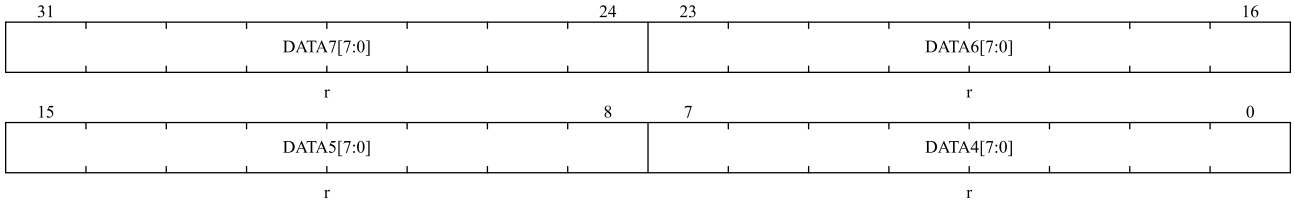
Bit Field	Name	Description
		Data byte 1 of the message.
7:0	DATA0[7:0]	Data byte 0 Data byte 0 of the message. Notes: the message contains 0 to 8 bytes of data, starting from byte 0.

20.7.4.8 Receive FIFO mailbox high byte data register(CAN_RMDHx) (x=0..1)

Address offset: 0x1BC, 0x1CC

Reset value: undefined

Note: All receiving mailbox registers are read-only.



Bit Field	Name	Description
31:24	DATA7[7:0]	Data byte 7 Data byte 7 of the message.
23:16	DATA6[7:0]	Data byte 6 Data byte 6 of the message.
15:8	DATA5[7:0]	Data byte 5 Data byte 5 of the message.
7:0	DATA4[7:0]	Data byte 4 Data byte 4 of the message.

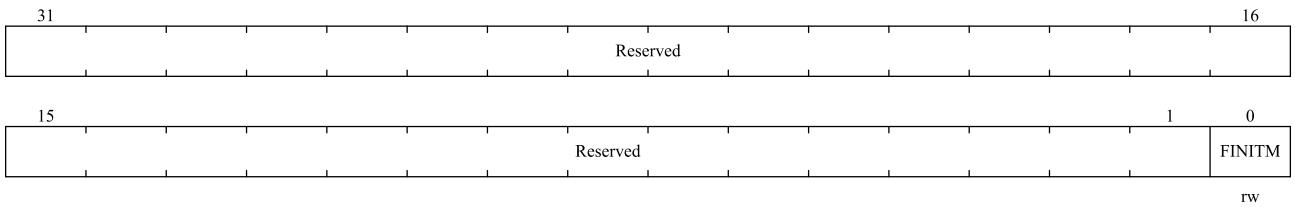
20.7.5 CAN filter register

20.7.5.1 CAN filter master control register (CAN_FMC)

Address offset: 0x200

Reset value: 0x2A1C 0E01

***Notes**: The unreserved bits of this register are completely controlled by software.*



Bit Field	Name	Description
31:1	Reserved	Reserved, the reset value must be maintained.
0	FINITM	Filter init mode

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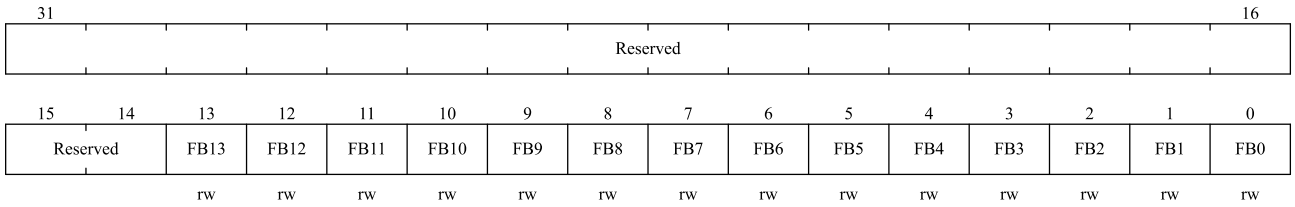
Bit Field	Name	Description
		Initialization mode settings for all filter groups. 0: The filter group works in normal mode; 1: The filter group works in initialization mode.

20.7.5.2 CAN filter mode register (CAN_FM1)

Address offset: 0x204

Reset value: 0x0000 0000

***Notes**: You can only write to this register when you set CAN_FMC.FINITM bit and put the filter in initialization mode.*



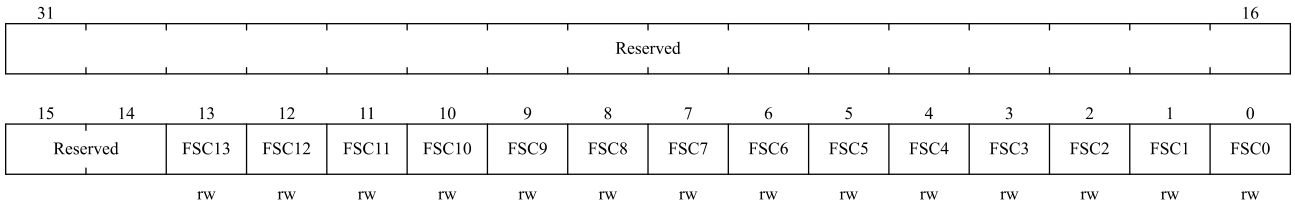
Bit Field	Name	Description
31:28	Reserved	Reserved, the reset value must be maintained.
13:0	FBx	Filter mode Working mode of filter group X 0: Two 32-bit registers of CAN_FiRx work in identifier mask mode; 1: Two 32-bit registers of CAN_FiRx work in identifier list mode.

20.7.5.3 CAN filter scale register (CAN_FS1)

Address offset: 0x20C

Reset value: 0x0000 0000

***Notes**: You can only write to this register when you set CAN_FMC.FINITM bit and put the filter in initialization mode.*



Bit Field	Name	Description
31:28	Reserved	Reserved, the reset value must be maintained.
13:0	FSCx	Filter scale configuration Bit width of filter group x (13~0). 0: The filter bit width is 2 16-bits; 1: The filter bit width is a single 32-bit.

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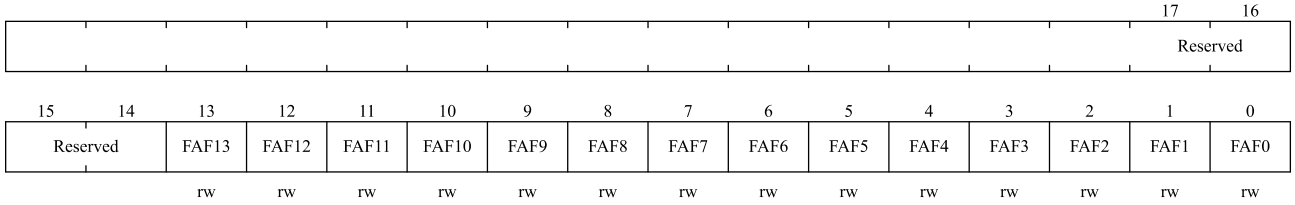
20.7.5.4 CAN filter FIFO assignment register (CAN_FFA1)

Address offset: 0x214

Reset value: 0x0000 0000

***Notes**: You can only write to this register when you set CAN_FMC.FINITM bit and put the filter in initialization mode.*

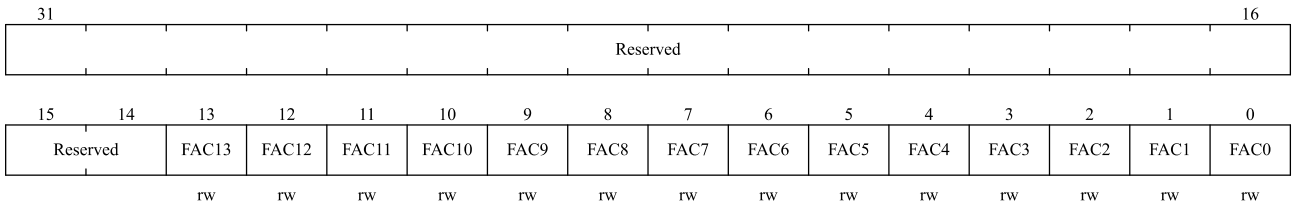


Bit Field	Name	Description
31:28	Reserved	Reserved, the reset value must be maintained.
13:0	FAFx	Filter FIFO assignment for filter x After the message is filtered by a certain filter, it will be stored in its associated FIFO. 0: the filter is associated to FIFO0; 1: the filter is associated to FIFO1.

20.7.5.5 CAN filter activation register (CAN_FA1)

Address offset: 0x21C

Reset value: 0x0000 0000



Bit Field	Name	Description
31:28	Reserved	Reserved, the reset value must be maintained.
13:0	FACx	Filter active The software sets '1' for someone to activate the corresponding filter. The corresponding filter register i(CAN_FiR[2:1]) can only be modified after the CAN_FA1.FACx bit is cleared or the CAN_FMC.FINITM bit is set. 0: The filter is disabled; 1: The filter is activated.

20.7.5.6 CAN filter i register x（CAN_FiRx）（i＝0..13;x=1..2）

Address offset: 0x240h, 0x31C

Reset value: undefined

***Notes**: 14 groups of filters: i = 0 ... 13. Each group of filters consists of two 32-bit registers, CAN_FiR[2:1].*

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Only when the corresponding CAN_FA1.FACx bit is cleared or the CAN_FMC.FINIT bit is set, the corresponding filter register can be modified.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
FBC31	FBC30	FBC29	FBC28	FBC27	FBC26	FBC25	FBC24	FBC23	FBC22	FBC21	FBC20	FBC19	FBC18	FBC17	FBC16
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FBC15	FBC14	FBC13	FBC12	FBC11	FBC10	FBC9	FBC8	FBC7	FBC6	FBC5	FBC4	FBC3	FBC2	FBC1	FBC0
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bit Field	Name	Description
31:0	FBC[31:0]	Filter bits Identifier pattern Each bit of the register corresponds to the level of the corresponding bit of the expected identifier. 0: the corresponding bit is expected to be dominant; 1: The corresponding bit is expected to be recessive. Mask bit pattern Each bit of the register indicates whether the corresponding identifier register bit must be consistent with the corresponding bit of the expected identifier. 0: Don't care, this bit is not used for comparison; 1: Must match, and the incoming identifier bit must be consistent with the identifier register bit corresponding to the filter.

***Notes**: According to the different settings of filter bit width and mode, the functions of the two registers in the filter bank are different. For the mapping of filters, function description and association of mask registers, see 20.4.5 Section: identifier filtering.*

Mask/identifier register in **mask mode** has the same definition as register bit in **identifier list mode**.

See for the address of the filter bank register Table 20-4.

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21 Serial Peripheral Interface/Inter-IC Sound (SPI/ I^2S)

21.1 Introduction

This module is about SPI/I2S. It works in SPI mode by default and users can choose to use I2S by setting the value of registers.

Serial peripheral interface (SPI) is able to work in master or slave mode, support full-duplex and simplex high-speed communication mode, and have hardware CRC calculation and configurable multi-master mode.

On-chip audio interface (I2S) is able to work in master and slave modes in simplex communication, and supports four audio standards: Philips I2S standard, MSB alignment standard, LSB alignment standard and PCM standard.

Both of them are synchronous serial interface communication protocols.

21.2 Main features

21.2.1 SPI features

- Full duplex mode and simplex synchronous mode.
- Support master mode, slave mode and multi-master mode.
- Supports 8-bit or 16-bit data frame format.
- Data bit sequence programmable.
- NSS management by hardware or software.
- Clock polarity and phase programmable.
- Sending and receiving support hardware CRC calculation and check.
- Supports DMA function.

21.2.2 I^2S features

- Simplex synchronous mode.
- Supports master mode and slave mode operation.
- Four audio standards are supported: Philips I^2S standard, MSB alignment standard, LSB alignment standard and PCM standard.
- The audio sampling frequency from 8kHz to 96kHz can be configured.
- Supports 16-bit, 24-bit or 32-bit data length and data frame format (configured according to requirements).
- Steady state clock polarity programmable.
- The data direction is always MSB first.
- Supports DMA function.

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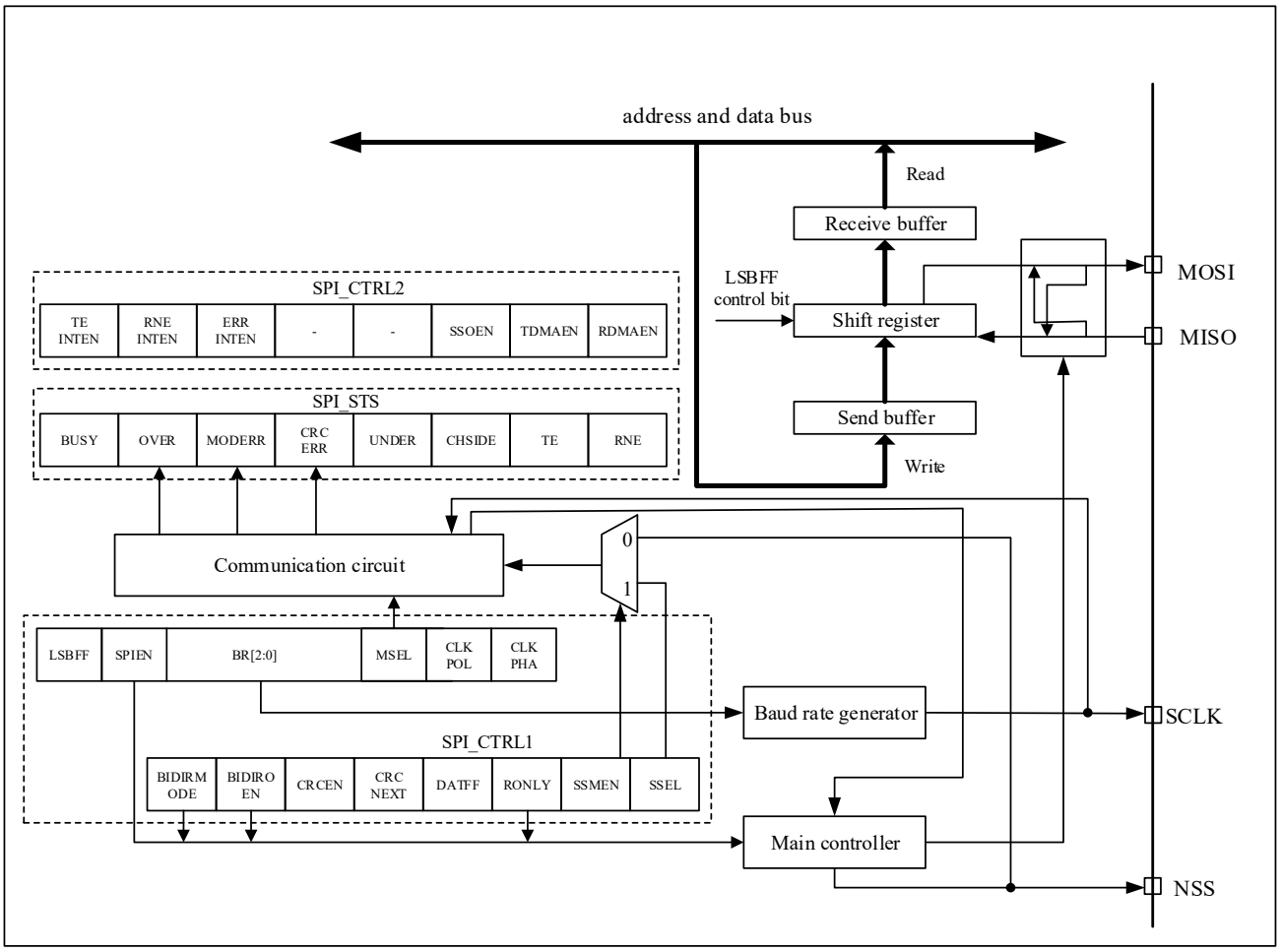
21.3 SPI function description

21.3.1 General description

Figure 21-1 SPI block diagram



To connected external devices, SPI has four pins, which are as follows:

- SCLK: serial clock pin. Serial clock signal is output from the SCLK pin of master device and input to SCLK pin of slave device.
- MISO: master input/slave output pin. Data is received from the MISO pin of master device and send by the MISO pin of slave device.
- MOSI: master output/slave input pin. Data is send by the MOSI pin of master device and received from the MOSI pin of slave device.
- NSS: chip select pin. There are two types of NSS pin, internal pin and external pin. If the internal pin detects a high level, SPI works in the master mode. Conversely, SPI works in the slave mode. Users can use a standard I/O pin of the master device to control the NSS pin of the slave device.

Software NSS mode

The software slave device management is enabled when SPI_CTRL1.SSMEN = 1.

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The NSS pin is not used in software NSS mode. In this mode the internal NSS signal level is driven by writing the SPI_CTRL1.SSEL bit (master mode SPI_CTRL1.SSEL = 1, slave mode SPI_CTRL1.SSEL = 0).

Hardware NSS mode

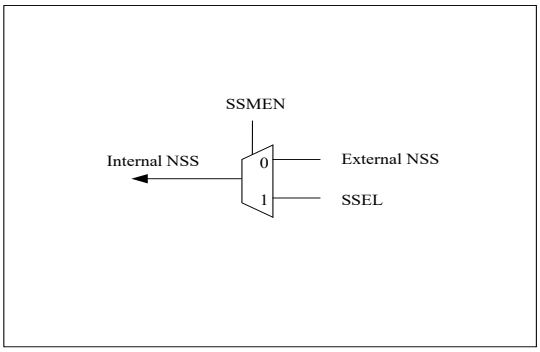
The software slave device management is disabled when SPI_CTRL1.SSMEN = 0.

NSS input mode: The NSS output of the master device is disabled (SPI_CTRL1.MSEL = 1, SPI_CTRL2.SSOEN = 0), allowing operation in multi-master mode. The master should connect NSS pin to the high level and the slave should connect NSS pin to the low level during the entire data frame transfer.

NSS output mode: NSS output of the master device is enable (SPI_CTRL1.MSEL = 1, SPI_CTRL2.SSOEN = 1). SPI as the master device must pull the NSS pin to low level, all device which connected to the master device and set to NSS hardware mode, will detect low level and enter the slave mode automatically. If the master device cannot pull the NSS pin to low level, device will enter the slave mode and generates the master mode failure error.

Note: The choice of software mode or hardware mode depends on whether NSS control is needed in the communication protocol. If not, you can choose the software mode, and release a GPIO pin for other purposes.

Figure 21-2 Selective management of hardware/software



The following figure is an example of the interconnection of single master and single slave devices

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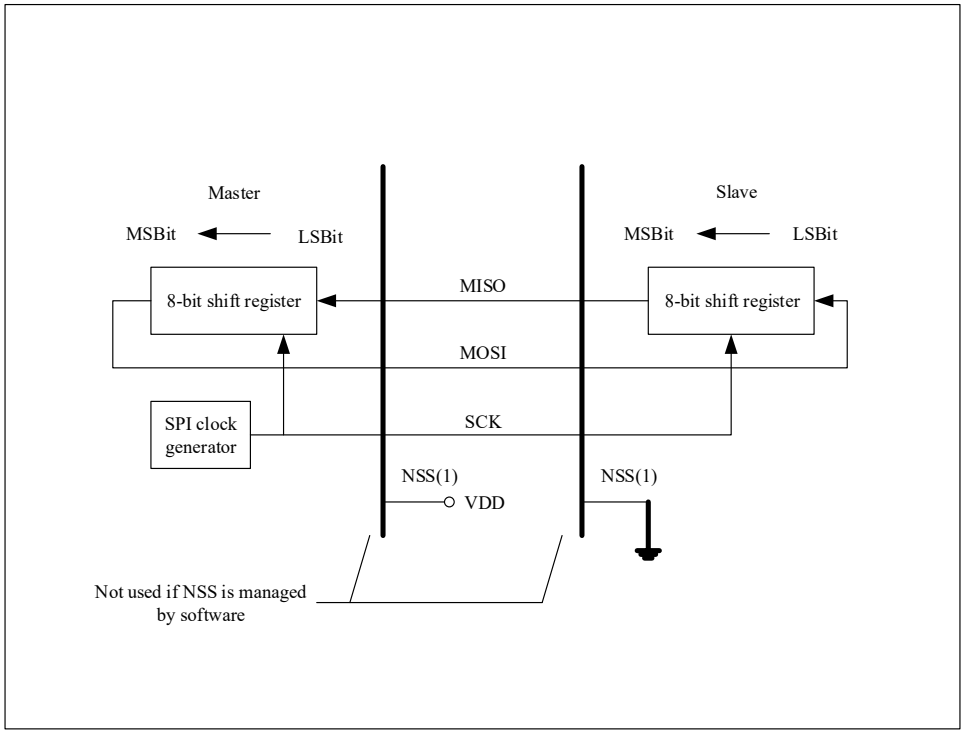
Figure 21-3 Master and slave applications



Note: NSS pin is set as input

SPI is a ring bus structure. The master device outputs a synchronous clock signal through the SCK pin, the MOSI pin of the master device is connected to the MOSI pin of the slave device, and the MISO pin of the master device is connected to the MISO pin of the slave device, so that data can be transferred between devices. Continuous data transfer between master and slave, sending data to slave through MOSI pin and slave sending data to master through MISO pin.

SPI timing mode

User can selects the clock edge of data capture by setting SPI_CTRL1.CLKPOL bit and SPI_CTRL1.CLKPHA bit.

- When CLKPOL = 0, CLKPHA = 0, the SCLK pin will keep low in idle state, and the data will be sampled at the first edge, which is rising edge.
- When CLKPOL = 0, CLKPHA = 1, the SCLK pin will keep low in idle state, and the data will be sampled at the second edge, which is falling edge.
- When CLKPOL = 1, CLKPHA = 0, the SCLK pin will keep high in idle state, and the data will be sampled at the first edge, which is falling edge.
- When CLKPOL = 1, CLKPHA = 1, the SCLK pin will keep high in idle state, and the data will be sampled at the second edge, which is rising edge.

Regardless of the timing mode used, the master and slave configuration must be the same.

Figure 21-4 is the combination timing of four CLKPHA and CLKPOL bits transmitted by SPI when the SPI_CTRL1.LSBFF = 0.

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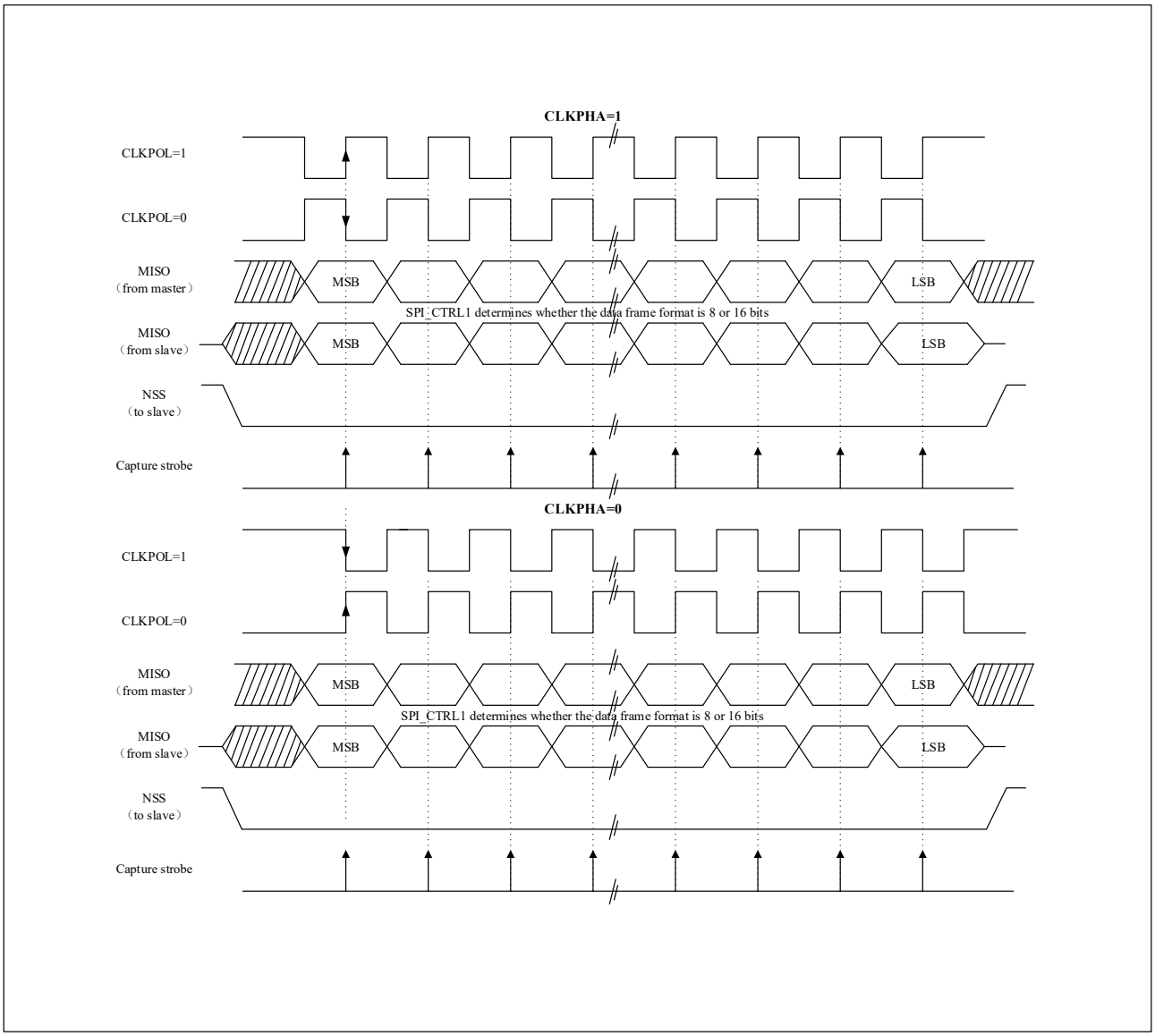
Figure 21-4 Data clock timing diagram



Data format

User can selects the data order by setting the SPI_CTRL1.LSBFF bit. When SPI_CTRL1.LSBFF = 0, SPI will send the high-order data (MSB) first; When SPI_CTRL1.LSBFF = 1, SPI will send low-order data (LSB) first.

User can selects the data frame by setting the SPI_CTRL1.DATFF bit.

21.3.2 SPI work mode

- **Master full duplex mode (SPI_CTRL1.MSEL = 1, SPI_CTRL1.BIDIRMODE = 0, SPI_CTRL1.RONLY = 0)**

After the first data is written to the SPI_DAT register, the transmission will start. When the first bit of the data is sent, the data bytes are loaded from the data register into the shift register in parallel, and then according to the configuration of the SPI_CTRL1.LSBFF bit, the data bits follow the MSB or LSB order is serially shifted to the MOSI pin. At the same time, the data received on the MISO pin is serially shifted into the shift register in the same order and then loaded into the SPI_DAT register in parallel. The software operation process is as follows:

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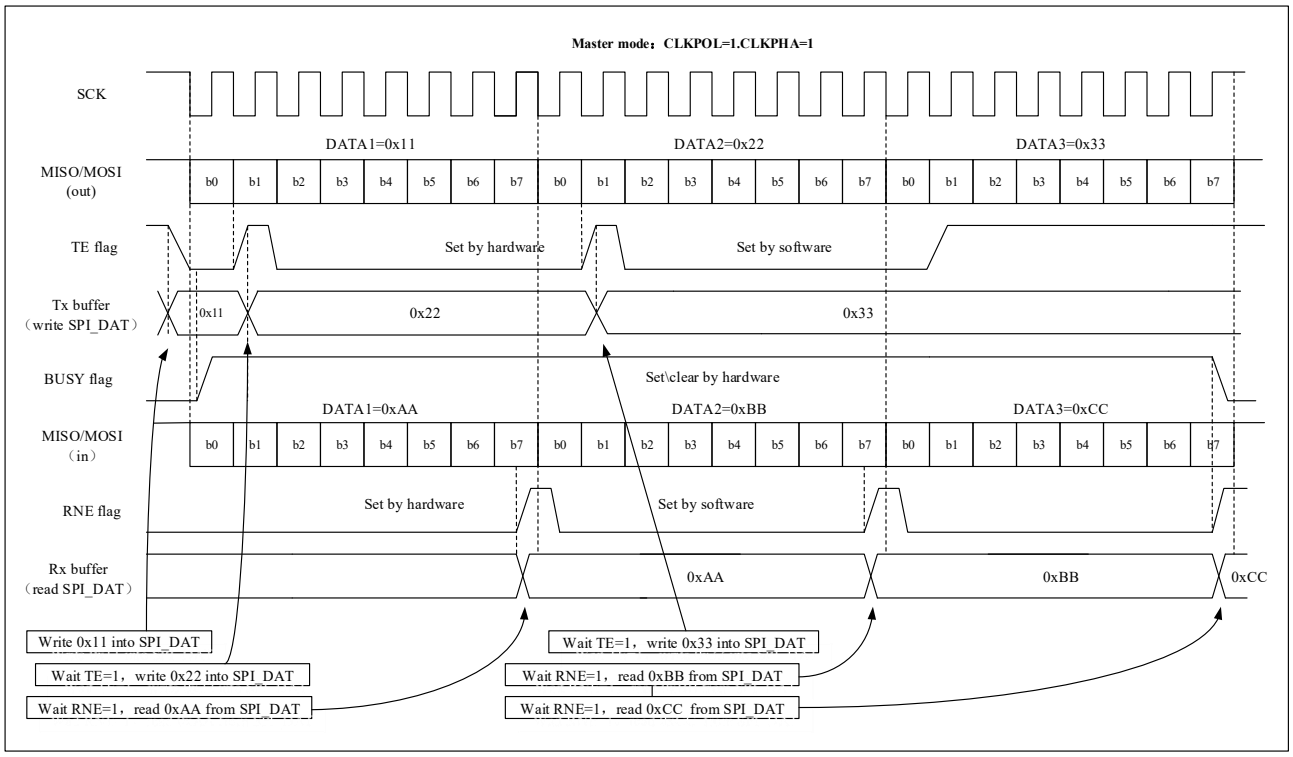
1. Set SPI_CTRL1.SPIEN = 1, Enable SPI module.
2. Write the first data to be sent into SPI_DAT register (this operation will clear SPI_STS.TE bit).
3. Wait for SPI_STS.TE bit to be set to '1', and write the second data to be sent into SPI_DAT. Wait for SPI_STS.RNE bit to be set to '1', read SPI_DAT to get the first received data, and the SPI_STS.RNE bit will be cleared by hardware while reading SPI_DAT. Repeat the above operation, sending subsequent data and receiving n-1 data at the same time;
4. Wait for SPI_STS.RNE bit to be set to '1' to receive the last data;
5. Wait for SPI_STS.TE to be set to '1', then wait for SPI_STS.BUSY bit to be cleared and turn off SPI module.

The process of data sending and data receiving can also be implemented in the interrupt handler generated by the rising edge of the SPI_STS.RNE or SPI_STS.TE flag.

Figure 21-5 Schematic diagram of the change of TE/RNE/BUSY when the host is continuously transmitting in full duplex mode



- **Master two-wire one-way send-only mode (SPI_CTRL1.MSEL = 1, SPI_CTRL1.BIDIRMODE = 0, SPI_CTRL1.RONLY = 0)**

Master two-wire one-way send-only mode is similar to master full-duplex mode. The difference is that this mode will not read the received data, so the SPI_STS.OVER bit will be set to '1', and the software will ignore it. The software operation process is as follows:

1. Set SPI_CTRL1.SPIEN = 1, Enable SPI module.
2. Write the first data to be sent into SPI_DAT register (this operation will clear SPI_STS.TE bit).
3. Wait for SPI_STS.TE bit to be set to '1', and write the second data to be sent into SPI_DAT. Repeat this operation to send subsequent data;

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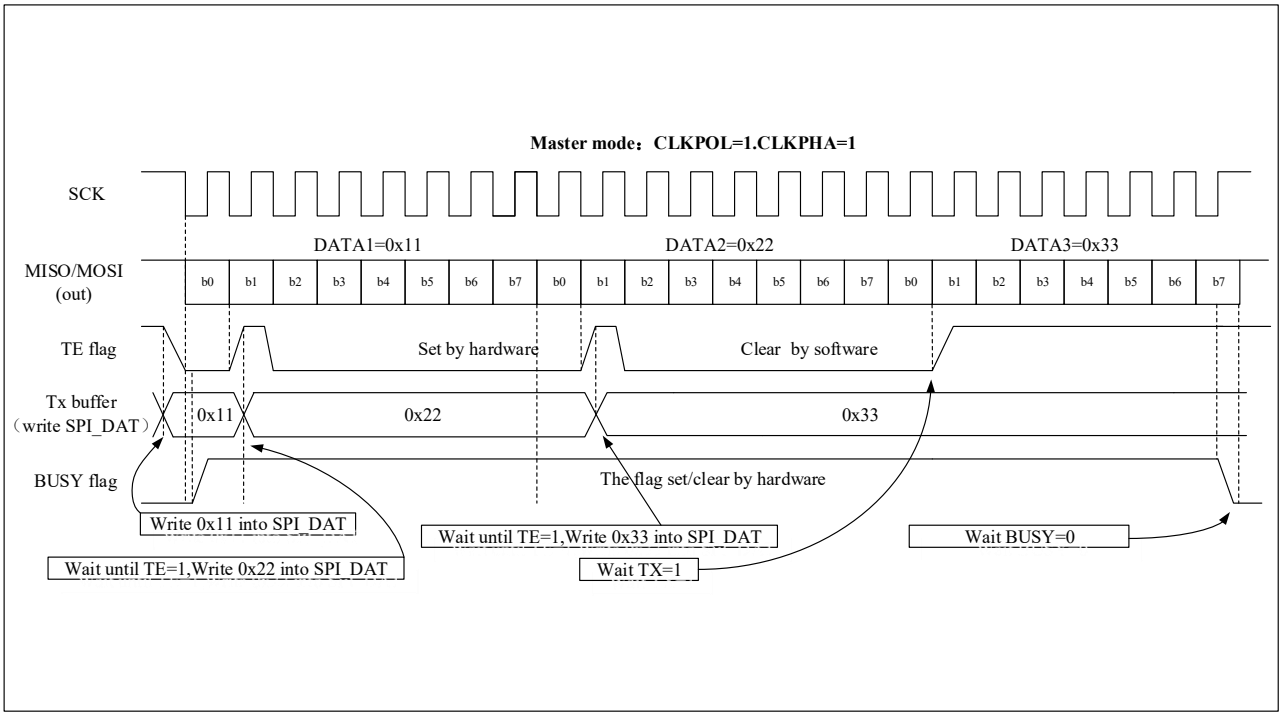
4. After writing the last data to SPI_DAT, wait for SPI_STS.TE bit to set '1'; then wait for SPI_STS.BUSY bit to be cleared to complete the transmission of all data.

The process of data sending can also be implemented in the interrupt handler generated by the rising edge of the TE flag.

Figure 21-6 Schematic diagram of TE/BUSY change when the host transmits continuously in one-way only mode



- **Master two-wire one-way receive-only mode (SPI_CTRL1.MSEL = 1, SPI_CTRL1.BIDIRMODE = 0, SPI_CTRL1.RONLY = 1)**

When SPI_CTRL1.SPIEN = 1, the receiving process starts. The data bits from the MISO pin are sequentially shifted into the shift register and then loaded into the SPI_DAT register(receive buffer) in parallel. The software operation process is as follows:

Enable the receive-only mode (SPI_CTRL1.RONLY = 1).

Enable SPI module, set SPI_CTRL1.SPIEN = 1: in master mode, SCLK clock signal is generated immediately, and serial data is continuously received before SPI is turned off (SPI_CTRL1.SPIEN = 0); in slave mode, serial data is continuously received when the SPI master device pulls low the NSS signal and generates SCLK clock.

Wait for SPI_STS.RNE bit to be set to '1', read the SPI_DAT register to get the received data, and the SPI_STS.RNE bit will be cleared by hardware while reading SPI_DAT register. Repeat this operation to receive all data.

The process of data receiving can also be implemented in the interrupt handler generated by the rising edge of the RNE flag (SPI_STS.RNE).

Figure 21-7 Schematic diagram of RNE change when continuous transmission occurs in receive-only mode (BIDIRMODE = 0 and

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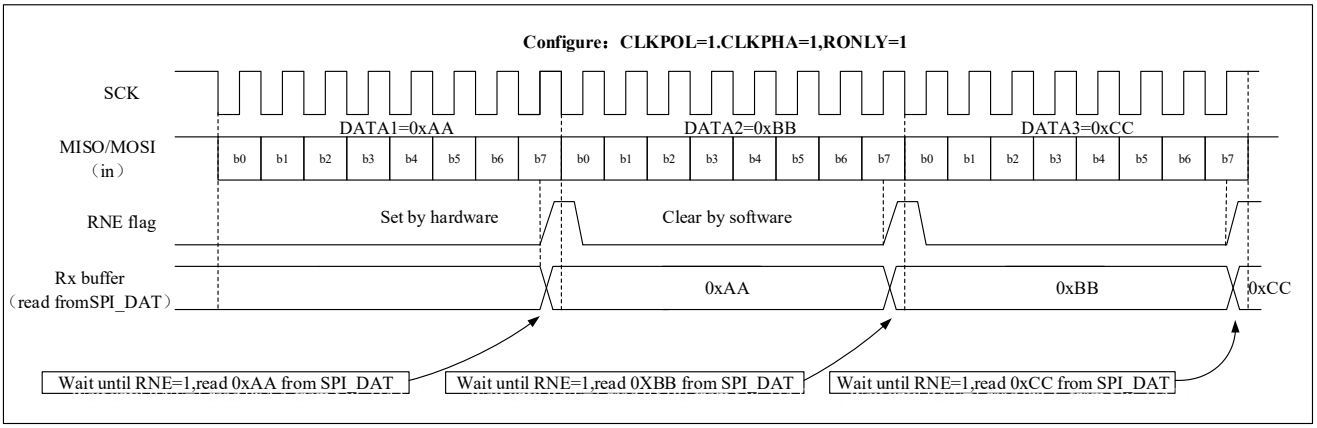
RONLY = 1)



- **Master one-wire bidirectional send mode (SPI_CTRL1.MSEL = 1, SPI_CTRL1.BIDIRMODE = 1, SPI_CTRL1.BIDIROEN = 1, SPI_CTRL1.RONLY = 0)**

After the data is written to the SPI_DAT register (send buffer), the transmission process starts. This mode does not receive data. At the same time as the first data bit is send, the data to be sent is loaded into the shift register in parallel, and then according to the configuration of the SPI_CTRL1.LSBFF bit, the SPI serially shifts the data bits to the MOSI pin in MSB or LSB order

The software operation flow of the master one-wire bidirectional send mode is the same as that of the send-only mode.

- **Master one-wire bidirectional receive mode (SPI_CTRL1.MSEL = 1, SPI_CTRL1.BIDIRMODE = 1, SPI_CTRL1.BIDIROEN = 0, SPI_CTRL1.RONLY = 0)**

When SPI_CTRL1.SPIEN = 1 , the receiving process starts. There is no data output in this mode, the received data bits are sequentially and serially shifted into the shift register, and then loaded into the SPI_DAT register (receive buffer) in parallel

The software operation flow of the master one-wire bidirectional receive mode is the same as that of the receive-only mode.

- **Slave full duplex mode (SPI_CTRL1.MSEL = 0, SPI_CTRL1.BIDIRMODE = 0, SPI_CTRL1.RONLY = 0)**

The data transfer process begins when the slave device receives the first clock edge. Before the master starts data transfer, software must ensure that the data to be send is written to the SPI_DAT register.

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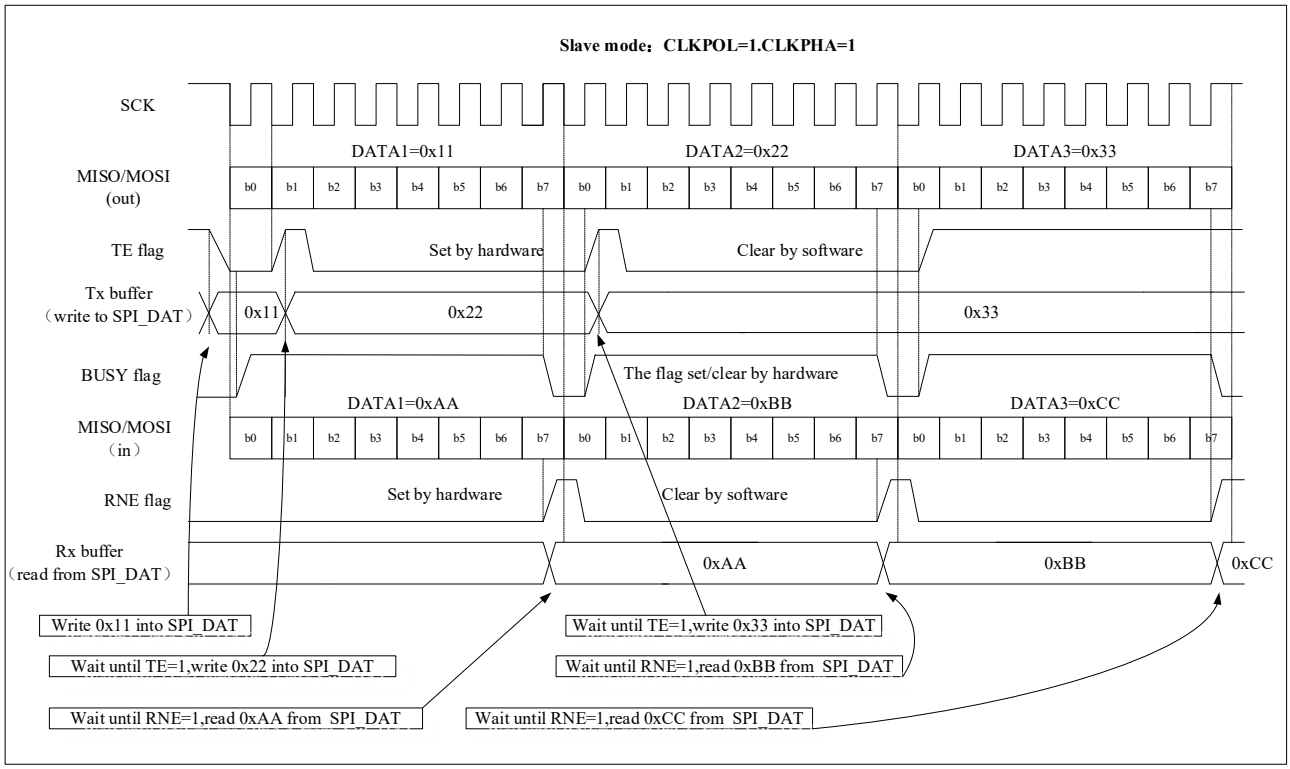
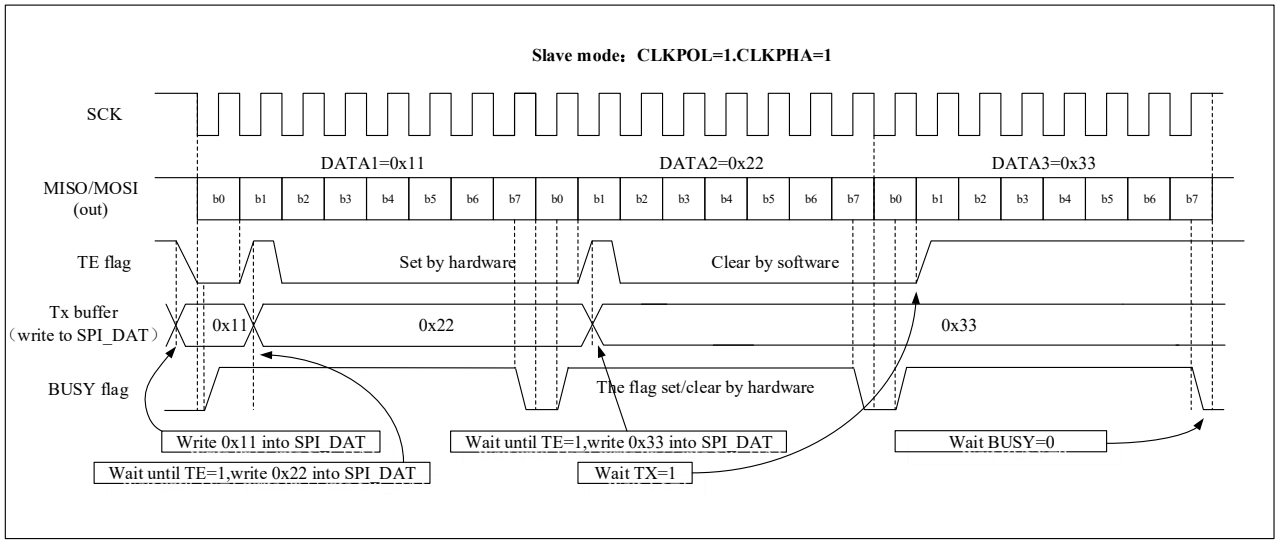
Figure 21-8 Schematic diagram of the change of TE/RNE/BUSY when the slave is continuously transmitting in full duplex mode



- **Slave two-wire one-way send-only mode (SPI_CTRL1.MSEL = 0, SPI_CTRL1.BIDIRMODE = 0 and SPI_CTRL1.RONLY = 0)**

Figure 21-9 Schematic diagram of TE/BUSY change during continuous transmission in slave unidirectional transmit-only mode



- **Slave two-wire one-way receive-only mode (SPI_CTRL1.MSEL = 0, SPI_CTRL1.BIDIRMODE = 0 and SPI_CTRL1.RONLY = 1)**

The data receiving process begins when the slave device receives the clock signal and the first data bit from the MOSI pin. The received data bits are sequentially and consecutively shifted serially into an shift register and then loaded into the SPI_DAT register (receive buffer) in parallel.

- **Slave one-wire bidirectional send mode (SPI_CTRL1.MSEL = 0, SPI_CTRL1.BIDIRMODE = 1 and**

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SPI_CTRL1.BIDIROEN = 1)

When the slave device receives the first edge of the clock signal, the sending process starts. No data is received in this mode, and the software must ensure that the data to be sent has been written in the SPI_DAT register before the SPI master device starts data transmission.

- **Slave one-wire bidirectional receive mode (SPI_CTRL1.MSEL = 0, SPI_CTRL1.BIDIRMODE = 1 and SPI_CTRL1.BIDIROEN = 0)**

Data receiving begins when the slave device receives the first clock edge and a data bit from the MOSI pin. There is no data output in this mode, the received data bits are sequentially and consecutively shifted serially into an shift register, and then loaded into the SPI_DAT register (receive buffer) in parallel.

Note: The software operation process of the slave can refer to the master.

SPI initialization process

1. The baud rate of serial clock is defined by the SPI_CTRL1.BR[2:0] bits (this step is ignored if it is working in slave mode).
2. Select SPI_CTRL1.CLKPOL bit and SPI_CTRL1.CLKPHA bit to define the phase relationship between data transmission and serial clock (see Figure 21-4).
3. Set SPI_CTRL1.DATFF bit to define 8-bit or 16-bit data frame format.
4. Configure the SPI_CTRL1.LSBFF bit to define the frame format.
5. Configure the NSS mode as described above for the NSS function.
6. Run mode is configured by SPI_CTRL1.MSEL bit, SPI_CTRL1.BIDIRMODE bit, SPI_CTRL1.BIDIROEN bit and SPI_CTRL1.RONLY bit.
7. Set the SPI_CTRL1.SPIEN = 1 to enable SPI.

Basic send and receive process

When SPI sends a data frame, it first loads the data frame from the data buffer into the shift register, and then starts to send the loaded data. When the data is transferred from the send buffer to the shift register, the send buffer empty flag is set (SPI_STS.TE = 1), and the next data can be loaded into the send buffer; if the TEINTEN bit is set (SPI_CTRL2.TEINTEN = 1), an interrupt will be generated; writing data to the SPI_DAT register will clear the SPI_STS.TE bit.

At the last edge of the sampling clock, when the data is transferred from the shift register to the receive buffer, the receive buffer non-empty flag is set (SPI_STS.RNE = 1), at this time the data is ready and can be read from the SPI_DAT register; if the receive buffer non-empty interrupt is enabled (SPI_CTRL2.RNEINTEN = 1), an interrupt will be generated; the SPI_STS.RNE bit can be cleared by reading the SPI_DAT register data.

In master mode, the sending process starts when data is written to the send buffer. If the next data has been written into the SPI_DAT register before the current data frame sending is completed, the continuous sending function can be achieved.

In slave mode, the NSS pin is low, and when the first clock edge arrives, the transmission process begins. In order to avoid accidental data transmission, software must write data to the transmit buffer before data transmission (it is recommended to enable the SPI module before the host sends the clock).

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In some configurations, when the last data is sent, the BUSY flag (SPI_STS.BUSY) can be used to wait for the end of the data sending.

Continuous and discontinuous transmission.

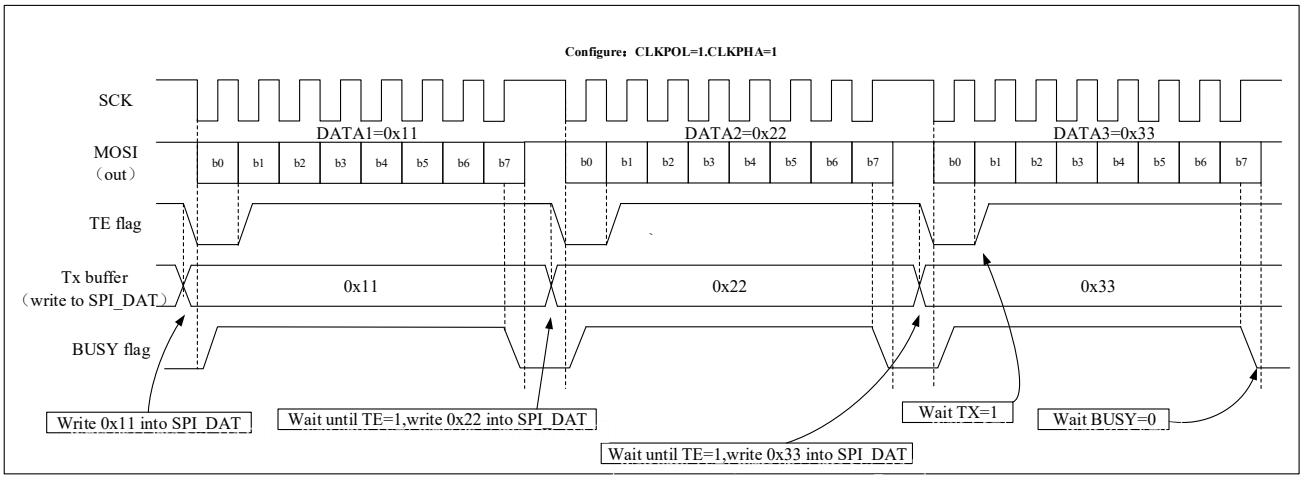
When sending data in master mode, if the software is fast enough to detect each TE (SPI_STS.TE) rising edge (or TE interrupt), and the data is written to the SPI_DAT register immediately before the end of the ongoing transmission. At this time, the SPI clock remains continuous between the transmission of data items, and the SPI_STS.BUSY bit will not be cleared, continuous communication can be achieved.

If the software is not fast enough, it will result in discontinuous communication; in this case, the SPI_STS.BUSY bit is cleared between the transmission of each data items (see Figure 21-10 below).

In master receive-only mode (SPI_CTRL1.RONLY = 1), communication is always continuous and the BUSY flag (SPI_STS.BUSY) is always high.

In slave mode, the continuity of communication is determined by the SPI master device. However, even if the communication is continuous, the BUSY flag (SPI_STS.BUSY) will be low for at least one SPI clock cycle between each data item (see Figure 21-9).

Figure 21-10 Schematic diagram of TE/BUSY change when BIDIRMODE = 0 and RONLY = 0 are transmitted discontinuously.



21.3.3 Status flag

The SPI_STS register has 3 flag bits to monitor the status of the SPI:

Send buffer empty flag bit (TE)

When the send buffer is empty, the TE flag (SPI_STS.TE) is set to 1, which means that new data can be written into the SPI_DAT register. When the send buffer is not empty, the hardware will clear this flag to 0.

Receive buffer non-empty flag bit (RNE)

When the receive buffer is not empty, the RNE flag (SPI_STS.RNE) is set to 1, so the user knows that there is data in the receive buffer. After reading the SPI_DAT register, the hardware will set this flag to 0.

BUSY flag bit (BUSY)

When the transmission starts, the hardware sets the BUSY flag (SPI_STS.BUSY) to 1, and after the transmission ends, the hardware sets the BUSY flag to 0.

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Only when the device is in the master one-wire bidirectional receive mode, the BUSY flag (SPI_STS.BUSY) will be set to 0 when the communication is in progress.

The BUSY flag (SPI_STS.BUSY) will be cleared to 0 in the following cases:

- End of transmission (except for continuous communication in master mode);
- Turn off the SPI module (SPI_CTRL1.SPIEN = 0);
- The master mode error occurs (SPI_STS.MODERR = 1)

When the communication is discontinuous: the BUSY flag (SPI_STS.BUSY) is cleared to '0' between the transmission of each data item.

When communication is continuous: in master mode, the BUSY flag (SPI_STS.BUSY) remains high during the entire transfer process; In slave mode, the BUSY flag (SPI_STS.BUSY) will be low for 1 SPI clock cycle between each data item transfer. So do not use the BUSY flag to handle the sending and receiving of each data item.

21.3.4 Disabling the SPI

In order to turn off the SPI module, different operation modes require different operation steps:

Master or slave full duplex mode

1. Wait for the RNE flag (SPI_STS.RNE) to be set to 1 and the last byte to be received;
2. Wait for the TE flag (SPI_STS.TE) to be set to 1;
3. Wait for the BUSY flag (SPI_STS.BUSY) to be cleared to 0;
4. Turn off the SPI module (SPI_CTRL1.SPIEN = 0).

Two-wire one-way send-only mode or one-wire bidirectional send mode for master or slave

1. After writing the last byte to the SPI_DAT register, wait for the TE flag (SPI_STS.TE) to be set to 1;
2. Wait for the BUSY flag (SPI_STS.BUSY) to be cleared to 0;
3. Turn off the SPI module (SPI_CTRL1.SPIEN = 0).

Two-wire one-way receive-only mode or one-wire bidirectional receive mode for master

1. Wait for the penultimate RNE (SPI_STS.RNE) to be set to 1;
2. Before closing the SPI module (SPI_CTRL1.SPIEN = 0), wait for 1 SPI clock cycle (using software delay);
3. Wait for the last RNE (SPI_STS.RNE) to be set before entering shutdown mode (or turning off the SPI module clock).

Two-wire one-way receive-only mode or one-wire bidirectional receive mode for slave

1. The SPI module can be turned off at any time (SPI_CTRL1.SPIEN = 0), and after the current transfer is over, the SPI module will be turned off;
2. If you want to enter the shutdown mode, you must wait for the BUSY flag (SPI_STS.BUSY) to be set to 0 before entering the shutdown mode (or turn off the SPI module clock).

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21.3.5 SPI communication using DMA

Users can choose DMA for SPI data transfer, the application program can be released, and the system efficiency can be greatly improved.

When the send buffer DMA is enabled (SPI_CTRL2.TDMAEN = 1), each time the TE flag (SPI_STS.TE) bit is 1, a DMA request will be generated, and the DMA will automatically write the data to the SPI_DAT register, which will clear the TE flag (SPI_STS.TE) bit. When the receive buffer DMA is enabled (SPI_CTRL2.RDMAEN = 1), each time the RNE flag (SPI_STS.RNE) bit is set to 1, a DMA request will be generated, and the DMA will automatically read the SPI_DAT register, which will clear the RNE flag (SPI_STS.RNE) bit.

When the SPI is only used for sending data, only the send DMA channel of the SPI needs to be enabled (SPI_CTRL2.TDMAEN = 1).

When the SPI is only used for receiving data, only the receive DMA channel of the SPI needs to be enabled (SPI_CTRL2.RDMAEN = 1).

In send mode, after DMA has sent all the data to be sent (DMA_INTSTS.TXCF = 1), BUSY flag (SPI_STS.BUSY) can monitor to confirm whether SPI communication is over, which can avoid destroying the transmission of the last data when the SPI is turned off or enters the shutdown mode. Therefore, the software needs to wait for the TE flag (SPI_STS.TE) bit to be set to 1, and wait for the BUSY flag (SPI_STS.BUSY) bit to be set to 0.

Figure 21-11 Transmission using DMA

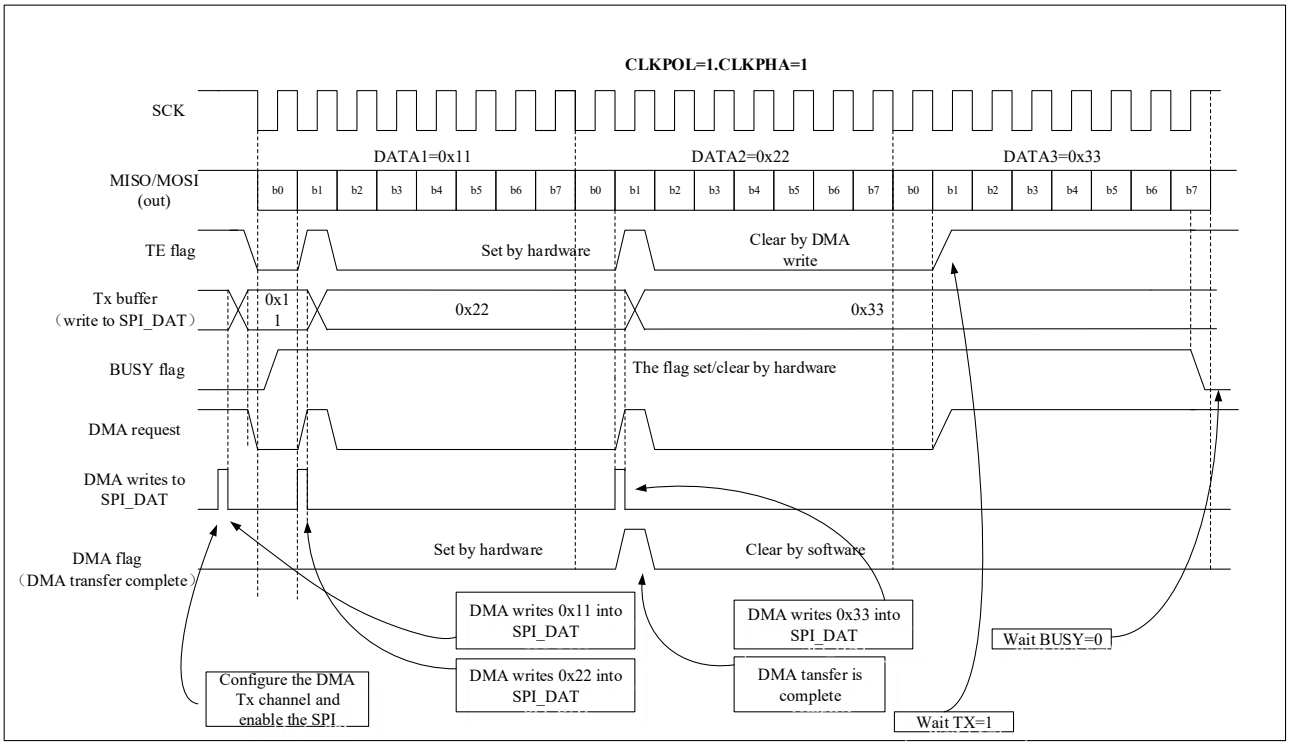

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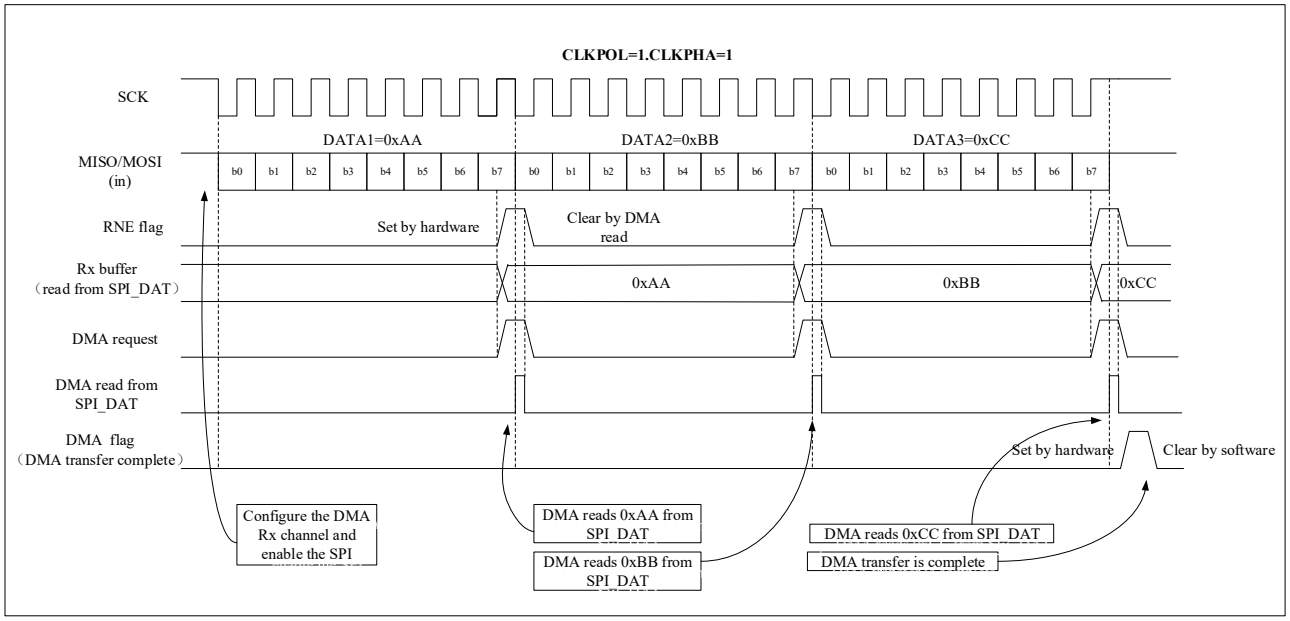
Figure 21-12 Reception using DMA



21.3.6 CRC calculation

SPI contains two independent CRC calculators for data sending and data receiving to ensure the correctness of data transmission. According to the sending and receiving data frame format, CRC adopts different calculation methods, the 8-bit data frame format adopts CRC8, and the 16-bit data frame format adopts CRC16. The polynomial used in the SPI CRC calculation is set by the SPI_CRCPOLY register, and the user enables the CRC calculation by setting the SPI_CTRL1.CRCEN = 1.

In send mode, after the last data is written into the send buffer, set the SPI_CTRL1.CRCNEXT = 1, which indicates that the hardware will start sending the CRC value (SPI_CRCTDAT value) after sending the data. When the CRC is sent, the CRC calculation will stop.

In receive mode, after the penultimate data frame is received, set the SPI_CTRL1.CRCNEXT = 1. The received CRC and SPI_CRCRDAT values are compared, if they are different, the SPI_STS.CRCERR bit is set to 1. If the SPI_CTRL2.ERRINTEN bit is set to 1, an interrupt will be generated.

In order to keep the synchronization of the next CRC calculation result of the master-slave device, the user should clear the CRC value of the master-slave device. Setting the SPI_CTRL1.CRCEN bit resets the SPI_CRCRDAT and SPI_CRCTDAT registers. Take the following steps in order: SPI_CTRL1.SPIEN = 0; SPI_CTRL1.CRCEN = 0; SPI_CTRL1.CRCEN = 1; SPI_CTRL1.SPIEN = 1.

Most importantly, when the SPI is configured in slave mode and CRC is enabled, as long as there is a clock pulse on SCLK pin, the CRC calculation will still be performed even if the NSS pin is high. This situation is common when the master device communicates with multiple slave devices alternately, so it is necessary to avoid CRC misoperation.

When the SPI hardware CRC check is enabled (SPI_CTRL1.CRCEN = 1) and the DMA is enabled, the hardware automatically completes the sending and receiving of CRC bytes when the communication ends.

21.3.7 Error flag

Master mode failure error (MODERR)

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The following two conditions will cause the master mode failure error:

- NSS pin hardware management mode, the master device NSS pin is pulled low;
- NSS pin software management mode, the SPI_CTRL1.SSEL bit is set to 0.

When a master mode failure error occurs, the SPI_STS.MODERR bit is set to 1. An interrupt is generated if the user enables the corresponding interrupt (SPI_CTRL2.ERRINTEN = 1). The SPI_CTRL1.SPIEN bit and SPI_CTRL1.MSEL bit will be write protected and both are cleared by hardware. SPI is turned off and forced into slave mode

Software performs a read or write operation to the SPI_STS register, and then writes to the SPI_CTRL1 register to clear the SPI_STS.MODERR bit (in multi-master mode, the master's NSS pin must be pulled high first).

Normally, the SPI_STS.MODERR bit of the slave cannot be set to 1. However, in a multi-master configuration, the slave's SPI_STS.MODERR bit may be set to 1. In this case, the SPI_STS.MODERR bit indicates that there is a multi-master collision. The interrupt routine can perform a reset or return to the default state to recover from an error state.

Overflow error (OVER)

When the SPI_STS.RNE bit is set to 1, but there is still data sent into the receive buffer, an overflow error will occur. At this time, the overflow flag SPI_STS.OVER bit is set to 1. An interrupt is generated if the user enables the corresponding interrupt (SPI_CTRL2.ERRINTEN = 1). All received data is lost, and the SPI_DAT register retains only previously unread data.

Read the SPI_DAT register and the SPI_STS register in turn to clear the SPI_STS.OVER bit.

CRC error (CRCERR)

The CRC error flag is used to check the validity of the received data. A CRC error occurs when the received CRC value does not match the SPI_CRCRDAT value. At this time, the SPI_STS.CRCERR flag bit is set to '1', and an interrupt will be generated if the user enables the corresponding interrupt (SPI_CTRL2.ERRINTEN = 1).

21.3.8 SPI interrupt

Table 21-1 SPI interrupt request

Interrupt event	Event flag bit	Enable control bit
Send buffer empty flag	TE	TEINTEN
Receive buffer non empty flag	RNE	RNEINTEN
Master mode failure event	MODERR	ERRINTEN
Overflow error	OVER	
CRC error flag	CRCERR	

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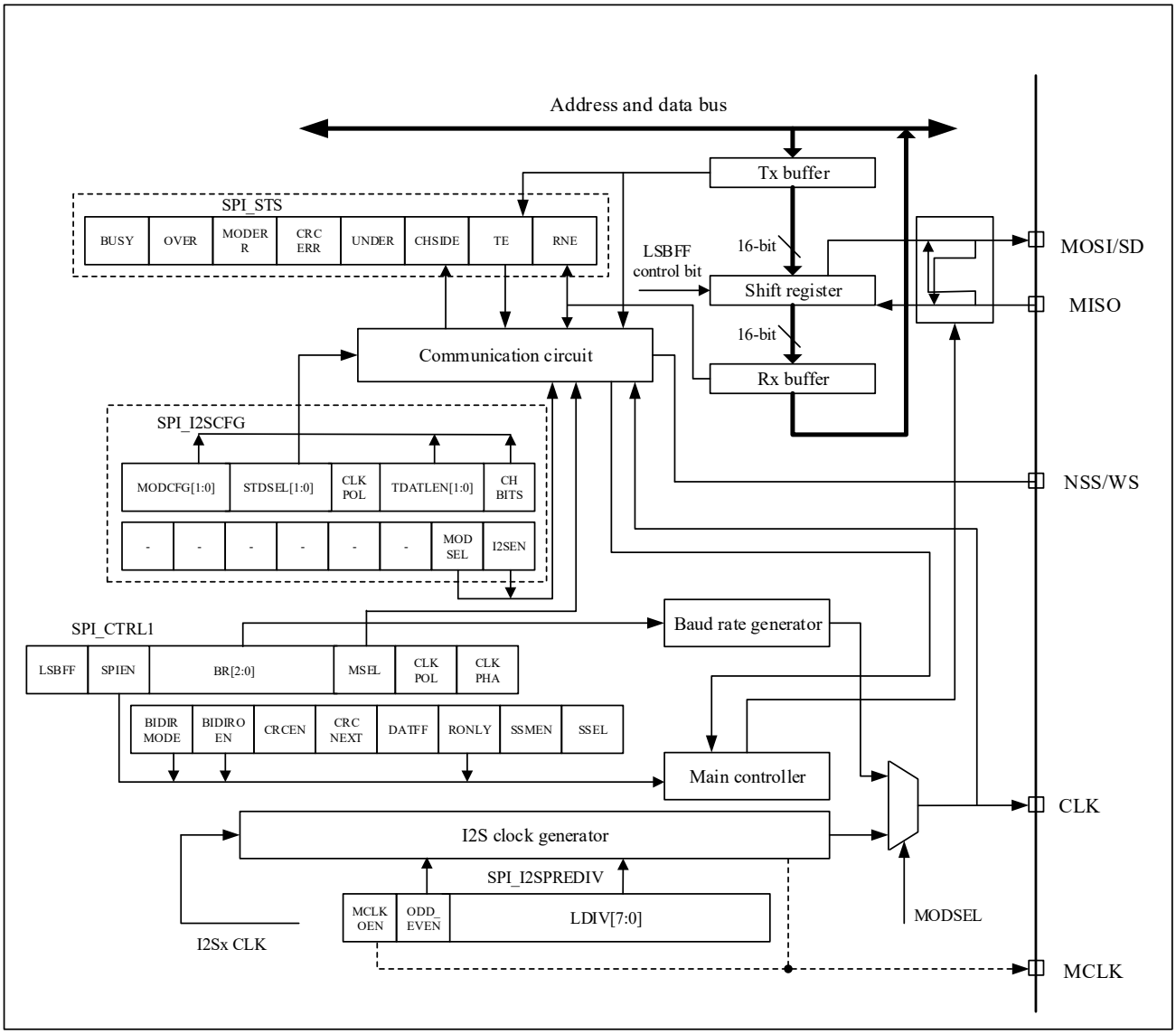
21.4 I²S function description

The block diagram of I2S is shown in the figure below:

Figure 21-13 I²S block diagram



The I2S interface uses the same pins, flags and interrupts as the SPI interface. Setting the SPI_I2SCFG.MODSEL = 1 selects the I2S audio interface.

I2S has a total of 4 pins, 3 of which are shared with SPI:

- CLK: Serial clock (shared with SCLK pin), CLK generates a pulse every time 1-bit audio data is sent.
- SD: Serial data (shared with MOSI pin), used for data send and receive;
- WS: Channel selection (shared with NSS pin), used as data control signal output in master mode, and used as input in slave mode;
- MCLK: master clock (independent mapping, optional), output 256 × Fs clock signal to ensure better synchronization between systems.

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Note: F_S is the sampling frequency of audio signal

In master mode, I2S uses its own clock generator to generate clock signals for communication, and this clock generator is also the clock source of the master clock output (SPI_I2SPREDIV.MCLKOEN = 1, the master clock output is enabled).

21.4.1 Supported audio protocols

Four audio standards can be selected by setting the SPI_I2SCFG.STDSEL[1:0] bits:

- I²S Philips standard
- MSB alignment standard
- LSB alignment standard
- PCM standard

The audio data of the left channel and the right channel are usually time-division multiplexed, and the left channel always sends data before the right channel. By checking the SPI_STS.CHSIDE bit, the user can distinguish which channel the received data belongs to. However, in the PCM audio standard, the CHSIDE bit has no meaning.

By setting the SPI_I2SCFG.TDATLEN bits, the user can set the length of the data to be transmitted, and set the data bit width of the channel by setting the SPI_I2SCFG.CHBITS bits. There are 4 data formats for sending data as follows:

- 16-bit data is packed into 16-bit data frame
- 16-bit data is packed into a 32-bit data frame (the first 16 bits are meaningful data, and the last 16 bits are set to 0 by hardware)
- 24-bit data is packed into 32-bit data frame (the first 24-bit data is meaningful data, and the latter 8-bit data is set to 0 by hardware)
- 32-bit data is packed into 32-bit data frame

I2S uses the same SPI_DAT register as SPI to send and receive 16-bit wide data. If I2S needs to send or receive 24-bit or 32-bit wide data, the CPU needs to read or write the SPI_DAT register twice. On the other hand, when I2S sends or receives 16-bit wide data, the CPU only needs to read or write the SPI_DAT register once.

Regardless of which data format and communication standard is used, I2S always sends the data high-order bit (MSB) first.

I²S Philips standard

Using the I2S Philips standard, the device that sends data changes the data on the falling edge of the clock, and the device that receives data samples the data on the rising edge of the clock. The WS signal should be valid one clock before the first data bit (MSB) is sent and will change on the falling edge of the clock signal.

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Figure 21-14 I²S Philips protocol waveform (16/32-bit full precision, CLKPOL = 0)

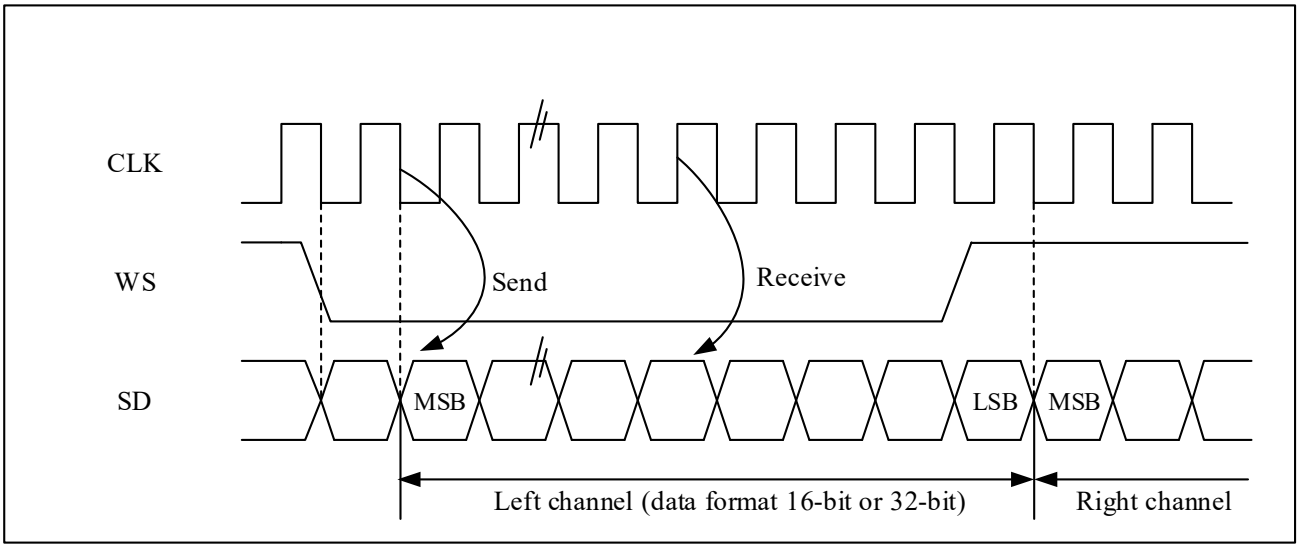
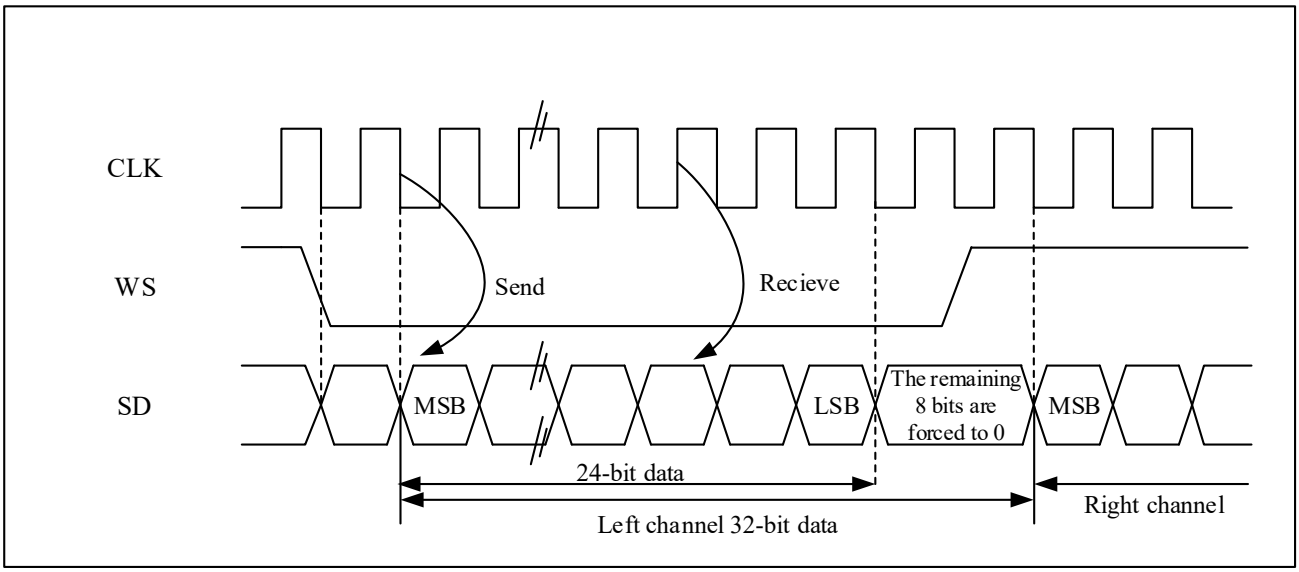


Figure 21-15 I²S Philips protocol standard waveform (24-bit frame, CLKPOL = 0)



If the 24-bit data needs to be packaged into 32-bit data frame format, the CPU needs to read or write the SPI_DAT register twice during each frame of data transmission. For example, if the user sends 24-bit data 0x95AA66, the CPU will first write 0x95AA into the SPI_DAT register, and then write 0x66XX into the SPI_DAT register (only the upper 8-bit data is valid, the lower 8-bit data is meaningless and can be any value); if the user receives 24-bit data 0x95AA66, the CPU will first read the SPI_DAT register to get 0x95AA, and then read the SPI_DAT register to get 0x6600 (only the upper 8-bit data is valid, and the lower 8-bit data is always 0).

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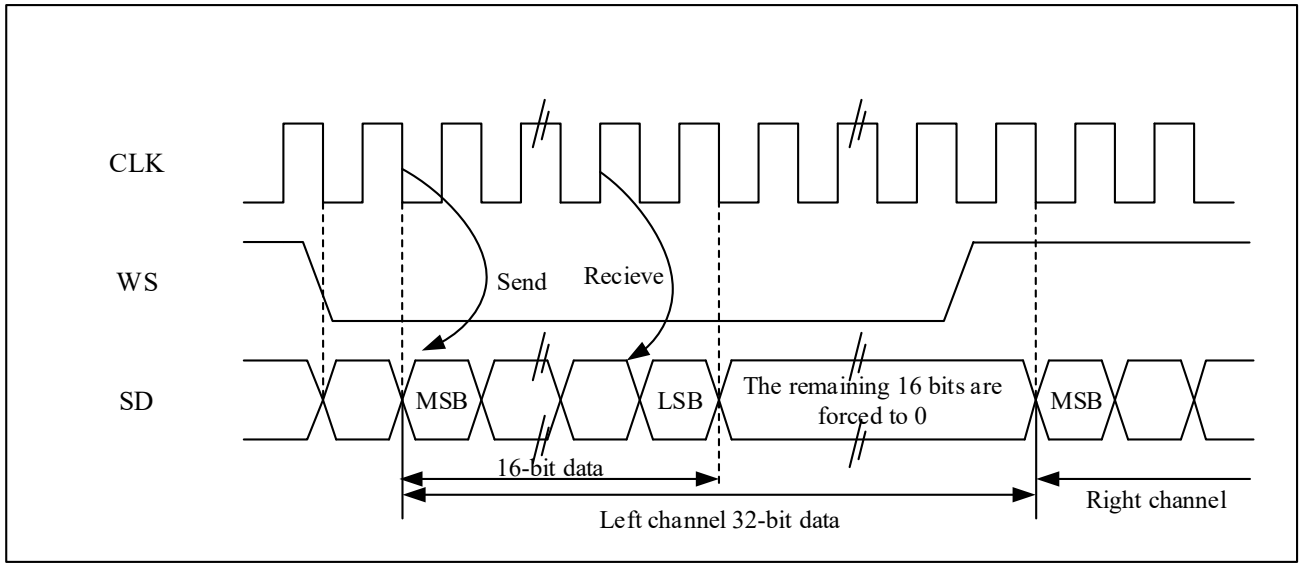
Figure 21-16 I²S Philips protocol standard waveform (16-bit extended to 32-bit packet frame, CLKPOL = 0)



If 16-bit data needs to be packed into 32-bit data frame format, the CPU only needs to read or write the SPI_DAT register once for each frame of data transmission. The lower 16 bits of data for expansion to 32 bits are always set to 0x0000. For example, if the user sends or receives 16-bit data 0x89C1 (extended to 32-bit data is 0x89C10000). In the process of sending data, the upper 16-bit half word (0x89C1) needs to be written into the SPI_DAT register; the user can write new data until the SPI_STS.TE bit is set. An interrupt is generated if the user enables the corresponding interrupt. The sending is performed by hardware, even if the last 16 bits (0x0000) are not sent, the hardware will set the TE (SPI_STS.TE) bit to 1 and the corresponding interrupt will be generated. In the process of receiving data, the RNE flag (SPI_STS.RNE) will be set to 1 after each time the device receives the upper 16-bit halfword (0x89C1). An interrupt is generated if the user enables the corresponding interrupt. In this way, there is more time between 2 reads and writes, which can prevent underflow or overflow from happening.

MSB alignment standard

In the MSB alignment standard, the device sending the data will change the data on the falling edge of the clock, and the device receiving the data will sample the data on the rising edge of the clock. The WS signal and the first data bit (MSB) are generated simultaneously.

The standard data receiving and sending processing mode is the same as I²S Philips standard.

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Figure 21-17 The MSB is aligned with 16-bit or 32-bit full precision, CLKPOL = 0.

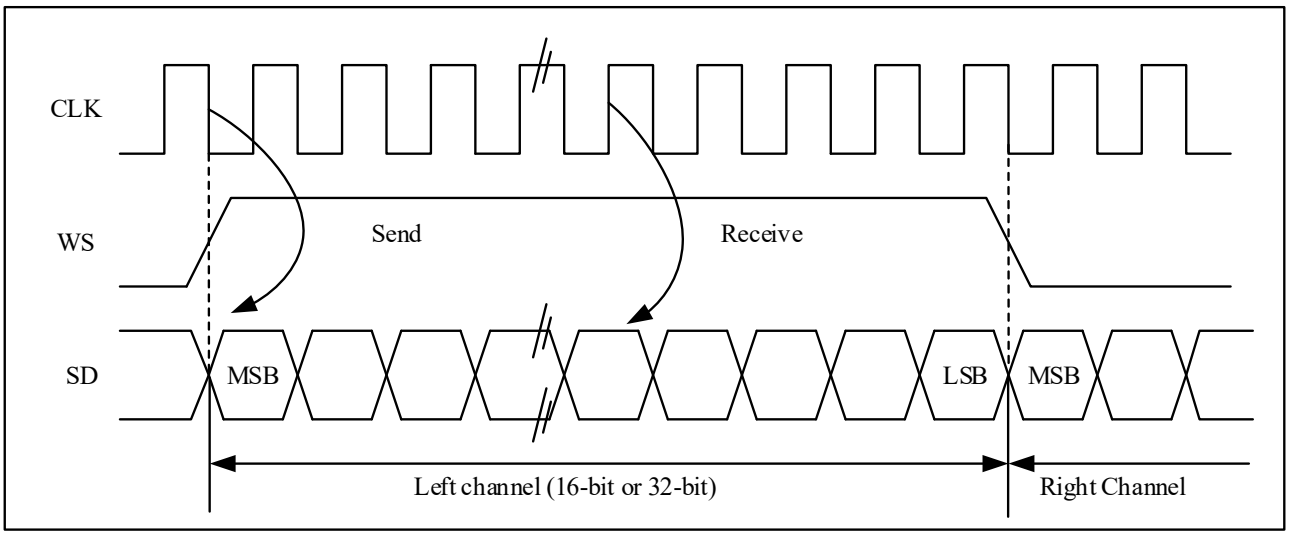


Figure 21-18 MSB aligns 24-bit data, CLKPOL = 0

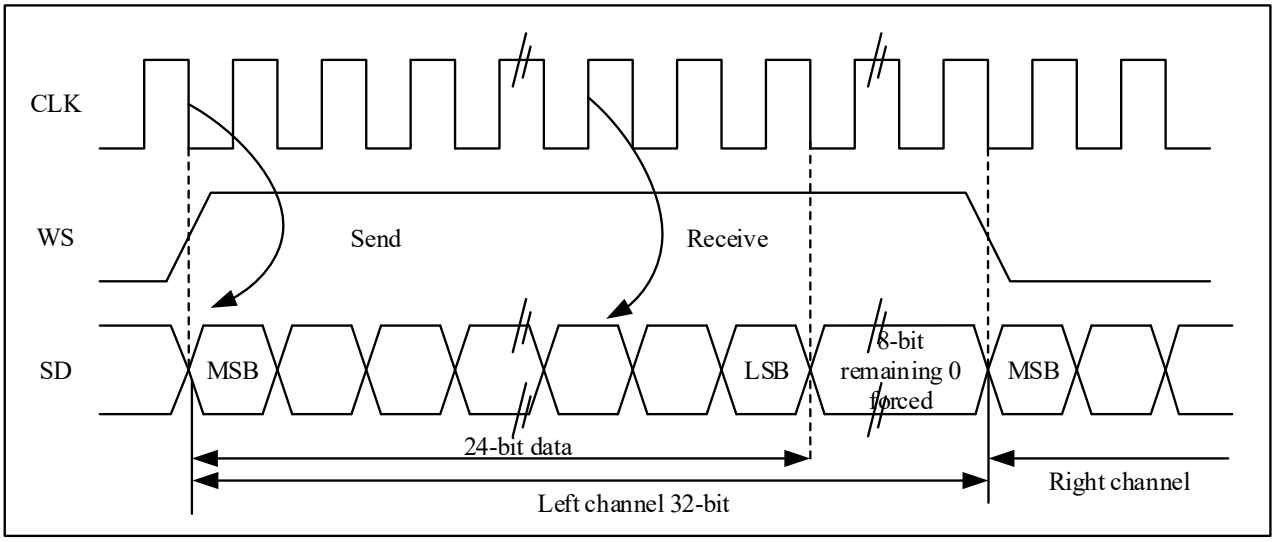
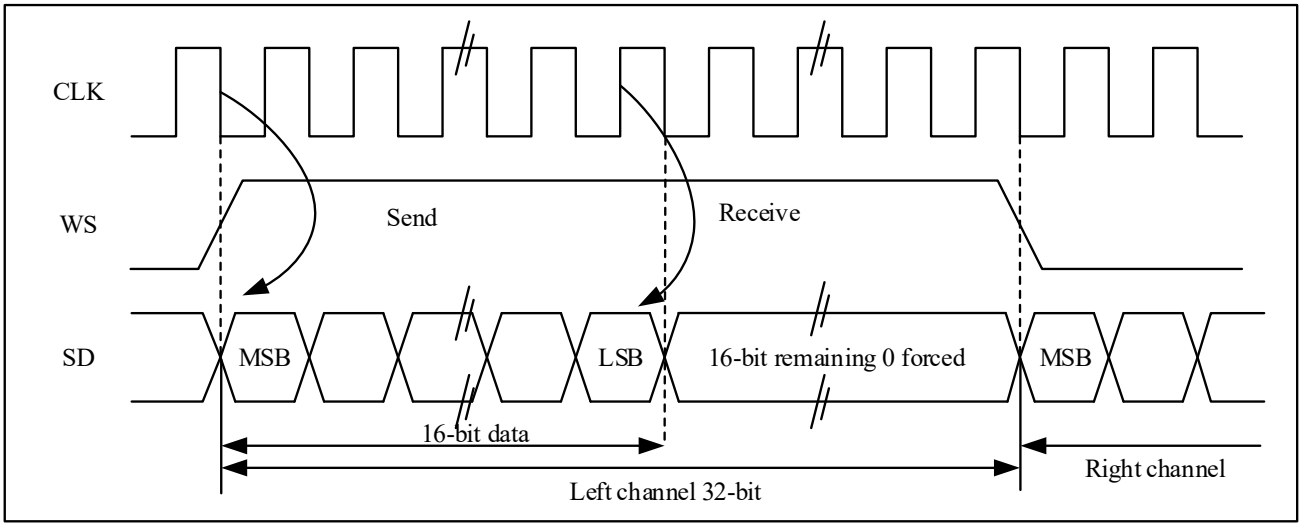


Figure 21-19 MSB-aligned 16-bit data is extended to 32-bit packet frame, CLKPOL = 0



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LSB alignment standard

In 16-bit or 32-bit full-precision frame format, LSB alignment standard is the same as MSB alignment standard.

Figure 21-20 LSB alignment 16-bit or 32-bit full precision, CLKPOL = 0

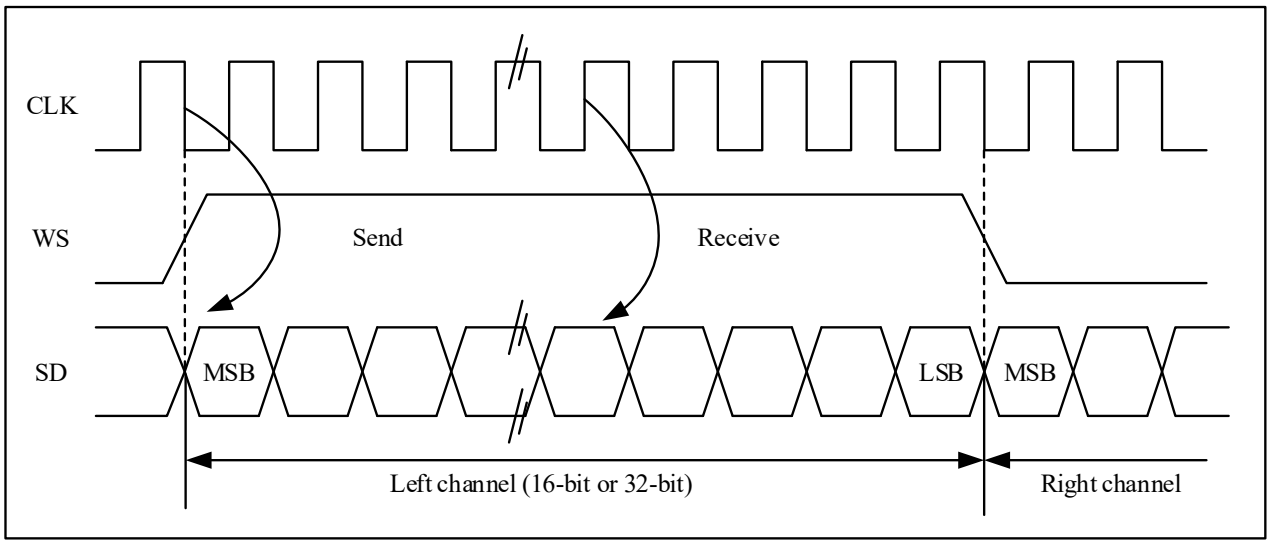
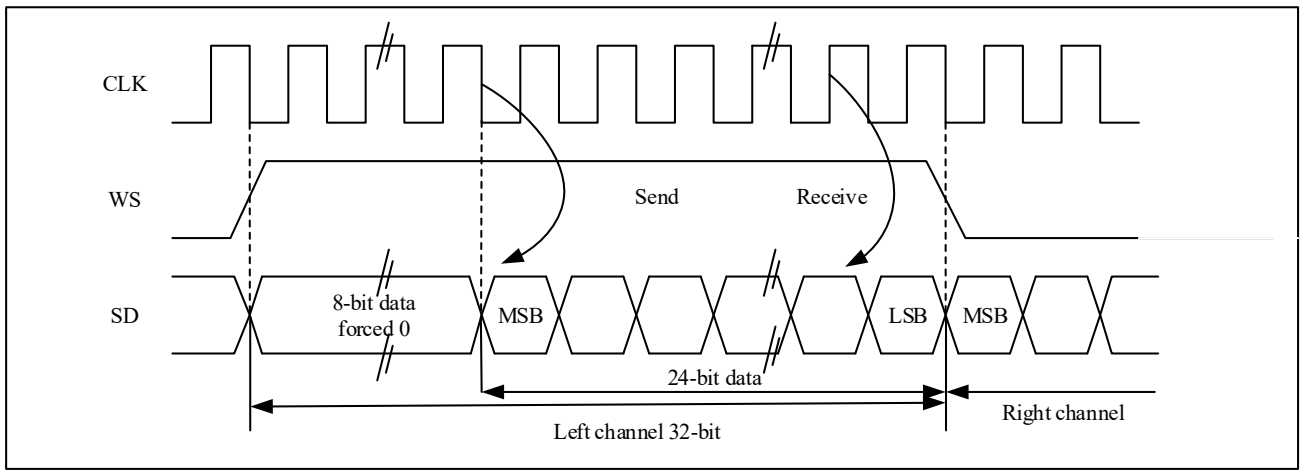


Figure 21-21 LSB aligns 24-bit data, CLKPOL = 0



If the 24-bit data needs to be packed into the 32-bit data frame format, the CPU needs to read or write the SPI_DAT register twice during each frame of data transmission. For example, if the user sends 24-bit data 0x95AA66, the CPU will first write 0xXX95 (only the lower 8-bit data is valid, the upper 8-bit data is meaningless and can be any value) into the SPI_DAT register, and then write 0xAA66 into the SPI_DAT register. If the user receives 24-bit data 0x95AA66, the CPU will first read the SPI_DAT register to get 0x0095 (only the lower 8 bits are valid, the upper 8 bits are always 0), and then read the SPI_DAT register to get 0xAA66.

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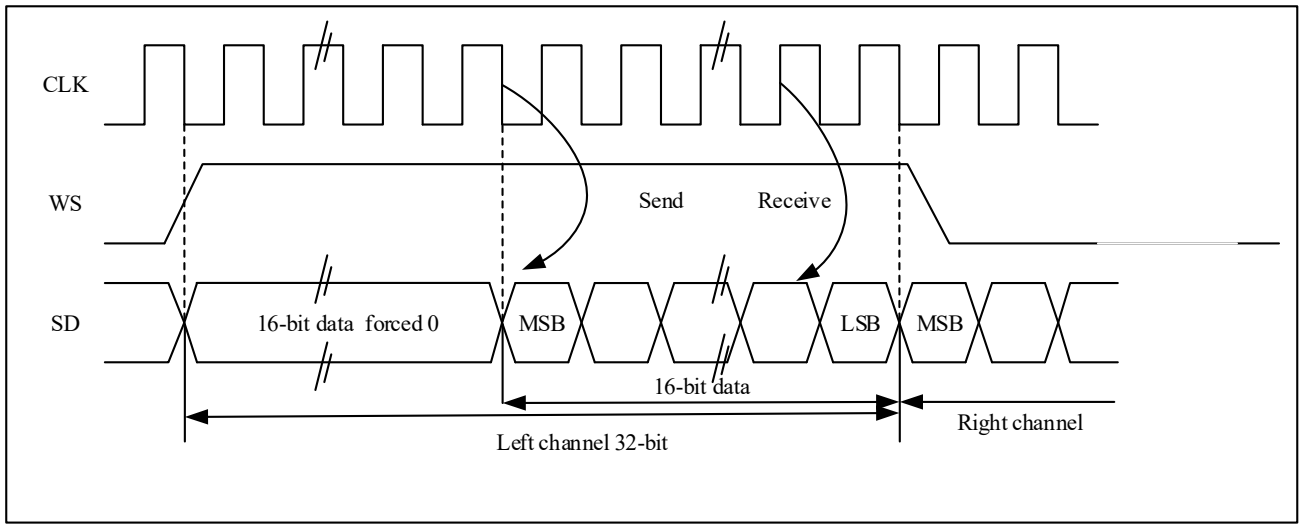
Figure 21-22 LSB aligned 16-bit data is extended to 32-bit packet frame, CLKPOL = 0



If the 16-bit data needs to be packaged into a 32-bit data frame format, the CPU only needs to read or write the SPI_DAT register once for each frame of data transmission. The upper 16 bits of extended to 32 bits data are set to 0x0000 by hardware, if the user sends or receives 16-bit data 0x89C1 (extended to 32-bit data is 0x000089C1). In the process of sending data, the upper 16-bit halfword (0x0000) needs to be written to the SPI_DAT register first; once the valid data starts to be send, the next TE (SPI_STS.TE) event will be generated. In the process of receiving data, once the device receives valid data, the RNE (SPI_STS.RNE) event will be generated. In this way, there is more time between 2 reads and writes, which can prevent underflow or overflow from happening.

PCM standard

In the PCM standard, there are two frame structures, short frame and long frame. The user can select the frame structure by setting the SPI_I2SCFG.PCMFSYNC bits. The WS signal indicates frame synchronization information. The WS signal for synchronizing long frames is 13 bits effective; the WS signal length for synchronizing short frames is 1 bit.

The standard data receiving and sending processing mode is the same as I^2S Philips standard.

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Figure 21-23 PCM standard waveform (16 bits)

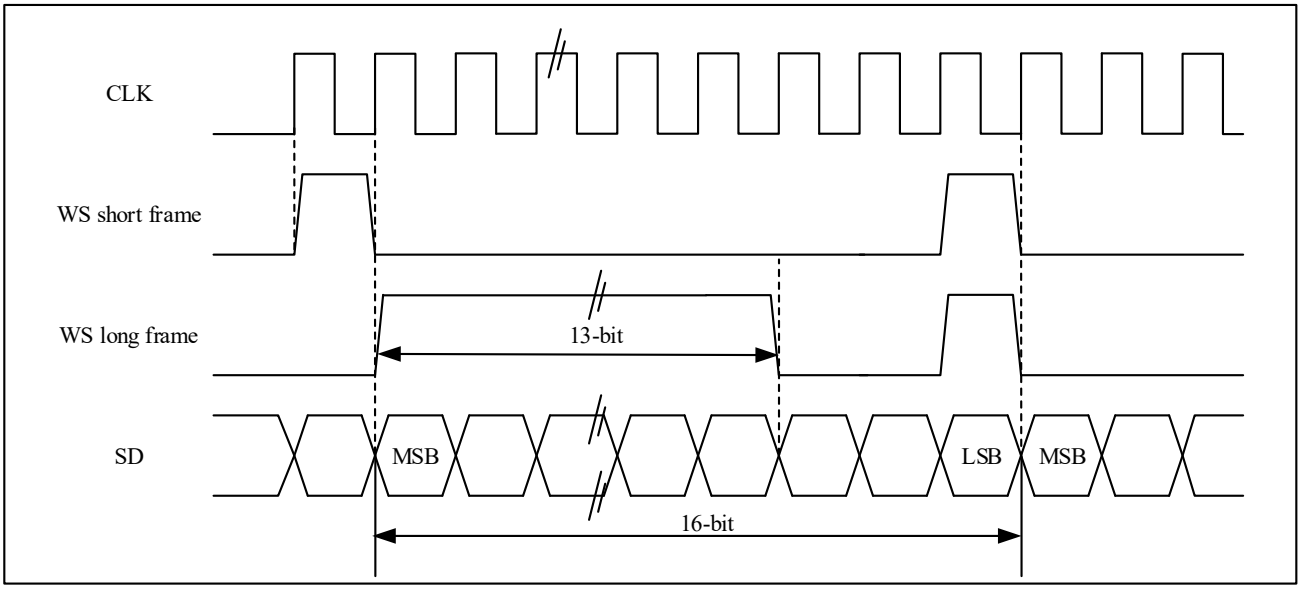
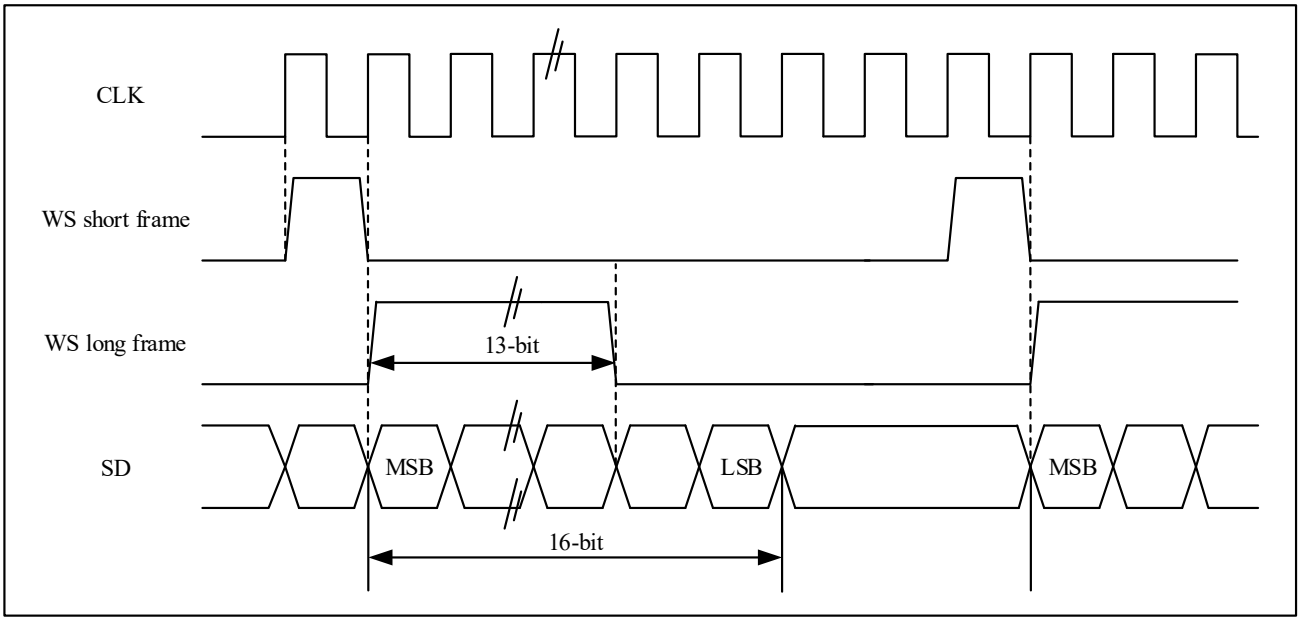


Figure 21-24 PCM standard waveform (16-bit extended to 32-bit packet frame)



21.4.2 Clock generator

In the master mode, the linear divider needs to be set correctly in order to obtain the desired audio frequency.

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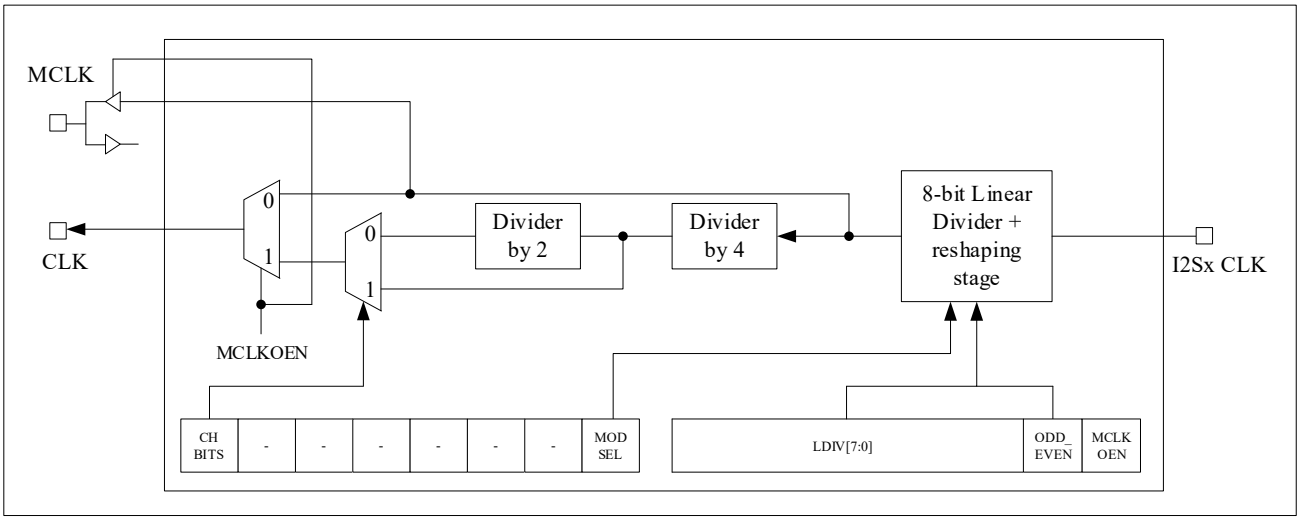
Figure 21-25 I²S clock generator structure



Note: The clock source of I²Sx CLK is HSI, HSE or PLL system clock that drives AHB clock.

The bit rate of I2S determines the data flow on the I2S data line and the frequency of the I2S clock signal.

I²S bit rate = number of bits per channel × number of channels × audio sampling frequency

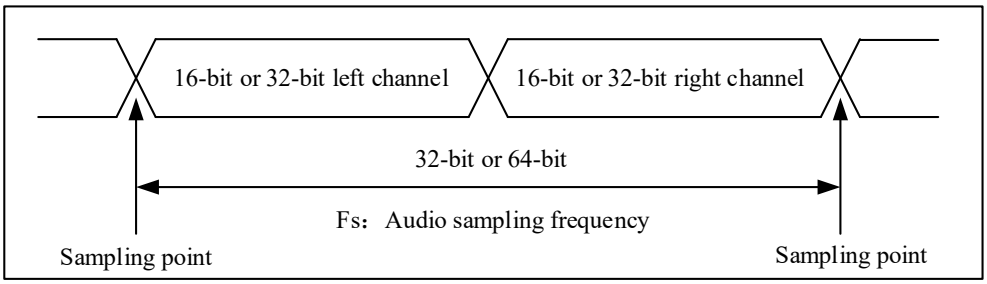
For a signal with left and right channels and 16-bit audio, the I2S bit rate is calculated as:

$$\textbf{I}^2\textbf{S bit rate} = 16 \times 2 \times F_S$$

If the packet length is 32 bits, there are:

$$\textbf{I}^2\textbf{S bit rate} = 32 \times 2 \times F_S$$

Figure 21-26 Audio sampling frequency definition



The sampling signal frequency of the audio can be set by setting the SPI_I2SPREDIV.ODD_EVEN bit and the SPI_I2SPREDIV.LDIV[7:0] bits. Audio can be sampled at 96kHz, 48kHz, 44.1kHz, 32kHz, 22.05kHz, 16kHz, 11.025kHz, or 8kHz (or any value within this range). Set the linear divider according to the following formula:

When MCLKOEN = 1 and CHBITS= 0, $F_S = I^2Sx\ CLK/\left[(16 \times 2) \times \left((2 \times LDIV) + ODD\_EVEN\right) \times 8\right]$

When MCLKOEN = 1 and CHBITS = 1, $F_S = I^2Sx\ CLK/\left[(32 \times 2) \times \left((2 \times LDIV) + ODD\_EVEN\right) \times 4\right]$

When MCLKOEN = 0 and CHBITS = 0, $F_S = I^2Sx\ CLK/\left[(16 \times 2) \times \left((2 \times LDIV) + ODD\_EVEN\right)\right]$

When MCLKOEN = 0 and CHBITS = 1, $F_S = I^2Sx\ CLK/\left[(32 \times 2) \times \left((2 \times LDIV) + ODD\_EVEN\right)\right]$

The exact audio frequency can be obtained by referring to the clock configuration in the table below.

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Table 21-2 Use the standard 8MHz HSE clock to get accurate audio frequency.

SYSCLK	I²S_LDIV		I²S_ODD_EVEN		MCLK	Target	Real Fs(Hz)		Error	
（MHz）	16 bits	32 bits	16 bits	32 bits		Fs(Hz)	16 bits	32 bits	16 bits	32 bits
72	11	6	1	0	without	96000	97826.09	93750	1.90%	2.34%
72	23	11	1	1	without	48000	47872.34	48913.04	0.27%	1.90%
72	25	13	1	0	without	44100	44117.65	43269.23	0.04%	1.88%
72	35	17	0	1	without	32000	32142.86	32142.86	0.44%	0.44%
72	51	25	0	1	without	22050	22058.82	22058.82	0.04%	0.04%
72	70	35	1	0	without	16000	15675.75	16071.43	0.27%	0.45%
72	102	51	0	0	without	11025	11029.41	11029.41	0.04%	0.04%
72	140	70	1	1	without	8000	8007.11	7978.72	0.09%	0.27%
72	2	2	0	0	yes	96000	70312.15	70312.15	26.76%	26.76%
72	3	3	0	0	yes	48000	46875	46875	2.34%	2.34%
72	3	3	0	0	yes	44100	46875	46875	6.29%	6.29%
72	4	4	1	1	yes	32000	31250	31250	2.34%	2.34%
72	6	6	1	1	yes	22050	21634.61	21634.61	1.88%	1.88%
72	9	9	0	0	yes	16000	15625	15625	2.34%	2.34%
72	13	13	0	0	yes	11025	10817.3	10817.3	1.88%	1.88%
72	17	17	1	1	yes	8000	8035.71	8035.71	0.45%	0.45%

21.4.3 I²S Transmission and reception sequence

I²S initialization sequence

1. The user can set the SPI_I2SPREDIV.LDIV [7:0] bits and SPI_I2SPREDIV.ODD_EVEN bit to configure the related prescaler and serial clock baud rate;
2. If the user needs the master device to provide the main clock MCLK to the external DAC/ADC audio device, set the SPI_I2SPREDIV.MCLKOEN = 1. (Calculate LDIV and ODD_EVEN according to different clock outputs, see section 21.4.2).
3. The user can set the SPI_I2SCFG.CLKPOL bit to define the polarity of the communication clock when idle; the user can set the SPI_I2SCFG.MODSEL = 1 to configure the device to be in I2S mode, and set SPI_I2SCFG.MODCFG[1:0] bits to select the I2S master-slave mode and transmission direction (send or receive); set SPI_I2SCFG.STDSEL[1:0] bits to select the corresponding I2S standard (under the PCM standard, set the SPI_I2SCFG.PCMFSYNC bit to select the PCM frame synchronization mode); set SPI_I2SCFG.TDATLEN [1:0] bits to select length of data to be transmitted, and select the number of data bits of per channel by set the SPI_I2SCFG.CHBITS bit;
4. When user needs to enable interrupt or DMA, the configuration operation is the same as SPI;
5. Finally, set the SPI_I2SCFG.I2SEN = 1 to start I2S communication.

Sending sequence

Master mode

When I2S works in master mode, the CLK pin outputs the serial clock, the WS pin generates the channel selection signal, and set the SPI_I2SPREDIV.MCLKOEN bit to select whether to output the master clock (MCLK).

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The sending process begins when data is written to the send buffer. When the data of the current channel is moved from the send buffer to the shift register in parallel, the flag bit TE (SPI_STS.TE) is set to '1'. At this time, the data of the other channel should be written into SPI_DAT. The channel corresponding to the current data to be transmitted is confirmed by the flag bit CHSIDE (SPI_STS. CHSIDE). The value of CHSIDE (SPI_STS. CHSIDE) is updated when TE (SPI_STS.TE) is set to '1'. A complete data frame includes left and right channels, and only part of the data frame cannot be transmitted. When the flag bit TE (SPI_STS.TE) is set to '1', if the SPI_CTRL2.TEINTEN = 1, an interrupt will be generated.

The operation of writing data depends on the selected I2S standard. See chapter 21.4.1 for details.

When the user wants to turn off the I2S function, wait for the TE flag (SPI_STS.TE) bit to be 1 and the BUSY flag (SPI_STS.BUSY) bit to be 0, and then clear the SPI_I2SCFG.I2SEN bit to 0.

Slave mode

The sending process of the slave mode is similar to that of the master mode, the difference is as follows:

When I2S works in slave mode, there is no need to configure the clock, and the CLK pin and WS pin are connected to the corresponding pins of the master device. The sending process begins when an external master sends a clock signal, and when a WS signal requires data transfer. Only when the slave device is enabled and the data has been written to the I2S data register, the external master device can start communication.

When the first clock edge representing the next data transfer arrives, the new data has not been written into the SPI_DAT register, an underflow occurs, and the SPI_STS.UNDER flag bit is set to 1. If the SPI_CTRL2.ERRINTEN bit is set to 1, an interrupt is generated to indicate that an error has occurred.

The SPI_STS.CHSIDE flag indicates which channel the currently transmitted data corresponds to. Compared with the master mode sending process, in the slave mode, CHSIDE depends on the WS signal of the external master I2S device (WS signal is 1 means the left channel)

Receiving sequence

Master mode

Audio is always received in 16-bit packets. According to the configured data and channel length, the received audio data will need to be transferred to the receive buffer once or twice.

When the data is transferred from the shift register to the receive buffer, the SPI_STS.RNE flag bit is set to 1, at this time, the data is ready and can be read from the SPI_DAT register. If the SPI_CTRL2.RNEINTEN bit is set to 1, an interrupt will be generated. Reading the SPI_DAT register to clear the SPI_STS.RNE flag. If the previously received data is not read, new data is received again, an overflow occurs, and the SPI_STS.OVER flag is set to 1. If the SPI_CTRL2.ERRINTEN bit is set to 1, an interrupt is generated to indicate that an error has occurred.

The channel corresponding to the currently transmitted data can be confirmed by the SPI_STS.CHSIDE bit. When the SPI_STS.RNE flag bit is set to 1, the SPI_STS.CHSIDE value is updated.

The operation of reading data depends on the selected I2S standard. See Section 21.4.1 for details.

When I2S function is turned off, different audio standards, data length and channel length adopt different operation steps:

- Data length is 16 bits, channel length is 32 bits (SPI_I2SCFG.TDATLEN = 00, SPI_I2SCFG.CHBITS = 1), LSB alignment standard (SPI_I2SCFG.STDSEL = 10).

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1. Wait for the penultimate RNE flag (SPI_STS.RNE) bit to be set to' 1'.
2. Software delay, waiting for 17 I^2S clock cycles.
3. Turn off I^2S (SPI_I2SCFG.I2SEN = 0).

- The data length is 16 bits, the channel length is 32 bits (SPI_I2SCFG.TDATLEN = 00 and SPI_I2SCFG.CHBITS = 1), the MSB alignment standard (SPI_I2SCFG.STDSEL = 01), I^2S Philips standard (SPI_I2SCFG.STDSEL = 00) or PCM standard (SPI_I2SCFG.STDSEL = 11)
  1. Wait for the last RNE flag (SPI_STS.RNE) bit to be set to' 1'.
  2. Software delay, waiting for 1 I^2S clock cycle.
  3. Turn off I^2S (SPI_I2SCFG.I2SEN = 0).
- Other combinations of SPI_I2SCFG.TDATLEN and SPI_I2SCFG.CHBITS and any audio mode selected by SPI_I2SCFG.STDSEL:
  1. Wait for the penultimate RNE flag (SPI_STS.RNE) bit to be set to' 1'.
  2. Software delay, waiting for 1 I^2S clock cycle.
  3. Turn off I^2S (SPI_I2SCFG.I2SEN = 0).

Slave mode

The receiving process of the slave mode is similar to that of the master mode, with the following differences:

The CHSIDE flag (SPI_STS.CHSIDE) indicates which channel corresponds to the currently transmitted data. Compared with the master mode receiving process, in the slave mode, SPI_STS.CHSIDE depends on the WS signal of the external master device. When the I2S function is turned off, clear the SPI_I2SCFG.I2SEN bit to 0 when the SPI_STS.RNE flag is 1.

21.4.4 Status flag

There are the following 4 flag bits in the SPI_STS register for monitoring the status of the I2S bus.

TX buffer empty flag (TE)

When the send buffer is empty, this flag is set to 1, indicating that new data can be written into the SPI_DAT register. When the send buffer is not empty, this flag is cleared to 0.

RX buffer not empty flag (RNE)

When the receive buffer is not empty, this flag is set to 1, indicating that valid data has been received into the receive buffer. When reading the SPI_DAT register, this flag is set to 0.

BUSY flag (BUSY)

When the transfer starts, the BUSY flag (SPI_STS.BUSY) is set to 1, and when the transfer ends, the BUSY flag (SPI_STS.BUSY) is set to 0 by hardware (software operation is invalid).

In master receiving mode (SPI_I2SCFG.MODCFG = 11), the BUSY flag (SPI_STS.BUSY) is set to 0 during receiving. When the I2S module is turned off or the transmission is completed, this flag is set to 0.

In the slave continuous communication mode, between each data item transmission, the BUSY flag (SPI_STS.BUSY) goes low in 1 I2S clock cycle. Therefore, do not use the BUSY flag(SPI_STS.BUSY) to handle the sending and

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receiving of each data item.

Channel Side flag (CHSIDE)

The CHSIDE (SPI_STS.CHSIDE) bit is used to indicate the channel where the data currently sent and received is located. Under the PCM standard, this flag has no meaning.

In send mode, the flag is updated when the TE flag (SPI_STS.TE) is set; in receive mode, the flag is updated when the RNE flag (SPI_STS.RNE) is set. In the process of sending and receiving, if an overflow (SPI_STS.OVER) or underflow (SPI_STS.UNDER) error occurs, this flag is meaningless, and the I2S needs to be turned off and then turned on again.

21.4.5 Error flag

The SPI_STS register has 2 error flag bits.

Overflow flag (OVER)

When the RNE flag (SPI_STS.RNE) is set to 1, but there is still data sent to the receive buffer, an overflow error will occur. At this time, the OVER flag (SPI_STS.OVER) is set to 1. An interrupt will be generated if the user enables the corresponding interrupt. All data received after this time will be lost, and the SPI_DAT register only retains the previously unread data.Reading the SPI_DAT register and the SPI_STS register in turn to clear the SPI_STS.OVER bit.

Underflow flag (UNDER)

In slave send mode, when the first clock edge of sending data arrives, if the send buffer is still empty, the UNDER flag (SPI_STS.UNDER) is set to 1. An interrupt will be generated if the user enables the corresponding interrupt.

Reading the SPI_STS register to clears the SPI_STS.UNDER bit.

21.4.6 I^2S interrupt

The following table lists all I^2S interrupts.

Table 21-3 I^2S interrupt request

Interrupt event	Event flag bit	Enable control bit
Send buffer empty flag	TE	TEINTEN
Receive buffer non empty flag	RNE	RNEINTEN
Underflow flag bit	UNDER	ERRINTEN
Overflow flag bit	OVER	

21.4.7 DMA function

Working in I2S mode, it does not need data transmission protection function, so it does not need to support CRC, other DMA functions are the same as SPI mode.

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21.5 SPI and I²S register

21.5.1 SPI register overview

Table 21-4 SPI register overview

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
000h	SPI_CTRL1	Reserved																BIDIRMODE	BIDIROEN	CRCEN	CRCNEXT	DATFF	RONLY	SSMEN	SSEL	LSBFF	SPIEN	BR[2:0]			MSEL	CLKPOL	CLKPHA
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
004h	SPI_CTRL2	Reserved																								TEINTEN	RNEINTEN	ERRINTEN	Reserved			SSOEN	TDMAEN	RDMAEN
	Reset Value																									0	0	0				0	0	0
008h	SPI_STS	Reserved																								BUSY	OVER	MODERR	CRCERR	UNDER	CHSIDE	TE	RNE
	Reset Value																									0	0	0	0	0	0	1	0
00Ch	SPI_DAT	Reserved																DAT[15:0]															
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
010h	SPI_CRCPOLY	Reserved																CRCPOLY[15:0]															
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1
014h	SPI_CRCRDAT	Reserved																CRCRDAT[15:0]															
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
018h	SPI_CRCTDAT	Reserved																CRCTDAT[15:0]															
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
01Ch	SPI_I2SCFG	Reserved																				MODSEL	I2SEN	MODCFG [1:0]		PCMFSYNC	Reserved	STDSEL [1:0]		CLKPOL	TDATLEN [1:0]		CHBITS
	Reset Value																					0	0	0	0	0		0	0	0	0	0	0
020h	SPI_I2SPREDIV	Reserved																						MCLKOEN	ODD_EVEN	LDIV[7:0]							
	Reset Value																							0	0	0	0	0	0	0	0	1	0

21.5.2 SPI control register 1 (SPI_CTRL1) (not used in I2S mode)

Address: 0x00

Reset value: 0x0000

15	14	13	12	11	10	9	8	7	6	5	3	2	1	0
BIDIR MODE	BIDIR OEN	CRCEN	CRC NEXT	DATFF	RONLY	SSMEN	SSEL	LSBFF	SPIEN	BR[2:0]		MSEL	CLKPOL	CLKPHA
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw		rw	rw	rw

Bit field	name	describe
15	BIDIRMODE	Bidirectional data mode enable 0: Select the "two-wire one-way" mode. 1: Select the "one-wire bidirectional " mode. *Note: Not used in I²S mode.*

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Bit field	name	describe
14	BIDIROEN	Output enable in bidirectional mode 0: Output disable (receive-only mode). 1: Output enabled (send-only mode). In master mode, the "one-wire" data line is the MOSI pin, and in slave mode, the "one-wire" data line is the MISO pin. *Note: Not used in I²S mode.*
13	CRCEN	Hardware CRC check enable 0: Disable CRC calculation. 1: Enable CRC calculation. *Note: This bit can only be written when SPI is disabled (SPI_CTRL1.SPIEN = 0), otherwise an error will occur.* This bit can only be used in full duplex mode. *Note: Not used in I²S mode.*
12	CRCNEXT	Send CRC next 0: The next sent value comes from the send buffer. 1: The next send value comes from the CRC register. *Note: This bit should be set immediately after the last data is written in SPI_DAT register.* *Note: Not used in I²S mode.*
11	DATFF	Data frame format 0: 8-bit data frame format is used for sending/receiving. 1: 16-bit data frame format is used for sending/receiving. *Note: This bit can only be written when SPI is disabled (SPI_CTRL1.SPIEN = 0), otherwise an error will occur.* *Note: Not used in I²S mode.*
10	RONLY	Only receive mode This bit, together with the SPI_CTRL1.BIDIRMODE bit, determines the transfer direction in two-wire one-way mode. In the application scenario of multiple slave devices, this bit is only set to 1 by the accessed slave device, and only the accessed slave device can output, so as to avoid data line conflicts. 0: Full duplex (sending mode and receiving mode). 1: Disable output (receive-only mode). *Note: Not used in I²S mode.*
9	SSMEN	Software slave device management When the SPI_CTRL1.SSMEN bit is set to 1, the NSS pin level is determined by the value of the SPI_CTRL1.SSEL bit. 0: Disable software slave device management. 1: Enable software slave device management. *Note: Not used in I²S mode.*
8	SSEL	Internal slave device selection This bit only has meaning when the SPI_CTRL1.SSMEN bit is set. It determines the NSS level, and I/O operations on the NSS pin have no effect. *Note: Not used in I²S mode.*

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Bit field	name	describe
7	LSBFF	Frame format 0: Send MSB first. 1: Send LSB first. *Note: This bit cannot be changed during communication.* *Note: Not used in I²S mode.*
6	SPIEN	SPI enable 0: Disable SPI device. 1: Enable the SPI device. *Note: Not used in I²S mode.* *Note: When turning off the SPI device, please follow paragraph 21.3.4 Section's procedure operation.*
5:3	BR[2:0]	Baud rate control 000: fPCLK/2 001: fPCLK/4 010: fPCLK/8 011: fPCLK/16 100: fPCLK/32 101: fPCLK/64 110: fPCLK/128 111: fPCLK/256 *Note: This bit cannot be changed during communication.* *Note: Not used in I²S mode.*
2	MSEL	Master device selection 0: Configure as the slave device. 1: Configure as the master device. *Note: This bit cannot be changed during communication.* *Note: Not used in I²S mode.*
1	CLKPOL	Clock polarity 0: In idle state, SCLK remains low. 1: In idle state, SCLK remains high. *Note: This bit cannot be changed during communication.* *Note: Not used in I²S mode.*
0	CLKPHA	Clock phase 0: Data is sampled on the first clock edge. 1: Data is sampled on the second clock edge. *Note: This bit cannot be changed during communication.* *Note: Not used in I²S mode.*

21.5.3 SPI control register 2 (SPI_CTRL2)

Address: 0x04

Reset value: 0x0000

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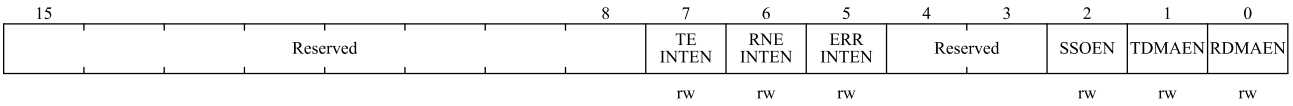
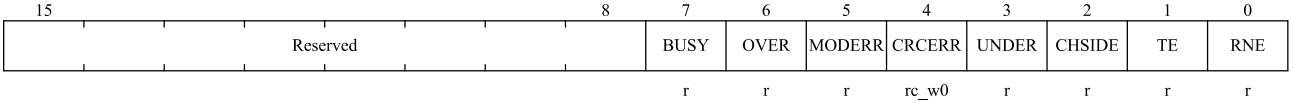


Bit field	name	describe
15:8	Reserved	Reserved, the reset value must be maintained.
7	TEINTEN	Send buffer empty interrupt enable 0: Disable TE interrupt. 1: Enable TE interrupt, and interrupt request is generated when TE flag (SPI_STS.TE) is set to '1'.
6	RNEINTEN	Receive buffer non-empty interrupt enable 0: Disable RNE interrupt. 1: Enable RNE interrupt, and generate interrupt request when RNE flag (SPI_STS.RNE) is set to '1'.
5	ERRINTEN	Error interrupt enable When an error (SPI_STS.CRCERR, SPI_STS.OVER, SPI_STS.UNDER, SPI_STS.MODERR) is generated, this bit controls whether an interrupt is generated 0: Disable error interrupt. 1: Enable error interrupt.
4:3	Reserved	Reserved, the reset value must be maintained.
2	SSOEN	NSS output enable 0: Disable NSS output in master mode, the device can work in multi-master mode. 1: When the device is turned on, enable NSS output in the master mode, the device cannot work in the multi-master device mode. *Note: Not used in I^2S mode.*
1	TDMAEN	Send buffer DMA enable When this bit is set, a DMA request is issued as soon as the TE flag (SPI_STS.TE) is set 0: Disable send buffer DMA. 1: Enable send buffer DMA.
0	RDMAEN	Receive buffer DMA enable When this bit is set, a DMA request is issued as soon as the RNE flag (SPI_STS.RNE) is set 0: Disable receive buffer DMA. 1: Enable receive buffer DMA.

21.5.4 SPI status register (SPI_STS)

Address: 0x08

Reset value: 0x0002



Bit field	name	describe
15:8	Reserved	Reserved, the reset value must be maintained.

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Bit field	name	describe
7	BUSY	Busy flag 0: SPI is not busy. 1: SPI is busy communicating or the send buffer is not empty. This bit is set or reset by hardware. *Note: special attention should be paid to the use of this sign, see Section 21.3.3 and Section 21.3.4 for details..*
6	OVER	Overflow flag 0: No overflow error. 1: An overflow error occurred. *Note:This bit is set by hardware and cleared according to the sequence of software operations. For more information about software sequences, refer to 21.3.7 for details.*
5	MODERR	Mode error 0: No mode error. 1: A mode error occurred. *Note:This bit is set by hardware and cleared according to the sequence of software operations. For more information about software sequences, refer to 21.3.7 for details.* *Note: Not used in I^2S mode.*
4	CRCERR	CRC error flag 0: The received CRC value matches the value the SPI_CRCRDAT register value. 1: The received CRC value does not match the SPI_CRCRDAT register value. *Note: this bit is set by hardware and cleared by software by writing 0.* *Note: Not used in I^2S mode.*
3	UNDER	Underflow flag 0: No underflow occurred. 1: Underflow occurred. *Note:This bit is set by hardware and cleared according to the sequence of software operations. For more information about software sequences, refer to 21.4.5 for details.* *Note: not used in SPI mode.*
2	CHSIDE	Channel 0: The left channel needs to be sent or received. 1: The right channel needs to be sent or received. *Note: not used in SPI mode. No meaning in PCM mode.*
1	TE	The send buffer is empty 0: The send buffer is not empty. 1: The send buffer is empty.
0	RNE	Receive buffer is not empty 0: The receive buffer is empty. 1: The receive buffer is not empty.

21.5.5 SPI data register (SPI_DAT)

Address: 0x0C

Reset value: 0x0000

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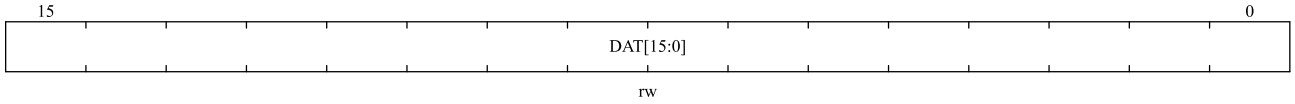
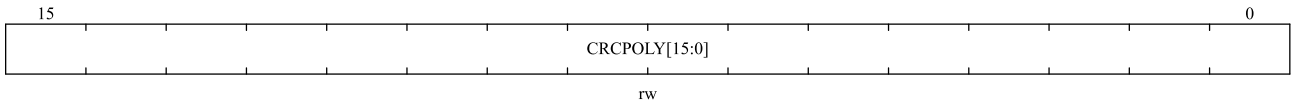


Bit field	name	describe
15:0	DAT[15:0]	Data register Data to be sent or received The data register corresponds to two buffers: one for write (send buffer); The other is for read (receive buffer).Write operation writes data to send buffer; The read operation will return the data in the receive buffer. Note on SPI mode: According to the selection of the data frame format by the SPI_CTRL1.DATFF bit, the data sending and receiving can be 8-bit or 16-bit. To ensure correct operation, the data frame format needs to be determined before enabling the SPI. For 8-bit data, the buffer is 8-bit, and only SPI_DAT[7:0] is used when sending and receiving. When receiving, SPI_DAT[15:8] is forced to 0. For 16-bit data, the buffer is 16-bit, and the entire data register is used when sending and receiving, that is, SPI_DAT[15:0].

21.5.6 SPI CRC polynomial register (SPI_CRCPOLY) (not used in I²S mode)

Address: 0x10

Reset value: 0x0007

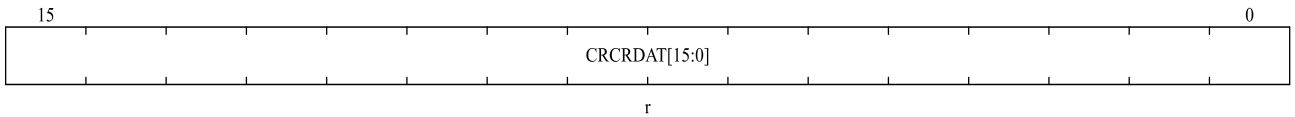


Bit field	name	describe
15:0	CRCPOLY [15:0]	CRC polynomial register This register contains the polynomial used for the CRC calculation. The reset value is 0x0007, other values can be set according to the application. *Note: not used in I²s mode.*

21.5.7 SPI RX CRC register (SPI_CRCRDAT) (not used in I²S mode)

Address offset: 0x14

Reset value: 0x0000



Bit field	name	describe

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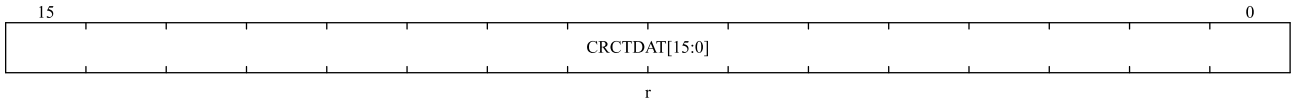
15:0	CRCRDAT	Receive CRC register When CRC calculation is enabled, CRCRDAT[15:0] will contain the calculated CRC value of subsequent received bytes. This register is reset when '1' is written to the SPI_CTRL1.CRCEN bit. The CRC calculation uses the polynomial in SPI_CRCPOLY. When the data frame format is set to 8 bits, only the lower 8 bits participate in the calculation and follow the CRC8 standard; when the data frame format is 16 bits, all 16 bits in the register participate in the calculation and follow the CRC16 standard. *Note: reading this register when the BUSY flag (SPI_STS.BUSY) is '1' may read incorrect values.* *Note: not used in I²s mode.*

21.5.8 SPI TX CRC register（SPI_CRCTDAT）

Address offset: 0x18

Reset value: 0x0000

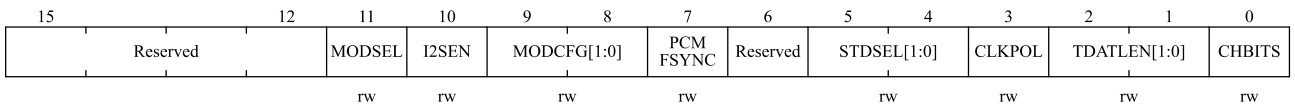


Bit field	Name	Description
15:0	CRCTDAT	Send CRC register When CRC calculation is enabled, CRCTDAT[15:0] contains the CRC value calculated by the bytes sent subsequently. This register is reset when '1' is written to the SPI_CTRL1.CRCEN bit. The CRC calculation uses the polynomial in SPI_CRCPOLY. When the data frame format is set to 8 bits, only the lower 8 bits participate in the calculation and follow the CRC8 standard; when the data frame format is 16 bits, all 16 bits in the register participate in the calculation and follow the CRC16 standard. *Note: reading this register when the BUSY flag (SPI_STS.BUSY) is '1' may read incorrect values.* *Note: not used in I²s mode.*

21.5.9 SPI_ I²S configuration register（SPI_I2SCFG）

Address offset: 0x1c

Reset value: 0x0000



Bit field	Name	Description
15:12	Reserved	Reserved, the reset value must be maintained.
11	MODSEL	I²S mode selection 0: Select SPI mode. 1: Select I²S mode.

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Bit field	Name	Description
		Note: this bit can only be set when SPI or I^2S *is turned off.*
10	I^2SEN	I^2S enable 0: Disable I^2S. 1: Enable I^2S. *Note: not used in SPI mode.*
9:8	MODCFG	I^2S mode setting 00: Slave device sends. 01: Slave device receives. 10: Master device sends. 11: Master device receives. *Note: This bit can only be set when I^2S is turned off.* *Note: not used in SPI mode.*
7	PCMFSYNC	PCM frame synchronization 0: Short frame synchronization. 1: Long frame synchronization. *Note: This bit is only meaningful when SPI_I2SCFG.STDSEL = 11 (used by the PCM standard).* *Note: not used in SPI mode.*
6	Reserved	Reserved, the reset value must be maintained.
5:4	STDSEL	Selection of I^2S standard 00: I^2S Philips standard. 01: High byte alignment standard (left alignment). 10: Low byte alignment standard (right alignment). 11: PCM standard. See for details of I^2S standard on section 21.4.1. *Note: For correct operation, this bit can only be set when I^2S is turned off.* *Not used in SPI mode.*
3	CLKPOL	Static clock polarity 0: I2S clock static state is low level. 1: I2S clock static state is high level. *Note: For correct operation, this bit can only be set when I^2S is turned off.* *Note: not used in SPI mode.*
2:1	TDATLEN	Length of data to be transmitted 00: 16-bit data length. 01: 24-bit data length; 10: 32-bit data length; 11: Not allowed. *Note: For correct operation, this bit can only be set when I^2S is turned off.* *Note: not used in SPI mode.*

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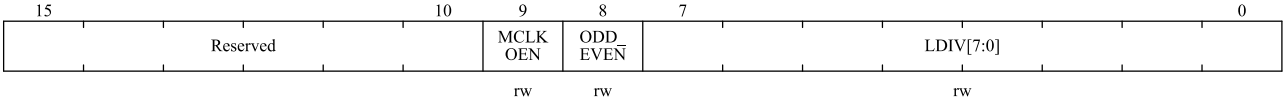
Bit field	Name	Description
0	CHBITS	Channel length (number of data bits per audio channel) 0: 16 bits wide; 1: 32 bits wide. Writing to this bit is meaningful only when SPI_I2SCFG.TDATLEN = 00, otherwise the channel length is fixed to 32 bits by hardware. *Note: For correct operation, this bit can only be set when I²S is turned off.* *Note: not used in SPI mode.*

21.5.10 SPI_I²S prescaler register (SPI_I2SPREDIV)

Address: 0x20

Reset value: 0x0002



Bit field	Name	Description
15:10	Reserved	Reserved, the reset value must be maintained.
9	MCLKOEN	Master clock output enable 0: Disable master clock output. 1: Enable master clock output. *Note: For correct operation, this bit can only be set when I²S is turned off.* *Note: not used in SPI mode.*
8	ODD _EVEN	Coefficient prescaler 0: actual frequency division coefficient = LDIV ×2. 1: actual frequency division coefficient = (LDIV × 2) + 1. See Section 21.4.2 for details. *Note: For correct operation, this bit can only be set when I²S is turned off. Use this bit only in I²S master mode.* *Not used in SPI mode.*
7:0	LDIV	I²S linear prescaler Setting LDIV [7:0] = 0 or LDIV [7:0] = 1 is prohibited. See Section 21.4.2 for details. *Note: For correct operation, this bit can only be set when I²S is turned off. Use this bit only in I²S master mode.* *Not used in SPI mode.*

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22 I²C interface

22.1 Introduction

I2C(Inter-Integrated Circuit) bus is a widely used bus structure, it has only two bidirectional lines, namely data bus SDA and clock bus SCL. All devices compatible with I2C bus can communicate directly with each other through I2C bus with these two lines.

I2C interface connects microcontroller and serial I2C bus, and can be used for communication between MCU and external I2C devices. It supports standard speed mode and fast mode, it supports CRC calculation and verification, SMBus (System Management Bus) and PMBus (Power Management Bus), it also provides multi-master function to control all I2C bus specific timing, protocol, arbitration. I2C interface module also supports DMA mode, which can effectively reduce the CPU overload.

22.2 Main Features

- Same interface can have both master function and slave function
- Parallel-bus to I²C protocol converter
- Supports 7-bit/10-bit address mode and broadcast addressing
- As I²C master, it can generate clock, start and stop signal
- As I²C slave, it supports address detection, stop bit detection function
- Support standard speed mode(up to 100 kHz) ,fast mode(up to 400kHz) and fast plus mode(up to 1MHz)
- Support interrupt vector, byte transfer successfully interrupt and error event interrupt
- Optional clock extending function
- Support DMA mode
- Optional PEC (Packet Error Check) generation and verification
- Compatible with SMBus 2.0 and PMBus

Note: not all of the above features are included in all products. Please refer to the relevant data manual to confirm the I²C functions supported by the product.

22.3 Function Description

I2C interface is connected to I2C bus through data pin (SDA) and clock pin (SCL) to communicate with external devices. It can be connected to standard (up to 100kHz) or fast (up to 400kHz) I2C bus. I2C module converts data from serial to parallel when receiving, and converts data from parallel to serial when sending. It support interrupt mode, users can enable or disable interrupt according to their needs.

22.3.1 SDA and SCL Line Control

I2C module has two interface lines: serial data line (SDA) and serial clock line (SCL). Devices connected to the bus and transmit information to each other through these two wires. SDA and SCL are two-way wires, it should connected

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to a current source or the positive of the power supply with a pull-up resistor. When the bus is idle, both lines are high level. The output of device which is connected to the bus must have open drain or open collector to provide wired-AND functionality. The data on I2C bus can reach 100 kbit/s in standard mode and 400kbit/s in fast mode. Since devices of different processors may be connected to the I2C bus, the levels of logic '0' and logic '1' are not fixed and depend on the actual level of VDD.

If the clock extending is allowed, the SCL line is pulled down which can be avoided the overload error during receiving and the under load error during transmission.

For example, when in the transmission mode, if the transmit data register is empty and the byte transmit end bit is set (I2C_STS1.TXDATE = 1, I2C_STS1.BSF = 1), the I2C interface keeps the clock line low before transmission to wait for the software to read STS1 and write the data into the data register (both buffer and shift register are empty); when In the receive mode, if the data register is not empty and the byte sending end bit is set (I2C_STS1.RXDATNE = 1, I2C_STS1.BSF = 1), the I2C interface keeps the clock line low after receiving the data byte, waiting for the software to read STS1, and then read the data register(buffer and shift register are full).

If clock extending is disable in slave mode, if the receive data register is not empty (I2C_STS1.RXDATNE = 1) in the receive mode, and the data has not been read before receiving the next byte, an overrun error will issue and the last word byte will be discarded. In transmit mode, if the transmit data register is empty (I2C_STS1.TXDATE = 1), no new data is written into the data register before the next byte must be sent, an underrun error will issue. The same byte will be send repeatedly. In this case, duplicate write conflicts are not controlled.

22.3.2 Software Communication Process

The data transmission of I2C device is divided into master and slave. Master is the device responsible for initializing the transmission of data on the bus and generating clock signal. At this time, any addressed device is a slave. Whether the I2C device is a master or a slave, it can send or receive data. Therefore, the I2C interface supports four operation modes:

- Slave transmitter mode
- Slave receiver mode
- Master transmitter mode
- Master receiver mode

After system reset, I2C works in slave mode by default. The I2C interface is configured by software to send a start bit on the bus, and then the interface automatically switches from the slave mode to the master mode. When arbitration is lost or a stop signal is generated, the interface will switched to the slave mode from the receive mode.

The block diagram of I^2C interface is shown in the figure below.

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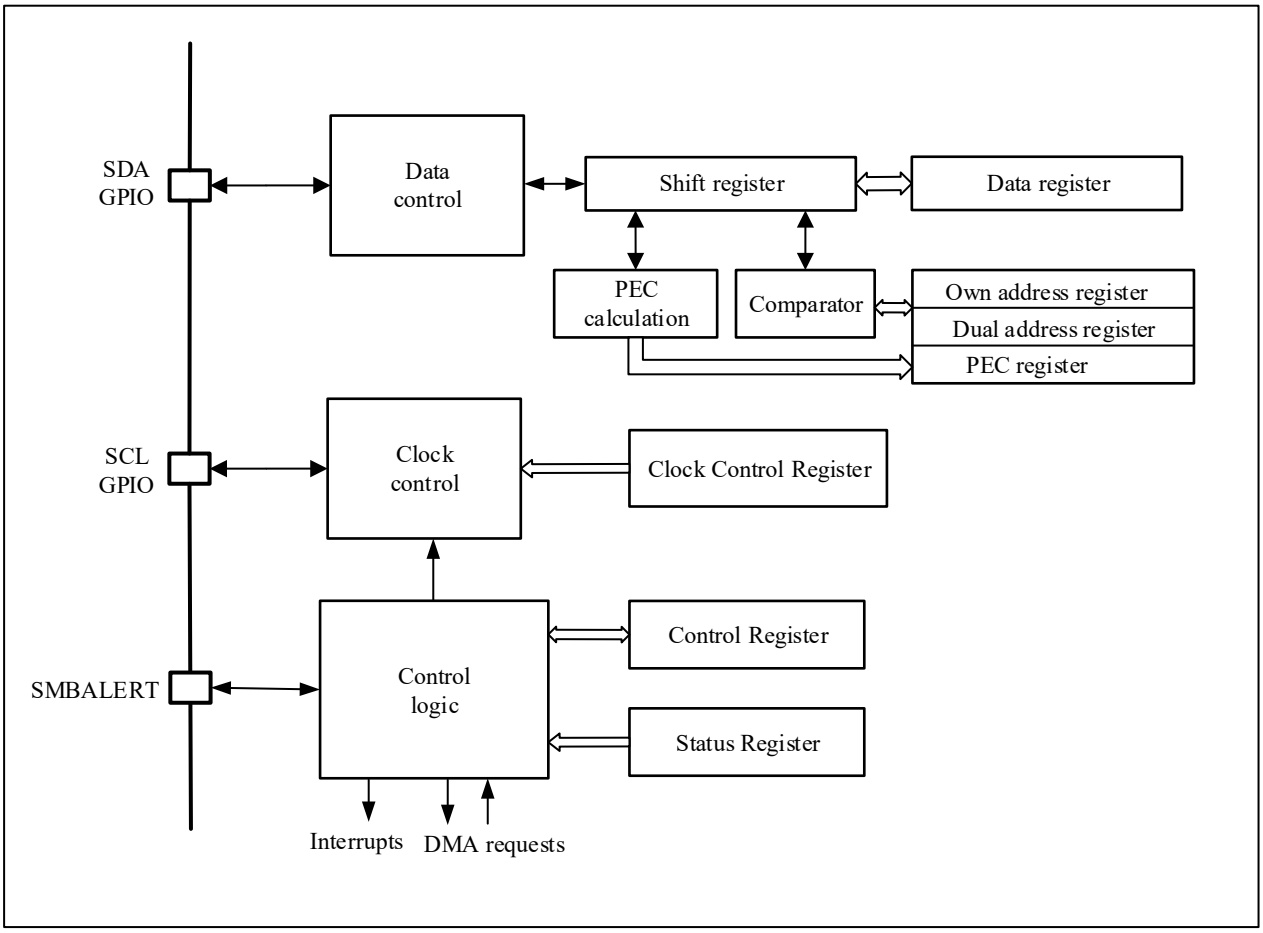
Figure 22-1 I²C functional block diagram

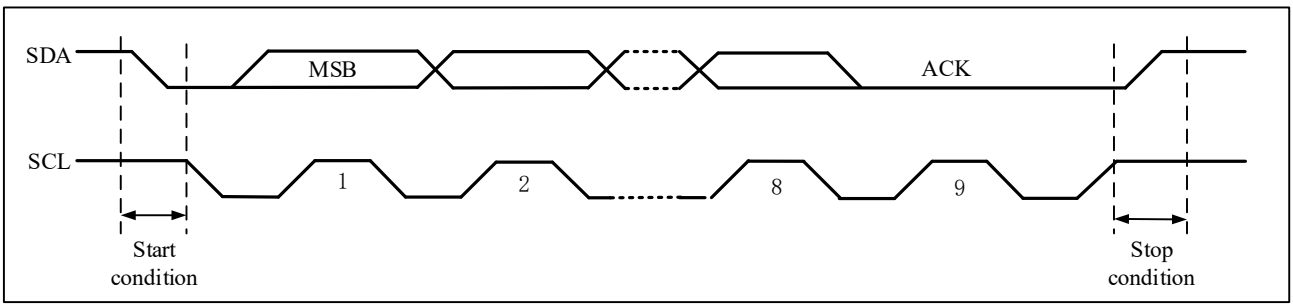


Note: in SMBus mode, SMBALERT is an optional signal. If SMBus is disabled, the signal cannot be used

22.3.2.1 Start and stop conditions

All data transfers always start with the start bit and end with the stop bit. The start and stop conditions are generated by software in the master mode. Start bit is a level conversion from high to low on SDA line when SCL is high. Stop bit is a level transition from low to high on SDA line when SCL is high. as shown in the figure below.

Figure 22-2 I2C bus protocol



22.3.2.2 Clock synchronization and Arbitration

The I2C module supports multi-master arbitration, which means two masters can initiate an I2C START operation

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concurrently when the bus is inactive. So some mechanisms are needed to grant a master the access to the bus. This process is generally named Clock Synchronization and Arbitration.

I2C module has two key features:

- SDA and SCL are drain open circuit structures, and the signal "wire-and" logic is realized through an external pull-up resistor.
- SDA and SCL pins will also detect the level on the pin while outputting the signal to check whether the output is consistent with the previous output. This provides the hardware basis for "Clock Synchronization" and "Bus Arbitration".

The I2C device on the bus is to output logic 0 by "grounding the line". Based on the characteristics of the I2C bus, if one device sends logic 0 and the other sends logic 1, then the line sees only logic 0, so there is no possibility of level conflicts on the line.

The physical connection of the bus allows the master to read data while writing data to the bus. In this way, when two masters are competing for the bus, the one that sends logic 0 does not know the occurrence of the competition. Only the one that sends logic 1 will find the conflict (when writing a logic 1, but read 0) and exit the competition.

Clock synchronization

The high-to-low switching of the SCL line causes the devices to begin counting their low-level periods, and once the device's clock goes low, it keeps the SCL line in this state until the high-level of the clock is reached. However, if another clock is still in the low period, the low-to-high switch of this clock will not change the state of the SCL line. Therefore, the SCL line is kept low by the device with the longest low-level period. A device with a short low-level period will enter a high-level wait state.

When all related devices have counted their low-level periods, the clock line is released and goes high-level, after which there is no difference in the state of the device clock and SCL lines, and all devices will begin counting their high-level periods, the device that completes the high-level period first will pull the SCL line low again.

In this way, the low-level period of the generated synchronous SCL clock is determined by the device with the longest low-level clock period, and the high-level period is determined by the device with the shortest high-level clock period.

Arbitration

Arbitration, like synchronization, is to resolve bus control conflicts in the case of multiple masters. The arbitration process has nothing to do with the slave. When the two masters both produce a valid start bit when the bus is idle, in this case, it is necessary to decide which master will complete the data transmission. This is the process of arbitration.

Each master controller does not have the priority level of controlling the bus, which is all determined by arbitration. The bus control is determined and carried out bit by bit. They follow the principle of "low level first", that is, whoever sends the low level first will control the bus. During the arbitration of each bit, when SCL is high, each host checks whether its own SDA level is the same as that sent by itself. In theory, if the content transmitted by two hosts is exactly the same, then they can successfully transmit without errors. If a host sends a high level but detects that the SDA line is low, it considers that it has lost arbitration and shuts down its SDA output driver, while the other host continues to complete its own transmission.

22.3.2.3 I2C data communication flow

Each I2C device is identified by a unique address. According to the device function, they can be either a transmitter or a receiver.

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The I2C host is responsible for generating the start bit and the end bit in order to start and end a transmission. And is responsible for generating the SCL clock.

The I2C module supports 7-bit and 10-bit addresses, and the user can configure the address of the I2C slave through software. After the I2C slave detects the start bit on the I2C bus, it starts to receive the address from the bus, and compares the received address with its own address. Once the two addresses are matched, the I2C slave will send an acknowledgement (ACK) and respond to subsequent commands on the bus: send or receive the requested data. In addition, if the software opens a broadcast call, the I2C slave always sends a confirmation response to a broadcast address (0x00).

Data and address are transmitted in 8-bit width, with the most significant bit first. The 1 or 2 bytes following the start condition is the address (1 byte in 7-bit mode, 2 bytes in 10-bit mode). The address is only sent in master mode. During the 9th clock period after 8 clocks of a byte transmission, the receiver must send back an acknowledge bit (ACK) to the transmitter, as shown in the Figure 22-2 I2C bus protocol.

Software can enable or disable acknowledgement (ACK), and can set the I2C interface address (7-bit, 10-bit address or general call address).

22.3.2.4 I2C slave transmission mode

In slave mode, the transmission reception flag bit (I2C_STS2.TRF) indicates whether it is currently in receiver mode or transmission mode. When sending data to I2C bus in transmission mode, the software should follow the following steps:

1. First, enable I2C peripheral clock and configure the clock related register in I2C_CTRL1, ensuring the correct I2C timing. After these two steps are completed, I2C runs in slave mode, waiting for receiving start bit and address.
2. I2C slave receives a start bit first, and then receives a matching 7-bit or 10-bit address. I2C hardware will set the I2C_STS1.ADDRF(received address and matched its own address). The software should monitor this bit regularly or have an interrupt to monitor this bit. After this bit is set, the software reads I2C_STS1 register and then read I2C_STS2 register to clear the I2C_STS1.ADDRF bit. If the address is in 10 bit format, the I2C master should then generate a START and send an address header to the I2C bus. After detecting START and the following address header, the slave will continue to set I2C_STS1.ADDRF bit. The software continues to read I2C_STS1 register and read I2C_STS2 register to clear the I2C_STS1.ADDRF bit a second time.
3. I2C enters the data sending state, and now shift register and data register I2C_DAT are all empty, so the hardware will set the I2C_STS1.TXDATE(send data empty). At this time, the software can write the first byte data to I2C_DAT register, however, because the byte of the I2C_DAT register is immediately moved into the internal shift register, the I2C_STS1.TXDATE bit is not cleared to zero. When the shift register is not empty, I2C starts to send data to I2C bus.
4. During the sending of the first byte, the software writes the second byte to I2C_DAT, neither the I2C_DAT register nor the shift register is empty. The I2C_STS1.TXDATE bit is cleared to 0.
5. After the first byte is sent, I2C_STS1.TXDATE is set again, and the software writes the third byte to I2C_DAT, the same time, the I2C_STS1.TXDATE bit is cleared.After that, as long as there is still data to be sent and I2C_STS1.TXDATE is set to 1, the software can write a byte to I2C_DAT register.
6. During the sending of the second last byte, the software writes the last data to the I2C_DAT register to clear the I2C_STS1.TXDATE flag bit, and then the I2C_STS1.TXDATE status is no longer concerned.

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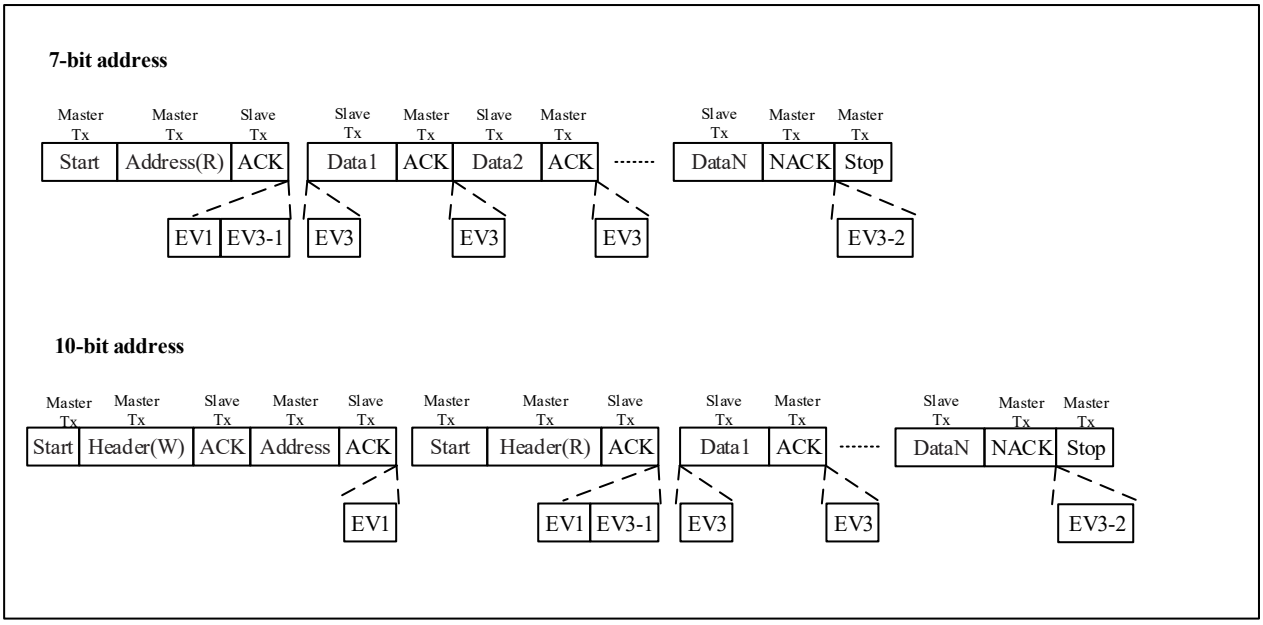
I2C_STS1.TXDATE bit is set after the second last byte is sent until the stop end bit is detected.

7. According to the I2C protocol, the I2C master will not send a ACK to the last byte received. Therefore, after the last byte is sent, the I2C_STS1.ACKFAIL bit (acknowledge fail) of the I2C slave will be set to notify the software of the end of sending. The software writes 0 to the I2C_STS1.ACKFAIL bit to clear this bit.

Figure 22-3 Slave transmitter transfer sequence diagram



Instructions：

1. EV1: I2C_STS1.ADDRF = 1, read STS1 and then STS2 register to clear the event.
2. EV3-1: I2C_STS1.TXDATE=1, shift register is empty, data register is empty, write DAT.
3. EV3: I2C_STS1.TXDATE=1, shift register is not empty, data register is empty, write DAT will clear the event.
4. EV3-2: I2C_STS1.ACKFAIL=1, ACKFAIL bit of STS1 register write "0" to clear the event.

Note: a) EV1 and EV3_1 event prolongs the low SCL time until the end of the corresponding software sequence.

b) The software sequence of EV3 must be completed before the end of the current byte transfer.

22.3.2.5 I2C slave receiving mode

When receiving data in slave mode, the software should operate as follows:

1. First, enable I2C peripheral clock and configure the clock related register in I2C_CTRL1 ensuring the correct I2C timing. After these two steps are completed, I2C runs in slave mode, waiting for receiving start bit and address.
2. After receiving the START condition and the matched 7-bit or 10-bit address, I2C hardware will set I2C_STS1.ADDRF bit(the address received and matched with its own address) to 1. This bit should be detected by software polling or interrupt. After it is found that it is set, the software clears the I2C_STS1.ADDRF bit by reading I2C_STS1 register first and then I2C_STS2 register. Once the I2C_STS1.ADDRF bit is cleared,The I2C slave starts to receive data from the I2C bus.
3. When the first byte is received, the I2C_STS1.RXDATNE bit (the received data is not empty) is set to 1 by hardware. If the I2C_CTRL2.EVTINTEN and I2C_CTRL2.BUFINTEN bits are set, an interrupt is generated.

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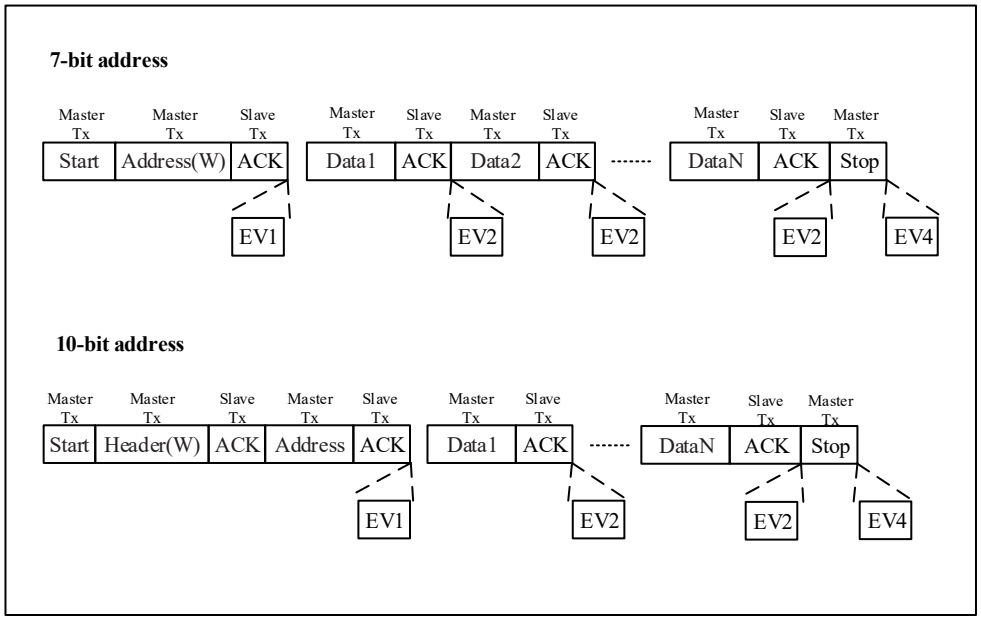
The software should check this bit by polling or interrupt. Once it is found that it is set, the software can read the first byte of I2C_DAT register, and then the I2C_STS1.RXDATNE bit is cleared to 0. Note that if the I2C_CTRL1.ACKEN bit is set, after receiving a byte,the slave should generate a response pulse.

4. At any time, as long as the I2C_STS1.RXDATNE bit is set to 1, the software can read a byte from the I2C_DAT register. When the last byte is received, I2C_STS1.RXDATNE is set to 1 and the software reads the last byte.

5. When the slave detects the STOP bit on I2C bus, set I2C_STS1.STOPF to 1, and if the I2C_CTRL2.EVTINTEN bit is set, an interrupt will be generated. The software clears the I2C_STS1.STOPF bit by reading the I2C_STS1 register before writing the I2C_CTRL1 register (see EV4 in the following figure).

Figure 22-4 Slave receiver transfer sequence diagram



Instructions：

1. EV1: I2C_STS1.ADDRF = 1, read STS1 and then STS2 to clear the event.

2. EV2: I2C_STS1.RXDATNE =1, reading DAT will clear this event.

3. EV4: I2C_STS1.STOPF=1, reading STS1 and then writing the CTRL1 register will clear this event.

Note: a)EV1 event prolongs the time when SCL is low until the end of the corresponding software sequence.

b) The software sequence of EV2 must be completed before the end of the current byte transmission.

22.3.2.6 I2C master transmission mode

In the master mode, the I2C interface starts data transmission and generates a clock signal. Serial data transmission always starts with a start condition and ends with a stop condition. When the START condition is generated on the bus through the start bit, the device enters the master mode.

When sending data to I2C bus in master mode, the software should operate as follows:

1. First, enable the I2C peripheral clock, and configure the clock-related registers in I2C_CTRL1 to ensure the correct I2C timing. When these two steps are completed, I2C runs in the slave mode by default, waiting for receiving the start bit and address.

2. When BUSY=0, I2C_CTRL1.STARTGEN bit set to 1, and the I2C interface will generate a start condition and

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switch to the master mode (I2C_STS2.MSMODE bit set to “1”).

3. Once the start condition is issued, I2C hardware will set I2C_STS1.STARTBF bit(START bit flag)and then enters the master mode. If the I2C_CTRL2.EVTINTEN bit is set, an interrupt will be generated. Then the software reads the I2C_STS1 register and then writes a 7-bit address bit or a 10-bit address bit with an address header to the I2C_DAT register to clear the I2C_STS1.STARTBF bit. After the I2C_STS1.STARTBF bit is cleared to 0, I2C starts sending addresses or address headers to I2C bus.

   In 10-bit address mode, sending a header sequence will generate the following events:

   – I2C_STS1.ADDR10F bit is set by hardware, and if I2C_CTRL2.EVTINTEN bit is set, an interrupt is generated. Then the master reads the STS1 register, and then writes the second address byte into the DAT register.

   – I2C_STS1.ADDRF bit is set by hardware, and if I2C_CTRL2.EVTINTEN bit is set, an interrupt is generated. Then the master reads the STS1 register, followed by the STS2 register.

   Note: In the transmitter mode, the master device first sends the header byte (11110xx0) and then sends the lower 8 bits of the slave address. (where xx represents the highest 2 bits of the 10-bit address).

   In the 7-bit address mode, only one address byte needs to be sent out. Once the address byte is sent out:

   – I2C_STS1.ADDRF bit is set by hardware, and if I2C_CTRL2.EVTINTEN bit is set, an interrupt is generated. Then the master device waits for reading the STS1 register once, followed by reading the STS2 register.

   Note: In the transmitter mode, when the master sends the slave address, set the lowest bit to "0".

   In 7-bit address mode, don’t set the slave address to 0xF0 to prevent the I2C_STS1.ADDR10F bit from being set by hardware.

4. After the 7-bit or 10-bit address bit is sent, the I2C hardware sets the I2C_STS1.ADDRF bit (address has been sent) to 1, if the I2C_CTRL2.EVTINTEN bit is set, an interrupt is generated, and the software is cleared by reading the I2C_STS1 register and then the I2C_STS2 register I2C_STS1.ADDRF.

5. I2C enters the data transmission state. Because the shift register and the data register (I2C_DAT) are empty, the hardware sets the I2C_STS1.TXDATE bit (transmission data empty) to 1, and then the software writes the first byte of data to the I2C_DAT register, but because the byte written into the I2C_DAT register is immediately moved into the internal shift register, the I2C_STS1.TXDATE bit will not be cleared at this time. Once the shift register is not empty, I2C starts sending data to the bus.

6. During the transmission of the first byte, the software writes the second byte to I2C_DAT, and I2C_STS1.TXDATE is cleared at this time. At any time, as long as there is data waiting to be sent and the I2C_STS1.TXDATE bit is set to 1, the software can write a byte to the I2C_DAT register.

7. In the process of sending the penultimate byte, the software writes the last byte of data to I2C_DAT to clear the I2C_STS1.TXDATE flag bit. After that, there is no need to care about the status of the I2C_STS1.TXDATE bit. The I2C_STS1.TXDATE bit will be set after the penultimate byte is sent, and will be cleared when the stop bit (STOP) is sent.

8. After the last byte is sent, because the shift register and the I2C_DAT register are empty at this time, the I2C host sets the I2C_STS1.BSF bit (byte transmission end), and the I2C interface will keep SCL low before clearing the I2C_STS1.BSF bit. After reading I2C_STS1, writing to the I2C_DAT register will clear the I2C_STS1.BSF

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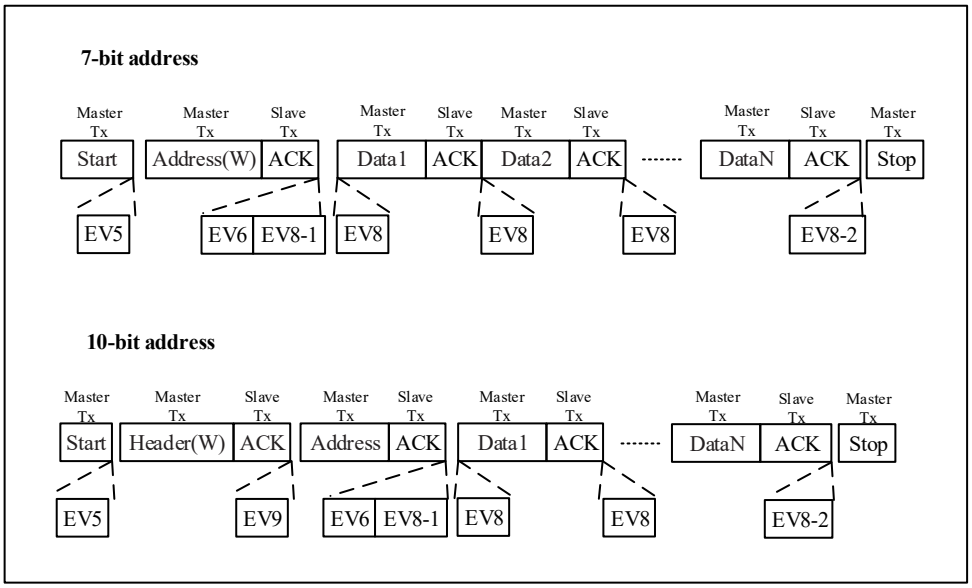
bit. The software sets the I2C_CTRL1.STOPGEN bit at this time to generate a stop condition, and then the I2C interface will automatically return to the slave mode (I2C_STS2.MSMODE bit is cleared).

Figure 22-5 Master transmitter transfer sequence diagram



Instructions：

1. EV5: I2C_STS1.STARTBF = 1, reading STS1 and writing the address to the DAT register will clear the event.
2. EV6: I2C_STS1.ADDRF = 1, read STS1 and then STS2 to clear the event.
3. EV8_1: I2C_STS1.TXDATE = 1, shift register is empty, data register is empty, write DAT register.
4. EV8: I2C_STS1.TXDATE = 1, shift register is not empty, data register is empty, write to DAT register will clear the event.
5. EV8_2: I2C_STS1.TXDATE = 1, I2C_STS1.BSF = 1, request to set stop bit. These two events are cleared by the hardware when a stop condition is generated.
6. EV9: I2C_STS1.ADDR10F = 1, read STS1 and then write to DAT register to clear the event.

Notes:

(1) EV5, EV6, EV9, EV8_1 and EV8_2 event prolonged the low SCL time until the end of the corresponding software sequence.

(2) The software sequence of EV8 must be completed before the end of the current byte transfer.

(3) When I2C_STS1.TXDATE or I2C_STS1.BSF bit is set, stop condition should be arranged when EV8_2 occurs.

22.3.2.7 I2C master receiving mode

In master mode, software receiving data from I2C bus should follow the following steps:

1. First, enable the I2C peripheral clock and configure the clock-related registers in I2C_CTRL1, in order to ensure that the correct I2C timing is output. After enabling and configuring, I2C runs in slave mode by default, waiting to receive the start bit and address.
2. When BUSY=0, set the I2C_CTRL.STARTGEN bit, and the I2C interface will generate a start condition and

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switch to the master mode (I2C_STS2.MSMODE bit is set to 1).

3. Once the start condition is issued, the I2C hardware sets I2C_STS1.STARTBF(start bit flag) and enters the host mode. If the I2C_CTRL2.EVTINTEN bit is set to 1, an interrupt will be generated. Then the software reads the I2C_STS1 register and then writes a 7-bits address or a 10-bits address with an address header to the I2C_DAT register, in order to clear the I2C_STS1.STARTBF bit. After the I2C_STS1.STARTBF bit is cleared to 0, I2C begins to send the address or address header to the I2C bus.

   In 10-bits address mode, sending a header sequence will generate the following events:

   – The I2C_STS1.ADDR10F bit is set to 1 by hardware, and if the I2C_CTRL2.EVTINTEN bit is set to 1, an interrupt will be generated. Then the master device reads the STS1 register, and then writes the second byte of address into the DAT register.

   – The I2C_STS1.ADDRF bit is set to 1 by hardware, and if the I2C_CTRL2.EVTINTEN bit is set to 1, an interrupt will be generated. Then the master device reads the STS1 register and the STS2 register in sequence.

   Note: In the receiver mode, the master device sends the header byte (11110xx0) firstly, then sends the lower 8 bits of the slave address, and then resends a start condition followed by the header byte (11110xx1) (where xx represents the highest 2 digits of the 10-bits address).

   In the 7-bits address mode, only one address byte needs to be sent, once the address byte is sent:

   – The I2C_STS1.ADDRF bit is set to 1 by hardware, and if the I2C_CTRL2.EVTINTEN bit is set to 1, an interrupt will be generated. Then the master device waits to read the STS1 register once, and then reads the STS2 register.

   Note: In the receiving mode, the master device sets the lowest bit as '1' when sending the slave address.

   In 7-bit address mode, don't set the slave address to 0xF0 to prevent the I2C_STS1.ADDR10F bit from being set by hardware.

4. After the 7-bits or 10-bits address is sent, the I2C hardware sets the I2C_STS1.ADDRF bit (address has been sent) to 1. If the I2C_CTRL2.EVTINTEN bit is set to 1, an interrupt will be generated. The software clears the I2C_STS1.ADDRF bit by reading the I2C_STS1 register and the I2C_STS2 register in sequence. If in the 10-bit address mode, software should set the I2C_CTRL1.STARTGEN bit again to regenerate a START. After the START is generated, the I2C_STS1.STARTBF bit will be set. The software should clear the I2C_STS1.STARTBF bit by reading I2C_STS1 firstly and then writing the address header to I2C_DAT, and then the address header is sent to the I2C bus, I2C_STS1.ADDRF is set to 1 again. The software should clear the I2C_STS1.ADDRF bit again by reading I2C_STS1 and I2C_STS2 in sequence.

5. After sending the address and clearing the I2C_STS1.ADDRF bit, the I2C interface enters the host receiving mode. In this mode, the I2C interface receives data bytes from the SDA line and sends them to the DAT register through the internal shift register. Once the first byte is received, the hardware will set the I2C_STS1.RXDATNE bit (not empty flag bit of received data) to 1, and if the I2C_CTRL1.ACKEN bit is set to 1, an acknowledge pulse will be sent. At this time, the software can read the first byte from the I2C_DAT register, and then the I2C_STS1.RXDATNE bit is cleared to 0. After that, as long as I2C_STS1.RXDATNE is set to 1, the software can read a byte from the I2C_DAT register.

6. The master device sends a NACK after receiving the last byte from the slave device. After receiving the NACK,

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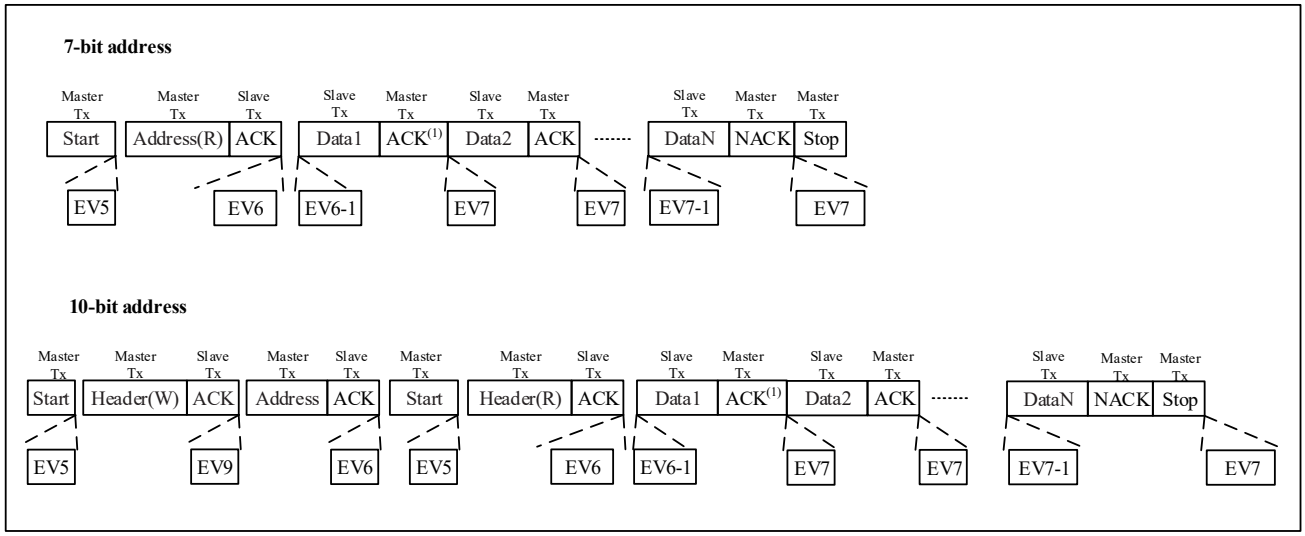
the slave device releases the control of SCL and SDA lines; the master device can send a stop/restart condition. In order to generate a NACK pulse after receiving the last byte, the software should clear the I2C_CTRL1.ACKEN bit immediately after receiving the penultimate byte (N-1). In order to generate a stop/restart condition, the software must set the I2C_CTRL1.STOPGEN bit or I2C_CTRL1.STARTGEN to 1 after reading the penultimate data byte. This process needs to be completed before the last byte is received to ensure that the NACK is sent for the last byte.

7. After the last byte is received, the I2C_STS1.RXDATNE bit is set to 1, and the software can read the last byte. Since I2C_CTRL1.ACKEN has been cleared to 0 in the previous step, I2C no longer sends ACK for the last byte, and generates a STOP bit after the last byte is sent.

Note: The above steps require the number of bytes N>1. If N=1, step 6 should be executed after step 4, and it needs to be completed before the reception of byte is completed.

Figure 22-6 Master receiver transfer sequence diagram



Instructions:

1. EV5: I2C_STS1.STARTBF=1, reading STS1 and then writing the address into the DAT register will clear this event.
2. EV6: I2C_STS1.ADDRF=1, reading STS1 and STS2 in sequence will clear this event. In the 10-bits master receiving mode, the I2C_CTRL1.STARTGEN should be set to 1 after this event.
3. EV6_1: There is no corresponding event flag, only suitable for receiving 1 byte. Just after EV6 (that is after clearing I2C_STS1.ADDRF), the generation bits for acknowledge and stop condition should be cleared.
4. EV7: I2C_STS1.RXDATNE=1, read the DAT register to clear this event.
5. EV7_1: I2C_STS1.RXDATNE =1, read the DAT register to clear this event. Set I2C_CTRL1.ACKEN=0 and I2C_CTRL1.STOPGEN=1.
6. EV9: I2C_STS1.ADDR10F=1, reading STS1 and then writing to the DAT register will clear this event.

Notes:

(1) If a single byte is received, it is NA.

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(2) EV5, EV6, and EV9 events extend the low level of SCL until the corresponding software sequence ends.

(3) The EV7 software sequence shall be completed before the end of the current byte transmission.

(4) The software sequence of EV6_1 or EV7_1 shall be completed before the ACK pulse of the current transmission byte.

22.3.3 Error Conditions Description

I2C errors mainly include bus error, acknowledge error, arbitration loss, overload\ underload error. These errors may cause communication failure.

22.3.3.1 Acknowledge Failure (ACKFAIL)

The interface have a acknowledge bit is detected that does not match the expectation, it will occurs acknowledge fail error, I2C_STS1.ACKFAIL bit is set. An interrupt occurs, when I2C_CTRL2.ERRINTEN bit is set to 1.

When transmitter receives a NACK, The communication must be reset: Device in slave mode, hardware release the bus; Device in master mode, it must generate a stop condition from software.

22.3.3.2 Bus Error (BUSERR)

when address or data is transmissing,I2C interface receive external stop or start condition,it will happen a bus error, I2C_STS1.BUSERR bit is set. An interrupt occurs, when I2C_CTRL2.ERRINTEN bit is set to 1.

I2C device as master, the hardware does not release bus, as the same time it done not affect the current status of transfer, The current transfer will determined by software whether suspend.

I2C device as slave, when data is discarded in transmission and the bus releases by hardware, it will have two situation: If an error start condition is detected, the slave device considers a restart condition and waits for an address or a stop condition. If an error stop condition is detected, the slave device operates as a normal stop condition and the hardware releases the bus.

22.3.3.3 Arbitration Lost (ARLOST)

The interface have arbitration lost is detected, hardware release the bus, it will occurs arbitration lost error, I2C_STS1.ARLOST bit is set. An interrupt occurs, when I2C_CTRL2.ERRINTEN bit is set to 1.

I2C interface will go to slave mode automatically(I2C_STS2.MSMODE bit is cleared). When the I2C interface lost the arbitration, in the same communication, it can not respond to its slave address, but it can respond when master win the bus retransmits a start signal. Hardware release the bus.

22.3.3.4 Overrun/Underrun Error (OVERRUN)

In slave mode, disable clock extend prone to Overrun/Underrun Error:

When I2C interface is receiving data (I2C_STS1.RXDATNE=1, data have received in register), and I2C_DAT register still have previous byte has not been read, it will occurs an overrun error. In this situation, the last received data is discarded. And software should clear I2C_STS1.RXDATNE bit, transmitter retransmit last byte.

When I2C interface is sending data (I2C_STS1.TXDATE=1, new data have not sending to register), and I2C_DAT register still empty, it will occurs an underrun error. In this situation, the previous byte in the I2C_DAT register is sending repeatedly. And User make sure that in the event of an underrun error, the receiver discard repeatedly byte, and transmitter should update the I2C_DAT register at the specified time according to the I2C bus standard.

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In sending the first byte, I2C_DAT register must be written after I2C_STS1.ADDRF bit is cleared and the before the first SCL rising edge. If cannot make sure do that, the first byte should be discard by receiver.

22.3.4 DMA Application

DMA can generate a requests when transfer data register empty or full. DMA can oprate write data to I2C or read data from I2C reduce burden of CPU.

Before transfer current byte at the end DMA requests must be answered. If set the DMA channel transfer data is done, DMA will send EOT(End Of Transmission) to I2C, and ocurrs a interrupt when enable interrupt bit.

In the master transfer mode, in EOT interrupt handler DMA request need to be disbale, and set stop condition after waiting for I2C_STS1.BSF event.

In the master receive mode, the data of received is great than or equal to 2, DMA will send a hardware signal EOT_1 in DMA transmission(byte number-1). If set I2C_CTRL2.DMALAST bit, when hardware have send the EOT_1 next byte it will send a NACK automatically. The user can set a stop condition in the interrupt handler after the DMA transfer is completed if interrupt enable.

Note: When I2C and other peripherals use the same DMA controller, they cannot be turned on at the same time.

22.3.4.1 Transmit process

If use the DMA mode need set the I2C_CTRL2.DMAEN bit. When I2C_STS1.TXDATE bit is set, the data will send to I2C_DAT from storage area by the DMA. DMA assign a channle for I2C transmission, (x is the channel number) the following step must be opreate:

1. In the DMA_PADDRx register set the I2C_DAT register address. Data will be send to address in every I2C_STS1.TXDATE event.
2. In the DMA_MADDRx register set the memory address. Data will send to I2C_DAT address in every I2C_STS1.TXDATE event.
3. In the DMA_TXNUMx register set the number of need to be transferred.In every I2C_STS1.TXDATE event this number-1 until 0.
4. In the DMA_CHCFGx register set PRIOLVL[1:0] bit to configure the priority of channel.
5. In the DMA_CHCFGx register set DIR bit to configure when ocurrs an interrupt whether send a half data or all completed.
6. In the DMA_CHCFGx register set CHEN bit to enable transfer channel.
7. When DMA transfer data is done, DMA need send a EOT/EOT_1 signal to I2C indicate this transfer is done. If interrupt is enable, DMA ocurrs a interrrupt.

Note: if DMA is used for transmission, do not set I2C_CTRL2.BUFINTEN bit.

22.3.4.2 Receive process

If use DMA mode need set I2C_CTRL2.DMAEN bit. When data byte is received,DMA will send I2C data to storage area, set DMA channel for I2C reception. The following steps must be opreate:

1. In DMA_PADDRx register set the address of the I2C_DAT register. In every I2C_STS1.RXDATEN event, data will send from address to storage area.

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2. In DMA_MADDRx register set the memory area address. In every I2C_STS1.RXDATEN event,data will send from I2C_DAT register to storage area.
3. In DMA_TXNUMx register set the number of need to be transferred. In every I2C_STS1.RXDATEN event the number-1 until 0.
4. In DMA_CHCFGx register set PRIOLVL[0:1] to configure the priority of channel.
5. In DMA_CHCFGx register clear DIR to configure when ocurrs a interrupt request whether received half data or all data is received.
6. In the DMA_CHCFGx register set CHEN bit to activate the channle.
7. When DMA tansfer data is done, DMA need to send EOT/EOT_1 signal to I2C indicate this transfer is done, if interrupt is enbale, DMA ocurrs a interrupt.

Note: If DMA is used for receiving, do not set I2C_CTRL2.BUFINTEN bit.

22.3.5 Packet Error Check

Setting the I2C_CTRL1.PECEN bit to 1 enables the PEC function. PEC uses CRC-8 algorithm to calculate all information bytes including address and read/write bits.it can improve the reliability of communication. The CRC-8 polynomial uses by the PEC calculator is $C(x) = x^8 + x^2 + x + 1$.

In transmit mode, software sets I2C_CTRL1.PEC transfer bit in the last I2C_STS1.TXDATE event, and then PEC will be transferred in the last byte. In receiving mode, software sets I2C_CTRL1.PEC transfer bit after the last I2C_STS1.RXDATNE event, and then receives the PEC byte and compares the received PEC byte to the internally calculated PEC value. If it is not equal to the internally calculated PEC value, the receiver needs to send a NACK. If it is host receiver mode, NACK will be sent after PEC regardless of the calculated result. It should pay attention that I2C_CTRL1.PEC bit has to be set before receiving.

If both DMA and PEC calculator are activated, I2C will automatically send or check the PEC value.

In transfer mode, when I2C interface receives EOT signal from DMA controller, it will automatically send PEC following the last byte. In receiving mode, when I2C interface receives an EOT_1 signal from DMA, it will automatically consider the next byte as PEC and compare it with the internally calculated PEC. It will happen a DMA request after receiving PEC.

In order to allow intermediate PEC transfer, I2C_CTRL2.DMALAST bit is used to determine whether it is the last DMA transfer. And if it does the last DMA request of the master receiver, NACK will be sent automatically after receiving the last byte.

When arbitration is lost, PEC calculation is invalid.

22.3.6 SMBus

22.3.6.1 Introduction

The System Management Bus(SMBus or SMB) is a dual-wire bus interface. Using SMBus can communicate with other device or other parts of the system, it able to commnicate with multiple devices without other independent control wire. SMBus base on I2C commincate standard. SMBus have a control bus for system and power management

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related tasks. If you want browse more information, please refer to the SMBus specification V2.0(http://smbus.org/specs/).

SMBus have three types of device standard.

- Master: device send command,generate clocks and stop transmmissions;
- Slave: device receive,respond to commands;
- Host: system have only one host. a device provides a master to system CPU. host have function of master and slave, it support SMBus alert protocol.

SMBus is a subset of the data transmission format of the I2C specification.

Similarities between SMBus and I2C:

- Both bus protocols contain of 2 wires (a clock wire SCL and a data wire SDA), with an optional SMBus alert wire.
- The data format is similar. SMBus data format is similar to 7-bit address format of I2C(See Figure 22-2).
- Both are master-slave communication modes, and the master device provides the clock.
- Both support multi master

Differences between SMBus and I2C:

Table 22-1 Comparison between SMBus and I2C

SMBus	I^2C
Maximum transmission speed 100kHz	Maximum transmission speed 1MHz
Minimum transmission speed 10kHz	No minimum transmission speed
Low clock timeout 35ms	No clock timeout
Fixed logic level	VDD determined logic level
Different address types (reserved, dynamic, etc.)	7-bit, 10-bit, and broadcast call slave address types
Different bus protocols (quick command, call handling, etc.)	No bus protocol

22.3.6.2 SMBus usage

SMBus uses the system management bus to meet lightweight communication requirements. In general, SMBus is commonly used on the computer motherboard. It is mainly used to transmit ON/OFF instructions for power unit and provide a control bus for system and power management-related tasks.

22.3.6.3 Device identification

On the SMBus, as a slave have a only address for any device, named slave address.

In order to distribute addres for each devices, it must have a unique device identifier(UDID) to distinguish devices.

22.3.6.4 Bus protocol

SMBus specification include eight bus protocols. If want browse the details on protocols or SMBus address types,it can refer to the SMBus specification v2.0(http://smbus.org/specs/). User's software can device what protocols are implemented.

Every packet through the SMBus complies with the SMBus protocol predefined format. SMBus is a subset of the data transfer format of I2C specification. As long as an I2C device can be accessed through one of the SMBus

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protocols, it is considered to be SMBus compliant.

Note: SMBus does not support Quick command protocol.

22.3.6.5 Address resolution protocol

The SMBus resolves address conflicts by dynamically assigning a new unique address to each slave device. This is the address resolution protocol(ARP) .

Any master device can connected bus to access all devices.

SMBus physical layer arbitration enable to distribute addresses.When device power on, the device's distribute address is not change, the protocol allows address retain when device power off.

When address is distributed, there is no extra SMBus packaging cost(the cost time that access distribute address device and access fixed address device is same).

22.3.6.6 Timeout function

A kind of feature related to timeout on SMBus: if it has taken too long time during the communication, it automatically resets the device. This is the reason why SMBus has a minimum transmission rate limitation -- to prevent the bus from locking up for a long time after the timeout occurs. I2C bus is essentially a "DC" bus, that is to say, if the slave is executing some subroutines and cannot respond in time while the master is accessing the slave, it can hold the clock. That can remind the host that the slave is busy but does not want to give up the current communication. This session can continue after the current task of the slave is over. I2c doesn't have a maximum limitation for the delay, but it is limited to 35ms in the SMBus system. According to the SMBus protocol, if a session takes too long, it means something is wrong with the bus, and all devices should be reset to eliminate this state. Like this, the slave device is not allowed to pull the clock down for too long. I2C_STS1.TIMOUT bit indicates the status of this feature.

22.3.6.7 SMBus alter mode

SMBus offer a optional interrupt signal SMBALERT(like SCL and SDA,is a wired-and signal) that devices uses to extend their control capabilities at expense of a pin. SMBus broadcast call address often combine with SMBALERT. There is 2 bytes message about SMBus.

A device which only has slave function can set I2C_CTRL1.SMBALERT bit to indicate it want to communicate with host. The host handles the interrupt and accesses all SMBALERT devices through the ARA (Alert Response Address, address value 0001100x). Only those devices that pull SMBALERT low can respond to ARA. This state is identified by the I2C_STS1.SMBALERT. The 7-bit device address provided from the sending device is placed on the 7 most significant bits of the byte, the eighth bit can be either '0' or '1'.

When more than one device's SMBALERT is low, the highest priority(The smaller the address, the higher the priority) can win bus communication through the standard arbitration during address transmission. If confirming the slave address, device's SMBALERT is no longer pulled low. If message transmitted completely,device's SMBALERT still is low,it mean host will read ARA again. The host can periodically access the ARA when the SMBALERT signal is not used.

22.3.6.8 SMBus communication process

The communication process on SMBus is similar to that on I2C.To use the SMBus mode, you need to configure SMBus specific registers in the program, respond and process SMBus specific flag, to implement the upper-layer protocols described in the SMBus manual.

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1. At first, set I2C_CTRL1.SMBMODE bit, and configure I2C_CTRL1.SMBTYPE bit and I2C_CTRL1.ARPEN bit according to the application requirements. If I2C_CTRL1.ARPEN=1 and I2C_CTRL1.SMBTYPE=0, use the default address of the SMB device. If I2C_CTRL1.ARPEN=1 and I2C_CTRL1.SMBTYPE=1, use the SMB master header field.
2. In order to support ARP (I2C_CTRL1.ARPEN=1), in SMBus host mode (I2C_CTRL1.SMBTYPE=1), software needs to respond to the I2C_STS2.SMBHADDR bit (in SMBus slave mode, respond to I2C_STS2.SMBDADDR bit) and implement the functions according to the ARP protocol.
3. To support the SMBus warning mode, software should respond to the I2C_STS1.SMBALERT bit and implement the corresponding functions.

22.4 Debug Mode

When the microcontroller enters the debug mode (Cortex-M4 core is in the stop state), configure the DBG_CTRL.I2CxSMBUS_TIMEOUT bit in the DBG module, Select SMBUS timeout to continue normal work or stop. See section 29.3.2 for details.

22.5 Interrupt Request

All I2C interrupt requests are listed in the following table.

Table 22-2 I²C interrupt request

Interrupt function	Interrupt event	Event flag	Set control bit
I2C event interrupt	Start bit sent (master)	STARTBF	EVTINTEN
	Address sent (master) or address matched (slave)	ADDRF	
	10-bit header sent (master)	ADDR10F	
	Received stop (slave)	STOPF	
	Data byte transfer completed.	BSF	
	Receive buffer is not empty.	RXDATNE	EVTINTEN and BUFINTEN
	Send buffer is empty.	TXDATE	
I2C error interrupt	Bus error	BUSERR	ERRINTEN
	Lost arbitration (master)	ARLOST	
	Acknowledge fail	ACKFAIL	
	Overrun/underrun	OVERRUN	
	PEC error	PECERR	
	Timeout /Tlow error	TIMOUT	
	SMBus Alert	SMBALERT	

Note: 1. STARTBF, ADDRF, ADDR10F, STOPF, BSF, RXDATNE and TXDATE are merged into the event interrupt channel through logical OR.

2. BUSERR, ARLOST, ACKFAIL, OVERRUN, PECERR, TIMEOUT and SMBALERT are merged into the error interrupt channel through logical OR.

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22.6 I2C Registers

These peripheral registers can be operated by half word (16 bits) or word (32 bits)

22.6.1 I2C Register Overview

Table 22-3 I2C register overview

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
000h	I2C_CTRL1	Reserved																SWRESET	Reserved	SMBALERT	PEC	ACKPOS	ACKEN	STOPGEN	STARTGEN	NOEXTEND	GCEN	PECEN	ARPEN	SMBTYPE	Reserved	SMBMODE	EN
	Reset Value																	0		0	0	0	0	0	0	0	0	0	0	0		0	0
004h	I2C_CTRL2	Reserved																			DMALAST	DMAEN	BUFINTEN	EVTINTEN	ERRINTEN	Reserved	CLKFREQ[5:0]						
	Reset Value																				0	0	0	0	0		0	0	0	0	0	0	
008h	I2C_OADDR1	Reserved																ADDRMODE	Reserved	Reserved				ADDR[9:8]		ADDR[7:1]							ADDR0
	Reset Value																	0						0	0	0	0	0	0	0	0	0	0
00Ch	I2C_OADDR2	Reserved																								ADDR2[7:1]							DUALEN
	Reset Value																									0	0	0	0	0	0	0	0
010h	I2C_DAT	Reserved																								DATA[7:0]							
	Reset Value																									0	0	0	0	0	0	0	0
014h	I2C_STS1	Reserved																SMBALERT	TIMOUT	Reserved	PECERR	OVERRUN	ACKFAIL	ARLOST	BUSERR	TXDATE	RXDATNE	Reserved	STOPF	ADDR10F	BSF	ADDRF	STARTBF
	Reset Value																	0	0		0	0	0	0	0	0	0		0	0	0	0	0
018h	I2C_STS2	Reserved																PECVAL[7:0]								DUALFLAG	SMBHADDR	SMBDADDR	GCALLADDR	Reserved	TRF	BUSY	MSMODE
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0		0	0	0
01Ch	I2C_CLKCTRL	Reserved																FSMODE	DUTY	Reserved	CLKCTRL[11:0]												
	Reset Value																	0	0		0	0	0	0	0	0	0	0	0	0	0	0	0
020h	I2C_TMRISE	Reserved																										TMRISE[5:0]					
	Reset Value																											0	0	0	0	0	0

22.6.2 I2C Control Register 1 (I2C_CTRL1)

Address offset: 0x00

Reset value: 0x0000

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SW RESET	Reserved	SMB ALERT	PEC	ACK POS	ACKEN	STOP GEN	START GEN	NO EXTEND	GCEN	PECEN	ARPEN	SMB TYPE	Reserved	SMB MODE	EN
rw		rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw		rw	rw

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Bit field	Name	Description
15	SWRESET	Software reset Make sure the I2C bus is idle before resetting this bit. 0:I2C not reset; 1:I2C reset. *Note: This bit can be used when the I2C_STS2.BUSY bit is set to 1 and no stop condition is detected on the bus.*
14	Reserved	Reserved, the reset value must be maintained.
13	SMBALERT	SMBus alert It can be set or cleared by software. When I2C_CTRL1.EN=0, it will be cleared by hardware. 0: SMBAlert pin go high. The response address header is followed by the NACK signal; 1: SMBAlert pin go low. The response address header is followed by the ACK signal.
12	PEC	Packet error checking It can be set or cleared by software. It will be cleared by hardware when PEC has been transferred, or by start or stop condition, or when I2C_CTRL1.EN=0. 0: No PEC transfer 1: PEC transfer. *Note: When arbitration is lost, the calculation of PEC is invalid.*
11	ACKPOS	Acknowledge/PEC Position（for data reception） It can be set or cleared by software. Or when I2C_CTRL1.EN=0, it will be cleared by hardware. 0: I2C_CTRL1.ACKEN bit determines whether to send an ACK to the byte currently being received; I2C_CTRL1.PEC bit indicates that the byte in the current shift register is PEC. 1: I2C_CTRL1.ACKEN bit etermines whether to send an ACK to the next received byte; I2C_CTRL1.PEC bit indicates that the next byte received in the shift register is PEC. *Note：* *ACKPOS bit can only be used in 2-byte receiving configuration and must be configured before receiving data.* *For the second byte of NACK, the I2C_CTRL1.ACKEN bit must be cleared after the I2C_STS1.ADDRF bit is cleared.* *To detect the PEC of the second byte, the I2C_CTRL1.PEC bit must be set after the ACKPOS bit is configured and when the ADDR event is extended.*
10	ACKEN	Acknowledge enable It can be set or cleared by software. Or when I2C_CTRL1.EN equals to 0, it will be cleared by hardware. 0：No acknowledge send; 1：Send an acknowledge after receiving a byte
9	STOPGEN	Stop generation It can be set or cleared by software. Or it will be cleared by hardware when a stop condition is detected. Or it will be set by hardware when SMBus timeout error is detected,. In the master mode: 0：No stop condition generates; 1：Generate a stop condition. In the slave mode: 0：No stop condition generates;

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Bit field	Name	Description
		1：Release SCL and SDA lines after the current byte. *Note：When the STOPGEN, STARTGEN or PEC bit is set, the software should not take any write operation to I2C_CTRL1 until this bit is cleared by hardware. Otherwise, the STOPGEN, STARTGEN or PEC bits may be set twice.*
8	STARTGEN	Start generation It can be set or cleared by software. Or it will be cleared by hardware when the start condition is transferred or I2C_CTRL1.EN=0. 0: No start condition generates; 1: Generate a start conditions.
7	NOEXTEND	Clock extending disable (Slave mode) This bit determines whether to pull SCL low when the data is not ready(I2C_STS1.ADDRF or I2C_STS1.BSF flag is set) in slave mode, and is cleared by software reset 0: Enable Clock extending. 1: Disable Clock extending.
6	GCEN	General call enable 0：Disable General call. not respond(NACK) to the address 00h; 1：Enable General call. respond(ACK) the address 00h.
5	PECEN	PEC enable 0：Disable PEC module; 1：Enable PEC module.
4	ARPEN	ARP enable 0: Disable ARP； 1: Enable ARP. If I2C_CTRL1.SMBTYPE=0, the default address of SMBus device is used. If I2C_CTRL1.SMBTYPE=1, the host address of SMBus is used.
3	SMBTYPE	SMBus type 0: Device 1: Host
2	Reserved	Reserved, the reset value must be maintained.
1	SMBMODE	SMBus mode 0：I2C mode； 1：SMBus mode.
0	EN	I2C Peripheral enable 0：Disable I2C module; 1：Enable I2C module *Note: If this bit is cleared when the communication is in progress, the I2C module is disabled and returns to the idle state after the current communication ends,all bits will be cleared.* *In master mode,this bit must never be cleared until the communication has ended.*

22.6.3 I2C Control Register 2 (I2C_CTRL2)

Address offset: 0x04

Reset value: 0x0000

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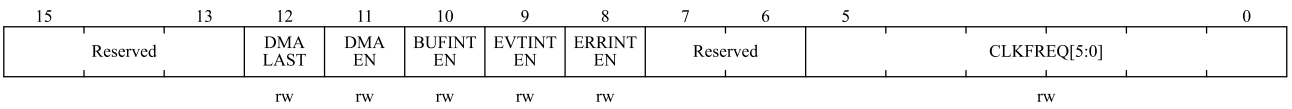

Bit field	Name	Description
15:13	Reserved	Reserved, the reset value must be maintained.
12	DMALAST	DMA last transfer 0: Next DMA EOT is not the last transfer 1: Next DMA EOT is the last transfer *Note: This bit is used in the master receiving mode, so that a NACK can be generated when data is received for the last time.*
11	DMAEN	DMA requests enable 0: Disable DMA 1: Enable DMA
10	BUFINTEN	Buffer interrupt enable 0: When I2C_STS1.TXDATE=1 or I2C_STS1.RXDATNE=1, any interrupt is not generated. 1: If I2C_CTRL2.EVTINTEN= 1,When I2C_STS1.TXDATE=1 or I2C_STS1.RXDATNE= 1, interrupt will be generated.
9	EVTINTEN	Event interrupt enable 0：Disable event interrupt； 1：Enable event interrupt This interrupt is generated when: I2C_STS1.STARTBF = 1 (Master) I2C_STS1.ADDR F = 1 (Master/Slave) I2C_STS1.ADD10F = 1 (Master) I2C_STS1.STOPF = 1 (Slave) I2C_STS1.BSF = 1 with no I2C_STS1.TXDATE or I2C_STS1.RXDATNE event I2C_STS1.TXDATE = 1 if I2C_CTRL2.BUFINTEN = 1 I2C_STS1.RXDATNE = 1 if I2C_CTRL2.BUFINTEN = 1
8	ERRINTEN	Error interrupt enable 0：Disable error interrupt； 1：Enable error interrupt. This interrupt is generated when: I2C_STS1.BUSERR = 1； I2C_STS1.ARLOST = 1； I2C_STS1.ACKFAIL = 1； I2C_STS1.OVERRUN = 1； I2C_STS1.PECERR = 1； I2C_STS1.TIMOUT = 1； I2C_STS1.SMBALERT = 1.
7:6	Reserved	Reserved, the reset value must be maintained.
5:0	CLKFREQ[5:0]	I2C Peripheral clock frequency CLKFREQ[5:0] should be the APB clock frequency to generate the correct timming. 000000：Disable 000001：Disable

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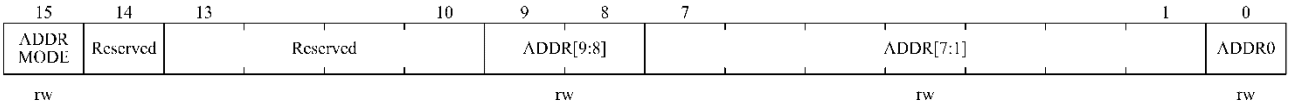
Bit field	Name	Description
		000010：2MHz 000011：3MHz ... 100100：36MHz 100101~111111：Disable.

22.6.4 I2C Own Address Register 1 (I2C_OADDR1)

Address offset: 0x08

Reset value: 0x0000

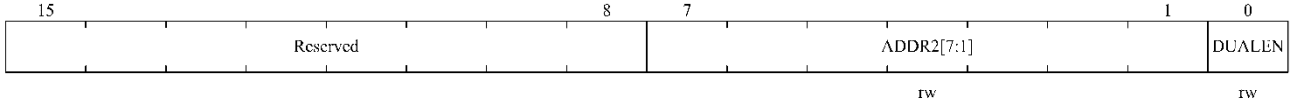


Bit field	Name	Description
15	ADDRMODE	Addressing mode (slave mode) 0: 7-bit slave address 1: 10-bit slave address
14	Reserved	Must always be kept as' 1' by the software.
13:10	Reserved	Reserved, the reset value must be maintained.
9:8	ADDR[9:8]	Interface address 9~8 bits of the address. *Note: don't care these bits in 7-bit address mode*
7:1	ADDR[7:1]	Interface address 7~1 bits of the address.
0	ADDR0	Interface address 0 bit of the address. *Note: don't care these bits in 7-bit address mode*

22.6.5 I2C Own Address Register 2 (I2C_OADDR2)

Address offset: 0x0C

Reset value: 0x0000



Bit field	Name	Description
15:8	Reserved	Reserved, the reset value must be maintained.
7:1	ADDR2[7:1]	Interface address 7~1 bits of address in dual address mode.
0	DUALEN	Dual addressing mode enable 0: Disable dual address mode, only OADDR1 is recognized;

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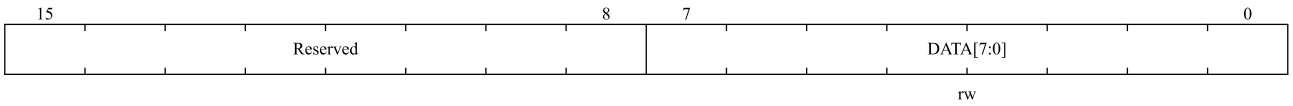
		1: Enable dual address mode, both OADDR1 and OADDR2 are recognized. *Note: Valid only for 7-bit address mode*

22.6.6 I2C Data Register (I2C_DAT)

Address offset: 0x10

Reset value: 0x0000



Bit field	Name	Description
15:8	Reserved	Reserved, the reset value must be maintained.
7:0	DATA[7:0]	8-bit data register Send or receive data buffer. *Note: In the slave mode, the address will not be copied into the data register;* *Note: if* I2C_STS1.*TXDATE =0, data can still be written into the data register;* *Note: If the ARLOST event occurs when processing the ACK pulse, the received byte will not be copied into the data register, so it cannot be read.*

22.6.7 I2C Status Register 1 (I2C_STS1)

Address offset: 0x14

Reset value: 0x0000

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SMB ALERT	TIM OUT	Reserved	PEC ERR	OVER RUN	ACK FAIL	AR LOST	BUS ERR	TXDATE	RXDAT NE	Reserved	STOPF	ADDR10F	BSF	ADDRF	START BF
rc_w0	rc_w0		rc_w0	rc_w0	rc_w0	rc_w0	rc_w0	r	r		r	r	r	r	r

Bit field	Name	Description
15	SMBALERT	SMBus alert Writing ‘0’ to this bit by software can clear it, or it is cleared by hardware when I2C_CTRL1.EN=0. 0: No SMBus alert(host mode) or no SMB alert response address header sequence(slave mode); 1: SMBus alert event is generated on the pin(host mode) or receive SMBAlert response address(slave mode)
14	TIMOUT	Timeout or Tlow error Writing ‘0’ to this bit by software can clear it, or it is cleared by hardware when I2C_CTRL1.EN=0. 0: No Timeout error； 1: A timeout error occurred Error in the following cases: • SCL has kept low for 25ms (Timeout).

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Bit field	Name	Description
		• Master cumulative clock low extend time more than 10 ms (Tlow:mext). • Slave cumulative clock low extend time more than 25 ms (Tlow:sext). Timeout in slave mode: slave device resets the communication and hardware frees the bus. Timeout in master mode: hardware sends the stop condition.
13	Reserved	Reserved, the reset value must be maintained.
12	PECERR	PEC Error in reception Writing '0' to this bit by software can clear it, or it is cleared by hardware when I2C_CTRL1.EN=0. 0: No PEC error 1: PEC error: receiver will returns NACK Whether the I2C_CTRL1.ACKEN bit is enabled
11	OVERRUN	Overrun/Underrun Writing '0' to this bit by software can clear it, or it is cleared by hardware when I2C_CTRL1.EN=0. 0: No Overrun/Underrun 1: Overrun/Underrun Set by hardware in slave mode when I2C_CTRL1.NOEXTEND=1, and when receiving a new byte in receiving mode, if the data within DAT register has not been read yet, over-run occurs,the new received byte will be lost.When transferring a new byte in transfer mode, but there is not new data that has not been written in DAT register, under-run occurs which leads that the same byte will be send twice.
10	ACKFAIL	Acknowledge failure Writing '0' to this bit by software can clear it, or it is cleared by hardware when I2C_CTRL1.EN=0. 0: No acknowledge failed; 1: Acknowledge failed.
9	ARLOST	Arbitration lost (master mode) Writing '0' to this bit by software can clear it, or it is cleared by hardware when I2C_CTRL1.EN=0. 0: No arbitration lost; 1: Arbitration lost. When the interface loses control of the bus to another host, the hardware will set this bit to '1', and the I2C interface will automatically switch back to slave mode (I2C_STS2.MSMODE=0). *Note: In SMBUS mode, the arbitration of data in slave mode only occurs in the data stage or the acknowledge transfer interval (excluding the address acknowledge).*
8	BUSERR	Bus error Writing '0' to this bit by software can clear it, or it is cleared by hardware when I2C_CTRL1.EN=0. 0: No start or stop condition error 1: Start or stop condition error
7	TXDATE	Data register empty (transmitters) Writing data to DAT register by software can clear this bit; Or after a start or stop condition occurs, or automatically cleared by hardware when I2C_CTRL1.EN=0. 0: Data register is not empty;

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Bit field	Name	Description
		1: Data register is empty. When sending data, this bit is set to' 1' when the data register is empty, and it is not set at the address sending stage. If a NACK is received, or the next byte to be sent is PEC(I2C_CTRL1.PEC=1), this bit will not be set. *Note: After the first data to be sent is written, or data is written when BSF is set, the TXDATE bit cannot be cleared, because the data register is still empty.*
6	RXDATNE	Data register not empty(receivers) This bit is cleared by software reading and writing to the data register, or cleared by hardware when I2C_CTRL1.EN=0. 0: Data register is empty; 1: Data register is not empty. During receiving data, this bit is set to' 1' when the data register is not empty, and it is not set at the address receiving stage. RXDATNE is not set when the ARLOST event occurs. *Note: When BSF is set, the RXDATNE bit cannot be cleared when reading data, because the data register is still full.*
5	Reserved	Reserved, the reset value must be maintained.
4	STOPF	Stop detection (slave mode) After the software reads the STS1 register, the operation of writing to the CTRL1 register will clear this bit, or when I2C_CTRL1.EN=0, the hardware will clear this bit. 0: No stop condition is detected; 1: Stop condition is detected. After a ACK, the hardware sets this bit to' 1' when the slave device detects a stop condition on the bus. *Note: I2C_STS1.STOPF bit is not set after receiving NACK.*
3	ADDR10F	10-bit header sent (Master mode) After the software reads the STS1 register, the operation of writing to the CTRL1 register will clear this bit, or when I2C_CTRL1.EN=0, the hardware will clear this bit. 0: No ADD10F event; 1: Master has sent the first address byte. In 10-bit address mode, when the master device has sent the first byte, the hardware sets this bit to' 1'. *Note: After receiving a NACK, the I2C_STS1.ADDR10F bit is not set.*
2	BSF	Byte transfer finished After the software reads the STS1 register, reading or writing the data register will clear this bit; Or after sending a start or stop condition in sending mode, or when I2C_CTRL1.EN=0, this bit is cleared by hardware. 0：Byte transfer does not finish. 1：Byte transfer finished. When I2C_CTRL1.NOEXTEND =0, the hardware sets this bit to' 1' in the following cases:

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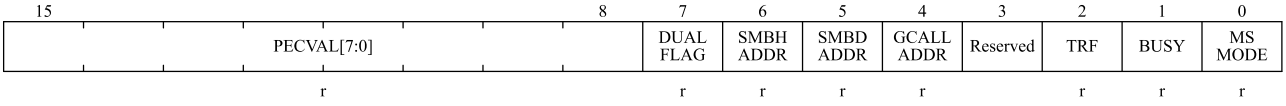
Bit field	Name	Description
		In receiving mode, when a new byte (including ACK pulse) is received and the data register has not been read (I2C_STS1.RXDATNE=1).In sending mode, when a new data is to be transmitted and the data register has not been written with the new data (I2C_STS1.TXDATE=1). *Note: After receiving a NACK, the BSF bit will not be set.* *If the next byte to be transferred is PEC (I2C _STS2.TRF is' 1' and I2C_CTRL1.PEC is' 1'), the BSF bit will not be set.*
1	ADDRF	Address sent (master mode) / matched (slave mode) After the STS1 register is read by software, reading the STS2 register will clear this bit, or when I2C_CTRL1.EN=0, it will be cleared by hardware. 0: Address mismatch or no address received(slave mode) or Address sending did not end(master mode); 1: Received addresses matched(slave mode) or Address sending ends(master mode) In master mode: In 7-bit address mode, this bit is set to' 1' after receiving the ACK of the address.In 10-bit address mode, this bit is set to' 1' after receiving the ACK of the second byte of the address. In slave mode: Hardware sets this bit to' 1' (when the corresponding setting is enabled) when the received slave address matches the content in the OADDR register, or a general call or SMBus device default address or SMBus host or SMBus alter is recognized. *Note: After receiving NACK, the I2C_STS1.ADDRF bit will not be set.*
0	STARTBF	Start bit (Master mode) After the STS1 register is read by software, writing to the data register will clear this bit, or when I2C_CTRL1.EN=0, the hardware will clear this bit. 0: Start condition was not sent; 1: Start condition has been sent. This bit is set to' 1' when the start condition is sent.

22.6.8 I2C Status Register 2 (I2C_STS2)

Address offset: 0x18

Reset value: 0x0000



Bit field	Name	Description
15:8	PECVAL[7:0]	Packet error checking register Stores the internal PEC value When I2C_CTRL1.PECEN =1.
7	DUALFLAG	Dual flag(Slave mode) Hardware clears this bit when a stop condition or a repeated start condition is generated, or when I2C_CTRL1.EN=0. 0: Received address matches the content in OADDR1; 1: Received address matches the content in OADDR2.

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Bit field	Name	Description
6	SMBHADDR	SMBus host header（Slave mode） Hardware clears this bit when a stop condition or a repeated start condition is generated, or when I2C_CTRL1.EN=0. 0: SMBus host address was not received; 1: when I2C_CTRL1.SMBTYPE=1 and I2C_CTRL1.ARPEN=1, SMBus host address is received.
5	SMBDADDR	SMBus device default address（Slave mode） Hardware clears this bit when a stop condition or a repeated start condition is generated, or when I2C_CTRL1.EN=0. 0: The default address of SMBus device has not been received; 1: when I2C_CTRL1.ARPEN=1, the default address of SMBus device is received.
4	GCALLADDR	General call address(Slave mode) Hardware clears this bit when a stop condition or a repeated start condition is generated, or when I2C_CTRL1.EN=0. 0: No general call address was received; 1: when I2C_CTRL1.GCEN=1, general call address was received.
3	Reserved	Reserved, the reset value must be maintained.
2	TRF	Transmitter/receiver After detecting the stop condition (I2C_STS1.STOPF=1), repeated start condition or bus arbitration loss (I2C_STS1.ARLOST=1), or when I2C_CTRL1.EN=0, the hardware clears it. 0: Data receiving mode; 1: Data transmission mode; At the end of the whole address transmission stage, this bit is set according to the R/W bit of the address byte.
1	BUSY	Bus busy Hardware clears this bit when a stop condition is detected. 0: No data communication on the bus; 1: Data communication on the bus. When detecting that SDA or SCL is low level, the hardware sets this bit to' 1'; *Note:This bit indicates the bus communication currently in progress, and this information is still updated when the interface is disabled (I2C_CTRL1.EN=0).*
0	MSMODE	Master/slave mode Hardware clears this bit when a stop condition is detected on the bus, arbitration is lost (I2C_STS1.ARLOST=1), or when I2C_CTRL1.EN=0. 0: In slave mode; 1: In master mode. When the interface is in the master mode (I2C_STS1.STARTBF=1), the hardware sets this bit;

22.6.9 I2C Clock Control Register (I2C_CLKCTRL)

Address offset: 0x1c

Reset value: 0x0000

Note: 1. F_{PCLK1} is required to be an integer multiple of 10 MHz, so that a fast clock of 400KHz can be generated

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correctly.

2. The CLKCTRL register can only be set when I²C is turned off (I2C_CTRL1.EN=0)

Bit field	Name	Description
15	FSMODE	I2C master mode selection 0: I2C in standard mode(duty cycle defaults to 1/1); 1: I2C in fast mode(duty cycle can be configured).
14	DUTY	Duty cycle in fast mode 0：Tlow/Thigh = 2； 1：Tlow/Thigh = 16/9
13:12	Reserved	Reserved, the reset value must be maintained.
11:0	CLKCTRL[11:0]	Clock control register in Fast/Standard mode (Master mode) This division factor is used to set the SCL clock in the master mode. ■ If duty cycle = Tlow/Thigh = 1/1: CLKCTRL = f_{PCLK1}(Hz)/100000/2 Tlow = CLKCTRL×T_{PCLK1} Thigh = CLKCTRL×T_{PCLK1} ■ If duty cycle = Tlow/Thigh = 2/1: CLKCTRL = f_{PCLK1}(Hz)/100000/3 Tlow = 2 ×CLKCTRL×TPCLK1 Thigh = CLKCTRL×T_{PCLK1} ■ If duty cycle = Tlow/Thigh = 16/9: CLKCTRL = f_{PCLK1}(Hz)/100000/25 Tlow = 16 ×CLKCTRL×T_{PCLK1} Thigh = 9 ×CLKCTRL×T_{PCLK1} For example, if f_{PCLK1}(Hz) = 8MHz, duty cycle = 1/1, CLKCTRL = 8000000/100000/2 = 0x28. *Note: 1. The minimum setting value is 0x04 in standard mode and 0x01 in fast mode;* *2. T_{high}= $T_{r(SCL)}$+$T_{w(SCLH)}$. See the definitions of these parameters in the data sheet for details.* *3. T_{low}= $T_{f(SCL)}$+$T_{w(SCLL)}$, see the definitions of these parameters in the data sheet for details;* *4. These delays have no filters;*

22.6.10 I2C Rise Time Register (I2C_TMRISE)

Address offset: 0x20

Reset value: 0x0002

Note: The I2C_TMRISE register function is only valid in master mode. changed when I2C is disabled (I2C_CTRL1.EN=0).

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Bit field	Name	Description
15:6	Reserved	Reserved, the reset value must be maintained.
5:0	TMRISE[5:0]	Maximum rise time in fast/standard mode (master mode). These bits must be set to the maximum SCL rising time given in the I2C bus specification, and incremented step is 1. For example, the maximum allowable SCL rise time in standard mode is 1000ns. if the value in I2C_CTRL2.CLKFREQ [5:0] is equal to 0x08 and TPCLK1=125ns ,09h(1000ns/125 ns + 1) must be written in TMRISE[5:0] ,. If the result is not an integer, write the integer part to TMRISE[5:0] to ensure the t_{HIGH} parameter.

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23 Universal Synchronous Asynchronous Receiver Transmitter (USART)

23.1 Introduction

USART is a full-duplex universal synchronous/asynchronous serial transceiver module. This interface is a highly flexible serial communication device that can perform full-duplex data exchange with external devices.

The USART has programmable transmit and receive baud rates and can communicate continuously using DMA. It also supports multiprocessor communication, LIN mode, synchronous mode, single-wire half-duplex communication, smart card asynchronous protocol, IrDA SIR ENDEC function, and hardware flow control function.

23.2 Main Features

Hjnnnnnnn-=Full-duplex operation

- Single-wire half-duplex operation
- Baud rate generator, the highest baud rate can reach 4.5Mbit/s
- Support serial data frame structure with 8 or 9 data bits, 1 or 2 stop bits
- Generation and checking of supported parity bits
- Support hardware flow control: RTS flow control and CTS flow control
- Support DMA receiving and sending
- Support multi-processor communication mode, can enter mute mode, wake up by idle detection or address mark detection
- Synchronous mode, allowing users to control bidirectional synchronous serial communication in master mode
- Comply with ISO7816-3 standard, support smart card asynchronous protocol
- IrDA SIR ENDEC function: IrDA normal mode and IrDA low power mode
- LIN (Local Area Network) mode
- Support data overflow error detection, frame error detection, noise error detection, parity error detection
- Interrupt requests include: transmit data register empty, CTS flag, transmit complete, receive data ready to read, data overflow detected, idle line detected, parity error, LIN break frame detection, noise flag/overflow error/frame error in multi-buffer communication

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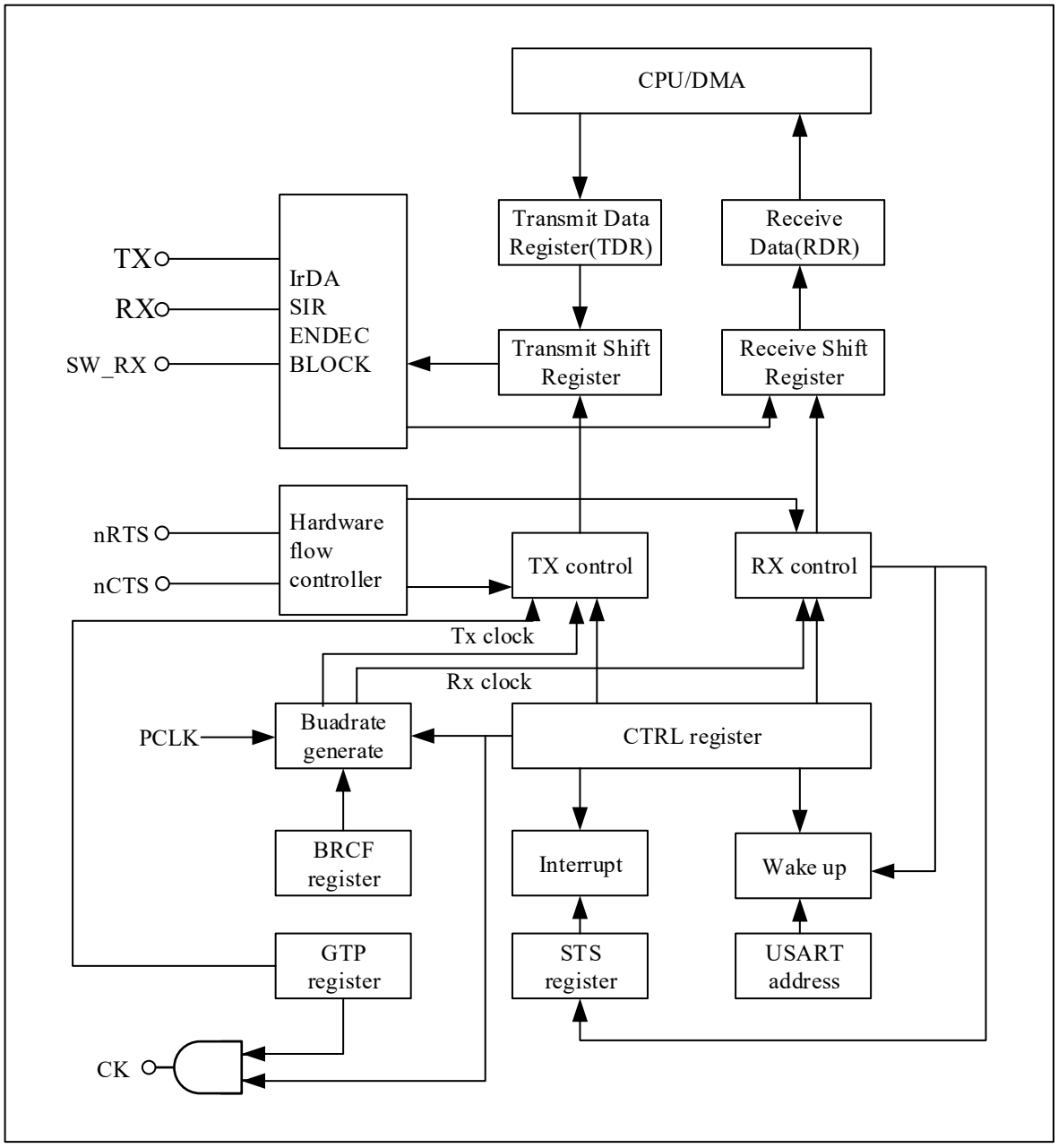
23.3 Functional Block Diagram

Figure 23-1 USART block diagram



23.4 Function Description

As shown in the Figure 23-1, the bidirectional communication of any USART needs to use the RX and TX pins of the external connection. Among them, TX is the output pin for serial data transmission. When the transmitter is active and not sending data, the TX pin is pulled high. When the transmitter is inactive, the TX pin reverts to the I/O port configuration. RX is an input pin for serial data reception, data is recovered by oversampling technique.

The data packets of serial communication are transmitted from the sending device to the RX interface of the receiving device through its own TX interface, and the bus is in an idle state before sending or receiving. Frame format is: 1

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start bit + 8 or 9 data bits (least significant bit first) + 1 parity bit (optional) + 0.5,1,1.5 or 2 stop bit.

Use the fractional baud rate generator to configure transmit and receive baud rates.

According to the block diagram, when using the hardware flow control mode, the nRTS output and nCTS input pins are required. When the USART receiver is ready to receive new data, nRTS becomes low level. If nCTS is valid (pulled to a low level), the next data is sent, otherwise the next frame of data is not sent.

When using synchronous mode, the CK pin is required. The CK pin is used for clock output for synchronous transfers. Clock phase and polarity are software programmable. During the start and stop bits, the CK pin does not output clock pulses.The CK pin is also used when using smart card mode.

23.4.1 USART Frame Format

The start bit of the data frame is low.

The word length can be selected as 8 or 9 bits by programming the USART_CTRL1.WL bits, least significant bit first.

The stop bit of the data frame is high.

An idle frame is a complete data frame consisting of '1's, including the start bit. followed by the start bit of a data frame containing the data .

A break frame is a complete data frame consisting of '0's, including the stop bit. at the end of the break frame, the transmitter inserts 1 or 2 more stop bits ('1') to acknowledge the start bit.

Figure 23-2 word length = 8 setting

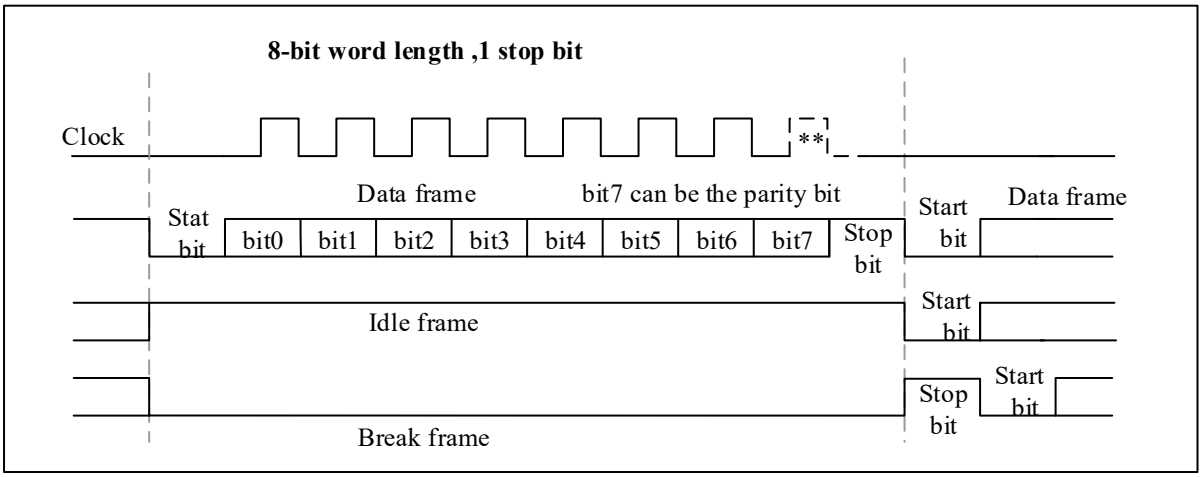

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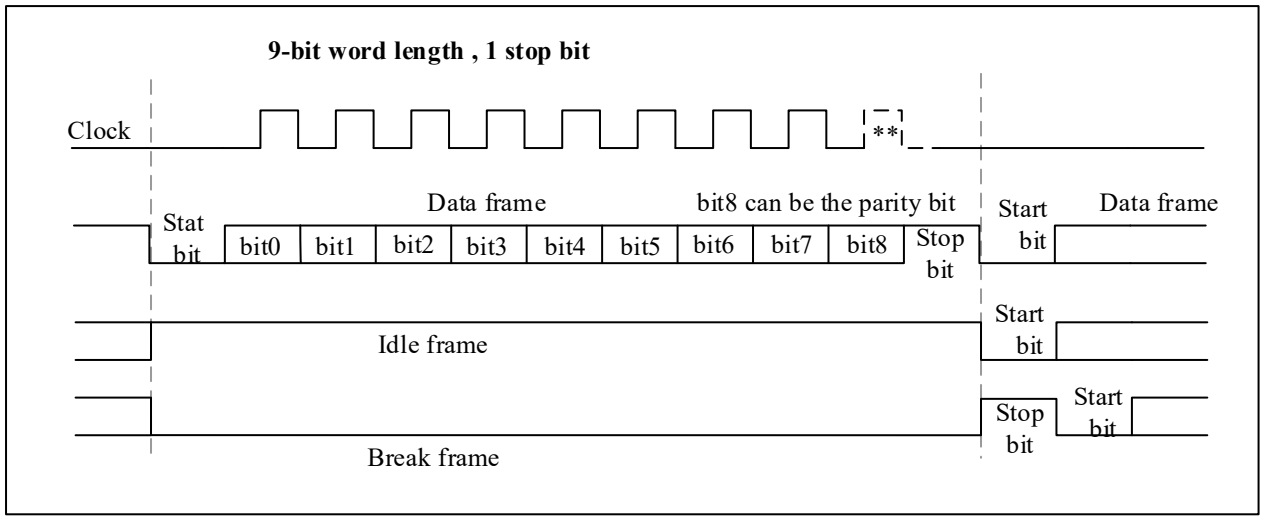
Figure 23-3 word length = 9 setting



23.4.2 Transmitter

After the transmitter is enabled, the data entered into the transmit shift register is sent out through the TX pin.

23.4.2.1 Idle frame

Setting USART_CTRL1.TXEN will cause the USART to transmit an idle frame before the first data frame.

23.4.2.2 Character send

Idle frames are followed by characters sent. Each character is preceded by a low start bit. The transmitter sends 8-bit or 9-bit data according to the configuration of the data bit length, with the least significant bit first. If USART_CTRL1.TXEN is reset during a data transfer, it will cause the baud rate counter to stop counting and the data being transferred will be corrupted.

23.4.2.3 Stop bit

The characters are followed by stop bits, the number of which can be configured by setting USART_CTRL2. STPB[1:0].

Table 23-1 Stop bit configuration

USART_CTRL2.STPB[1:0]	Stop bit length (bits)	functional description
00	1	default
01	0.5	Receiving in Smartcard mode
10	2	General USART mode, single-wire mode and modem mode.
11	1.5	Transmitting and receiving in Smartcard mode

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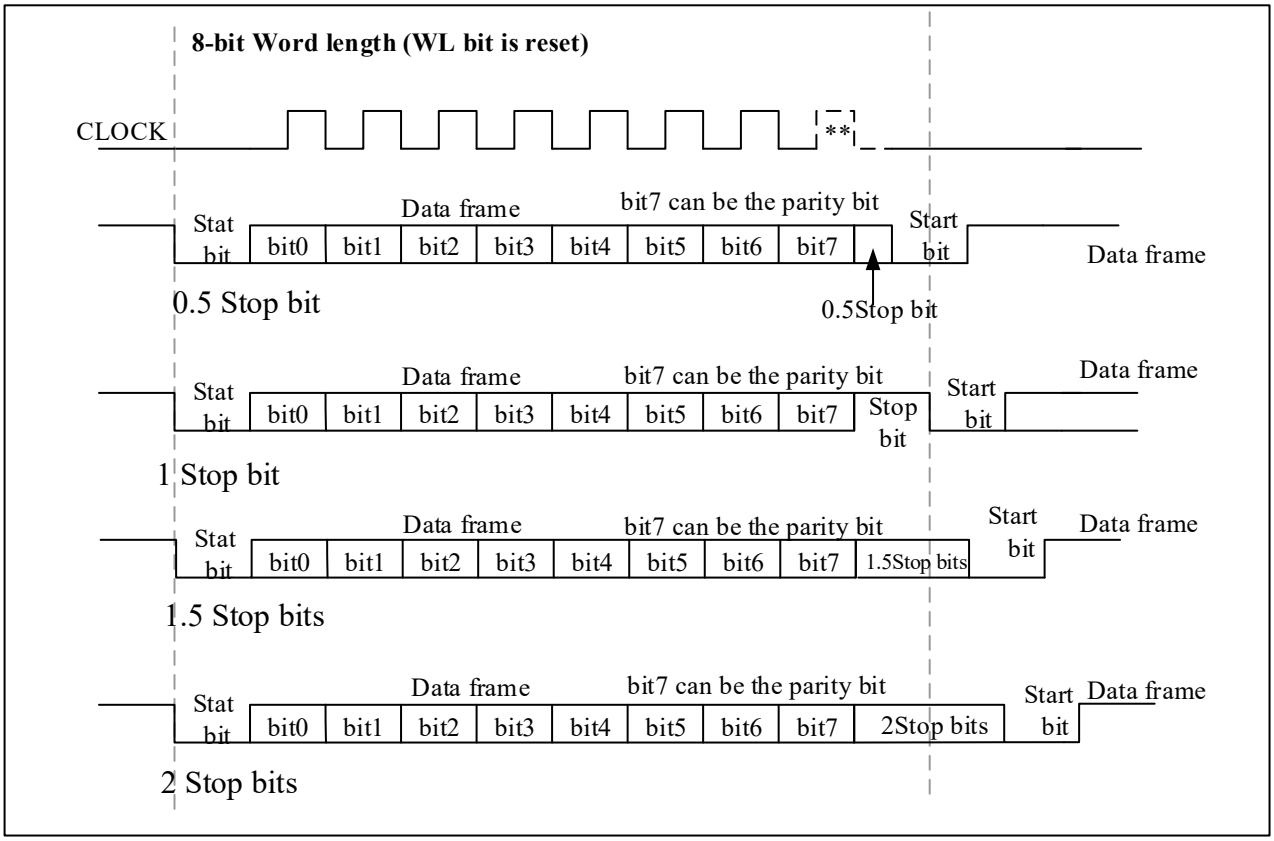
Figure 23-4 configuration stop bit



23.4.2.4 Break frame

Use USART_CTRL1.SDBRK to send the break character. When there is 8-bit data, the break frame consists of 10 bits of low level, followed by a stop bit; when there is 9-bit data, the break frame consists of 11 bits of low level, followed by a stop bit.

After the break frame is sent, USART_CTRL1.SDBRK is cleared by hardware, and the stop bit of the break frame is being sent. Therefore, to send a second break frame, USART_CTRL1.SDBRK should be set after the stop bit of the previous break frame has been sent.

If software resets the USART_CTRL1.SDBRK bit before starting to send the break frame, the break frame will not be sent.

23.4.2.5 Transmitter process

1. Enable USART_CTRL1.UEN to activate USART;
2. Configure the transmitter's baud rate, data bit length, parity bit (optional), the number of stop bits or DMA configuration;
3. Activate the transmitter (USART_CTRL1.TXEN);
4. Send each data to be sent to the USART_DAT register through the CPU or DMA, and the write operation to the USART_DAT register will clear USART_STS.TXDE;
5. After writing the last data word in the USART_DAT register, wait for USART_STS.TXC =1, which indicates the end of the transmission of the last data frame.

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23.4.2.6 Single byte communication

A write to the USART_DAT register clears the USART_STS.TXDE bit.

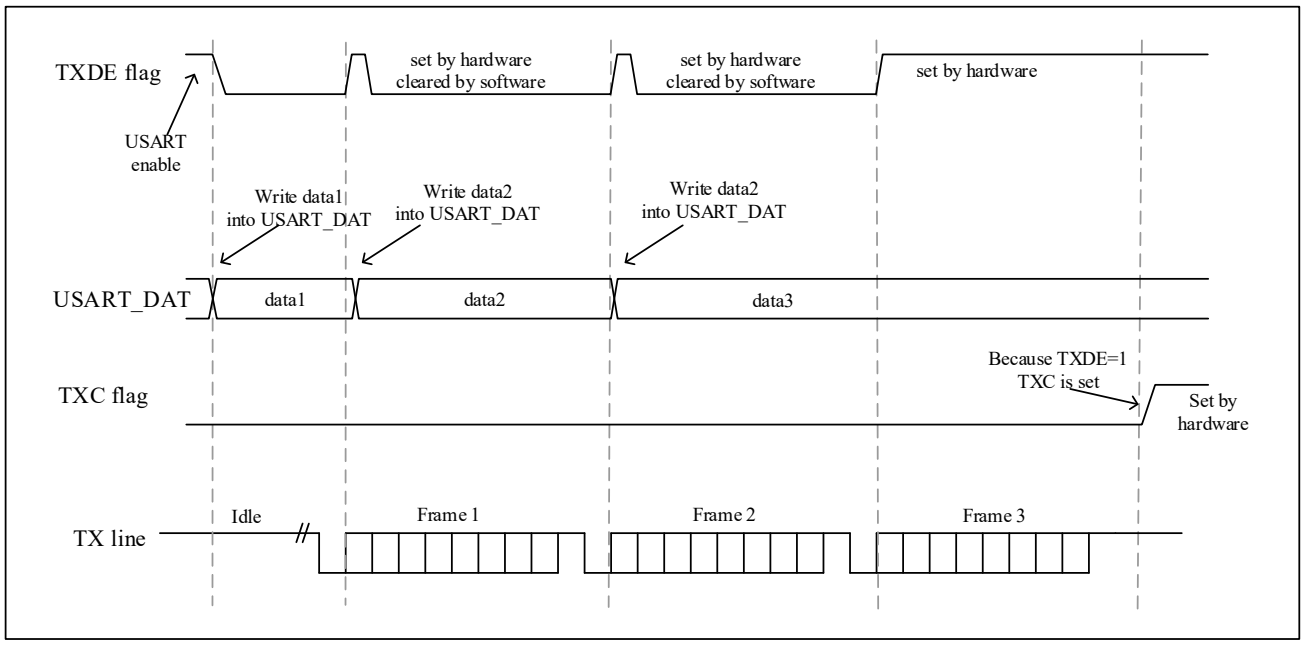
The USART_STS.TXDE bit is set by hardware when the data in the TDR register is transferred to the transmit shift register (indicating that data is being transmitted). An interrupt will be generated if USART_CTRL1.TXDEIEN is set. At this point, the next data can be sent to the USART_DAT register because the TDR register has been cleared and will not overwrite the previous data.

Write operation to USART_DAT register:

- When the transmit shift register is not sending data and is in an idle state, the data is directly put into the shift register for transmission, and the USART_STS.TXDE bit is set by hardware;
- When the transmit shift register is sending data, the data is stored in the TDR register, and after the current transmission is completed, the data is put into the shift register.

When a frame containing data is sent and USART_STS.TXDE=1, the USART_STS.TXC bit is set to '1' by hardware. An interrupt is generated if USART_CTRL1.TXCIEN is '1'. USART_STS.TXC bit is cleared by a software sequence (read USART_STS register first, then write USART_DAT register).

Figure 23-5 TXC/TXDE changes during transmission



23.4.3 Receiver

23.4.3.1 Start bit detection

When the received sampling sequence is: 1 1 1 0 X 0 X 0 X 0 0 0 0, it is considered that a start bit is detected.

The samples at the 3rd, 5th, and 7th bits, and the samples at the 8th, 9th, and 10th bits are all '0' (that is, 6 '0'), then confirm the receipt of the start bit, the USART_STS.RXDNE flag bit is set, and if USART_CTRL1.RXDNEIEN=1, an interruption occurs and will not Set the NEF noise flag.

The samples of the 3rd, 5th, and 7th bits have two '0' points, and at the same time, the samples of the 8th, 9th, and

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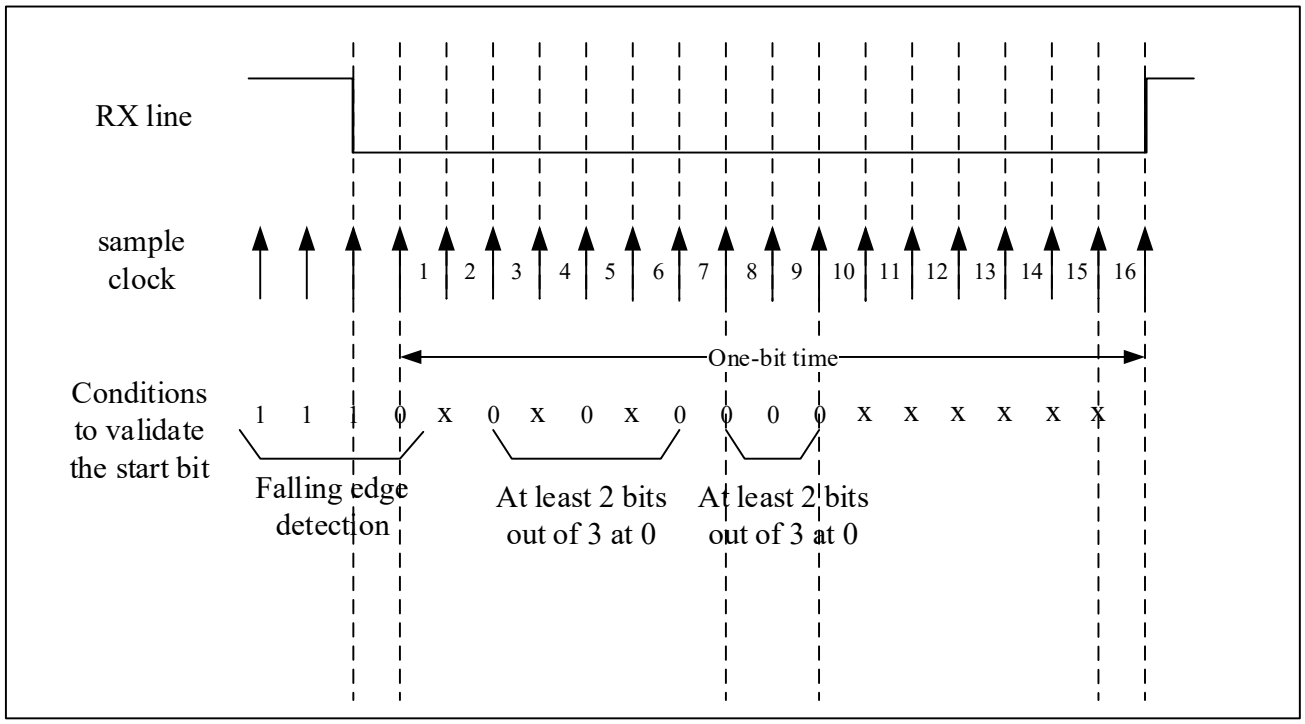
10th bits have three '0' points, then the start bit is confirmed, but it will be set NEF noise flag.

The samples of the 3rd, 5th, and 7th bits have three '0' points, and at the same time, the samples of the 8th, 9th, and 10th bits have two '0' points, then the start bit is confirmed, but it will be set NEF noise flag.

The samples of the 3rd, 5th, and 7th bits have two '0' points, and at the same time, the samples of the 8th, 9th, and 10th bits have two '0' points, then it is confirmed that the start bit is received, but it will be set bit NEF noise flag.

If the sampling values in the 3rd, 5th, 7th, 8th, 9th and 10th bits cannot meet the above four requirements, the USART receiver thinks that it has not received the correct start bit, and will exit the start bit detection and Return to idle state and wait for falling edge.

Figure 23-6 Start bit detection



23.4.3.2 Stop bit description

During data reception, the number of data stop bits can be configured by the USART_CTRL2.STPB[1:0]. In normal mode, 1 or 2 stop bits can be selected. In Smartcard mode, 0.5 or 1.5 stop bits can be selected.

1. 0.5 stop bits (receive in smartcard mode): 0.5 stop bits are not sampled. Therefore, if 0.5 stop bits is selected, framing errors and broken frames cannot be detected.

2. 1 stop bit: the sampling of one stop bit is carried out through three points, and the 8th, 9th and 10th sampling bits are selected.

3. 1.5 stop bit (Smartcard mode): when sending in Smartcard mode, the device must check whether the data is sent correctly. So the receiver function block must be activated (USART_CTRL1.RXEN=1) and sample the signal on the data line during the transmission of the stop bit. If a parity error occurs, the smartcard will pull down the data line when the transmitter samples the NACK signal, that is, within the time corresponding to the stop bit on the bus, indicating that a framing error has occurred. The USART_STS.FEF is set together with the USART_STS.RXDNE at the end of the 1.5th stop bit. The 1.5 stop bits were sampled at points 16, 17 and 18.

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The 1.5 stop bits can be divided into two parts: one is 0.5 clock cycles, during which nothing is done. This is followed by the stop bit of 1 clock cycle, which is sampled at the midpoint of this period of time. For details, see 23.4.14 Smartcard mode.

4. 2 stop bits: the sampling of the 2 stop bits is completed at the 8th, 9th and 10th sampling points of the first stop position. If a frame error is detected during the first stop bit, the frame error flag is set. The second stop bit does not detect framing error. The USART_STS.RXNE flag will be set at the end of the first stop bit.

23.4.3.3 Receiver process

1. Enable USART_CTRL1.UEN to activate USART;
2. Configure the receiver's baud rate, data bit length, parity bit (optional), stop bit number or DMA configuration;
3. Activate the receiver (USART_CTRL1.RXEN) and start looking for the start bit;
4. The receiver receives 8-bit or 9-bit data according to the configuration of the data bit length, and the least significant bit of the data is first shifted from the RX pin into the receive shift register;
5. When the data of the received shift register is moved to the RDR register, USART_STS.RXDNE is set, and the data can be read out. If USART_CTRL1.RXNEIEN is 1, an interrupt will be generated;
6. When an overflow error, noise error, or frame error is detected in the received frame, the corresponding error flag status bit will be set. If USART_CTRL1.RXEN is reset during data transmission, the data being received will be lost;
7. USART_STS.RXDNE is set after receiving data, and a read operation of USART_DAT can clear this bit:

– During multi-buffer communication, the data register is cleared by the DMA read operation;

– During single-buffer communication, it is cleared by software reading the USART_DAT register.

23.4.3.4 Idle frame detection

The receiver of the USART can detect idle frames. An interrupt is generated if USART_CTRL1.IDLEIEN is '1'. USART_STS.IDLEF bit is cleared by a software sequence (read USART_STS register first, then read USART_DAT register).

23.4.3.5 Break frame detection

The frame error flag(USART_STS.FEF) is set by hardware when the receiver detects a break frame. It can be cleared by a software sequence (read USART_STS register first, then read USART_DAT register).

23.4.3.6 Framing error

A framing error occurs when a stop bit is not received and recognized at the expected time. At this time, the frame error flag USART_STS.FEF will be set by hardware, and the invalid data will be transferred from the shift register to the USART_DAT register. During single-byte communication, no framing error interrupt will be generated because it occurs with USART_STS.RXDNE and the hardware will generate an interrupt when the USART_STS.RXDNE flag is set. In multi-buffer communication mode, an interrupt will be generated if the USART_CTRL3.ERRIEN bit is set.

23.4.3.7 Overrun error

When USART_STS.RXDNE is still '1', when the data currently received in the shift register needs to be transferred to the RDR register, an overflow error will be detected, and the hardware will set USART_STS.OREF. When this bit

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is set, the value in the RDR register is not lost, but the data in the shift register is overwritten. It is cleared by a software sequence (read USART_STS register first, then write USART_DAT register).

When an overflow error occurs, USART_STS.RXDNE is '1', and an interrupt is generated. If the USART_CTRL3.ERRIEN bit is set, an interrupt will be generated when the USART_STS.OREF flag is set in multi-buffer communication mode.

23.4.3.8 Noise error

USART_STS.NEF is set by hardware when noise is detected on a received frame. It is cleared by software sequence (read USART_STS register first, then write USART_DAT register). During single-byte communication, no noise interrupt generated because it occurs with USART_STS.RXDNE and the hardware will generate an interrupt when the USART_STS.RXDNE flag is set. In multi-buffer communication mode, an interrupt is generated when the USART_STS.NEF flag is set if the USART_CTRL3.ERRIEN bit is set.

Table 23-2 Data sampling for noise detection

Sample value	NE status	Received bits	Data validity
000	0	0	Effective
001	1	0	be invalid
010	1	0	be invalid
011	1	1	be invalid
100	1	0	be invalid
101	1	1	be invalid
110	1	1	be invalid
111	0	1	Effective

23.4.4 Generation of Fractional Baud Rate

The baud rate of the USART can be configured in the USART_BRCF register. This register defines the integer and fractional parts of the baud rate divider. The baud rate of the transmitter and receiver should be configured to the same value. Be careful not to change the value of the USART_BRCF register during communication, because the baud rate counter will be replaced by the new value of the baud rate register.

$$\text{TX / RX baud rate} = f_{PCLK} /(16 * \text{USARTDIV})$$

where f_{PCLK} is the clock provided to the peripheral:

- PCLK1 is used for USART2, USART3, UART4, UART5, up to 36MHz;
- PCLK2 is used for USART1, UART6, UART7, up to 72MHz.

USARTDIV is an unsigned fixed-point number.

23.4.4.1 USARTDIV and USART_BRCF register configuration

Example 1:

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If USARTDIV = 27.75, then：

DIV_Decimal = 16*0.75 = 12 = 0x0C

DIV_Integer = 27=0x1B

So USART_BRCF = 0x1BC

Example 2:

If USARTDIV = 20.98, then：

DIV_Decimal = 16*0.98 = 15.68

Nearest integer: DIV_Decimal = 16 = 0x10, out of configurable range, so a carry to integer is required

So DIV_Integer = 20+1 = 21 = 0x15

DIV_Decimal = 0x0

So USART_BRCF = 0x150

Example 3:

If USART_BRCF = 0x19B：

DIV_Integer = 0x19 = 25

DIV_Decimal = 0x0B = 11

So USARTDIV = 25+11/16 = 25.6875

Table 23-3 Error calculation when setting baud rate

Baud rate		**f_{PCLK}=36MHz**			**f_{PCLK}=72MHz**		
serial number	Kbps	reality	Set value in register	Error(%)	reality	Set value in register	Error(%)
1	2.4	2.4	937.5	0%	2.4	1875	0%
2	9.6	9.6	234.375	0%	9.6	468.75	0%
3	19.2	19.2	117.1875	0%	19.2	234.375	0%
4	57.6	57.6	39.0625	0%	57.6	78.125	0%
5	115.2	115.384	19.5	0.15%	115.2	39.0625	0%
6	230.4	230.769	9.75	0.16%	230.769	19.5	0.16%
7	460.8	461.538	4.875	0.16%	461.538	9.75	0.16%
8	921.6	923.076	2.4375	0.16%	923.076	4.875	0.16%
9	2250	2250	1	0%	2250	2	0%

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10	4500	impossible	impossible	impossible	4500	1	0%

Notes: The lower the clock frequency of the CPU, the lower the error for a particular baud rate.

23.4.5 Receiver's tolerance clock deviation

Variations due to transmitter errors (including transmitter side oscillator variations), receiver side baud rate rounding errors, receiver side oscillator variations, variations due to transmission lines (usually due to The inconsistency between the low-to-high transition timing of the transceiver and the high-to-low transition timing of the transceiver), these factors will affect the overall clock system variation. Only when the sum of the above four changes is less than the tolerance of the USART receiver, the USART asynchronous receiver can work normally.

When receiving data normally, the tolerance of the USART receiver depends on the selection of the data bit length and whether it is generated using a fractional baud rate. The tolerance of the USART receiver is equal to the maximum tolerable variation.

Table 23-4 when DIV_Decimal = 0. Tolerance of USART receiver

WL bit	NF is an error	NF is don't care
0	3.75%	4.375%
1	3.41%	3.97%

Table 23-5 when DIV_Decimal != 0. Tolerance of USART receiver

WL bit	NF is an error	NF is don't care
0	3.33%	3.88%
1	3.03%	3.53%

23.4.6 Parity Control

Parity can be enabled by configuring the USART_CTRL1.PCEN bit.

When the parity bit is enabled for transmission, A parity bit is generated, parity check is performed on reception.

Table 23-6 Frame format

WL bit	PCEN bit	USART frame
0	0	| Start bit | 8-bit data | Stop bit |
0	1	| Start bit | 7 bits of data | Parity bit | Stop bit |
1	0	| Start bit | 9-bit data | Stop bit |
1	1	| start bit | 8-bit data | parity bit | stop bit |

Even parity

Configure USART_CTRL1.PSEL to 0, and even parity can be selected.

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Make the number of '1' in the transmitted data (including parity bit) be an even number. That is: if Data=11000101, there are 4 '1's, then the parity bit will be '0' (4 '1' in total). After the data and check digit are sent to the receiver, the receiver calculates the number of 1s in the data again. If it is an even number, the check is passed, indicating that no errors occurred during the transmission process. If it is not even, it means that an error has occurred, the USART_STS.PEF flag is set to '1', and if USART_CTRL1.PEIEN is enabled, an interrupt is generated.

Odd parity

Configure USART_CTRL1.PSEL to 1, you can choose odd parity.

Make the number of '1' in the transmitted data (including parity bit) be an odd number. That is: if Data=11000101, there are 4 '1's, then the parity bit will be '1' (5 '1' in total). After the data and check digit are sent to the receiver, the receiver calculates the number of 1s in the data again. If it is an odd number, the check is passed, indicating that no errors occurred during the transmission process. If it is not an odd number, it means that an error has occurred, the USART_STS.PEF flag is set to '1', and if USART_CTRL1.PEIEN is enabled, an interrupt is generated.

23.4.7 DMA Application

The USART supports the DMA mode using multi-buffer configuration, which can realize high-speed data communication.

23.4.7.1 Using DMA transmission

Set USART_CTRL3.DMATXEN to enable DMA mode when transmitting. When the USART's transmit shift register is empty (USART_STS.TXDE=1), the DMA will transfer the data from the SRAM to the USART_DAT register of the USART.

When using DMA transmission, the process of configuring the DMA channel is as follows:

1. Set the address of the data memory. When a data transfer request occurs, the transferred data will be read from this address.
2. Set the address of the USART_DAT register. When a data transfer request occurs, this address will be the destination address of the data transfer.
3. Set the amount of data to transfer.
4. Set the priority of the channel, set whether to use the cyclic mode, the incremental mode of peripherals and memory, the data width of peripherals and memory, the interrupt generated by half of the transfer or the interrupt when the transfer is completed.
5. Start the channel.
6. After the data transfer is completed, the transfer complete flag (DMA_INTSTS.TXCFx) is set to 1.

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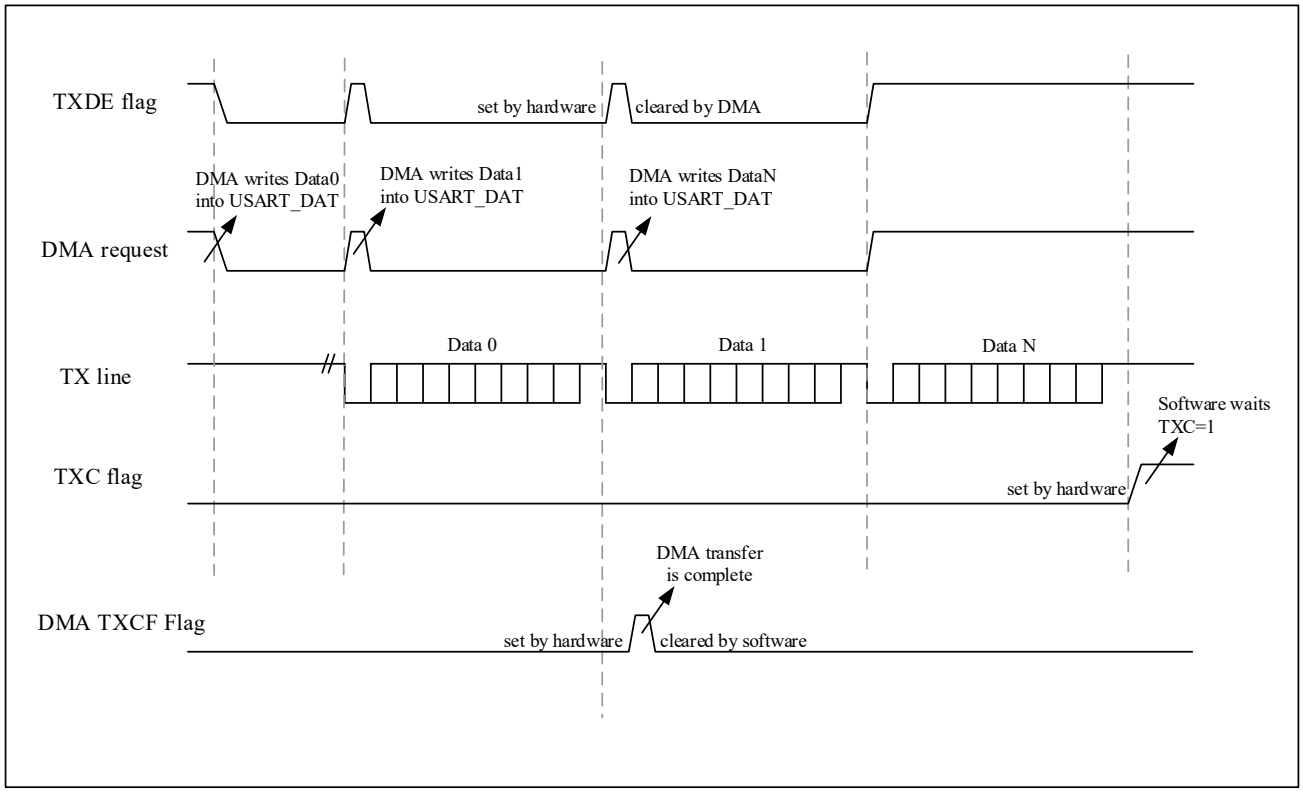
Figure 23-7 Transmission using DMA



23.4.7.2 Using DMA reception

Set USART_CTRL3.DMARXEN to enable DMA mode when receiving. When a byte is received (USART_STS.RXDNE=1), the DMA will transfer the data from the USART_DAT register of the USART to the SRAM.

When using DMA reception, the process of configuring the DMA channel is as follows:

1. Set the address of the USART_DAT register. When a data transfer request occurs, this address will be the source address of the data transfer.
2. Set the address of the data memory. When a data transfer request occurs, the transferred data will be written to this address.
3. Set the amount of data to transfer.
4. Set the priority of the channel, set whether to use the cyclic mode, the incremental mode of peripherals and memory, the data width of peripherals and memory, the interrupt generated by half of the transfer or the interrupt when the transfer is completed.
5. Start the channel.

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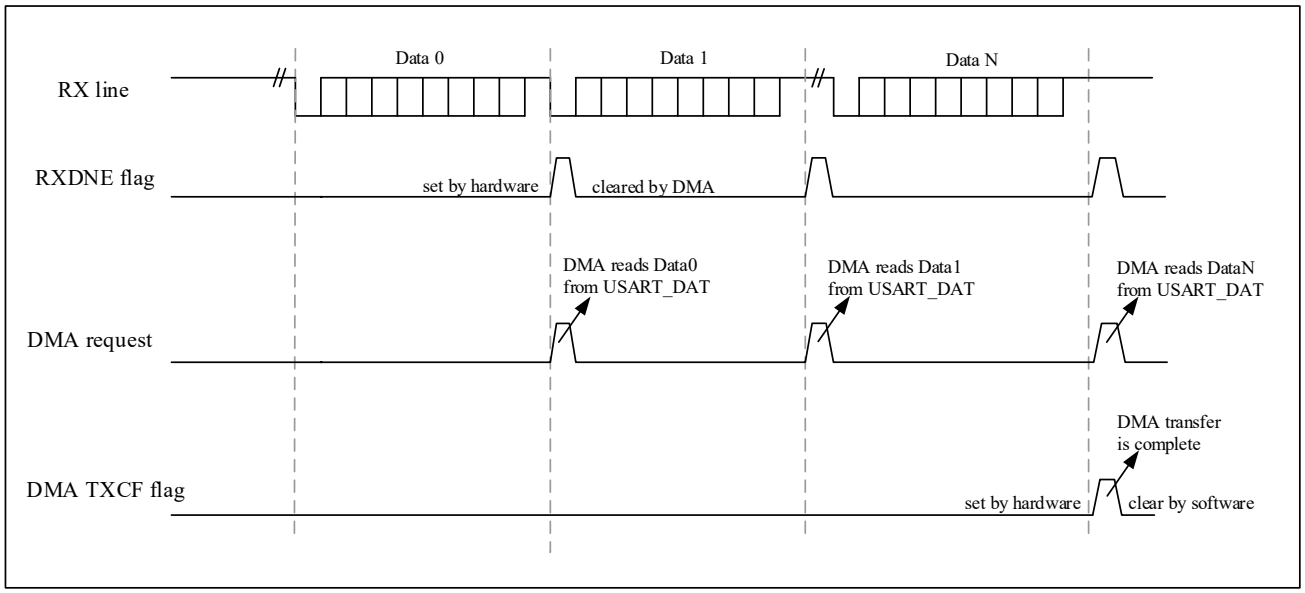
Figure 23-8 Reception using DMA

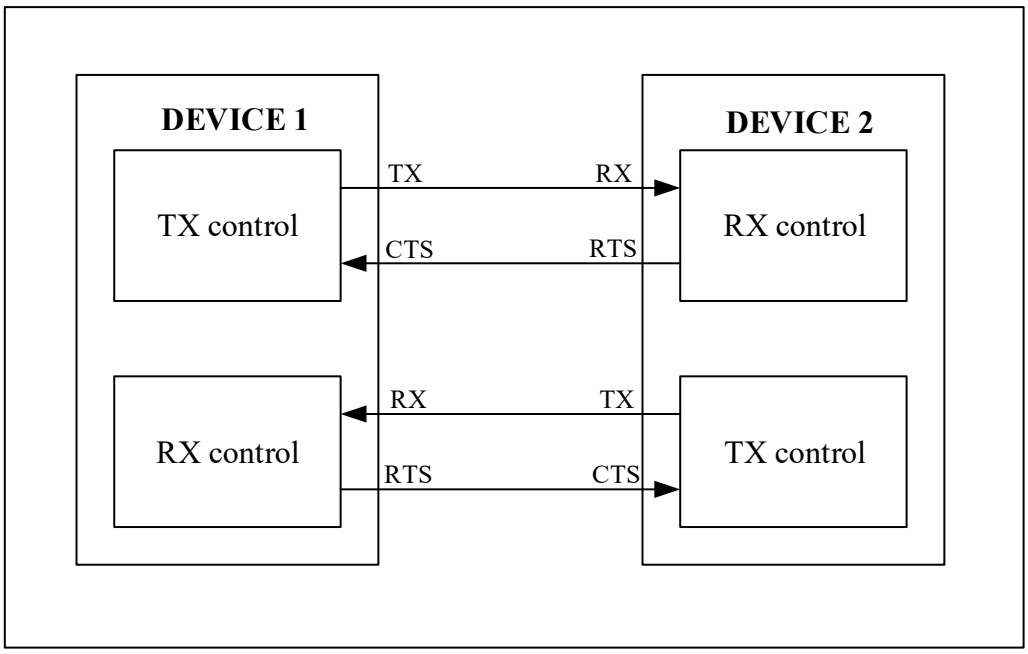


In multi-buffer communication mode, the error flag will be set when there is a frame error, overrun or noise error. An interrupt will be generated if the error interrupt is enabled (USART_CTRL3.ERRIEN=1).

23.4.8 Hardware Flow Control

USART supports hardware flow control. The purpose is to coordinate the sending and receiving parties so that the data will not be lost. The connection method is shown in the following figure.

Figure 23-9 hardware flow control between two USART



23.4.8.1 RTS flow control

Set USART_CTRL3.RTSEN to enable RTS. RTS is the output signal used to indicate that the receiver is ready. When

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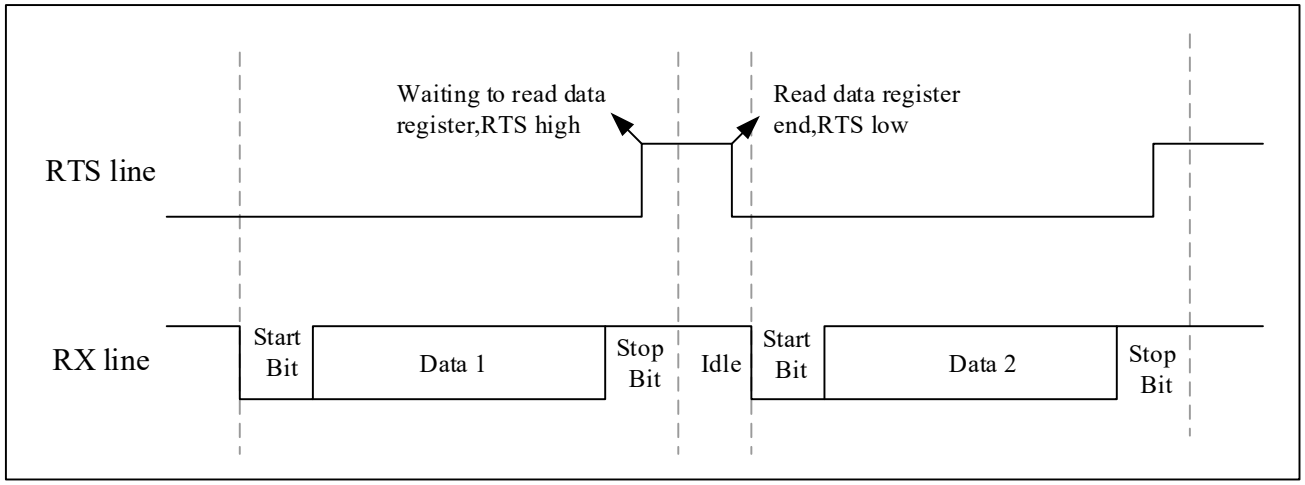
data arrives in RDR, pull high nRTS output, notifying the sender to stop data transmission at the end of the current frame. when receiver is ready to receive new data, assert (pull low) the nRTS output.

Figure 23-10 RTS flow control

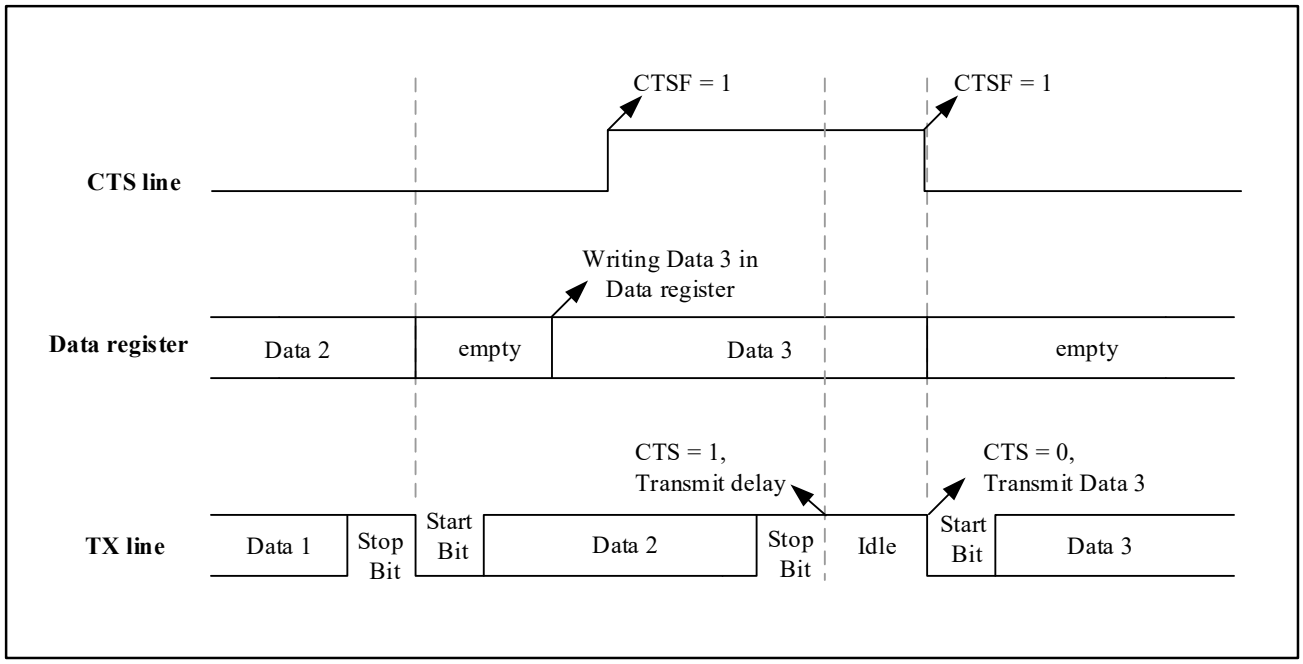


23.4.8.2 CTS flow control

Set USART_CTRL3.CTSEN to enable CTS. CTS is an input signal, used to judge whether data can be sent to the other device. The low level is valid, and the low level indicates that the device can send data to the other device. If the nCTS signal becomes invalid during data transmission, the transmission will stop after sending the data. If you write data to the data register when nCTS is invalid, the data will not be sent until nCTS is valid.

If the USART_CTRL3.CTSEN bit is set, the USART_STS.CTSF bit will be set high by hardware when the nCTS input changes state. An interrupt will be generated if USART_CTRL3.CTSIEN is enabled.

Figure 23-11 CTS flow controls



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23.4.9 Multiprocessor Communication

USART allows multiprocessor communication. The principle is: multiple processors communicate through USART, and it is necessary to determine who is the master device, and the remaining processors are all slave devices. The TX output of the master device is directly connected to the RX port of all slave device. The TX outputs of the slaves are logically AND together and connected to the RX inputs of the master.

When multi-processor communication is performed, the slave devices are all in mute mode, and the host uses a specific method to wake up a slave device to be communicated when needed, so that the slave device is in an active state and transmits data with the master device.

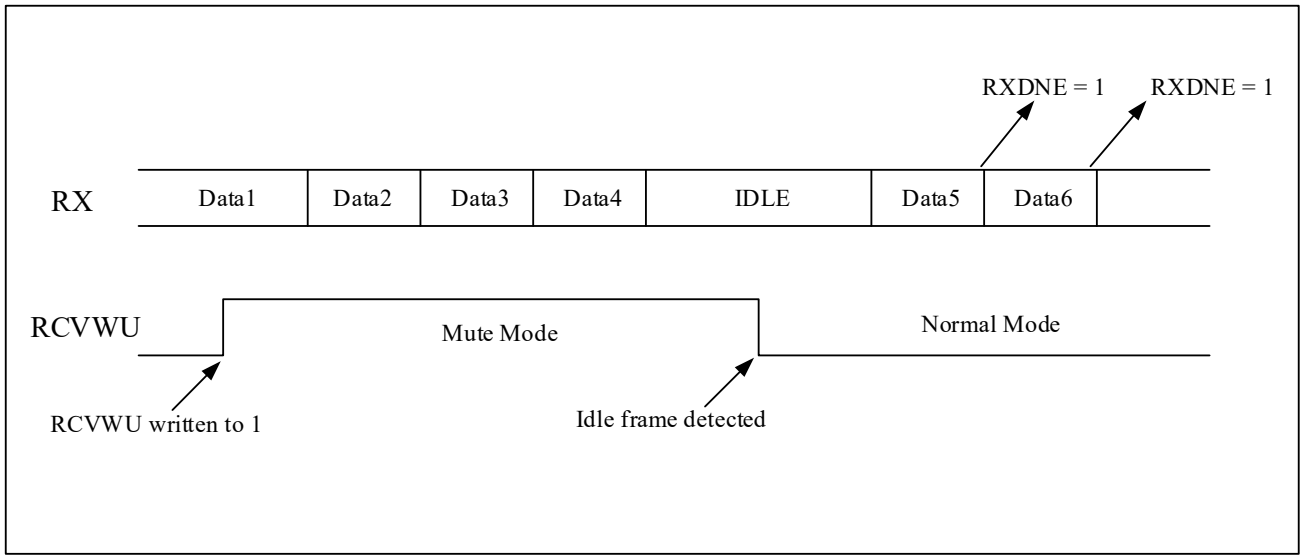
The USART can wake up from mute mode by idle line detection or address mark detection.

23.4.9.1 Idle line detection

The idle line detection configuration process is as follows:

1. Configure the USART_CTRL1.WUM bit to 0, and the USART performs idle line detection;
2. When USART_CTRL1.RCVWU is set (which can be automatically controlled by hardware or written by software under certain conditions), USART enters mute mode. In mute mode, none of the receive status bits are set, and all receive interrupts are disabled;
3. As shown in the Figure 23-12 below, when an idle frame is detected, USART is woken up, and then USART_CTRL1.RCVWU is cleared by hardware. At this time, USART_STS.IDLEF is not set.

Figure 23-12 Mute mode using idle line detection



23.4.9.2 Address mark detection

By configuring the USART_CTRL1.WUM bit to 1, the USART performs address mark detection. The address of the receiver is programmable through the USART_CTRL2.ADDR[3:0] bits. If the MSB is 1, the byte is considered an address, otherwise it is considered data.

In this mode, the USART can enter mute mode by:

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- When the receiver does not contain data, USART_CTRL1.RCVWU can be written to 1 by software, and USART enters mute mode;

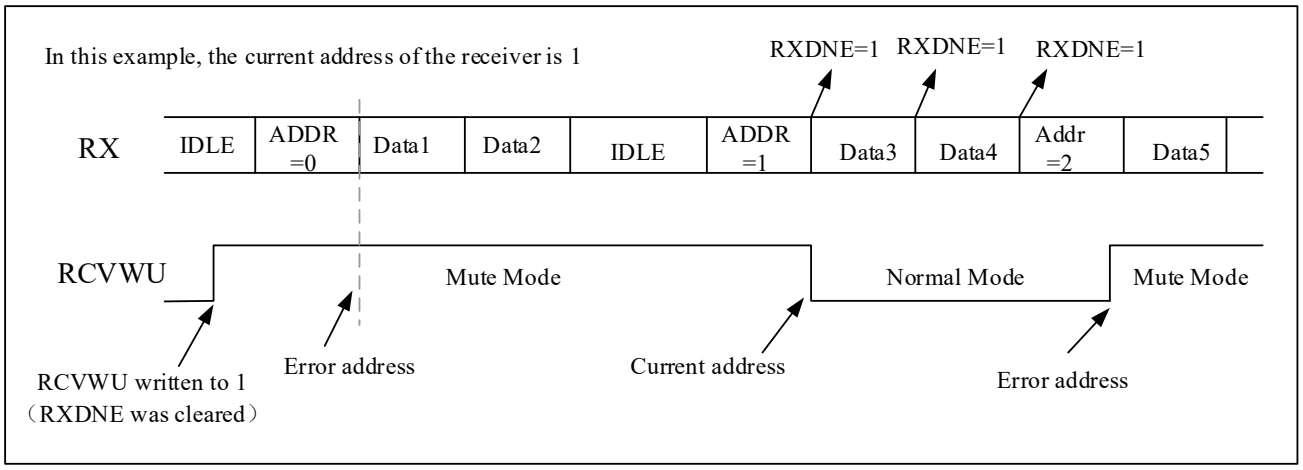
  Note: When the receive buffer contains no data (RXNE=0 in USART_SR), the USART_CTRL1.RCVWU bit can be written to 0 or 1. Otherwise, the write operation is ignored.

- When the received address does not match the address of the USART_CTRL2.ADDR[3:0] bits, USART_CTRL1.RCVWU is written to 1 by hardware.

In mute mode, none of the receive status bits are set and all receive interrupts are disabled.

When the received address matches the address of the USART_CTRL2.ADDR[3:0] bits, the USART is woken up and USART_CTRL1.RCVWU is cleared. The USART_STS.RXDNE bit will be set when this matching address is received. Data can then be transmitted normally.

Figure 23-13 Mute mode detected using address mark



23.4.10 Synchronous Mode

USART supports synchronous serial communication. The USART only supports the master mode, and cannot use the input clock from other devices to receive and transmit data. Synchronous mode can be enabled by configuring the USART_CTRL2.CLKEN bit.

Note: When using synchronous mode, USART_CTRL2.LINMEN, USART_CTRL3.SCMEN, USART_CTRL3.HDMEN, USART_CTRL3. IRDAMEN, these bits need to be kept clear.

23.4.10.1 Synchronized clock

The CK pin is the output of the USART transmitter clock. During the bus idle period, before the actual data arrives and when the break symbol is sent, the clock not output.

Clock phase and polarity are software programmable and need to be configured when both the transmitter and receiver are disabled. When the clock polarity is 0 (USART_CTRL2.CLKPOL=0), the default level of CLK is low; when the clock polarity is 1 (USART_CTRL2.CLKPOL=1), the default level of CLK is high. When the phase polarity is 0 (USART_CTRL2.CLKPHA=0), the data is sampled on the first edge of the clock; when the phase polarity is 1 (USART_CTRL2.CLKPHA=1), the data is sampled on the second edge.

During the start and stop bits, the CK pin does not output clock pulses.

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A sync data cannot be received when no data is sent. Because the clock is only available when the transmitter is activated and data is written to the USART_DAT register.

The USART_CTRL2.LBCLK bit controls whether to output the clock pulse corresponding to the last data byte (MSB) sent on the CK pin. This bit needs to be configured when both the transmitter and receiver are disabled. If USART_CTRL2.LBCLK is 1, the clock pulse of the last bit of data will be output from CK. If USART_CTRL2.LBCLK is 0, the clock pulse of the last bit of data is not output from CK.

23.4.10.2 Synchronized transmitting

The transmitter in synchronous mode works the same as in asynchronous mode. Data on the TX pin is sent out synchronously with CK.

23.4.10.3 Synchronized receiving

The receiver in synchronous mode works differently than in asynchronous mode. Data is sampled on CK without any oversampling. But setup time and hold time (depending on baud rate, 1/16 bit time) must be considered.

Figure 23-14 USART synchronous transmission example

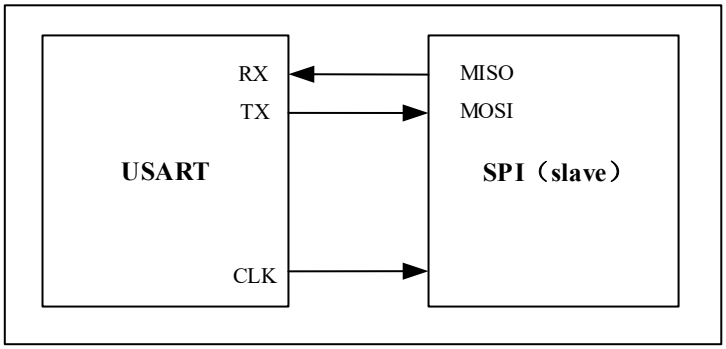

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Figure 23-15 USART data clock timing example (WL=0)

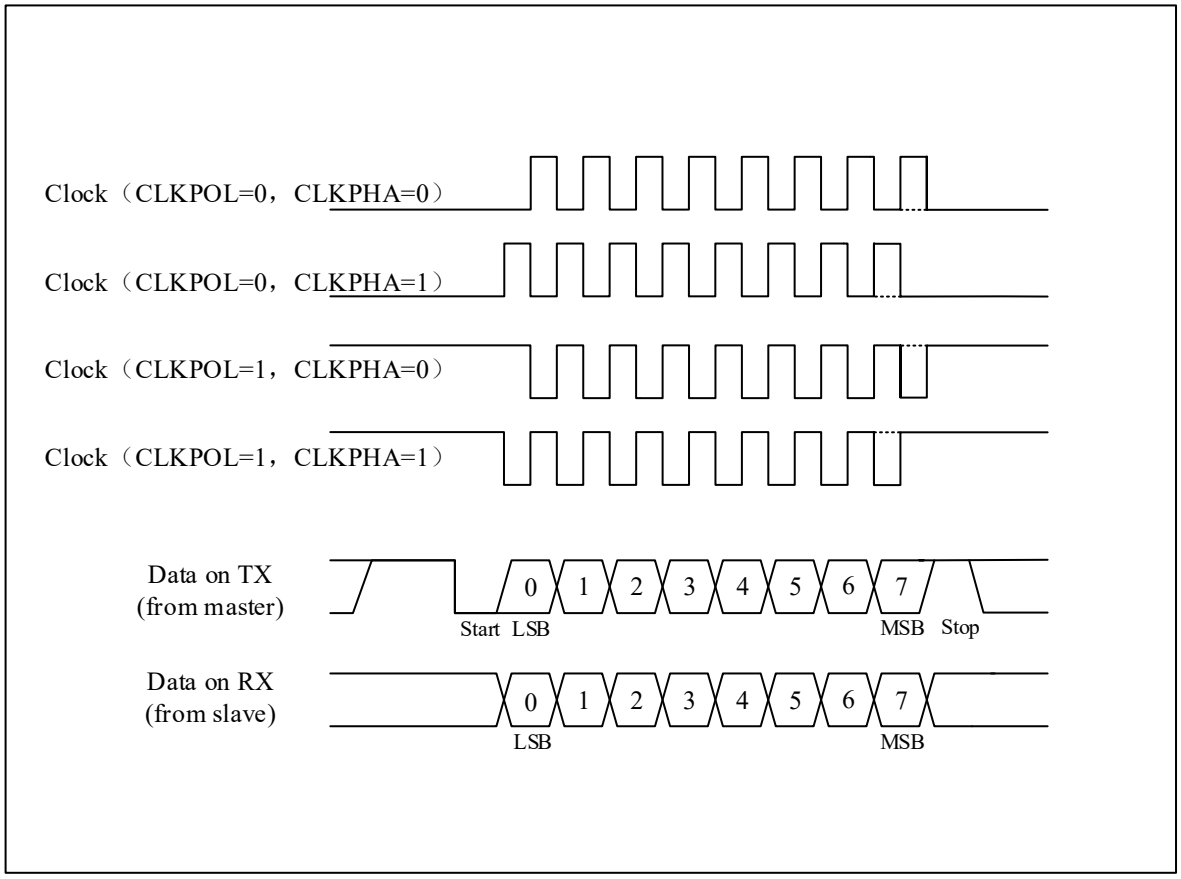

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Figure 23-16 USART data clock timing example (WL=1)

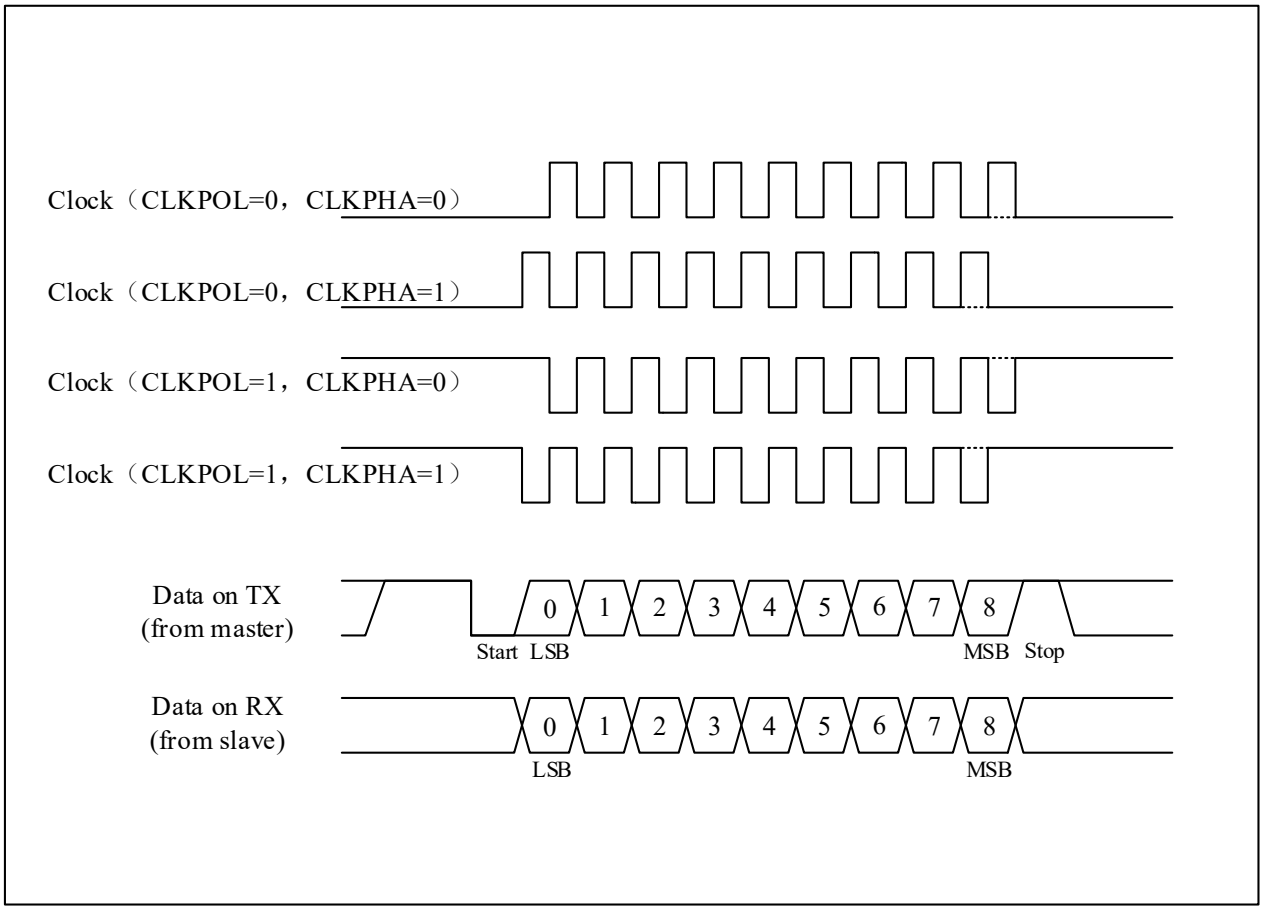
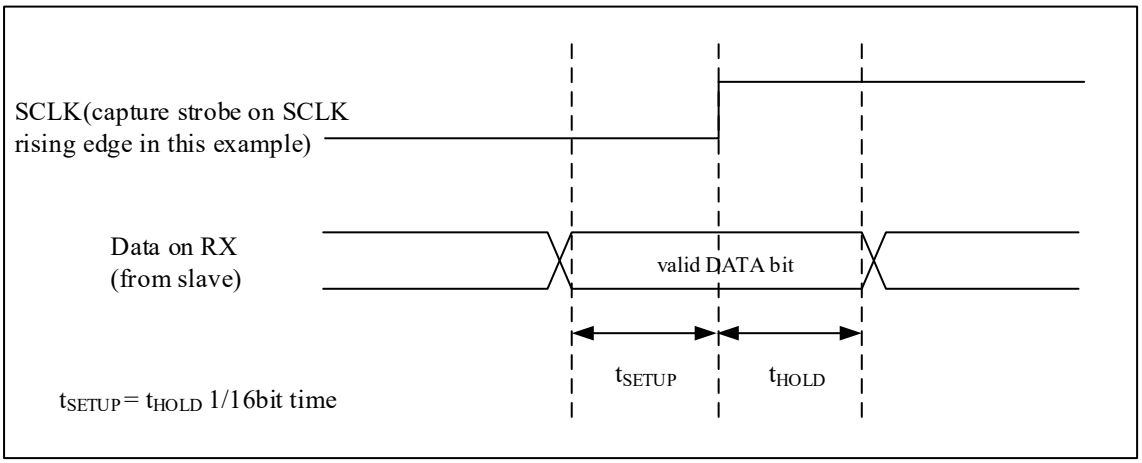


Figure 23-17 RX data sampling / holding time



Note: the function of CK is different in Smartcard mode, please refer to the Smartcard mode section for details.

23.4.11 Single-wire Half-duplex Mode

USART supports single-wire half-duplex communication, allowing data to be transmitted in both directions, but only allows data to be transmitted in one direction at the same time. Communication conflicts are managed by software.

Through the USART_CTRL3.HDMEN bit, you can choose whether to enable half-duplex mode. When using single-

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wire half-duplex, USART_CTRL2. CLKEN, USART_CTRL2. LINMEN, USART_CTRL3. SCMEN, USART_CTRL3. IRDAMEN, these bits should be kept clear.

After the half-duplex mode is turned on, the TX pin and the RX pin are interconnected inside the chip, and the Rx pin is no longer used. When there is no data to transmit, TX is always released. Therefore, when not driven by the USART, the TX pin must be configured as a floating input or an open-drain output high.

23.4.12 IrDA SIR ENDEC Mode

USART supports the IrDA (Infrared Data Association) SIR ENDEC specification.

Through the USART_CTRL3. IRDAMEN bit, you can choose whether to enable the infrared mode. When using the infrared function, USART_CTRL2.CLKEN, USART_CTRL2.STPB[1:0], USART_CTRL2.LINMEN, USART_CTRL3.HDMEN, USART_CTRL3.SCMEN, these bits should be kept clear.

Through the USART_CTRL3. IRDALP bit, it can be used to select normal mode or low power infrared mode.

23.4.12.1 IrDA normal mode

When USART_CTRL3.IRDALP=0, select normal infrared mode.

IrDA is a half-duplex communication protocol, so there should be a minimum delay of 10ms between sending and receiving.that uses a inverted return-to-zero modulation scheme (RZI), which uses an infrared light pulse to represent a logic '0', and the pulse width is specified as 3/16 of a bit period in normal mode, as shown in the Figure 23-19.USART only supports up to 115200bps for SIR ENDEC.

The USART sends data to the SIR encoder, and the bit stream output by the USART will be modulated. A modulated stream of pulses is sent from the infrared transmitter and then received by the infrared receiver. The SIR receiver decoder demodulates it and outputs the data to the USART.

The transmit encoder output has opposite polarity to the decoder input. When idle, SIR transmit is low, while SIR receive is high. The high pulse sent by SIR is '0' and the low level is '1', while SIR reception is the opposite.

If the USART is sending data to the IrDA transmit encoder, then the IrDA receive decoder will ignore any data on the IrDA receive line. If the USART is receiving data sent from the SIR receiver decoder, the data sent by the USART to the IrDA transmitter encoder will not be encoded.

Pulse width is programmable. The IrDA specification requires pulses to be wider than 1.41us. For pulse widths less than 2 cycles, the receiver will filter them out. PSCV is the prescaler value programmed in the USART_GTP register.

23.4.12.2 IrDA low power mode

When USART_CTRL3.IRDALP=1, select low power infrared mode.

For the transmitter, when in low power mode, the pulse width is 3 times the low power baud rate, which is a minimum of 1.42MHz. Typically this value is 1.8432MHz (1.42 MHz < PSC < 2.12 MHz).

For the receiver, the requirement for a valid signal is that the duration of the low level signal must be greater than 2 cycles of the IrDA low power baud rate clock.

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Figure 23-18 IrDASIRENDEC-Block diagram

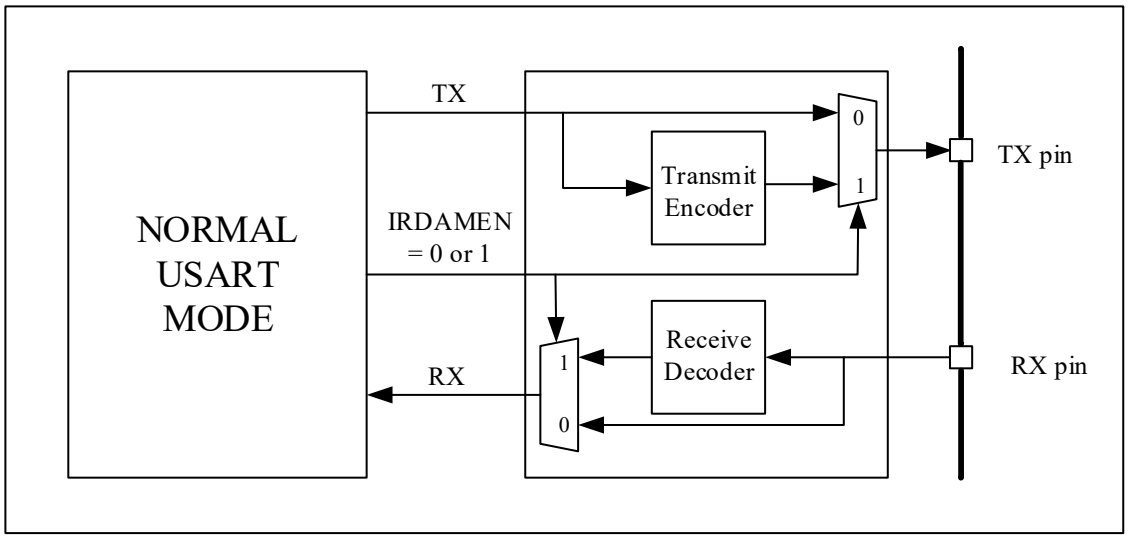
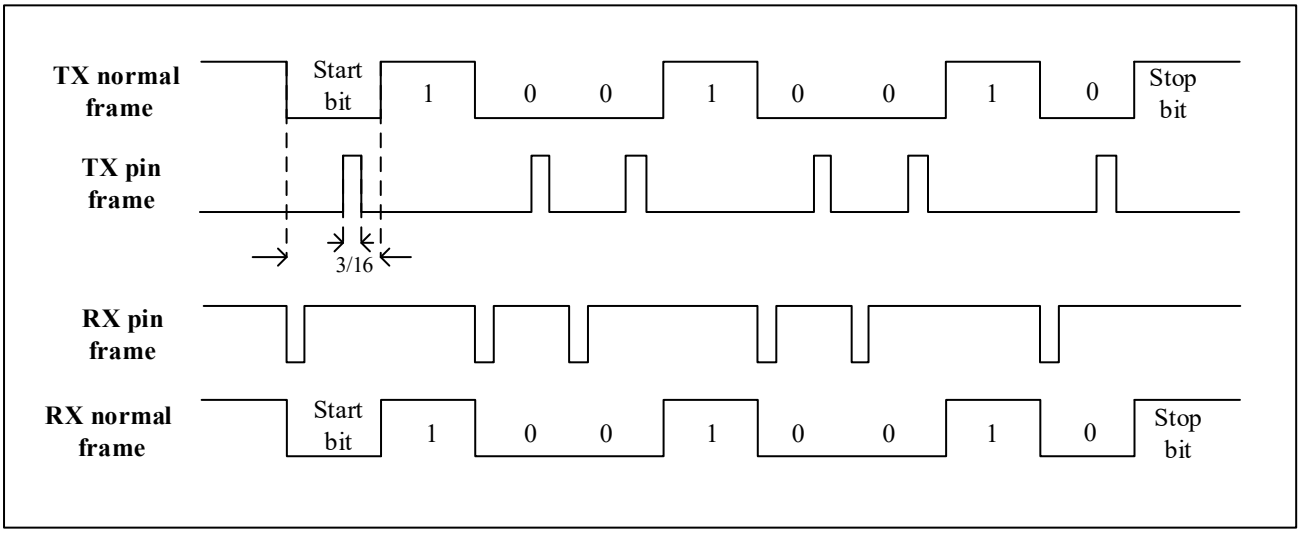


Figure 23-19 IrDA data Modulation (3/16)-normal mode



23.4.13 LIN Mode

USART supports the ability of a LIN(Local interconnection Network) master to send a synchronization break and the ability of a LIN slave to detect a break. LIN mode can be enabled by configuring the USART_CTRL2.LINMEN bit.

Note: When using LIN mode, USART_CTRL2.STPB[1:0], USART_CTRL2.CLKEN, USART_CTRL3.SCMEN, USART_CTRL3.HDMEN, USART_CTRL3. IRDAMEN, these bits should be kept clear.

23.4.13.1 LIN transmitting

When LIN is sent, the length of the data bits sent can only be 8 bits. By setting USART_CTRL1.SDBRK, a 13-bit '0' will be sent as the break symbol, and insert a stop bit.

23.4.13.2 LIN receiving

Whether the bus is idle or during the transmission of a data frame, as long as the break frame appears, it can be detected. the break symbol detection is independent of the USART receiver.

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By configuring the USART_CTRL2.LINBDL bit, 10-bit or 11-bit break character detection can be selected.

After the receiver detects the start bit, the circuit samples each subsequent bit at the 8th, 9th, and 10th oversampling clock points of each bit. When 10 or 11 consecutive bits are detected as '0' and followed by a delimiter, it means that a LIN break is detected, and USART_STS.LINBDF is set. Before confirming the break symbol, check the delimiter as it means the RX line has gone back to high.An interrupt is generated if the LIN breaker detection interrupt (USART_CTRL2.LINBDIEN) is enabled.

If a '1' is sampled before the 10th or 11th sample point, the current detection is canceled and the start bit is searched again.

Figure 23-20 Break detection in LIN mode (11-bit break length-the LINBDL bit is set)

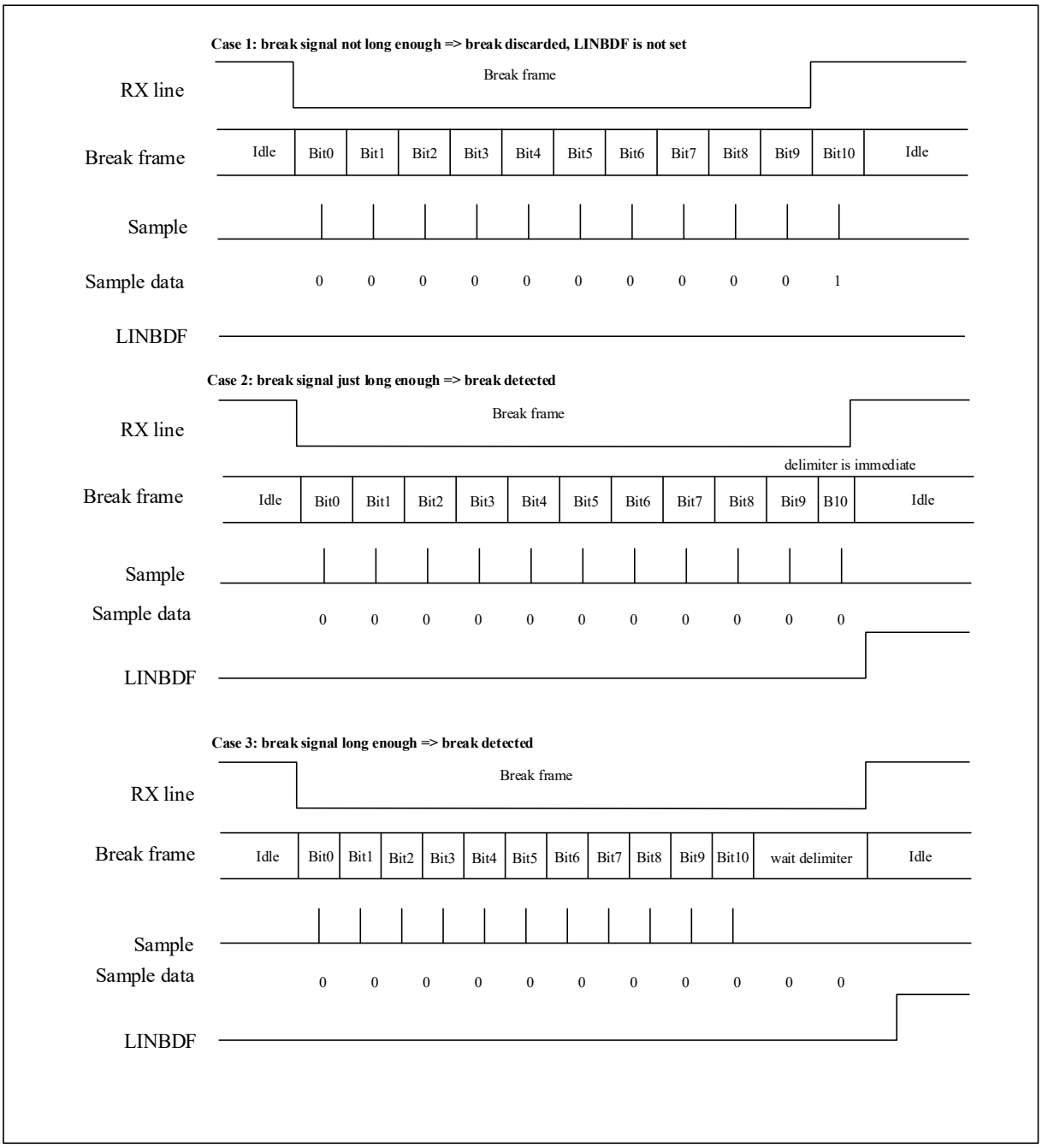

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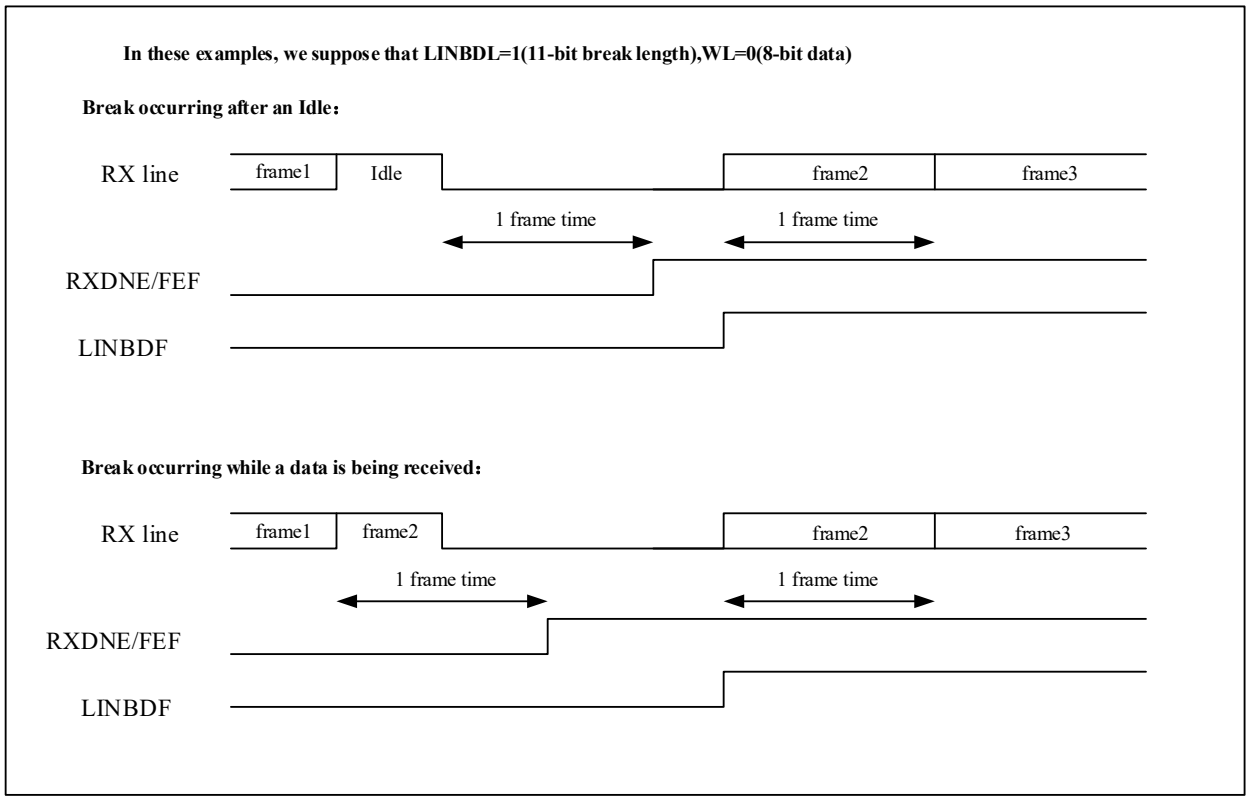
Figure 23-21 Break detection and framing error detection in LIN mode



23.4.14 Smartcard Mode (ISO7816)

USART supports smart card protocol. The smart card interface supports the asynchronous smart card protocol defined in the ISO7816-3 standard.

Through the USART_CTRL3.SCMEN bit, you can choose whether to enable smart card mode. When using smart card mode, USART_CTRL2.LINMEN, USART_CTRL3.HDMEN, USART_CTRL3.IRDAMEN, these bits should be kept clear.

In smart card mode, the USART can provide a clock through the CK pin. The system clock is divided by the prescaler register to provide the clock to the smart card. The CK frequency can be from $f_{CK}/2$ to $f_{CK}/62$, where f_{CK} is the peripheral input clock.

In smart card mode, 0.5 and 1.5 stop bits can be used when receiving data, and only 1.5 stop bits can be used when sending data. So 1.5 stop bits are recommended as this avoids configuration transitions.

In smart card mode, the data bits should be configured as 8 bits, and the parity bit should be configured.

When a parity error is detected by receiver, the transmit data line is pulled low for one baud clock cycle at the end of the stop bit as NACK signal(If USART_CTRL3.SCNACK is set). This NACK signal will generate a framing error on the transmit side (transmit side is configured with 1.5 stop bits).

When the transmitter receives a NACK signal (framing error) from the receiver, it does not detect the NACK as a start bit (according to the ISO protocol, the duration of the received NACK can be 1 or 2 baud clock cycles).

The example given in the following figure illustrates the signal on the data line with and without parity errors.

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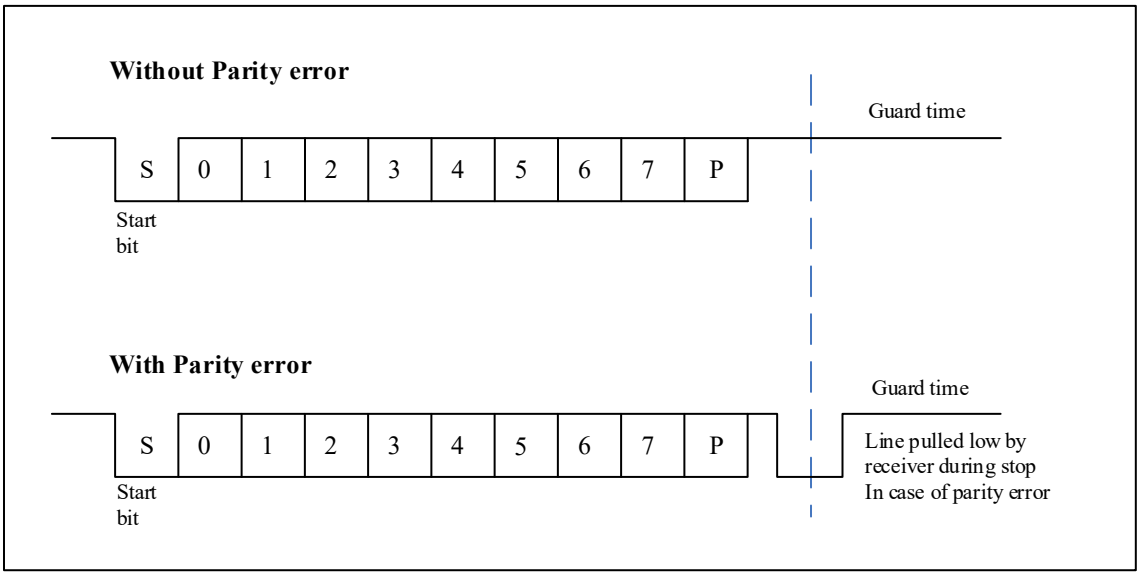
Figure 23-22 ISO7816-3 Asynchronous Protocol



The break frame has no meaning in smart card mode. A 00h data with a framing error will be treated as data instead of a break symbol.

Under normal operation, data will be shifted out of the transmit shift register on the next baud clock. The smart card mode is delayed by a minimum of 1/2 baud clock than normal operation.

In normal operation, USART_STS.TXC is set when a frame containing data is sent and USART_STS.TXDE=1.In smart card mode, the transmission completion flag (USART_STS.TXC) is set high when the guard time counter reaches the value (USART_GTP.GTV[7:0]). The clearing of the USART_STS.TXC flag is not affected by the smart card mode.

The following figure details how USART samples NACK signals.

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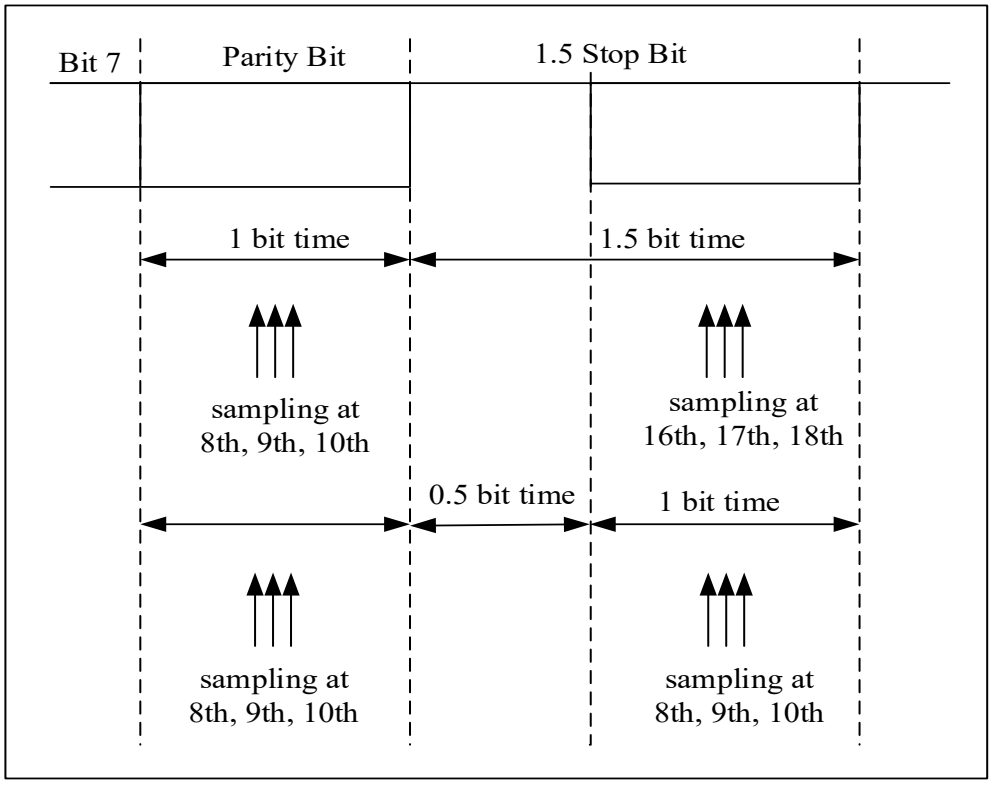
Figure 23-23 Use 1.5 stop bits to detect parity errors



23.5 Interrupt Request

The various interrupt events of USART are logical OR relations, if the corresponding enable control bit is set, these events can generate their own interrupts, but only one interrupt request can be generated at the same time.

Table 23-7 USART interrupt request

Interrupt function	Interrupt event	Event flag	Enable bit
USART global interrupt	Transmission data register is empty.	TXDE	TXDEIEN
	CTS flag	CTSF	CTSIEN
	Transmission complete	TXC	TXCIEN
	Receive data ready to be read	RXDNE	RXDNEIEN
	Data overrun error detected.	ORERR	
	Idle line detected	IDLEF	IDLEIEN
	Parity error	PEF	PEIEN
	Disconnect flag	LINBDF	LINBDIEN
	Noise, overrun error and framing error in multi-buffer communication	NEF/OREF/FEF	ERRIEN(1)

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(1) This flag bit is used only when DMA is used to receive data(USART_CTRL3.DMARXEN=1).

23.6 Mode Support

Table 23-8 USART mode setting (1)

Communication mode	USART1	USART2	USART3	UART4	UART5	UART6	UART7
Asynchronous mode	Y	Y	Y	Y	Y	Y	Y
Multiprocessor	Y	Y	Y	Y	Y	Y	Y
LIN mode	Y	Y	Y	Y	Y	Y	Y
Synchronous mode	Y	Y	Y	N	N	N	N
Single-wire half duplex mode	Y	Y	Y	Y	Y	Y	Y
Smartcard mode	Y	Y	Y	N	N	N	N
IrDA infrared mode	Y	Y	Y	Y	Y	Y	Y
DMA communication mode	Y	Y	Y	Y	Y	Y	Y
Hardware flow control mode	Y	Y	Y	N	N	N	N

(1) Y = support this mode, N = do not support this mode

23.7 USART Registers

23.7.1 USART Register Overview

Table 23-9 USART register overview

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
000h	USART_STS	Reserved																						CTSF	LINBDF	TXDE	TXC	RXDNE	IDLEF	OREF	NEF	FEF	PEF
	Reset Value																							0	0	1	1	0	0	0	0	0	0
004h	USART_DAT	Reserved																						DATV[8:0]									
	Reset Value																							0	0	0	0	0	0	0	0	0	0
008h	USART_BRCF	Reserved																DIV_Integer[11:0]												DIV_Decimal [3:0]			
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
00Ch	USART_CTRL1	Reserved																		UEN	WL	WUM	PCEN	PSEL	PEIEN	TXDEIEN	TXCIEN	RXDNEIEN	IDLEIEN	TXEN	RXEN	RCVWU	SDBRK
	Reset Value																			0	0	0	0	0	0	0	0	0	0	0	0	0	0
010h	USART_CTRL2	Reserved																	LINMEN	STPB [1:0]		CLKEN	CLKPOL	CLKPHA	LBCLK	Reserved	LINBDIEN	LINBDL	Reserved	ADDR[3:0]			

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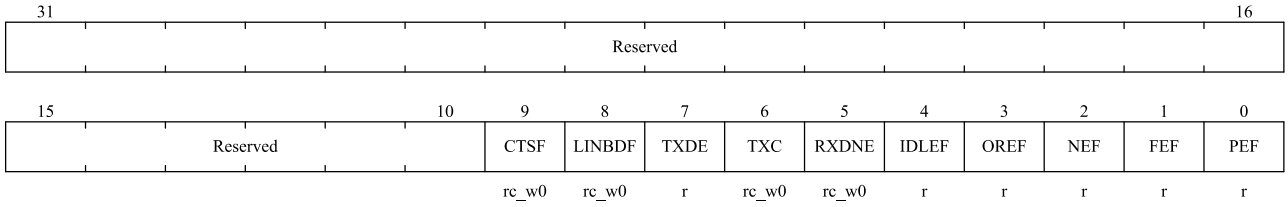
Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reset Value																		0	0	0	0	0	0	0		0	0		0	0	0	0
014h	USART_CTRL3	Reserved																					CTSIEN	CTSEN	RTSEN	DMATXEN	DMARXEN	SCMEN	SCNACK	HDMEN	IRDALP	IRDAMEN	ERRIEN
	Reset Value																						0	0	0	0	0	0	0	0	0	0	0
018h	USART_GTP	Reserved																GTV[7:0]								PSCV[7:0]							
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

23.7.2 USART Status Register (USART_STS)

Address offset : 0x00

Reset value : 0x0000 00C0



Bit field	Name	Description
31:10	Reserved	Reserved, the reset value must be maintained
9	CTSF	CTS flag If USART_CTRL3.CTSEN bit is set, this bit is set by hardware when the nCTS input changes. If USART_CTRL3.CTSIEN bit is set, an interrupt will be generated. This bit is cleared by software. 0:nCTS status line has not changed. 1:nCTS status line changes. *Note: This bit is invalid for UART4/5/6/7.*
8	LINBDF	LIN break detection flag. If USART_CTRL2.LINMEN bit is set, this bit is set by hardware when LIN disconnection is detected. If USART_CTRL2.LINBDIEN bit is set, an interrupt will be generated. This bit is cleared by software. 0: LIN break character not detected. 1: LIN break character detected.
7	TXDE	The Transmit data register empty. Set to 1 after power-on reset or data to be sent has been sent to the shift register. Setting USART_CTRL1.TXDEIEN will generate an interrupt. This bit is cleared to 0 when the software writes the data to be sent into USART_DAT. 0: Send data buffer is not empty. 1: The transmitting data buffer is empty.
6	TXC	Transmission complete. This bit is set to 1 after power-on reset. If USART_STS.TXDE is set, this bit is set when

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Bit field	Name	Description
		the current data transmission is completed. Setting USART_CTRL1.TXCIEN bit will generate an interrupt. This bit is cleared by software. 0: Transmitting did not complete. 1: Send completed.
5	RXDNE	The Read data register not empty. This bit is set when the read data buffer receives data from the shift register. When USART_CTRL1.RXDNEIEN bit is set, an interrupt will be generated. Software can clear this bit by writing 0 to it or reading the USART_DAT register. 0: The read data buffer is empty. 1: The read data buffer is not empty.
4	IDLEF	IDLE line detected flag. Within one frame time, the idle state is detected at the RX pin, and this bit is set to 1. When USART_CTRL1.IDLEIEN bit is set, an interrupt will be generated. The software can clear this bit by reading USART_STS first and then reading USART_DAT. 0: No idle frame detected. 1: idle frame detected. *Note: IDLEF bit will not be set high again until USART_STS.RXDNE bit is set (that is, an idle line is detected again).*
3	OREF	Overrun error With RXDNE set, this bit is set if the USART_DAT register receives data from the shift register. When USART_CTRL3.ERRIEN bit is set, an interrupt will be generated. The software can clear this bit by reading USART_STS first and then reading USART_DAT. 0: No overrun error was detected. 1: Overflow error detected.
2	NEF	Noise error flag. When noise is detected in the received frame, this bit is set by hardware. It is cleared by the software sequence (read first USART_STS, read USART_DAT again). 0: No noise error detected. 1: Noise error detected. *Note: this bit will not generate an interrupt because it appears with USART_STS.RXDNE, and the hardware will generate an interrupt when setting the USART_STS.RXDNE flag. In the multi-buffer communication mode, if the USART_CTRL3.ERRIEN bit is set, an interrupt will be generated when the NEF flag is set.*
1	FEF	Framing error. When the data is not synchronized or a large amount of noise is detected, and the stop bit is not received and recognized at the expected time, it will be judged that a framing error has been detected, and this bit will be set to 1. First read USART_STS, then read USART_DAT can cleared this bit. 0: No framing errors were detected.

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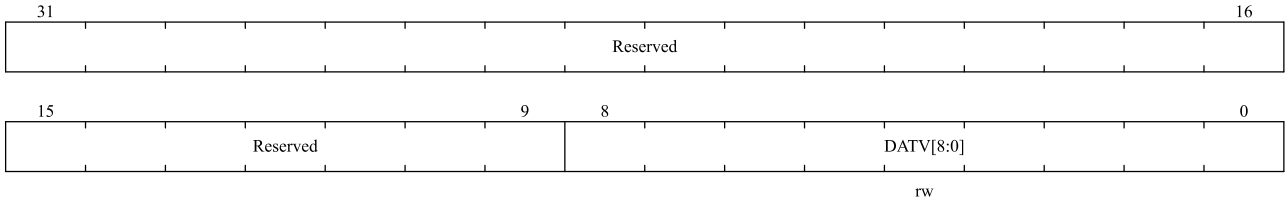
Bit field	Name	Description
		1: A framing error or a Break Character is detected. *Note: this bit will not generate an interrupt because it appears with USART_STS.RXDNE, and the hardware will generate an interrupt when setting the USART_STS.RXDNE flag. If the currently transmitted data has both framing errors and overload errors, the hardware will continue to transmit the data and only set the USART_STS.OREF flag bit.* *In the multi-buffer communication mode, if the USART_CTRL3.ERRIEN bit is set, an interrupt will be generated when the FEF flag is set.*
0	PEF	Parity error. This bit is set when the parity bit of the received data frame is different from the expected check value. The software can clear this bit by reading USART_STS first and then reading USART_DAT. 0: No parity error was detected. 1: Parity error detected.

23.7.3 USART Data Register (USART_DAT)

Address offset : 0x04

Reset value : undefined (uncertain value)



Bit field	Name	Description
31:9	Reserved	Reserved, the reset value must be maintained
8:0	DATV[8:0]	Data value Contains the data sent or received; Software can change the transmitted data by writing these bits, or read the values of these bits to obtain the received data. If parity is enabled, when the transmitted data is written into the register, the highest bit of the data (the 7th or 8th bit depends on USART_CTRL1.WL bit) will be replaced by the parity bit.

23.7.4 USART Baud Rate Register (USART_BRCF)

Address offset : 0x08

Reset value : 0x0000 0000

Note: When USART_CTRL1.UEN=1, this register cannot be written;The baud counter stops counting if USART_CTRL1.TXEN or USART_CTRL1.RXEN are disabled respectively.

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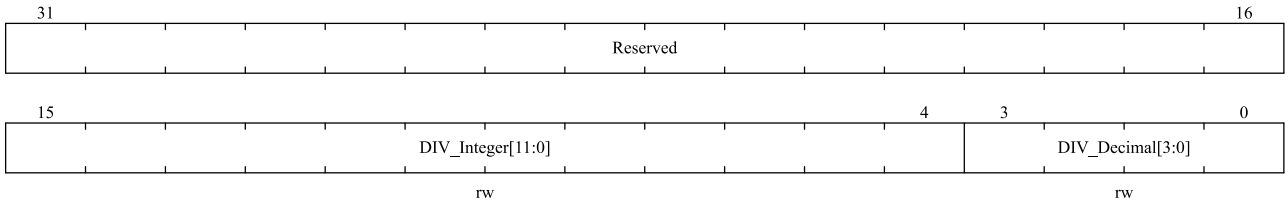
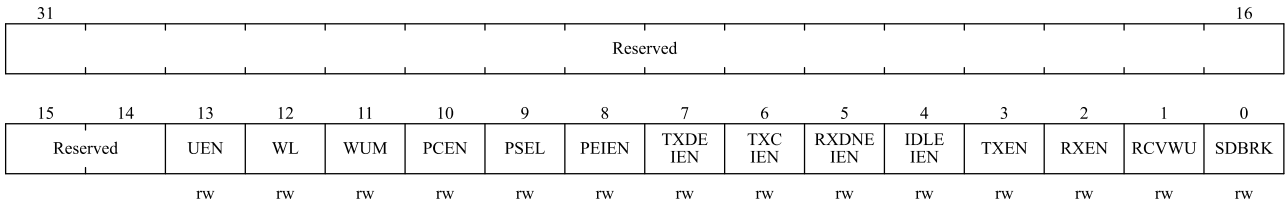


Bit field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained
15:4	DIV_Integer[11:0]	Integer part of baud rate divider.
3:0	DIV_Decimal[3:0]	Fractional part of baud rate divider.

23.7.5 USART Control Register 1 Register (USART_CTRL1)

Address offset : 0x0C

Reset value : 0x0000 0000



Bit field	Name	Description
31:14	Reserved	Reserved, the reset value must be maintained
13	UEN	USART enable When this bit is cleared, the divider and output of USART stop working after the current byte transmission is completed to reduce power consumption. Software can set or clear this bit. 0:USART is disabled. 1:USART is enabled.
12	WL	Word length. 0:8 data bits. 1:9 data bits. *Note: If data is in transit, this bit cannot be configured.*
11	WUM	Wake up mode from mute mode. 0: Idle frame wake up. 1: Address identifier wake up.
10	PCEN	Parity control enable 0: Parity control is disabled. 1: Parity control is enabled.
9	PSEL	Parity selection. 0: even check. 1: odd check.

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Bit field	Name	Description
8	PEIEN	PE interrupt enable If this bit is set to 1, an interrupt is generated when USART_STS.PEF bit is set. 0: Parity error interrupt is disabled. 1: Parity error interrupt is enabled.
7	TXDEIEN	TXDE interrupt enable If this bit is set to 1, an interrupt is generated when USART_STS.TXDE bit is set. 0: Send buffer empty interrupt is disabled. 1: Send buffer empty interrupt is enabled.
6	TXCIEN	Transmit complete interrupt enable. If this bit is set to 1, an interrupt is generated when USART_STS.TXC is set. 0: Transmission completion interrupt is disabled. 1: Transmission completion interrupt is enabled.
5	RXDNEIEN	RXDNE interrupt enable If this bit is set to 1, an interrupt is generated when USART_STS.RXDNE or USART_STS.OREF is set. 0: Data buffer non-empty interrupt o and overrun error interrupt are disabled. 1: Data buffer non-empty interrupt o and overrun error interrupt are enabled.
4	IDLEIEN	IDLE interrupt enable. If this bit is set to 1, an interrupt is generated when USART_STS.IDLEF is set. 0:IDLE line detection interrupt is disabled. 1: IDLE line detection interrupt is enabled.
3	TXEN	Transmitter enable. 0: The transmitter is disabled. 1: the transmitter is enabled.
2	RXEN	Receiver enable 0: The receiver is disabled. 1: the receiver is enabled.
1	RCVWU	The receiver wakes up Software can set this bit to 1 to make USART enter mute mode, and clear this bit to 0 to wake up USART. In idle frame wake-up mode (USART_CTRL1.WUM=0), this bit is cleared by hardware when an idle frame is detected. In address wake-up mode (USART_CTRL1.WUM=1), when an address matching frame is received, this bit is cleared by hardware. Or when an address mismatch frame is received, it is set to 1 by hardware. 0: The receiver is in normal operation mode. 1: The receiver is in mute mode.
0	SDBRK	Send Break Character. The software transmits a break character by setting this bit to 1. This bit is cleared by hardware during stop bit of the break frame transmission. 0: No break character was sent. 1: Send a break character.

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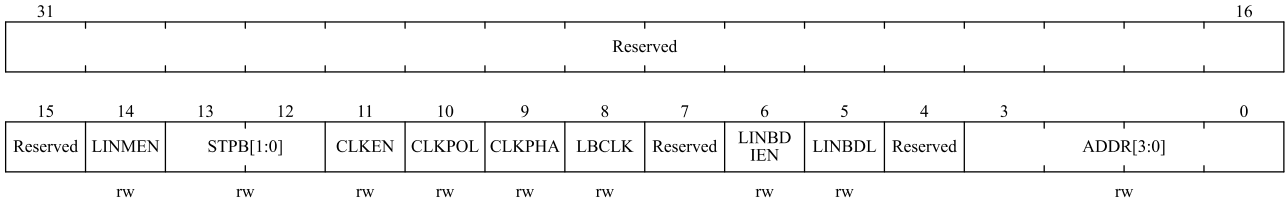
23.7.6 USART Control Register 2 Register (USART_CTRL2)

Address offset : 0x10

Reset value : 0x0000 0000



Bit field	Name	Description
31:15	Reserved	Reserved, the reset value must be maintained
14	LINMEN	LIN mode enable 0:LIN mode is disabled 1:LIN mode enabled
13:12	STPB[1:0]	STOP bits. 00:1 stop bit. 01:0.5 stop bit. 10:2 stop bit. 11:1.5 stop bit. *Note: For UART4/5/6/7, only one stop bit and two stop bits are valid.*
11	CLKEN	Clock enable 0:CK pin is disabled 1:CK pin enabled *Note: This bit cannot be used for UART4/5/6/7.*
10	CLKPOL	Clock polarity. This bit is used to set the polarity of CK pin in synchronous mode. 0: CK pin remains low when it is not transmitted to the outside. 1: CK pin remains high when it is not sent to the outside. *Note: This bit is invalid for UART4/5/6/7.*
9	CLKPHA	Clock phase. This bit is used to set the phase of CK pin in synchronous mode. 0: Sample the first data at the first clock edge. 1: Sample the first data at the second clock edge. *Note: This bit cannot be used for UART4/5/6/7.*
8	LBCLK	The Last bit clock pulse. This bit is used to set whether the clock pulse corresponding to the last transmitted data byte (MSB) is output on CK pin in synchronous mode. 0: The clock pulse of the last bit of data is not output from CK. 1: The clock pulse of the last bit of data will be output from CK. *Note: This bit cannot be used for UART4/5/6/7.*
7	Reserved	Reserved, the reset value must be maintained

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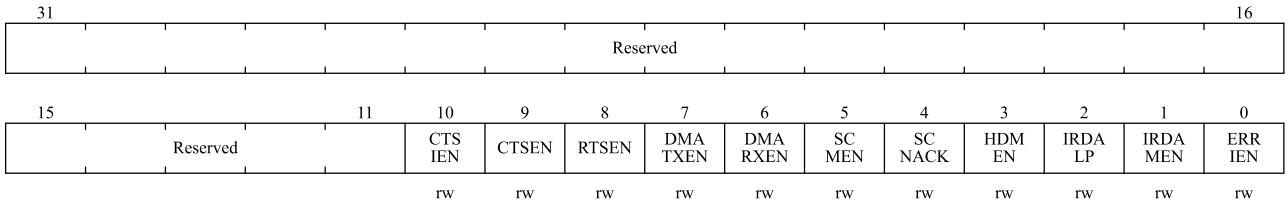
Bit field	Name	Description
6	LINBDIEN	LIN break detection interrupt enable. If this bit is set to 1, an interrupt will be generated when USART_STS.LINBDF bit is set. 0: Disconnect signal detection interrupt is disabled. 1: Turn-off signal detection interrupt enabled
5	LINBDL	LIN break detection length. This bit is used to set the length of the break frame. 0:10 bit break detection 1:11 bit break detection *Note: LINBDL can be used to control the detection length of Break Characters in LIN mode and other modes, and the detection length is the same as that in LIN mode.*
4	Reserved	Reserved, the reset value must be maintained
3:0	ADDR[3:0]	USART address. Used in the mute mode of multiprocessor communication, using address identification to wake up a USART device. In address wake-up mode (USART_CTRL1.WUM=1), if the lower four bits of the received data frame are not equal to the ADDR[3:0] value, USART will enter the mute mode; If the lower four bits of the received data frame are equal to the ADDR[3:0] value, USART will be awakened.

23.7.7 USART Control Register 3 Register (USART_CTRL3)

Address offset : 0x14

Reset value : 0x0000 0000



Bit field	Name	Description
31:11	Reserved	Reserved, the reset value must be maintained
10	CTSIEN	CTS interrupt enable. If this bit is set to 1, an interrupt will be generated when USART_STS.CTSF bit is set. 0:CTS interrupt is disabled. 1:CTS interrupt is enabled. *Note: This bit cannot be used for UART4/5/6/7*
9	CTSEN	CTS enable. This bit is used to enable the CTS hardware flow control function. 0:CTS hardware flow control is disabled. 1:CTS hardware flow control is enabled. *Note: This bit cannot be used for UART4/5/6/7*

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Bit field	Name	Description
8	RTSEN	RTS enable. This bit is used to enable RTS hardware flow control function. 0:RTS hardware flow control is disabled. 1:RTS hardware flow control is enabled. *Note: This bit cannot be used for UART4/5/6/7*
7	DMATXEN	DMA transmitter enable. 0:DMA transmission mode is disabled. 1:DMA transmission mode is enabled.
6	DMARXEN	DMA receiver enable. 0:DMA receive mode is disabled. 1:DMA receive mode is enabled.
5	SCMEN	Smartcard mode enable. This bit is used to enable Smartcard mode. 0: Smartcard mode is disabled. 1: Smartcard mode is enabled. *Note: This bit cannot be used for UART4/5/6/7*
4	SCNACK	Smartcard NACK enable. This bit is used for Smartcard mode to enable transmitting NACK when parity error occurs. 0: Do not send NACK when there is a parity error. 1: send NACK when there is a parity error. *Note: This bit cannot be used for UART4/5/6/7*
3	HDMEN	Half-duplex mode enable. This bit is used to enable half-duplex mode. 0: Half-duplex mode is disabled. 1: Half-duplex mode is enabled.
2	IRDALP	IrDA low-power mode. This bit is used to select the low power consumption mode for IrDA mode. 0: Normal mode. 1: Low power mode.
1	IRDAMEN	IrDA mode enable. 0:IrDA is disabled. 1:IrDA is enabled.
0	ERRIEN	Error interrupt enable. When DMA receive mode (USART_CTRL3.DMARXEN=1) is enabled, an interrupt will be generated when USART_STS.FEF, USART_STS. OREF or USART_STS. NEF bit is set. 0: Error interrupt is disabled. 1: Error interrupt enabled.

23.7.8 USART Guard time and Prescaler Register (USART_GTP)

Address offset : 0x18

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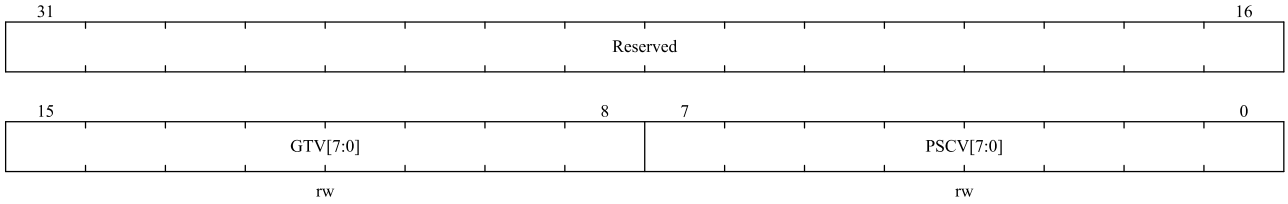
Reset value : 0x0000 0000



Bit field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained
15:8	GTV[7:0]	Guard time value in Smartcard mode. This bit field specifies the guard time in baud clock. In Smartcard mode, this function is required. The setting time of USART_STS.TXC flag is delayed by GTV[7:0] baud clock cycles. *Note: This bit is invalid for UART4/5/6/7.*
7:0	PSCV[7:0]	Prescaler value. In IrDA low power consumption mode: these bits are used to set the frequency division coefficient for dividing the peripheral clock (PCLK1/PCLK2) to generate low power consumption frequency. 00000000: reserved-do not write this value. 00000001: divide the source clock by 1. … 11111111: divide the source clock by 255. In IrDA normal mode: PSCV can only be set to 00000001. In Smartcard mode: PSCV[7:5] is reserved, PSCV[4:0] is used to set the frequency division factor of the peripheral clock (APB1/APB2) to generate the smart card clock. The actual frequency division factor is twice the set value of PSCV[4:0]. 0000: reserved - do not write this value. 0001: Divide the source clock by 2. 0010: Divide the source clock by 4. … 1111: Divide the source clock by 62. *Note: This bit is invalid for UART4/5/6/7.*

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24 Quad Serial Peripheral Interface (QSPI)

24.1 Introduction

QSPI is an interface for single,dual or quad SPI peripheral communication. It can work in indirect or memory mapped modes.

Indirect Mode: All operations are performed using QSPI registers.

Memory Mapped Mode: The external flash memory is mapped into the microcontroller address space, and the system treats it as internal storage space.

24.2 QSPI Main Features

The main features of the QSPI controller are as follows:

- Support Single SPI/Dual SPI/Quad SPI mode. In Single mode, it supports standard SPI operation and can work in half-duplex and full-duplex modes;
- Support indirect mode and memory mapped mode;
- 8-bit, 16-bit, 32-bit data access mode support;
- Support Individual RX FIFO and TX FIFO that are depth is 32 and width is 32bit;
- Support DMA operation;
- Support FIFO interrupt, operation completion interrupt, data access error interrupt;
- Maximum speed 4 × 36Mbps;
- In indirect mode or memory-mapped mode, operations are divided into Instruction phase, Address phase, Mode bits phase, wait cycles phase, and Data phase. These phase can be configured to be skipped, but at least one phase remains.

Note: The Mode bits phase is only used in XIP mode.

Note: In XIP mode, only read operations are supported to external memory, and write operations are not supported.

Note: Only big endian mode is supported when reading external memory data in XIP mode.

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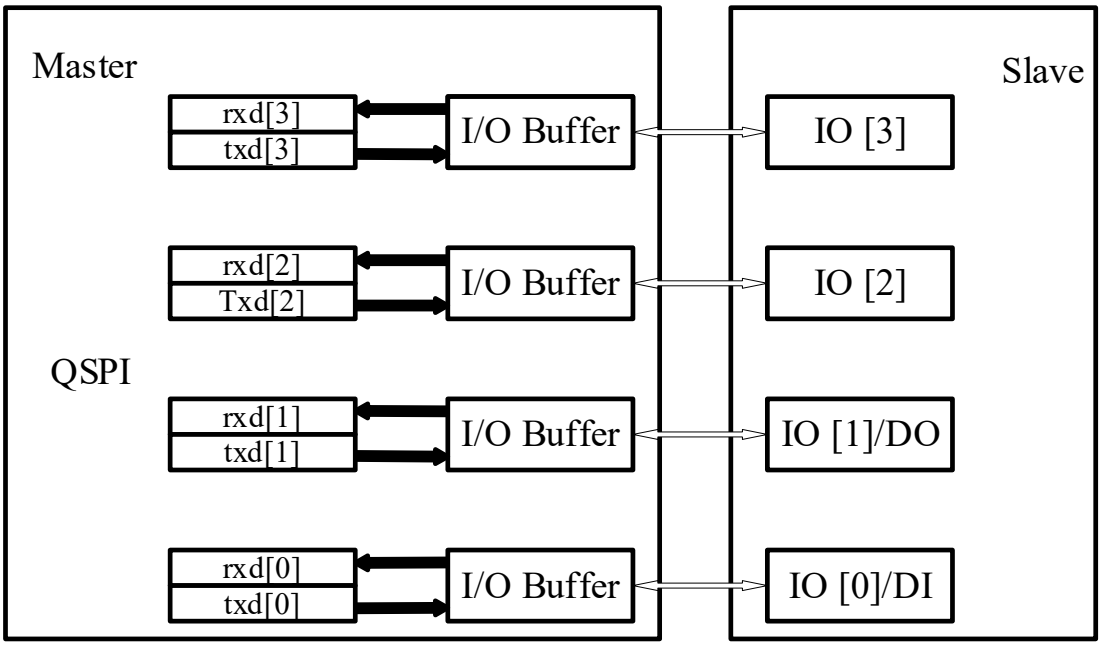
24.3 Function Description

Figure 24-1 QSPI block diagram



24.4 QSPI Command Sequence

QSPI communicates with peripherals through commands. Each command includes five phase: Instruction phase, Address phase, Mode bits phase, Wait cycles phase and Data phase. Any phase can be skipped, but at least remains one of Instruction phase, Address phase, Mode bits phase or the Data phase.

Note: The Mode bits phase is only used in XIP mode.

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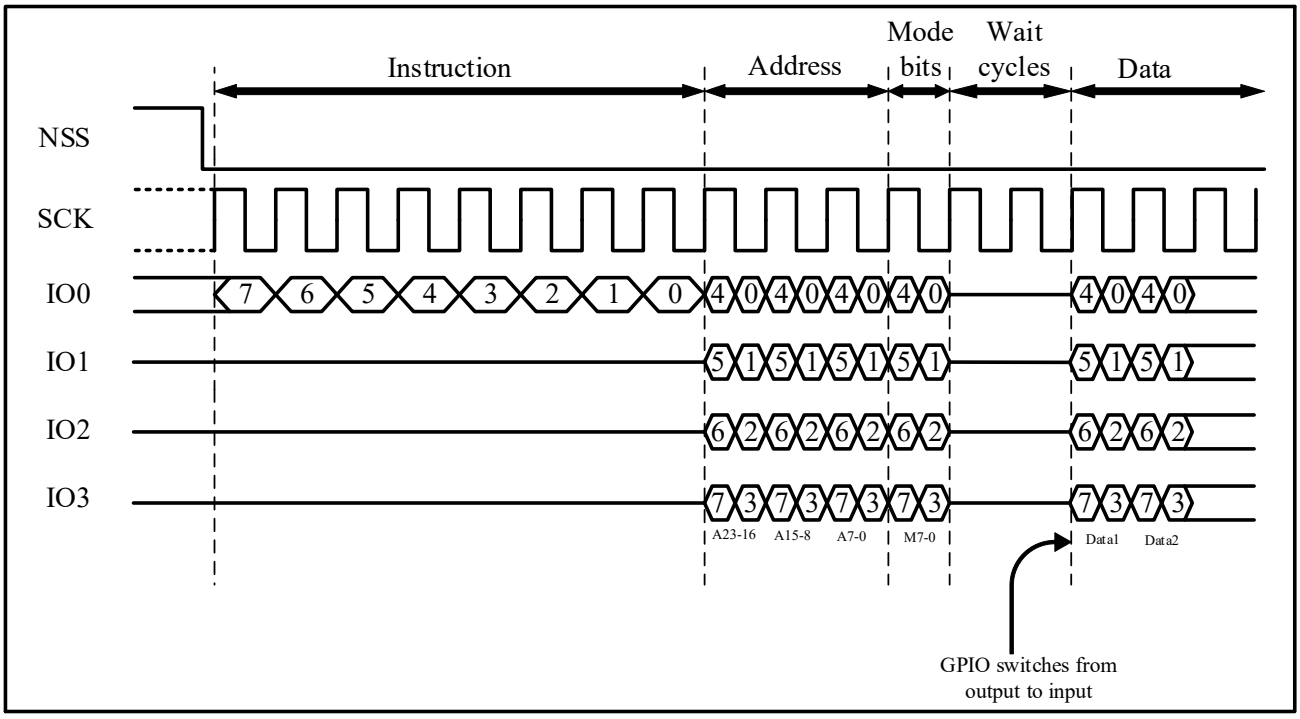
Figure 24-2 QSPI command sequence



24.5 Operating Procedures

24.5.1 QSPI Indirect Mode

In indirect mode, instruction are initiated by writing to the QSPI registers, and data is transferred by reading and writing to the data registers, in the same manner as other communication peripherals.

When QSPI_CTRL0.TMOD[1:0] = 00, it is working in Tx and Rx mode, both transmit and receive data is valid. Transmission of data continues until the transmit FIFO is empty. The data received from the external device is stored in the receive FIFO memory and can be accessed by the host processor.

Note: Tx and Rx modes are only available in Single SPI mode (QSPI_CTRL0.SPI_FRF[1:0] = 00)

When QSPI_CTRL0.TMOD[1:0] = 01, the QSPI is in indirect transmission mode, and the byte to be transmitted is sent to the flash memory during the data transmission phase, and the data is provided by writing the QSPI_DATx register.

When QSPI_CTRL0.TMOD[1:0] = 10, the QSPI is in indirect receive mode, the data to be received is received from the flash memory in the data receive phase, and the data is obtained by reading the QSPI_DATx register.

When QSPI_CTRL0.TMOD[1:0] = 11, EEPROM read mode, transmit data is used to send opcode or address to EEPROM device.

Note: EEPROM read mode is only available in Single SPI mode (QSPI_CTRL0.SPI_FRF[1:0] = 00)

The number of bytes to read is specified in QSPI_CTRL1.NDF[15:0].

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24.5.2 QSPI Indirect Send Operation

1 QSPI_CTRL0.SPI_FRF[1:0] specifies the frame transmission format (standard/dual-wire/quad-wire mode)

2 QSPI_CTRL0.DFS[4:0] specifies the data length (4～32bit)

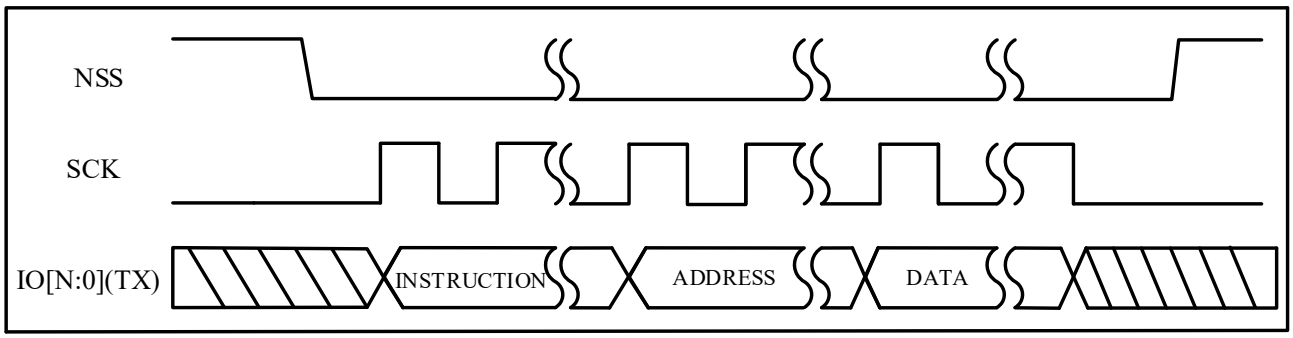
3 QSPI_ENH_CTRL0.ADDR_LEN[3:0] specifies the address length (4bit～60bit, configurable to skip the Address phase)

4 QSPI_ENH_CTRL0.INST_L[1:0] specifies the instruction length (4bit, 8bit, 16bit, configurable to skip the Instruction stage)

Note: One instruction occupies one FIFO address, and the address can occupy multiple FIFO locations. Both instructions and addresses must be programmed in the QSPI_DATx registers.

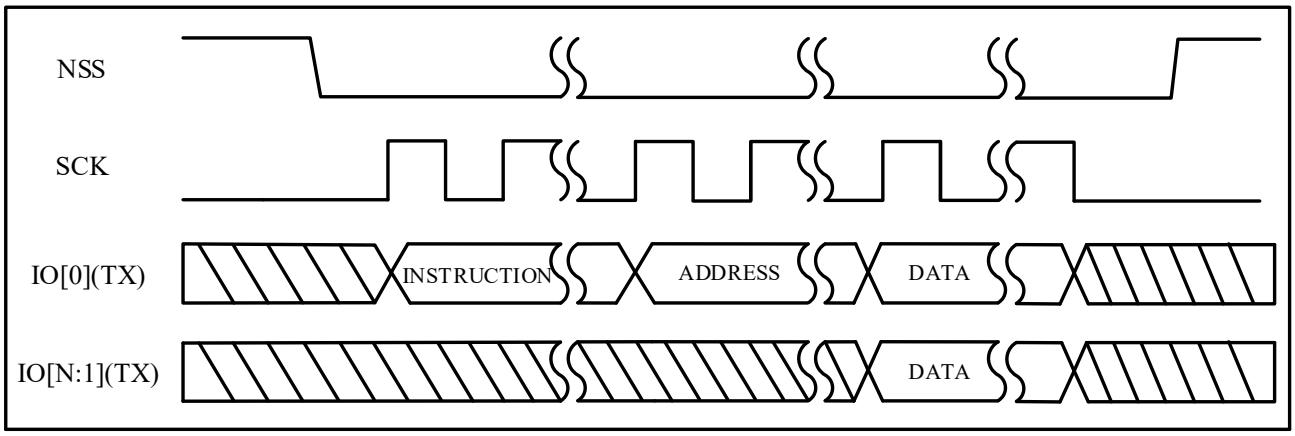
The write operation can be divided into three phase: the Instruction phase, the Address phase, and the Data phase.

- Typical Write Timing



In Quad mode N=3, for 1 write operation, the instruction and address are sent only once, then the data frame stored in QSPI_DATx registers, until the send FIFO is empty.

- When both instruction and address are sent in standard SPI format



QSPI_ENH_CTRL0.TRANS_TYPE[1:0] shall be configured as 0. When QSPI_CTRL0.SPI_FRF[1:0] is configured as 0x02 (Quad mode), N=3; when QSPI_CTRL0.SPI_FRF[1:0] is configured as 0x01 (Dual mode), N=1.

- The instruction is sent in standard SPI mode, and the address is sent in the CTRL0.SPI_FRF mode.

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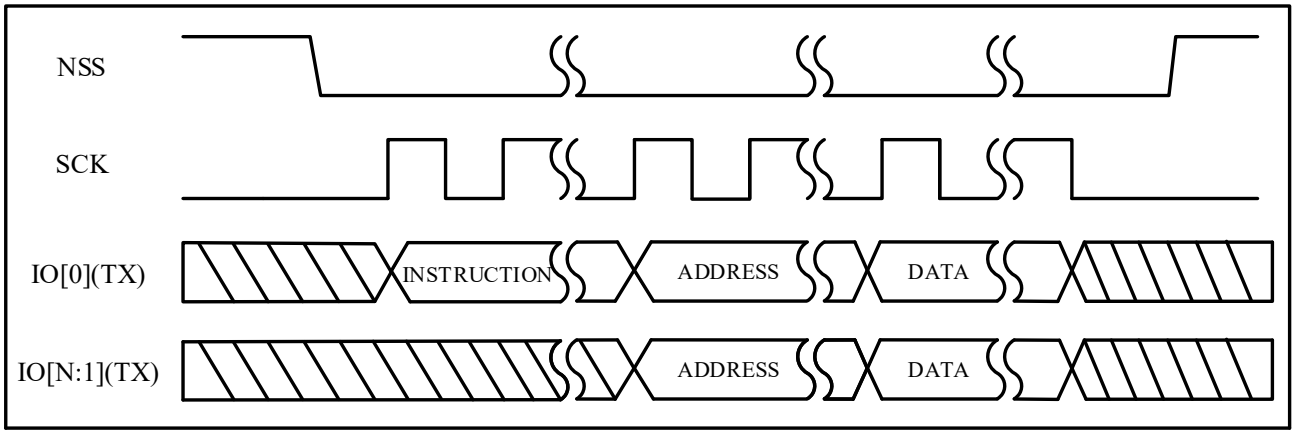
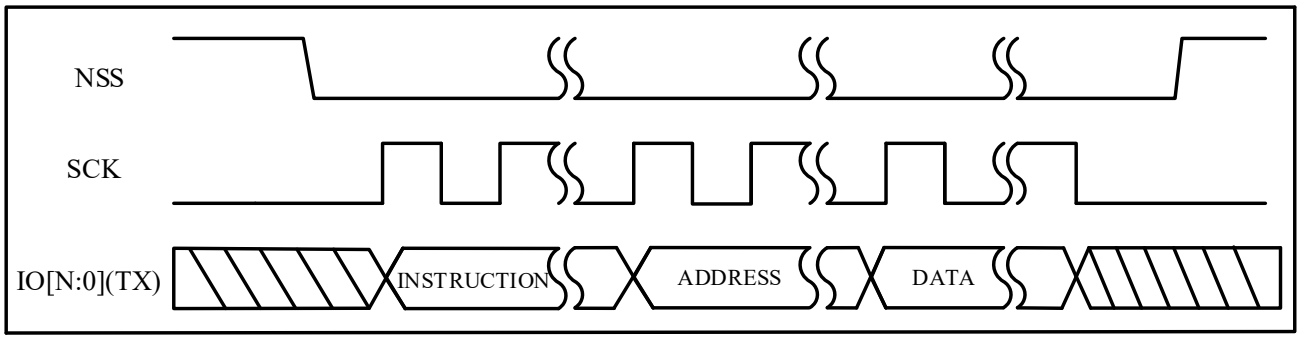


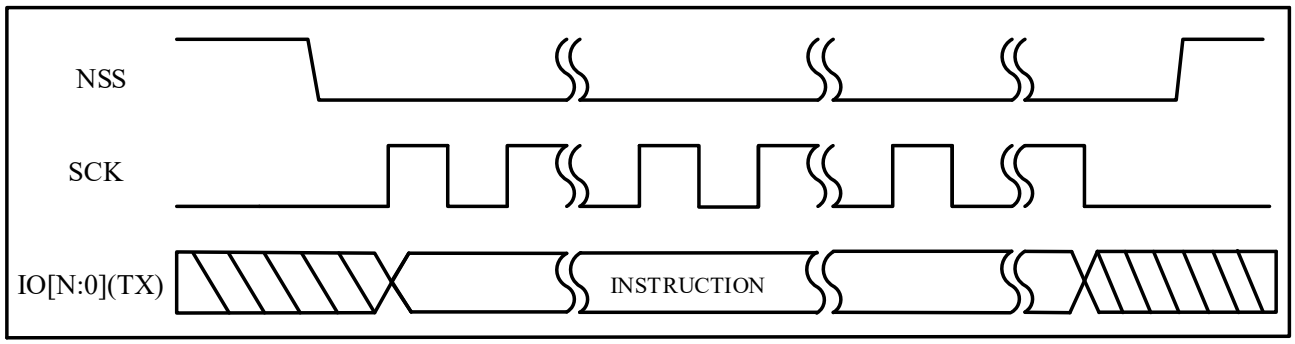
QSPI_ENH_CTRL0.TRANS_TYPE[1:0] shall be configured as 0x01. When QSPI_CTRL0.SPI_FRF[1:0] is configured as 0x02 (Quad mode), N=3; when QSPI_CTRL0.SPI_FRF[1:0] is configured as 0x01 (Dual mode), N=1.

- Instruction and address are sent timing in CTRL0.SPI_FRF specified mode



QSPI_ENH_CTRL0.TRANS_TYPE[1:0] shall be configured as 0x02. When QSPI_CTRL0.SPI_FRF[1:0] is configured as 0x02 (Quad mode), N=3; when QSPI_CTRL0.SPI_FRF[1:0] is configured as 0x01 (Dual mode), N=1.

- Only the send timing of the Instruction phase



Regardless of the QSPI_ENH_CTRL0.TRANS_TYPE[1:0] configuration. When QSPI_CTRL0.SPI_FRF[1:0] is configured as 0x02 (Quad mode), N=3; when QSPI_CTRL0.SPI_FRF[1:0] is configured as 0x01 (Dual mode), N=1.

24.5.3 QSPI Indirect Receive Operation

For a read operation, QSPI sends the command and control data once until it receives data equal to the number of

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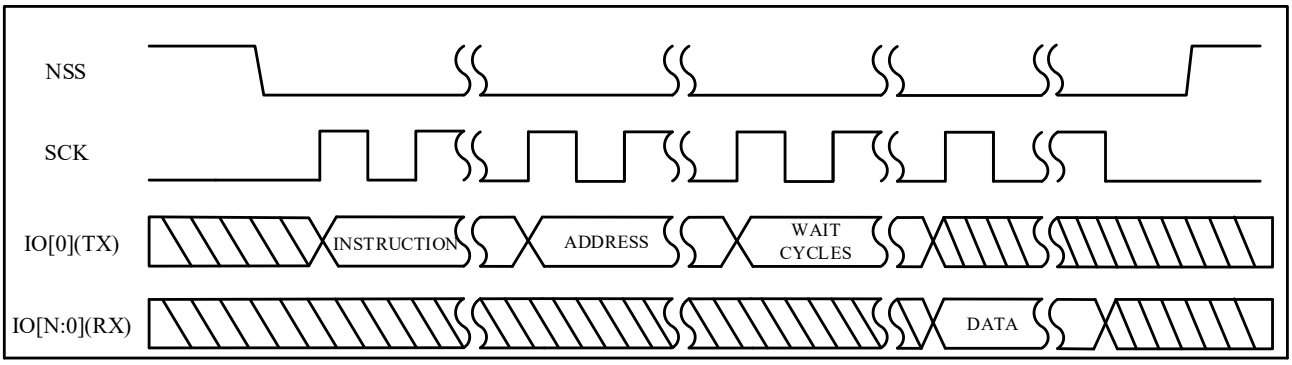
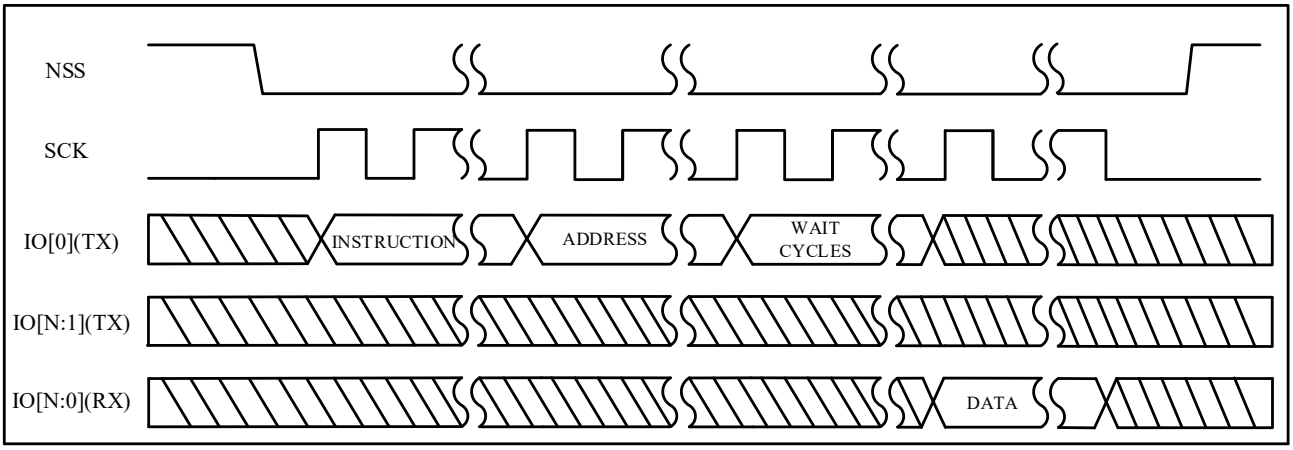
NDF (QSPI_CTRL1[15:0]), and then cancels the slave select signal. The read operation can be divided into 4 phase: Instruction phase, Address phase, Wait cycles phase and Data phase.

- Typical Read Operation Timing



In quad mode N=3, each read command data will be transmitted in the format configured by QSPI_CTRL0.SPI_FRF[1:0]. Configured as 0x2 for quad mode.

- Both address and instruction receive timing in standard SPI format



QSPI_ENH_CTRL0.TRANS_TYPE[1:0] should be configured as 0x0, QSPI_ENH_CTRL0.WAIT_CYCLES[4:0] configure the cycle of WAIT. When QSPI_CTRL0.SPI_FRF[1:0] is configured as 0x02 (Quad mode), N=3; when QSPI_CTRL0.SPI_FRF[1:0] is configured as 0x01 (Dual mode), N=1.

- The instruction is sent in standard SPI mode, and the address is received in the mode specified by QSPI_CTRL0.SPI_FRF.

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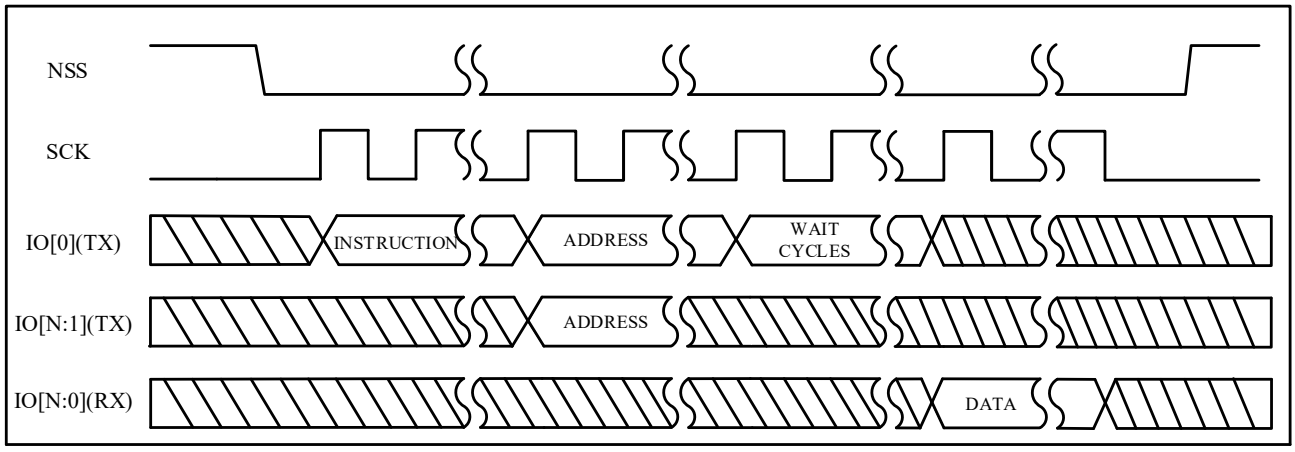
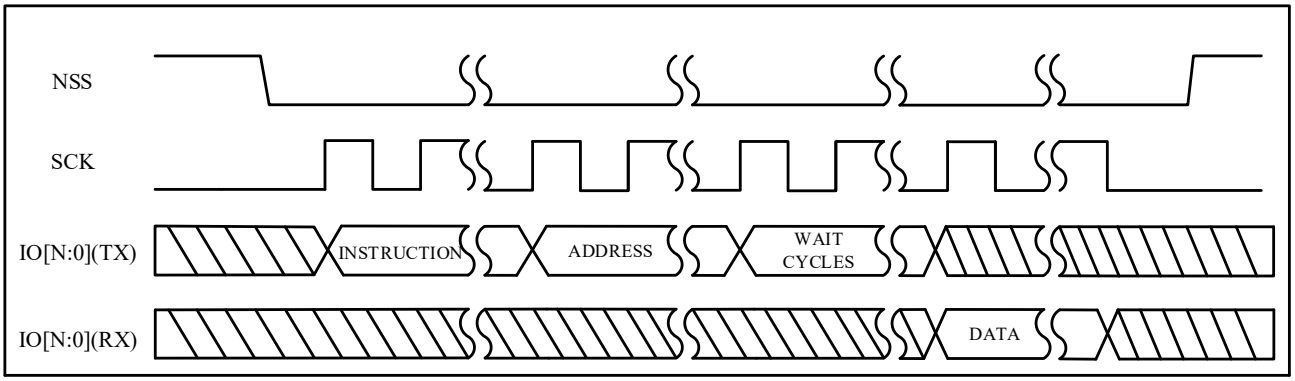


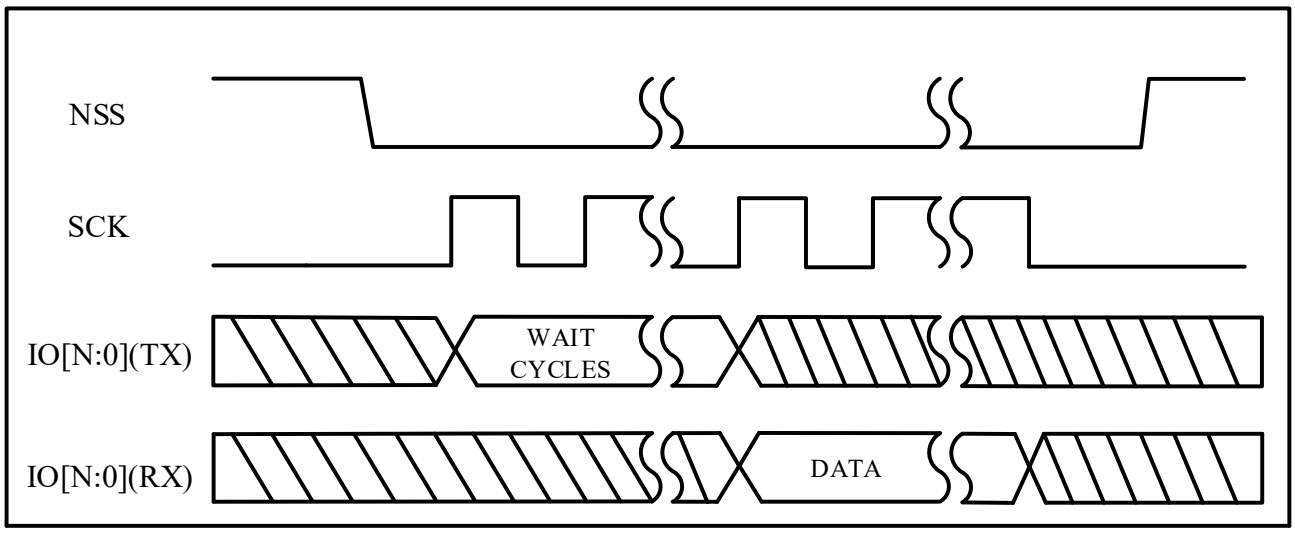
QSPI_ENH_CTRL0.TRANS_TYPE[1:0] should be configured as 0x1, QSPI_ENH_CTRL0.WAIT_CYCLES[4:0] configure the cycle of WAIT. When QSPI_CTRL0.SPI_FRF[1:0] is configured as 0x02 (Quad mode), N=3; when QSPI_CTRL0.SPI_FRF[1:0] is configured as 0x01 (Dual mode), N=1.

- Instruction and address are received timing in QSPI_CTRL0.SPI_FRF specified mode



The QSPI_ENH_CTRL0.TRANS_TYPE[1:0] configuration should be 0x2. When QSPI_CTRL0.SPI_FRF[1:0] is configured as 0x02 (Quad mode), N=3; when QSPI_CTRL0.SPI_FRF[1:0] is configured as 0x01 (Dual mode), N=1.

- Only the receive timing of the Wait cycles phase



QSPI_ENH_CTRL0.ADDR_LEN[3:0] is configured to 0, QSPI_ENH_CTRL0.INST_L[1:0] is configured to 0, and

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QSPI_ENH_CTRL0.WAIT_CYCLES[4:0] is configured to wait cycles. When QSPI_CTRL0.SPI_FRF[1:0] is configured as 0x02 (Quad mode), N=3; when QSPI_CTRL0.SPI_FRF[1:0] is configured as 0x01 (Dual mode), N=1.

24.6 QSPI Register

24.6.1 QSPI Register Overview

Table 24-1 QSPI register overview

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
000h	QSPI_CTRL0	Reserved								SPI_FRF[1:0]		Reserved		CFS[3:0]				Reserved	SSTE	SRL	Reserved	TMOD[1:0]		SCPOL	SCPH	FRF[1:0]		Reserved	DFS[4:0]				
	Reset Value									1	0			0	0	0	0		1	0		0	1	0	0	0	0		0	0	1	1	1
004h	QSPI_CTRL1	Reserved																NDF[15:0]															
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
008h	QSPI_EN	Reserved																															QEN
	Reset Value																																0
00Ch	QSPI_MW_CTRL	Reserved																													MHS_EN	MC_DIR	MWMOD
	Reset Value																														0	0	0
010h	QSPI_SLAVE_EN	Reserved																															SEN
	Reset Value																																0
014h	QSPI_BAUD	Reserved																CLK_DIV[15:0]															
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
018h	QSPI_TXFT	Reserved												TXFT_ST[4:0]				Reserved													TXFT_TEI[4:0]		
	Reset Value													0	0	0	0														0	0	0
01Ch	QSPI_RXFT	Reserved																															RXFT_TFI[4:0]
	Reset Value																																0
020h	QSPI_TXFN	Reserved																															TXFN[5:0]
	Reset Value																																0
024h	QSPI_RXFN	Reserved																															RXFN[5:0]
	Reset Value																																0

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Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
028h	QSPI_STS	Reserved																									DC_ERR	Reserved		RXFF	RXFNE	TXFE	TXFNF	BUSY
	Reset Value																										0		0	0	1	1	0
02Ch	QSPI_IMASK	Reserved																									XRXOIM	MMCIM	RXFFIM	RXFOIM	RXFUIM	TXFOIM	TXFEIM
	Reset Value																										1	1	1	1	1	1	1
030h	QSPI_ISTS	Reserved																									XRXOIS	MMCIS	RXFFIS	RXFOIS	RXFUIS	TXFOIS	TXFEIS
	Reset Value																										0	0	0	0	0	0	0
034h	QSPI_RISTS	Reserved																									XRXORI	MMCRIS	RXFFRIS	RXFORIS	RXFURIS	TXFORIS	TXFERIS
	Reset Value																										0	0	0	0	0	0	0
038h	QSPI_TXFOI_CLR	Reserved																															TXFOIC
	Reset Value																																0
03Ch	QSPI_RXFOI_CLR	Reserved																															RXFOIC
	Reset Value																																0
040h	QSPI_RXFUI_CLR	Reserved																															RXFUIC
	Reset Value																																0
044h	QSPI_MMC_CLR	Reserved																															MMCIC
	Reset Value																																0
048h	QSPI_ICLR	Reserved																															INTC
	Reset Value																																0
04Ch	QSPI_DMA_CTRL	Reserved																														TX_DMA_E	RX_DMA_E
	Reset Value																															0	0
050h	QSPI_DMATDL_CTRL	Reserved																									DMATDL[5:0]						
	Reset Value																										0	0	0	0	0	0	
054h	QSPI_DMARDL_CTRL	Reserved																									DMARDL[5:0]						
	Reset Value																										0	0	0	0	0	0	
060h+004h*x(x=0~31)	QSPI_DATx	DATx[31:0]																															
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0F0h	QSPI_RS_DELAY	Reserved															SES	Reserved									SDCN[7:0]						
	Reset Value																0										0	0	0	0	0	0	0
0F4h	QSPI_ENH_CTRL0	Reserved	CLK_STRETCH_EN	Reserved												INST_DDR_EN	SPI_DDR_EN	WAIT_CYCLES[4:0]					Reserved	INST_L[1:0]		Reserved	ADDR_LEN[3:0]				TRANS_TYPE[1:0]		

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Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reset Value		0													0	0	0	0	0	0	0		1	0			0	0	0	0	0	0
0F8h	QSPI_DDR_TXDE	Reserved																								TXDE[7:0]							
	Reset Value																									0	0	0	0	0	0	0	0
0FCh	QSPI_XIP_MODE	Reserved																XIP_MD_BITS[15:0]															
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
100h	QSPI_XIP_INCR_TOC	Reserved																ITOC[15:0]															
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
104h	QSPI_XIP_WRAP_TOC	Reserved																WTOC[15:0]															
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
108h	QSPI_XIP_CTRL	Reserved		XIP_MBL[1:0]		Reserved		XIP_CT_EN	XIP_INST_EN	Reserved	INST_DDR_EN	DDR_EN	DFS_HC	WAIT_CYCLES[4:0]					MD_BITS_EN	Reserved	INST_L[1:0]		Reserved	ADDR_LEN[3:0]				TRANS_TYPE[1:0]		FRF[1:0]		
	Reset Value			1	0			1	1		0	0	0	0	0	0	0	0	0		1	0		0	0	0	0	0	0	1	0	
10Ch	QSPI_XIP_SLAVE_EN	Reserved																															SEN
	Reset Value																																0
110h	QSPI_XIP_RXFOI_CLR	Reserved																															XRXFOIC
	Reset Value																																0
114h	QSPI_XIP_TOUT	Reserved																								XTOUT[7:0]							
	Reset Value																									0	0	0	0	0	0	0	0

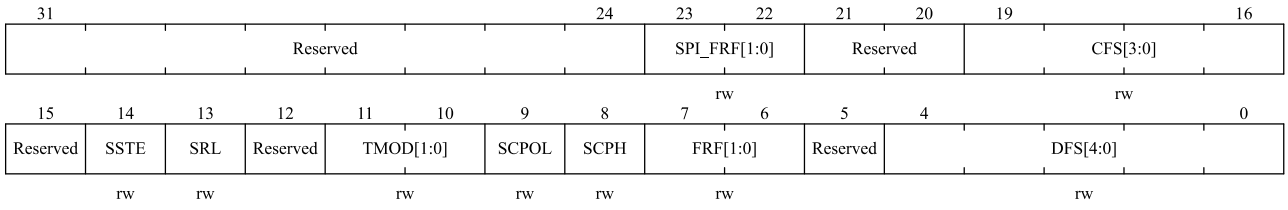
24.6.2 QSPI Control 0 Register (QSPI_CTRL0)

QSPI_CTRL0 register controls the serial data transfer.

Note: This register cannot be written when the QSPI_EN.QEN = 1.

Address offset: 0x00

Reset value: 0x0080 4407



Bit field	Name	Description
31:24	Reserved	Reserved, the reset value must be maintained
23:22	SPI_FRF[1:0]	SPI Frame Format 00: Standard SPI Format

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Bit field	Name	Description
		01: Dual SPI Format 10: Quad SPI Format 11: Reserved
21:20	Reserved	Reserved, the reset value must be maintained
19:16	CFS[3:0]	Control Frame Size Selects the length of the control word for the Microwire frame format. 0000: 1bit Control Word 0001: 2bit Control Word 0010: 3bit Control Word 0011: 4bit Control Word …… 1110: 15bit Control Word 1111: 16bit Control Word
15	Reserved	Reserved, the reset value must be maintained
14	SSTE	Slave Select Toggle Enable While operating in SPI mode with clock phase (SCPH) set to 0, this bit controls the behavior of the NSS between data frames. 0: NSS will stay low and serial clock will run continuously for the duration of the transfer. 1: NSS will toggle between consecutive data frames, with the serial clock being held to its default value while NSS is high.
13	SRL	Shift Register Loop Used for testing purposes only. When active, connects the transmit shift register output to the receive shift register input. 0: Disable 1: Enable
12	Reserved	Reserved, the reset value must be maintained
11:10	TMOD[1:0]	Transfer Mode 00: Tx and Rx 01: Tx only 10: Rx only 11: EERPOM read
9	SCPOL	Serial Clock Polarity 0: low 1: high
8	SCPH	Serial Clock Phase 0: Capture data on the first edge of the serial clock; 1: Toggles one cycle after activation of the select line and captures data on the second edge of the serial clock.
7:6	FRF[1:0]	Frame Format 00: Motorola SPI 01: TI SSP 10: National Semiconductors Microwire

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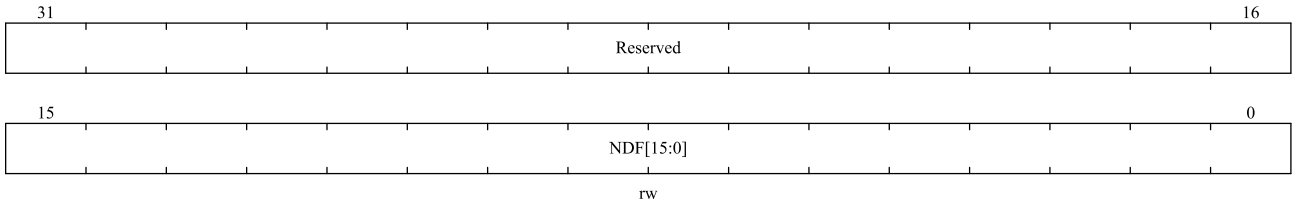
Bit field	Name	Description
		11: Reserved
5	Reserved	Reserved, the reset value must be maintained
4:0	DFS[4:0]	Data Frame Size Selects the data frame length. When the data frame size is programmed to be less than 32 bits, the data is automatically right-aligned. 0x0/0x01/0x02: Reserved 0x03: 4bit 0x04: 5bit 0x05: 6bit …… 0x1D: 30bit 0x1E: 31bit 0x1F: 32bit

24.6.3 QSPI Control 1 Register (QSPI_CTRL1)

Address offset: 0x04

Reset value: 0x0000 0000

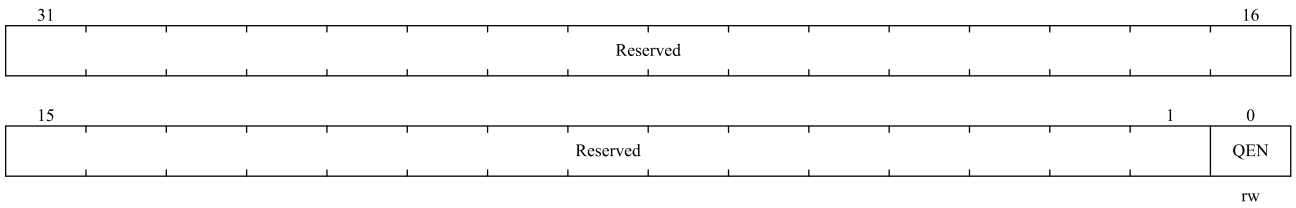


Bit field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained
15:0	NDF[15:0]	Number of Data Frames. When QSPI_CTRL0.TMOD[1:0] = 10 or 11, this register configures the number of consecutively received data frames

24.6.4 QSPI Enable Register (QSPI_EN)

Address offset: 0x08

Reset value: 0x0000 0000



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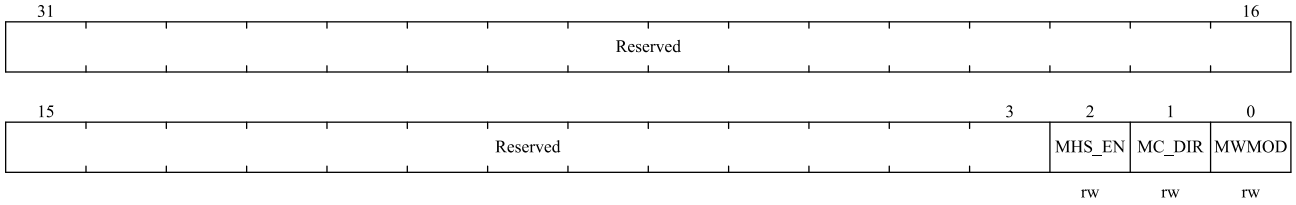
Bit field	Name	Description
31:1	Reserved	Reserved, the reset value must be maintained
0	QEN	QSPI Enable 0: Disabled. when QSPI is disabled, all serial transfers stop immediately. 1: Enable QSPI.

24.6.5 QSPI Microwire Control Register (QSPI_MW_CTRL)

Note: This register cannot be written when the QSPI_EN.QEN = 1.

Address offset: 0x0C

Reset value: 0x0000 0000



Bit field	Name	Description
31:3	Reserved	Reserved, the reset value must be maintained
2	MHS_EN	Microwire Handshaking Enable 0: Handshaking diable 1: Handshaking enable. When enabled, the QSPI checks for a ready status from the target slave, after the transfer of the last data or control bit, before clearing the QSPI_STS.BUSY status.
1	MC_DIR	Direction of Data when Microwire Control 0: Rx 1: Tx
0	MWMOD	Microwire Transfer Mode 0: Non-Sequential Transfer. A control word must be specified for each transmitted or received block of data; 1: Sequential Transfer. Only one control word is required to send or receive data bytes.

24.6.6 QSPI Slave Enable Register (QSPI_SLAVE_EN)

Note: Enable the QSPI_EN register, the QSPI_SLAVE_EN register will be enabled for external slave device selection to enable chip select.

Address offset: 0x10

Reset value: 0x0000 0000

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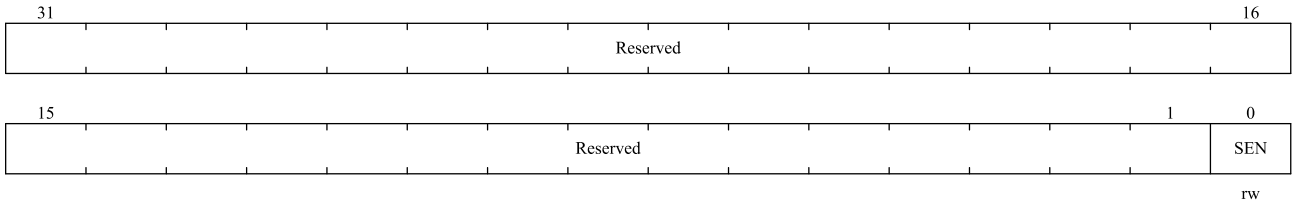
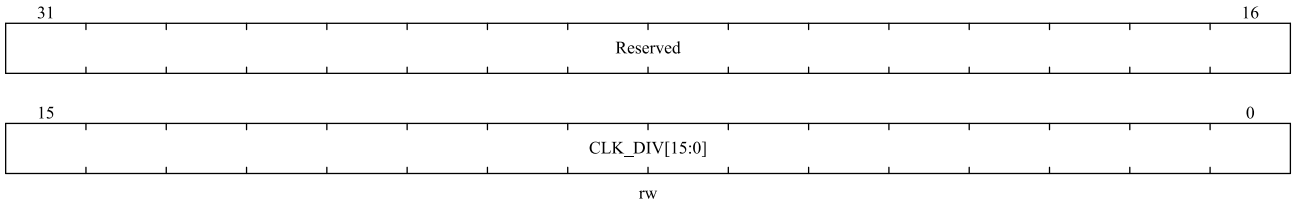


Bit field	Name	Description
31:1	Reserved	Reserved, the reset value must be maintained
0	SEN	Slave Enable 0: Disable 1: Enable *Note: You cannot write to this register when QSPI is busy and when QSPI_EN.QEN = 1.*

24.6.7 QSPI Baud Rate Select Register (QSPI_BAUD)

Address offset: 0x14

Reset value: 0x0000 0000

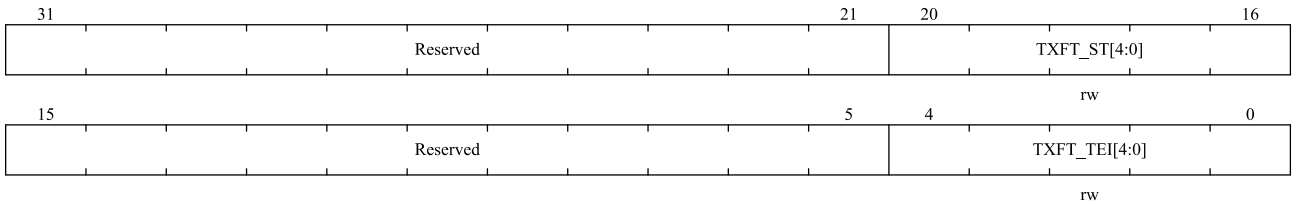


Bit field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained
15:0	CLK_DIV[15:0]	Clock Divider Bit 0 of this register is always configured as 0 and is not affected by write operations, which ensures that even values are preserved in this register. The serial output clock is disabled if CLK_DIV[15:0]=0x0000. Serial output clock frequency = AHB/CLK_DIV[15:0], the value range of CLK_DIV[15:0] is an even number between 2 and 65534.

24.6.8 QSPI Transmit FIFO Threshold Level Register (QSPI_TXFT)

Address offset: 0x18

Reset value: 0x0000 0000



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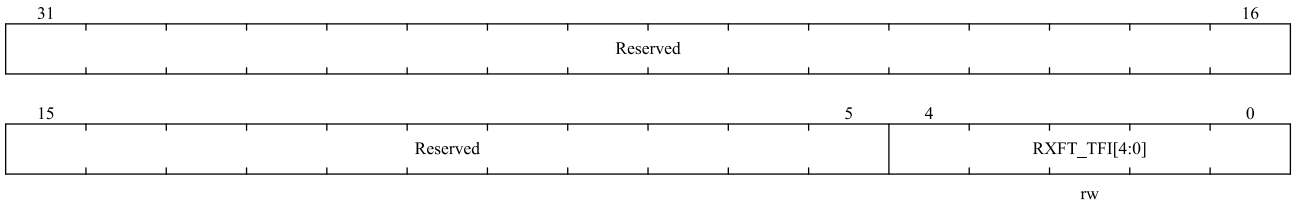
Bit field	Name	Description
31:21	Reserved	Reserved, the reset value must be maintained
20:16	TXFT_ST[4:0]	Transmit FIFO Threshold to Start to Transfer. Tx transmission threshold, after reaching this value, start Tx transmission.
15:5	Reserved	Reserved, the reset value must be maintained
4:0	TXFT_TEI[4:0]	Transmit FIFO Threshold to Trigger Empty Interrupt. Tx transmission threshold, when the number of transmit FIFOs is less than this value, an empty interrupt is triggered.

24.6.9 QSPI Receive FIFO Threshold Level Register (QSPI_RXFT)

Address offset: 0x1C

Reset value: 0x0000 0000

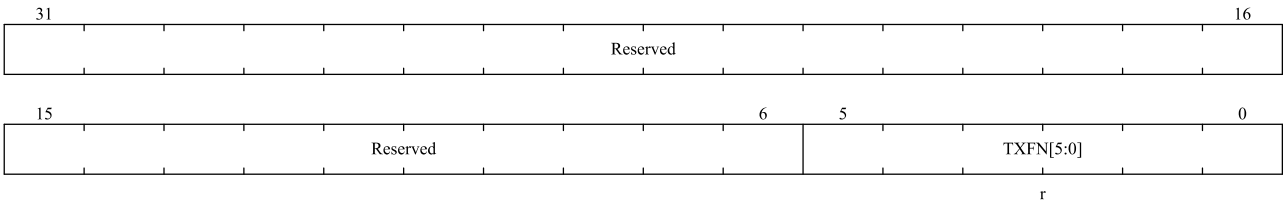


Bit field	Name	Description
31:5	Reserved	Reserved, the reset value must be maintained
4:0	RXFT_TFI[4:0]	Receive FIFO Threshold to Trigger Full Interrupt. Rx transmission threshold, when the number of receive FIFO is greater than this value plus 1, a full interrupt is triggered.

24.6.10 QSPI Transmit FIFO Level Register (QSPI_TXFN)

Address offset: 0x20

Reset value: 0x0000 0000



Bit field	Name	Description
31:6	Reserved	Reserved, the reset value must be maintained
5:0	TXFN[5:0]	Number of Transmit FIFO.

24.6.11 QSPI Receive FIFO Level Register (QSPI_RXFN)

Address offset: 0x24

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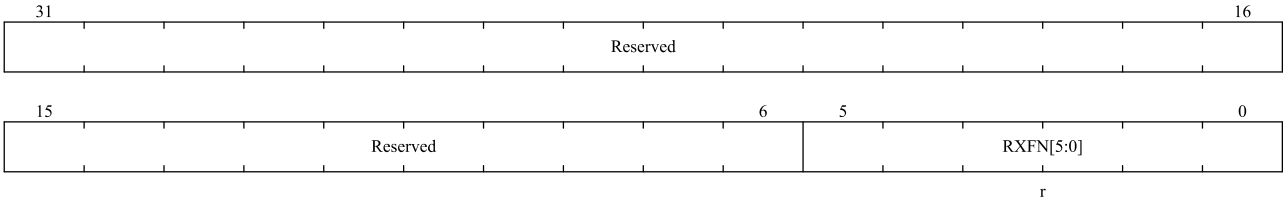
Reset value: 0x0000 0000

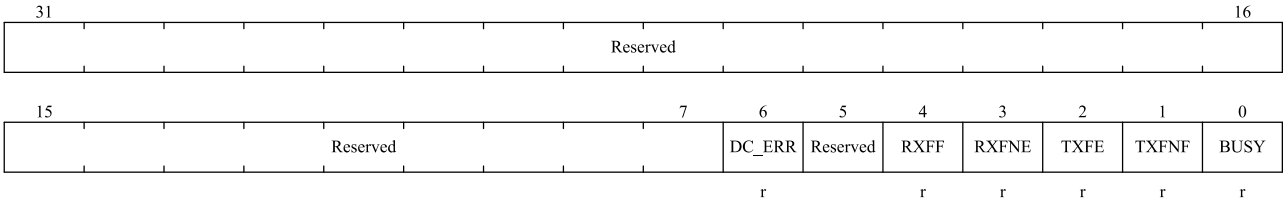


Bit field	Name	Description
31:6	Reserved	Reserved, the reset value must be maintained
5:0	RXFN[5:0]	Number of Receive FIFO.

24.6.12 QSPI Status Register (QSPI_STS)

Address offset: 0x28

Reset value: 0x0000 0006



Bit field	Name	Description
31:7	Reserved	Reserved, the reset value must be maintained
6	DC_ERR	Data Conflict Error 0: No Error 1: Transmit Data Collision Error
5	Reserved	Reserved, the reset value must be maintained
4	RXFF	Receive FIFO Full. 0: Receive FIFO is not full 1: Receive FIFO is full When the receive FIFO is completely full, this bit is set.When the receive FIFO contains one or more empty location, this bit is cleared.
3	RXFNE	Receive FIFO Not Empty. 0: Receive FIFO is empty 1: Receive FIFO is not empty Set when the receive FIFO contains one or more entries and is cleared when the receive FIFO is empty.
2	TXFE	Transmit FIFO Empty. 0: Transmit FIFO is not empty 1: Transmit FIFO is empty When the transmit FIFO is completely empty, this bit is set. When the transmit FIFO contains one or more valid entries, this bit is cleared.

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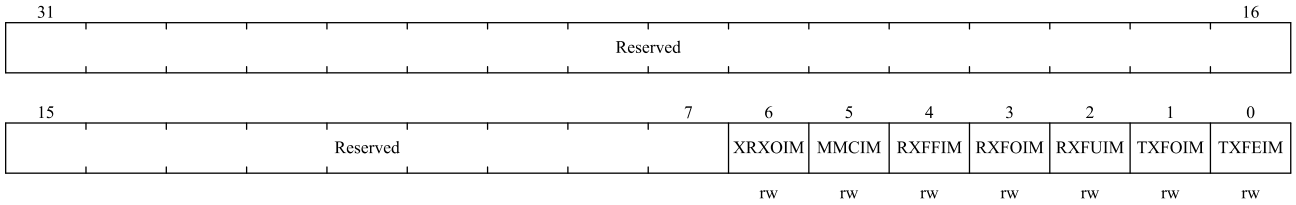
Bit field	Name	Description
1	TXFNF	Transmit FIFO Not Full. 0: Tx FIFO is full 1: Tx FIFO is not Full Set when the transmit FIFO contains one or more empty locations, and is cleared when the FIFO is full.
0	BUSY	Transfer Busy Flag. 0: QSPI is idle or disabled 1: QSPI is actively transferring data

24.6.13 QSPI Interrupt Mask Register (QSPI_IMASK)

Address offset: 0x2C

Reset value: 0x0000 007F



Bit field	Name	Description
31:7	Reserved	Reserved, the reset value must be maintained
6	XRXOIM	XIP Receive FIFO Overflow Interrupt Mask. 0: Mask 1: Not mask
5	MMCIM	Multi-Master Contention Interrupt Mask. 0: Mask 1: Not mask
4	RXFFIM	Receive FIFO Full Interrupt Mask. 0: Mask 1: Not mask
3	RXFOIM	Receive FIFO Overflow Interrupt Mask. 0: Mask 1: Not mask
2	RXFUIM	Receive FIFO Underflow Interrupt Mask. 0: Mask 1: Not mask
1	TXFOIM	Transmit FIFO Overflow Interrupt Mask. 0: Mask 1: Not mask
0	TXFEIM	Transmit FIFO Empty Interrupt Mask. 0: Mask 1: Not mask

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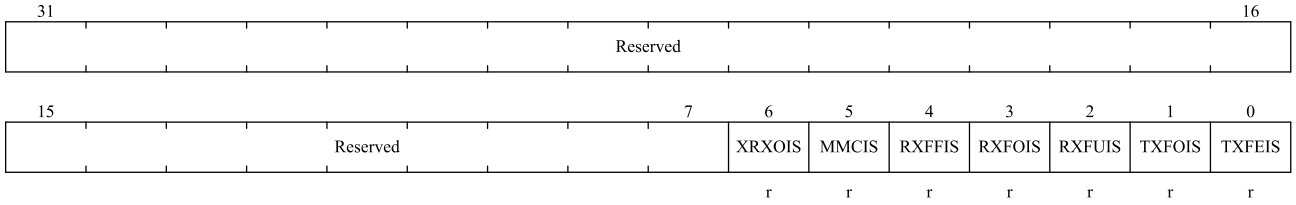
24.6.14 QSPI Interrupt Status Register (QSPI_ISTS)

Address offset: 0x30

Reset value: 0x0000 0000



Bit field	Name	Description
31:7	Reserved	Reserved, the reset value must be maintained
6	XRXOIS	XIP Receive FIFO Overflow Interrupt Status. 0: Invalid, after masking. 1: Validafter, after masking.
5	MMCIS	Multi-Master Contention Interrupt Status. 0: Invalid, after masking. 1: Valid, after masking.
4	RXFFIS	Receive FIFO Full Interrupt Status. 0: Invalid, after masking. 1: Valid, after masking.
3	RXFOIS	Receive FIFO Overflow Interrupt Status. 0: Invalid, after masking. 1: Valid, after masking.
2	RXFUIS	Receive FIFO Underflow Interrupt Status. 0: Invalid, after masking. 1: Valid, after masking.
1	TXFOIS	Transmit FIFO Overflow Interrupt Status. 0: Invalid, after masking. 1: Valid, after masking.
0	TXFEIS	Transmit FIFO Empty Interrupt Status. 0: Invalid, after masking. 1: Valid, after masking.

24.6.15 QSPI Raw Interrupt Status Register (QSPI_RISTS)

Address offset: 0x34

Reset value: 0x0000 0000

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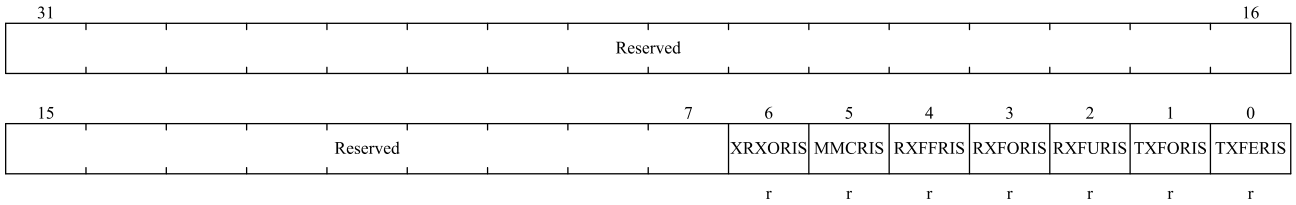
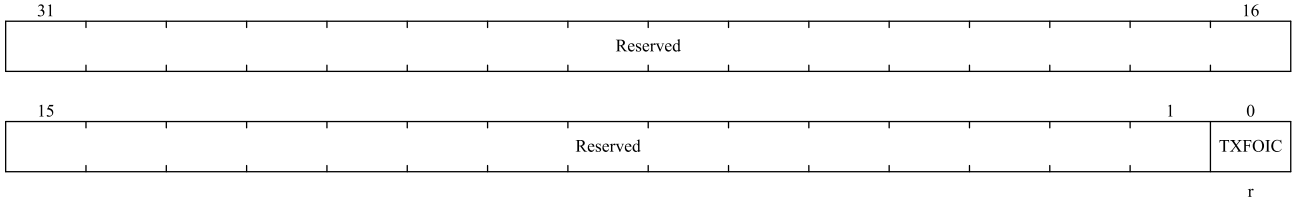


Bit field	Name	Description
31:7	Reserved	Reserved, the reset value must be maintained
6	XRXORIS	XIP Receive FIFO Overflow Raw Interrupt Status. 0: Invalid, prior to masking. 1: Valid, prior to masking.
5	MMCRIS	Multi-Master Contention Raw Interrupt Status. 0: Invalid, prior to masking. 1: Valid, prior to masking.
4	RXFFRIS	Receive FIFO Full Raw Interrupt Status. 0: Invalid, prior to masking. 1: Valid, prior to masking.
3	RXFORIS	Receive FIFO Overflow Raw Interrupt Status. 0: Invalid, prior to masking. 1: Valid, prior to masking.
2	RXFURIS	Receive FIFO Underflow Raw Interrupt Status. 0: Invalid, prior to masking. 1: Valid, prior to masking.
1	TXFORIS	Transmit FIFO Overflow Raw Interrupt Status. 0: Invalid, prior to masking. 1: Valid, prior to masking.
0	TXFERIS	Transmit FIFO Empty Raw Interrupt Status. 0: Invalid, prior to masking. 1: Valid, prior to masking.

24.6.16 QSPI Transmit FIFO Overflow Interrupt Clear Register (QSPI_TXFOI_CLR)

Address offset: 0x38

Reset value: 0x0000 0000



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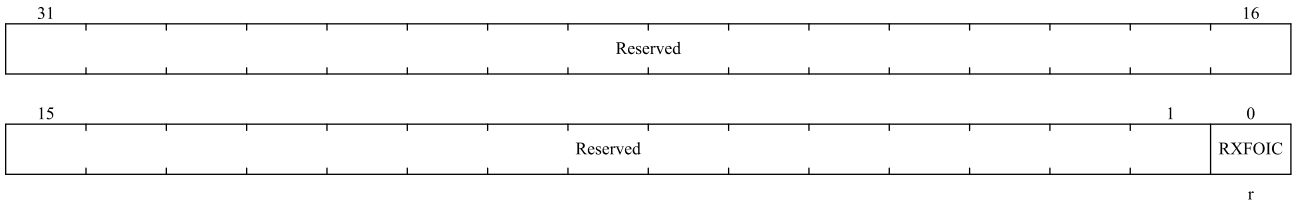
Bit field	Name	Description
31:1	Reserved	Reserved, the reset value must be maintained
0	TXFOIC	Clear Transmit FIFO Overflow Interrupt. After reading this register, clear the Tx FIFO overflow interrupt status.

24.6.17 QSPI Receive FIFO Overflow Interrupt Clear Register (QSPI_RXFOI_CLR)

Address offset: 0x3C

Reset value: 0x0000 0000

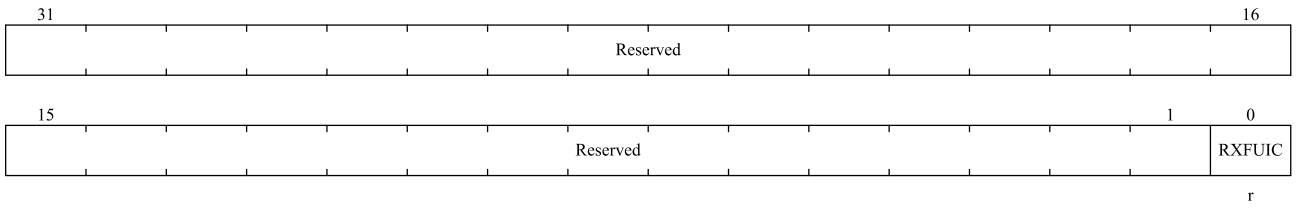


Bit field	Name	Description
31:1	Reserved	Reserved, the reset value must be maintained
0	RXFOIC	Clear Receive FIFO Overflow Interrupt. After reading this register, clear the Rx FIFO overflow interrupt status.

24.6.18 QSPI Receive FIFO Underflow Interrupt Clear Register (QSPI_RXFUI_CLR)

Address offset: 0x40

Reset value: 0x0000 0000



Bit field	Name	Description
31:1	Reserved	Reserved, the reset value must be maintained
0	RXFUIC	Clear Receive FIFO Underflow Interrupt. After reading this register, clear the Rx Fifo underflow interrupt status.

24.6.19 QSPI Multi-Master Interrupt Clear Register (QSPI_MMCI_CLR)

Address offset: 0x44

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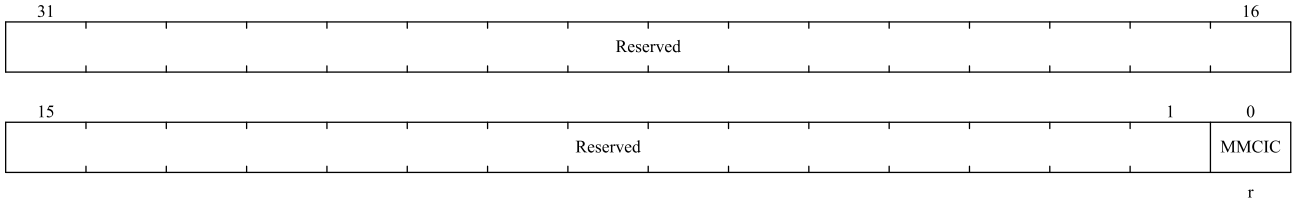
Reset value: 0x0000 0000

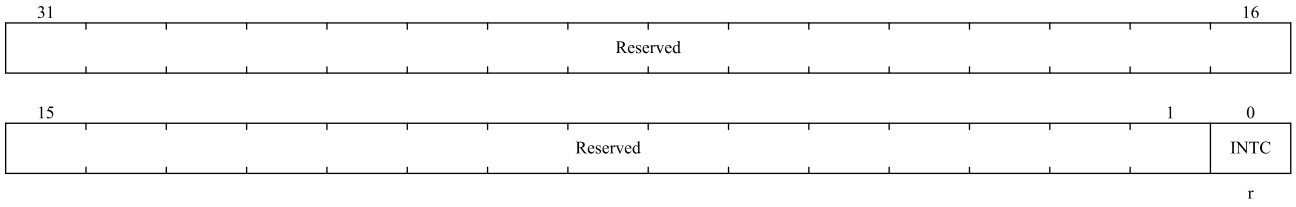


Bit field	Name	Description
31:1	Reserved	Reserved, the reset value must be maintained
0	MMCIC	Clear Multi-Master Contention Interrupt. After reading this register, clear the multi-master conflict interrupt status.

24.6.20 QSPI Interrupt Clear Register (QSPI_ICLR)

Address offset: 0x48

Reset value: 0x0000 0000

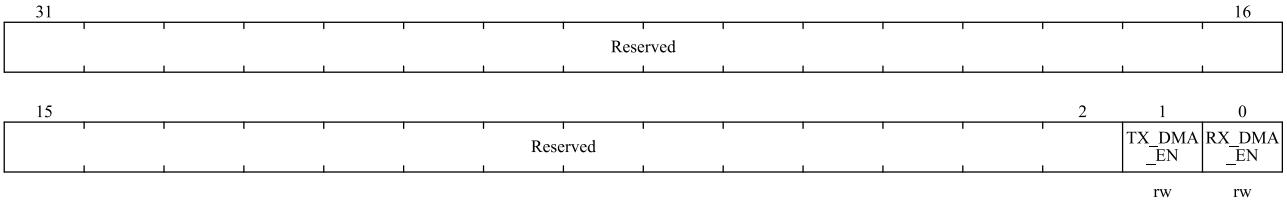


Bit field	Name	Description
31:1	Reserved	Reserved, the reset value must be maintained
0	INTC	Clear Interrupts. After reading this register, clear transmit FIFO overflow interrupt, receive FIFO overflow interrupt, receive FIFO underflow interrupt, and multi-master conflict interrupt status.

24.6.21 QSPI DMA Control Register (QSPI_DMA_CTRL)

Address offset: 0x4C

Reset value: 0x0000 0000



Bit field	Name	Description
31:2	Reserved	Reserved, the reset value must be maintained

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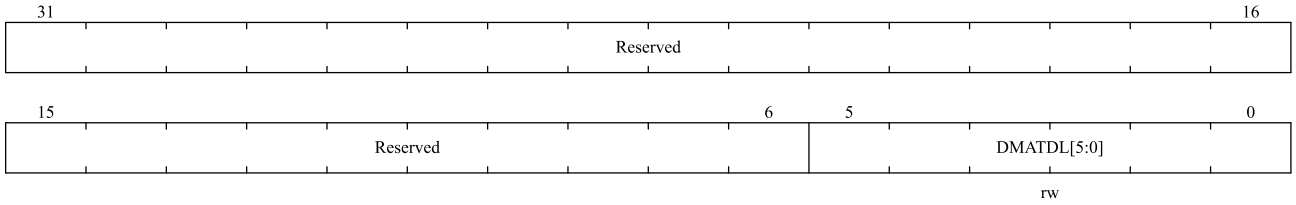
Bit field	Name	Description
1	TX_DMA_EN	Transmit DMA Enable. 0: Disable 1: Enable
0	RX_DMA_EN	Receive DMA Enable. 0: Disable 1: Enable

24.6.22 QSPI DMA Transmit Data Level Register (QSPI_DMATDL_CTRL)

Address offset: 0x50

Reset value: 0x0000 0000

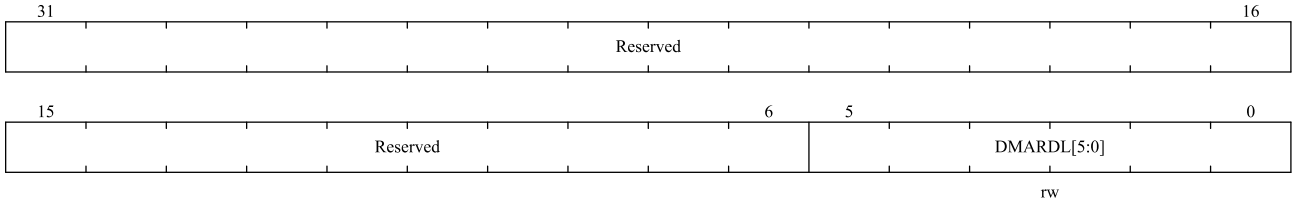


Bit field	Name	Description
31:6	Reserved	Reserved, the reset value must be maintained
5:0	DMATDL[5:0]	DMA Transmit Data Level.

24.6.23 QSPI DMA Receive Data Level Register (QSPI_DMARDL_CTRL)

Address offset: 0x54

Reset value: 0x0000 0000



Bit field	Name	Description
31:6	Reserved	Reserved, the reset value must be maintained
5:0	DMARDL[5:0]	DMA Receive Data Level.

24.6.24 QSPI Data Register（QSPI_DATx）

Address offset: 0x60+0x04 × x （x=0~31）

Reset value: 0x0000 0000

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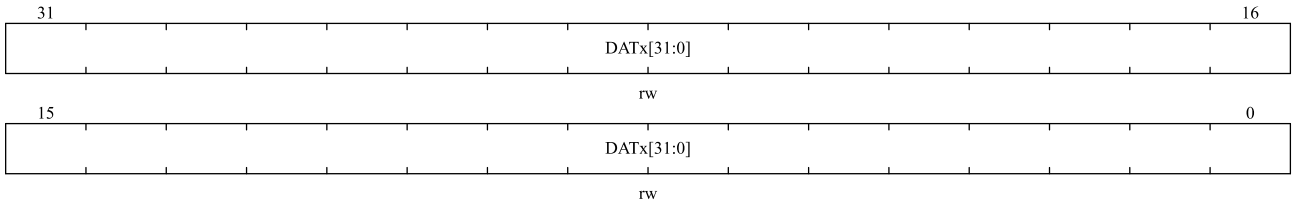
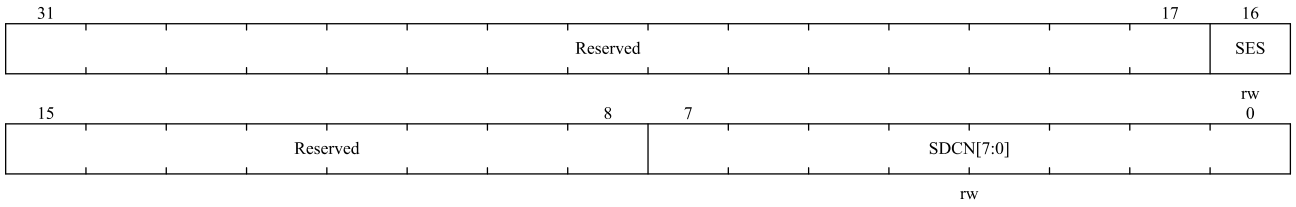


Bit field	Name	Description
31:0	DATx[31:0]	In the Rx state, it is the receive buffer, and the read data is automatically right-aligned; in the Tx state, it is the send buffer, and the write data must be right-aligned. *Note: a total of 32 register addresses are 0x60+(0:31) × 0x04.*

24.6.25 QSPI RX Sample Delay Register (QSPI_RS_DELAY)

Address offset: 0xF0

Reset value: 0x0000 0000



Bit field	Name	Description
31:17	Reserved	Reserved, the reset value must be maintained
16	SES	Sampling Edge Select of Receive Data 0: rising edge sampling 1: falling edge sampling *Note: The sampling edge selection bit configures the QSPI to sample on the rising or falling edge of the core clock AHB*
15:8	Reserved	Reserved, the reset value must be maintained
7:0	SDCN[7:0]	Sample Delay Cycle Number This bit configures the number of AHB cycles to delay sampling. *Note: When 0x6 is exceeded, 0-delay sampling will be used.*

24.6.26 QSPI Enhanced SPI Mode Control 0 Register（QSPI_ENH_CTRL0）

This register is used to control serial data transfer in Enhanced SPI mode of operation. Configuring this register is valid only when QSPI_CTRL0.SPI_FRF ≠ 00. This register cannot be written to after the QSPI_EN register is enabled.

Address offset: 0xF4

Reset value: 0x0000 0200

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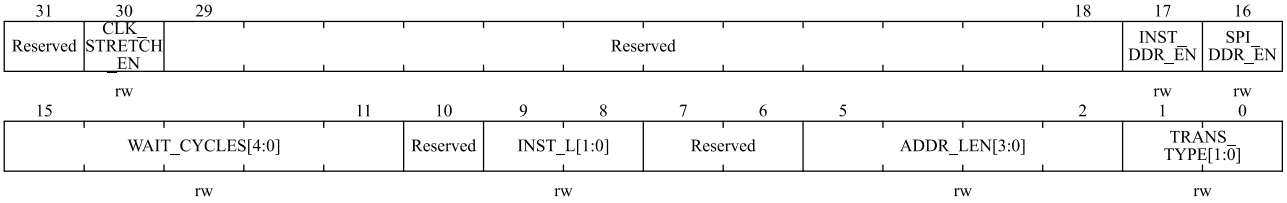

Bit field	Name	Description
31	Reserved	Reserved, the reset value must be maintained
30	CLK_STRETCH_EN	Clock Stretch Enable in SPI transfers. In case of write, if the FIFO becomes empty QSPI will stretch the clock until FIFO has enough data to continue the transfer. In case of read, if the receive FIFO becomes full QSPI will stop the clock until data has been read from the FIFO. 0: Disable 1: Enable
29:18	Reserved	Reserved, the reset value must be maintained
17	INST_DDR_EN	Instruction DDR enable bit. 0: Disable 1: Enable
16	SPI_DDR_EN	SPI DDR Enable bit. This will enable Dual-data rate transfers in Dual/Quad frame formats of SPI 0: Disable 1: Enable
15:11	WAIT_CYCLES[4:0]	Wait Cycles in Dual/Quad mode between control frames transmit and data reception.
10	Reserved	Reserved, the reset value must be maintained
9:8	INST_L[1:0]	Dual/Quad mode instruction length in bits. 00: No Instruction 01: 4bit 10: 8 bit 11: 16 bit
7:6	Reserved	Reserved, the reset value must be maintained
5:2	ADDR_LEN[3:0]	Length of Address to transmit. 0x0: No Address 0x1: 4bit 0x2: 8bit 0x3: 12bit …… 0xE: 56bit 0xF: 60bit
1:0	TRANS_TYPE[1:0]	Address and instruction transfer format. 00: Instruction and Address will be sent in Standard SPI Mode.

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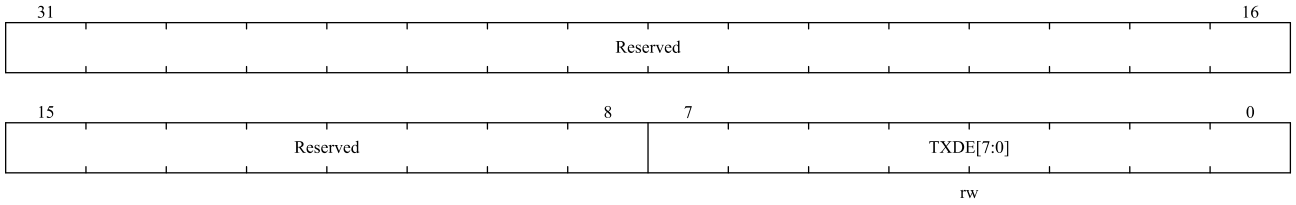
Bit field	Name	Description
		01: Instruction will be sent in Standard SPI Mode and Address will be sent in the mode specified by QSPI_CTRL0.SPI_FRF. 10: Both Instruction and Address will be sent in the mode specified by QSPI_CTRL0.SPI_FRF. 11: Reserved

24.6.27 QSPI DDR Transmit Drive Edge Register (QSPI_DDR_TXDE)

Address offset: 0xF8

Reset value: 0x0000 0000

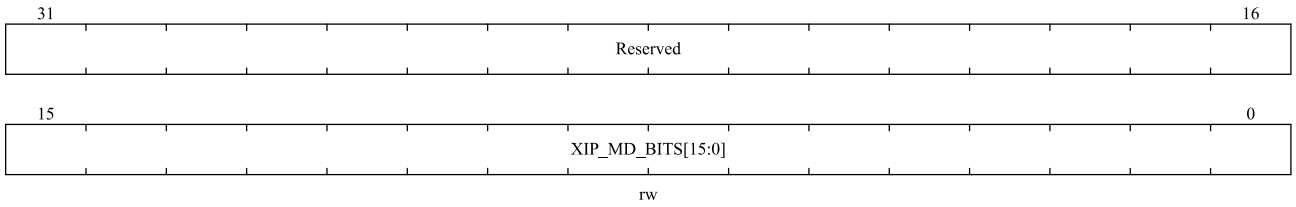


Bit field	Name	Description
31:8	Reserved	Reserved, the reset value must be maintained
7:0	TXDE[7:0]	Transmit Drive Edge. Determines the driving edge of the core clock to transmit data in DDR mode, the maximum value of this register = QSPI_BAUD/2 - 1.

24.6.28 QSPI XIP Mode bits Register (QSPI_XIP_MODE)

Address offset: 0xFC

Reset value: 0x0000 0000



Bit field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained
15:0	XIP_MD_BITS [15:0]	XIP mode bits to be sent after address phase of XIP transfer.

24.6.29 QSPI XIP INCR Transfer Opcode Register (QSPI_XIP_INCR_TOC)

Address offset: 0x100

Reset value: 0x0000 0000

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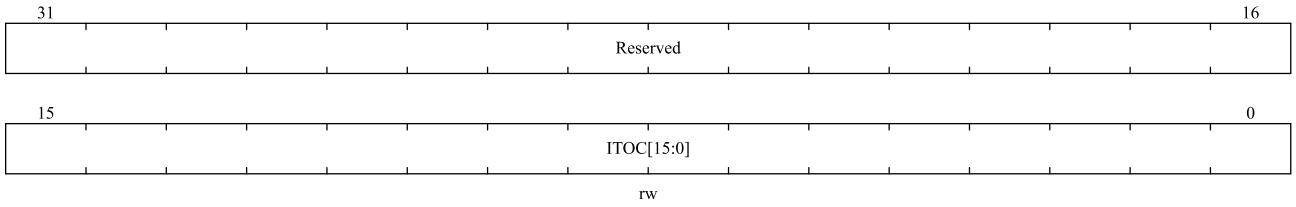
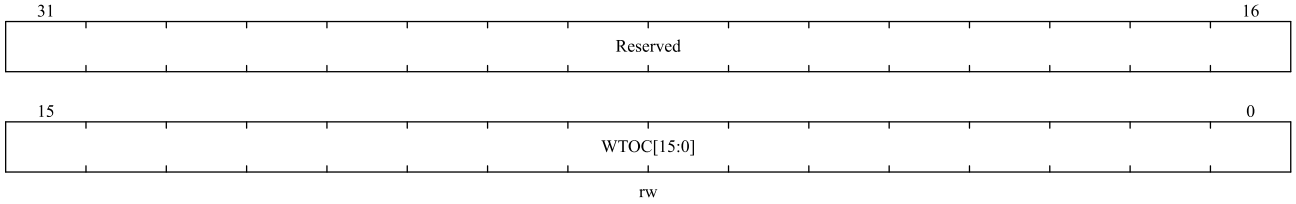


Bit field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained
15:0	ITOC[15:0]	XIP INCR transfer OpCode. When QSPI_XIP_CTRL.XIP_INST_EN=1, QSPI sends XIP INCR type transmission instruction code. The number of bits to be sent during the command phase is determined by the QSPI_XIP_CTRL.INST_L field.

24.6.30 QSPI XIP WRAP Transfer Opcode Register (QSPI_XIP_WRAP_TOC)

Address offset: 0x104

Reset value: 0x0000 0000

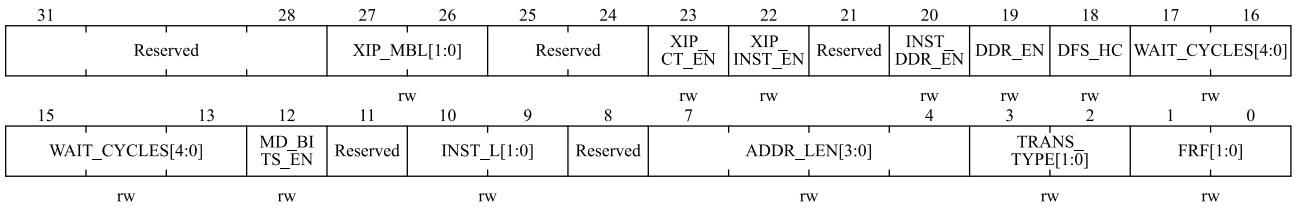


Bit field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained
15:0	WTOC[15:0]	XIP WRAP transfer OpCode. When QSPI_XIP_CTRL.XIP_INST_EN=1, QSPI sends XIP WRAP type transmission instruction code. The number of bits to be sent during the command phase is determined by the QSPI_XIP_CTRL.INST_L field.

24.6.31 QSPI XIP Control Register (QSPI_XIP_CTRL)

Address offset: 0x108

Reset value: 0x28C0 0402



Bit field	Name	Description
31:28	Reserved	Reserved, the reset value must be maintained

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Bit field	Name	Description
27:26	XIP_MBL [1:0]	XIP Mode bits length. 00: Mode bits length equal to 2 01: Mode bits length equal to 4 10: Mode bits length equal to 8 11: Mode bits length equal to 16
25:24	Reserved	Reserved, the reset value must be maintained
23	XIP_CT_EN	Enable continuous transfer in XIP mode.
22	XIP_INST_EN	XIP instruction enable. XIP instruction enabled. When enabled, XIP transfers will also have an instruction phase. The instruction opcode will be selected from the XIP_INCR_TOC or XIP_WRAP_TOC registers depending on the AHB transfer type. 0: Disable 1: Enable
21	Reserved	Reserved, the reset value must be maintained
20	INST_DDR_EN	Instruction DDR enable bit.
19	DDR_EN	SPI DDR Enable bit. This bit configure Dual-data rate transfers in Dual/Quad frame formats of SPI. 0: Disable 1: Enable
18	DFS_HC	Fix DFS for XIP transfers. 0: The size and number of data frames depend on the HSIZE and HBURST signals of the AHB bus 1: The XIP data frame size is fixed to the configuration value of QSPI_CTRL0.DFS
17:13	WAIT_CYCLES[4:0]	Wait Cycles in Dual/Quad mode between control frames transmit and data reception.
12	MD_BITS_EN	Mode bits enable in XIP mode. When enabled, XIP mode will insert Mode bits after the Address phase. These bits are configured in register XIP_MODE. The length of Mode bits is usually 8 bits.
11	Reserved	Reserved, the reset value must be maintained
10:9	INST_L[1:0]	Dual/Quad mode instruction length in bits. 00: No Instruction 01: 4bit 10: 8 bit 11: 16 bit
8	Reserved	Reserved, the reset value must be maintained
7:4	ADDR_LEN[3:0]	Length of Address to transmit. 0x0: No Address 0x1: 4bit 0x2: 8bit

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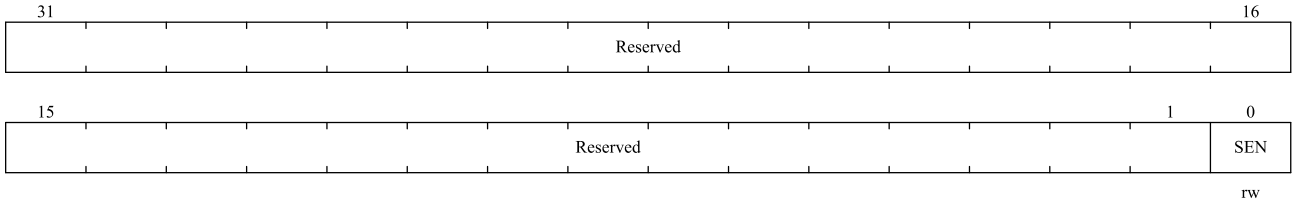
Bit field	Name	Description
		0x3: 12bit …… 0xE: 56bit 0xF: 60bit
3:2	TRANS_TYPE[1:0]	Address and instruction transfer format. 00: Instruction and Address will be sent in Standard SPI Mode. 01: Instruction will be sent in Standard SPI Mode and Address will be sent in the mode specified by QSPI_XIP_CTRL.FRF[1:0] 10: Both Instruction and Address will be sent in the mode specified by QSPI_XIP_CTRL.FRF[1:0]. 11: Reserved
1:0	FRF[1:0]	SPI Frame Format 00: Reserved 01: Dual SPI Format 10: Quad SPI Format 11: Reserved

24.6.32 QSPI XIP Slave Enable Register (QSPI_XIP_SLAVE_EN)

Enable the QSPI_EN register, the QSPI_XIP_SLAVE_EN register will be enabled for external slave device selection to enable chip select.

Address offset: 0x10C

Reset value: 0x0000 0000



Bit field	Name	Description
31:31	Reserved	Reserved, the reset value must be maintained
0	SEN	Slave Select Enable 0: Not Selected 1: Selected

24.6.33 QSPI XIP Receive FIFO Overflow Interrupt Clear Register (QSPI_XIP_RXFOI_CLR)

Address offset: 0x110

Reset value: 0x0000 0000

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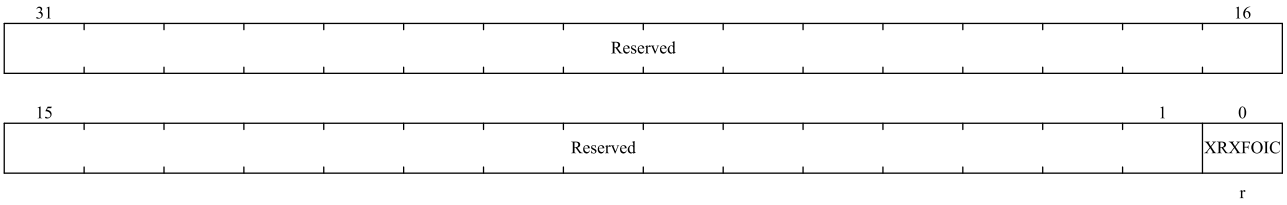
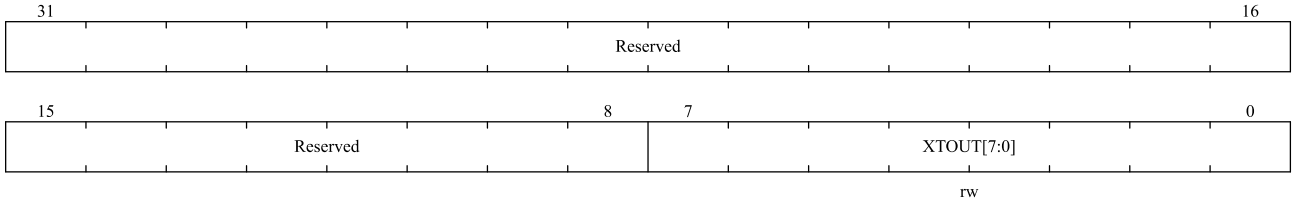


Bit field	Name	Description
31:1	Reserved	Reserved, the reset value must be maintained
0	XRXFOIC	Clear XIP Receive FIFO Overflow Interrupt. After reading this register, clear the Rx FIFO overflow interrupt status

24.6.34 QSPI XIP Timeout for Continuous Transfers Register （QSPI_XIP_TOUT）

Address offset: 0x114

Reset value: 0x0000 0000



Bit field	Name	Description
31:8	Reserved	Reserved, the reset value must be maintained
7:0	XTOUT[7:0]	XIP time out value in terms of AHB. XIP time out value in terms of APB. Once slave is selected in continuous XIP mode this counter will be used to de-select the slave if there is no request for the time specified in the counter

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25 Ethernet (ETH)

MAC: Media Access Control

MII: Media-Independent Interface

RMII: Reduced Media-Independent Interface

SMI: Station Management Interface

CSMA/CD: Carrier Sense Multiple Access/Collision Detection

SFD: Start Frame Delimiter

FCS: Frame Check Sequence

SOF: Start Of Frame

EOF: End Of Frame

Note: Only N32G457xx series chips support Ethernet module.

25.1 Introduction

Ethernet module includes a 10/100Mbps Ethernet MAC, which uses DMA to optimize the transmission and reception performance of data frames, supports MII and RMII two standard interfaces for communication with the physical layer (PHY), and realizes the transmission and reception of Ethernet data frames. Ethernet module complies with the IEEE 802.3-2008 standard and the IEEE 1588-2002 standard.

25.2 Main Features

- Main features of Ethernet MAC:
  - Support MII/RMII interface, MII is defined in IEEE 802.3 specification, RMII conforms to RMII specification of RMII Alliance
  - Support 10/100Mbps data transfer rate
  - Support half-duplex operation:
    - CSMA/CD protocol
    - Back pressure flow control
  - Support full duplex operation:
    - IEEE 802.3x flow control
    - Forward pause control frame to application
    - When the flow control input signal fails, automatically send a zero-wait pause frame
  - Support automatic generation of CRC and PAD padding bits when transmit frames, and automatic stripping of CRC/PAD when receive frames
  - Support programmable frame length (up to 16K bytes)

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- Support programmable frame gap (40~96 bits, but must be an integer multiple of 8)
- Support a variety of flexible address filtering
- Support IEEE 802.1Q VLAN tag detection for receive frames
- Support for mandatory network statistics using RMON/MIB counter (RFC2819/RFC2665)
- Support MDIO interface for configuring and managing external PHY devices
- Support to detect LAN remote wake-up frame and AMD Magic Packet™ frame two kinds of wake-up frame
- In receive function, support offloading the checksum of the received IPv4 and TCP packets encapsulated by Ethernet frames
- Support checking IPv4 header checksums, as well as checksums for TCP, UDP or ICMP (encapsulated by IPv4 or IPv6 data formats)
- Support Ethernet frame timestamps defined by the IEEE 1588-2002 standard, recording 64-bit timestamps in the frame's receive or transmit status
- Support automatic retransmission when transmit conflict, support automatic discarding of frames when late collision, excessive collision, excessive deferral and underrun
- 2 2K byte FIFOs, one is TxFIFO (for sending), the other is RxFIFO (for receiving), the threshold is configurable, the default is 64 bytes
- Support store-forward mechanism to transmit data to MAC core
- In store-forward mode, all error frames received can be filtered, but error frames are not forwarded to the application
- In store-and-forward mode, support for inserting calculated IPv4 header checksums in sent frames, as well as TCP, UDP, or ICMP checksums
- Support MII interface loopback for debugging

- Main features of Ethernet DMA:
  - AHB slave interface support all types of AHB burst transfer, AHB master interface can choose fixed or unfixed length AHB burst transfer type and address aligned burst transfer
  - Optimized packet-oriented DMA transfer with frame delimiter
  - Support addressing of data buffers in a byte-aligned manner
  - Support descriptors in double buffer (ring structure) or linked list form (chain structure)
  - Each descriptor can transmit 8K bytes of data
  - Support to echo the status information of each transmission
  - Can configure the corresponding interrupts in various working status
  - Support polling or fixed priority to arbitrate DMA transmit and receive
- PTP main features:
  - Set timestamp of received frame and transmitted frame

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- Support two calibration methods: rough adjustment and fine adjustment
- Interrupt can be triggered when the system time reaches a predetermined time
- Output second pulse

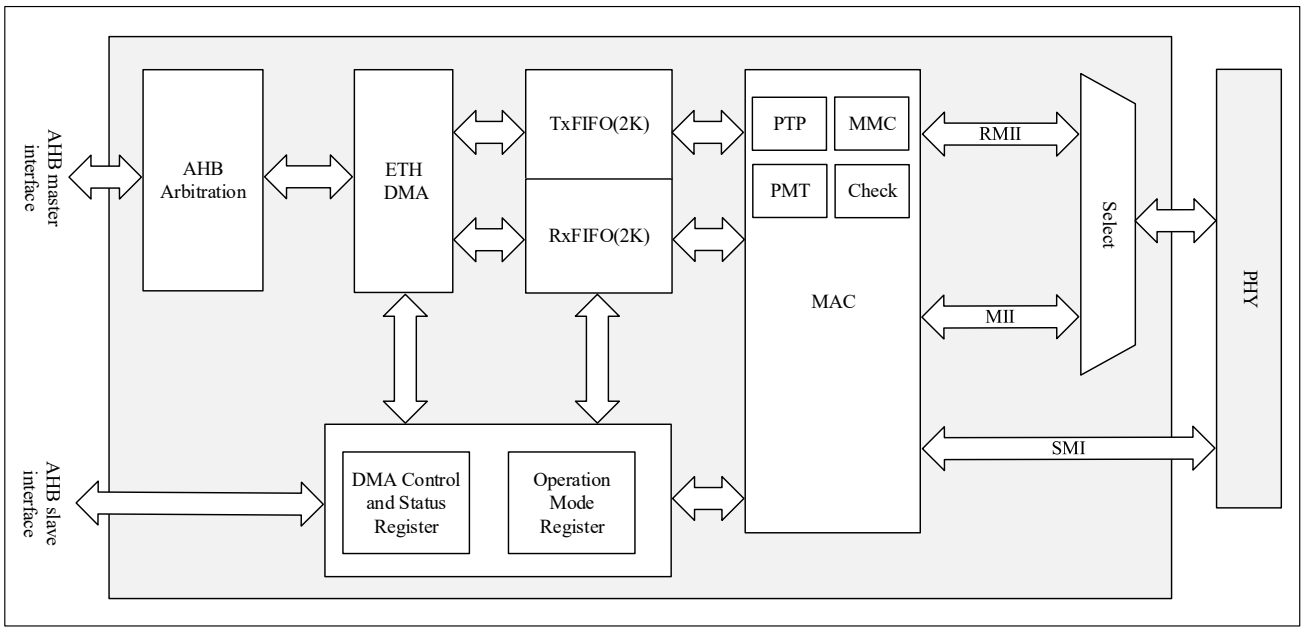
25.3 Function Block Diagram

Ethernet peripheral mainly includes MAC module, MII/RMII interface module and a DMA module controlled in the form of descriptor. MAC module is connected to the off-chip PHY device through MII or RMII. MII or RMII connection method must be selected by software configuration AFIO_RMP_CFG.MII_RMII_SEL before the Ethernet controller enables the clock or in the reset state. The default configuration is MII mode. SMI interface for configuring and managing external PHY devices.

Ethernet DMA controller accesses the MAC controller through the AHB master interface to control data transfer; accesses the MAC memory through the slave interface to access the control and status register areas.

Before the MAC controller sends data, the Ethernet DMA will first read the data from the system memory area and store it in the TxFIFO. The Ethernet frame received by the MAC controller from the bus will be first buffered in the RxFIFO, and then transferred to the system storage area by the Ethernet DMA.

Figure 25-1 Ethernet Module Block Diagram



25.4 Function Description

25.4.1 IEEE 802.3 Ethernet Frame Format

There are two frame formats for the data communication of the MAC compliant with the IEEE 802.3-2008 standard:

- Basic MAC frame format (unlabeled frame)
- Tagged MAC frame format

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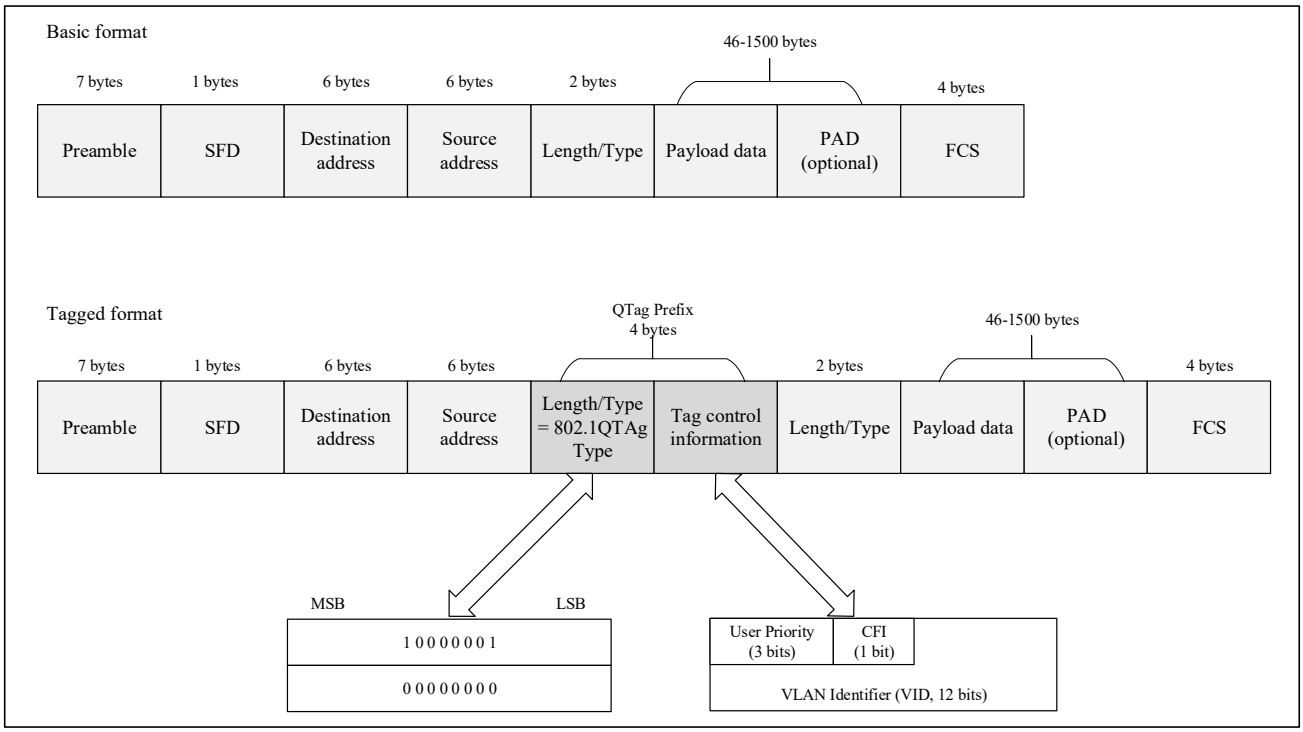
Figure 25-2 MAC frame format and frame structure



Note: Except for FCS, the Ethernet controller transmits each byte in little-endian first-out order.

CRC calculation includes all bytes of frame data except preamble and SFD. The 32-bit CRC generator polynomial of the Ethernet frame is 0x04C11DB7, and this polynomial is used for all 32-bit CRC calculations in the Ethernet module, as shown in the following formula:

$$G(x) = x^{32} + x^{26} + x^{23} + x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^8 + x^7 + x^5 + x^4 + x^2 + x + 1$$

25.4.2 Pin Configuration (alternate) Method

Table 25-1 ETH module pin configuration (alternate)

MII Signal	RMII Signal	Default mapping	Remap 1	Remap 2	Remap 3	Pin configuration
MDC	MDC	PC1				Push-pull alternate output, high speed (50MHz)
TXD2	-	PC2				Push-pull alternate output, high speed (50MHz)
Tx_CLK	-	PC3				Input floating (reset state)
CRS	-	PA0				Input floating (reset state)
Rx_CLK	REF_CLK	PA1				Input floating (reset state)
MDIO	MDIO	PA2				Push-pull alternate output, high speed (50MHz)
COL	-	PA3				Input floating (reset state)
Rx_DV	CRS_DV	PA7	PD8	PA7	PD8	Input floating (reset state)
RxD0	RxD0	PC4	PD9	PC4	PD9	Input floating (reset state)

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MII Signal	RMII Signal	Default mapping	Remap 1	Remap 2	Remap 3	Pin configuration
RxD1	RxD1	PC5	PD10	PC5	PD10	Input floating (reset state)
RxD2	-	PB0	PD11	PB0	PB0	Input floating (reset state)
RxD3	-	PB1	PD12	PB1	PB1	Input floating (reset state)
Rx_ER	-	PB10				Input floating (reset state)
Tx_EN	Tx_EN	PB11				Push-pull alternate output, high speed (50MHz)
TxD0	TxD0	PB12				Push-pull alternate output, high speed (50MHz)
TxD1	TxD1	PB13				Push-pull alternate output, high speed (50MHz)
PPS_OUT	PPS_OUT	PB5		PB6		Push-pull alternate output, high speed (50MHz)
TxD3	-	PB8		PB7		Push-pull alternate output, high speed (50MHz)

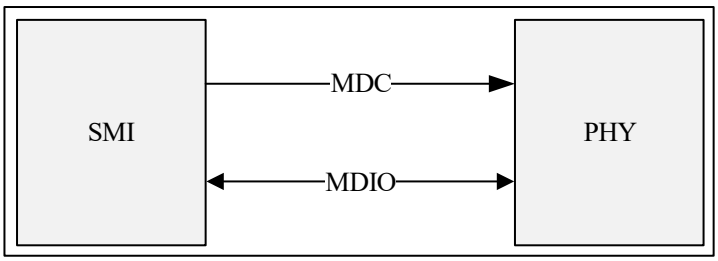
25.4.3 SMI Interface

SMI is used to access and set the configuration of the PHY. It communicates with the external PHY through the clock line MDC and the data line MDIO, and can access any register of any PHY. SMI interface can support up to 32 PHYs, but they cannot be accessed at the same time, and only one register of one PHY can be accessed at the same time.

The functions of the clock line MDC and the data line MDIO are as follows:

- MDC: Clock signal, the highest frequency is 2.5MHz, in idle state, this pin keeps low level state. When transmitting data, the minimum holding time of the high level and low level of the signal is 160ns, and the minimum period of the signal is 400ns;
- MDIO: Receive/transmit data with the PHY, and complete the transmission with the clock line MDC.

Figure 25-3 SMI interface signal line



25.4.3.1 SMI write operation

To implement the SMI write operation, the data to be transmitted needs to be written into the ETH_MACMIIDAT register, and the relevant bits of the ETH_MACMIIADDR register need to be operated:

1. Set device address and specific register address of the PHY to be operated, and set ETH_MACMIIADDR.MW to 1 to enable the write mode;
2. Set ETH_MACMIIADDR.MB to 1 to start transmission. The ETH_MACMIIADDR.MB bit can be used to

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judge whether the transmission is completed. During the transmission process, the ETH_MACMIIADDR.MB bit is always high until the transmission is completed, and the hardware will automatically clear the ETH_MACMIIADDR.MB bit. When the ETH_MACMIIADDR.MB bit is 1, modifying the contents of ETH_MACMIIADDR and ETH_MACMIIDAT will be invalid.

25.4.3.2 SMI read operation

To implement the SMI read operation, it is necessary to operate the relevant bits of the ETH_MACMIIADDR register:

1. Set device address and specific register address of the PHY to be operated, and set ETH_MACMIIADDR.MW to 0 to enable the read mode;
2. Set ETH_MACMIIADDR.MB to 1 to start receiving data. The ETH_MACMIIADDR.MB bit can be used to judge whether the transmission is completed. When receiving data, the ETH_MACMIIADDR.MB bit is always high. After the reception is completed, the hardware will automatically clear the ETH_MACMIIADDR.MB bit. When the ETH_MACMIIADDR.MB bit is 1, modifying the contents of ETH_MACMIIADDR and ETH_MACMIIDAT will be invalid.

Note: The contents of the PHY registers with addresses 16-31 are customized by the manufacturer, so you need to make corresponding settings according to the PHY device manual to access this part of the registers.

25.4.3.3 SMI clock configuration

The clock of SMI interface is derived from AHB clock frequency division. Set the ETH_MACMIIADDR.CR[2:0] bits according to the AHB clock frequency, configure the appropriate frequency division factor, and ensure that the MDC clock frequency does not exceed 2.5MHz.

The SMI clock configuration ranges are as follows:

Table 25-2 SMI clock configuration range

ETH_MACMIIADDR.CR[2:0] value	MDC frequency	HCLK frequency
000	HCLK/42	60~100MHz
001	HCLK/62	100~144MHz
010	HCLK/16	20~35MHz
011	HCLK/26	35~60MHz

25.4.4 MII Interface

MII is used for MAC and external PHY interconnection, and supports 10Mbps and 100Mbps data rate transmission modes.

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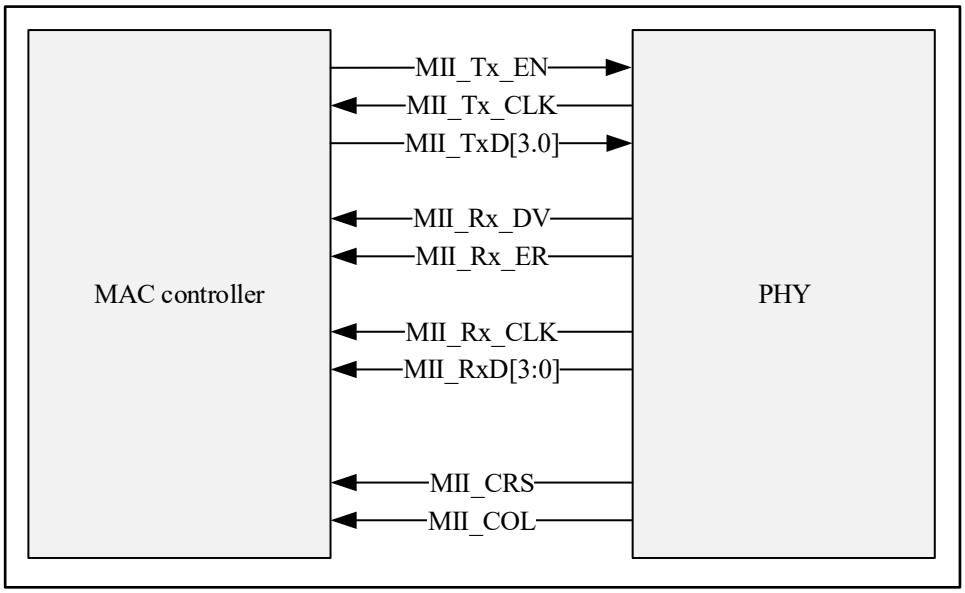
Figure 25-4 MII interface signal line



- MII_Tx_EN: Transmit enable signal, this signal must appear synchronously with the start bit of the data preamble, and keep it until the transmission is completed.
- MII_Tx_CLK: The continuous clock signal used for transmit data. When the data transmission rate is 10Mbps, the clock is 2.5MHz; when the data transmission rate is 100Mbps, the clock is 25MHz.
- MII_TxD[3:0]: Transmit data line, transmit 4-bit data each time, the data is only valid when the MII_Tx_EN signal is enabled. MII_TxD[0] is the lowest bit of the data and MII_TxD[3] is the highest bit. When the MII_Tx_EN signal is disabled, the data transmitted by the PHY is invalid.
- MII_Rx_DV: Receive data valid signal, controlled by PHY, signal valid means PHY has prepared data for MAC to receive. This signal must appear synchronously with the first 4 bits of the frame data and remains active until the data transfer is complete. This signal must be deasserted before the first clock occurs after the last 4 bits of data have been transferred. In order to ensure that the received data is normal, the active level cannot appear after the SFD on the data line appears.
- MII_Rx_ER: Receive error signal, keep the valid state for at least one MII_Rx_CLK clock cycle, indicating that the MAC detects an error in reception. The cause of the error needs to be analyzed according to the state of MII_Rx_DV and the value of MII_RxD[3:0]. Please refer to Table 25-4 for the code of the receiving interface signal.
- MII_Rx_CLK: The clock signal used to receive data. When the data transmission rate is 10Mbps, the clock is 2.5MHz; when the data transmission rate is 100Mbps, the clock is 25MHz.
- MII_RxD[3:0]: Receive data line, receive 4-bit data each time, the data is valid when the MII_Rx_DV signal is valid. MII_RxD[0] is the lowest bit of the data and MII_RxD[3] is the highest bit. If MII_Rx_DV is invalid, but MII_Rx_ER is valid, MII_RxD[3:0] data value has specific meaning, please refer to Table 25-4 for details.
- MII_CRS: Carrier sense signal, controlled by PHY, only works in half-duplex mode. This signal is enabled when the transmitting or receiving medium is not idle. PHY must ensure that the MII_CRS signal remains valid for the entire duration of the collision. This signal does not need to be synchronized with the transmit/receive clock.

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- MII_COL: Collision detection signal, controlled by PHY, only works in half-duplex mode. This signal is enabled when a medium collision is detected and remains active for the duration of the collision. This signal does not need to be synchronized with the transmit/receive clock.

Table 25-3 Transmit interface signal code

MII_Tx_EN	MII_TxD[3:0]	Explanation
0	0000 to 1111	Normal frame interval
1	0000 to 1111	Normal data transfer

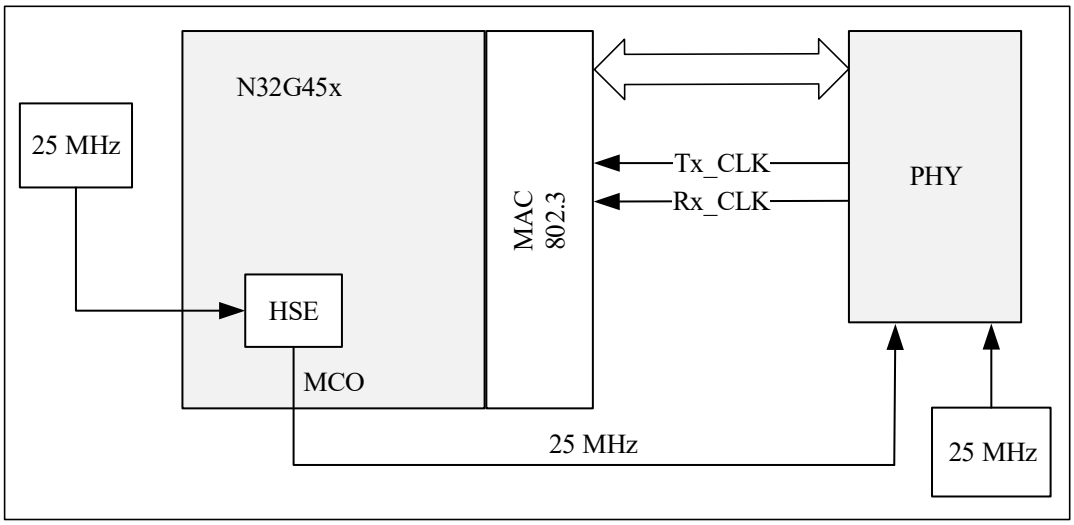
Table 25-4 Receive interface signal code

MII_Rx_DV	MII_Rx_ERR	MII_RxD[3:0]	Explanation
0	0	0000 to 1111	Normal frame interval
0	1	0000	Normal frame interval
0	1	0001 to 1101	Reserved
0	1	1110	Wrong carrier indication
0	1	1111	Reserved
1	0	0000 to 1111	Normal data receive
1	1	0000 to 1111	Error receiving data

25.4.4.1 MII clock source

External PHY module needs an external 25MHz clock drive to generate the Tx_CLK and Rx_CLK clock signals. External 25MHz clock can be different from the MAC clock. Can use an external 25MHz crystal oscillator or configure the appropriate PLL to make the MCU clock output the 25MHz clock provided by the MCO pin.

Figure 25-5 MII clock source



25.4.5 RMII Interface

The RMII specification reduces the number of pins required for communication. The IEEE802.3 standard stipulates that the MII interface requires 16 pins for data and control signals, while the RMII standard reduces the number of pins to 7.

RMII has only one clock signal of 50MHz, both MAC and external PHY need to use this clock source, and transmit

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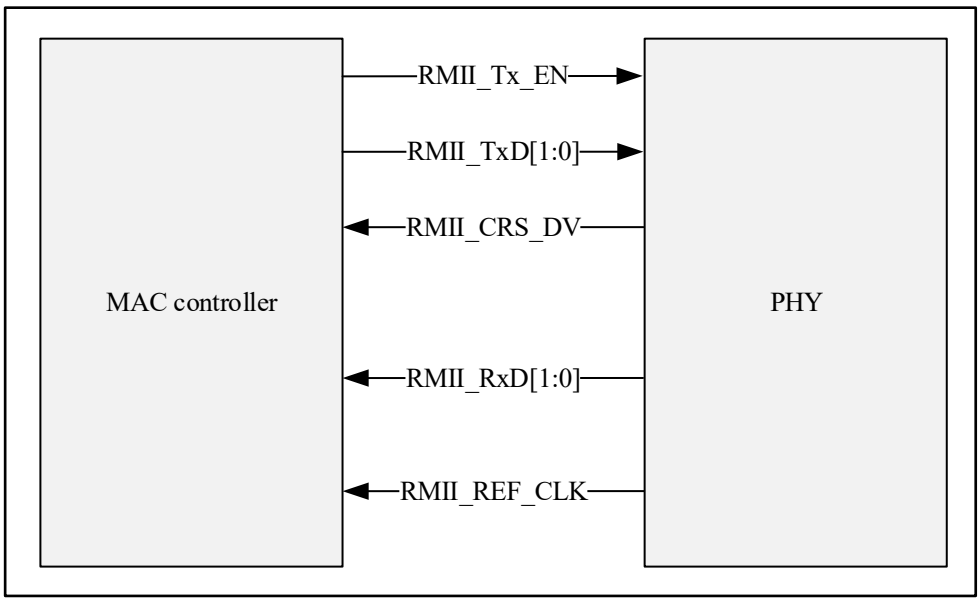
and receive data are transmitted through 2-bit line width respectively.

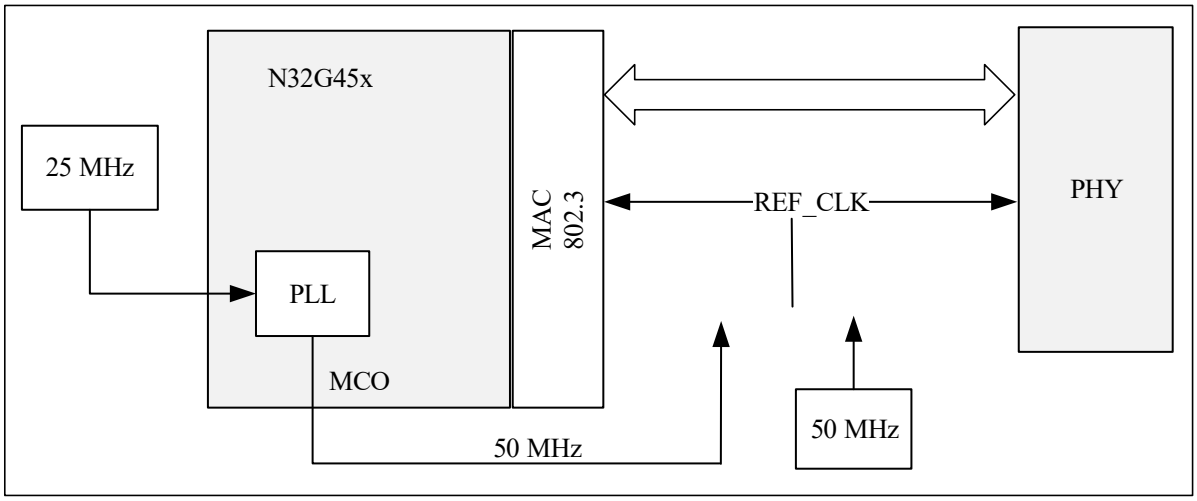
Figure 25-6 RMII interface signal line



25.4.5.1 RMII clock source

As shown in the figure below, an external clock source or by configuring a suitable PLL, the clock output pin MCO of the MCU can provide a 50MHz clock signal.

Figure 25-7 RMII clock source



25.4.6 MAC Function Description

The MAC module performs the encapsulation of transmitted data and received data, and supports half-duplex or full-duplex working modes. Data encapsulation enables frame detection/decoding, frame boundary delimitation, addressing (managing source and destination addresses), and error detection. In half-duplex mode, the CSMA/CD algorithm is used to preempt access to the physical medium, and only two sites in one transmission direction are valid at the same time, preventing and handling conflicts for medium access management; in full-duplex mode, as long as the physical medium supports simultaneous transmit and receive operations, and only two stations that are configured

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in full-duplex mode access the LAN, they can transmit and receive at the same time without conflict.

25.4.6.1 MAC frame transmission process

The DMA controller and MAC in the Ethernet module control all Ethernet frame data transmission. After received the application transmitted instruction, DMA will read the transmit frame from the system storage area and store it in the TxFIFO with a size of 2K. According to the selected cut-through or store-and-forward mode, the data will be taken out to the MAC controller, and the data will transmit to Ethernet PHY through MII/RMII interface, optionally configured to have the MAC controller automatically add a hardware-calculated CRC value to FCS of the data frame. When the MAC controller receives the EOF signal from the TxFIFO, the transmission process ends, and the transmission status information is generated by the MAC controller and written back to the DMA controller, and the transmission status can be queried through the DMA current transmit descriptor.

There are two modes to fetch TxFIFO data to MAC controller:

- Cut-Through (Threshold) mode. When the data in the TxFIFO reaches the set threshold or the EOF is written before the threshold is reached, the data will be taken out of the TxFIFO and transmitted to the MAC controller. ETH_DMAOPMOD.TTC can set this threshold.
- Store-and-Forward mode. After a complete frame is written into TxFIFO, the data in TxFIFO will be transmitted to MAC controller. If the frame is not completely written into TxFIFO, that is, the size of TxFIFO is smaller than the length of the Ethernet frame to be transmitted, the data will also be transmitted to MAC controller when TxFIFO is about to be full.

25.4.6.2 Special case handling when frame is transmitting

When transferring data, if the ETH_DMAOPMOD.FTF is mis-operated, TxFIFO will be cleared (when this bit is set to 1, the data in TxFIFO will be cleared and the pointer of the TxFIFO will be reset. After the clearing operation is completed, this bit will be cleared by hardware), or if the idle DMA transmit descriptor is insufficient, the data cannot be transmitted continuously in time, and MAC controller will identify the data underflow state. If only the SOF signal is received and the EOF signal is not received, MAC will consider the SOF signal invalid, and regard this frame of data as the continuation of the previous frame of data.

If a frame of data to be transmitted occupies two DMA transmit descriptors, the first segment bit (TDES1.FS) and the last segment bit (TDES1.LS) of the first descriptor should be 10b, and the second descriptor should be 01b. If the TDES1.FS of the first descriptor and the second descriptor are both set, and the TDES1.LS of the first descriptor is reset, the TDES1.FS of the second descriptor will be considered invalid, and treat two descriptors as if only one frame was transmitted.

If the length of the data field of MAC frame to be transmitted is less than 46 or the length of the data field of tagged MAC frame to be transmitted is less than 42, can choose to configure MAC controller to automatically fill in data 0, make the length of the frame data field consistent with the relevant definitions of the IEEE802.3 specification. At this time, MAC will ignore the configuration of the DMA descriptor TDES1.DC, and automatically calculate and add the CRC value to FCS of the frame.

25.4.6.3 Jabber timer

The built-in Jabber timer of Ethernet will terminate the transmission of Ethernet frames after more than 2048 bytes are transmitted, to prevent the same station from occupying PHY for a long time. Jabber timer is enabled by default. If the Ethernet frame transmitted more than 2048 bytes, MAC will only transmit 2048 bytes and discard the exceeded frame data.

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25.4.6.4 Retransmission conflict handling mechanism

When the working mode is half-duplex, the data frame transmitted by MAC may collide. If a conflict event occurs and only frame data of no more than 96 bytes in TxFIFO is taken out to MAC, the frame retransmission function will be activated, and MAC will abort the current data transmission, read the data from TxFIFO and retransmit it. If a collision event occurs and more than 96 bytes of data are taken out of TxFIFO to MAC, MAC will abort the current transmission without activating the retransmission function and set TDES0.LC in the descriptor to notify the application.

25.4.6.5 Status information word of frame transmit

After MAC controller frame transmission is completed, the transmission status information word is updated, which includes a number of transmission status flags for the application. If the timestamp function is enabled, the timestamp will be written back to the transmit descriptor along with the transmit status information word.

25.4.6.6 Clear TxFIFO operation

Regardless of whether TxFIFO is popping data into MAC, as long as ETH_DMAOPMOD.FTF is set to 1, TxFIFO is immediately emptied and TxFIFO data pointer is reset. When receiving the clear operation command, all the data taken out from TxFIFO to MAC will be discarded until the descriptor with TDES1.FS of 1 is received. The clear operation will cause MAC controller to generate a data underflow event, and end the transmission of the current frame, and return the transmission status information of the frame to the application program, and also mark the data underflow error flag (TDES0.UF) and frame clear flag (TDES0.FF). After the DMA receives all the status information words of the cleared frame, the clearing operation is completed, and ETH_DMAOPMOD.FTF will also be automatically cleared to 0.

Note: If the amount of received data is large, the flash function needs to be turned on, at the same time, when the receive overflow interrupt occurs, reset the ETH module and re-initialize the related data structure.

25.4.6.7 Transmit flow control

When ETH_MACFLWCTRL.TFE is enabled and working in full-duplex mode, MAC will automatically generate and transmit Pause frames with CRC values when needed. When the software sets ETH_MACFLWCTRL.FCB_BPA to 1, or RxFIFO is full, it will start to generate the Pause frame and transmit the Pause frame out. The pause time specified by the Pause frame is the pause time value preset by the register ETH_MACFLWCTRL.

- If ETH_MACFLWCTRL.FCB_BPA is set to 1 to request flow control, MAC will generate and transmit a single Pause frame. If want to extend the pause time, or abort the pause, need to reconfigure the pause time in the register ETH_MACFLWCTRL and request the transmission of a new Pause frame.
- If transmit flow control is enabled, MAC will generate and transmit a Pause frame when RxFIFO is full. If the RxFIFO is still full after the configured pause time is reached, MAC will transmit another Pause frame. This process is repeated as long as RxFIFO is full. If RxFIFO is not full and the pause time has not been reached, MAC transmits a Pause frame with a pause time of 0 to inform the remote site that the local buffer is ready to receive new data frames.

25.4.6.8 Transmit frame interval management

MAC manages the frame gap time (ie the time interval between two frames). When working in full-duplex mode, after the frame data transmission is completed or MAC enters the idle state, the frame gap counter starts to count. If the next transmission frame arrives before the frame gap time reaches the preset value of these bits of ETH_MACCFG.IFG[2:0], the new transmission frame will not be transmitted until the frame gap time value is

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reached. Otherwise, the frame will be transmitted immediately. When working in half-duplex mode, MAC will start the frame gap counter after the previous transmission frame is completed or MAC enters the idle state. Depending on the situation in which the carrier signal is detected, the processing is different:

1. If the carrier signal appears in the first 2/3 of the frame gap time, the frame gap counter will be reset and count again.
2. If the carrier signal appears in the last 1/3 of the frame gap time, the frame gap counter will not be reset, but continue to count until the frame gap time is reached, and MAC transmit a new frame.
3. If the carrier signal does not appear in the entire frame gap time, after the frame gap time is reached, the frame slot counter will be stopped, and if a previous frame is delayed, a new frame will be transmitted immediately.

25.4.6.9 Transmit checksum module

In order to ensure the reliability of transmission, Ethernet controller automatically calculates and inserts checksums when transmitting, and detects checksum errors when receiving. Only when ETH_DMAOPMOD.TSF is configured to 1, that is, the TxFIFO is set to the store-and-forward mode, and the size of the TxFIFO can accommodate the complete data of the frame to be transmitted, the transmit checksum function can be enabled. If TxFIFO size is less than the frame length, only the checksum of the IPv4 header will be calculated and inserted.

- **IP header checksum**

If the value of the type field of the Ethernet frame is 0x0800, and the value of the version field of the IP packet is 0x4, the checksum module will mark it as an IPv4 data packet, and then replace the content of the checksum field of the frame with the calculation result , and write the corresponding status to TDES0.IHE.

For IPv4 data frames, TDES0.IHE is set by hardware when:

– The value of the received Ethernet type field is 0x0800, but the value of the IP header version field is not 0x4

– The value of the IPv4 header length field is greater than the total length of the frame

– The value of the IPv4 header length field is less than the total IP header length 0x5

For IPv6 data frames, its header does not contain the checksum field, so the checksum module does not change the value of the IPv6 header. TDES0.IHE is set by hardware when:

– The value of the received Ethernet type field is 0x86DD, but the value of the IP header version field is not 0x6

– The frame ends before the complete received of the IPv6 header or extension header

- **TCP/UDP/ICMP checksum**

The checksum module analyzes and judges the frame type (TCP, UDP or ICMP) according to the IPv4 or IPv6 header (including extension header).

The checksum module does not process the frame as follows:

– IPv4 or IPv6 frame is incomplete

– IP frame contain authentication header or encapsulate security functions such as security data

– IP frame is not TCP/UDP/ICMPv4/ICMPv6 data

– IPv6 frame with routing header

The checksum module calculates the data of TCP, UDP or ICMP, and inserts the result into the corresponding field

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of the header. There are two processing methods:

1. Not included the pseudo-headers of TCP, UDP, or ICMPv6 are in the calculation. First include the checksum field in the checksum calculation, and then insert and replace the value of the original checksum field after the calculation is completed.
2. Include the pseudo-header of TCP, UDP or ICMPv6 in the calculation. First, clear the checksum field of the transmission frame to zero, and then insert the original checksum field of the transmission frame after the checksum calculation is completed.

Note: ICMP packets over IPv4 do not define pseudo-headers. To ensure correct checksum calculation, the checksum field must have a value of 0x0000 regardless of the processing method.

After the checksum calculation is complete, the result is written to TDES0.PCE. TDES0.PCE is set by hardware when:

– In store-and-forward mode, frames are forwarded to MAC controller before they are completely written to TxFIFO. Checksum values are not inserted into TCP, UDP, or ICMP headers.
– The frame data has been transmitted, but the data packet taken out by MAC from TxFIFO is smaller than the value indicated by the data length field in the IP header. The result of the checksum calculation will still be inserted into the corresponding field of the header.

If the packet length is greater than the indicated value, the following data will be discarded as padding bytes without reporting an error.

25.4.6.10 MAC receive frame filtering

MAC filtering includes address filtering and error filtering such as short frames, CRC errors, and bad frames. When using receive filters, it is recommended to receive data via store-and-forward mode.

25.4.6.10.1 Address filter

Address filtering is implemented by filtering static physical addresses and multicast HASH lists. If ETH_MACFFLT.RA = 0, only the received frame that passes the address filter will be forwarded; if ETH_MACFFLT.RA = 1, all received frame data will be forwarded, and the filtering result of the frame will still be updated in the receive descriptor, but it will not affect whether frames will be filtered. Address filtering function will filter the destination address and source address of the unicast frame or multicast frame according to the frame filter register parameters set by the application program, discard all frames that cannot pass the filter, and report the corresponding address filtering result.

25.4.6.10.2 Unicast destination filter

If ETH_MACFFLT.HUC is set to 0, unicast filtering can be implemented by using a static physical address; if ETH_MACFFLT.HUC is set to 1, unicast filtering can be implemented by using HASH list.

- **Static physical address filtering**

MAC controller can support up to 4 MAC addresses to perfectly filter the unicast address. MAC will compare the 6-byte unicast address of the received frame with the preset MAC address register bit by bit to confirm whether they are the same. MAC address 0 register is always enabled, MAC address 1 ~ MAC address 3 registers can be enabled through their corresponding enable bits, or they can be set through ETH_MACADDRxHI.MBC[5:0] these bits correspond to the destination address of the received frame bytes are compared.

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- **HASH list filtering**

MAC uses HASH mechanism to imperfectly filter unicast addresses using a 64-bit HASH list, which can cover any possible address with just a small table, but sometimes frames that should be discarded are also received. The filtering process is as follows:

1. MAC calculates the CRC value of the destination address of the received frame, and uses the upper 6 bits of the CRC calculation result as an index to retrieve the HASH list;
2. If the upper 6-bit value of CRC is '000000', select bit0 of the HASH list register; if the upper 6-bit value of the CRC is '111111', select bit63 of the HASH list register. If the corresponding bit is 1, the corresponding frame can pass HASH filter, otherwise it cannot pass HASH filter.

25.4.6.10.3 Multicast destination filter

Clear ETH_MACFFLT.PAM to enable MAC multicast address filtering, and then configure ETH_MACFFLT.HMC to perform different address filtering, similar to the two methods of unicast destination address filtering.

25.4.6.10.4 HASH or perfect address filter

Set ETH_MACFFLT.HPF to 1, and set ETH_MACFFLT.HUC bit for unicast frames or ETH_MACFFLT.HMC bit for multicast frames to 1, can be realized that when the destination address of the received frame matches any one of the HASH filter or the physical address filter, the corresponding frame data is passed.

25.4.6.10.5 Broadcast address filter

By default, MAC will receive any broadcast frame. When ETH_MACFFLT.DBF is set to 1, MAC will discard all received broadcast frames.

25.4.6.10.6 Unicast source address filter

Enable MAC address 1 ~ MAC address 3 registers and set the corresponding ETH_MACADDRxHI.SA to 1. MAC compares and filters the physical address set in the MAC address 1 ~ MAC address 3 registers with the source address of the received frame. MAC also supports filtering of multiple source addresses. If ETH_MACFFLT.SAF is set to 1, MAC will discard frames that cannot be filtered by the source address, and the filtering results will be reflected in the RDES0.SAF of the DMA receive descriptor. When the source address filter is working, the destination address filter is also working. As long as the frame fails to pass any filter, it will be discarded. MAC will only forward the frame that passes both the source address filter and the destination address filter to application.

25.4.6.10.7 Reverse filtering operation

No matter what kind of filter it is, setting ETH_MACFFLT.DAIF and ETH_MACFFLT.SAIF to 1 can reverse the operation at the output of the filter, that is, when the address matches the filter, the frame will not pass, otherwise it will pass. Set ETH_MACFFLT.DAIF to reverse the filtering result of the destination address of unicast and multicast frames, and set ETH_MACFFLT.SAIF to reverse the filtering result of the source address of unicast and multicast frames.

25.4.6.10.8 Promiscuous mode

Setting ETH_MACFFLT.PRM to 1 will enable promiscuous mode. At this time, all received frames can pass the filter, the address filter is invalid, and the destination address error bit and source address error bit of the receive status information are always 0.

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25.4.6.10.9 Pause control frame filtering

MAC will detect the 6-byte destination address field in the received control frame. If ETH_MACFLWCTRL.UP = 0, it will judge whether the value of the destination address field is equal to 0x0180 C200 0001 (the unique value of the control frame in line with the IEEE802.3 specification); if ETH_MACFLWCTRL.UP = 1, in addition to comparing with the unique value defined by the IEEE802.3 specification, it is also compared bit by bit with MAC address set by the controller. If the destination address field comparison is passed, and ETH_MACFLWCTRL.RFE = 1, the corresponding pause control frame function will be triggered. According to the value set by these bits of ETH_MACFFLT.PCF[1:0], it is determined whether the pause frame that passes the filter is forwarded to application.

25.4.6.11 Destination address/source address filtering result

Table 25-5 Destination address filter result list and Table 25-6 Source address filter result list show the filtering results of received frames under different settings according to the destination address filter and the source address filter.

Table 25-5 Destination address filter result list

Frame type	PRM	HPF	HUC	DAIF	HMC	PAM	DBF	Description of destination address filtering results
Broadcast frame	1	x	x	x	x	x	x	Pass
	0	x	x	x	x	x	0	Pass
	0	x	x	x	x	x	1	Fail
Unicast frame	1	x	x	x	x	x	x	All frames pass
	0	x	0	0	x	x	x	Pass when perfect/group filter matches
	0	x	0	1	x	x	x	Fail when perfect/group filter matches
	0	0	1	0	x	x	x	Pass when HASH filter matches
	0	0	1	1	x	x	x	Fail when HASH filter matches
	0	1	1	0	x	x	x	Pass when HASH or perfect/group filter matches
	0	1	1	1	x	x	x	Fail when HASH or perfect/group filter matches
Multicast frame	1	x	x	x	x	x	x	All frames pass
	x	x	x	x	1	x	x	All frames pass
	0	x	0	0	0	x	x	Pass when perfect/group filter matches, if ETH_MACFFLT.PCF = 0x, drop Pause control frame
	0	0	0	1	0	x	x	Pass when HASH filter matches, if ETH_MACFFLT.PCF = 0x, drop Pause control frame
	0	1	0	1	0	x	x	Pass when HASH or perfect/group filter match, if ETH_MACFFLT.PCF = 0x, drop Pause control frame
	0	x	1	0	0	x	x	Fail when perfect/group filter matches, if ETH_MACFFLT.PCF = 0x, drop Pause control frame
	0	0	1	1	0	x	x	Fail when HASH filter matches, if ETH_MACFFLT.PCF = 0x, drop Pause control frame
	0	1	1	1	0	x	x	Fail when HASH or perfect/group filter match, if ETH_MACFFLT.PCF = 0x, drop Pause control frame

Table 25-6 Source address filter result list

Frame type	PRM	SAIF	SAF	Source address filtering result description
Unicast	1	x	x	all frames pass

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Frame type	PRM	SAIF	SAF	Source address filtering result description
frame	0	0	0	Pass when perfect/group filter matches, but don't drop frames that fail
	0	1	0	Fail when perfect/group filter matches, but don't drop frames
	0	0	1	Pass when perfect/group filter matches, drop frames that fail
	0	1	1	Fail when perfect/group filter matches, drop frames that fail

25.4.6.12 MAC frame receive process

As soon as MAC detects an SFD on the interface, the receive procedure is initiated. After MAC receives the frame, it strips its preamble and SFD first, then filters it through the header, and checks the CRC value of the frame with FCS. If the IEEE1588 timestamp is enabled, MAC will record the current time of the system while detecting the SFD of the frame. If the frame passes the address filter check, MAC will transmit the timestamp to the application along with the DMA receive descriptor, otherwise the frame will be discarded. After the receiving engine starts, it will start from the first byte (destination address) after the SFD and send data frames to the RxFIFO.

If ETH_MACCFG.ACS is set and the value of the received frame length/type field is less than 0x600, MAC will automatically strip the PAD and FCS. After the number of bytes transmitted by MAC to RxFIFO reaches the value of the frame length/type field, all remaining bytes (including FCS) are discarded. If the value of the length/type field is greater than or equal to 0x600, regardless of whether the automatic CRC stripping option is enabled, MAC will transmit all received Ethernet frame data to RxFIFO.

If the watchdog timer is enabled (ETH_MACCFG.WD is reset), it will be cut off when the frame length exceeds 2048 bytes (destination address + source address + length/type + data + PAD + FCS). Even if the watchdog timer is disabled, MAC will still cut off frames longer than 16384 bytes.

When RxFIFO works in the cut-through (threshold) mode, if the amount of data in RxFIFO is greater than the threshold set by these bits of ETH_DMAOPMOD.RTC[1:0], it will start to take out data from RxFIFO and notify DMA. When the complete frame is fetched from RxFIFO, MAC controller transmit the receive status information word to DMA controller and writes it back to the receive descriptor. If a frame has started to be taken out of RxFIFO and carried by DMA to the application, even if an error is detected, the frame will continue to be received until the entire frame is received. Since the error information will not be transmitted to DMA controller until this time, the first part of the frame has been read by DMA, so setting MAC to discard all error frames in this mode will have no effect.

When setting ETH_DMAOPMOD.RSF to make RxFIFO work in store-and-forward mode, DMA will only read out a frame after RxFIFO has received a complete frame. If MAC is set to discard all erroneous frames, then DMA will only read out legitimate frames and forward them to application.

25.4.6.13 Receive of multiple frames

Different from TxFIFO, since the status information of the frame follows the frame data, MAC can judge the status of the received frame according to the frame status information immediately after the frame data, so the transmission of the second received frame is immediately followed by the data and status information of the first received frame, as long as RxFIFO is not full, any number of frames can be stored.

25.4.6.14 Receive flow control

When working in full-duplex mode, can set ETH_MACFLWCTRL.RFE to enable or disable the Pause frame detection function. If the Pause frame detection is enabled, MAC can decode the received Pause frame, identify the type field, operand field and pause time field, and transmit it after a certain period of time according to the parameters

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of the pause time field in the Pause frame. During a pause, if a new Pause frame is received, the new pause time will be loaded into the pause time counter immediately. If the value of the received pause time field is 0, MAC will stop the pause time counter and resume data transmission. Determine how these received control frames are handled by configuring these bits in ETH_MACFFLT.PCF[1:0]. If the Pause frame detection function is disabled, MAC will ignore the received Pause frame.

25.4.6.15 Receive frame error handling

- If RxFIFO is full before MAC receives the EOF, MAC controller will drop the entire frame and return to the overflow state, and the overflow counter will be incremented accordingly.
- If RxFIFO works in store-and-forward mode, MAC filter and discard all error frames, but by setting ETH_DMAOPMOD.FEF and ETH_DMAOPMOD.FUF, RxFIFO can still receive error frames and frames whose length is lower than the minimum frame length.
- If RxFIFO works in the cut-through (threshold) mode, all error frames cannot be dropped. Only when DMA reads the SOF of the frame from RxFIFO and RxFIFO obtains the error status of the frame, the error frame can be dropped.

25.4.6.16 Receive frame status information word

After receiving the Ethernet frame, MAC will analyze and record the frame itself and some status information in the receiving process, and write the receiving status information back to the DMA receive descriptor and related status flags. Applications can utilize these status bits to implement upper layer protocols.

Note: The frame length value of 0 indicates that the frame written to RxFIFO is incomplete, such as RxFIFO overflows or the value of the filter is dynamically modified during the receiving process, resulting in failure to pass the filter.

25.4.6.17 Receive checksum module

Set ETH_MACCFG.IPC to enable the receive checksum module. The receive checksum module can calculate the checksum of the IPv4 header and check that it matches the contents of the checksum field of the IPv4 header. If the received Ethernet frame type field value is 0x0800, the frame is an IPv4 frame; if the received Ethernet frame type field value is 0x86DD, the frame is an IPv6 frame.

RDES0.ICEGF is set to 1 when the received IP header:

– The calculated checksum value of IPv4 header does not match the content of its checksum field

– The data type indicated by Ethernet type field does not match IP header version field

– The received frame length is less than the length indicated by IPv4 header length field, or IPv4/IPv6 header is less than 20 bytes

The receiving checksum module can determine whether the data type of the IP packet is TCP, UDP or ICMP, and calculate their checksum according to their respective specifications, including the data of TCP/UDP/ICMPv6 pseudo-header.

RDES0.RMAPCE is set to 1 when the received IP packet:

– The calculated TCP, UDP or ICMP checksum does not match the value of the checksum field of its frame

– The received TCP, UDP or ICMP data length does not match the length indicated by IP header

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The receive checksum module does not calculate if IP packet is incomplete or with security features, IPv6 routing headers, and data types other than TCP, UDP, or ICMP.

25.4.6.18 MAC loopback mode

Loopback mode is disabled by default, which is generally used for application testing and debugging of system hardware and software. Set ETH_MACCFG.LM to 1 to enter MAC loopback mode, and MAC will transmit data by itself and receive it by itself, that is, the sender transmit the frame to its own receiver.

25.4.6.19 MAC management counter (MMC)

MMC is a management counting unit that uses a set of registers to count the sent and received frames. See Section 25.5.22 ~ Section 25.5.32 for the specific function of each register and the address of each statistic counter. These addresses can be used to read/write access to the required transmit/receive counters.

If there is no frame underflow, no carrier, carrier loss, excessive deferral, late collision, excessive collision, or Jabber timeout error in the transmitted frame, it is considered that the transmission process is normal, and MMC transmission counter will be automatically updated.

If the received frame is not aligned, CRC calculation result is inconsistent with the FCS value, the frame length is less than 64 bytes, the value of the length field does not match the actual number of bytes received, exceeds the range, and the MII_Rx_ER input is incorrect, the receiving process is considered normal. MMC receive counter is automatically updated. In addition, if the destination address is not received completely and the length of the discarded frame is less than 6 bytes, MMC reception counter will also be updated.

Note: The maximum range is 1518 bytes for basic frame and 1522 bytes for tagged frame (VLAN frames) (both with preamble and SFD stripped).

25.4.7 Power Management (PMT)

Ethernet module supports two methods to wake up the system from low power mode: Remote Wakeup Frame and Magic Packet Wakeup Frame. To reduce power consumption, the host system and Ethernet module can be put into a low-power state and listen for wake-up frames. If ETH_MACPMTCTRLSTS.PWRDWN is set to 1, Ethernet module will enter a low-power state, and MAC will discard all frames until it receives a remote wake-up frame or a Magic Packet wake-up frame to exit the low-power state. Set ETH_MACPMTCTRLSTS.RWKPKTEN to 1 to wake up the Ethernet module when a remote wake-up frame is received; set ETH_MACPMTCTRLSTS.MGKPKTEN to 1 to wake up the Ethernet module when a Magic Packet wake-up frame is received. Any wake-up function is enabled, as long as MAC receives the corresponding wake-up frame, Ethernet module will generate a wake-up interrupt and exit the low-power state.

25.4.7.1 Remote wakeup frame filter register

The wake-up frame filter has 8 registers that share the same offset address. When the reading or writing of a filter register is completed, the internal pointer will automatically point to the next filter register. Whether it is a read operation or a write operation, it is strongly recommended to operate 8 times continuously, that is, when setting the register, need to divide the set value into 8 times and write the wake-up frame filter register address one by one, and read the wake-up frame filter register 8 times continuously to read the value of the register.

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Table 25-7 Remote wakeup frame filter register overview

Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Wakeup frame filter register 0	Filter 0 byte mask																															
Wakeup frame filter register 1	Filter 1 byte mask																															
Wakeup frame filter register 2	Filter 2 byte mask																															
Wakeup frame filter register 3	Filter 3 byte mask																															
Wakeup frame filter register 4	Reserved				Filter 3 command				Reserved				Filter 2 command				Reserved				Filter 1 command				Reserved				Filter 0 command			
Wakeup frame filter register 5	Filter 3 offset								Filter 2 offset								Filter 1 offset								Filter 0 offset							
Wakeup frame filter register 6	Filter 1 CRC-16																Filter 0 CRC-16															
Wakeup frame filter register 7	Filter 3 CRC-16																Filter 2 CRC-16															

- Filter n byte mask

This register defines which part of the frame is used by filter n (n = 0, 1, 2, 3) to determine whether it is a wake-up frame. Bit 31 of this register is fixed at 0, and bits[30:0] are byte mask bits. Only if the mth bit (m = 0~30) of filter n (n = 0, 1, 2, 3) is 1, CRC module of wake-up frame detection will process the input frame [filter n offset + m] bytes, otherwise ignored and not processed.

- Filter n command

A total of 4 bits control the working mode of filter n. The third part of this register is the address type selection. If this bit is 1, only multicast frames are detected; if this bit is 0, only unicast frames are detected. Bit 2 and bit 1 are fixed to 0. Bit 0 is the enable bit of filter n. When set, filter n is enabled, otherwise, filter n is disabled.

- Filter n offset

Filter n offset defines the offset within the frame of the first byte to be checked by filter n, used in conjunction with the filter n byte mask. The minimum allowed value of the offset value is 12, which represents the 13th byte of the frame (the offset value of 0 represents the first byte of the frame).

- Filter n CRC-16

When the filter n is offset and the corresponding byte mask is 1, this register with a preset CRC-16 code is used for comparison with the CRC-16 value calculated by the frame data (generator polynomial is 0x8005).

25.4.7.2 Remote wakeup frame detection

Set ETH_MACPMTCTRLSTS.RWKPKTEN to 1 to enable detection of remote wakeup frames. PMT module supports 4 programmable filters, allowing different receive frame modes to be supported. If the received frame passes the address filtering of the filter command, and the filter CRC-16 matches the CRC of the incoming frame, MAC identifies the frame as a wake-up frame. The Remote Wakeup CRC field determines the CRC value to compare with the filter CRC-16. PMT module only checks whether the length of the remote wake-up frame is wrong, whether FCS

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is wrong, whether Dribble bit is wrong, whether MII is wrong, whether there is a collision, and ensuring that the remote wake-up frame is not a stub frame. Even if the length of the remote wake-up frame exceeds 512 bytes, if the frame has a valid CRC value, it is still considered a valid wake-up frame. ETH_MACPMTCTRLSTS.RWKPRCVD is set whenever a remote wakeup frame is detected. A remote wakeup frame wakeup interrupt will also be generated if ETH_MACPMTCTRLSTS.RWKPKTEN is enabled.

25.4.7.3 Magic Packet detection

Setting ETH_MACPMTCTRLSTS.MGKPKTEN to 1 enables detection of Magic Packet wakeup frames. A Magic Packet frame is a specially constructed data packet dedicated to wake-up that can be received, analyzed and recognized by the Ethernet module and triggers a wake-up event. The frame format of the Magic Packet wake-up frame is as follows: 6 bytes of all 1 (0xFFFF FFFF FFFF) at any position after the destination address and source address fields, followed by 16 repeated MAC addresses without any interruption and pause; If there are any gaps between these 16 repetitions, need to recheck 0xFFFF FFFF FFFF in the input frame. PMT module will always monitor each frame sent to this node. MAC will filter the Magic Packet frame by address first, and then check whether it conforms to the format of Magic Packet. If it conforms, it will wake up MAC from a low-power state. Both unicast and multicast frames can be used as Magic Packet frames.

The following is an example of a Magic Packet frame with station address 0xAABB CCDD EEFF:

Destination address Source address……FF FF FF FF FF FF

AABB CCDD EEFF AABB CCDD EEFF AABB CCDD EEFF AABB CCDD EEFF

AABB CCDD EEFF AABB CCDD EEFF AABB CCDD EEFF AABB CCDD EEFF

AABB CCDD EEFF AABB CCDD EEFF AABB CCDD EEFF AABB CCDD EEFF

AABB CCDD EEFF AABB CCDD EEFF AABB CCDD EEFF AABB CCDD EEFF

……....CRC

ETH_MACPMTCTRLSTS.MGKPRCVD will be set whenever a Magic Packet frame is detected. Magic Packet wakeup interrupt will also be generated if ETH_MACPMTCTRLSTS.MGKPKTEN is enabled.

25.4.7.4 Considerations when system is in low-power mode

If the external interrupt line 19 is enabled, Ethernet PMT module can also detect frames when MCU is in low-power mode. ETH_MACCFG.RE must be kept as 1 to ensure that MAC also performs Magic Packet/remote wake-up frame detection in a low-power state. In order to reduce power consumption, it is necessary to clear ETH_MACCFG.TE to close the transmission engine in the low-power consumption state, and to close Ethernet DMA module by setting ETH_DMAOPMOD.ST and ETH_DMAOPMOD.SR (corresponding to TxDMA and RxDMA respectively) to 0.

It is recommended to perform the following steps to enter low-power state and wake up:

1. Wait for the transmission of the current frame to complete, then reset ETH_DMAOPMOD.ST to turn off TxDMA;
2. Clear ETH_MACCFG.TE and ETH_MACCFG.RE, close MAC transmit engine and MAC receive engine;
3. By reading ETH_DMASTS.RI, make sure to wait for RxDMA to read all frames in RxFIFO before closing RxDMA;
4. Configure and enable external interrupt line 19 to generate events or interrupts. If external interrupt line 19 is configured to generate an interrupt, also need to write the interrupt handler ETH_WKUP_IRQHandler, and clear

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the interrupt flag bit of external interrupt line 19 in interrupt handler;

5. Set ETH_MACPMTCTRLSTS.MGKPKTEN to 1 to enable detection of Magic Packet wakeup frames or set ETH_MACPMTCTRLSTS.RWKPKTEN to 1 to enable detection of remote wakeup frames;
6. Set ETH_MACPMTCTRLSTS.PWRDWN to 1 to enable low-power consumption mode;
7. Set ETH_MACCFG.RE to 1, open MAC receive engine;
8. Configure MCU to enter the relevant low-power mode;
9. After received a valid wake-up frame, Ethernet module exits low-power state;
10. Read ETH_MACPMTCTRLSTS register to clear power management event flag, turn on MAC transmit engine, and TxDMA and RxDMA;
11. Set system clock, enable HSE and configure RCC clock parameters to restore system to normal state.

25.4.8 Ethernet DMA Function Description

The dedicated DMA controller of Ethernet module can realize the frame data transmission between FIFO and system storage, reducing the intervention of CPU. The communication between DMA and CPU is achieved through 2 data structures:

- Descriptor list (chain or ring) and data buffer
- Control and Status register

The application needs to allocate a list of storage descriptors and physical memory for data caching. Contains two descriptor queues for transmitting and receiving respectively, and the descriptors are stored in the memory in the form of pointers to the buffer. The base address of the transmit descriptor queue is stored in ETH_DMATXDLADDR register, and the transmit descriptor is composed of four descriptor words TDES0-TDES3; the base address of the receive descriptor queue is stored in ETH_DMARXDLADDR register, and the receive descriptor is composed of four descriptor words RDES0-RDES3. Each descriptor can point to up to 2 buffers for storing frame data.

The data buffer allows to store the entire or partial data of the same frame, but not more than one frame. Descriptor queues can be forward-connected through an explicit chain structure or an implicit ring structure. Set RDES1.RCH of the receive descriptor and TDES1.TCH of the transmit descriptor to 1, which can realize the explicit connection of the descriptor (the chain structure of the descriptor), and the buffer address will be stored in RDES2 and TDES2. The address where the next descriptor is stored. Set RDES1.RCH of the receive descriptor and TDES1.TCH of the transmit descriptor to 0, which can realize the implicit connection of the descriptor (the ring structure of the descriptor), and the buffer address will be stored in RDES2 and TDES2, RDES3 and TDES3. When using the buffer address pointed to by the current descriptor, the descriptor pointer will point to the next descriptor. When the chain structure is used, the descriptor pointer points to the second buffer; when the ring structure is used, the next address pointed to by the descriptor pointer is calculated as follows:

Next descriptor address = Current descriptor address + 16 + ETH_DMABUSMOD.DSL [4:0]×4

If current descriptor is the last descriptor in descriptor list, TDES1.TER or RDES1.RER must be set under the ring structure to identify the current descriptor as the last descriptor in the list, and next descriptor will point to the first descriptor in descriptor list. Under chain structure, can also point to the first address in the descriptor list by setting the value of TDES3 or RDES3. Once DMA detects the end of the frame it will jump to the buffer for next frame.

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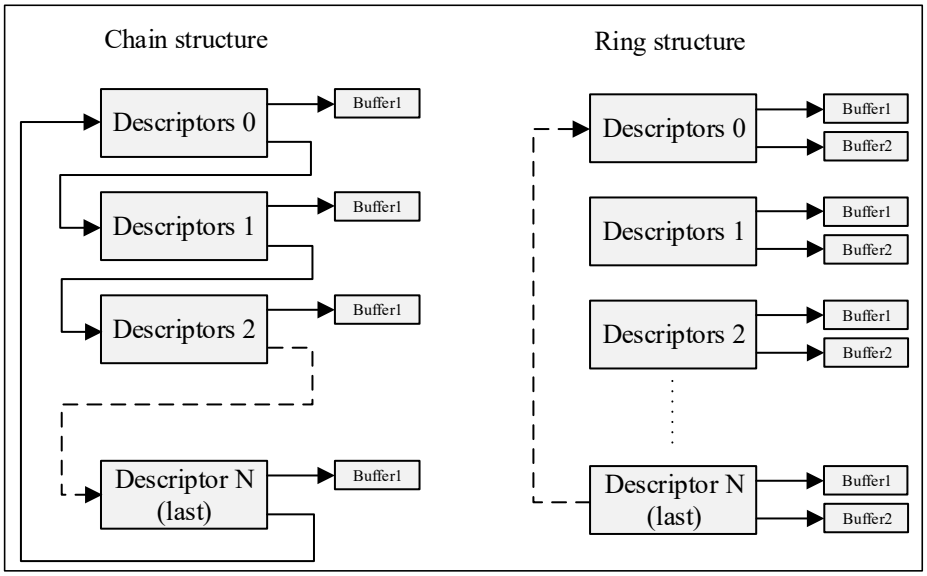
Figure 25-8 Two structures of descriptor



25.4.8.1 Data buffer address alignment

The alignment types supported by Ethernet DMA controller include byte alignment, halfword alignment, and word alignment. So the application can configure the transmit data buffer address and receive data buffer address to any address. However, when DMA initiates a transfer, the address is always accessed in a word-aligned manner. The read buffer and write buffer accesses are also different:

- Read buffer: If the address of transmit buffer is 0x2000 01A2, and need to transfer 15 bytes. After starting the read operation, DMA will actually read 20 bytes from addresses 0x2000 01A0, 0x2000 01A4, 0x2000 01A8, 0x2000 01AC and 0x2000 01B0, and then discard the first 2 bytes (0x2000 01A0 and 0x2000 01A1) and the last 3 bytes (0x2000 01B1, 0x2000 01B2 and 0x2000 01B3).
- Write buffer: If the address of receive buffer is 0x2000 0AB2, and need to transfer 16 bytes. After starting the write operation, DMA will actually write five 32-bit data from address 0x2000 0AB0 to 0x2000 0AC0. But the first 2 bytes (0x2000 0AB0 and 0x2000 0AB1) and the last 2 bytes (0x2000 0AC2 and 0x2000 0AC3) are filled with null data instead.

Note: DMA controller will not write any data beyond the defined buffer address.

25.4.8.2 Buffer effective length

In process of transmit a frame, TxDMA will transmit the bytes of effective length of buffer indicated in TDES1 to MAC controller. Data for a frame can be in multiple different buffers. If TDES0.FS read by DMA controller is 1, indicating the beginning of a new frame buffer, DMA will mark the first byte transmitted as the beginning of the frame. If TDES0.LS read by DMA controller is 1, it indicates the last part of the data of current frame. As long as the frame length is not particularly large, generally a frame will be stored in a buffer, so TDES0.FS and TDES0.LS will be set at the same time in same descriptor.

In process of receive a frame, the value of the buffer length field of the received frame must be word-aligned. For word-aligned or non-word-aligned buffer addresses, the receive operation is not the same as the transmit operation. If the receive buffer address is word-aligned, it is similar to the sending process, and the effective length of the buffer is determined by the value configured in RDES1; If the receive buffer address is not word-aligned, the effective length of the buffer shall be the value configured in RDES1 minus the lower 2 bits of the buffer address. Assuming

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that the total size of the cache is 1024 bytes, the address of the buffer is 0x2000 0001, and the lower 2 bits of the address are 01b, then the effective length of the buffer is 1023 bytes, ranging from 0x2000 0001 at the beginning of the frame to 0x2000 03FF.

When an SOF is received, DMA controller will set RDES0.FS to 1, and when an EOF is received, RDES0.LS will be set to 1. If the value of the receive buffer length field is configured to be large enough to store a complete frame, RDES0.FS and RDES0.LS will be set in the same descriptor. The actual received frame length can be obtained through these bits of RDES0.FL[13:0]. Application can calculate the unused buffer space by subtracting the actual received frame length from the value of receive buffer length configuration field. RxDMA always uses a new descriptor to receive the next frame.

25.4.8.3 TxDMA

25.4.8.3.1 Transmit frame format

IEEE 802.3 stipulates that a complete transmission frame should consist of preamble, SFD, destination address (DA), source address (SA), QTAG prefix (optional), length/type field (LT), data, PAD padding field (optional) and FCS composition. Both preamble and SFD are automatically generated by MAC, and application only needs to store the destination address, source address, length/type, data, and QTAG, padding field and FCS configured as needed. PAD and FCS can be automatically generated by configuring TDES1.DP and TDES1.DC respectively.

25.4.8.3.2 Transmit frame processing

A frame can be spread across different buffers and also requires multiple descriptors. When TDES1.FS is set, it means that the buffer pointed to by current descriptor is frame header. When TDES1.LS is set, it means that the buffer pointed to by current descriptor is the end of the frame. For other descriptors of current frame (descriptors whose TDES1.LS is 0), TxDMA controller only modifies and clears its TDES0.OWN bit. After transmit the data of last buffer, DMA will write the transmit status information of the entire frame into TDES0 of the last transmit descriptor and return. The data is transferred from system memory to TxFIFO, and start transmit data, but the actual data transmission is determined by MAC according to cut-through (threshold) mode or store-and-forward mode.

25.4.8.3.3 TxDMA descriptor

TxDMA descriptor structure contains four 32-bit words TDES0, TDES1, TDES2 and TDES3. If IEEE 1588 timestamp function is enabled, TDES2 and TDES3 are also used to store the lower 32 bits of timestamp and the upper 32 bits of timestamp respectively (TxDMA controller will write the timestamp into TDES2 and TDES3 after frame transmission is completed. And at the same time, set TDES0.TTSS to 1 to mark timestamp of current frame as recorded). Each bit is defined and described in detail as follows:

Note: If a frame is described by multiple descriptors, the control bits for descriptors (except TDES1.IC) are only valid for first descriptor. Status information and time stamps (if time stamping is enabled) are only written back to last descriptor.

Table 25-8 Transmit descriptor overview

Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TDES0	OWN	Status bits																														
TDES1	Control bits																Buffer 2 bytes count														
																						Buffer 1 bytes count										

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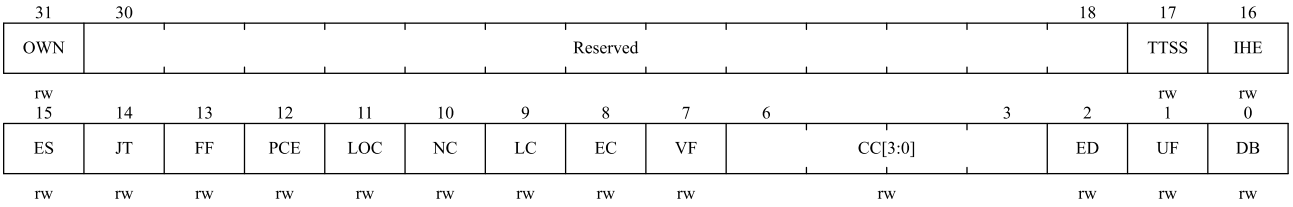
Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TDES2	Buffer 1 address/Timestamp low
TDES3	Buffer 2 address/Next descriptor address/Timestamp high

- **TDES0: Transmit descriptor word 0**



Bit field	Name	Description
31	OWN	Occupancy bit. 0: Indicates that CPU occupies descriptor. 1: Indicates that DMA occupies descriptor. DMA clears this bit to 0 after transferring a complete frame or reading out all the data in buffer. The occupancy bit of first descriptor of the same frame can only be set to 1 after the occupancy bits of the following descriptors are all set to 1.
30:18	Reserved	Reserved, the reset value must be maintained.
17	TTSS	Transmit timestamp status bit. As a flag bit, when set to 1, it means that the frame timestamp corresponding to the descriptor is recorded, and the recorded timestamp is placed at TDES2 and TDES3. This bit is only valid when TDES1.LS is 1.
16	IHE	IP header error. An IP header error occurs when any of the following occurs: IPv4 frame: • The value of the header length field is less than 0x5 • The value of the header length field does not match the received header length • The value of the header version field does not match the value of the frame length/type field IPv6 frame: • The length of the main header is less than 40 bytes • The value of the header version field does not match the value of the frame length/type field 0: No errors found for IP packet header. 1: MAC sender found an error in IP packet header.
15	ES	Error summary. This bit is the logical OR of the following bits (if an error occurs, this bit is set to 1): TDES0[16]: IP header error TDES0[14]: Jabber timeout TDES0[13]: Frame clear TDES0[12]: IP data error

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Bit field	Name	Description
		TDES0[11]: Carrier loss TDES0[10]: No carrier TDES0[9]: Late collision TDES0[8]: Excessive collision TDES0[2]: Excessive deferral TDES0[1]: Data underflow error
14	JT	Jabber timeout. This bit is only set when ETH_MACCFG.JD bit is reset. 0: No Jabber timeout occurred. 1: A Jabber timeout occurred at MAC sender.
13	FF	Frame clear. When set to 1, it indicates that the data in TxFIFO has been emptied.
12	PCE	IP data error. The sender will check the value of data length field of IPv4 or IPv6 header with the actual number of TCP, UDP and ICMP data received, and set 1 to report an error if they do not match. 0: No IP data error occurred. 1: An IP data error occurred at MAC sender.
11	LOC	Carrier loss. When transmitting, carrier loss will probabilistically occur if CRS signal (MII_CRS) is inactive for one or more transmit clock cycles and no collision occurs. This bit is only valid in half-duplex mode. 0: No carrier loss occurred. 1: A carrier loss occurred when frame is transmitted.
10	NC	No carrier. 0: Carrier sense signal of PHY is valid. 1: Carrier sense signal of PHY is invalid when frame is transmitted (Carrier signal is not sensed).
9	LC	Late collision. If a collision occurs after 64 bytes (including the preamble) have been transmitted, the situation is called a late collision. 0: No late collision occurred. 1: A late conflict has occurred. *Note: This bit has no effect if the overflow error bit (TDES0.UF) is set.*
8	EC	Excessive collision. If ETH_MACCFG.DR (close retry bit) is 1, then after a collision, this bit is set to 1; if ETH_MACCFG.DR (close retry bit) is 0, then after 16 consecutive collisions, this bit is set 1. If this bit is set, the transmission of the current frame is aborted. 0: No excessive collision occurred. 1: Excessive collision occurred.
7	VF	VLAN frame. 0: The transmitted frame is a normal frame. 1: The transmitted frame is a VLAN frame.

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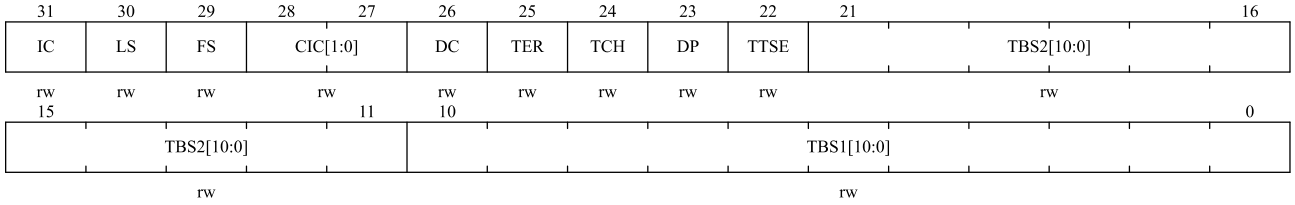
Bit field	Name	Description
6:3	CC[3:0]	Collision count. This 4-bit value records the number of collision that occurred before frame was transmitted. These bits have no effect when TDES0.EC is 1.
2	ED	Excessive deferral. This bit is valid when ETH_MACCFG.DC is 1. If this bit is set, the transmission of the current frame is aborted. 0: Excessive deferral has not occurred. 1: Excessive deferral caused by the delay of more than 3036 bytes.
1	UF	Data underflow error. The data underflow error means that DMA encounters an empty buffer when transmission a frame, causing MAC to abort the transmitting of current frame because the data arrives too slowly. At this time, the transmit process enters suspended state, and ETH_DMASTS.UNF and ETH_DMASTS.TI are both set to 1. 0: No data underflow error occurred. 1: A data underflow error has occurred.
0	DB	Deferral status bit. This bit indicates whether frame delay occurs because the carrier sense signal CRS is occupied before MAC transmit the frame. This bit is only valid in half duplex mode. 0: No transmission delay has occurred. 1: MAC is delayed and the transmission is delayed.

- **TDES1: Transmit descriptor word 1**



Bit field	Name	Description
31	IC	Interrupt-on-completion control bit. This bit is valid after TDES1.LS is set. 0: ETH_DMASTS.TI will not be set when frame transmission is complete. 1: ETH_DMASTS.TI will be set when frame transmission is complete.
30	LS	Last block. This bit indicates that buffer contains the last block of frame. 0: The descriptor buffer does not contain the last block of frame. 1: The descriptor buffer stores the last block of frame.
29	FS	First block. This bit indicates that buffer contains the first block of frame. 0: The descriptor buffer does not contain the first block of frame. 1: The descriptor buffer stores the first block of frame.
28:27	CIC[1:0]	Checksum insertion control bits. 00: Do not insert checksum.

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Bit field	Name	Description
		01: Only enable calculation and insertion of checksum of hardware IP header. 10: Enable calculation and insertion of checksums of hardware IP headers and data fields, but do not calculate checksums of pseudo-headers. 11: Enable calculation and insertion of checksum of hardware IP header and data field, and also calculate checksum of pseudo-header.
26	DC	Disable CRC. This bit is only valid when TDES1.FS is 1. 0: MAC automatically insert CRC field. 1: MAC does not insert CRC field.
25	TER	Ring transmit end mode bit. This bit is only used in ring structures and has higher priority than the TDES1.TCH bit. 0: Current descriptor is not the last of descriptor queue. 1: Current descriptor reaches the last of descriptor queue, and DMA returns base address of list.
24	TCH	Second address linked list mode bit. This bit is used in a chain structure. When this bit is 1, the value of these bits in TDES1.TBS2[10:0] is invalid. 0: Second address in descriptor is the address of second buffer. 1: Second address in descriptor is the address of next descriptor.
23	DP	Disable PAD. This bit is only valid when TDES1.FS is 1. 0: MAC automatically adds padding bytes to frames whose frame length is less than 64 bytes, and inserts CRC value, ignoring TDES1.DC. 1: MAC does not automatically pad bytes for frames whose frame length is less than 64 bytes.
22	TTSE	Transmit timestamp enable bit. This bit is only valid when TDES1.FS is 1. When this bit is 1 and ETH_PTPTSCTRL.TSENA is 1, transmit frame timestamp function is enabled. 0: Disable transmit frame timestamp function. 1: Enable transmit frame timestamp function.
21:11	TBS2[10:0]	Transmit buffer 2 size. These bits give the size (in bytes) of second data buffer and are invalid if TDES1.TCH is 1.
10:0	TBS1[10:0]	Transmit buffer 1 size. These bits give the size (in bytes) of first data buffer, if its value is 0, DMA skips this buffer and according to TDES1.TCH uses buffer 2 (TDES1.TCH = 0) or next descriptor (TDES1.TCH = 1).

- **TDES2: Transmit descriptor word 2**

Before transmit a frame, application must configure TDES2 as the address of transmit buffer 1. After data is transmitted, DMA can use them to store the lower 32 bits of the frame's timestamp.

When the value of TDES2 represents the physical address of buffer 1, there is no restriction on the address alignment

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of the cache. When the value of these bits represents the lower 32 bits of the timestamp, TDES1.TTSE and TDES1.LS of the current descriptor must be set.

- **TDES3: Transmit descriptor word 3**

Before transmit a frame, application must configure TDES3 as the address of transmit buffer 2, or as the address of next descriptor (depending on whether the descriptor type is chain or ring). After data is transmitted, DMA can use them to store the upper 32 bits of the frame's timestamp.

When the value of TDES3 represents the physical address of buffer 2 (TDES1.TCH = 0), there is no restriction on the address alignment of the buffer. When the value of TDES3 represents next descriptor address (TDES1.TCH = 1), these bits must be word-aligned. When the value of TDES3 represents the upper 32 bits of timestamp, TDES1.TTSE and TDES1.LS of the current descriptor must be set.

25.4.8.3.4 Processing after sending query suspension

After the transmission is started, DMA will continuously query transmit descriptor. DMA will enter the suspended state and suspend the transmission in the following cases. The current descriptor is fixed to the last descriptor before suspension.

- When DMA detects that TDES0.OWN is 0, that is, CPU occupies the descriptor, DMA will enter suspended state and suspend the query. At this time, ETH_DMASTS.NIS and ETH_DMASTS.TU will be set to 1. In this case, it is necessary to set TDES0.OWN to 1 to transfer the ownership of descriptor to DMA, and then initiate a send query command to try to re-acquire descriptor.
- In process of transmit a frame, if a data underflow error is detected, frame transmission will be suspended and enter suspended state. TDES0.ES and TDES0.UF will be set, as will ETH_DMASTS.AIS and ETH_DMASTS.UNF. In this case, it is still necessary to initiate a transmit query command to try to re-obtain descriptor.

25.4.8.3.5 TxDMA operation flow

DMA operation of the sender is divided into two cases: non-OSF mode and OSF mode. By default, non-OSF mode is operated. The specific description and operation flow are as follows:：

- **Non-OSF mode**

The operation flow of TxDMA in default mode is as follows:

1. Initialize frame data to transmit buffer, configure transmit descriptor (TDES0~TDES3), and set TDES0.OWN to 1;
2. Set ETH_DMAOPMOD.ST to 1 to enable TxDMA controller;
3. Start TxDMA controller to poll transmit descriptor list for frames to be transmitted. If TxDMA detects that an error has occurred, or TDES0.OWN is 0, controller will terminate transfer and enter suspension state and set ETH_DMASTS.TU (transmit buffer unavailable) and ETH_DMASTS.NIS (normal interrupt summary) to 1, and then skip to step 8;
4. If TDES0.OWN bit is set to 1, that is, fetched descriptor is occupied by DMA, then DMA parses the configured transmit frame and transmit data buffer address from descriptor;
5. DMA fetches data from memory, and then dumps it to TxFIFO;
6. TxDMA controller will keep polling descriptor list until TDES1.LS is set to 1 after the end of frame has been

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transmitted. If TDES1.LS of current descriptor is 0, after all buffered data is transmitted to TxFIFO, clear TDES0.OWN to close this descriptor. TxDMA controller will wait to write back the descriptor status and the IEEE 1588 timestamp value (provided that timestamp function is enabled);

7. After completing a complete frame transmission, ETH_DMASTS.TI (transmit status bit) will be set only when TDES1.IC is 1. If DMA interrupt is enabled, corresponding interrupt will be entered. Then DMA controller returns to step 3 to continue processing next frame;
8. In suspended state, if any write operation is performed to ETH_DMATXPD register, TxDMA will return to running state, try to re-acquire descriptor, and return to step 3, and transmit underflow flag will be cleared.

- **OSF mode**

Set ETH_DMAOPMOD.OSF to 1 to enter Operation Second Frame (OSF) mode. In this mode, TxDMA can transmit next frame before status information of the previous frame is written back. OSF mode can improve the transmission efficiency when system clock frequency is much higher than MAC frequency (10Mbps or 100Mbps). After DMA has transmitted the previous frame of data, it can immediately query the transmit descriptor of second frame without waiting for the status of the frame to be written back. If both TDES0.OWN and TDES1.FS are set to 1, TxDMA will immediately read the second frame data and store it in TxFIFO.

The operation flow of TxDMA in OSF mode is as follows:

1. Follow steps 1~6 of TxDMA default mode;
2. DMA directly fetches the next descriptor without waiting until last descriptor of previous frame is closed (TDES1.LS is 1);
3. If TDES0.OWN is 1, that is, fetched descriptor is occupied by DMA, the data of next frame is read from the parsed transmit buffer address; if TDES0.OWN is 0, fetched descriptor is not occupied by DMA, TxDMA enters suspended state and skips to step 7;
4. TxDMA controller will poll descriptor list until the end of frame is transmitted. If a frame is described by multiple descriptors, the intermediate descriptors are closed after acquisition;
5. TxDMA waits for transmit status information and timestamp of the previous frame (provided that timestamp is enabled). After receive status information, TDES0.OWN is cleared, indicating that ownership of descriptor is handed over to CPU, and at the same time the relevant status information will be written to corresponding bit of TDES0 by DMA;
6. After transmit a complete frame, ETH_DMASTS.TI will be set only when TDES1.IC is 1. If DMA interrupt is enabled, corresponding interrupt will be entered. If status information returned by previous frame is normal, skip to step 3; if it indicates that there is a data underflow error, TxDMA enters suspended state and skips to step 7;
7. If the pending status information and timestamp of a transmit frame are received in suspended state (provided that timestamp is enabled), TxDMA will write this information into transmit descriptor and corresponding TDES0.OWN cleared, then set relevant interrupt flag and return to suspend state;
8. In suspended state, if any write operation is performed to register ETH_DMATXPD, TxDMA will return to running state and try to re-acquire descriptor, and transmit underflow flag will be cleared. If there is pending status information, skip to step 1 again; otherwise, skip to step 2 again.

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25.4.8.4 RxDMA

25.4.8.4.1 Receive frame processing

When MAC receives the frame data, address filtering module also starts to work. If the frame does not pass address filtering, MAC RxFIFO will discard frame and will not forward it to receiving buffer through RxDMA. Conversely, if working in cut-through (threshold) mode and the received frame length is greater than or equal to the preset receive threshold, or working in store-and-forward mode and a complete frame is stored in the RxFIFO, it will be forwarded to the receive buffer. In the process of receiving a frame, if the data in RxFIFO is less than 64 bytes, the receiving process collides, or the receiving frame is terminated in advance, the data in RxFIFO will be lost and will not be forwarded.

When the forwarding conditions are met, RxDMA controller starts to transfer data from RxFIFO to the receive buffer. If the current buffer contains SOF, RDES0.FS will be set when RxDMA controller writes back the frame receiving state, indicating that the first part of the frame is stored in this descriptor. If the current buffer contains EOF, RDES0.LS is set when RxDMA controller writes back the frame received state to indicate that this descriptor stores the last part of the frame. Usually when the receive buffer size is larger than the length of the received frame, RDES0.FS and RDES0.LS will be set in the same descriptor. When the buffer receives EOF, or the buffer of the current descriptor is not enough to store the entire frame, RxDMA will get the next receive descriptor and clear the RDES0.OWN of the previous descriptor to close the previous descriptor. When RDES1.DIC = 0 and RDES0.LS is set, other states of the descriptor will also be updated and ETH_DMASTS.RI will be set; when RDES1.DIC = 1, ETH_DMASTS.RI will not be set. When a new frame is received, if RDES0.OWN of the descriptor is 1, the above RxDMA controller operation is repeated. If the descriptor's RDES0.OWN is 0, DMA controller enters the pending state and sets ETH_DMASTS.RU to 1. Record the current value of the descriptor list address pointer and use it as the starting address of the descriptor after exiting the pending state.

25.4.8.4.2 RxDMA descriptor

RxDMA descriptor structure contains four 32-bit words, RDES0, RDES1, RDES2, and RDES3. If IEEE 1588 timestamp function is enabled, RDES2 and RDES3 are also used to store the lower 32 bits of the timestamp and the upper 32 bits of timestamp, respectively (MAC controller will complete the reception of the timestamped frame and before DMA closes descriptor (RDES0.OWN is cleared to 0), and the timestamp is written to RDES2 and RDES3). Each bit is defined and described in detail as follows:

Table 25-9 Receive descriptor overview

Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RDES0	OWN	AFM	Status bits																													
RDES1	DIC	Control bits														Buffer 2 bytes count																
RDES2	Buffer 1 address/Timestamp low																															
RDES3	Buffer 2 address/Next descriptor address/Timestamp high																															

- **RDES0: Receive descriptor word 0**

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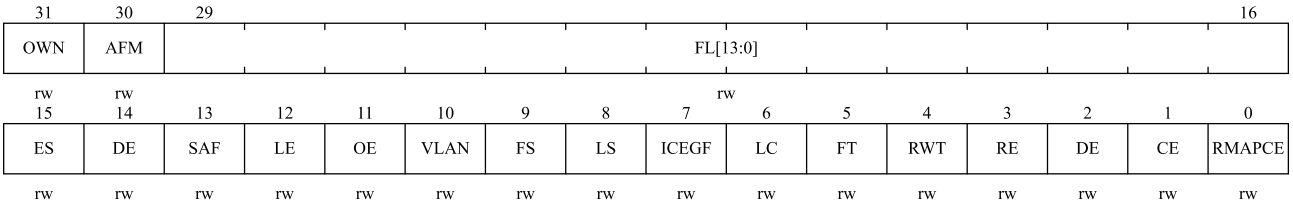

Bit field	Name	Description
31	OWN	Occupancy bit. 0: Indicates that CPU occupies descriptor. 1: Indicates that DMA occupies descriptor. DMA clears this bit to 0 after transferring a complete frame or filling the buffer corresponding to descriptor.
30	AFM	Failed destination address filter. 0: The received frame passes destination address filter. 1: The received frame does not pass destination address filter.
29:16	FL[13:0]	Frame length. These bits indicate the byte length of the received frame transferred to the input buffer. This bit is only valid when RESD0.LS is 1 and RDES0.DE is 0. If both RESD0.LS and RESD0.ES are 0, these bits indicate the cumulative number of bytes that the current received frame has transferred to the memory.
15	ES	Error summary. This bit is only valid when RESD0.LS is 1. This bit is the logical OR of: RDES0[14]: Descriptor error RDES0[11]: Overflow error RDES0[7]: IP header error RDES0[6]: Late collision RDES0[4]: Watchdog timeout RDES0[3]: Receive error RDES0[1]: CRC error
14	DE	Descriptor error. This bit is only valid when RESD0.LS is 1. When the buffer size of current descriptor is smaller than the frame length of received frame and DMA cannot occupy the next descriptor, a descriptor error will occur. 0: No descriptor error occurred. 1: A descriptor error has occurred.
13	SAF	Failed source address filter. 0: No fail source address filter event occurred. 1: The received frame did not pass source address filter.
12	LE	Length error. This bit is only valid when RDES0.FT is 0, which indicates that the value of the received Ethernet frame header length/type field does not match the actual length of the received frame.

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Bit field	Name	Description
		0: No length error occurred. 1: A length error has occurred.
11	OE	Overflow error. This bit is set when RxFIFO has overflowed and part of the received frame has been transferred to input buffer. 0: No overflow error occurred. 1: RxFIFO overflow occurred and frame data is invalid.
10	VLAN	VLAN frame. 0: Received frame is a non-VLAN frame. 1: Currently received frame is a VLAN frame.
9	FS	First descriptor. This bit indicates that the current descriptor holds the first part of received frame. 0: The current descriptor does not hold the first part of frame. 1: The current descriptor holds the first part of frame.
8	LS	Last descriptor. This bit indicates that the current descriptor holds the last part of received frame. 0: The current descriptor does not hold the last part of frame. 1: The current descriptor holds the last part of frame.
7	ICEGF	IP frame header checksum error. 0: No IPv header checksum error occurred. 1: An IPv4 or IPv6 header error has occurred. Errors may be due to mismatched values in EtherType and IP Version fields, an incorrect IPv4 header checksum, or insufficient IP header bytes for Ethernet frame.
6	LC	Late collision. A late collision indicates that a collision occurred after 64 bytes of data were received. This bit is only valid in half-duplex mode. 0: No late collision occurred. 1: A late collision occurred in the process of receiving frame.
5	FT	Frame type. 0: Received frame is an IEEE802.3 frame. 1: Received frame is an Ethernet type frame (the value of Ethernet frame header length/type field is greater than or equal to 0x0600, when the received frame is too short (the frame length is less than 14 bytes), this bit is invalid).
4	RWT	Receive watchdog timeout. When ETH_MACCFG.WD = 0, this bit indicates that more than 2048 bytes of frame data have been received; when ETH_MACCFG.WD = 1, this bit indicates that more than 16384 bytes of frame data have been received. 0: No receive watchdog timeout occurred. 1: A watchdog timeout occurred while receiving a frame, and current received frame will be truncated.
3	RE	Receive error. This bit indicates that the valid interface signal Rx_ER is received when the Rx_DV signal is valid during the frame receiving process.

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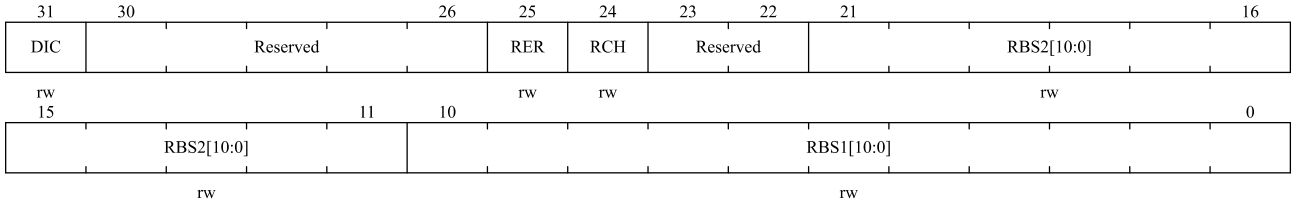
Bit field	Name	Description
		0: No reception error occurred. 1: A reception error has occurred.
2	DE	Dribble bit error. This bit is only valid in MII mode, indicating that the received frame length is not an integer multiple of bytes. 0: No Dribble bit error occurred. 1: A Dribble bit error has occurred.
1	CE	CRC error. This bit is only valid when RDES0.LS is 1, indicating that the FCS of the received frame does not match the hardware calculation result. 0: No CRC error occurred. 1: A CRC error has been detected in received frame.
0	RMAPCE	Data checksum error. 0: No data checksum error occurred. 1: TCP, UDP or ICMP checksum calculated by hardware does not match the value of TCP, UDP or ICMP checksum field of received frame. This bit is also set to 1 when the data length of received Ethernet frame does not match the value of IPv4 or IPv6 packet length field.

- **RDES1: Receive descriptor word 1**



Bit field	Name	Description
31	DIC	Turn off receive completion interrupt. 0: ETH_DMASTS.RI will be set to 1 immediately after receive is completed. At this time, if the corresponding interrupt is enabled, an interrupt will be triggered. 1: ETH_DMASTS.RI will not be set to 1 after receive is completed, and the corresponding interrupt will not be triggered.
30:26	Reserved	Reserved, the reset value must be maintained.
25	RER	End of receive descriptor ring structure. This bit indicates that the last descriptor in descriptor list is reached, and next descriptor automatically returns the base address of the list. 0: Current descriptor is not the last descriptor. 1: Reach the last descriptor of the descriptor list.
24	RCH	Second address list. This bit is only used in chain structure. When this bit is 1, these bit values of RDES1.RBS2[10:0] are ignored. 0: Second address in descriptor points to the address of second buffer. 1: Second address in descriptor is the address of next descriptor.

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Bit field	Name	Description
		Note: When RER=1, even if this bit is set, the next descriptor will return the list base address.
23:22	Reserved	Reserved, the reset value must be maintained.
21:11	RBS2[10:0]	Receive buffer 2 size. These bits indicate the size of receive buffer 2 in bytes. The buffer size must be set to a multiple of 4. These bits are ignored when RDES1.RCH is 1.
10:0	RBS1[10:0]	Receive buffer 1 size. These bits indicate the size of receive buffer 1 in bytes. The buffer size must be set to a multiple of 4. If these bits are 0, DMA ignores the buffer and uses buffer 2 (RDES1.RCH = 0) or next descriptor (RDES1.RCH = 1) depending on RDES1.RCH.

- **RDES2: Receive descriptor word 2**

RDES2 has 2 functions: the address pointer of buffer 1 and the lower 32 bits of the timestamp. Configured as the address of buffer 1 before DMA controller acquires this descriptor. If RDES1.RBS1 is not 0, the address in RDES2 is used to store the received data frame. There is no restriction on the address alignment of the cache. When timestamp function is enabled and RDES0.LS is 1, if the received frame passes the address filtering and corresponding frame type enable bit is set, DMA will write the lower 32 bits of the timestamp into RDES2. If corresponding frame type enable bit is not set in received frame, RDES2 will keep the value of the original address.

- **RDES3: Receive descriptor word 3**

RDES3 has 2 functions: when data is received, the address of buffer 2 or the address of next descriptor and the high 32-bit timestamp are stored. Before DMA controller obtains the descriptor, if RDES1.RCH = 0, configure RDES3 as the address of buffer 2. At this time, if RDES1.RBS1 is not 0, use the address of RDES3 to store the received data frame; if RDES1.RCH = 1, then configure RDES3 as the next descriptor address, and the address needs to be word-aligned. If RDES1.RER is not 0, then RDES3 is ignored.

When timestamp function is enabled and RDES0.LS is 1, if the received frame passes the address filtering and the corresponding frame type enable bit is set, DMA will write the high 32 bits of the timestamp to RDES3. If the corresponding frame type enable bit is not set in the received frame, RDES3 will keep the value of the original address.

25.4.8.4.3 Processing when a new frame is received in suspended state

In suspended state, when a new frame is received and the forwarding conditions are met, RxDMA will obtain the frame descriptor. If RDES0.OWN is 1, RxDMA controller exits the suspend state and resumes the running state to start receiving frames. But when RDES0.OWN is 0, application can choose whether to clear the frame in RxFIFO by configuring ETH_DMAOPMOD.DFF. If ETH_DMAOPMOD.DFF = 0, RxDMA controller will drop the current frame at the top of RxFIFO and increment ETH_DMAMFBOCNT.MISFRMCNT (missed frame count) by 1 (repeat the process if there is more than one frame in RxFIFO). If ETH_DMAOPMOD.DFF = 1, the frame at the top of RxFIFO will not be dropped. When RDES0.OWN is 0, ETH_DMASTS.RU bit will be set and RxDMA controller is still suspended.

25.4.8.4.4 Get receive descriptor

DMA will attempt to acquire a receive descriptor whenever any of the following conditions are met:

- ETH_DMAOPMOD.SR changes from 0 to 1, when DMA controller enters the running state

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- Before EOF is received, the buffer of current descriptor is full, and the entire buffer of current descriptor is not large enough to receive the entire frame
- A complete frame is received and forwarded to receive buffer, but current descriptor has not been closed
- A new frame is received when DMA is suspended without occupying the descriptor
- Perform any write operation to ETH_DMARXPD register

25.4.8.4.5 RxDMA operation flow

The operation flow of RxDMA is as follows:

1. Initialize DMA receive descriptor and set RDES0.OWN to 1;
2. Set ETH_DMAOPMOD.SR bit to 1 to enable RxDMA controller. After DMA enters running state, receive descriptor is obtained from the base address of the descriptor list configured by ETH_DMARXDLADDR register. If RDES0.OWN is 1, the current descriptor starts to receive frames; if RDES0.OWN is 0, DMA enters suspended state and skips to step 9;
3. If the obtained descriptor shows that the descriptor is occupied DMA (RDES0.OWN = 1), then the control bit and cache address of the descriptor will be parsed and recorded by DMA;
4. Process the received frame and transfer the data from RxFIFO to receive buffer;
5. If frame transfer is complete or buffer is full, receiving controller will get next receive descriptor from descriptor queue;
6. If current frame transfer ends, DMA operation skips to step 7. If current frame transmission does not end (end of frame EOF is not received), two things can happen:
   a) If RDES0.OWN of next descriptor is 0 and receive frame clearing function is not enabled, RxDMA controller sets RDES0.DE (descriptor error bit). RxDMA controller clears RDES0.OWN of the current descriptor to close the descriptor, if frame clearing function is not enabled, sets RDES0.LS, otherwise does not set RDES0.LS, and then skips to step 8.
   b) If RDES0.OWN of next descriptor is 1, RxDMA clears RDES0.OWN to close current descriptor, and then returns to step 4.
7. If IEEE 1588 timestamp function is enabled, and received frame meets the conditions of the frame that needs to record the timestamp, DMA controller will write the low and high bits of the acquired timestamp into RDES2 and RDES3 of current descriptor after receiving the frame. At the same time, DMA writes the received status information returned from MAC into RDES0, clears RDES0.OWN to 0, and sets RDES0.LS to 1;
8. If RDES0.OWN of newly acquired descriptor is 1, RxDMA controller operates jumping step 4; if RDES0.OWN is 0, received frame will be cleared first (provided that the receive frame clearing function is enabled), and then RxDMA controller enters suspend state and sets ETH_DMASTS.RU (receive buffer unavailable) to 1;
9. When any write operation is performed to ETH_DMARXPD register or RxFIFO receives the next frame of data, the suspend state can be exited. When DMA exits suspended state, DMA operation jumps to step 2 and attempts to re-acquire next descriptor.

25.4.8.5 MAC initialization using DMA

The MAC initialization process using DMA controller is as follows:

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1. Set ETH_DMABUSMOD register bus access related parameters.
2. Set ETH_DMAINTEN register to mask unnecessary interrupt sources.
3. First write the base address of the transmit descriptor list into ETH_DMATXDLADDR register, and then write the base address of the receive descriptor list into ETH_DMARXDLADDR register.
4. Configure the relevant filter registers as required.
5. Set the values of ETH_MACCFG.FES and ETH_MACCFG.DM according to the register result read from the external PHY, and select half-duplex or full-duplex communication mode and the communication speed of 10Mbps or 100Mbps. Set ETH_MACCFG.TE and ETH_MACCFG.RE to 1 to enable the transmit engine and receive engine of MAC.
6. Set ETH_DMAOPMOD.ST and ETH_DMAOPMOD.SR to 1 to enable TxDMA and RxDMA.

Note: If the HCLK frequency configuration is too low, RxFIFO may overflow at startup. It is recommended to enable RxDMA first, and then set ETH_MACCFG.RE to 1.

25.4.8.6 Arbiter for TxDMA and RxDMA

DMA arbiter can improve the efficiency of DMA controller through fixed and polling priority arbitration methods. When ETH_DMABUSMOD.DA is set to 0, the polling priority arbitration method is adopted. If TxDMA and RxDMA request to access the data bus at the same time, the access priority between TxDMA and RxDMA can be configured by setting these bits of ETH_DMABUSMOD.PR[1:0] level ratio. When ETH_DMABUSMOD.DA is set to 1, a fixed priority is selected. If TxDMA and RxDMA request to access the data bus at the same time, in this arbitration mode, RxDMA has a higher access priority to the bus.

25.4.8.7 Error response to DMA

If DMA has a wrong bus response during the transfer, DMA controller will treat it as a fatal error, stop all operations immediately, and update the status register ETH_DMASTS. Once this happens, Ethernet peripheral must be reset and DMA reinitialized before DMA can resume normal operation.

25.4.9 Precision Time Protocol (PTP)

MAC's Precision Time Protocol (PTP) module mainly supports recording the exact time when PTP packets are sent and received from the Ethernet port, and returns it to the application. Much of the protocol is implemented by application software on top of the UDP layer.

For details on Precision Time Protocol (PTP), please refer to the IEEE 1588™ related documentation.

25.4.9.1 Reference clock source

In IEEE 1588 protocol standard, the upper 32 bits of the 64-bit system reference time are second-level time information, and the lower 32 bits are nanosecond-level time information.

PTP reference clock input is used to generate the system reference time (referred to as the system time) and obtain the timestamp value of PTP frame. PTP reference clock frequency cannot be less than the resolution of the timestamp counter, and the time synchronization accuracy between the master node and the slave node is about 0.1us.

25.4.9.2 Synchronization accuracy

The accuracy of time synchronization depends on the frequency of PTP reference clock input and the frequency drift

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characteristics of the crystal oscillator used, as well as how often the synchronization process is performed.

25.4.9.3 System time calibration method

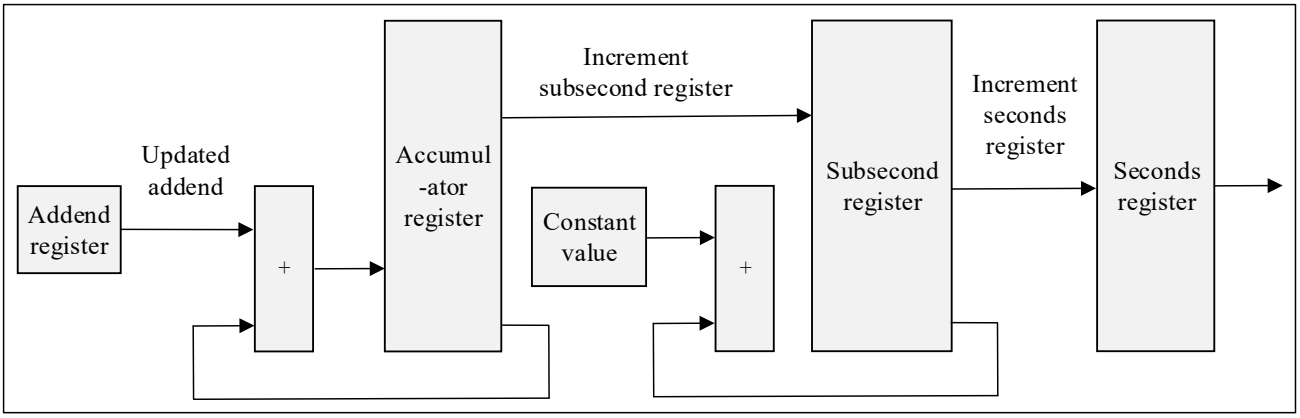
The 64-bit PTP system time is used as the basis for recording send/receive timestamps, and is updated by PTP input reference clock. In order to correct the frequency offset, PTP system time needs to be calibrated, and the initialization and calibration support two modes of coarse adjustment and fine adjustment.

Rough Adjustment Calibration Perform system time initialization and calibration by configuring the PTP timestamp update registers (ETH_PTPSECUP and ETH_PTPNSUP). If ETH_PTPTSCTRL.TSINIT is set, the PTP timestamp update register is used for initialization; if ETH_PTPTSCTRL.TSUPDT is set, the system time plus or minus the value of PTP timestamp update register is used to adjust the system time.

Fine-tuning calibration is to add the value in the addend register ETH_PTPTSADD to the accumulator every HCLK cycle. A pulse is generated when the accumulator overflows, causing the value of the timestamp low register ETH_PTPSS to increment according to the value of the subsecond increment register ETH_PTPSSINC. This process needs to wait for a period of time to complete, to ensure that the slave clock can be linearly synchronized with the master clock to avoid large jitter.

The following diagram illustrates the flow of the fine-tuning algorithm:

Figure 25-9 System time precision calibration



The following example illustrates the configuration method of updating system time in fine adjustment mode:

Set the initial value of the addend register (Clock_Addend_Value(0)) to the slave clock, the initial value is calculated in the following way: The accuracy of the system clock update circuit needs to reach 20ns (the update frequency is 50MHz). When the reference clock HCLK is 70MHz, the frequency ratio is 70/50 = 1.4, the addend that should be written into the ETH_PTPTSADD register is $2^{32}/1.4$ = 0xB6DB 6DB6; when the frequency drift of the reference clock is reduced to 60MHz, the frequency ratio becomes 60/50 = 1.2, and the addend written to the addend register is the value should be $2^{32}/1.2$ = 0xD555 5555; when the base clock frequency drift increases to 80MHz, the frequency ratio becomes 80/50 = 1.6, and the value written to the addend register should be $2^{32}/1.6$ = 0xA000 0000. After configuring the up-counter, it is necessary to configure the sub-second increment register to ensure the accuracy of 20ns. The value of the subsecond increment register updates the timestamp low register each time the accumulation register overflows. Since bits 0 to 30 of the timestamp low register represent the sub-second value of the system time, the precision is equal to 10^9ns/2^{31} = 0.46ns. In order to achieve a system time accuracy of 20ns, the value of the sub-second increment register should be set to 20/0.46 = 43.

Assuming that the delay Master_to_Slave_Delay transmitted between the master and slave devices is a fixed value, the time when the master device sends a SYNC message to the slave device is MSYNCT(n), the local time of the

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slave device is SLOCALT(n), and the local time of the master device is MLOCALT(n), the master clock count between two SYNC messages is MCLOCKC(n), the slave clock count between two SYNC messages is SCLOCKC(n), and the slave clock frequency adjustment factor is SCFAF(n)), the clock addend value of the addend register is Clock_Addend_Value(n), then the calculation method to determine the synchronization frequency in multiple SYNC cycles is as follows, but note that multiple SYNC messages may be required to complete the synchronization of the master and slave devices according to the situation:

MLOCALT(n) = MSYNCT(n) + Master_to_Slave_Delay(n)

MCLOCKC(n) = MLOCALT(n) - MLOCALT(n-1)

SCLOCKC(n) = SLOCALT (n) - SLOCALT(n-1)

SCFAF(n) = (MCLOCKC(n) + MCLOCKC(n) - SCLOCKC(n)) / SCLOCKC(n)

Clock_Addend_Value(n) = SCFAF(n) * Clock_Addend_Value(n-1)

25.4.9.4 System time initialization process

Timestamp function needs to configure ETH_PTPTSCTRL.TSENA to 1 first, and then initialize timestamp counter as follows to start timestamp operation:

1. Set ETH_MACINTMSK.TSIM to 1 to mask timestamp trigger interrupt;
2. Set ETH_PTPTSCTRL.TSENA to 1 to enable timestamp;
3. Set sub-second increment register to configure clock precision;
4. If choose coarse adjustment and calibration, skip directly to step 7; if choose fine adjustment and calibration, first configure timestamp adder register ETH_PTPTSADD, and then set ETH_PTPTSCTRL.TSADDREG to enable the update of timestamp adder register;
5. Query and wait for ETH_PTPTSCTRL.TSADDREG to become 0;
6. Set ETH_PTPTSCTRL.TSCFUPDT to 1, and update system timestamp with fine adjustment and calibration;
7. Set timestamp update high register and timestamp update low register to configure system time value;
8. Set ETH_PTPTSCTRL.TSINIT to 1, initialize system time, replace original system time with the value of timestamp high and low update registers, and timestamp counter starts to work.

25.4.9.5 Steps to update system time with coarse adjustment

1. Set offset value to timestamp update high register and timestamp update low register, the value can be negative;
2. Set ETH_PTPTSCTRL.TSUPDT to 1, enable updating system time, and add the offset values of timestamp high and low update registers to the original system time;
3. Wait for ETH_PTPTSCTRL.TSUPDT bit to be cleared.

25.4.9.6 Steps to update system time with fine adjustment

1. Calculate the value of the addend register corresponding to the desired system clock frequency according to the introduction of the "System time calibration method" above;
2. Write the value to upcounter, and set ETH_PTPTSCTRL.TSADDREG to 1, and update the value to PTP module;
3. Write the desired time into the timestamp update high register and timestamp update low register, and set ETH_MACINTMSK.TSIM to 0 to allow timestamp interrupts;

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4. Set ETH_PTPTSCTRL.TSTRIG to 1 to enable timestamp interrupt;
5. When timestamp interrupt occurs, read the value of ETH_MACINTSTS register and clear the corresponding interrupt flag bit;
6. Write the original value into the timestamp addend register, then set ETH_PTPTSCTRL.TSADDREG to 1, and update the value to PTP module.

25.4.9.7 Transmission and receive of frames with PTP function

If IEEE 1588 (PTP) timestamp function is enabled, when MAC outputs the SFD of the transmitted frame or receives the SFD of the received frame, the 64-bit timestamp value will be recorded, and stored together with the frame's transmit/receive status information. To the corresponding transmit/receive descriptor, "TxDMA descriptor" and "RxDMA descriptor" are described in detail.

25.4.9.8 PTP pulse-per-second output signal (PPS)

After ETH module is enabled, PPS output function is automatically turned on, and it is output to PB5/PB6 in different pin reset methods. The default clock cycle of the output pulse is 18M/HCLK (when the HCLK is 144M, the pulse width is 125ms). The function can check whether all nodes in the network are synchronized. Connect the PPS outputs of both the master and slave devices to an oscilloscope to test the difference between the local slave clock and the master clock.

25.4.10 Typical Ethernet Configuration Flow Xxample

After a power-on reset or system reset, the recommended configuration and startup process for Ethernet module is as follows:

1. Configure RCC module, enable HCLK clock and Ethernet transmit/receive clock;
2. Configure AFIO_RMP_CFG to select MII or RMII connection mode, and map corresponding function pins to alternate functions;
3. Poll ETH_DMABUSMOD register until ETH_DMABUSMOD.SWR bit is reset after reset is completed;
4. Get and configure PHY register parameters:

   According to the HCLK frequency, configure SMI clock frequency, communicate with the external PHY and access the corresponding registers, confirm whether the external PHY supports half/full duplex working mode, 10Mbps/100Mbps communication speed, etc., and configure the information of the external PHY register to the ETH_MACCFG register.
5. Initialize Ethernet DMA module:

   Configure ETH_DMABUSMOD, ETH_DMARXDLADDR, ETH_DMATXDLADDR, ETH_DMAOPMOD registers to initialize DMA module for data transfer.
6. Initialize physical memory space for storing descriptor list and data cache:

   Based on the addresses in ETH_DMARXDLADDR and ETH_DMATXDLADDR registers, DMA is initialized to hold transmit and receive descriptors (TDES0.OWN = 0 or RDES0.OWN = 1) and data buffers.
7. Enable the MAC and DMA modules to start data transfer:

   Start MAC transmitter and receiver by setting ETH_MACCFG.TE and ETH_MACCFG.RE to 1, and enable

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DMA transmission and reception by setting ETH_DMAOPMOD.ST and ETH_DMAOPMOD.SR to 1.

8. When transmit frame data:
   a) Select one or more transmit descriptors, write the transmit frame data to the buffer address specified in the transmit descriptor, and set TDES0.OWN in transmit descriptor to make DMA occupy descriptor;
   b) Write any value into ETH_DMATXPD register to make TxDMA exit the suspend mode and start sending data;
   c) It is possible to confirm whether the transmission of current frame is completed by polling TDES0.OWN of current descriptor until it is reset or polling ETH_DMASTS.TI until it is set (only applicable when TDES1.IC is 1).
9. When receive frame data:
   a) View first receive descriptor in descriptor list (the address of descriptor can be obtained through the ETH_DMARXDLADDR register);
   b) Query RDES0.OWN, if it is reset, it means that descriptor has been used, and receive buffer has stored received frame;
   c) Process received frame data in buffer;
   d) Set RDES0.OWN of current descriptor to receive a new frame by alternate current descriptor;
   e) To view next descriptor in list, skip to step b.

25.4.11 Ethernet Interrupt

Ethernet module has 2 interrupt vectors for Ethernet wake-up events (detecting remote wake-up frames or Magic Packet wake-up frames) mapped to EXTI line 19 and Ethernet normal operation.

The interrupt vector mapped to the Ethernet wake-up event is used for the interrupt generated by PMT module during the wake-up event. The wake-up event is a remote wake-up frame reception event or a Magic Packet wake-up frame reception event. The wake-up event is mapped to EXTI line 19, and if the rising edge interrupt on EXTI line 19 is enabled, the wake-up event can cause MCU to exit low-power mode. If PMT interrupt is also enabled, both the EXTI line 19 interrupt and the Ethernet interrupt are triggered.

Note: Since PMT register is located in Rx_CLK domain, there may be a delay caused by the difference between the HCLK and Rx_CLK clock frequencies from the time the application reads PMT register until these flags are cleared. To avoid entering the same interrupt twice, it is strongly recommended that the application program Wait for ETH_MACPMTCTRLSTS.RWKPRCVD and ETH_MACPMTCTRLSTS.MGKPRCVD to become 0 in the interrupt, and then exit the interrupt service routine.

Interrupt vectors mapped to normal Ethernet operation are used for interrupts generated by MAC and Ethernet DMA, as described below.

25.4.11.1.1 MAC interrupts

MAC controller has multiple interrupt trigger sources. ETH_MACINTSTS register describes all types of MAC interrupts that can be generated, and each bit has its own interrupt mask bit to prevent an event from triggering an interrupt. As long as one of MAC interrupts occurs, MAC interrupt signal will be generated.

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25.4.11.1.2 Ethernet DMA interrupts

DMA controller has two types of interrupt events, normal and abnormal, and has a corresponding interrupt enable bit to control whether an interrupt is generated. When the interrupt enable bit is cleared, or all interrupt events are cleared, the corresponding interrupt summary bit is also cleared. When both normal class and exception class interrupts are cleared, DMA interrupts are also cleared.

25.5 ETH Rregister

The registers of this peripheral can be accessed in the form of bytes (8 bits), halfwords (16 bits) and words (32 bits).

25.5.1 ETH Register Overview

Table 25-10 ETH register overview

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
000h	ETH_MACCFG	Reserved								WD	JD	Reserved		IFG[2:0]			DCRS	Reserved	FES	DO	LM	DM	IPC	DR	Reserved	ACS	BL[1:0]		DC	TE	RE	Reserved	
	Reset Value									0	0			0	0	0	0		0	0	0	0	0	0		0	0	0	0	0	0		
004h	ETH_MACFFLT	RA	Reserved																				HPF	SAF	SAIF	PCF[1:0]		DBF	PAM	DAIF	HMC	HUC	PRM
	Reset Value	0																					0	0	0	0	0	0	0	0	0	0	0
008h	ETH_MACHASHHI	HTH[31:0]																															
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
00Ch	ETH_MACHASHLO	HTL[31:0]																															
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
010h	ETH_MACMIIADDR	Reserved																PA[4:0]					MR[4:0]					Reserved	CR[2:0]			MW	MB
	Reset Value																	0	0	0	0	0	0	0	0	0	0		0	0	0	0	0
014h	ETH_MACMIIDAT	Reserved																MD[15:0]															
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
018h	ETH_MACFLWCTRL	PT[15:0]																Reserved								DZQP	Reserved	PLT[1:0]		UP	RFE	TFE	FCB_BPA
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0									0		0	0	0	0	0	0
01Ch	ETH_MACVLANTAG	Reserved															ETC	VLTI[15:0]															
	Reset Value																0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
028h	ETH_MACRMTWUFRMFLT	DAT[31:0]																															
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
02Ch	ETH_MACPMTCTRLSTS	RWKUPFLTRST	Reserved																					GLBLUCAST	Reserved	RWKPRCVD	MGKPRCVD	Reserved			RWKPKTEN	MGKPKTEN	PWRDWN
	Reset Value	0																						0		0	0				0	0	0
038h	ETH_MACINTSTS	Reserved																						TSTS	Reserved	MMCTXIS	MMCRXIS	MMCIS	PMTIS	Reserved			
	Reset Value																							0		0	0	0	0				

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03Ch	ETH_MACINTMSK	Reserved																						TSIM	Reserved					PMTIM	Reserved		
	Reset Value																							0						0			
040h	ETH_MACADDR0HI	Reserved																ADDRHI[15:0]															
	Reset Value																	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
044h	ETH_MACADDR0LO	ADDRLO[31:0]																															
	Reset Value	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
048h	ETH_MACADDR1HI	AE	SA	MBC[5:0]						Reserved								ADDRHI[15:0]															
	Reset Value	0	0	0	0	0	0	0	0									1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
04Ch	ETH_MACADDR1LO	ADDRLO[31:0]																															
	Reset Value	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
050h	ETH_MACADDR2HI	AE	SA	MBC[5:0]						Reserved								ADDRHI[15:0]															
	Reset Value	0	0	0	0	0	0	0	0									1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
054h	ETH_MACADDR2LO	ADDRLO[31:0]																															
	Reset Value	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
058h	ETH_MACADDR3HI	AE	SA	MBC[5:0]						Reserved								ADDRHI[15:0]															
	Reset Value	0	0	0	0	0	0	0	0									1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
05Ch	ETH_MACADDR3LO	ADDRLO[31:0]																															
	Reset Value	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
100h	ETH_MMCCTRL	Reserved																												CNTFREEZ	RSTONRD	CNTSTOPRO	CNTRST
	Reset Value																													0	0	0	0
104h	ETH_MMCRXINT	Reserved														RXUCGFIS	Reserved													RXALIGNERFIS	RXCRCERFIS	Reserved	
	Reset Value															0														0	0		
108h	ETH_MMCTXINT	Reserved										TXGFRMIS	Reserved					TXMCOLGFIS	TXSCOLGFIS	Reserved													
	Reset Value											0						0	0														
10Ch	ETH_MMCRXINTMSK	Reserved														RXUCGFIM	Reserved													RXALIGNERFIM	RXCRCERFIM	Reserved	
	Reset Value															0														0	0		
110h	ETH_MMCTXINTMSK	Reserved										TXGFRMIM	Reserved					TXMCOLGFIM	TXSCOLGFIM	Reserved													
	Reset Value											0						0	0														
14Ch	ETH_MMCTXGFASCCNT	CNT[31:0]																															
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
150h	ETH_MMCTXGFAMSCCNT	CNT[31:0]																															
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
168h	ETH_MMCTXGFCNT	CNT[31:0]																															
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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194h	ETH_MMCRXFCECNT	CNT[31:0]																															
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
198h	ETH_MMCRXFAECNT	CNT[31:0]																															
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1C4h	ETH_MMCRXGUFCNT	CNT[31:0]																															
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
700h	ETH_PTPTSCTRL	Reserved																										TSADDREG	TSTRIG	TSUPDT	TSINIT	TSCFUPDT	TSENA
	Reset Value																											0	0	0	0	0	0
704h	ETH_PTPSSINC	Reserved																								SSINC[7:0]							
	Reset Value																									0	0	0	0	0	0	0	0
708h	ETH_PTPSEC	TSS[31:0]																															
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
70Ch	ETH_PTPNS	PN	TSSS[30:0]																														
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
710h	ETH_PTPSECUP	TSS[31:0]																															
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
714h	ETH_PTPNSUP	ADDSUB	TSSS[30:0]																														
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
718h	ETH_PTPTSADD	TSA[31:0]																															
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
71Ch	ETH_PTPTTSEC	TTS[31:0]																															
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
720h	ETH_PTPTTNS	TTSLO[31:0]																															
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1000h	ETH_DMABUSMOD	Reserved						AALB	PBLX8	USP	RPBL[5:0]						FB	PR[1:0]		PBL[5:0]					Reserved	DSL[4:0]					DA	SWR
	Reset Value							0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	1	Reserved	0	0	0	0	0	0	1
1004h	ETH_DMATXPD	TPD[31:0]																															
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1008h	ETH_DMARXPD	RPD[31:0]																															
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
100Ch	ETH_DMARXDLADDR	SRL[31:0]																															
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1010h	ETH_DMATXDLADDR	STL[31:0]																															
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1014h	ETH_DMASTS	Reserved		TTI	PMTI	MMCI	Reserved	EB[2:0]			TPS[2:0]			RPS[2:0]			NIS	AIS	ERI	FBI	Reserved			ETI	RWT	RPSS	RU	RI	UNF	OVF	TJT	TU	TPSS	TI
	Reset Value		0	0	0		0	0	0	0	0	0	0	0	0	0	0	0	0	0				0	0	0	0	0	0	0	0	0	0	0
1018h	ETH_DMAOPMOD	Reserved					DT	RSF	DFF	Reserved		TSF	FTF	Reserved			TTC[2:0]			ST	Reserved						FEF	FUF	Reserved	RTC[1:0]		OSF	SR	Reserved
	Reset Value						0	0	0			0	0				0	0	0	0							0	0		0	0	0	0	
101Ch	ETH_DMAINTEN	Reserved															NISE	AISE	ERIE	FBIE	Reserved			ETIE	RWTE	RPSE	RUE	RIE	UNFE	OVFE	TJTE	TUE	TPSE	TIE
	Reset Value																0	0	0	0				0	0	0	0	0	0	0	0	0	0	0

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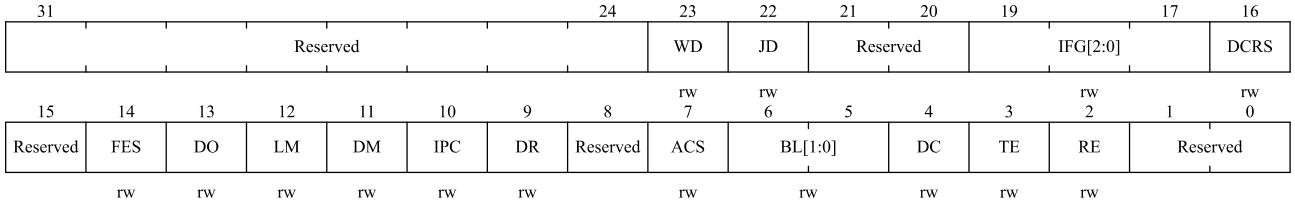
1020h	ETH_DMAMFBOCNT	Reserved			OVFCNTOVF	OVFFRMCNT[10:0]											MISCNTOVF	MISFRMCNT[15:0]															
	Reset Value				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1048h	ETH_DMACHTXDESC	ADDR[31:0]																															
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
104Ch	ETH_DMACHRXDESC	ADDR[31:0]																															
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1050h	ETH_DMACHTXBADDR	ADDR[31:0]																															
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1054h	ETH_DMACHRXBADDR	ADDR[31:0]																															
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

25.5.2 ETH MAC Configuration Register (ETH_MACCFG)

Address offset: 0x0000

Reset value: 0x0000 8000

MAC configuration register is the operating mode register of the MAC. It defines the working mode of receiving and sending.



Bit field	Name	Description
31:24	Reserved	Reserved, the reset value must be maintained.
23	WD	Disable watchdog. 0: Frames exceeding 2048 bytes are not allowed to be received, and data exceeding 2048 bytes will be truncated. 1: Turn off receive watchdog timer, and MAC can receive frames with a maximum length of 16383 bytes.
22	JD	Disable Jabber detection. 0: Allows transmit frames of up to 2048 bytes. 1: Disable Jabber timer, and MAC can transmit frames of up to 16383 bytes.
21:20	Reserved	Reserved, the reset value must be maintained.
19:17	IFG[2:0]	Frame gap selection. These bits are used to control the shortest gap between two transmitted frames. 000: 96-bit time 001: 88-bit time 010: 80-bit time ... 111: 40-bit time

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Bit field	Name	Description
		In half-duplex mode, these bits can be configured with a minimum interframe gap of 64-bit time.
16	DCRS	Disable carrier sense function. 0: MAC will report an error and terminate the transmission when the carrier signal is wrong. 1: In half-duplex mode, MAC will ignore the CRS signal of MII in the process of sending the frame, and no error will be reported if the carrier is lost or there is no carrier.
15	Reserved	Reserved, the reset value must be maintained.
14	FES	Ethernet speed selection. 0: 10Mbps 1: 100Mbps
13	DO	Disable self-receive function. This bit has no meaning in full duplex mode. 0: MAC receives all packets from the PHY when transmitting. 1: MAC does not receive frames in half-duplex mode.
12	LM	Loopback mode. 0: MAC works in normal mode. 1: MAC works in Loopback mode (receive clock Rx_CLK input is required).
11	DM	Duplex mode selection. 0: Half-duplex mode. 1: Full duplex mode.
10	IPC	IP frame checksum. 0: Disable TCP/UDP/ICMP header checksum check of receiver. 1: Enable checksum check function of receiver.
9	DR	Disable retry. This bit is only valid in half-duplex mode. 0: MAC will retransmit after a certain period of time according to the settings of these bits in ETH_MACCFG.BL[1:0] after a collision. 1: MAC will only attempt to send 1 time. If a collision occurs on MII, MAC will abort the transmission and report an excessive collision error in the transmit status message.
8	Reserved	Reserved, the reset value must be maintained.
7	ACS	Automatic PAD/CRC stripping. 0: MAC will forward all received frames without changing the content of the frame. 1: MAC will remove PAD field and CRC field of frames less than or equal to 1536 bytes, and frames exceeding 1536 bytes will be forwarded directly.
6:5	BL[1:0]	Back off limit. After a collision, MAC needs to delay for some time before retransmitting the current frame. The time base unit of this delay time (dt) is called a time slot, and a time slot is 512 bits of time. This delay time (dt) is a random integer value calculated by: $0 \le dt < 2^k$ 00：k = min(n, 10)

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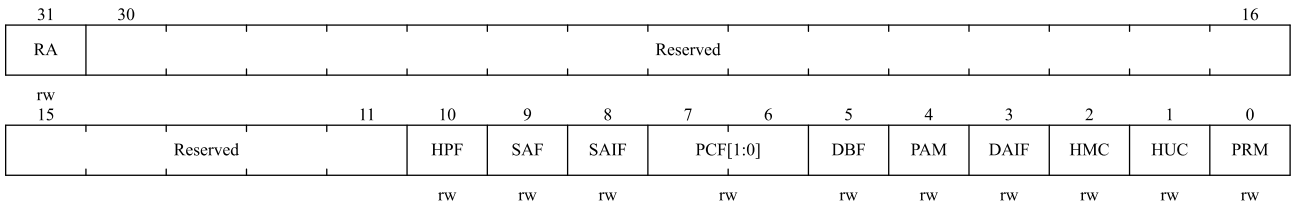
Bit field	Name	Description
		01：k = min(n, 8) 10：k = min(n, 4) 11：k = min(n, 1) Where: n = number of retransmissions. Note: These bits are only valid in half-duplex mode.
4	DC	Deferral inspection. This bit is only valid in half-duplex mode. 0: Disable MAC deferral check function. MAC will delay sending until the CRS signal is disabled. 1: MAC delay check function is enabled. If the delay exceeds the 24288 bit time, an excessive delay error occurs and MAC will abort the transmission. But if a valid CRS signal is detected within the delay time, the delay counter will be reset to 0 and the delay timing will be restarted.
3	TE	Enable transmitter. 0: MAC closes transmit state machine. If the current frame is being transmitted, it will be closed after transmitting is completed. 1: MAC enables transmit state machine.
2	RE	Enable receiver. 0: MAC closes receiving state machine. If the current frame is being received, it will be closed after receiving is completed. 1: MAC enables receive state machine.
1:0	Reserved	Reserved, the reset value must be maintained.

25.5.3 ETH MAC Frame filter Register (ETH_MACFFLT)

Address offset: 0x0004

Reset value: 0x0000 0000

MAC Frame Filter Register contains the filter control bits for received frames.



Bit field	Name	Description
31	RA	Receive all frames. This bit controls the frame filter function. 0: Only received frames that pass the address filter will be forwarded to the application. 1: All received frames will be forwarded to application, but the result of the filtering will be reflected in the corresponding flags in the updated receive descriptor status information.

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Bit field	Name	Description
30:11	Reserved	Reserved, the reset value must be maintained.
10	HPF	HASH or perfect filtering. 0: If ETH_MACFFLT.HMC or ETH_MACFFLT.HUC is set to 1, only frames that conform to the HASH filter can pass the receive address filter. 1: If ETH_MACFFLT.HMC or ETH_MACFFLT.HUC is set to 1, and the received frame passes either HASH filter or the perfect filter, it is considered that it has passed the receiving address filter.
9	SAF	Source address filter. Enables energy address filter in addition to destination address filter. The filter compares the value of the source address field of the received frame with the value configured in the enabled source address register. If the source address values match, the source address match status bit in the receive descriptor will be set. 0: Source address filter is off. 1: Source address filter is enabled.
8	SAIF	Invert source address filtering result. This bit inverts the source address comparison result. 0: Disable source address filter result inversion, all frames whose source address does not match the source address register will be marked as failing the source address filter. 1: Invert source address filter result, all frames whose source address matches the source address register will be marked as failing the source address filter.
7:6	PCF[1:0]	Control frame forwarding bit. These bits are used to set the forwarding conditions of all control frames (including unicast and multicast pause frames), and whether to process pause control frames depends only on the value of ETH_MACFLWCTRL.RFE. 00: MAC does not forward any control frames to the application. 01: MAC forwards control frames other than pause frames to the application. 10: MAC forwards all control frames to the application, even those that do not pass address filter. 11: MAC forwards control frames that pass address filter to the application.
5	DBF	Refuse to receive broadcast frames. 0: The filter receives all broadcast frames. 1: The filter does not receive all broadcast frames.
4	PAM	Pass all multicast frames. 0: Multicast frame filtering depends on the value of ETH_MACFFLT.HMC. 1: All frames with a multicast destination address (the first bit of the address is 1) can pass the filter.
3	DAIF	Invert destination address filtering result. This bit inverts the destination address filter result. 0: Disable destination address filtering result inversion. 1: Enable destination address filtering result inversion.
2	HMC	Multicast HASH filter. 0: MAC will compare the value of the destination address field of the received

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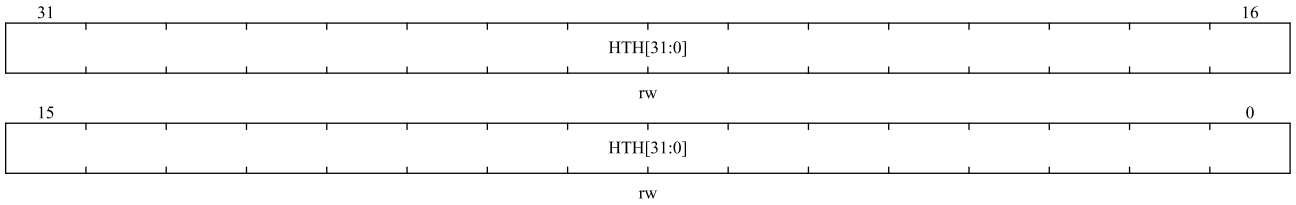
Bit field	Name	Description
		multicast frame with the set value of the destination address register. 1: MAC filters the destination address of the received multicast frame according to the HASH list.
1	HUC	Unicast HASH filter. 0: MAC will compare the value of the destination address field of the received unicast frame with the set value of the destination address register. 1: MAC filters the destination address of the received unicast frame according to the HASH list.
0	PRM	Promiscuous mode. This bit disables the address filter, which means that all frames pass the filter while the destination/source error bit of the status information in the receive descriptor is always 0. 0: Disable promiscuous mode. 1: Enable promiscuous mode.

25.5.4 ETH MAC HASH List High Register (ETH_MACHASHHI)

Address offset: 0x0008

Reset value: 0x0000 0000

A 64-bit HASH list can be used for group address filtering. This register contains the upper 32 bits of the multicast HASH list.



Bit field	Name	Description
31:0	HTH[31:0]	HASH list high. These bits are the upper 32 bits of the HASH list.

25.5.5 ETH MAC HASH List Low Register (ETH_MACHASHLO)

Address offset: 0x000C

Reset value: 0x0000 0000

A 64-bit HASH list can be used for group address filtering. This register contains the lower 32 bits of the multicast HASH list.

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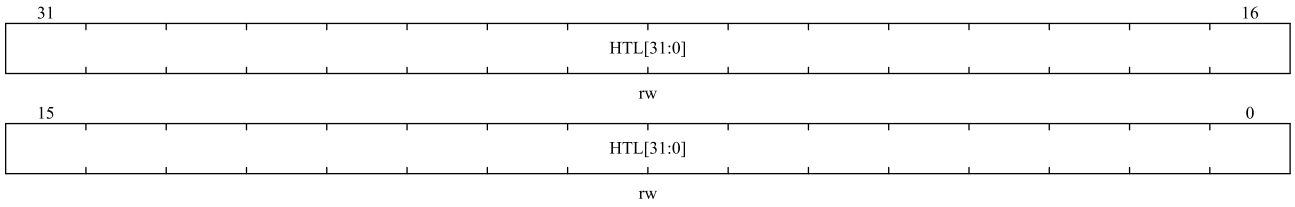


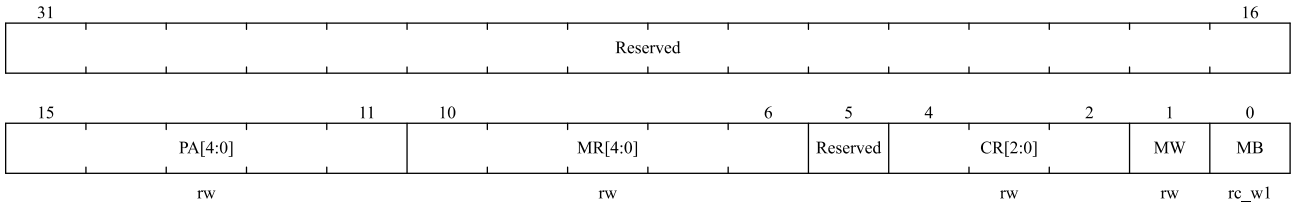
Bit field	Name	Description
31:0	HTL[31:0]	HASH list low. These bits are the lower 32 bits of the HASH list.

25.5.6 ETH MAC MII Address Register (ETH_MACMIIADDR)

Address offset: 0x0010

Reset value: 0x0000 0000

This register controls the management signals of the external PHY through the interface.



Bit field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained.
15:11	PA[4:0]	PHY address. These bits represent the accessed PHY address.
10:6	MR[4:0]	MII PHY registers. These bits select the PHY register to be accessed.
5	Reserved	Reserved, the reset value must be maintained.
4:2	CR[2:0]	Clock range. These bits are used to configure the clock of MDC according to the frequency of HCLK.
1	MW	MII write operation. 0: Read the PHY. 1: Write to PHY.
0	MB	MII busy. This bit should be 0 before writing to register ETH_MACMIIADDR and

value	MDC frequency	HCLK frequency
000	HCLK/42	60~100MHz
001	HCLK/62	100~144MHz
010	HCLK/16	20~35MHz
011	HCLK/26	35~60MHz
other	Reserved	Reserved

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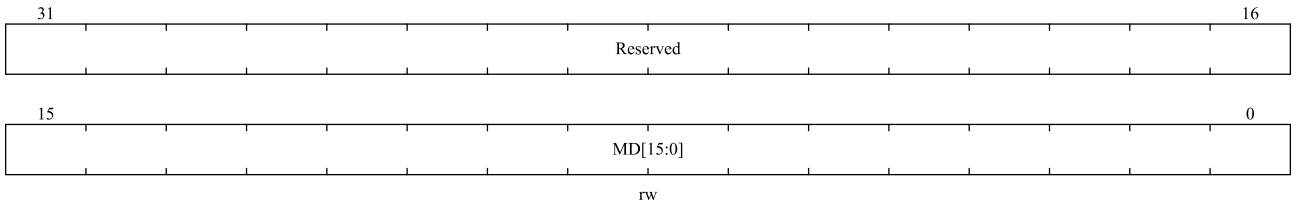
Bit field	Name	Description
		ETH_MACMIIDAT. When accessing the PHY, this bit is set by the application program to indicate that a read or write operation is being performed on the PHY. When writing to the PHY, the value of the ETH_MACMIIDAT register must be retained until this bit is cleared by hardware. When the PHY is read, the value of the ETH_MACMIIDAT register is valid after the hardware clears this bit.

25.5.7 ETH MAC MII Data Register (ETH_MACMIIDAT)

Address offset: 0x0014

Reset value: 0x0000 0000

This register holds the value to be written to or read from PHY register.



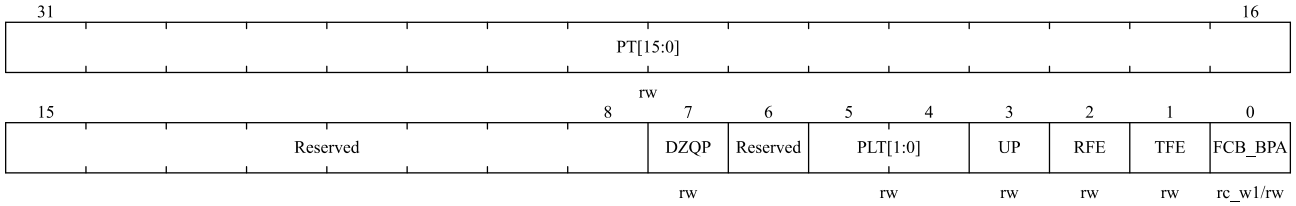
Bit field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained.
15:0	MD[15:0]	MII data. These bits contain the 16-bit data read out after a read operation on PHY. Or the 16-bit data to be written before writing to PHY.

25.5.8 ETH MAC Flow Control Register (ETH_MACFLWCTRL)

Address offset: 0x0018

Reset value: 0x0000 0000

This register is used for the generation and reception of configuration control (PAUSE) frames.



Bit field	Name	Description
31:16	PT[15:0]	PAUSE time. The value of these bits is used as the value of the PAUSE time field of the control frame. If the PAUSE time is set to be synchronized to MII clock domain twice, there must be at least 4 destination domain clock cycles between consecutive writes to the register.

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Bit field	Name	Description
15:8	Reserved	Reserved, the reset value must be maintained.
7	DZQP	Disable zero-value PAUSE function. 0: Normal operation, turning on the automatic generation of zero-value PAUSE control frames. 1: When the FIFO layer flow control signal is withdrawn, the automatic generation of the automatic zero-valued PAUSE control frame is turned off.
6	Reserved	Reserved, the reset value must be maintained.
5:4	PLT[1:0]	PAUSE low threshold. These bits set the timer threshold for automatic retransmission of PAUSE frames. This threshold should be greater than 0 and less than the pause time defined by these bits in ETH_MACFLWCTRL.PT[15:0]. The low threshold is calculated as PT - PLT. For example, PT = 0x80 (128 time slots), PLT = 0x1 (28 time slots), then the second PAUSE frame will be automatically retransmit 100 (128-28) time slots after the first PAUSE frame is transmitted. 00: Pause time - 4 time slots 01: Pause time - 28 time slots 10: Pause time - 144 time slots 11: Pause time - 256 time slots *Note: A time gap refers to the time it takes for the MII interface to send 512 bits (64 bytes) of data.*
3	UP	Unicast PAUSE frame detection. 0: MAC only receives PAUSE frames that conform to the unique multicast address defined by the IEEE802.3 specification. 1: In addition to PAUSE frames with unique multicast addresses, MAC also uses the MAC address 0 to detect PAUSE frames.
2	RFE	Receive flow control enable bit. When this bit is set to 1, MAC will turn off the transmitter for the specified time (the value of the Pause Time field in the received frame). 0: MAC does not parse PAUSE frames. 1: MAC parses and processes the received PAUSE frame.
1	TFE	Transmit flow control enable bit. In full-duplex mode, this bit is 1 to indicate that MAC can transmit PAUSE frames, and this bit is cleared to 0 to indicate that PAUSE frames are not transmitted. In half-duplex mode, this bit is 1 to indicate that MAC enables the back pressure function, and this bit is cleared to 0 to indicate that the back pressure function is turned off. 0: MAC disables transmit flow control function. 1: MAC enables transmit flow control function.
0	FCB_BPA	Flow control busy/back pressure active. In full-duplex mode, this bit can transmit PAUSE frames; in half-duplex mode, when ETH_MACFLWCTRL.TFE is set, this bit can activate the back pressure function. In full-duplex mode, the application should ensure that this bit is 0 before writing to the ETH_MACFLWCTRL register. After this bit is set to 1, MAC will transmit a

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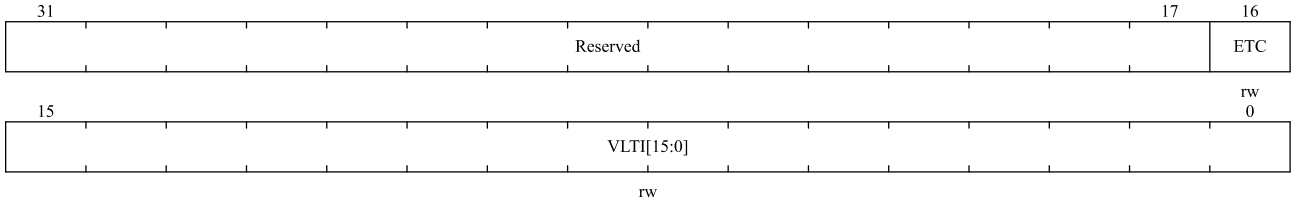
Bit field	Name	Description
		PAUSE frame to the interface. During the process of transmit the control frame, the bit is always 1, and MAC resets this bit to 0 after the PAUSE control frame is transmitted. In half-duplex mode, setting this bit to 1 activates the backpressure function. When the backpressure function is valid, if MAC receives a new frame, it will transmit a blocking signal at the sender to notify that there is a conflict. The back pressure function is automatically disabled in full duplex mode.

25.5.9 ETH MAC VLAN Tag Register (ETH_MACVLANTAG)

Address offset: 0x001C

Reset value: 0x0000 0000

This register contains the IEEE802.1Q VLAN tag used to identify VLAN frames. MAC compares the 13th and 14th bytes (length/type fields) of the received frame with 0x8100, and then compares the next 2 bytes (15th and 16th bytes) with the VLAN tag.



Bit field	Name	Description
31:17	Reserved	Reserved, the reset value must be maintained.
16	ETC	12-bit VLAN tag comparison bits. This bit selects VLAN tag to be compared with ETH_MACVLANTAG.VLTI[11:0] (12 bits) or ETH_MACVLANTAG.VLTI[15:0] (16 bits). 0: Use all 16-bit data for comparison. 1: Use only 12-bit data for comparison.
15:0	VLTI[15:0]	VLAN tag identifier bits. These bits are used to identify the 802.1Q VLAN tag format of VLAN frame. The format is as follows: VLTI[15:13]: UP (user priority) VLTI[12]: CFI (Standard Format Indicator) VLTI[11:0]: VID (VLAN identifier) Define VLTI[n:0], when ETH_MACVLANTAG.ETC = 1, n = 11; when ETH_MACVLANTAG.ETC = 0, n = 15. If the value of VLTI[n:0] is all 0, MAC will no longer compare and check the 15th and 16th bytes of VLAN frame, and will directly regard the frame with the type field value of the received frame as 0x8100 as a VLAN frame. If VLTI[n:0] is not all 0, use VLTI[n:0] for comparison.

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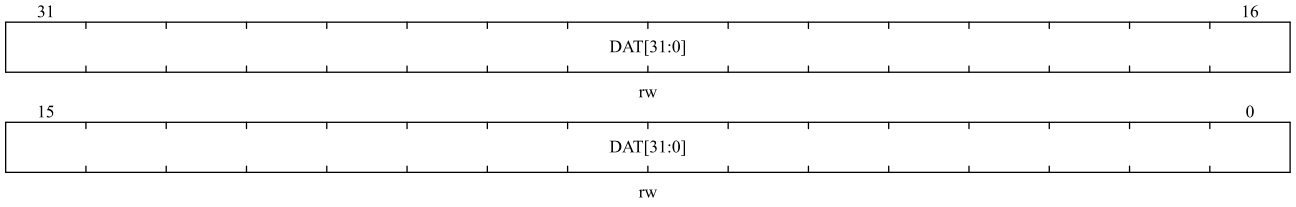
25.5.10 ETH MAC Remote Wakeup Frame Filter Register (ETH_MACRMTWUFRMFLT)

Address offset: 0x0028

Reset value: 0x0000 0000

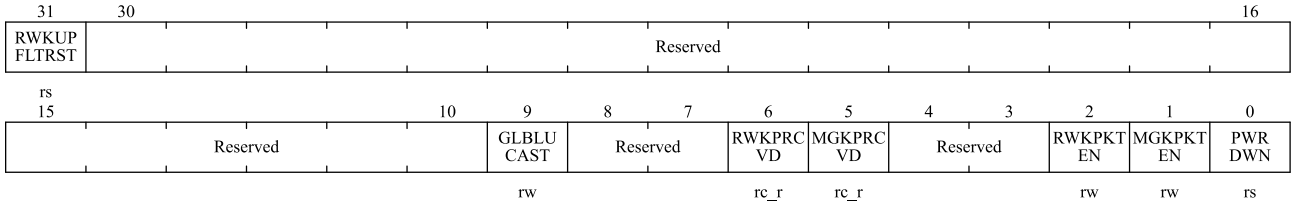


This register is essentially a pointer to 8 opaque wakeup frame filter registers (using the same offset). 8 consecutive write operations to this register address (offset 0x0028) can write all 8 wake-up frame filter registers; 8 consecutive read operations to this register address (offset 0x0028) can read all 8 wake-up frame filter registers. Refer to Table 25-7 Remote wakeup frame filter register overview.

25.5.11 ETH MAC PMT Control and Status Register (ETH_MACPMTCTRLSTS)

Address offset: 0x002C

Reset value: 0x0000 0000



Bit field	Name	Description
31	RWKUPFLTRST	Remote wakeup frame filter register pointer reset. 0: No effect. 1: Reset ETH_MACRMTWUFRMFLT register pointer, which is automatically cleared to 0 after the pointer reset is completed.
30:10	Reserved	Reserved, the reset value must be maintained.
9	GLBLUCAST	Global unicast. 0: Not all received unicast frames are considered wakeup frames. 1: All unicast frames that can pass MAC address filter are considered as wake-up frames.
8:7	Reserved	Reserved, the reset value must be maintained.
6	RWKPRCVD	Remote wakeup frame received. This bit is cleared to 0 by reading this register.

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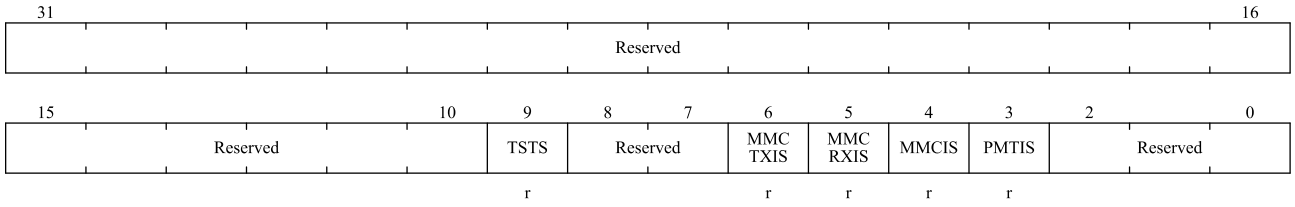
Bit field	Name	Description
		0: No remote wakeup frame was received. 1: A remote wakeup frame is received and a wakeup event occurs.
5	MGKPRCVD	Magic Packet received. This bit is cleared to 0 by reading this register. 0: No Magic Packet wakeup frame was received. 1: A Magic Packet wakeup frame is received and a wakeup event occurs.
4:3	Reserved	Reserved, the reset value must be maintained.
2	RWKPKTEN	Remote wake-up frame enable bit. 0: Disables to generate wakeup event when remote wakeup frame is received. 1: Enable to generate wakeup event when remote wakeup frame is received.
1	MGKPKTEN	Magic Packet enable bit. 0: Disable to generate wakeup event when Magic Packet wakeup frame is received. 1: Enable to generate wakeup event when Magic Packet wakeup frame is received.
0	PWRDWN	Low power bit. This bit is set by software and reset by hardware. When this bit is set, MAC discards all received frames. When a wakeup event occurs and the low-power mode is exited, the hardware will automatically clear this bit to 0. This bit can only be set when ETH_MACPMTCTRLSTS.RWKPKTEN or ETH_MACPMTCTRLSTS.MGKPKTEN is 1.

25.5.12 ETH MAC Interrupt Status Register (ETH_MACINTSTS)

Address offset: 0x0038

Reset value: 0x0000 0000



Bit field	Name	Description
31:10	Reserved	Reserved, the reset value must be maintained.
9	TSTS	Timestamp trigger state. This bit is cleared to 0 by reading this register. 0: System time value is less than the expected time value. 1: System time value is equal to or exceeds the expected time value.
8:7	Reserved	Reserved, the reset value must be maintained.
6	MMCTXIS	MMC sends status. 0: All bits in ETH_MMCTXINT register are 0. 1: Any interrupt bit in ETH_MMCTXINT register is 1.
5	MMCRXIS	MMC receive status. 0: All bits in ETH_MMCRXINT register are 0.

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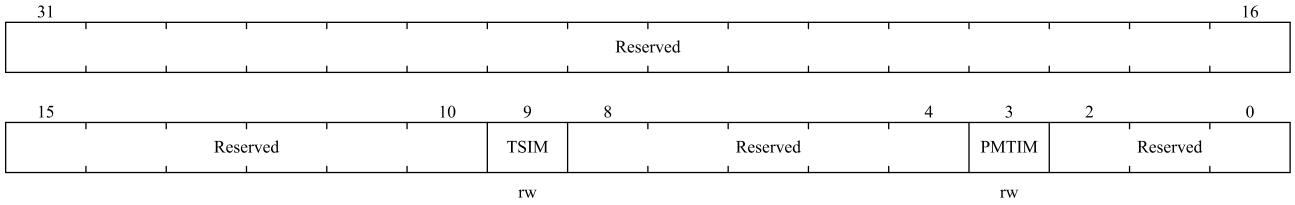
Bit field	Name	Description
		1: Any interrupt bit in ETH_MMCRXINT register is 1.
4	MMCIS	MMC status. 0: ETH_MACINTSTS.MMCTXIS and ETH_MACINTSTS.MMCRXIS are both 0. 1: One of ETH_MACINTSTS.MMCTXIS and ETH_MACINTSTS.MMCRXIS is 1.
3	PMTIS	PMT status. In low power mode, this bit is set to 1 when a remote wakeup frame or Magic Packet wakeup frame is received. This bit is also cleared to 0 after clearing ETH_MACPMTCTRLSTS.RWKPRCVD and ETH_MACPMTCTRLSTS.MGKPRCVD by reading the ETH_MACPMTCTRLSTS register.
2:0	Reserved	Reserved, the reset value must be maintained.

25.5.13 ETH MAC Interrupt Mask Register (ETH_MACINTMSK)

Address offset: 0x003C

Reset value: 0x0000 0000



Bit field	Name	Description
31:10	Reserved	Reserved, the reset value must be maintained.
9	TSIM	Timestamp trigger interrupt mask bit. 0: Enable generation of timestamp interrupts. 1: Disable generation of timestamp interrupts.
8:4	Reserved	Reserved, the reset value must be maintained.
3	PMTIM	PMT interrupt mask bit. 0: Enable generation of interrupts caused by ETH_MACINTSTS.PMTIS being set to 1. 1: Disable generation of interrupts caused by ETH_MACINTSTS.PMTIS being set to 1.
2:0	Reserved	Reserved, the reset value must be maintained.

25.5.14 ETH MAC Address 0 High Register (ETH_MACADDR0HI)

Address offset: 0x0040

Reset value: 0x8000 FFFF

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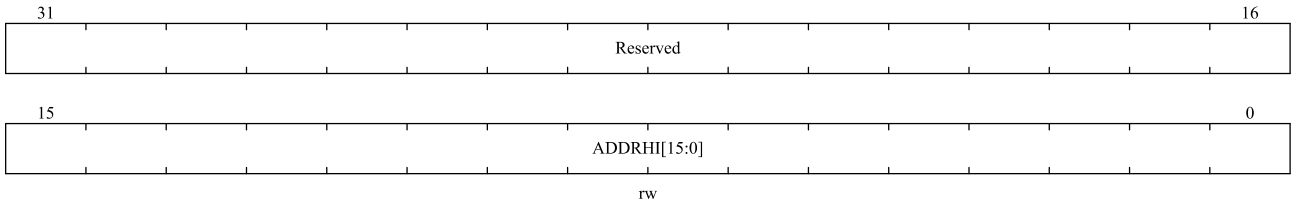
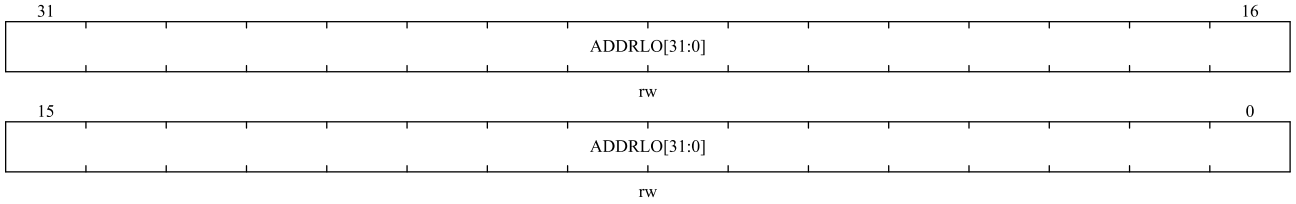


Bit field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained.
15:0	ADDRHI[15:0]	MAC address 0 high 16 bits. These bits contain the upper 16 bits of the 6-byte MAC address 0. These bits are used as the address filtering of the received frame, it is also used in transmit flow control, and is inserted as the source address of the frame when transmit a PAUSE frame.

25.5.15 ETH MAC Address 0 Low Register (ETH_MACADDR0LO)

Address offset: 0x0044

Reset value: 0xFFFF FFFF

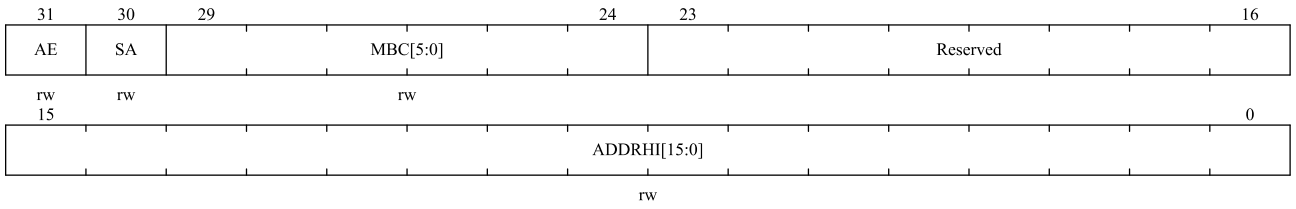


Bit field	Name	Description
31:0	ADDRLO[31:0]	MAC address 0 low 32 bits. These bits contain the lower 32 bits of the 6-byte MAC address 0. These bits are used as the address filtering of the received frame, it is also used in transmit flow control, and is inserted as the source address of the frame when transmit a PAUSE frame.

25.5.16 ETH MAC Address 1 High Register (ETH_MACADDR1HI)

Address offset: 0x0048

Reset value: 0x0000 FFFF



Bit field	Name	Description
31	AE	Address enable. 0: Address filter does not use MAC address 1 for perfect filtering.

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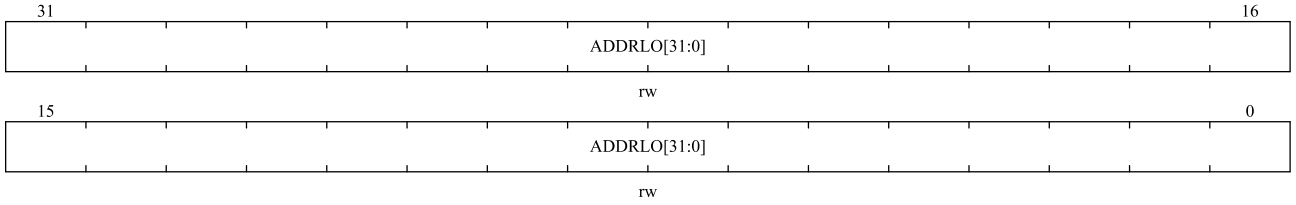
Bit field	Name	Description
		1: Address filter uses MAC address 1 for perfect filtering.
30	SA	Source address comparison. 0: MAC address 1 is used to compare with the destination address of the received frame. 1: MAC address 1 is used to compare with the source address of the received frame.
29:24	MBC[5:0]	Mask byte control bits. When a bit is set to 1, MAC will ignore the comparison of the corresponding byte of the destination/source address of the received frame with the corresponding byte of the MAC address 1. The MAC address bytes corresponding to each control bit are as follows: MBC[5]: ETH_MACADDR1HI[15:8] MBC[4]: ETH_MACADDR1HI[7:0] MBC[3]: ETH_MACADDR1LO[31:24] MBC[2]: ETH_MACADDR1LO[23:16] MBC[1]: ETH_MACADDR1LO[15:8] MBC[0]: ETH_MACADDR1LO[7:0]
23:16	Reserved	Reserved, the reset value must be maintained.
15:0	ADDRHI[15:0]	MAC address 1 high 16 bits. These bits contain the upper 16 bits of the 6-byte MAC address 1.

25.5.17 ETH MAC Address 1 Low Register (ETH_MACADDR1LO)

Address offset: 0x004C

Reset value: 0xFFFF FFFF



Bit field	Name	Description
31:0	ADDRLO[31:0]	MAC address 1 low 32 bits. These bits contain the lower 32 bits of the 6-byte MAC address 1.

25.5.18 ETH MAC Address 2 High Register (ETH_MACADDR2HI)

Address offset: 0x0050

Reset value: 0x0000 FFFF

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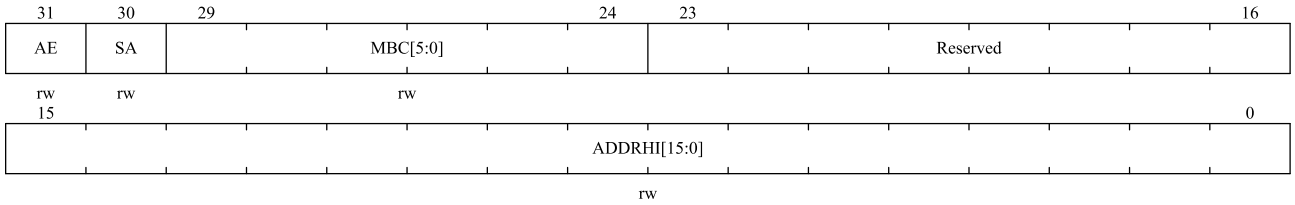
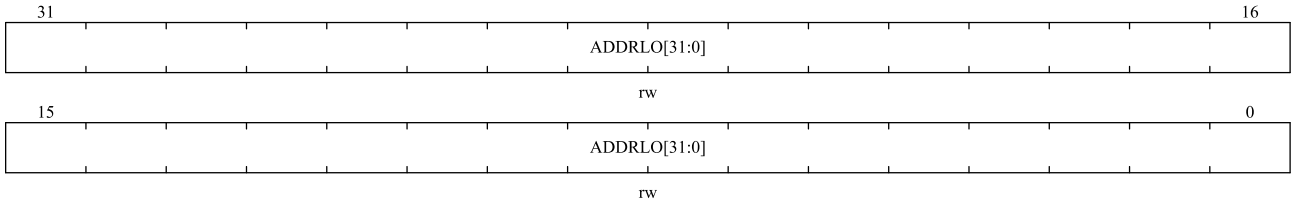


Bit field	Name	Description
31	AE	Address enable. 0: Address filter does not use MAC address 2 for perfect filtering. 1: Address filter uses MAC address 2 for perfect filtering.
30	SA	Source address comparison. 0: MAC address 2 is used to compare with the destination address of the received frame. 1: MAC address 2 is used to compare with the source address of the received frame.
29:24	MBC[5:0]	Mask byte control bits. When a bit is set to 1, MAC will ignore the comparison of the corresponding byte of the destination/source address of the received frame with the corresponding byte of the MAC address 2. The MAC address bytes corresponding to each control bit are as follows: MBC[5]: ETH_MACADDR2HI[15:8] MBC[4]: ETH_MACADDR2HI[7:0] MBC[3]: ETH_MACADDR2LO[31:24] MBC[2]: ETH_MACADDR2LO[23:16] MBC[1]: ETH_MACADDR2LO[15:8] MBC[0]: ETH_MACADDR2LO[7:0]
23:16	Reserved	Reserved, the reset value must be maintained.
15:0	ADDRHI[15:0]	MAC address 2 high 16 bits. These bits contain the upper 16 bits of the 6-byte MAC address 2.

25.5.19 ETH MAC Address 2 Low Register (ETH_MACADDR2LO)

Address offset: 0x0054

Reset value: 0xFFFF FFFF



Bit field	Name	Description
31:0	ADDRLO[31:0]	MAC address 2 low 32 bits. These bits contain the lower 32 bits of the 6-byte MAC address 2.

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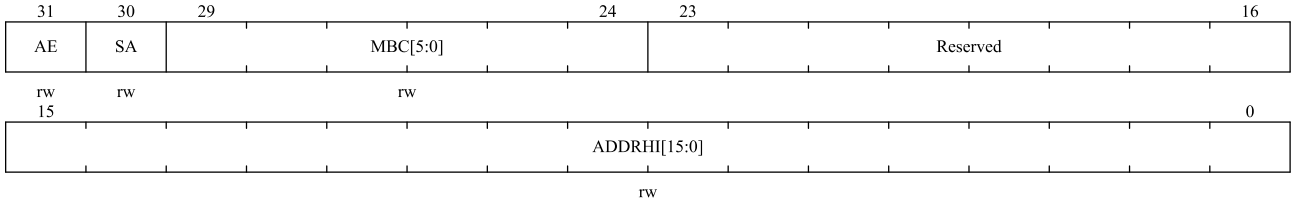
25.5.20 ETH MAC Address 3 High Register (ETH_MACADDR3HI)

Address offset: 0x0058

Reset value: 0x0000 FFFF



Bit field	Name	Description
31	AE	Address enable. 0: Address filter does not use MAC address 3 for perfect filtering. 1: Address filter uses MAC address 3 for perfect filtering.
30	SA	Source address comparison. 0: MAC address 3 is used to compare with the destination address of the received frame. 1: MAC address 3 is used to compare with the source address of the received frame.
29:24	MBC[5:0]	Mask byte control bits. When a bit is set to 1, MAC will ignore the comparison of the corresponding byte of the destination/source address of the received frame with the corresponding byte of the MAC address 3. The MAC address bytes corresponding to each control bit are as follows: MBC[5]: ETH_MACADDR3HI[15:8] MBC[4]: ETH_MACADDR3HI[7:0] MBC[3]: ETH_MACADDR3LO[31:24] MBC[2]: ETH_MACADDR3LO[23:16] MBC[1]: ETH_MACADDR3LO[15:8] MBC[0]: ETH_MACADDR3LO[7:0]
23:16	Reserved	Reserved, the reset value must be maintained.
15:0	ADDRHI[15:0]	MAC address 3 high 16 bits. These bits contain the upper 16 bits of the 6-byte MAC address 3.

25.5.21 ETH MAC Address 3 Low Register (ETH_MACADDR3LO)

Address offset: 0x005C

Reset value: 0xFFFF FFFF

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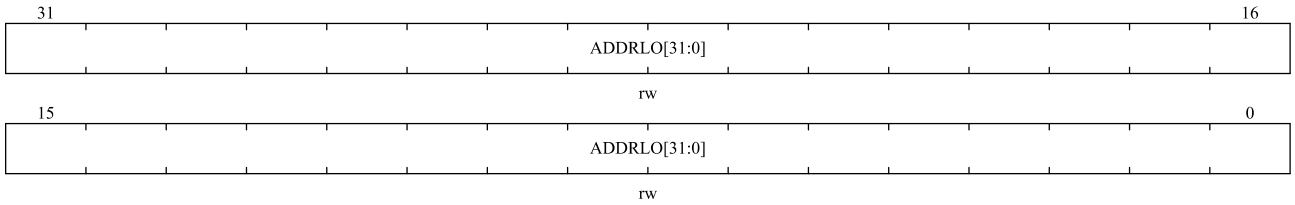
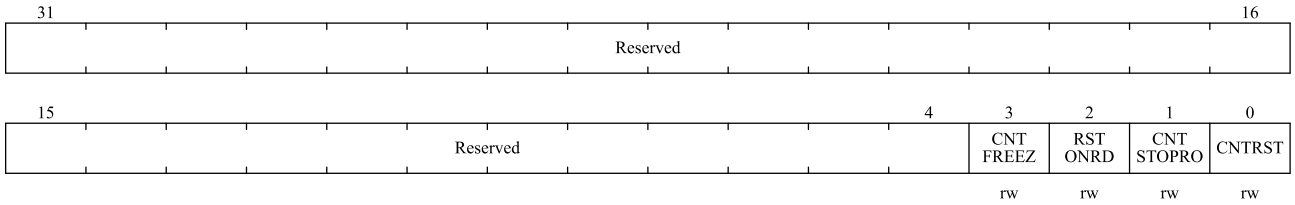


Bit field	Name	Description
31:0	ADDRLO[31:0]	MAC address 3 low 32 bits. These bits contain the lower 32 bits of the 6-byte MAC address 3.

25.5.22 ETH MMC Control Register (ETH_MMCCTRL)

Address offset: 0x0100

Reset value: 0x0000 0000



Bit field	Name	Description
31:4	Reserved	Reserved, the reset value must be maintained.
3	CNTFREEZ	MMC counter freezes. 0: MMC counter works normally. 1: All MMC counters are frozen, keeping the current value. RSTONRD function still works in this mode.
2	RSTONRD	Reset on read. 0: After reading the MMC counter, the counter is not reset. 1: After reading the MMC counter, the counter is reset.
1	CNTSTOPRO	Counter stop rollover. 0: After the counter reaches the maximum value, it will start counting from 0 again. 1: After the counter reaches the maximum value, it will not start counting from 0 again.
0	CNTRST	Counter reset. After this bit is set, it will be automatically cleared by hardware after 1 clock cycle. 0: No effect. 1: Reset all counters.

25.5.23 ETH MMC Receive Interrupt Status Register (ETH_MMCRXINT)

Address offset: 0x0104

Reset value: 0x0000 0000

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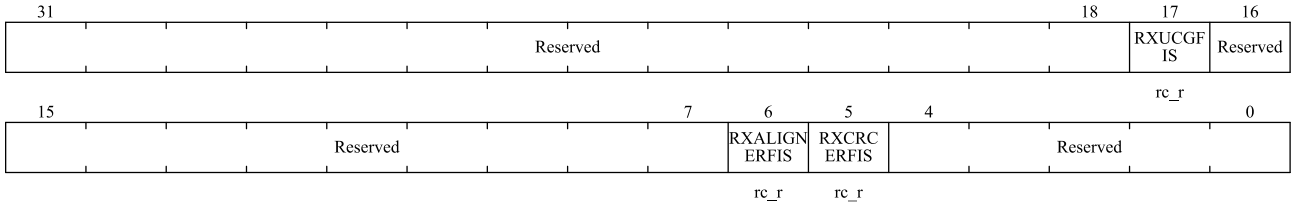
This register records the interrupt generated when the receive statistics register counts to half the maximum value (the highest bit of the counter is set). Reading the MMC counter that generates an interrupt can clear the corresponding interrupt bit (must read the lower 8 bits of the corresponding counter).



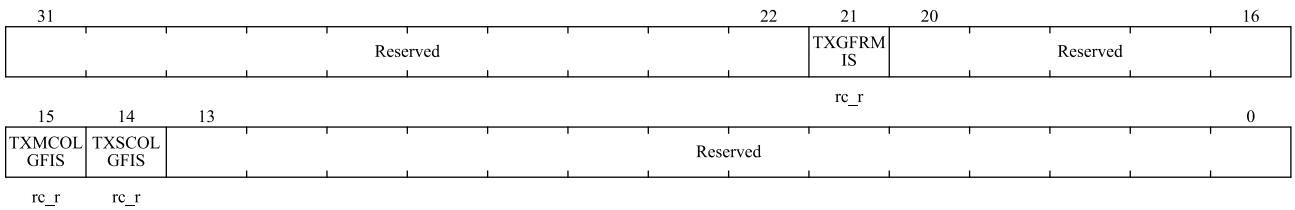
Bit field	Name	Description
31:18	Reserved	Reserved, the reset value must be maintained.
17	RXUCGFIS	"Good" unicast frame status received. 0: "Good" unicast frame received counter value has not reached half of the maximum value. 1: "Good" unicast frame received counter value reaches half of the maximum value.
16:7	Reserved	Reserved, the reset value must be maintained.
6	RXALIGNERFIS	A frame alignment error status was received. 0: Alignment error received frame counter value has not reached half of the maximum value. 1: Alignment error received frame counter value reaches half of the maximum value.
5	RXCRCERFIS	Received frame CRC error status. 0: CRC error received frame counter value has not reached half of the maximum value. 1: CRC error received frame counter value reaches half of the maximum value.
4:0	Reserved	Reserved, the reset value must be maintained.

25.5.24 ETH MMC Transmit Interrupt Status Register (ETH_MMCTXINT)

Address offset: 0x0108

Reset value: 0x0000 0000

This register records the interrupt generated when the transmit statistics register counts to half the maximum value (the highest bit of the counter is set). Reading the MMC counter that generates an interrupt can clear the corresponding interrupt bit (must read the lower 8 bits of the corresponding counter).



Bit field	Name	Description
31:22	Reserved	Reserved, the reset value must be maintained.
21	TXGFRMIS	"Good" frame status transmit.

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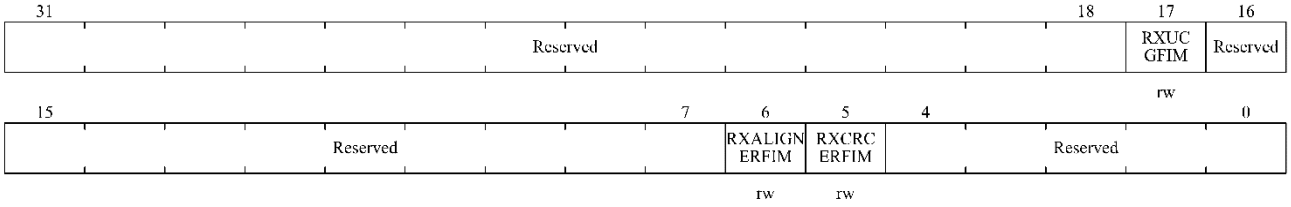
Bit field	Name	Description
		0: Transmit "good" frame counter value has not reached half of the maximum value. 1: Transmit "good" frame counter value reaches half of the maximum value.
20:16	Reserved	Reserved, the reset value must be maintained.
15	TXMCOLGFIS	More than 1 collision state was encountered while transmit a "good" frame. 0: After more than 1 collision, transmit "good" frame counter value has not reached half of the maximum value. 1: After more than 1 collision, transmit "good" frame counter value reaches half of the maximum value.
14	TXSCOLGFIS	Only 1 collision state was encountered while transmit a "good" frame. 0: After 1 collision, transmit "good" frame counter value has not reached half of the maximum value. 1: After 1 collision, transmit "good" frame counter value reaches half of the maximum value.
13:0	Reserved	Reserved, the reset value must be maintained.

25.5.25 ETH MMC Receive Interrupt Mask Register (ETH_MMCRXINTMSK)

Address offset: 0x010C

Reset value: 0x0000 0000



Bit field	Name	Description
31:18	Reserved	Reserved, the reset value must be maintained.
17	RXUCGFIM	Receive "good" unicast frame interrupt mask bit. 0: Do not mask the interrupt that occurs when ETH_MMCRXINT.RXUCGFIS is 1. 1: Mask the interrupt that occurs when ETH_MMCRXINT.RXUCGFIS is 1.
16:7	Reserved	Reserved, the reset value must be maintained.
6	RXALIGNERFIM	Receive frame alignment error interrupt mask bit. 0: Do not mask the interrupt that occurs when ETH_MMCRXINT.RXALIGNERFIS is 1. 1: Mask the interrupt that occurs when ETH_MMCRXINT.RXALIGNERFIS is 1.
5	RXCRCERFIM	Receive frame CRC error interrupt mask bit. 0: Do not mask the interrupt that occurs when ETH_MMCRXINT.RXCRCERFIS is 1. 1: Mask the interrupt that occurs when ETH_MMCRXINT.RXCRCERFIS is 1.
4:0	Reserved	Reserved, the reset value must be maintained.

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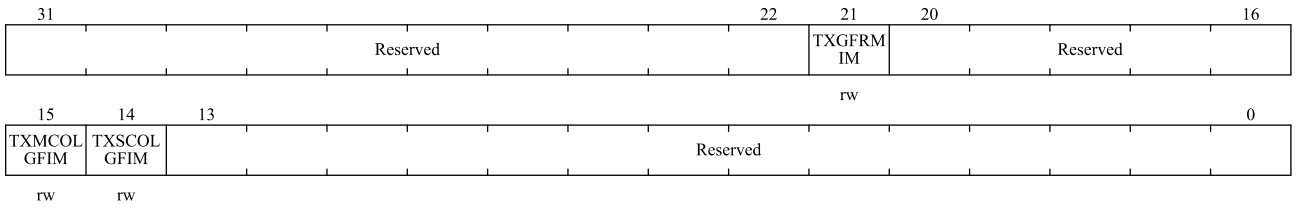
25.5.26 ETH MMC Transmit Interrupt Mask Register (ETH_MMCTXINTMSK)

Address offset: 0x0110

Reset value: 0x0000 0000



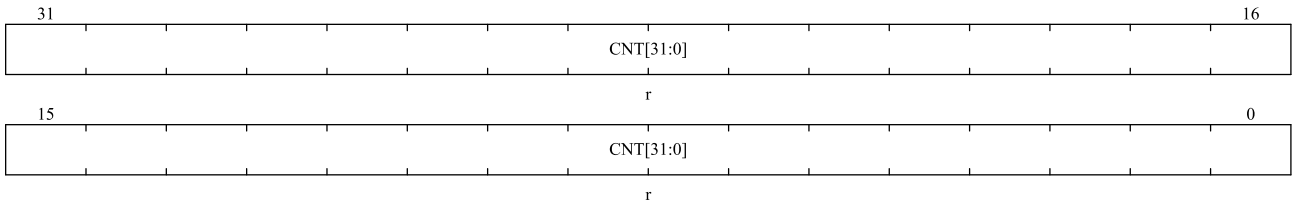
Bit field	Name	Description
31:22	Reserved	Reserved, the reset value must be maintained.
21	TXGFRMIM	Transmit "good" frame interrupt mask bit. 0: Do not mask the interrupt that occurs when ETH_MMCTXINT.TXGFRMIS is 1. 1: Mask the interrupt that occur when the ETH_MMCTXINT.TXGFRMIS bit is 1.
20:16	Reserved	Reserved, the reset value must be maintained.
15	TXMCOLGFIM	Transmit "good" frame interrupt mask bit after more than 1 collision. 0: Do not mask the interrupt that occurs when ETH_MMCTXINT.TXMCOLGFIS is 1. 1: Mask the interrupt that occurs when ETH_MMCTXINT.TXMCOLGFIS is 1.
14	TXSCOLGFIM	Transmit "good" frame interrupt mask bit after only 1 collision. 0: Do not mask the interrupt that occurs when ETH_MMCTXINT.TXSCOLGFIS is 1. 1: Mask the interrupt that occurs when ETH_MMCTXINT.TXSCOLGFIS is 1.
13:0	Reserved	Reserved, the reset value must be maintained.

25.5.27 ETH MMC Transmitted “good” Frame Counter Register After 1 Collision (ETH_MMCTXGFASCCNT)

Address offset: 0x014C

Reset value: 0x0000 0000

This register is used to count the number of frames successfully transmitted after only one collision in half-duplex mode.



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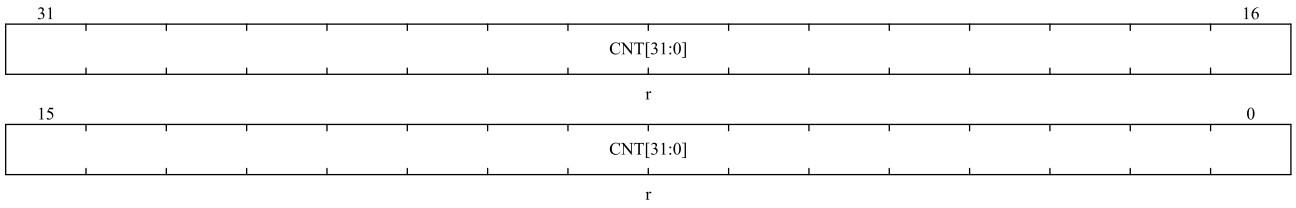
Bit field	Name	Description
31:0	CNT[31:0]	Transmitted "good" frame counter after 1 collision. These bits are a counter of "good" frame transmitted after 1 collision.

25.5.28 ETH MMC Transmitted “good” Frame Counter Register After More Collision (ETH_MMCTXGFAMSCCNT)

Address offset: 0x0150

Reset value: 0x0000 0000

This register is used to count the number of frames successfully transmitted after more than one collision in half-duplex mode.



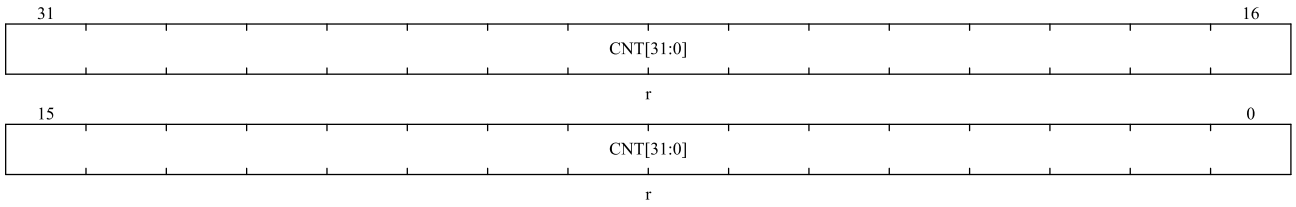
Bit field	Name	Description
31:0	CNT[31:0]	Transmitted "good" frame counter after more than 1 collision. These bits are a counter of "good" frame transmitted after more than 1 collision.

25.5.29 ETH MMC Transmitted “good” Frame Counter Register (ETH_MMCTXGFCNT)

Address offset: 0x0168

Reset value: 0x0000 0000

This register is used to count the number of "good" frames transmitted.



Bit field	Name	Description
31:0	CNT[31:0]	Transmitted "good" frame counter. These bits are a counter of "good" frame transmitted.

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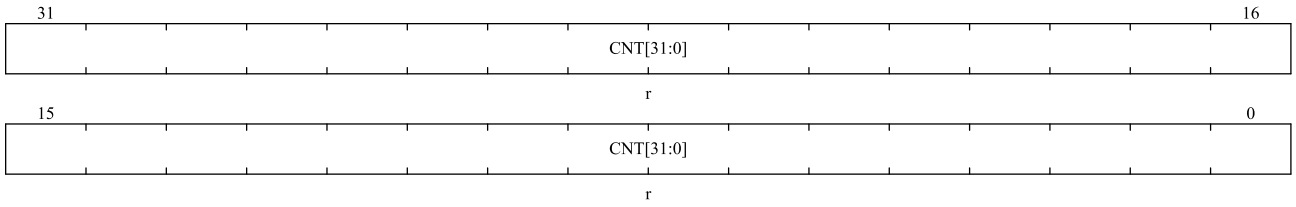
25.5.30 ETH MMC CRC Error Received Frame Counter Register (ETH_MMCRXFCECNT)

Address offset: 0x0194

Reset value: 0x0000 0000

This register is used to count the number of frames with CRC errors in the received frames.



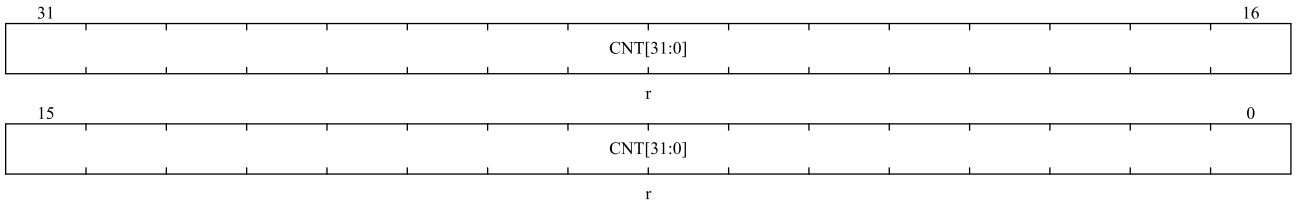
Bit field	Name	Description
31:0	CNT[31:0]	CRC error received frame counter. These bits are a counter of frames with CRC errors in the received frame.

25.5.31 ETH MMC Alignment Error Received Frame Counter Register (ETH_MMCRXFAECNT)

Address offset: 0x0198

Reset value: 0x0000 0000

This register is used to count the number of frames with alignment errors in received frames.



Bit field	Name	Description
31:0	CNT[31:0]	Alignment error received frame counter. These bits are a counter of frames with misalignment in the received frame.

25.5.32 ETH MMC Receive "good" Unicast Frame Counter Register (ETH_MMCRXGUFCNT)

Address offset: 0x01C4

Reset value: 0x0000 0000

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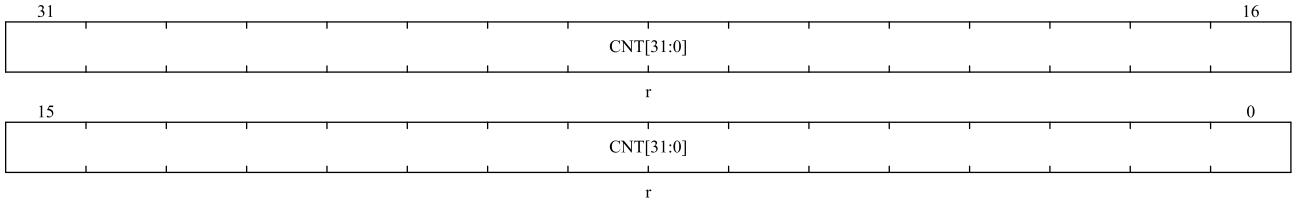
This register is used to count the number of "good" unicast frames received.



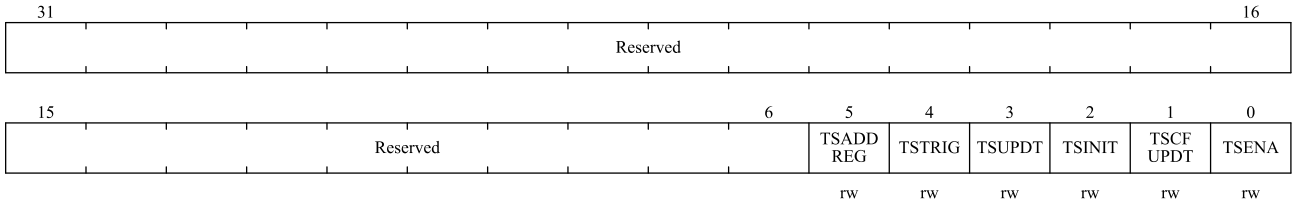
Bit field	Name	Description
31:0	CNT[31:0]	"Good" unicast frame receive counter. These bits are a counter of "good" unicast frames received.

25.5.33 ETH PTP Timestamp Control Register (ETH_PTPTSCTRL)

Address offset: 0x0700

Reset value: 0x0000 0000

This register controls the timestamp generation and update logic.



Bit field	Name	Description
31:6	Reserved	Reserved, the reset value must be maintained.
5	TSADDREG	Timestamp adder register update bit. This bit is cleared to 0 after the update is complete. This bit must be read as 0 before being set to 1. 0: Do not update the value of the timestamp addend register to the PTP module for fine adjustment. 1: Update the value of the timestamp addend register to the PTP module for fine adjustment.
4	TSTRIG	Timestamp interrupt trigger enable bit. 0: Disable time stamp interrupt. 1: Enable time stamp interrupt, which will generate an interrupt when the system time exceeds the expected time register value. *Note: This bit will be cleared to 0 after the timestamp interrupt is generated.*
3	TSUPDT	Timestamp system time update bit. Before setting this bit, must ensure that both this bit and ETH_PTPTSCTRL.TSINIT read 0. 0: System time remains unchanged. 1: Update system time, add or subtract the value of the timestamp high and low update registers to the original system time, and the hardware will clear this bit after

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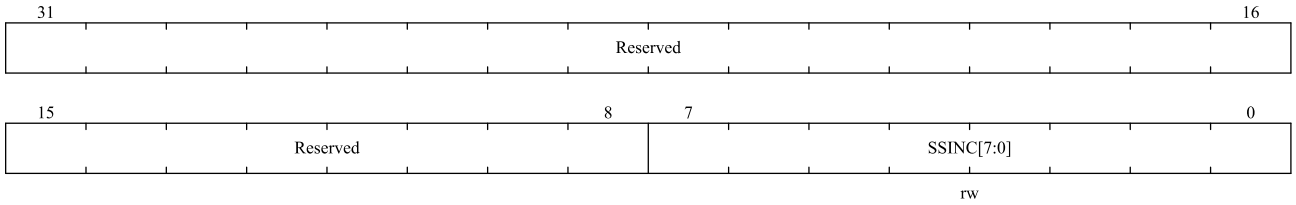
Bit field	Name	Description
		the update is completed.
2	TSINIT	Timestamp system time initialization bit. Before setting this bit, must ensure that this bit read 0. 0: System time remains unchanged. 1: Initialize system time and replace the original system time with the values of the timestamp high and low update registers. Hardware will clear this bit after initialization is complete.
1	TSCFUPDT	Timestamp coarse adjustment or fine adjustment update bit. 0: Update system timestamp with coarse adjustment. 1: Update system timestamp with fine adjustment.
0	TSENA	Timestamp enable bit. 0: Disable timestamp function. 1: Enable timestamp function of received and transmitted frames. *Note: The system time needs to be re-initialized every time this bit is set to '1'.*

25.5.34 ETH PTP Subsecond Increment Register (ETH_PTPSSINC)

Address offset: 0x0704

Reset value: 0x0000 0000

This register is used to configure the 8-bit increment value of the subsecond increment register. In coarse adjustment mode, the system time is incremented by the value of this register after every HCLK clock cycle. In fine adjustment mode, the system time is incremented by the value of this register only when the accumulator overflows.



Bit field	Name	Description
31:8	Reserved	Reserved, the reset value must be maintained.
7:0	SSINC[7:0]	System time subsecond increment value. The value of these bits is added to the subsecond value of the system time each time the system time is incremented.

25.5.35 ETH PTP Timestamp High Register (ETH_PTPSEC)

Address offset: 0x0708

Reset value: 0x0000 0000

This register is read-only and contains the second value of the system time. The system time high and low 2 registers contain the current system time value of the MAC, which is continuously updated.

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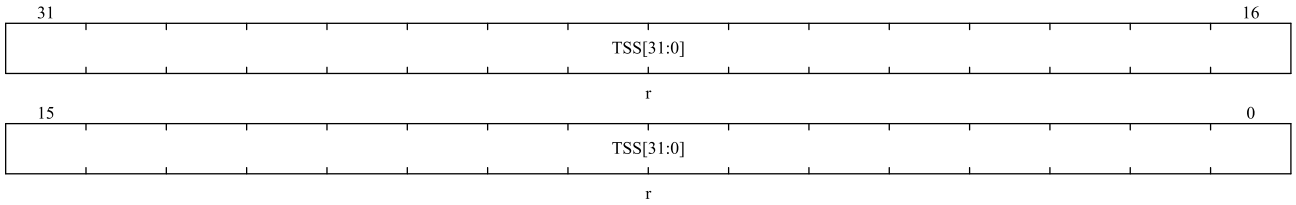


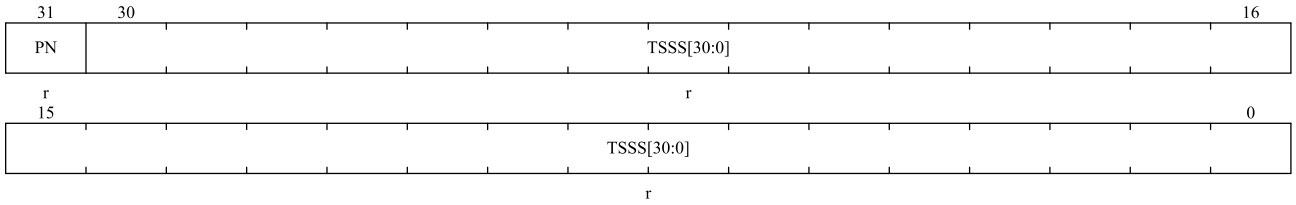
Bit field	Name	Description
31:0	TSS[31:0]	System time seconds. These bits represent the second value of the MAC's current system time.

25.5.36 ETH PTP Timestamp Low Register (ETH_PTPNS)

Address offset: 0x070C

Reset value: 0x0000 0000

This register is read-only and contains the subsecond value of the system time.



Bit field	Name	Description
31	PN	System time positive or negative sign. 0: Time value is positive value. 1: Time value is negative value.
30:0	TSSS[30:0]	System time subsecond. These bits represent the sub-second value of the current system time, sub-second precision is 0.46ns.

25.5.37 ETH PTP Timestamp High Update Register (ETH_PTPSECUP)

Address offset: 0x0710

Reset value: 0x0000 0000

Use the value of this register to replace, add or subtract the current system time. The timestamp high update register and the timestamp low update register can be used to initialize or update the current system time of the MAC. These 2 registers should be written first, and then ETH_PTPTSCTRL.TSINIT or ETH_PTPTSCTRL.TSUPDT should be set.

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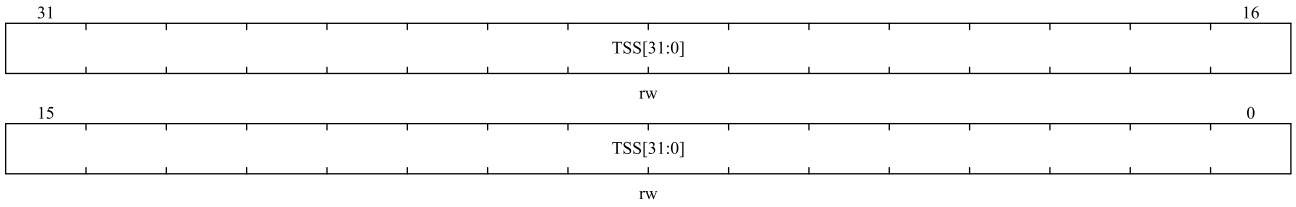
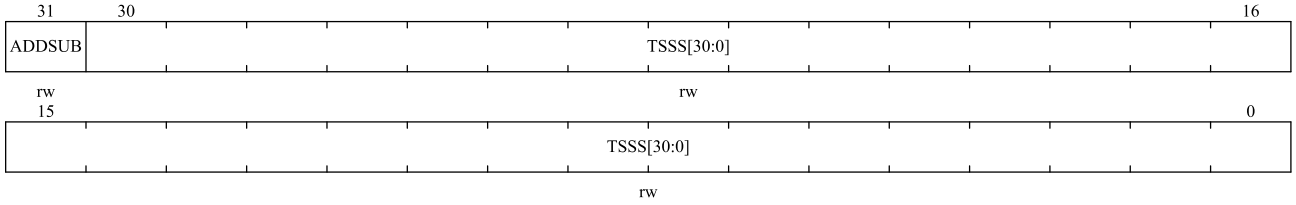


Bit field	Name	Description
31:0	TSS[31:0]	Timestamp seconds update value. The value represented by these bits is used to replace the system time when initialized, and when updated, it represents the value of seconds added or subtracted from the system time.

25.5.38 ETH PTP Timestamp Low Update Register (ETH_PTPNSUP)

Address offset: 0x0714

Reset value: 0x0000 0000



Bit field	Name	Description
31	ADDSUB	Timestamp update positive or negative sign. When ETH_PTPTSCTRL.TSINIT is set to 1, this bit should be 0. When ETH_PTPTSCTRL.TSUPDT is set to 1 and this bit is 0, the timestamp update value is added to the system time, otherwise, the timestamp update value is subtracted from the system time. 0: Time value is positive value. 1: Time value is negative value.
30:0	TSSS[30:0]	System time subsecond. These bits represent the sub-second value of the current system time, sub-second precision is 0.46ns.

25.5.39 ETH PTP Timestamp Addend Register (ETH_PTPTSADD)

Address offset: 0x0718

Reset value: 0x0000 0000

This register is only used when the system time update mode is fine adjustment mode. Software can use this register to linearly calibrate the clock frequency to the main clock. The value of this register is accumulated to the 32-bit accumulator every clock cycle, and the system time is updated once the accumulator overflows.

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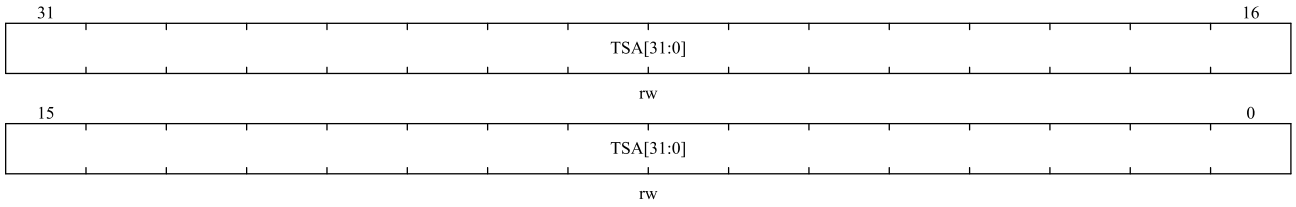
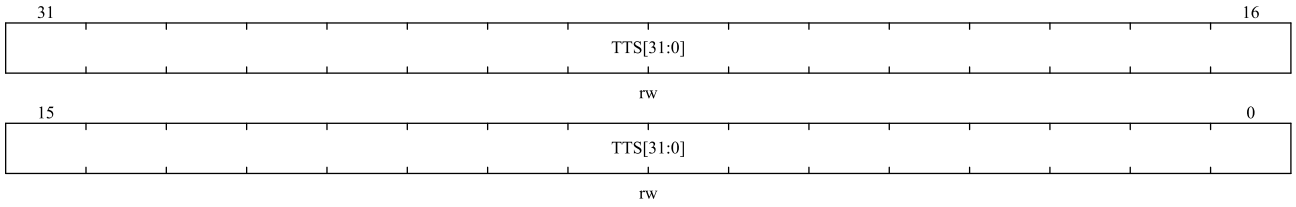


Bit field	Name	Description
31:0	TSA[31:0]	Timestamp addend. These bits represent the 32-bit value added to the accumulator when the clocks are synchronized.

25.5.40 ETH PTP Target Time High Register (ETH_PTPTTSEC)

Address offset: 0x071C

Reset value: 0x0000 0000

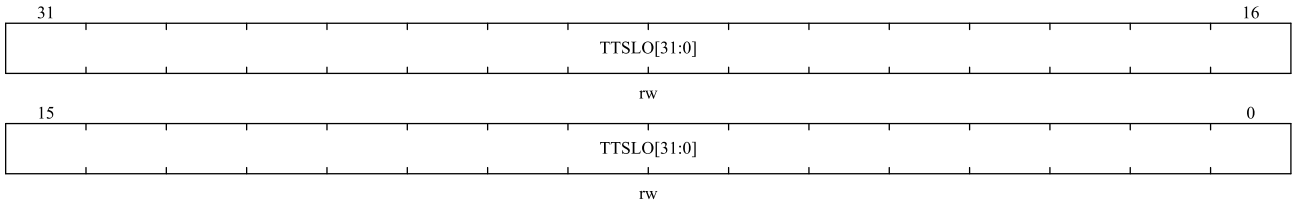


Bit field	Name	Description
31:0	TTS[31:0]	Target timestamp high. These bits represent the seconds value of the target time. If the timestamp value equals or exceeds the target time, and the corresponding interrupt is enabled, MAC will generate an interrupt.

25.5.41 ETH PTP Target Time Low Register (ETH_PTPTTNS)

Address offset: 0x0720

Reset value: 0x0000 0000



Bit field	Name	Description
31:0	TTSLO[31:0]	Target timestamp low. These bits represent the nanosecond value of the target time. If the timestamp value equals or exceeds the target time, and the corresponding interrupt is enabled, MAC will generate an interrupt.

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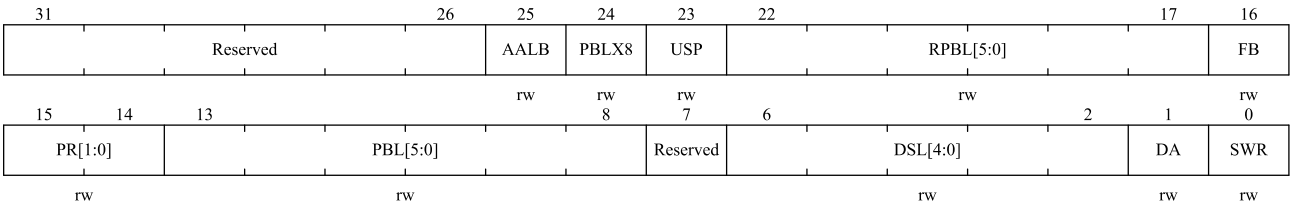
25.5.42 ETH DMA Bus Mode Register (ETH_DMABUSMOD)

Address offset: 0x1000

Reset value: 0x0000 2101



Bit field	Name	Description
31:26	Reserved	Reserved, the reset value must be maintained.
25	AALB	Address alignment. 0: Disable the transfer address alignment function. 1: Enable transfer address alignment, if ETH_DMABUSMOD.FB is 1, the AHB interface aligns all LS bits of consecutive transfers to the starting address. If ETH_DMABUSMOD.FB is 0, except the address of the first AHB access (the starting address of accessing the data buffer) is not aligned, subsequent transfers and addresses are aligned.
24	PBLX8	8x PBL mode. 0: The PBL value is used as the DMA transfer length value. 1: The PBL value is multiplied by 8 as the DMA transfer length value. For specific values, see ETH_DMABUSMOD.RPBL[5:0] or ETH_DMABUSMOD.PBL[5:0].
23	USP	Use dispersed PBL. 0: The PBL value set by ETH_DMABUSMOD.PBL[5:0] is valid for both DMA receive and transmit controllers. 1: The value of ETH_DMABUSMOD.RPBL[5:0] is used as the PBL value of receiving DMA, and the value of ETH_DMABUSMOD.PBL[5:0] is only used as the PBL value of sending DMA.
22:17	RPBL[5:0]	RxDMA PBL. If ETH_DMABUSMOD.USP = 0, these bits have no effect. When ETH_DMABUSMOD.USP = 1, these bits define the maximum number of data transfers for one DMA forwarding. 000001: The maximum number of data transfers is 1 000010: The maximum number of data transfers is 2 000100: The maximum number of data transfers is 4 001000: The maximum number of data transfers is 8 010000: The maximum number of data transfers is 16 100000: The maximum number of data transfers is 32 Other: reserved
16	FB	Fixed burst bit.

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Bit field	Name	Description
		This bit controls whether the AHB master interface performs fixed burst length transfers. 0: AHB uses only SINGLE and INCR data transfer operations during continuous transfer. 1: AHB uses SINGLE, INCR4, INCR8 and INCR16 data transfer operations during continuous transfer.
15:14	PR[1:0]	Receive and transmit priority ratio. These bits represent the access priority ratio between RxDMA and TxDMA. 00: RxDMA:TxDMA = 1:1 01: RxDMA:TxDMA = 2:1 10: RxDMA:TxDMA = 3:1 11: RxDMA:TxDMA = 4:1 *Note: This bit is only valid when the DMA arbitration mode is cyclic mode (ETH_DMABUSMOD.DA = 0).*
13:8	PBL[5:0]	Programmable burst length. These bits define the maximum number of data transfers for one DMA transfer. If ETH_DMABUSMOD.USP = 1, these bits are only used for TxDMA transfers. If ETH_DMABUSMOD.USP = 0, these bits are used for both TxDMA and RxDMA transfers. 000001: The maximum number of data transfers is 1 000010: The maximum number of data transfers is 2 000100: The maximum number of data transfers is 4 001000: The maximum number of data transfers is 8 010000: The maximum number of data transfers is 16 100000: The maximum number of data transfers is 32 Other: reserved
7	Reserved	Reserved, the reset value must be maintained.
6:2	DSL[4:0]	Descriptor skip length. These bits define the jump distance between 2 descriptors connected in a ring structure, in words (32 bits). Address jump refers to the address difference from the end of the current descriptor to the beginning of the next descriptor.
1	DA	DMA arbitration bit. This bit indicates the arbitration mode between TxDMA and RxDMA. 0: Arbitrate in a round-robin manner according to the value of these bits in ETH_DMABUSMOD.PR[1:0]. 1: Fixed priority mode, the priority of receiving is higher than that of sending.
0	SWR	Software reset. 0: No effect 1: Reset the internal registers and logic circuits of all subsystems of ETH. After the reset operation of different clock domain modules in the MAC is completed, this bit is automatically cleared. *Note: Make sure this bit is 0 before writing to any ETH register.*

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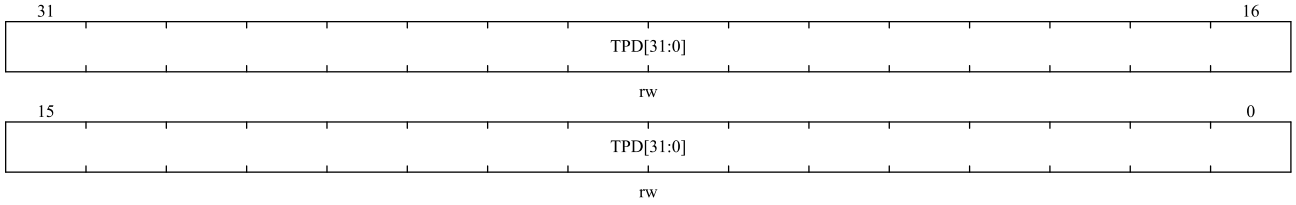
25.5.43 ETH DMA Transmit Query Request Register (ETH_DMATXPD)

Address offset: 0x1004

Reset value: 0x0000 0000

This register is used for TxDMA to query the list of transmit descriptors. TxDMA usually enters the pending state due to a data underflow error in the transmit frame or the descriptor is occupied by the CPU (TDES0.OWN = 0). Any value can be written to this register to enable sending queries.



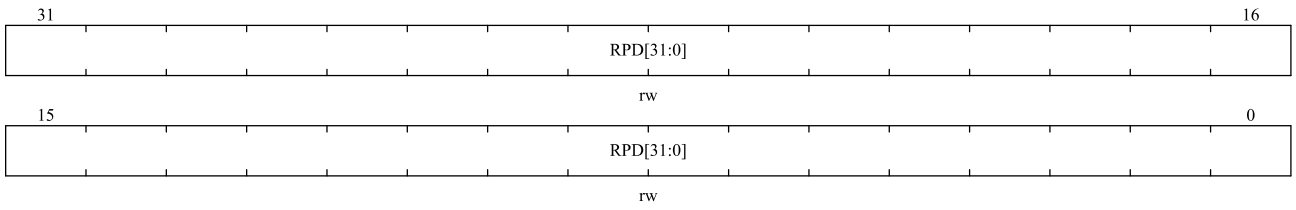
Bit field	Name	Description
31:0	TPD[31:0]	Transmit query request bit. Write any value to these bits to enable TxDMA transmit query, which will query whether the current descriptor (descriptor address is in the ETH_DMACHTXDESC register) is occupied by the CPU. If not (TDES0.OWN = 1), the descriptor is available and TxDMA exits the suspend state and resumes work. On the contrary (TDES0.OWN = 0), the TxDMA returns to the suspended state and ETH_DMASTS.TU is set to 1.

25.5.44 ETH DMA Receive Query Request Register (ETH_DMARXPD)

Address offset: 0x1008

Reset value: 0x0000 0000

This register is used for RxDMA query of the receive descriptor list. Writing any value to this register enables the receive query.



Bit field	Name	Description
31:0	RPD[31:0]	Receive query request bit. Write any value to these bits to enable RxDMA receive query, which will query whether the current descriptor (descriptor address is in the ETH_DMACHRXDESC register) is occupied by the CPU. If not (RDES0.OWN = 1), the descriptor is available and RxDMA exits the suspend state and resumes work. On the contrary (RDES0.OWN = 0), the RxDMA returns to the suspended state and ETH_DMASTS.RU is set to 1.

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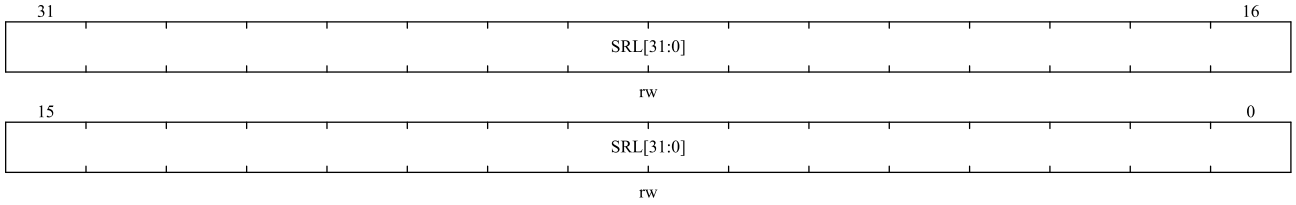
25.5.45 ETH DMA Receive Descriptor List Address Register (ETH_DMARXDLADDR)

Address offset: 0x100C

Reset value: 0x0000 0000

The receive descriptor list register points to the beginning of the receive descriptor queue. Descriptor queues are located in physical memory, and their addresses must be word-aligned. Writing to this register is only allowed when reception is stopped. This register must be configured correctly before starting the RxDMA receive process.



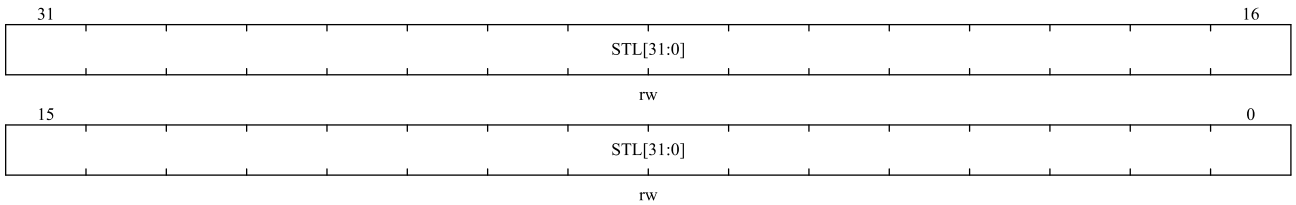
Bit field	Name	Description
31:0	SRL[31:0]	Receive queue base address. These bits contain the address of the first descriptor in the receive descriptor queue. RxDMA ignores the lowest 2 bits and defaults to 0.

25.5.46 ETH DMA Transmit Descriptor List Address Register (ETH_DMATXDLADDR)

Address offset: 0x1010

Reset value: 0x0000 0000

This register points to the start of the transmit descriptor queue. Descriptor queues are located in physical memory, and their addresses must be word-aligned. Writing to this register is only allowed when transmission is stopped. Before starting the TxDMA transmission process, this register must be configured correctly.



Bit field	Name	Description
31:0	STL[31:0]	Transmit queue base address. These bits contain the address of the first descriptor of the transmit descriptor queue. TxDMA ignores the lowest 2 bits and defaults to 0.

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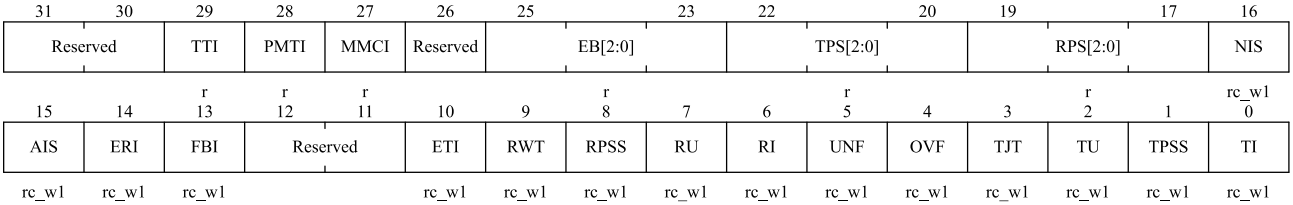
25.5.47 ETH DMA Status Register (ETH_DMASTS)

Address offset: 0x1014

Reset value: 0x0000 0000

This register contains all the status bits that the DMA feeds back to the application. Software usually reads this register in an interrupt service routine or during polling. Most bits in this register can trigger interrupts. Reading this register does not clear the flags in it. Writing 1 to bit0~bit16 (except reserved bits) can clear them, while writing 0 is invalid. By setting the corresponding bits in the ETH_DMAINTEN register, the interrupts triggered by these bits (except reserved bits) of bit0~bit16 can be masked.



Bit field	Name	Description
31:30	Reserved	Reserved, the reset value must be maintained.
29	TTI	Timestamp trigger status. This bit indicates that a timestamp interrupt event has occurred. Clear this bit by clearing ETH_MACINTSTS.TSTS. When this bit is set to 1, an interrupt is generated if the corresponding interrupt is enabled. 0: No timestamp interrupt event occurred. 1: A timestamp interrupt event has occurred.
28	PMTI	PMT status. This bit indicates that an interrupt event has occurred in the PMT module of the MAC controller. Software must read the corresponding register of the MAC controller, find the source of the interrupt and clear it, in order to clear this bit. When this bit is set, an interrupt is generated if the corresponding interrupt is enabled. 0: No PMT interrupt event occurred. 1: A PMT interrupt event has occurred.
27	MMCI	MMC status. This bit indicates that an interrupt event has occurred in the MMC module of the MAC controller. Software must read the corresponding register of the MAC controller, find the source of the interrupt and clear it, in order to clear this bit. When this bit is set, an interrupt is generated if the corresponding interrupt is enabled. 0: No MMC interrupt event occurred. 1: An MMC interrupt event has occurred.
26	Reserved	Reserved, the reset value must be maintained.
25:23	EB[2:0]	Error bit status. When ETH_DMASTS.FBI = 1, these bits will do error type resolution for bus response errors on the AHB bus, these bits will not trigger an interrupt. EB[0]:

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Bit field	Name	Description
		0: Error during RxDMA transfer of data. 1: Error during TxDMA transfer of data. EB[1]: 0: Error during write transfer. 1: Error during read transfer. EB[2]: 0: Error during data buffer access. 1: Error during descriptor access.
22:20	TPS[2:0]	Transmit process status. These bits indicate the status of TxDMA. 000: Stop, receive reset or stop transmitting command. 001: Running, getting transmit descriptor. 010: Running, waiting status information. 011: Running, data in memory is being read and stored in TxFIFO. 100, 101: Reserved. 110: Pause, transmit descriptor unavailable or transmit buffer data underflow. 111: Running, closing transmit descriptor.
19:17	RPS[2:0]	Receive process status. These bits indicate the status of RxDMA. 000: Stop, receive reset or stop receiving command. 001: Running, getting receive descriptor. 010: Reserved. 011: Running, waiting receive packets. 100: Pause, receive descriptor not available. 101: Running, closing receive descriptor. 110: Reserved. 111: Running, forwarding received packets from RxFIFO to memory.
16	NIS	Normal interrupt summary. With the corresponding interrupt enabled in the ETH_DMAINTEN register, the normal interrupt summary bits are the logical OR of the following bit values: • ETH_DMASTS [0]: Transmit interrupt • ETH_DMASTS [2]: Transmit buffer unavailable • ETH_DMASTS [6]: Receive interrupt • ETH_DMASTS [14]: Early receive interrupt Only unmasked interrupts will affect this bit. The value of this bit is bound to the above bits. After it is set to 1, this bit can only be cleared to 0 by clearing the bit that caused the bit to 1 (write 1).
15	AIS	Abnormal interrupt summary. With the corresponding interrupt enabled in the ETH_DMAINTEN register, the exception interrupt summary bit is the logical OR of the following bit values: • ETH_DMASTS [1]: Transmit process stopped • ETH_DMASTS [3]: Transmit Jabber timeout • ETH_DMASTS [4]: RxFIFO overflow

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Bit field	Name	Description
		• ETH_DMASTS [5]: Transmit data underflow • ETH_DMASTS [7]: Receive buffer unavailable • ETH_DMASTS [8]: Receive process stopped • ETH_DMASTS [9]: Receive watchdog timeout • ETH_DMASTS [10]: Early send interrupt • ETH_DMASTS [13]: Bus fatal error Only unmasked interrupts will affect this bit. The value of this bit is bound to the above bits. After it is set to 1, this bit can only be cleared to 0 by clearing the bit that caused the bit to 1 (write 1).
14	ERI	Early receive status. This bit is automatically cleared to 0 when ETH_DMASTS.RI is set to 1. 0: Frame data is not received. 1: The received data frame has filled the first buffer by DMA.
13	FBI	Bus fatal error status. This bit indicates that an AHB interface response error has occurred, the type of error can be explained by these bits of ETH_DMASTS.EB[2:0]. 0: No bus error occurred. 1: A bus error has occurred and the corresponding DMA controller closes all bus accesses.
12:11	Reserved	Reserved, the reset value must be maintained.
10	ETI	Early transmit status. 0: Transmit frame has not been fully transferred into TxFIFO. 1: Transmit frame has been completely transferred into TxFIFO.
9	RWT	Receive watchdog timeout status. 0: Received frame length less than 2048 bytes. 1: Received frame length exceeds 2048 bytes.
8	RPSS	Receive process stop status. 0: Receive process no stop. 1: Receive process enters stop status.
7	RU	Receive buffer unavailable status. When this bit is set to 1, it means that the next receive descriptor is not occupied by RxDMA, and RxDMA will enter the pause (suspend) state. In this case, it is necessary to reconfigure the ownership of the descriptor and initiate the receive query request command to exit the pause (suspend) state. Refer to the description of relevant steps in Section 25.4.8.4.5. 0: RDES0.OWN of the next receive descriptor is 1. 1: RDES0.OWN of the next receive descriptor is 0.
6	RI	Receive status. 0: Frame receive not complete. 1: Frame receive complete.
5	UNF	Transmit data underflow status. When this bit is set, the transmission enters the pause (suspend) state and set TDES0.UF to 1.

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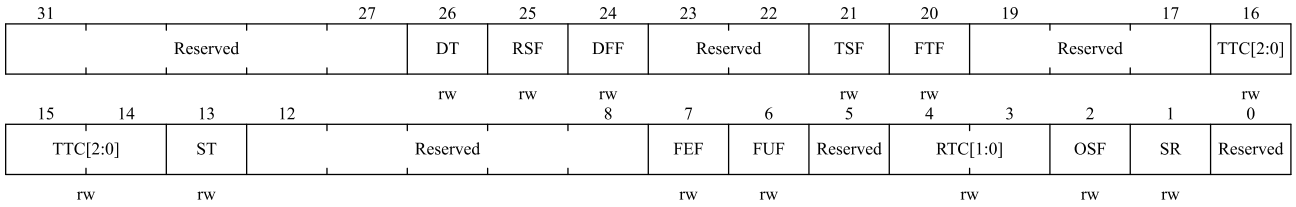
Bit field	Name	Description
		0: No transmit data underflow error occurred. 1: Data underflow error occurred during frame transmission.
4	OVF	Receive overflow status. When this bit is 1, if some frame data has been forwarded to the memory, set RDES0.OE to 1. 0: No receive data overflow error occurred. 1: Data overflow error occurred during frame receive.
3	TJT	Transmit Jabber timeout status. When this bit is 1, the sending process is aborted and enters the stop state, and TDES0.JT is set to 1 at the same time. 0: No transmit Jabber timer timeout event occurred. 1: Transmit Jabber timer timeout.
2	TU	Transmit buffer unavailable status. When this bit is 1, it means that the next transmit descriptor is not occupied by TxDMA, and TxDMA will enter the pause (suspend) state. In this case, it is necessary to reconfigure the ownership of the descriptor and initiate a query request command to exit the pause (suspend) state. Refer to the description of relevant steps in Section 25.4.8.3.5. 0: TDES0.OWN of the next transmit descriptor is 1. 1: TDES0.OWN of the next transmit descriptor is 0.
1	TPSS	Transmit process stop status 0: Transmit process no stop. 1: Transmit process enters stop state.
0	TI	Transmit status. When this bit is set to 1, TDES0.OWN of the first descriptor is also set to 1. 0: Frame transmission has not yet been completed. 1: Frame transmission has been completed.

25.5.48 ETH DMA Operation Mode Register (ETH_DMAOPMOD)

Address offset: 0x1018

Reset value: 0x0000 0000

This register sets the working mode and command for receiving and sending. This register should be written last in the entire DMA initialization process.



Bit field	Name	Description
31:27	Reserved	Reserved, the reset value must be maintained.

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Bit field	Name	Description
26	DT	Do not drop TCP/IP checksum error frames. 0: If ETH_DMAOPMOD.FEF is 0, MAC discards all erroneous frames. 1: If the received frame has only checksum errors, MAC will not discard the frame.
25	RSF	Receive store-and-forward. 0: RxFIFO works in cut-through (threshold) mode, and the forwarding threshold is determined by these bits of ETH_DMAOPMOD.RTC[1:0]. 1: RxFIFO works in store-and-forward mode. Only after the frame is completely written to RxFIFO, RxDMA will forward it to the application, and the value of ETH_DMAOPMOD.RTC will be ignored.
24	DFF	Do not clear received frames. 0: When the receive descriptor is not available (or the receive buffer is not available), the RxDMA empties the receive frame in the RxFIFO. 1: RxDMA does not clear receive frames, even if receive descriptors are not available (or receive buffers are not available).
23:22	Reserved	Reserved, the reset value must be maintained.
21	TSF	Transmit store-and-forward. 0: TxFIFO works in cut-through (threshold) mode, and the transmit threshold is determined by these bits of ETH_DMAOPMOD.TTC[2:0]. 1: TxFIFO works in store-and-forward mode. Only after the frame is completely written to TxFIFO, MAC will transmit it out. At this time, the value of ETH_DMAOPMOD.TTC will be ignored. *Note: This bit can only be modified when the transmission is stopped.*
20	FTF	Clear TxFIFO. When this bit is set to 1, TxFIFO control logic is reset to its initial state, so that all data in the TxFIFO is emptied/lost. This bit is automatically cleared to 0 after the clear operation is complete. Writing to this register is not allowed until this bit is 0.
19:17	Reserved	Reserved, the reset value must be maintained.
16:14	TTC[2:0]	Transmit threshold control. These bits control the threshold of TxFIFO in cut-through (threshold) mode. These bits are ignored when ETH_DMAOPMOD.TSF = 1. 000: 64 001: 128 010: 192 011: 256 100: 40 101: 32 110: 24 111: 16
13	ST	Start/stop transmission. 0: After the current frame is transmit or TxDMA enters the pause (suspend) state, the transmit process enters stop mode. Holds the position of the next transmit descriptor in the transmit descriptor queue, which becomes the current descriptor when the transfer resumes.

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Bit field	Name	Description
		1: Transmit process enters running state. TxDMA obtains the current transmit descriptor, and the transmit frame descriptor can be obtained from the ETH_DMATXDLADDR base address. If the last transmission was stopped, it can also be obtained from the pointer position of the transmit descriptor queue. If the TDES0.OWN of the current descriptor is 0, the TxDMA enters suspend (suspended) state and sets ETH_DMASTS.TU to 1. *Note: Unpredictable consequences may occur if this bit is set before other DMA registers have been set.*
12:8	Reserved	Reserved, the reset value must be maintained.
7	FEF	Forward error frames. 0: When RxFIFO is operating in cut-through (threshold) mode, if a framing error (CRC error, collision error, checksum error, watchdog timeout, overflow) is detected before forwarding the RxFIFO data to memory, RxFIFO will discard this wrong frame. But if a frame error is detected after the RxFIFO data has been forwarded to memory, the frame will not be discarded. When RxFIFO works in store-and-forward mode, once a frame error is detected during reception, the frame will be discarded. 1: All frames except too short frames are forwarded to DMA.
6	FUF	Forward "good" frames of insufficient length. 0: RxFIFO discards all frames less than 64 bytes in length, but will forward frames if they start to be forwarded to the application before too short frames are detected (e.g. in cut-through (threshold) mode, frame length is less than the receive threshold) whole frame. 1: RxFIFO forwards "good" frames with insufficient length (frame length less than 64 bytes but no errors) to the application.
5	Reserved	Reserved, the reset value must be maintained.
4:3	RTC[1:0]	Receive threshold control. These bits control the threshold of the RxFIFO in cut-through (threshold) mode. 00: 64 01: 32 10: 96 11: 128 *Note: These bits are only valid when ETH_DMAOPMOD.RSF is 0.*
2	OSF	Operation second frame. 0: TxDMA starts to transmit the data of the next frame only after receiving the transmission status information of the previous frame. 1: TxDMA starts to transmit the data of the next frame after the data of the previous frame is all stored in the TxFIFO and before receiving the transmission status information of the previous frame.
1	SR	Start/stop receive. 0: RxDMA enters stop mode after forwarding the current received frame. Holds the position of the next receive descriptor in the receive descriptor queue, which becomes the current descriptor when the transfer resumes. "Stop receive" can only be done while reception is running or when reception is paused.

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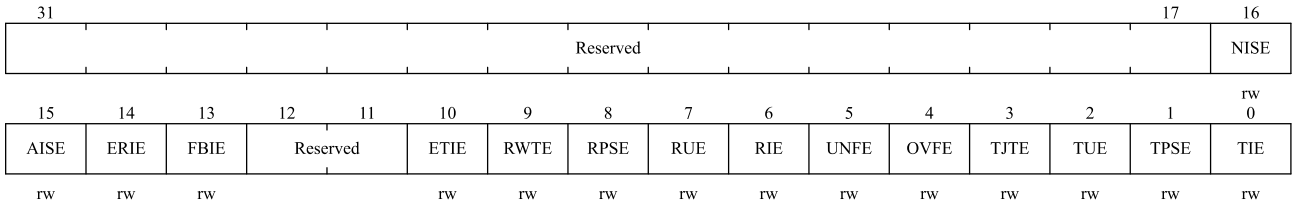
Bit field	Name	Description
		1: Put the receiving process into the running state, and the DMA checks the current position of the receiving descriptor queue to process the next received frame. The receiving frame descriptor can be obtained from the base address of ETH_DMARXDLADDR, or from the pointer position of the receiving descriptor queue if the last receiving was stopped. If the RDES0.OWN of the current descriptor is 0, then the receiving process enters the suspended (suspended) state and sets the ETH_DMASTS.RU bit to 1. The "Start receive" command is valid only when reception is stopped or when reception is paused. *Note: Unpredictable consequences may occur if the "Start Receive" command is issued before all other DMA registers have been set.*
0	Reserved	Reserved, the reset value must be maintained.

25.5.49 ETH DMA Interrupt Enable Register (ETH_DMAINTEN)

Address offset: 0x101C

Reset value: 0x0000 0000

For Ethernet interrupts, the interrupt will only occur if ETH_DMASTS.TTI or ETH_DMASTS.PMTI is 1 and the corresponding interrupt is not masked, or if ETH_DMASTS.NIS or ETH_DMASTS.AIS is set to 1 and the corresponding interrupt is enabled.



Bit field	Name	Description
31:17	Reserved	Reserved, the reset value must be maintained.
16	NISE	Normal interrupt summary enabled. 0: Mask normal interrupt. 1: Enable normal interrupt. This bit enables the following bits: • ETH_DMASTS[0]: Transmit interrupt • ETH_DMASTS[2]: Transmit buffer unavailable • ETH_DMASTS[6]: Receive interrupt • ETH_DMASTS[14]: Early receive interrupt
15	AISE	Abort summary enable. 0: Mask abnormal interrupt. 1: Enable exception interrupt. This bit enables the following bits: • ETH_DMASTS[1]: Transmit process stop • ETH_DMASTS[3]: Transmit Jabber timeout • ETH_DMASTS[4]: Receive overflow

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Bit field	Name	Description
		• ETH_DMASTS[5]: Transmit underflow • ETH_DMASTS[7]: Receive buffer unavailable • ETH_DMASTS[8]: Receive process stop • ETH_DMASTS[9]: Receive watchdog timeout • ETH_DMASTS[10]: Early transmit interrupt • ETH_DMASTS[13]: Bus fatal error
14	ERIE	Early receive interrupt enable. 0: Mask early receive interrupt. 1: When ETH_DMAINTEN.NISE is 1, enable early receive interrupt.
13	FBIE	Bus fatal error interrupt enable. 0: Mask bus fatal error interrupt. 1: When ETH_DMAINTEN.AISE is 1, enable bus fatal error interrupt.
12:11	Reserved	Reserved, the reset value must be maintained.
10	ETIE	Early transmit interrupt enable. 0: Mask early transmit interrupt. 1: When ETH_DMAINTEN.AISE is 1, enable early transmit interrupt.
9	RWTE	Receive watchdog timeout interrupt enable. 0: Mask receive watchdog timeout interrupt. 1: When ETH_DMAINTEN.AISE is 1, enable receive watchdog timeout interrupt.
8	RPSE	Receive process stop interrupt enable. 0: Mask receive process stop interrupt. 1: When ETH_DMAINTEN.AISE is 1, enable receive process stop interrupt.
7	RUE	Receive buffer unavailable interrupt enable. 0: Mask receive buffer unavailable interrupt. 1: When ETH_DMAINTEN.AISE is 1, enable receive buffer unavailable interrupt.
6	RIE	Receive interrupt enable. 0: Mask receive interrupt. 1: When ETH_DMAINTEN.NISE is 1, enable receive interrupt.
5	UNFE	Transmit underflow interrupt enable. 0: Mask transmit underflow interrupt. 1: When ETH_DMAINTEN.AISE is 1, enable transmit underflow interrupt.
4	OVFE	Receive overflow interrupt enable. 0: Mask receive overflow interrupt. 1: When ETH_DMAINTEN.AISE is 1, enable receive overflow interrupt.
3	TJTE	Transmit Jabber timeout interrupt enable. 0: Mask transmit Jabber timeout interrupt. 1: When ETH_DMAINTEN.AISE is 1, enable transmit Jabber timeout interrupt.
2	TUE	Transmit buffer unavailable interrupt enable. 0: Mask transmit buffer unavailable interrupt. 1: When ETH_DMAINTEN.NISE is 1, enable transmit buffer unavailable interrupt.
1	TPSE	Transmit process stop interrupt enable 0: Mask transmit process to stop the interrupt. 1: When ETH_DMAINTEN.AISE is 1, enable transmit process stop interrupt.

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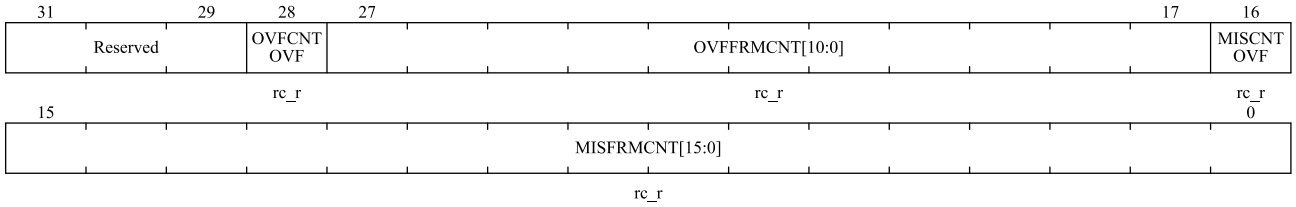
Bit field	Name	Description
0	TIE	Transmit interrupt enable. 0: Mask transmit interrupt. 1: When ETH_DMAINTEN.NISE is 1, enable transmit interrupt.

25.5.50 ETH DMA Missed Frames and Buffer Overflow Counter Register (ETH_DMAMFBOCNT)

Address offset: 0x1020

Reset value: 0x0000 0000

Ethernet DMA has 2 counters to count the number of frames lost during reception. The current value of the counter can be obtained by reading this register. This counter is often used for troubleshooting.



Bit field	Name	Description
31:29	Reserved	Reserved, the reset value must be maintained.
28	OVFCNTOVF	FIFO overflow counter overflow bit.
27:17	OVFFRMCNT[10:0]	Frames missed by application. These bits indicate the number of frames missed by the RxFIFO.
16	MISCNTOVF	Missed frame counter overflow bit.
15:0	MISFRMCNT[15:0]	Frames missed by controller. These bits indicate the number of frames missed by RxDMA due to the unavailability of the MCU's receive buffer. This counter is incremented by 1 each time the DMA clears an incoming frame.

25.5.51 ETH DMA Current Transmit Descriptor Address Register (ETH_DMACHTXDESC)

Address offset: 0x1048

Reset value: 0x0000 0000

This register points to the start address (base address) of the transmit descriptor that TxDMA is reading.

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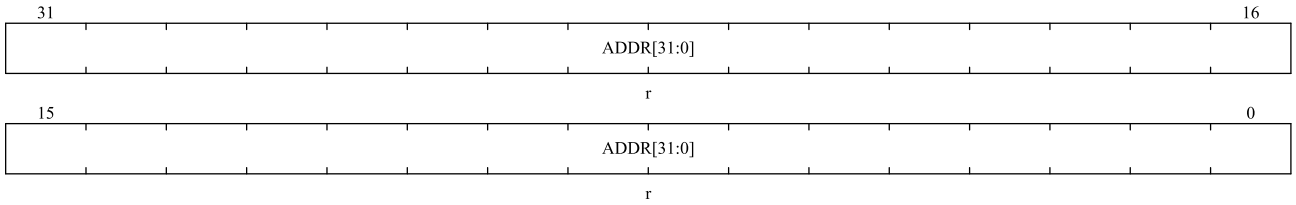


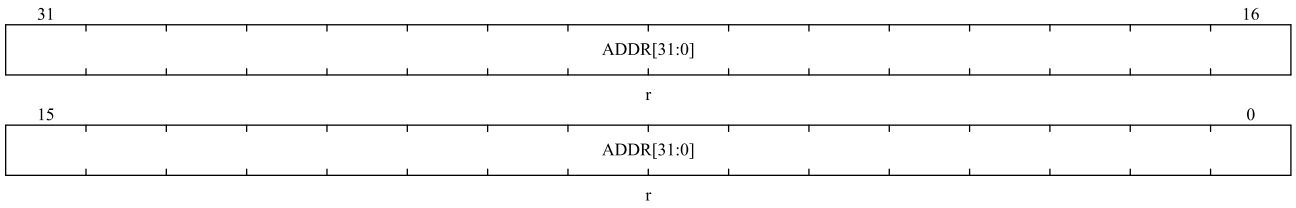
Bit field	Name	Description
31:0	ADDR[31:0]	Transmit descriptor address pointer. These bits are cleared on reset and are automatically updated by TxDMA during operation.

25.5.52 ETH DMA Current Receive Descriptor Address Register (ETH_DMACHRXDESC)

Address offset: 0x104C

Reset value: 0x0000 0000

This register points to the start address (base address) of the receive descriptor that RxDMA is reading.



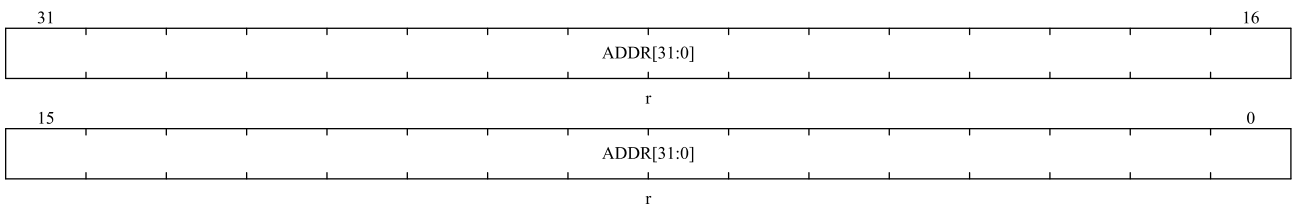
Bit field	Name	Description
31:0	ADDR[31:0]	Receive descriptor address pointer. These bits are cleared on reset and are automatically updated by RxDMA during operation.

25.5.53 ETH DMA Current Transmit Buffer Address Register (ETH_DMACHTXBADDR)

Address offset: 0x1050

Reset value: 0x0000 0000

This register points to the address of the transmit buffer that TxDMA is reading.



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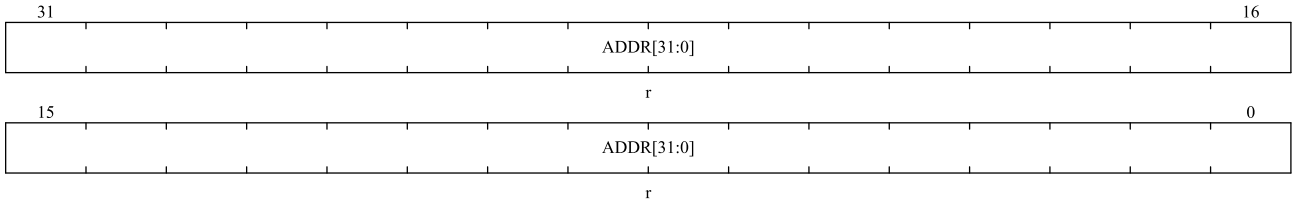
Bit field	Name	Description
31:0	ADDR[31:0]	Transmit buffer address pointer. These bits are cleared on reset and updated by TxDMA during operation.

25.5.54 ETH DMA Current Receive Buffer Address Register (ETH_DMACHRXBADDR)

Address offset: 0x1054

Reset value: 0x0000 0000

This register points to the address of the receive buffer that RxDMA is reading.



Bit field	Name	Description
31:0	ADDR[31:0]	Receive buffer address pointer. These bits are cleared on reset and updated by RxDMA during operation.

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26 Comparator (COMP)

The COMP module is used to compare the analog voltages of two inputs and output high/low levels based on the comparison results. When "INP" input voltage is higher than "INM" input voltage, the comparator output is high level, when "INP" input voltage is lower than "INM" input voltage, the comparator output is low level.

26.1 COMP System Connection Block Diagram

The COMP module supports a maximum of seven independent comparators, which are connected to the APB1 bus..

Figure 26-1 Comparator1 and comparator2 connection diagram

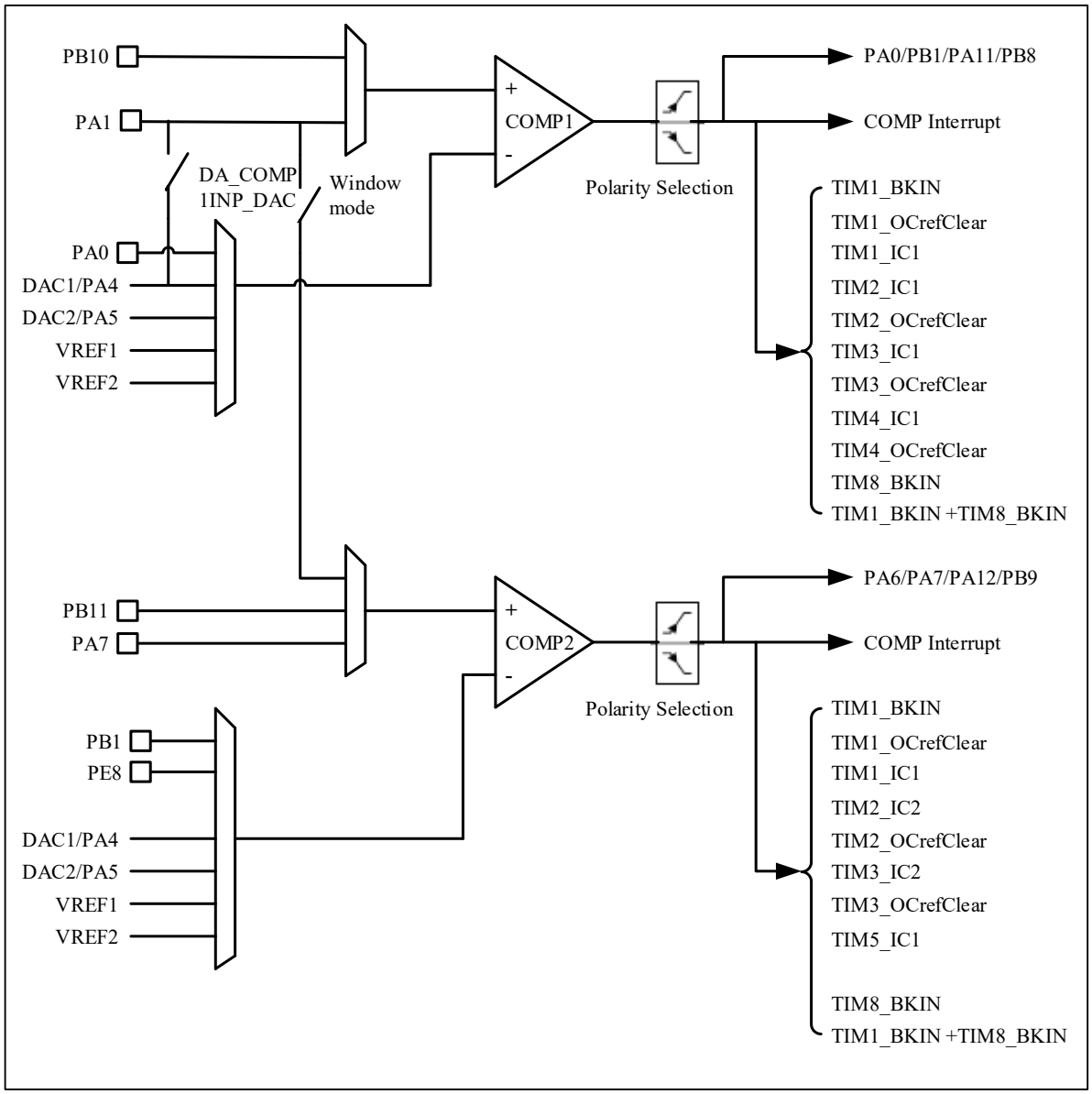

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Figure 26-2 Comparator3 and comparator4 connection diagram

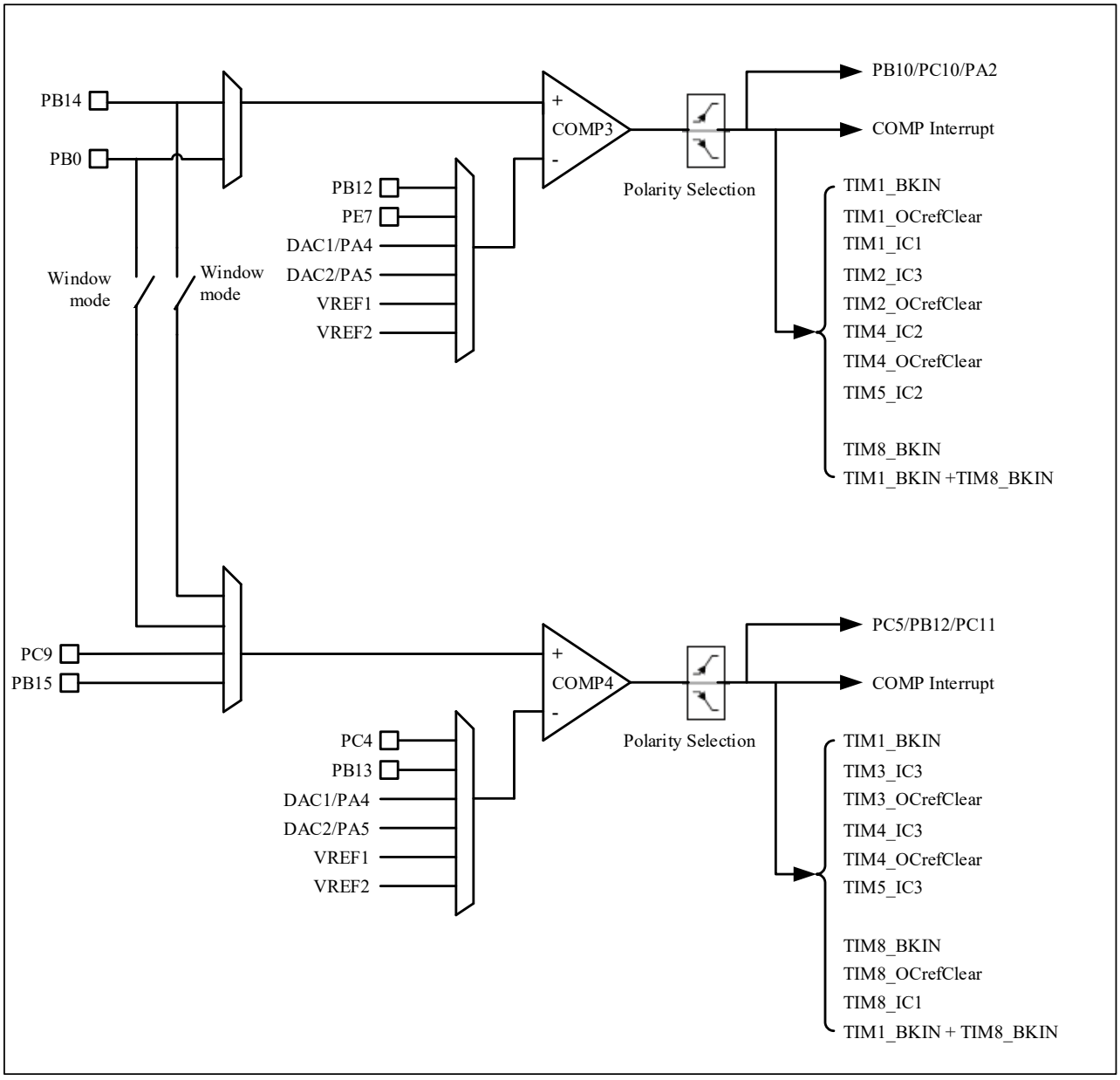

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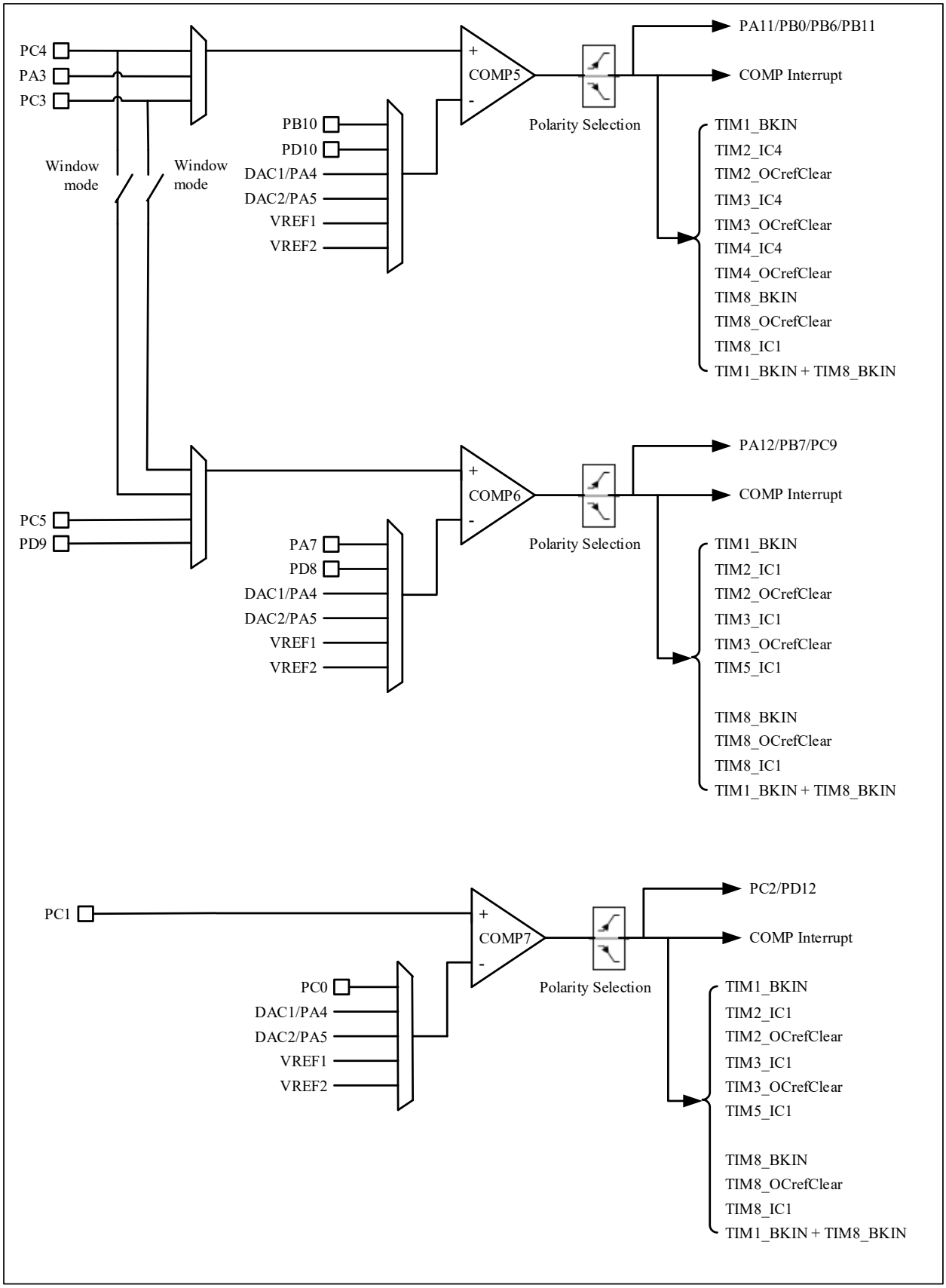
Figure 26-3 Comparator5,Comparator6,comparator7 connection diagram



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26.2 Main Features

- Up to 7 independent comparators.
- Built-in two 64 level programmable comparison voltage reference sources VREF1, VREF2.
- Support filter clock, filter reset.
- Output polarity can be configured high and low.
- Hysteresis The value can be none, low, medium, or high.
- The comparison result can be output to the I/O port or trigger timer, which is used to capture events, OCREF_CLR events, brake events, and generate interrupts.
- Input channels can check I/O ports, channel outputs of DAC, VREF1, VREF2.
- It can be read - only or read - write, and can be unlocked only after a reset.
- Blanking support, Blanking source can be configured to produce Blanking.
- COMP1/COMP2, COMP3/COMP4, COMP5/COMP6 can form window comparators.
- You can wake the system from Sleep mode or STOP0 mode by generating an interrupt.
- Filter window size can be configured.
- Filter threshold size can be configured.
- The sampling frequency for filtering can be configured.

26.3 COMP Configuration Process

Complete configuration items are as follows. If the default configuration is used, skip the corresponding configuration items.

1. Configurable hysteresis level COMPx_CTRL.HYST[1:0]
2. Configure the output polarity COMPx_CTRL.POL
3. Configuration input selection, comparator non-inverting input COMPx_CTRL.INPSEL[3:0], inverting input COMPx_CTRL. INMSEL [2:0]
4. Select COMPx_CTRL.OUTSEL[3:0]for configuration output
5. Configure the blanking source COMPx_CTRL.BLKING[2:0]
6. Configure the comparator window mode COMP_WINMODE. CMP12MD
7. Configure the filter sampling window COMPx_FILC.SAMPW[4:0]
8. Configure the threshold COMPx_FILC.THRESH[4:0] (threshold should be greater than COMPx_FILC.SAMPW[4:0]/2)
9. Configure the filter sampling frequency (for timer applications, sampling frequency should be greater than 5MHz)
10. Enable COMPx_FILC.FILEN filter

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11. Enable COMPx_CTRL.EN on the comparator

Note: For the above steps, the filter should be enabled first and then the comparator should be enabled. The comparator should be enabled after the filtering (if enabled) is configured and enabled. In addition, when the comparator control register is locked, the LOCK can be cancelled only through reset.

26.4 COMP Working Mode

26.4.1 Window Mode

The comparators can be combined into 3 window comparators as follows:

- Comparator 1 and comparator 2 share PA1 to form window comparators.
- Comparator 3 and comparator 4 share PB14 or PB0 to form window comparators.
- Comparator 5 and comparator 6 share PC3 or PC4 to form window comparators.

26.4.2 Independent Comparator

The seven comparators can be configured independently to complete the comparator function. The output of a comparator can be output to an I/O port. Each comparator has a different remapped port. You can configure the comparator register COMPx_CTRL. OUTSEL[3:0] to enable the corresponding feature pin at the output.

Comparator output, support trigger events, such as can be configured as timer 1, timer 8 brake function.

Note: Refer to the comparator interconnection for specific configuration

26.5 Comparator Interconnection

For the interconnection of the output port of the comparator, please refer to the AFIO register chapter, which defines the value of the remapping of the comparator OUT.

OUT	COMP1[1:0]	COMP2[3:2]	COMP3[5:4]	COMP4[7:6]	COMP5[9:8]	COMP6[11:10]	COMP7[12]
00	PA0	PA6	PB10	PC5	PB0	PC9	PC2
01	PB1	PA7	PC10	PB12	PB11	PA12	PD12
10	PA11	PA12	Not Used	Not Used	PB6	Not Used	--
11	PB8	PB9	PA2	PC11	PA11	PB7	--

Notes:

1. *COMP7 has only 1 bit to control output remapping.*
2. *After COMP1, COMP2, COMP5, and COMP7 are enabled, the IO ports corresponding to COMP1_OUT, COMP2_OUT, COMP5_OUT, and COMP7_OUT cannot be configured as the output mode of other peripherals, but can be the input mode of other peripherals, GPIO input, GPIO output.*

The comparator INP pin has the following configuration.

INPSEL	COMP1	COMP2	COMP3	COMP4	COMP5	COMP6	COMP7
000	PA1	PA1	PB14	PB14	PC4	PC4	PC1
001	PB10	PB11	PB0	PB0	PC3	PC3	--

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010	--	PA7	--	PC9	PA3	PC5	--
011	--	--	--	PB15	--	PD9	--
100	--	--	--	--	--	--	--
Other	--	--	--	--	--	--	--

The comparator INM pins have the following configuration.

INMSEL	COMP1	COMP2	COMP3	COMP4	COMP5	COMP6	COMP7
000	PA0	PB1	PB12	PC4	PB10	PA7	PC0
001	DAC1/PA4	PE8	PE7	PB13	PD10	PD8	DAC1/PA4
010	DAC2/PA5	DAC1/PA4	DAC1/PA4	DAC1/PA4	DAC1/PA4	DAC1/PA4	DAC2/PA5
011	VREF1	DAC2/PA5	DAC2/PA5	DAC2/PA5	DAC2/PA5	DAC2/PA5	VREF1
100	VREF2	VREF1	VREF1	VREF1	VREF1	VREF1	VREF2
101	--	VREF2	VREF2	VREF2	VREF2	VREF2	--
Other	--	--	--	--	--	--	--

Comparator output TRIG signal has the following interconnection.

TRIG	COMP1	COMP2	COMP3	COMP4	COMP5	COMP6	COMP7
0000	NC	NC	NC	NC	NC	NC	NC
0001	TIM1_BKIN	TIM1_BKIN	TIM1_BKIN	TIM1_BKIN	TIM1_BKIN	TIM1_BKIN	TIM1_BKIN
0010	TIM1_IC1	TIM1_IC1	TIM1_IC1	TIM3_IC3	TIM2_IC4	TIM2_IC1	TIM2_IC1
0011	TIM1_OCrefclear	TIM1_OCrefclear	TIM1_OCrefclear	TIM3_OCrefclear	TIM2_OCrefclear	TIM2_OCrefclear	TIM2_OCrefclear
0100	TIM2_IC1	TIM2_IC2	TIM2_IC3	TIM4_IC3	TIM3_IC4	TIM3_IC1	TIM3_IC1
0101	TIM2_OCrefclear	TIM2_OCrefclear	TIM2_OCrefclear	TIM4_OCrefclear	TIM3_OCrefclear	TIM3_OCrefclear	TIM3_OCrefclear
0110	TIM3_IC1	TIM3_IC2	TIM4_IC2	TIM5_IC3	TIM4_IC4	TIM5_IC1	TIM5_IC1
0111	TIM3_OCrefclear	TIM3_OCrefclear	TIM4_OCrefclear	--	TIM4_OCrefclear	--	--
1000	TIM4_IC1	TIM5_IC1	TIM5_IC2	TIM8_IC1	TIM8_IC1	TIM8_IC1	TIM8_IC1
1001	TIM4_OCrefclear	--	--	TIM8_OCrefclear	TIM8_OCrefclear	TIM8_OCrefclear	TIM8_OCrefclear
1010	TIM8_BKIN	TIM8_BKIN	TIM8_BKIN	TIM8_BKIN	TIM8_BKIN	TIM8_BKIN	TIM8_BKIN
1011	TIM1_BKIN + TIM8_BKIN	TIM1_BKIN + TIM8_BKIN	TIM1_BKIN + TIM8_BKIN	TIM1_BKIN + TIM8_BKIN	TIM1_BKIN + TIM8_BKIN	TIM1_BKIN + TIM8_BKIN	TIM1_BKIN + TIM8_BKIN
Other	--	--	--	--	--	--	--

26.6 Interrupt

COMP supports interrupt response, and COMP1, COMP1, COMP2, COMP3 share one interrupt entry , COMP4, COMP5, and COMP6 share one interrupt entry, , COMP7 has one interrupt entry exclusively. There are two cases of interrupt generation as follows.

- The polarity of COMPx_CTRL.POL is not reversed, and the interrupt is enabled. When INPSEL > INMSEL, the comparator interrupt will be generated when COMPx_CTRL.OUT is set to 1 by hardware.

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- The polarity of COMPx_CTRL.POL is reversed, and the interrupt is enabled. When INPSEL < INMSEL, the comparator interrupt is generated when COMPx_CTRL.OUT is set to 1 by hardware.

26.7 COMP Register

26.7.1 COMP register overview

Table 26-1 COMP register overview

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
010h	COMP1_CTRL	Reserved													INPDAC	OUT	BLKING[2:0]			HYST[1:0]		POL	OUTSEL[3:0]				INPSEL[2:0]			INMSEL[2:0]			EN
	Reset Value														0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
014h	COMP1_FILC	Reserved																					SAMPW[4:0]					THRESH[4:0]					FILEN
	Reset Value																						0	0	0	0	0	0	0	0	0	0	0
018h	COMP1_FILP	Reserved																CLKPSC[15:0]															
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
01Ch	Reserved																																
020h	COMP2_CTRL	Reserved													INPDAC	OUT	BLKING[2:0]			HYST[1:0]		POL	OUTSEL[3:0]				INPSEL[2:0]			INMSEL[2:0]			EN
	Reset Value														0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
024h	COMP2_FILC	Reserved																					SAMPW[4:0]					THRESH[4:0]					FILEN
	Reset Value																						0	0	0	0	0	0	0	0	0	0	0
028h	COMP2_FILP	Reserved																CLKPSC[15:0]															
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
02Ch	Reserved																																
030h	COMP3_CTRL	Reserved													INPDAC	OUT	BLKING[2:0]			HYST[1:0]		POL	OUTSEL[3:0]				INPSEL[2:0]			INMSEL[2:0]			EN
	Reset Value														0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
034h	COMP3_FILC	Reserved																					SAMPW[4:0]					THRESH[4:0]					FILEN
	Reset Value																						0	0	0	0	0	0	0	0	0	0	0
038h	COMP3_FILP	Reserved																CLKPSC[15:0]															
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
03Ch	Reserved																																

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Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
040h	COMP4_CTRL	Reserved													INPDAC	OUT	BLKING[2:0]			HYST[1:0]		POL	OUTSEL[3:0]				INPSEL[2:0]			INMSEL[2:0]			EN
	Reset Value														0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
044h	COMP4_FILC	Reserved																					SAMPW[4:0]					THRESH[4:0]					FILEN
	Reset Value																						0	0	0	0	0	0	0	0	0	0	0
048h	COMP4_FILP	Reserved																CLKPSC[15:0]															
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
04Ch	Reserved																																
050h	COMP5_CTRL	Reserved													INPDAC	OUT	BLKING[2:0]			HYST[1:0]		POL	OUTSEL[3:0]				INPSEL[2:0]			INMSEL[2:0]			EN
	Reset Value														0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
054h	COMP5_FILC	Reserved																					SAMPW[4:0]					THRESH[4:0]					FILEN
	Reset Value																						0	0	0	0	0	0	0	0	0	0	0
058h	COMP5_FILP	Reserved																CLKPSC[15:0]															
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
05Ch	Reserved																																
060h	COMP6_CTRL	Reserved													INPDAC	OUT	BLKING[2:0]			HYST[1:0]		POL	OUTSEL[3:0]				INPSEL[2:0]			INMSEL[2:0]			EN
	Reset Value														0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
064h	COMP6_FILC	Reserved																					SAMPW[4:0]					THRESH[4:0]					FILEN
	Reset Value																						0	0	0	0	0	0	0	0	0	0	0
068h	COMP6_FILP	Reserved																CLKPSC[15:0]															
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
06Ch	Reserved																																
070h	COMP7_CTRL	Reserved													INPDAC	OUT	BLKING[2:0]			HYST[1:0]		POL	OUTSEL[3:0]				INPSEL[2:0]			INMSEL[2:0]			EN
	Reset Value														0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
074h	COMP7_FILC	Reserved																					SAMPW[4:0]					THRESH[4:0]					FILEN
	Reset Value																						0	0	0	0	0	0	0	0	0	0	0
078h	COMP7_FILP	Reserved																CLKPSC[15:0]															
	Reset Value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
07Ch	Reserved																																

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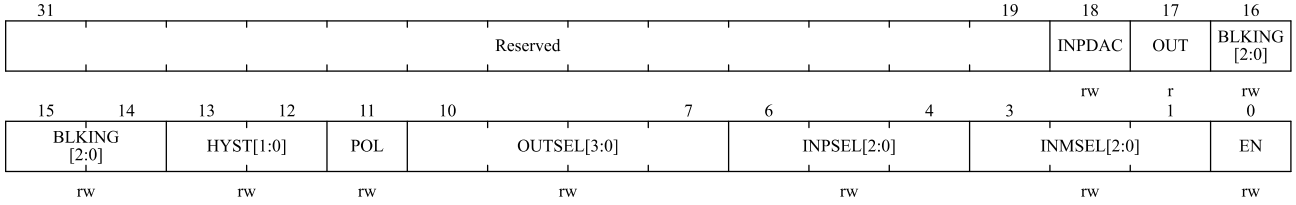
Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
080h	COMP_WINMODE	Reserved																													CMP56MD	CMP34MD	CMP12MD
	Reset Value																														0	0	0
084h	COMP_LOCK	Reserved																										CMP6LK	CMP5LK	CMP4LK	CMP3LK	CMP2LK	CMP1LK
	Reset Value																											0	0	0	0	0	0
088h	Reserved																																
08Ch	COMP_INTEN	Reserved																									CMP6IEN	CMP5IEN	CMP4IEN	CMP3IEN	CMP2IEN	CMP1IEN	CMP0IEN
	Reset Value																										0	0	0	0	0	0	0
090h	COMP_INTSTS	Reserved																									CMP7IS	CMP6IS	CMP5IS	CMP4IS	CMP3IS	CMP2IS	CMP1IS
	Reset Value																										0	0	0	0	0	0	0
094h	COMP_VREFSCL	Reserved																		VV2TRM[5:0]						VV2EN	VV1TRM[15:0]						VV1EN
	Reset Value																			0	0	0	0	0	0	0	0	0	0	0	0	0	0

26.7.2 COMP Control Register (COMPx_CTRL)

Comparator 1's INPDAC is valid, comparator 2 to comparator 7, the INPDAC bits are invalid.

Address offset : 0x10,0x20,0x30,0x40,0x50,0x60,0x70

Reset value : 0x0000 0000



Bit field	Name	Description
31:19	Reserved	Reserved, the reset value must be maintained
18	INPDAC	Connection selection of PA1 and DAC output at the non-inverting input of comparator 1 0: connect to PA1; 1: Connect to DAC output. *Note: Only COMP1 supports this bit.*
17	OUT	This read-only bit is a copy of comparator output state. 0: Output is low (non-inverting input below inverting input); 1: Output is high (non-inverting input above inverting input).
16：14	BLKING[2:0]	These bits select which Timer output controls the comparator output blanking. 000: No blanking; 001: TIM1 OC5 selected as blanking source; 010: TIM8 OC5 selected as blanking source.

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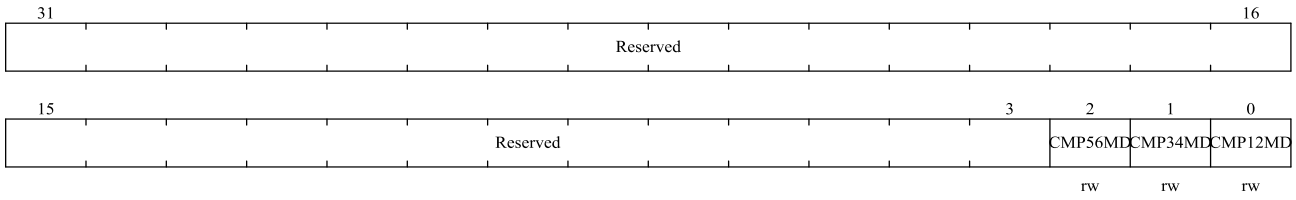
Bit field	Name	Description
		Other configurations: reserved.
13:12	HYST[1:0]	These bits control the hysteresis level. 00: No hysteresis; 01: Low hysteresis; 10: Medium hysteresis; 11: High hysteresis.
11	POL	This bit is used to invert the comparator output. 0: Output is not inverted; 1: Output is inverted.
10:7	OUTSEL[3:0]	Comparator output connection selection *Note: For the specific enumeration value correspondence, please refer to chapter 26.5"Comparator interconnection".*
6:4	INPSEL[2:0]	Comparator non-inverting input selection *Note: For the specific enumeration value correspondence, please refer to chapter 26.5"Comparator interconnection".*
3:1	INMSEL[2:0]	Comparator inverting input selection *Note: For the specific enumeration value correspondence, please refer to chapter 26.5"Comparator interconnection".*
0	EN	This bit switches COMP ON/OFF. 0: Comparator disabled; 1: Comparator enabled.

26.7.3 COMP Window Mode Register (COMP_WINMODE)

Address offset : 0x80

Reset value : 0x0000 0000



Bit field	Name	Description
31:3	Reserved	Reserved, the reset value must be maintained
2	CMP56MD	This bit selects window mode: the two non-inverting inputs of the comparator share the PC3 or PC4 input. 0: Comparators 5 and 6 are not in window mode; 1: Comparators 5 and 6 are in window mode.
1	CMP34MD	This bit selects window mode: the two non-inverting inputs of the comparator share the PB14 or PB0 input. 0: Comparators 3 and 4 are not in window mode; 1: Comparators 4 and 4 are in window mode.
0	CMP12MD	This bit selects window mode: the two non-inverting inputs of the comparator share the PA1

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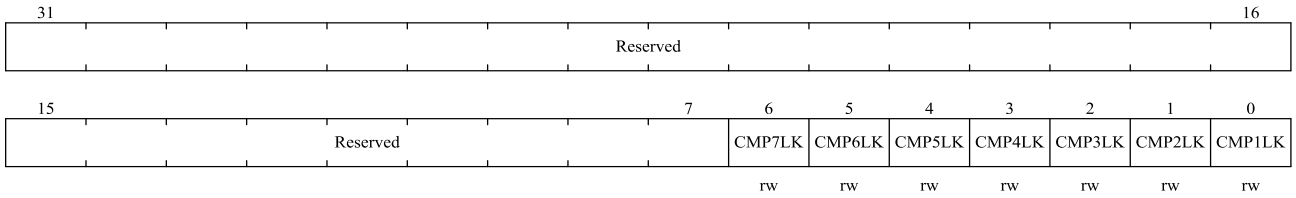
Bit field	Name	Description
		input. 0: Comparators 1 and 2 are not in window mode. 1: Comparators 1 and 2 are in window mode.

26.7.4 COMP Lock Register (COMP_LOCK)

Address offset : 0x84

Reset value : 0x0000 0000

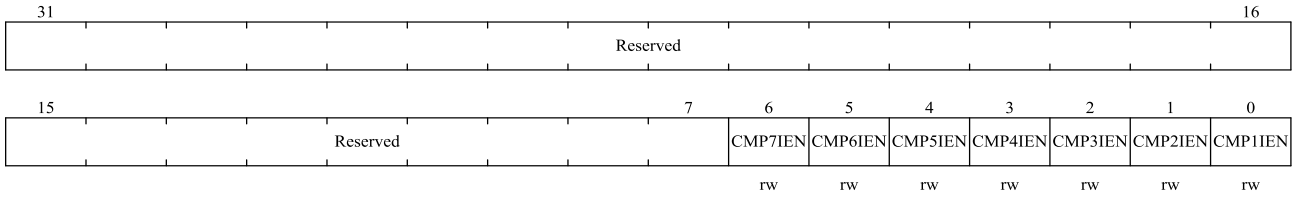


Bit field	Name	Description
31:7	Reserved	Reserved, the reset value must be maintained
6	CMP7LK	This bit is write-once. It is set by software. It can only be cleared by a system reset. If set it causes COMP7_CTRL register to be read-only. 0: COMP7_CTRL is read-write. 1: COMP7_CTRL is read-only
5	CMP6LK	Same function as CMP7LK.
4	CMP5LK	Same function as CMP7LK.
3	CMP4LK	Same function as CMP7LK.
2	CMP3LK	Same function as CMP7LK.
1	CMP2LK	Same function as CMP7LK.
0	CMP1LK	Same function as CMP7LK.

26.7.5 COMP Interrupt Enable Register (COMP_INTEN)

Address offset : 0x8C

Reset value : 0x0000 0000



Bit field	Name	Description
31:7	Reserved	Reserved, the reset value must be maintained
6	CMP7IEN	Software controlled Interrupt enable of COMP7. 0: Disable; 1: Enable. *Note: COMPx_CTRL.OUT high level triggers an interrupt.*

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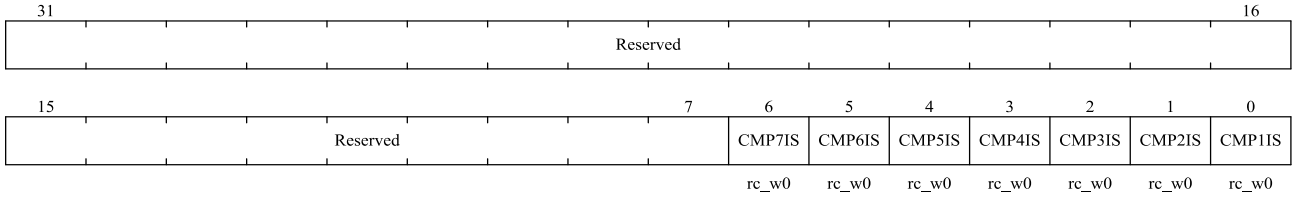
Bit field	Name	Description
5	CMP6IEN	Same function as CMP7IEN.
4	CMP5IEN	Same function as CMP7IEN.
3	CMP4IEN	Same function as CMP7IEN.
2	CMP3IEN	Same function as CMP7IEN.
1	CMP2IEN	Same function as CMP7IEN.
0	CMP1IEN	Same function as CMP7IEN.

26.7.6 COMP Interrupt Status Register (COMP_INTSTS)

Address offset : 0x90

Reset value : 0x0000 0000

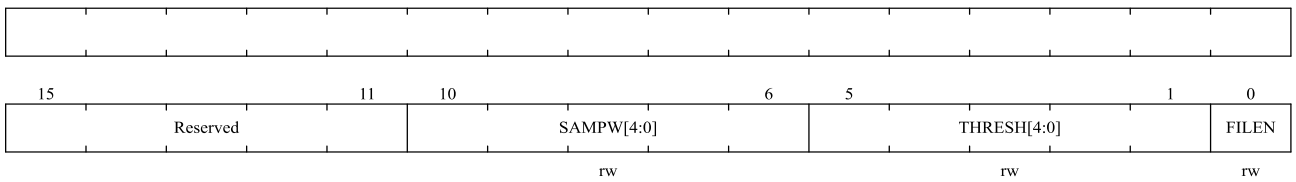


Bit field	Name	Description
31:7	Reserved	Reserved, the reset value must be maintained
6	COMP7IS	This bit indicate the interrupt status of COMP7,write 0 to clear.
5	COMP6IS	Same function as COMP7IS.
4	COMP5IS	Same function as COMP7IS.
3	COMP4IS	Same function as COMP7IS.
2	COMP3IS	Same function as COMP7IS.
1	COMP2IS	Same function as COMP7IS.
0	COMP1IS	Same function as COMP7IS.

26.7.7 COMP Filter Register (COMPx_FILC)

Address offset : 0x14,0x24,0x34,0x44,0x54,0x64,0x74

Reset value : 0x0000 0000



Bit field	Name	Description
31:11	Reserved	Reserved, the reset value must be maintained
10:6	SAMPW[4:0]	Filter sampling window size, sampling window = SAMPW + 1.
5:1	THRESH[4:0]	The filter threshold is set. At least the sampling threshold of the opposite state in the sample window can change the output state. This value is required to be greater than SAMPW / 2.
0	FILEN	Filter enable.

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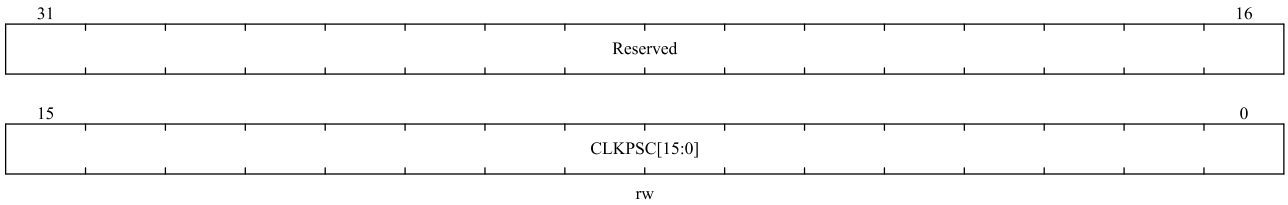
Bit field	Name	Description
		0: Disable 1: Enable

26.7.8 COMP Filter Frequency Division Register (COMPx_FILP)

Address offset : 0x18,0x28,0x38,0x48,0x58,0x68,0x78

Reset value : 0x0000 0000

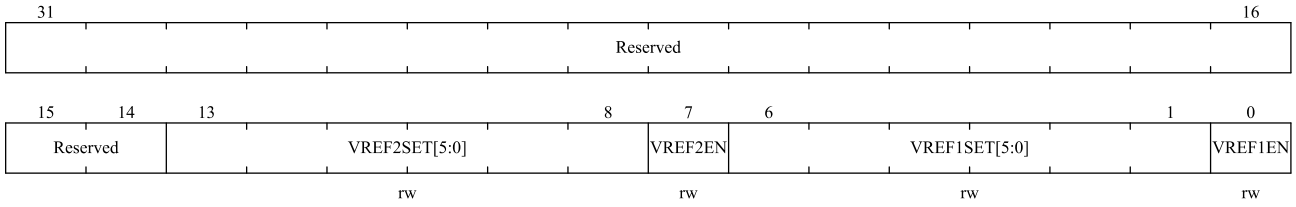


Bit field	Name	Description
31:16	Reserved	Reserved, the reset value must be maintained
15:0	CLKPSC[15:0]	Low filter sample clock prescale. System clock divider = CLK_PRE_CYCLE + 1, 0: Every cycle 1: Every 2 cycle 2: Every 3 cycle …

26.7.9 COMP Reference Voltage Register (COMP_VREFSCL)

Address offset : 0x94

Reset value : 0x0000 0000



Bit field	Name	Description
31:14	Reserved	Reserved, the reset value must be maintained
13:8	VREF2SET[5:0]	VREF2 voltage scaler trim value.
7	VREF2EN	VREF2 voltage scaler: 0: disable; 1: enable.
6:1	VREF1SET[5:0]	VREF1 voltage scaler trim value.
0	VREF1EN	VREF1 voltage scaler: 0: disable;

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Bit field	Name	Description
		1: enable.

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27 Operational Amplifier (OPAMP)

The OPAMP module can be flexibly configured, suitable for applications such as independent op amp mode , programmable gain amplifier and follower mode, The internal op-amps can be configured as combined amplifiers with different gains or cascaded using external resistors..OPAMP has an input range of 0V to VDDA and an output range of 0.1V to VDDA-0.1V.

27.1 Main Features

- Four independently configured operational amps
- Support track-to-track input, input range is 0 to VDDA, output range is 0.1V to VDDA-0.1V programmable gain
- The OPAMP can be configured as an instrument amplifier through an external resistor connection
- The following modes can be configured
  - Independent op amp mode
  - Voltage follower
  - Programmable gain amplifier
  - Differential op amp of two op amps
- Programmable gain settings are 2X, 4X, 8X, 16X, 32X times
- Gain bandwidth: 4MHz
- Support TIM1_CC6 to automatically switch the input PIN of OPAMP1 and OPAMP2, TIM8_CC6 to automatically switch the input PIN of OPAMP3 and OPAMP4
- Independent write protection is supported

27.1.1 OPAMP Function Description

The four OPAMPs can be configured for various PGA modes through register selection, and can also be configured for the user to use the OPAMP function of external components. The output of the OPAMP can be used as the channel input of the ADC, and the four OPAMP outputs are connected to the analog channels of the ADC as follows.

The output of OPAMP1 is connected to the analog input channel 3 of ADC1

The output of OPAMP2 is connected to the analog input channel 3 of ADC2

The output of OPAMP3 is connected to the analog input channel 1 of ADC3

The output of OPAMP4 is connected to the analog input channel 3 of ADC4

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Figure 27-1 Block diagram of OPAMP1 and OPAMP2 connection diagram

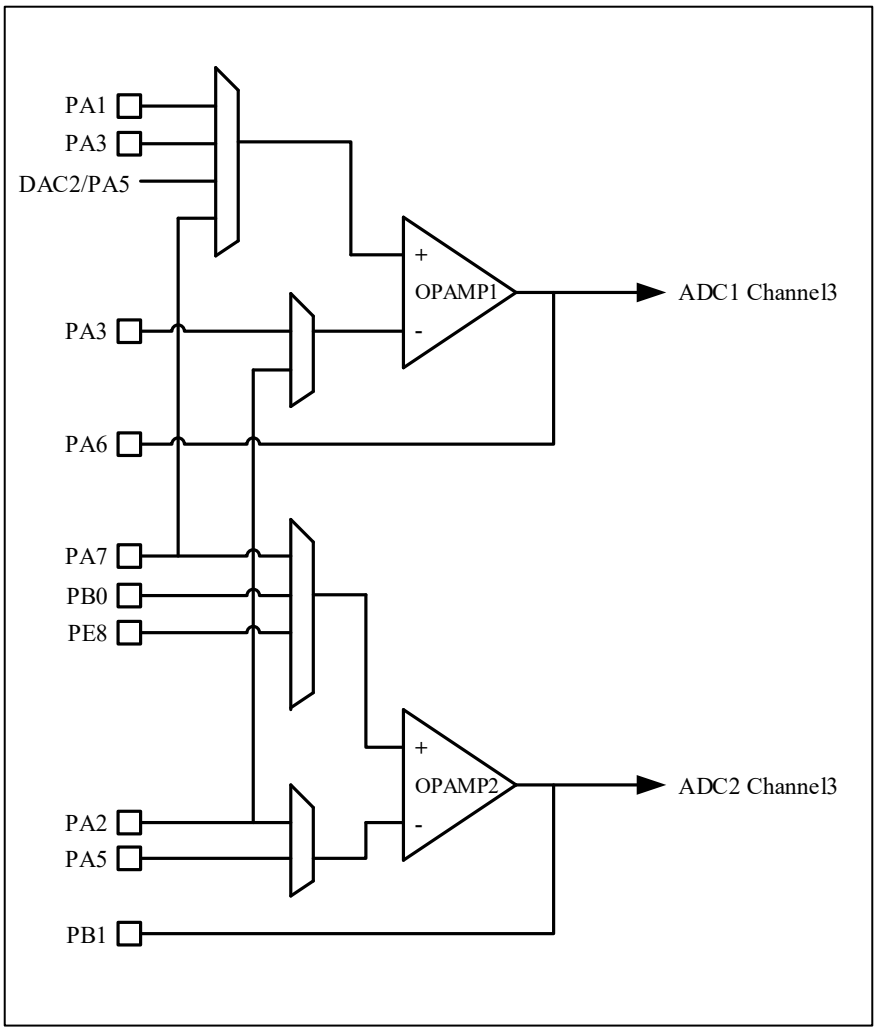

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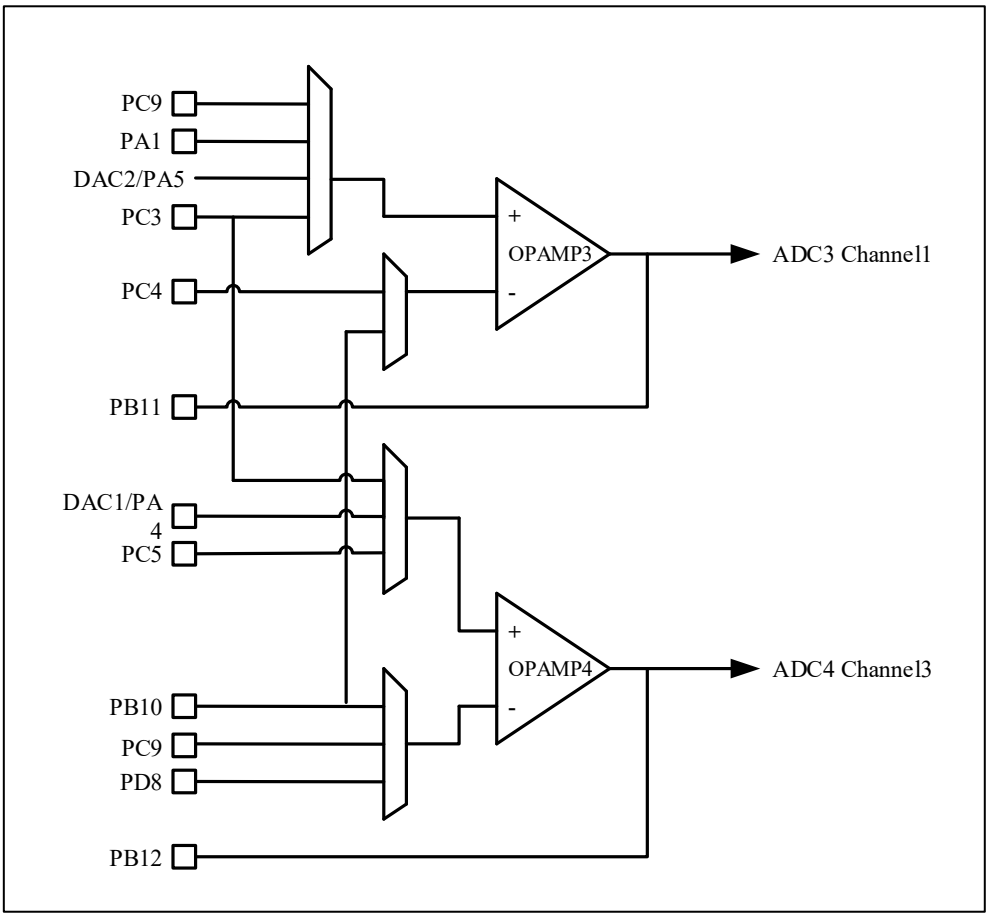
Figure 27-2 Block diagram of OPAMP3 and OPAMP4 connection diagram



27.1.2 Internal Connection Between OPAMP and COMP

OPAMP1, OPAMP2, COMP1, COMP2, COMP3, ADC1 and ADC2 constitute a group of analog linkage applications, and the topology relationship is as follows:

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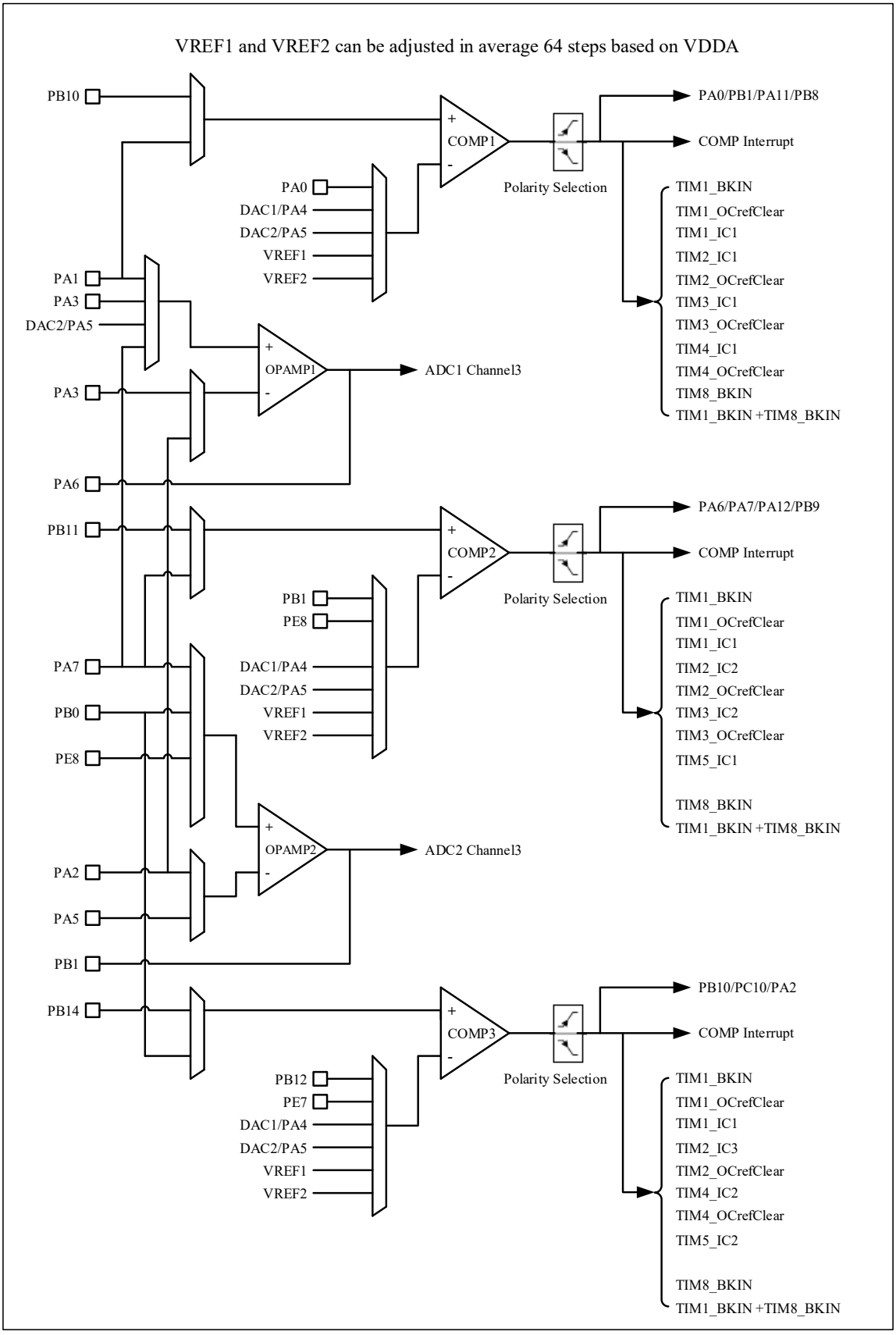
Figure 27-3 Simulation module linkage relationship 1



OPAMP3, OPAMP4, COMP4, COMP5, COMP6, ADC3 and ADC4 constitute a group of analog linkage applications, and the topology relationship is as follows:

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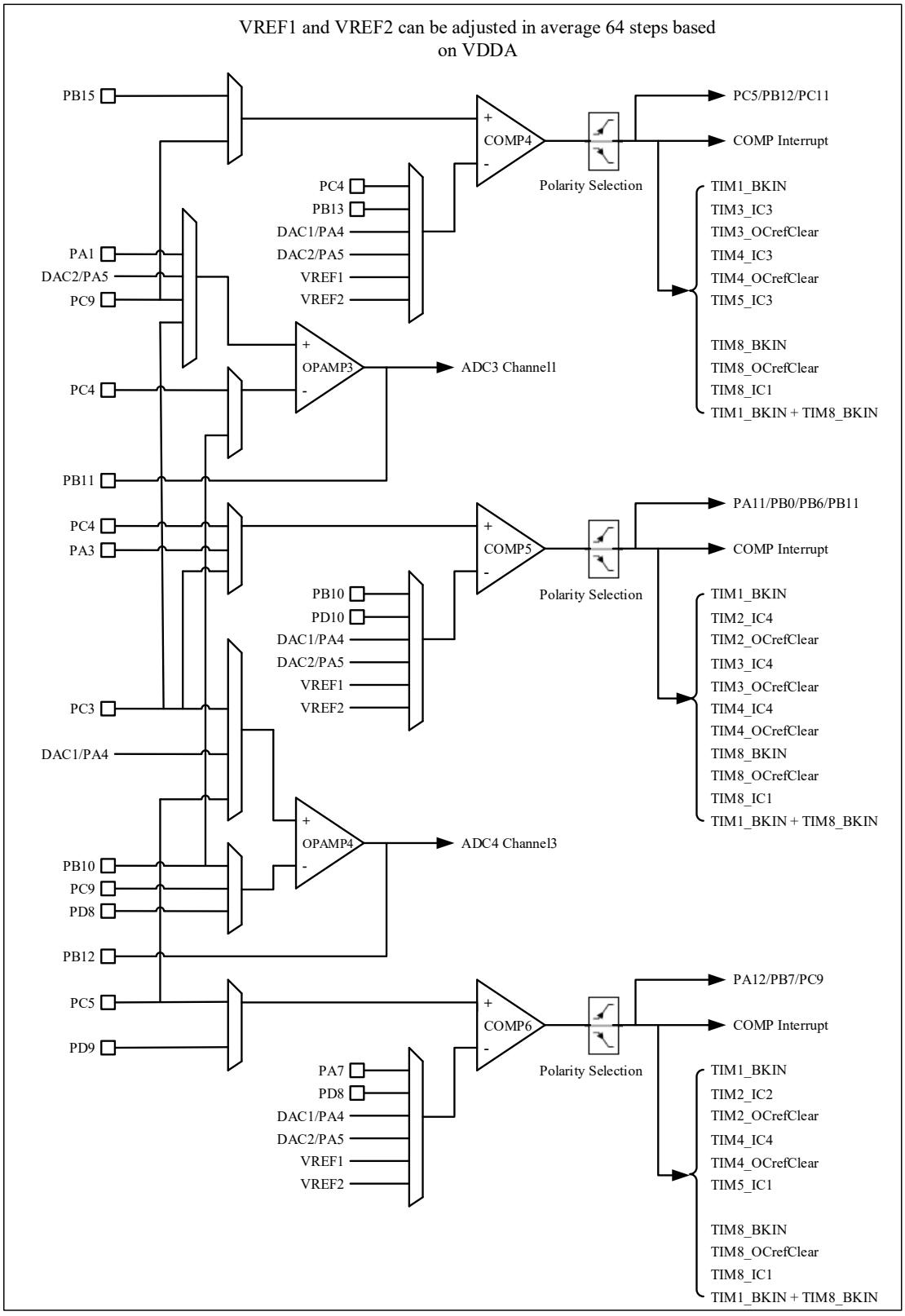
Figure 27-4 Simulation module linkage relationship 2



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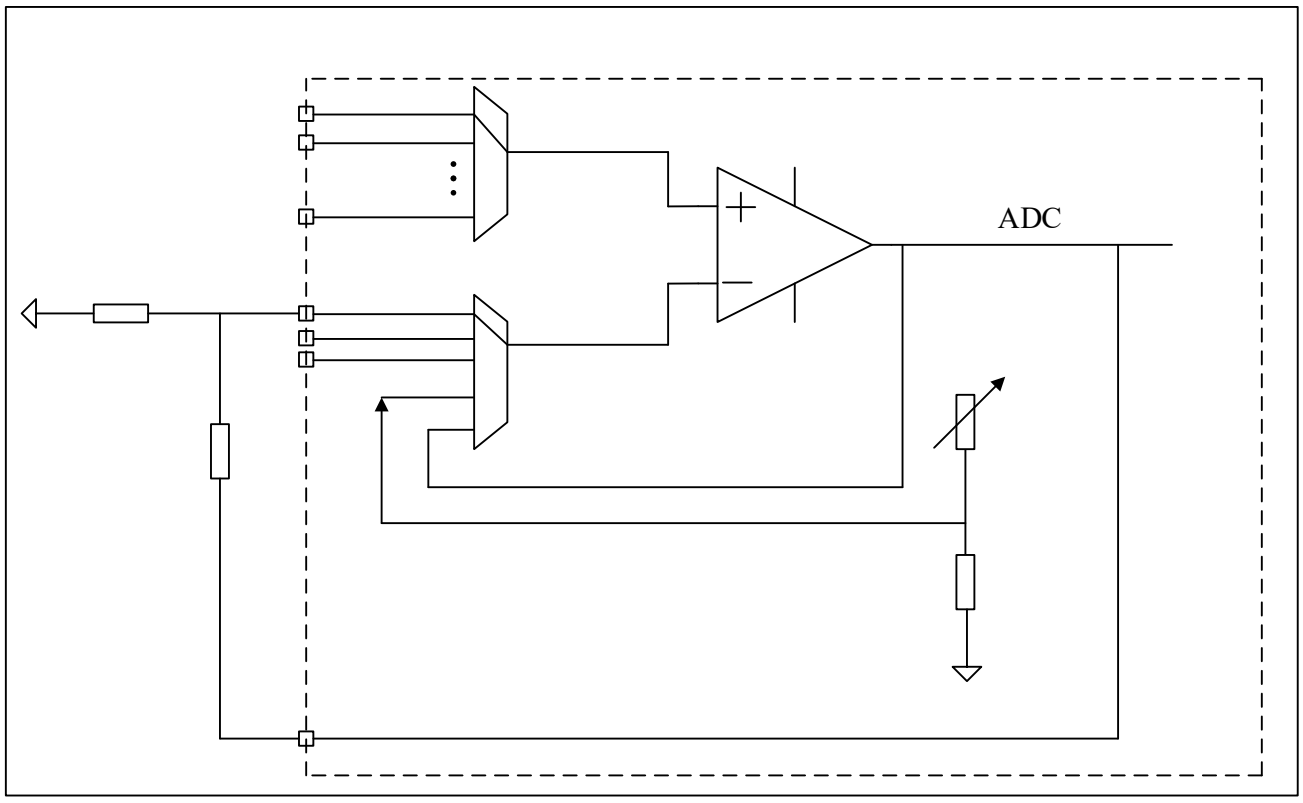
27.2 OPAMP Working Mode

27.2.1 OPAMP Independent OPAMP Mode

The amplification factor of the independent op amp mode is determined by the connected resistance and capacitance. When OPAMPx_CS.MOD is set to 2'b00 or 2'b01, it is the op amp function, OPAMPx_CS.VPSSEL or OPAMPx_CS.VPSEL selects the positive input, and OPAMPx_CS.VMSSEL or OPAMPx_CS.VMSEL selects the negative input. Use an external resistor to form a closed-loop amplification system.

Four completely independent OPAMPs. At this time, the gain is determined by the external resistor network. It can also be cascaded as required to form the required amplification gain. As shown in the figure below, the positive terminal, negative terminal and output terminal of the OPAMP are connected to the external port , the amplification factor is determined by the external RC network.

Figure 27-5 OPAMP standalone operational amplifier mode



27.2.2 OPAMP Follow Mode

In follow mode, the voltage is directly follow. The VMSEL terminal must be directly connected to the OPAMP output port.

OPAMPx_CS. MOD = 2b’11 is the internal follow function, OPAMPx_CS. VPSSEL or OPAMPx_CS. VPSEL selects the positive end input, OPAMPx_CS. VMSSEL or OPAMPx_CS. VMSEL is connected to the output port from the chip interior.

A VM pin that is not occupied can be used as another GPIO.

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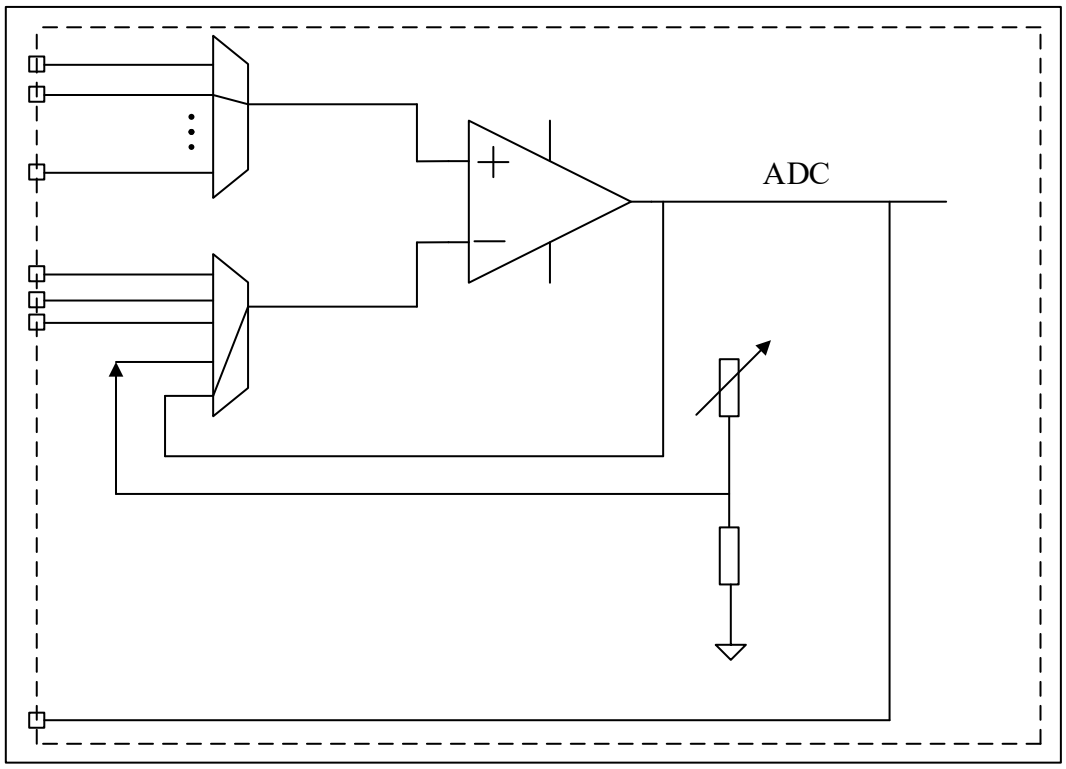
Figure 27-6 Follow mode



27.2.3 OPAMP Internal gain (PGA) Mode

The internal amplification mode, amplifies the input voltage through a built-in resistor feedback network.

OPAMPx_CS. MOD = 2b'10 is a PGA function that supports 2/4/8/16/32 magnification. OPAMPx_CS. VMSSEL or OPAMPx_CS. VMSEL pins must be set to float. OPAMPx_CS.VPSSEL or OPAMPx_CS.VPSEL select positive input.The positive input can be connected to an external pin, which can be an output port for another OPAMP or a resistive network.Set OPAMPx_CS. PGAGAN to gain selection.The output of an OPAMP can be input to another OPAMP or a resistive network.

OPAMP's VM input pin can be used as a normal GPIO.

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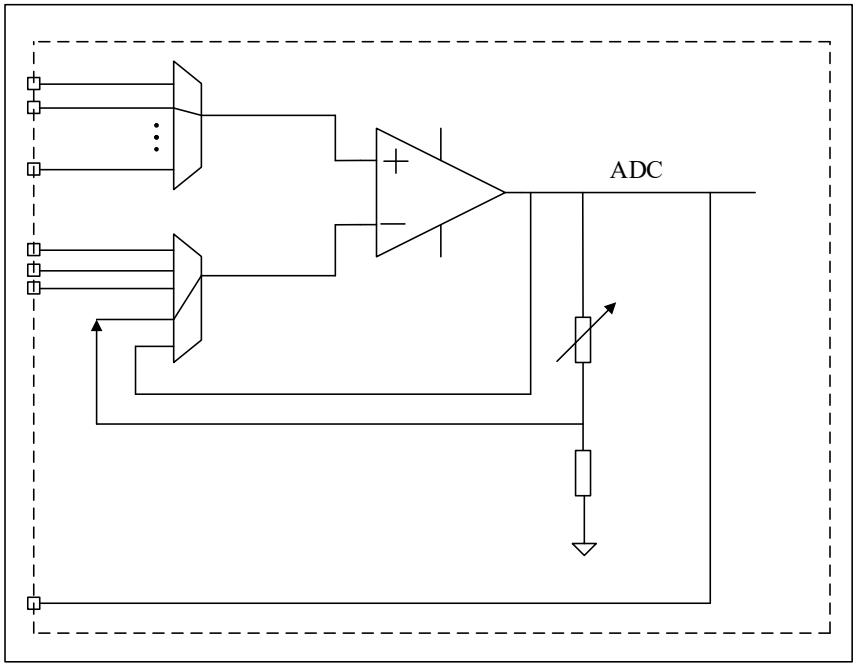
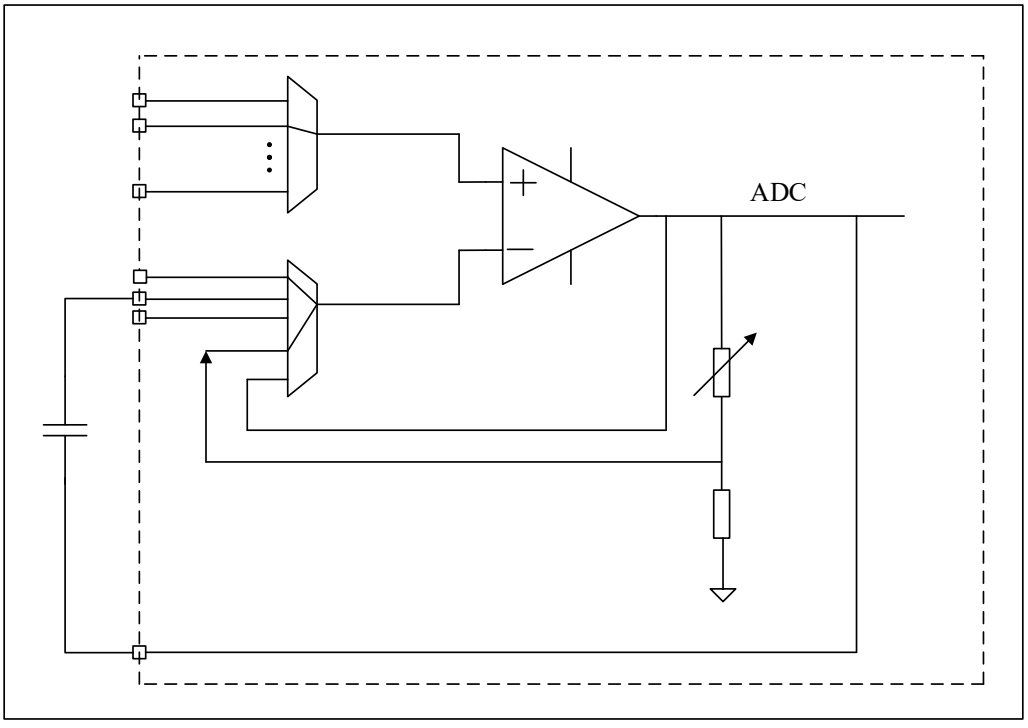
Figure 27-7 Internal gain mode



27.2.4 OPAMP with Filter Internal Gain Mode

In this mode, the amplification voltage is adjustable, supports 2/4/8/16/32, and the OPAMPx_CS.VPSSEL or OPAMAPx_CS.VPSEL is set to be connected to the external pin, and the negative of OPAMP can be connected to components such as capacitors.

Figure 27-8 Internal gain mode with filter



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27.2.5 OPAMP Calibration

The chip has been calibrated before delivery. Users can calibrate the chip again according to the actual environment.
Note: Contact Nations for specific calibration methods to obtain relevant information.

27.2.6 OPAMP Independent Write Protection

By configuring the OPAMP_LOCK register, the write protection of OPAMP can be set independently.After the write protection is set, the software cannot write to the corresponding OPAMP register. Only after the chip is reset, the write protection can be cancelled.

27.2.7 OPAMP TIMER Controls the Switching Mode

In some applications, the input switching of the OPAMP can be performed through TIMx_CC6 .TIM1_CC6 controls the input switching of OPAMP1 and OPAMP2, and TIM8_CC6 controls the input switching of OPAMP3 and OPAMP4.

When TIM1_CC6 is high, OPAMP1 and OPAMP2 select the port configured by VPSSEL/VMSSEL as input, otherwise use VPSEL/VMSEL. When TIM8_CC6 is high, OPAMP3 and OPAMP4 select the port configured by VPSSEL/VMSSEL as input, otherwise use VPSEL/VMSEL.

Set OPAMPx_CS. TCMEN to 1 to enable the automatic switchover input function. The process for configuring the automatic switchover is as follows:

- Enable automatic switching function OPAMPx_CS.TCMEN (OPAMP independent control)
- Configured two conversion MUX configuration (VPSEL,VMSEL, VPSSEL, VMSSEL)
- Start OPAMP and TIM

27.3 OPAMP Register

27.3.1 OPAMP Register Overview

Table 27-1 OPAMP register overview

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
000h	OPAMP_CS1	Reserved										VPSSEL[2:0]			VMSSEL[1:0]		TCMEN	RANGE	CALOUT	TSTREF	Reserved	CALON	VPSEL[2:0]			VMSEL[1:0]		PGAGAN[2:0]			MOD[1:0]		EN
	Reset Value											0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
010h	OPAMP_CS2	Reserved										VPSSEL[2:0]			VMSSEL[1:0]		TCMEN	RANGE	CALOUT	TSTREF	Reserved	CALON	VPSEL[2:0]			VMSEL[1:0]		PGAGAN[2:0]			MOD[1:0]		EN
	Reset Value											0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
020h	OPAMP_CS3	Reserved										VPSSEL[2:0]			VMSSEL[1:0]		TCMEN	RANGE	CALOUT	TSTREF	Reserved	CALON	VPSEL[2:0]			VMSEL[1:0]		PGAGAN[2:0]			MOD[1:0]		EN
	Reset Value											0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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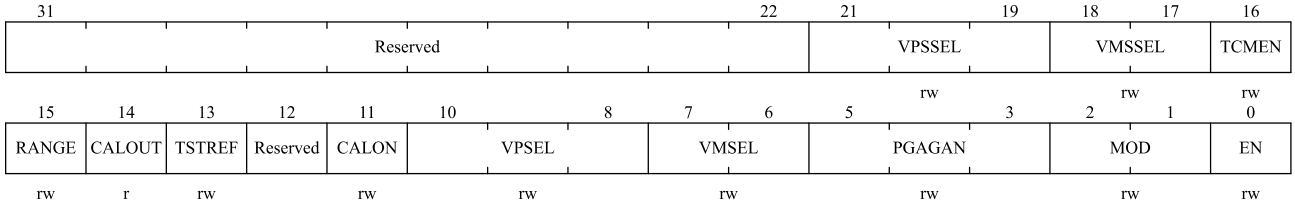
Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
030h	OPAMP_CS4	Reserved										VPSSEL[2:0]			VMSSEL[1:0]		TCMEN	RANGE	CALOUT	TSTREF	Reserved	CALON	VPSEL[2:0]			VMSEL[1:0]		PGAGAN[2:0]			MOD[1:0]		EN
	Reset Value											0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
040h	OPAMP_LOCK	Reserved																												OPAMP4LK	OPAMP3LK	OPAMP2LK	OPAMP1LK
	Reset Value																													0	0	0	0

27.3.2 OPAMP Control Status Register (OPAMPx_CS)

Offset address: 0x00,0x10,0x20,0x30

Reset value: 0x0000 0000



Bit field	Name	Description
31:22	Reserved	Retained, the reset value must be maintained.
21:19	VPSSEL[2:0]	OPAMP non inverted input secondary selection VPSSEL[2:0] / OPAMP1 / OPAMP2 / OPAMP3 / OPAMP4 000 / PA1 / PA7 / PC9 / PC3 001 / PA3 / PB0 / PA1 / DAC1/PA4 010 / DAC2/PA5 / PE8 / DAC2/PA5 / PC5 011 / PA7 / Reserved / PC3 / Reserved 100 / Reserved / Reserved / Reserved / Reserved others / Reserved / Reserved / Reserved / Reserved *Note: DAC2 is directly connected to PA5*
18:17	VMSSEL[1:0]	OPAMP inverted input secondary selection VMSSEL[1:0] / OPAMP1 / OPAMP2 / OPAMP3 / OPAMP4 00 / PA3 / PA2 / PC4 / PB10 01 / PA2 / PA5 / PB10 / PC9 10 / Reserved / Reserved / Reserved / PD8 11 / Floating / Floating / Floating / Floating *Note: VM is floating (for internal PGA (No Filter) mode, follow mode)*
16	TCMEN	Timer controlled Mux mode enable. This bit is set or cleared by software to control the automatic switching between primary and secondary inputs (VPSEL, VMSEL and VPSSEL, VMSSEL). TIM1_CC6 automatically switches between OPAMP1 and OPAMP2, and TIM8_CC6

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<table>
<tr><th>Bit field</th><th>Name</th><th>Description</th></tr>
<tr><td></td><td></td><td>automatically switches between OPAMP3 and OPAMP4.
0: Disable automatic switching;
1: Enable automatic switching.</td></tr>
<tr><td>15</td><td>RANGE</td><td>OPAMP voltage range (OPAMP Operational amplifier power supply range).
0: Low voltage range (VDDA < 2.4V);
1: High voltage range.</td></tr>
<tr><td>14</td><td>CALOUT</td><td>OPAMP calibration output (Operation amplifier calibration output)
When this signal toggles, the offset during calibration mode is calibrated.</td></tr>
<tr><td>13</td><td>TSTREF</td><td>Retained, the reset value must be maintained.</td></tr>
<tr><td>12</td><td>Reserved</td><td>Retained, the reset value must be maintained.</td></tr>
<tr><td>11</td><td>CALON</td><td>Calibration mode enabled
0: Normal mode;
1: Calibration mode.</td></tr>
<tr><td>10:8</td><td>VPSEL[2:0]</td><td>OPAMP non inverted input selection
<table>
<tr><td>VPSEL[2:0</td><td>OPAMP1</td><td>OPAMP2</td><td>OPAMP3</td><td>OPAMP4</td></tr>
<tr><td>000</td><td>PA1</td><td>PA7</td><td>PC9</td><td>PC3</td></tr>
<tr><td>001</td><td>PA3</td><td>PB0</td><td>PA1</td><td>DAC1/PA4</td></tr>
<tr><td>010</td><td>DAC2/PA5</td><td>PE8</td><td>DAC2/PA5</td><td>PC5</td></tr>
<tr><td>011</td><td>PA7</td><td>Reserved</td><td>PC3</td><td>Reserved</td></tr>
<tr><td>100</td><td>Reserved</td><td>Reserved</td><td>Reserved</td><td>Reserved</td></tr>
<tr><td>others</td><td>Reserved</td><td>Reserved</td><td>Reserved</td><td>Reserved</td></tr>
</table>
Note: DAC2 is directly connected to PA5</td></tr>
<tr><td>7:6</td><td>VMSEL[1:0]</td><td>OPAMP inverted input selection
<table>
<tr><td>VMSEL[1:0]</td><td>OPAMP1</td><td>OPAMP2</td><td>OPAMP3</td><td>OPAMP4</td></tr>
<tr><td>00</td><td>PA3</td><td>PA2</td><td>PC4</td><td>PB10</td></tr>
<tr><td>01</td><td>PA2</td><td>PA5</td><td>PB10</td><td>PC9</td></tr>
<tr><td>10</td><td>Reserved</td><td>Reserved</td><td>Reserved</td><td>PD8</td></tr>
<tr><td>11</td><td>Floating</td><td>Floating</td><td>Floating</td><td>Floating</td></tr>
</table>
Note: VM is floating (for internal PGA (No Filter) mode, follow mode)</td></tr>
<tr><td>5:3</td><td>PGAGAN[2:0]</td><td>OPAMP gain setting (Operational amplifier Programmable amplifier gain value)
000: Internal PGA gain 2;
001: Internal PGA gain 4;
010: Internal PGA gain 8;
011: Internal PGA gain 16;
100: Internal PGA gain 32;
Others: Internal PGA gain 2.</td></tr>
<tr><td>2:1</td><td>MOD[1:0]</td><td>OPAMP mode selection (Operational amplifier PGA mode)
0x: External zoom mode;
10: Internal PGA enable;
11: Internal follow mode.</td></tr>
<tr><td>0</td><td>EN</td><td>OPAMP Enable (Operational amplifier Enable)
0: Disable;</td></tr>
</table>

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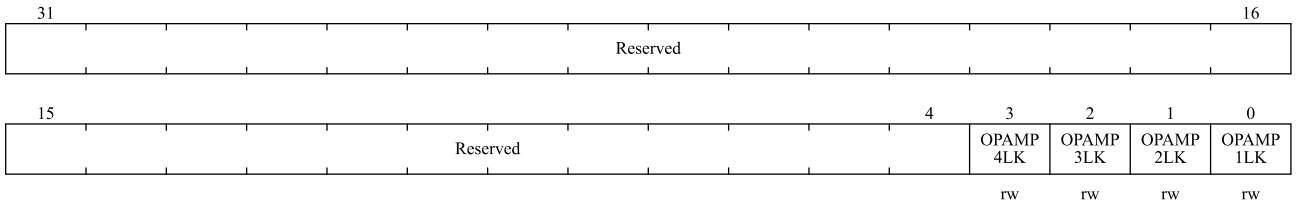
Bit field	Name	Description
		1: Enable.

27.3.3 OPAMP Lock Register (OPAMP_LOCK)

Offset address: 0x40

Reset value: 0x0000 0000



Bit field	Name	Description
31:4	Reserved	Reserved, the reset value must be maintained
3	OPAMP4LK	OPAMP4 lock (OPAMP4 lock bit) After the reset, this bit can be written only once 0: OPAMP4 register can read and write; 1: OPAMP4 register is read-only.
2	OPAMP3LK	Same as OPAMP4LK.
1	OPAMP2LK	Same as OPAMP4LK.
0	OPAMP1LK	Same as OPAMP4LK.

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28 DVP interface (DVP)

28.1 Introduction

DVP is a flexible and powerful CMOS optical sensor interface, which can easily achieve the customer's image capture requirements, and the entire capture process does not require CPU intervention.

The functional characteristics of the DVP interface module are as follows:

- Pure hardware capture method;
- Pure input interface;
- Support clock output (output through MCO, typical value is 24MHz) to provide clock to external CMOS sensor;
- The polarity of input pixel clock DVP_PCLK, frame synchronization signal DVP_VSYNC, and horizontal synchronization signal DVP_HSYNC can be independently configured.
- Support 8x 32bit FIFO;
- FIFO transmits 4 bytes at a time, and the transmission speed is extremely fast;
- Support DMA, no CPU intervention is required in the whole process of image capture;
- The size of the captured image must be an integer multiple of 4 bytes;
- Support hardware inversion of captured image data

28.2 Hardware Interface

28.2.1 Pin Multiplexing Mode

Table 28-1 DVP pin multiplexing

Signal	Default Mapping	Remap 1	Remap 3
DVP_HSYNC	PA1	PE2	PE2
DVP_VSYNC	PA2	PE3	PE3
DVP_ PCLK	PA3	PE4	PE4
DVP_D0	PA4	PE5	PE5
DVP_D1	PA5	PE6	PE6
DVP_D2	PA6	PC0	PC0
DVP_D3	PA7	PB2	PB2
DVP_D4	PC4	PF12	PB10
DVP_D5	PC5	PF13	PB11
DVP_D6	PB0	PF14	PF14
DVP_D7	PB1	PF15	PF15

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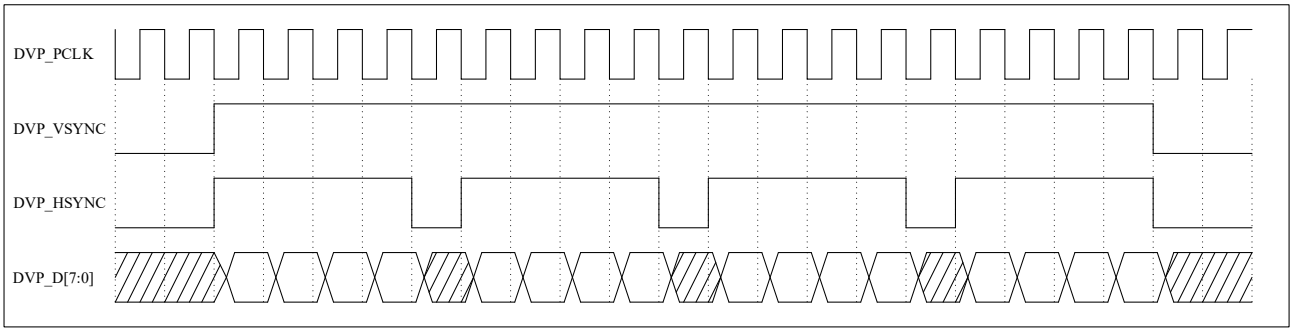
28.2.2 Interface Timing

Figure 28-1 DVP interface timing example



As shown in above figure:

- DVP_PCLK is the pixel clock, and capture 1 byte (8bit) of valid data per clock cycle;
- DVP_VSYNC is a vertical sync (frame sync) signal, active high;
- DVP_HSYNC is the horizontal sync signal, active high;
- When DVP_VSYNC and DVP_HSYNC are both high level, the data is valid;
- There is a gap of at least one pixel clock cycle between every two lines;
- According to the timing in the above figure, the user needs to configure DVP_VSYNC and DVP_HSYNC in the DVP module to be active high and capture data on the falling edge of DVP_PCLK to receive data correctly;
- DVP data is only valid when the capture enable bit (register DVP_CTRL.CAPTURE) is 1, and the capture enable bit must be 1 at least 4 pixel clock cycles earlier than the DVP_VSYNC valid signal (high level), otherwise the current frame will be discarded .

Note: The DVP_VSYNC and DVP_HSYNC signals in the above figure are active high, and may also be active low in practical applications. It is necessary to configure the signal polarity in the DVP module according to the actual situation.

28.3 Operating Instructions

28.3.1 General Operation Process

1. Turn on the clock of the CMOS optical sensor, enable the relevant control port (usually the I2C interface), and configure the sensor parameters;
2. DVP port and parameter configuration (for example: capture mode, window mode, DMA, etc.);
3. Configure the capture enable bit (register DVP_CTRL.CAPTURE), ready to receive data;
4. Turn on the CMOS sensor and start sending data.

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28.3.2 DMA Application

1. Configure and enable the corresponding DMA channel (DMA2 channel 8);
2. Configure the DVP FIFO watermark value (register DVP_CTRL.FWM) to 1 (DMA mode only supports transfers with a watermark of 1);
3. Enable DMA transfer (register DVP_INTEN.DMAEN);
4. When the FIFO receives 1 WORD data, it will send a DMA request;
5. The DMA moves the FIFO data to the designated SRAM area.

28.3.3 Image Size

The image size can be configured according to the user's needs (register DVP_WSIZE), corresponding to the data size that the user can read, among which:

- VLINE is the number of valid data lines of each image frame;
- HCNT is the effective data length of each line, in bytes.

28.3.4 Image Area

The capture area of image can be configured (register DVP_WST), in each image frame, the user can intercept part of the data to retain as needed. The DVP module only stores the area data that needs to be reserved into the FIFO, and other data are automatically discarded:

- DVP_WST.VST configures the starting line of the capture area;
- In the valid line, DVP_WST.HST configures the data position of the starting pixel, calculated in bytes;
- Each register is allowed to be configured as 0.

28.3.5 Image Scaling

The DVP module can reduce the captured image and save it (registers DVP_CTRL.LSM, DVP_CTRL.BSM). The first data must be the required data, and then select the data that needs to be retained as required.

- DVP_CTRL.LSM is the line selection configuration bits. When LSM is set to 3, only keep 1 line of each 3 lines: first keep the 1st line as a valid line,and discard the 2nd and 3rd line, then keep the 4th line, discard the 5th and 6th lines, and so on, until the end of one frame.
- DVP_CTRL.BSM is the pixel selection configuration bits calculated in bytes. Similar to LSM, when BSM is set to 4, only keep 1 byte data of each 4 bytes: first keep the 1st byte as valid data, and discard the 2nd, 3rd, 4th byte, then keep the 5th byte, discard the 6th,7th,8th byte, and so on, until the end of the line.

For specific configuration, please refer to the register list.

28.3.6 Soft Reset

The DVP_CTRL.FFSWRST controls the soft reset. The soft reset is a synchronous reset. Write 1 to reset. Because it

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is a synchronous reset, it must be ensured that the input pixel clock (DVP_PCLK) and the DVP module clock (APB2 clock PCLK2) exist at the same time.

The soft reset requires 8 PCLK2 clock cycles to synchronize. Do not operate the registers during the soft reset. The soft reset only resets the state machine, not the registers. It is recommended that users use a soft reset before each image capture.

Note: The DVP_CTRL.CAPTURE must be set to 0 before soft reset, and the pixel clock (DVP_PCLK) must be clocked during this period.

28.3.7 Interrupts

There are three registers related to interrupts, DVP_INTSTS, DVP_INTEN, DVP_MINTSTS:

- DVP_INTEN is the interrupt enable register.
- DVP_INTSTS is the interrupt status register. Even if the interrupt is not enabled, the interrupt status will change, but the interrupt will not be reported to the system. The corresponding interrupt will be reported only after the corresponding interrupt enable bit in DVP_INTEN is turned on.
- DVP_MINTSTS is the register of interrupt status that reported to system, and users generally only use this status to check the interrupt status.
- When the user wants to use an interrupt, the corresponding flag in the register DVP_INTSTS must be cleared (write 0 to clear) first, in order to avoid the previous state affecting of the interrupt reporting.
- There are two special flag bits in the DVP_INTSTS register: FIFO watermark flag FWIS, FIFO full flag FFIS. These two flag bits are related to the real-time status of the FIFO and cannot be cleared by writing 0, only cleared by reading the FIFO.

28.3.8 Read FIFO Data

FIFO data can be read directly by software, and also supports DMA or interrupt mode.

- DMA mode: when the FIFO data reaches the waterline value (FWM, must be 1), a DMA request will be generated, and the DMA will move the data to the configured SRAM;
- Interrupt mode: When the FIFO data reaches the watermark value (FWM), an interrupt will be generated, and the user will read the data through the register DVP_FIFO

Note: Because the data from the interface is 8 bits, but the data in the FIFO is 32 bits, the module will put the first data in the high order.

28.3.9 Notes

- It must be ensured that the external CMOS optical sensor clock is turned on first, that is, DVP_PCLK is valid.
- It must be ensured that the valid data to be captured is an integer multiple of 4 bytes.
- The configuration of watermark can only be configured as 1 when using DMA mode. (The system only supports reading one data at a time).

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28.4 DVP Register

28.4.1 DVP Register Overview

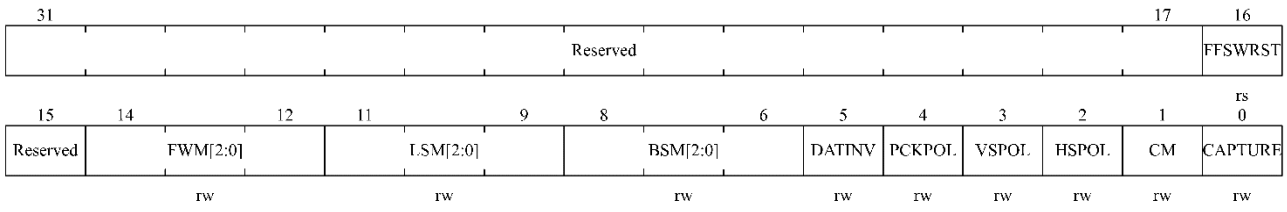
Table 28-2 DVP register overview

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
000h	DVP_CTRL	Reserved															FFSWRST	Reserved	FWM[2:0]			LSM[2:0]			BSM[2:0]			DATINV	PCKPOL	VSPOL	HSPOL	CM	CAPTURE
	Reset Value																0		0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
004h	DVP_STS	Reserved																												FCNT[2:0]			FNE
	Reset Value																													0	0	0	0
008h	DVP_INTSTS	Reserved																						HERRIS	VERRIS	FOIS	FWIS	FFIS	FEIS	LEIS	LSIS	FMEIS	FMSIS
	Reset Value																							0	0	0	0	0	1	0	0	0	0
00Ch	DVP_INTEN	Reserved																					DMAEN	HERRIE	VERRIE	FOIE	FWIE	FFIE	FEIE	LEIE	LSIE	FMEIE	FMSIE
	Reset Value																						0	0	0	0	0	0	0	0	0	0	0
010h	DVP_MINTSTS	Reserved																						HERRMIS	VERRMIS	FOMIS	FWMIS	FFMIS	FEMIS	LEMIS	LSMIS	FMEMIS	FMSMIS
	Reset Value																							0	0	0	0	0	0	0	0	0	0
014h	DVP_WST	Reserved								VST[10:0]												Reserved	HST[10:0]										
	Reset Value									0	0	0	0	0	0	0	0	0	0	0	0		0	0	0	0	0	0	0	0	0	0	0
018h	DVP_WSIZE	Reserved								VLINE[10:0]												Reserved	HCNT[10:0]										
	Reset Value									0	0	0	0	0	0	0	0	0	0	0	0		0	0	0	0	0	0	0	0	0	0	0
01Ch	DVP_FIFO	DAT3[7:0]								DAT2[7:0]								DAT1[7:0]										DAT0[7:0]					
	Reset Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

28.4.2 DVP Control Register（DVP_CTRL）

Address offset : 0x00

Reset value : 0x0000 1000



Bit field	Name	Description
31:17	Reserved	Reserved, the reset value must be maintained.
16	FFSWRST	FIFO soft reset enable bit. Set to 1 by software and cleared to 0 by hardware. When resetting, it must be ensured

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Bit field	Name	Description
		that both DVP_PCLK and PCLK2 are provided normally, at least 8 PCLK2 clock cycles can be guaranteed to reset successfully, and the DVP module register can be operated after the reset is completed. Soft reset only resets the internal logic of the DVP module, not the registers. 0: No effect 1: enable soft reset
15	Reserved	Reserved, the reset value must be maintained.
14:12	FWM[2:0]	FIFO watermark value. DMA or interrupt is triggered when the data length in the FIFO reaches this value.
11:9	LSM[2:0]	Line selection mode. 000: capture all lines 001: Capture 1 line of each 2 lines 010: Capture 1 line of each 3 lines 011: Capture 1 line of each 4 lines 100: Capture 1 line of each 5 lines 101: Capture 1 line of each 6 lines 110: Capture 1 line of each 7 lines 111: Capture 1 line of each 8 lines
8:6	BSM[2:0]	Byte selection mode. Indicates the proportion of valid pixels extracted and retained in each line of data, calculated in bytes, only applicable to the case where the pixel data does not exceed 1 byte. For example, when the input data is in RGB565 format, 1 pixel occupies 2 bytes, and the byte selection mode is not supported. 000: capture all pixels 001: Capture 1 pixel of each 2 pixels 010: Capture 1 pixel of each 3 pixels 011: Capture 1 pixel of each 4 pixels 100: Capture 1 pixel of each 5 pixels 101: Capture 1 pixel of each 6 pixels 110: Capture 1 pixel of each 7 pixels 111: Capture 1 pixel of each 8 pixels
5	DATINV	Data inversion. 0: Data is not inversed 1: Data is inversed
4	PCKPOL	Pixel clock polarity. This bit is used to configure the capture edge of the pixel clock. 0: Capture on falling edge 1: Capture on rising edge
3	VSPOL	Vertical sync signal polarity. This bit indicates the level of the VSYNC pin when there is valid data on the parallel interface. 0: VSYNC active low 1: VSYNC active high

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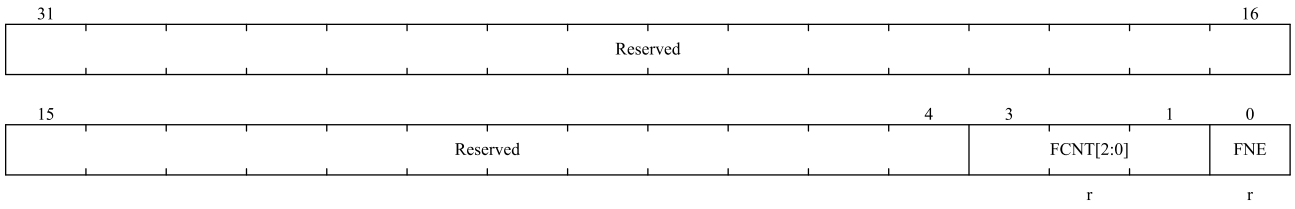
Bit field	Name	Description
2	HSPOL	Horizontal sync polarity. This bit indicates the level of the HSYNC pin when there is valid data on the parallel interface. 0: HSYNC active low 1: HSYNC active high
1	CM	capture mode. 0: Single frame mode. Once activated, the interface waits for the frame sync signal to be valid, and then starts transmitting data. After a frame of data is transmitted, the CAPTURE bit is automatically cleared. 1: Continuous mode. After transmitting a frame of data, the CAPTURE bit is not cleared and continues to wait for the next frame synchronization signal.
0	CAPTURE	Capture enable. In single frame mode, this bit is automatically cleared to 0 after the first frame is received. In continuous mode, it needs to be cleared by software. If the software clears 0 while the capture is in progress, this bit is not cleared until the current frame is captured. 0: Disable capture function 1: Enable capture function *Note: Before enabling capture, the DMA controller and DVP configuration registers must be properly configured as required.*

28.4.3 DVP Status Register（DVP_STS）

Address offset : 0x04

Reset value : 0x0000 0000



Bit field	Name	Description
31:4	Reserved	Reserved, the reset value must be maintained.
3:1	FCNT[2:0]	Length of data in FIFO.
0	FNE	FIFO not empty flag. 0: FIFO is empty 1: There is valid data in the FIFO

28.4.4 DVP Interrupt Status Register（DVP_INTSTS）

Address offset : 0x08

Reset value : 0x0000 0010

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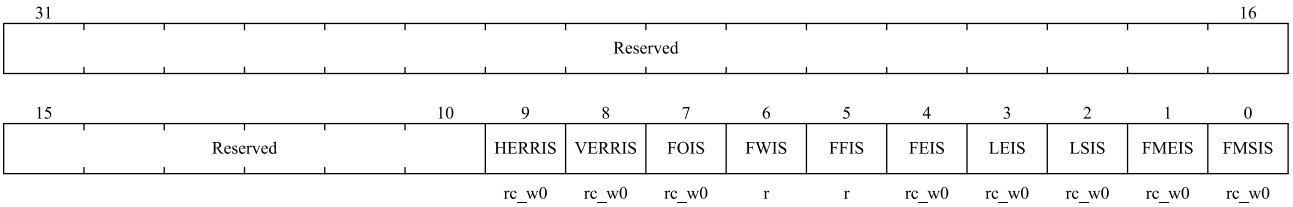

Bit field	Name	Description
31:10	Reserved	Reserved, the reset value must be maintained.
9	HERRIS	HSYNC error status. Software write 0 to clear. When the received row data is smaller than the configured data size per line, an HSYNC error is generated (HSYNC arrives early). 0: No error 1: There is an HSYNC error
8	VERRIS	VSYNC error status. Software write 0 to clear. When the number of received data lines is less than the configured number of data lines per frame, a VSYNC error is generated (VSYNC arrives early) 0: No error 1: There is a VSYNC error
7	FOIS	FIFO overflow status. Software write 0 to clear. This bit needs to be cleared manually. 0: FIFO has not overflowed 1: FIFO overflow
6	FWIS	FIFO watermark status. This bit is related to the real-time status of the FIFO and can only be cleared by reading the FIFO. 0: The data length in the FIFO has not reached DVP_CTRL.FWM[2:0] 1: The data length in the FIFO has reached DVP_CTRL.FWM[2:0]
5	FFIS	FIFO full status. This bit is related to the real-time status of the FIFO and can only be cleared by reading the FIFO. 0: FIFO is not full 1: FIFO is full
4	FEIS	FIFO is empty. Software write 0 to clear. This bit needs to be cleared manually. 0: FIFO is not empty 1: FIFO is empty
3	LEIS	End of line status. Software write 0 to clear. 0: Line not ended. 1: Line has ended.
2	LSIS	row start state. Software write 0 to clear. 0: Line not started.

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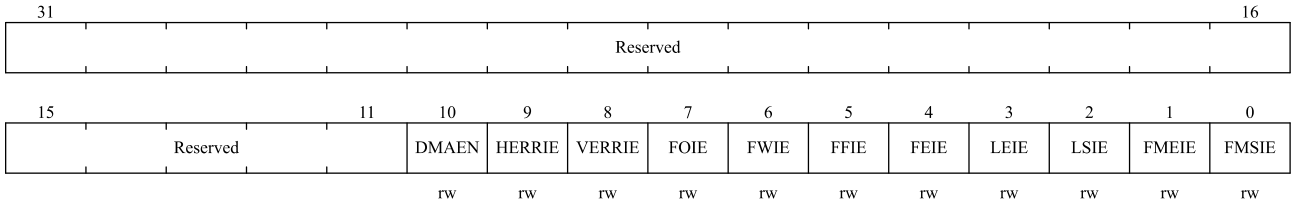
Bit field	Name	Description
		1: Line has started.
1	FMEIS	Frame end state. Software write 0 to clear. 0: Frame not ended. 1: Frame has ended.
0	FMSIS	Frame start state. Software write 0 to clear. 0: Frame not started. 1: Frame has started.

28.4.5 DVP Interrupt Enable Register

Address offset : 0x0c

Reset value : 0x0000 0000



Bit field	Name	Description
31:11	Reserved	Reserved, the reset value must be maintained.
10	DMAEN	DMA enable bit. When this bit is enabled, a DMA request will be generated when the data length of the FIFO reaches the watermark. 0: DMA is not enabled. 1: DMA is enabled.
9	HERRIE	HSYNC error interrupt enable. 0: Disable HSYNC error interrupt 1: Enable HSYNC error interrupt
8	VERRIE	VSYNC error interrupt enable. 0: Disable VSYNC error interrupt 1: Enable VSYNC error interrupt
7	FOIE	FIFO overflow interrupt enable. 0: Disable FIFO overflow interrupt 1: Enable FIFO overflow interrupt
6	FWIE	FIFO watermark interrupt enable. 0: Disable FIFO watermark interrupt 1: Enable FIFO waterline interrupt
5	FFIE	FIFO full interrupt enable. 0: Disable FIFO full interrupt 1: Enable FIFO full interrupt

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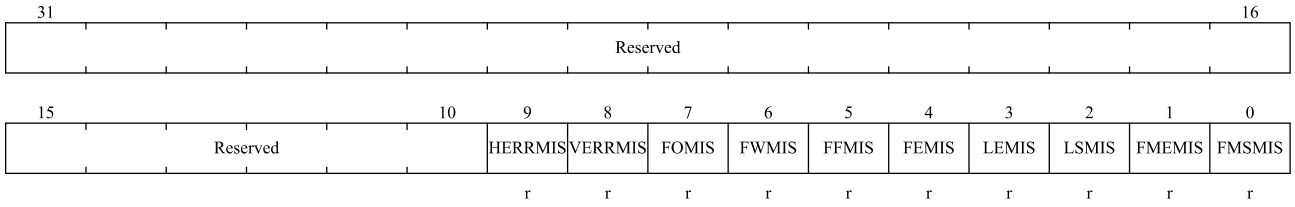
Bit field	Name	Description
4	FEIE	FIFO empty interrupt enable. 0: Disable FIFO empty interrupt 1: Enable FIFO empty interrupt
3	LEIE	End of line interrupt enable. 0: End-of-line interrupt is not enabled 1: Enable end-of-line interrupt
2	LSIE	Line start interrupt enable. 0: Disable line start interrupt 1: Enable line start interrupt
1	FMEIE	End of frame interrupt enable. 0: End-of-frame interrupt is not enabled 1: Enable end-of-frame interrupt
0	FMSIE	Start of Frame Interrupt Enable. 0: Disable start of frame interrupt 1: Enable frame start interrupt

28.4.6 DVP Interrupt Trigger Status Register（DVP_MINTSTS）

Address offset : 0x10

Reset value : 0x0000 0000

When there is an interrupt in the system, this register should be polled to determine which interrupt it is. The corresponding interrupt flag in this register is valid only when both the interrupt enable and interrupt status bits are valid. The interrupt flag can be cleared by clearing the corresponding bit in the interrupt status register DVP_INTSTS.



Bit field	Name	Description
31:10	Reserved	Reserved, the reset value must be maintained.
9	HERRMIS	HSYNC error interrupt trigger status. 0: No HSYNC error. 1: HSYNC error interrupt triggered.
8	VERRMIS	VSYNC error interrupt trigger status. 0: No VSYNC error. 1: VSYNC error interrupt triggered.
7	FOMIS	FIFO overflow interrupt trigger status. Software write 0 to clear. This bit needs to be cleared manually. 0: FIFO has not overflowed. 1: FIFO overflow interrupt triggered.

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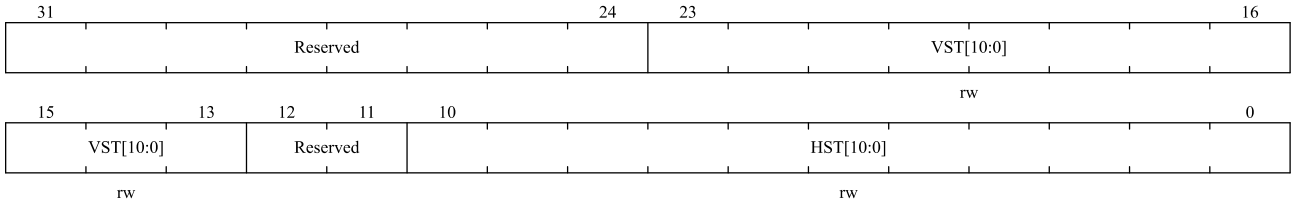
Bit field	Name	Description
6	FWMIS	FIFO watermark interrupt status. This bit is related to the real-time status of the FIFO and can only be cleared by reading the FIFO. 0: The data length in the FIFO has not reached DVP_CTRL.FWM[2:0]. 1: The data length in the FIFO has reached DVP_CTRL.FWM[2:0] and interrupt triggered.
5	FFMIS	FIFO full interrupt status. This bit is related to the real-time status of the FIFO and can only be cleared by reading the FIFO. 0: FIFO is not full. 1: FIFO is full and interrupt triggered.
4	FEMIS	FIFO empty interrupt state. Software write 0 to clear. This bit needs to be cleared manually. 0: FIFO is not empty 1: FIFO is empty and interrupt triggered.
3	LEMIS	End of line interrupt status. Software write 0 to clear. 0: Line not ended. 1: Line has ended and interrupt triggered.
2	LSMIS	Line start interrupted state. Software write 0 to clear. 0: Line not started. 1: Line has started and interrupt triggered.
1	FMEMIS	End of frame interrupt status. Software write 0 to clear. 0: Frame not ended. 1: Frame has ended and interrupt triggered.
0	FMSMIS	Frame start interrupted state. Software write 0 to clear. 0: Frame not started. 1: Frame has started and interrupt triggered.

28.4.7 DVP Image Start Register（DVP_WST）

Address offset : 0x14

Reset value : 0x0000 0000



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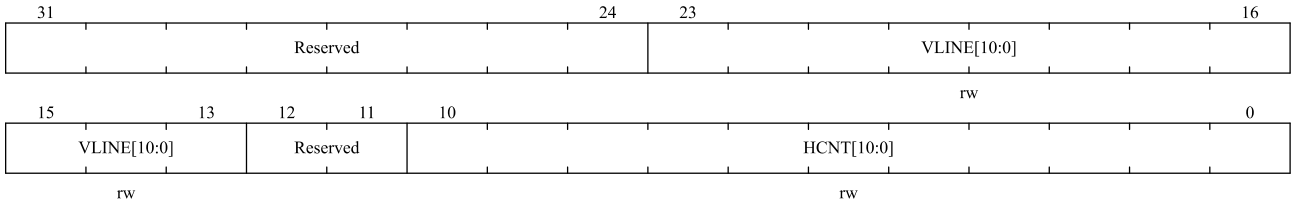
Bit field	Name	Description
31:24	Reserved	Reserved, the reset value must be maintained.
23:13	VST[10:0]	Start line number, the first line starts at 0.
12:11	Reserved	Reserved, the reset value must be maintained.
10:0	HST[10:0]	Starting pixel number, the first pixel starts at 0.

28.4.8 DVP Image Size Register（DVP_WSIZE）

Address offset : 0x18

Reset value : 0x0000 0000

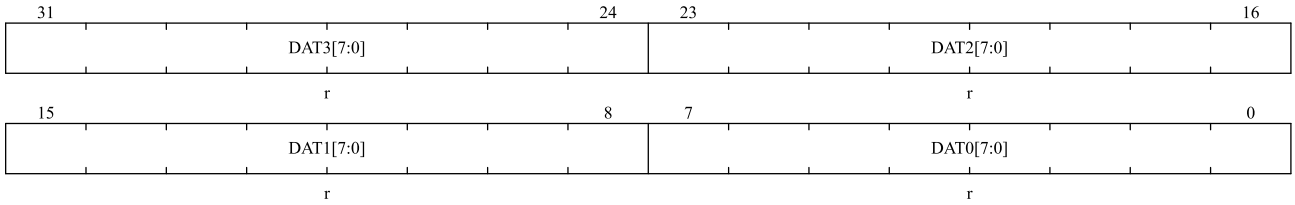


Bit field	Name	Description
31:24	Reserved	Reserved, the reset value must be maintained.
23:13	VLINE[10:0]	The number of lines per frame.
12:11	Reserved	Reserved, the reset value must be maintained.
10:0	HCNT[10:0]	The number of pixels per line, calculated in bytes.

28.4.9 DVP FIFO Register（DVP_FIFO）

Address offset : 0x1c

Reset value : 0x0000 0000



Bit field	Name	Description
31:24	DAT3[7:0]	Data byte 3
23:16	DAT2[7:0]	Data byte 2
15:8	DAT1[7:0]	Data byte 1
7:0	DAT0[7:0]	Data byte 0

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29 Debug Support (DBG)

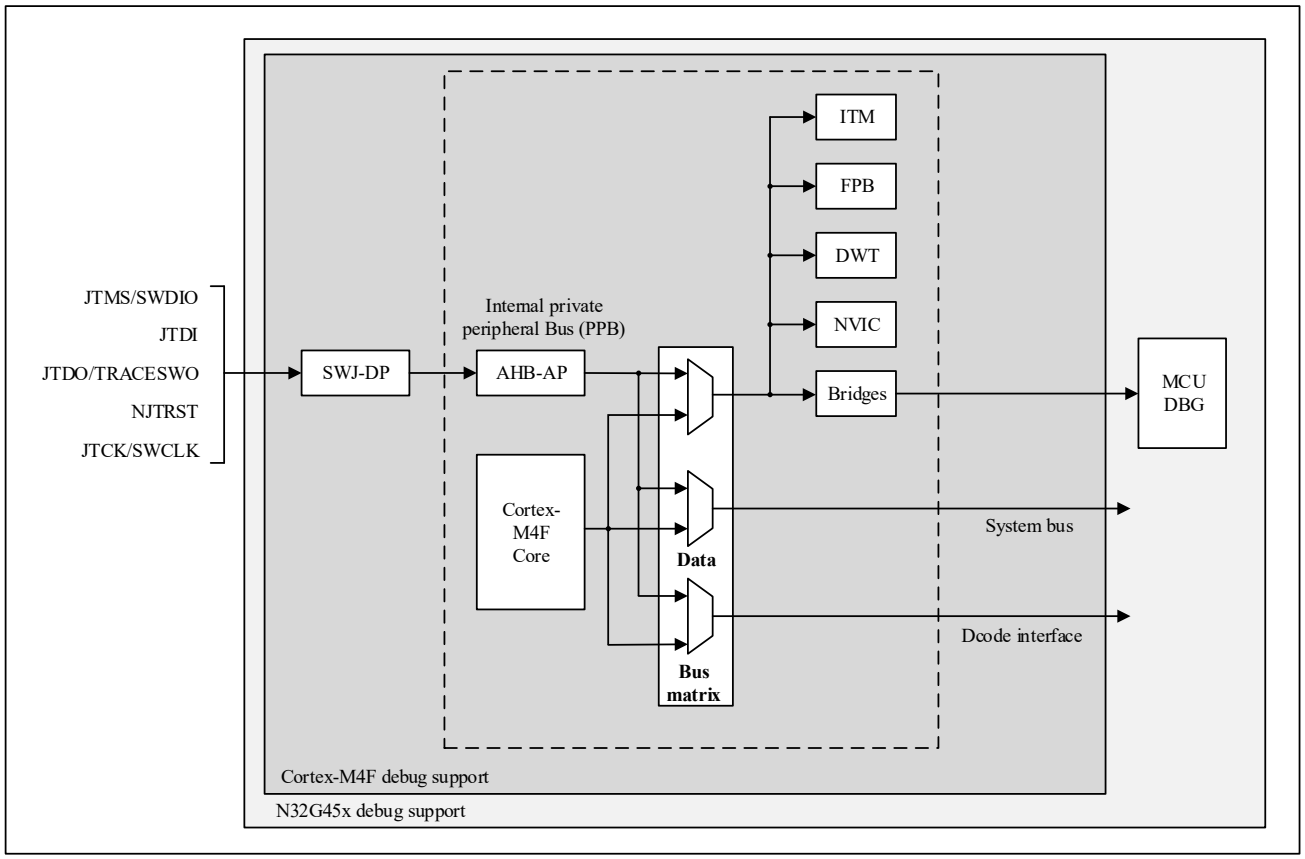
29.1 Overview

N32G45x uses Cortex™-M4F core, which integrates hardware debugging module. Support instruction breakpoint (stop when instruction fetches value) and data breakpoint (stop when data access). When the kernel is stopped, the user can view the internal state of the kernel and the external state of the system. After the user's query operation is completed, the kernel and peripherals can be restored, and the corresponding program can continue to be executed. The hardware debugging module of the N32G45x kernel can be used when it is connected to the debugger (when it is not disabled).

N32G45x supports the following debugging interfaces:

- Serial wire
- JTAG debugging interface

Figure 29-1 N32G45x level and Cortex™-M4F level debugging block diagram



The ARM Cortex™-M4F core hardware debugging module can provide the following debugging functions:

- SWJ-DP: serial /JTAG debug port
- AHP-AP:AHB access port
- ITM: execution tracking unit
- FPB: Flash instruction breakpoint

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- DWT: data trigger

Reference:

- Cortex™-M4 Technical Reference Manual (TRM)
- ARM debugging interface V5 structure specification
- ARM CoreSight development tool set (r1p0 version) technical reference manual

The system supports low-power mode debugging and debugging of some peripherals. The peripherals supporting debugging include: CAN, I2C interface and TIMER, WWDG and IWDG modules. The user needs to set the corresponding bit of the debug control register (DBG_CTRL) to 1 when debugging with low power consumption or peripherals.

29.2 JTAG/SWD Function

The debugging tool can call the debugging function through the SWD debugging interface or JTAG debugging interface mentioned above.

29.2.1 Switch JTAG/SWD Interface

The chip uses JTAG debug interface by default. If you need to switch the debug interface, you can switch between SWD interface and JTAG interface through the following operations:

JTAG debug to SWD debug switch:

1. Sending JTMS = 1 signals with more than 50 JTCK cycles;
2. Send 16-bit JTMS = 1110011110011110(0xE79E LSB) signal;
3. Send JTMS = 1 signal with more than 50 JTCK cycles.

Switch from SWD debugging to JTAG debugging:

1. Sending JTMS = 1 signals with more than 50 JTCK cycles;
2. Send 16-bit JTMS = 1110011100111100(0xE73C LSB) signal;
3. Send JTMS = 1 signal with more than 50 JTCK cycles.

29.2.2 Pin Allocation

JTAG debugging interface includes five pins: JTCK(JTAG clock pin), JTMS(JTAG mode selection pin), JTDI(JTAG data input pin), JTDO(JTAG data output pin) and NJTRST(JTAG data reset pin, low level reset pin).

SWD (serial debugging) interface includes two pins: SWCLK (clock pin) and SWDIO (data input and output pin), which provide the interface of two pins: data input and output pin (SWDIO) and clock pin (SWCLK).

See the following Table for the pin allocation of JTAG debugging interface and SWD debugging interface (SWDIO is multiplexed with JTMS, SWCLK is multiplexed with JTCK):

Table 29-1 Debug port pin

Debug port	Pin allocation

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JTMS/SWDIO	PA13
JTCK/SWCLK	PA14
JTDI	PA15
JTDO	PB3
NJTRST	PB4

- When both JTAG debugging interface and SWD debugging interface are enabled, the 5-wire JTAG debugging interface will be used by default after reset.
- When using JTAG interface, users can not use NJTRST pin. In this case, NJTRST pin (PB4, internal hardware pull-up) can be used as a general-purpose GPIO.
- When SWD interface is used, three pins JTDI(PA15), JTDO(PB3) and NJTRST(PB4) can be used as general GPIO.
- When the debugging function is not used, the above five pins can be used as general-purpose GPIO.

29.3 MCU Debugging Function

29.3.1 Low Power Mode Support

N32G45x can provide a variety of low power consumption modes (refer to Power Control (PWR) for details). When debugging, ensure that the FCLK and HCLK of the kernel are on, and provide the necessary clock for kernel debugging. Users can debug MCU in low power mode according to specific operation (ensuring the output of FCLK or HCLK in low power mode).

If users want to debug MCU in low power mode, they first need the debugger to configure registers related to low power mode:

- DBG_SLEEP mode:

  The DBG_CTRL.SLEEP bit needs to be configured to provide HCLK with the same clock as provided to FCLK (ie: the original configured system clock).

- DBG_STOP mode:

  The DBG_CTRL.STOP bit needs to be configured to start the internal RC oscillator to provide the clock for HCLK and FCLK.

- DBG_STANDBY mode:

  The DBG_CTRL.STDBY bit needs to be configured to start the internal RC oscillator to provide the clock for HCLK and FCLK.

29.3.2 Peripheral Debugging Support

When the corresponding bit of the peripheral control bit in the DBG_CTRL register is set to 1, the corresponding peripheral enters the debugging state after the kernel stops:

- Timer peripheral: the timer counter stops and debugs;
- I2C peripheral: the SMBUS of I2C keeps the state and carries out debugging;

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- WWDG/IWDG peripheral: WWDG/IWDG counter clock stops and debugs;
- CAN peripheral: the CAN interface receiving register stops counting and debugs.

29.4 DBG Registers

29.4.1 DBG Register Overview

These peripheral registers must be operated as words (32 bits). The base address of the register is 0xE004 2000.

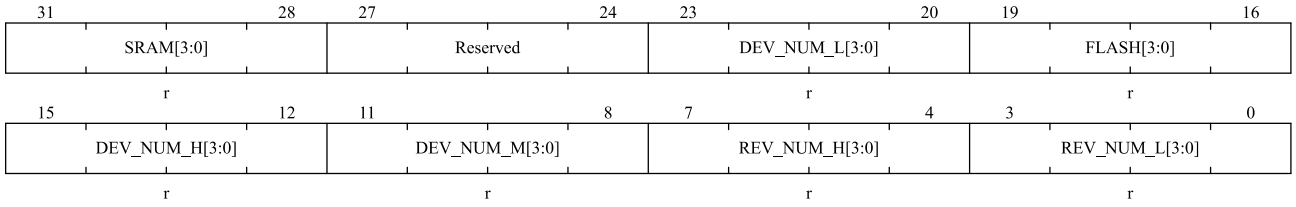
Table 29-2 DBG register overview

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
000h	DBG_ID	SRAM[3:0]				Reserved				DEV_NUM_L[3:0]				FLASH[3:0]				DEV_NUM_H[3:0]				DEV_NUM_M[3:0]				REV_NUM_H[3:0]				REV_NUM_L[3:0]			
	Reset Value	x	x	x	x					x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
004h	DBG_CTRL	Reserved											CAN2_STOP	TIM7_STOP	TIM6_STOP	TIM5_STOP	TIM8_STOP	I2C2SMBUS_TIMEOUT	I2C1SMBUS_TIMEOUT	CAN1_STOP	TIM4_STOP	TIM3_STOP	TIM2_STOP	TIM1_STOP	WWDG_STOP	IWDG_STOP	Reserved				STDBY	STOP	SLEEP	
	Reset Value												0	0	0	0	0	0	0	0	0	0	0	0	0	0					0	0	0

29.4.2 ID Register (DBG_ID)

Address offset: 0x04

Only 32-bit access is supported, and fixed values cannot be modified



Bit field	Name	Description
31:28	SRAM[3:0]	SRAM capacity. The chip SRAM capacity is (SRAM[3:0] + 1) * 16KB
27:24	Reserved	Reserved, must keep the reset value.
23:20	DEV_NUM_L[3:0]	Lower 4 digits of device model. Device model consists of 12 bits, including high, medium and low, representing the model of MCU. The values are as follows: ■ 0x452: Basic N32G452 ■ 0x455: Incremental N32G455 ■ 0x457: Interconnect N32G457
19:16	FLASH[3:0]	FLASH capacity.

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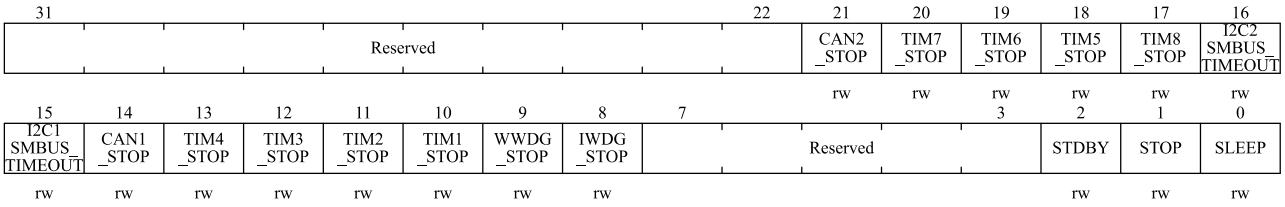
Bit field	Name	Description
		Chip FLASH capacity is FLASH[3:0] * 64KB
15:12	DEV_NUM_H[3:0]	The upper 4 digits of the device model. See the description of DEV_NUM_L[3:0].
11:8	DEV_NUM_M[3:0]	The middle 4 digits of the device model. See the description of DEV_NUM_L[3:0].
7:4	REV_NUM_H[3:0]	High 4 bits of MCU version number
3:0	REV_NUM_L[3:0]	Low 4 bits of MCU version number

29.4.3 Debug Control Register (DBG_CTRL)

Address offset: 0x04

POR reset value: 0x0000 0000 (not reset by system reset)



Bit field	Name	Description
31:22	Reserved	Reserved, the reset value must be maintained.
21	CAN2_STOP	When the kernel enters the debugging state, CAN2 stops running. Set or cleared by software. 0: CAN2 is still running normally; 1: The receiving register of CAN2 does not continue to receive data
20:17	TIMx_STOP	Stop the timer counter when the core stops (x=7,6,5,8). Set or cleared by software. 0: When the core stops, the clock is still provided to the counter of the related timer, and the timer output works normally; 1: When the core stops, turn off the clock of the counter of the related timer and turn off the output of the timer at the same time.
16:15	I2CxSMBUS_TIMEOUT	Stop the SMBUS timeout mode when the core stops (x=2,1). Set or cleared by software. 0: Same as normal mode operation; 1: Freeze the timeout control of SMBUS.
14	CAN1_STOP	When the kernel enters the debugging state, CAN1 stops running. Set or cleared by software. 0: CAN1 is still running normally; 1: The receiving register of CAN1 does not continue to receive data
13:10	TIMx_STOP	When the kernel enters the debugging state, the counter stops working (x=4,3,2,1). Set or cleared by software. 0: The counter of the selected timer still works normally; 1: The counter of the selected timer stops working.

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Bit field	Name	Description
9	WWDG_STOP	When the kernel enters the debug state, the debug window watchdog stops working. Set or cleared by software. 0: The window watchdog counter still works normally; 1: Window watchdog counter stops working.
8	IWDG_STOP	The watchdog stops working when the kernel enters the debugging state. Set or cleared by software. 0: Watchdog counter still works normally; 1: Watchdog counter stops working.
7:3	Reserved	Reserved, must keep the reset value.
2	STDBY	Debug standby mode. Set or cleared by software. 0: (FCLK OFF, HCLK OFF) The whole digital circuit is powered off. From the software point of view, exiting the STANDBY mode is the same as resetting (except that some status bits indicate that the microcontroller has just exited from the STANDBY state). 1: (FCLK ON, HCLK ON) The digital circuit part is not powered down, and the FCLK and HCLK clocks are clocked by the internal RLD oscillator. In addition, it is the same as resetting that the microcontroller exits the STANDBY mode by generating a system reset.
1	STOP	Debug stop mode. Set or cleared by software. 0: (FCLK OFF, HCLK OFF) In stop mode, the clock controller disables all clocks (including HCLK and FCLK). When exiting from STOP mode, the configuration of the clock is the same as that after reset (the microcontroller is clocked by the 8MHz internal RC oscillator (HSI)). Therefore, the software must reconfigure the clock control system to start PLL, crystal oscillator, etc. 1: (FCLK ON, HCLK ON) In stop mode, the FCLK and HCLK clocks are provided by the internal RC oscillator. When exiting the stop mode, the software must reconfigure the clock system to start PLL, crystal oscillator, etc. (the same operation as when this bit is set to 0).
0	SLEEP	Debug sleep mode. Set or cleared by software. 0: (FCLK is ON, HCLK is OFF) In sleep mode, FCLK is provided by the previously configured system clock, while HCLK is off. Since sleep mode does not reset the configured clock system, the software does not need to reconfigure the clock system when exiting from sleep mode. 1: (FCLK ON, HCLK ON) In sleep mode, both the FCLK and HCLK clocks are provided by the previously configured system clock.

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30 Unique Device Serial Number (UID)

30.1 Introduction

MCU series products have two built-in unique device serial numbers with different lengths, namely 96-bit UID (Unique device ID) and 128-bit UCID (Unique Customer ID). These two device serial numbers are stored in the system configuration block of the flash memory, and the information is programmed during manufacture, and any MCU microcontroller is guaranteed to be unique under any circumstances. It can be read by user applications or external devices through CPU or SWD interface and cannot be modified.

UID is 96 bits, which is usually used as serial number or password. When writing flash memory, this unique identifier is combined with software encryption and decryption algorithm to further improve the security of code in flash memory.

UCID is 128 bits and complies with the definition of the Nations Technologies chip serial number. It contains information about chip production and version.

30.2 UID Register

Start address: 0x1FFF_F7F0, 96 bits in length.

30.3 UCID Register

Start address: 0x1FFF_F7C0, 128 bits in length.

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31 Version History

Version	Date	Remark
V3.0	2022.7.8	Initial version
V3.1.0	2022.09.07	1. Modify VERF to VREF in chapter 26.5 2. Setion 7.2.5.7, add TIMx_ETR 3. Figure 12-1, Add description of ETR 4. Delete RTC periodic wake-up support Standby mode. 5. Modfiy PVD threshold gear information description error. 6. Modfiy Figure 21-25 I2S clock generator structure. 7. Modfiy ADC sampling clock and sampling rate 8. Add Clock Tree Figure note: When PLL is selected as system clock source, PLL minimum clock output is 32MHz 9. Added comments to the I2C master send/receive mode chapter

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