N32G451xB/xC/xE Datasheet

The N32G451 series adopts the 32-bit ARM Cortex-M4F core, with a maximum operating frequency of 144MHz. It supports floating-point operations and DSP instructions. The series integrates up to 512KB Flash, 96KB SRAM, 3x12bit 4.7Msps ADC, 2x1Msps 12bit DAC, multiple communication interfaces including U(S)ART, I2C, SPI, USB, CAN, and 1x SDIO interface. It has a built-in cryptographic algorithm hardware acceleration engine.

Key Features

- **CPU core**
  - 32-bit ARM Cortex-M4 core + FPU, single-cycle hardware multiplication and division instructions, supports DSP instructions and MPU
  - Built-in 8KB instruction Cache supports Flash acceleration unit with 0 wait execution.
  - Maximum frequency 144MHz, 180DMIPS
- **Memory**
  - Up to 512KByte on-chip Flash, supports encrypted storage fuction, multi-user partition management and data protection, supports hardware ECC verification, 100,000 erase/write cycles, 10 years of data retention.
  - 96KByte on-chip SRAM (including 16KByte Retention RAM), Retention RAM supports hardware parity check.
- **Clock**
  - HSE: 4MHz~32MHz external high-speed crystal
  - LSE: 32.768KHz external low-speed crystal
  - HSI: internal high-speed RC OSC 8MHz
  - LSI: internal low-speed RC OSC 40KHz
  - Built-in high-speed PLL
  - Supports 1 clock output, configurable system clock, HSE, HSI or PLL post-divider output.
- **Reset**
  - Supports power-on/power-down/brown-out/external pin reset.
  - Supports watchdog reset, software reset.
- **Communication Interfaces**
  - 7 U(S)ART interfaces, maximum baud rate up to 4.5 Mbps, including 3 USART interfaces (supporting ISO7816, IrDA, LIN), 4 UART interfaces.
  - 3 SPI interfaces, speed up to 36 MHz, 2 of which support I2S.
  - 4 I2C interfaces, speed up to 1 MHz, master/slave mode configurable, supports dual address response in slave mode.
  - 1 USB2.0 Full Speed Device interface
  - 1 CAN 2.0A/B bus interface
  - 1 SDIO interface, supports SD/SDIO/MMC format.
- **High-performance analog interfaces**

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- 3x 12bit 4.7Msps high-speed ADC, configurable accuracy, sampling rate up to 8.9Msps in 6bit mode, up to 18 external single-ended input channels, supports differential mode.
- 2x 12bit DAC, 1Msps sampling rate
- Supports external input independent reference voltage source.
- All analog interfaces support 1.8~3.6V full voltage operation.

- **Up to 80 general-purpose I/Os supporting multiplexing functions, most GPIOs support 5V tolerance.**
- **2 high-speed DMA controllers, each controller supports 8 channels, channel source and destination addresses are arbitrarily configurable.**
- **RTC real-time clock, supports leap-year calendar, alarm events, periodic wake-up, supports internal and external clock calibration.**
- **Timers**
  - 2x 16-bit advanced control timers, supporting input capture, output compare, PWM output and quadrature encoding input functions, with a maximum control accuracy of 6.9ns. Each timer has 4 independent channels, 3 of which support 6-way complementary PWM output.
  - 4x 16-bit general-purpose timers, each with 4 independent channels, supporting input capture/output compare/PWM output/single-pulse output.
  - 2x 16-bit basic timers
  - 1x 24-bit SysTick
  - 1x 7-bit window watchdog (WWDG)
  - 1x 12-bit independent watchdog (IWDG)
- **Programming mode**
  - Supports SWD/JTAG online debugging interface.
  - Supports UART, USB Bootloader
- **Security features**
  - Built-in cryptographic algorithm hardware acceleration engine
  - Supports AES, DES, SHA, MD5 algorithms.
  - Flash storage encryption.
  - Multi-user partition management (MMU)
  - TRNG true random number generator
  - CRC16/32
  - Supports write protection (WRP), multiple read protection (RDP) levels (L0/L1/L2)
  - Supports secure boot, encrypted program download, secure update.
  - Supports external clock failure detection, anti-tamper detection.
- **96-bit UID and 128-bit UCID**
- **Operating Conditions**
  - Operating voltage range: 1.8V~3.6V
  - Operating temperature range: -40°C to 105°C
  - ESD: ±4KV (HBM model), ±1KV (CDM model)

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- **Packages**
  - LQFP48(7mm x 7mm)
  - LQFP64(10mm x 10mm)
  - LQFP100(14mm x 14mm)
- **Ordering Information**

Series	Models
N32G451xB	N32G451CBL7, N32G451RBL7
N32G451xC	N32G451CCL7, N32G451RCL7, N32G451VCL7
N32G451xE	N32G451CEL7, N32G451REL7, N32G451VEL7

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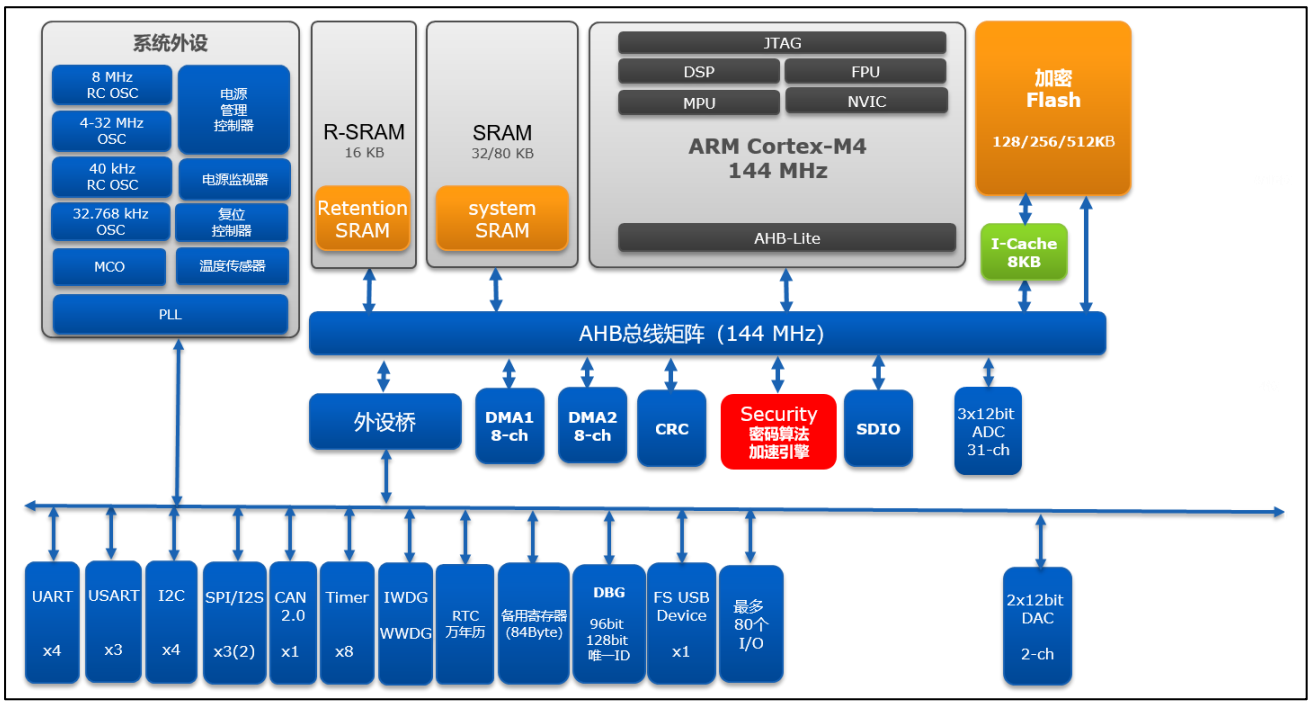
1 Product Overview

The N32G451 series microcontroller products adopt the high-performance 32-bit ARM Cortex™-M4F core, integrating a floating-point unit (FPU) and digital signal processor (DSP), and support parallel computing instructions. The maximum operating main frequency is 144MHz, integrating up to 512KB encrypted Flash memory, and supporting multi-user partition management, up to 96KB SRAM. Built-in one internal high-speed AHB bus, two low-speed peripheral clock buses APB and bus matrix, supporting up to 80 general-purpose I/Os. Provides rich high-performance analog interfaces, including three 12-bit 5Msps ADCs,
supporting up to 31 external input channels, and two 1Msps 12-bit DACs. It also provides various digital communication interfaces, including 7 U(S)ARTs, 4 I2Cs, 3 SPIs, 2 I2Ss, 1 USB 2.0 device, 1 CAN 2.0B, 1 SDIO communication interface, and a built-in cryptographic algorithm hardware acceleration engine,
supporting various international and national cryptographic algorithm hardware acceleration.

The N32G451 series products can stably work in the temperature range of -40°C to +105°C, with a supply voltage of 1.8V to 3.6V, providing multiple power modes for users to choose from, meeting the requirements of low-power applications. This series of products provide 3 different package forms from 48 pins to 100 pins. According to different package forms, the peripheral configuration of the device varies.
Figure 1-1 shows the block diagram of this series of products.

Figure 1-1 N32G451 series Block diagram



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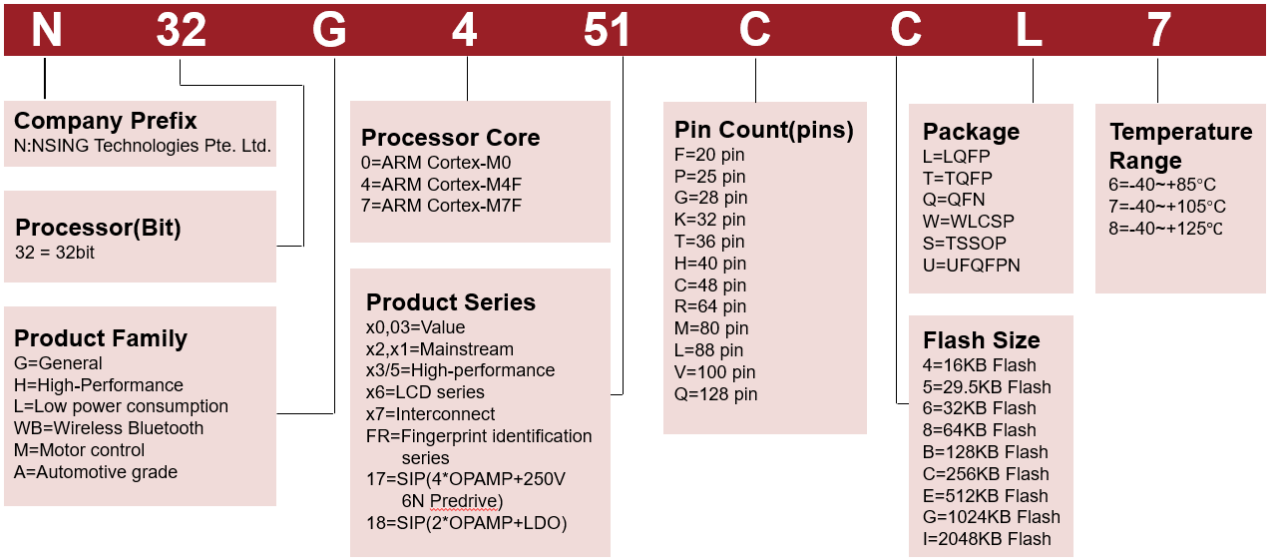
1.1 Naming Convention

Figure 1-2 Illustration of N32G451 Series Order Code Information



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1.2 Device List

Table 1-1 N32G451 Series Resource Configuration

Device Model		N32G451CB/CC/CE			N32G451RB/RC/RE			N32G451VC/VE	
Flash Capacity (KB)		128	256	512	128	256	512	256	512
SRAM Capacity (KB)		48	96	96	48	96	96	96	96
CPU Frequency		ARM Cortex-M4F @144MHz,180DMIPS							
Operating Environment		1.8~3.6V/-40~105℃							
Timer	General	4							
	Advanced	2							
	Basic	2							
Communication Interface	SPI	3(1)							
	I2S	2							
	I2C	3			4				
	USART	3							
	UART	3			4				
	USB	1							
	CAN	1							
	SDIO	No			1				
GPIO		37			51			80	
DMA Number of Channels		2 16Channel							
12bit ADC Number of channels		3 13Channel			3 19Channel			3 31Channel	
12bit DAC Number of channels		2 2Channel							
Algorithm Support		DES/3DES、AES、 SHA1/SHA224/SHA256, MD5, CRC16/CRC32, TRNG							
Security Protection		Reas-write protection (RDP/WRP), storage encryption, partition protection, secure boot							
Package		LQFP48			LQFP64			LQFP100	

Note:(1) The SPI2 and SPI3 interfaces can be flexibly switched between SPI mode and I2S audio mode.

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2 Functional Overview

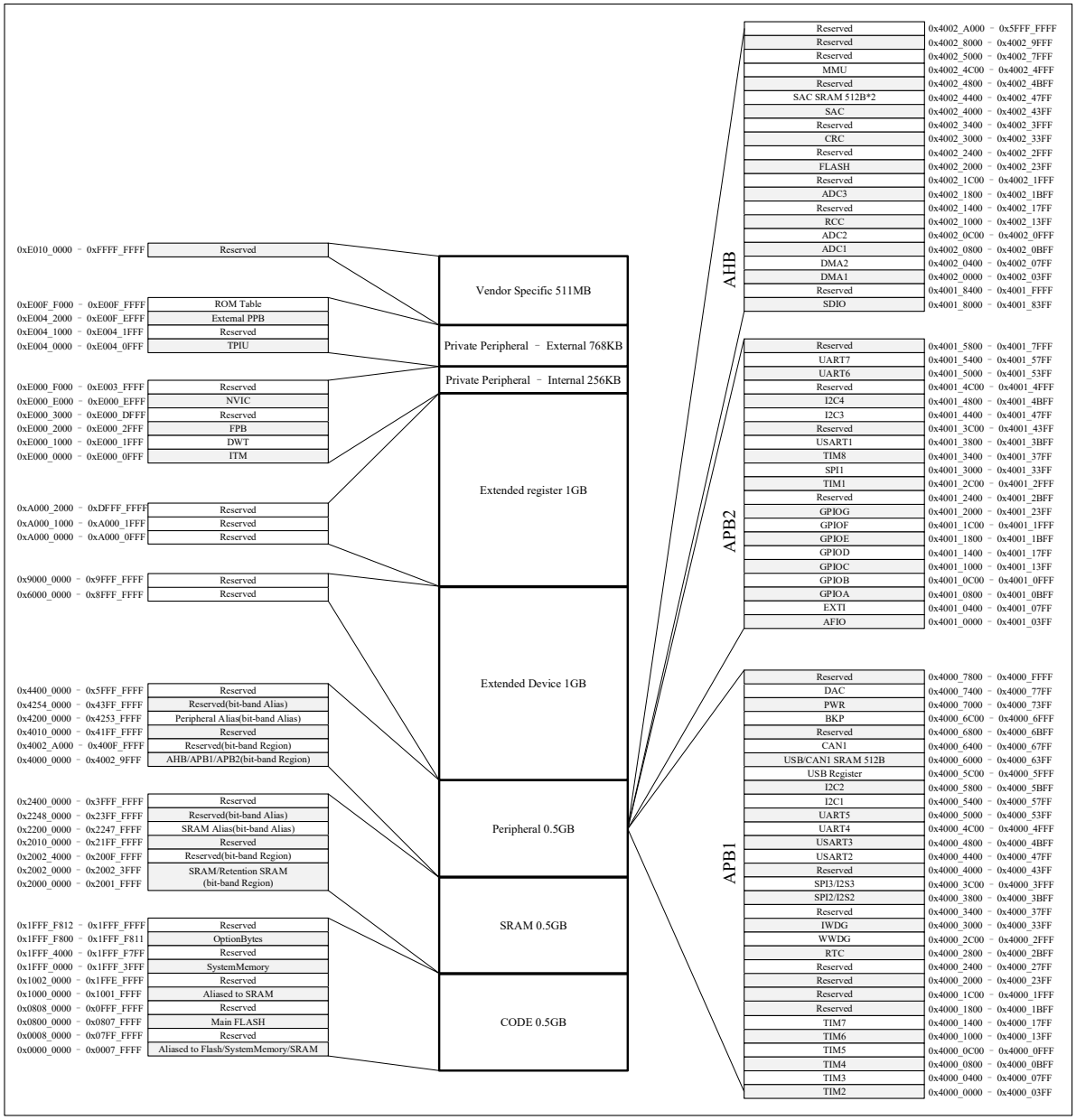
2.1 Processor Core

The N32G451 series integrates the latest generation embedded ARM Cortex™-M4F processor, which enhances computing power based on the Cortex™-M3 core, adds a floating-point arithmetic processing unit (FPU), DSP, and parallel computing instructions, providing excellent performance of 1.25DMIPS/MHz. At the same time, its efficient signal processing capabilities are combined with the low power consumption, low cost, and ease of use of the Cortex-M series processors to meet the application scenarios that require a mix of control and signal processing capabilities.

2.2 Memory

The N32G451 series devices contain embedded Flash memory and embedded SRAM.
Figure 2-1 shows the memory map.

Figure 2-1 Memory Map



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2.2.1 Embedded Flash Memory

The chip integrates embedded Flash memory from 128K to 512K bytes for storing programs and data, with a page size of 2Kbyte, supporting page erase, word write, word read, half-word read, and byte read operations.

It supports storage encryption protection, automatic encryption during writing, and automatic decryption during reading (including program execution operations).

It supports user partition management, with a maximum of 3 user partitions, and data cannot be accessed between different users (only executable code).

2.2.2 Embedded SRAM

The chip integrates up to 96K bytes of built-in SRAM and R-SRAM. R-SRAM is Retention SRAM with a size of 16K bytes. R-SRAM supports Retention and can maintain data in VBAT and Standby modes.

(can be configured to maintain or not). Data is maintained by default in other operating modes.

(RUN/SLEEP/STOP0/STOP2); PWR needs to control its Retention management.

2.2.3 Nested Vectored Interrupt Controller (NVIC)

The built-in nested vectored interrupt controller can handle up to 86 maskable interrupt channels (excluding 16 Cortex™-M4F interrupt lines) and 16 priorities.

- A tightly coupled NVIC can achieve low-latency interrupt response processing.
- Interrupt vector entry goes directly into the kernel.
- Tightly coupled NVIC interface
- Allows early handling of interruptions.
- Handle late higher priority interruptions!
- Support interrupt tail-chaining function.
- Automatically save processor state
- Automatically restore when the interrupt returns, no additional instruction overhead

This module provides flexible interrupt management functions with minimal interrupt latency.

2.3 External Interrupt/Event Controller (EXTI)

The external interrupt/event controller includes 21 edge detectors to generate interrupt/event requests. Each interrupt line can independently configure its trigger event (rising edge, falling edge, or both edges) and
can be individually masked; a pending register maintains the status of all interrupt requests. EXTI can
detect pulse widths smaller than the internal APB2 clock cycle. Up to 80 general-purpose I/O ports are connected to 16 external interrupt lines.

2.4 Clock System

It provides a variety of clocks for users to choose from, including the internal high-speed RC clock HSI (8MHz), internal low-speed clock LSI (40KHz), external high-speed clock HSE (4MHz~32MHz), external low-speed clock LSE (32.768KHz), and PLL.
During reset, the internal HSI clock is set as the CPU clock by default. Subsequently, the user can choose the external HSE clock with failure monitoring function; when an external clock failure is detected, it will be isolated, and the system will automatically switch to HSI. And if the interrupt is enabled, the software can receive the corresponding interrupt. Similarly, complete interrupt management of the PLL clock can be adopted when needed (such as when an indirectly used external oscillator fails).
Multiple prescalers are used to configure the frequency of the AHB, high-speed APB (APB2), and low-speed APB (APB1) regions. The maximum frequency of AHB is 144MHz,

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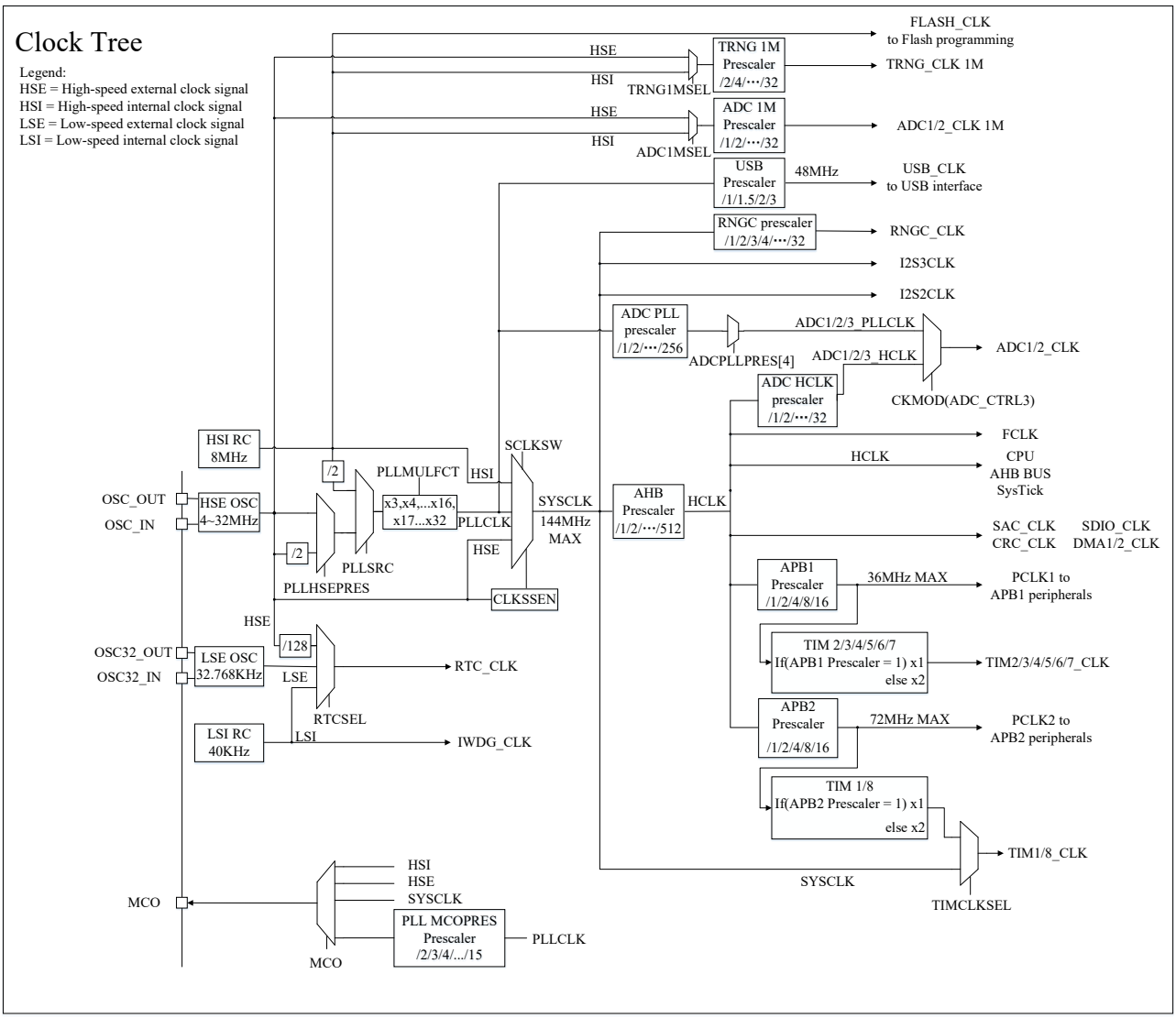
The maximum frequency of APB2 is 72MHz, and the maximum frequency of APB1 is 36MHz. Refer to Figure 2-2 frthe clock tree diagram.

Figure 2-2 Clock Tree



Note:

1. When HSI is used as the PLL clock input, the maximum system clock frequency can only reach 128MHz.
2. When using the USB function, both HSE and PLL must be used, and the CPU frequency must be 48MHz, 72MHz, 96MHz, or 144MHz.

2.5 Boot Mode

At startup, the boot mode after reset can be selected through the BOOT0/1 pin:

- Boot from program Flash memory.
- Boot from system memory.
- Boot from internal SRAM.

The Bootloader is stored in the system memory and can program the Flash Memory through the USART1 and USB interfaces.

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2.6 Power Supply Scheme

- V_{DD} = 1.8~3.6V: The V_{DD} pin supplies power to the I/O pins and internal voltage regulator.
- V_{DDA} = 1.8~3.6V: Supplies power to the analog parts of ADC and DAC. VDDA and
- V_{DD} and V_{SSA} must be connected to V_{DD} and V_{SS} respectively.
- VBAT = 1.8~3.6V: Powers the RTC, external 32kHz oscillator, and backup registers when VDD is turned off.

For detailed information on how to connect the power supply pins, refer to Figure 4-3 Power Supply Scheme.

2.7 Reset

The chip integrates a power-on reset (POR) and power-down reset (PDR) circuit, which is always working to ensure that the system operates when the supply voltage exceeds 1.8V, when V_{DD} is lower than theset threshold (VPOR/PDR), the device is put into a reset state without the need for an external reset circuit.

2.8 Programmable Voltage Monitor

A built-in programmable voltage monitor (PVD) monitors the VDD/VDDA power supply and compares it with the threshold VPVD. When VDD is lower or higher than the threshold VPVD, it will generate an interrupt, and the interrupt handler can issue a warning. The PVD function needs to be enabled through the program. For the values of VPOR/PDR and VPVD, refer to Table 4-6.

2.9 Voltage Regulator

The working modes of the voltage regulator are as follows:

- The chip operates in RUN and SLEEP modes: the main voltage regulator (MR) operates in normal mode.
- The chip operates in STOP0 mode: the main voltage regulator (MR) can operate in normal mode or low-power mode.
- The chip operates in STOP2 and STANDBY modes: the main voltage regulator (MR) is turned off, and the backup domain voltage regulator (BKR) is turned on. After the chip is reset, the main voltage regulator (MR) defaults to normal operation mode.

2.10 Low Power Modes

The N32G451 series products support five low power modes.

- SLEEP mode.

In SLEEP mode, only the CPU stops, all peripherals are in working state and can wake up the CPU when an interrupt/event occurs.

- STOP0 mode

STOP0 mode is based on the Cortex-M4F deep sleep mode, STOP0 mode can achieve low power consumption while keeping the SRAM and register contents from being lost. In STOP0 mode, most clocks in the main power domain are shut down, such as PLL, HSI, HSE, the main regulator can be optionally placed in normal mode or low power mode.
Wake-up: The chip can be woken up from STOP0 mode by any signal configured as EXTI, the EXTI

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signal can be any of the 16 external EXTI signals (I/O related), PVD output, RTC wake-up, RTC alarm, USB wake-up signal.

- STOP2 mode

STOP2 mode is based on Cortex-M4F deep sleep mode, all core digital logic area power supplies are completely shut down. The main voltage regulator is shut down, HSE/HSI/PLL are shut down. CPU registers are kept, LSE/LSI can be configured to work, all GPIOs are kept, peripheral I/O multiplexing. functions are not kept. 16K bytes R-SRAM are kept, other SRAM and register data will all be lost. 84 bytes of backup registers are kept.
Wake-up: The chip can be woken up from STOP2 mode by any signal configured as EXTI, the EXTI signal can be any of the 16 external EXTI signals (I/O related), PVD output, RTC periodic wake-up, RTC alarm, RTC tamper, NRST reset, IWDG reset.

- STANDBY mode

In STANDBY mode, the lowest current consumption state can be achieved. The internal voltage regulator is shut down, PLL, HSI RC oscillator and HSE crystal oscillator are also shut down; after entering.
STANDBY mode, the contents of the registers will be lost, but the contents of the backup registers are still retained, R-SRAM can be kept, standby circuit is still working.
An external reset signal on NRST, IWDG reset, a rising edge on the WKUP pin, RTC wake-up or RTC alarm can wake up the microcontroller from STANDBY mode.

- VBAT mode

Whenever VDD is powered down, it will automatically enter VBAT mode. In VBAT mode, except for NRST, PA0-WKUP, PC13_TAMPER, PC14, PC15, most I/O pins are in a high impedance state.

Note: When entering STANDBY mode, RTC, IWDG and the corresponding clocks will not be stopped.

2.11 Direct Memory Access (DMA)

Integrated 2 flexible general-purpose DMA controllers, each DMA controller supports 8 channels, which can manage data transfers from memory to memory, peripherals to memory, and memory to peripherals; 2 DMA controllers support the management of ring buffers to avoid interrupts generated when the controller transfer reaches the end of the buffer.
Each channel has dedicated hardware DMA request logic, and each channel can also be triggered by software. The transfer length, source address and destination address of each channel can be separately. set by software.
DMA can be used for the main peripherals: SPI, I2C, USART, advanced/general/basic timer TIMx, DAC, I2S, SDIO, ADC.

2.12 Real-time Clock (RTC)

RTC is a set of continuously running counters with a built-in calendar clock module that can provide. perpetual calendar functions, it also has alarm interrupt and periodic interrupt (minimum 2 clock cycles) functions. RTC can be powered via VDD or VBAT pin, when VDD is valid, VDD is selected for power supply, otherwise it is powered by the VBAT pin, automatically selected, and switched by hardware. RTC will not be reset by the system or power reset source, nor will it be reset when waking up from STANDBY mode.
The drive clock of RTC can be selected as 32.768KHz external crystal oscillator, internal low power. 40KHz RC oscillator, or an arbitrary high-speed external clock divided by 128. For application scenarios that require very high timing accuracy, it is recommended to use an external 32.768KHz clock as the clock source, meanwhile, to compensate for the clock deviation of natural crystals, a 256Hz signal can be output to calibrate the clock of RTC. RTC has a 22-bit prescaler for time base clock, by default, when the clock is 32.768kHz, it will generate a time reference of 1 second. In addition, RTC can be used to trigger wake-up in low power states.

2.13 Timers and Watchdogs

Up to 2 advanced control timers, 4 general timers and 2 basic timers, as well as 2 watchdog timers and 1 systick timer.

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The table below compares the functions of advanced control timers, general timers and basic timers:

Table 2-1 Comparison of Timer Functions

Timer	Counter Resolution	Counter Type	Prescaler Value	Generate DMA Request	Capture/Compare Channel	ComplementaryOutput
TIM1 TIM8	16位	Up, Down, Up/Down	Any integer between 1 and 65536	Yes	4	Yes
TIM2 TIM3 TIM4 TIM5	16位	Up, Down, Up/Down	Any integer between 1 and 65536	Yes	4	No
TIM6 TIM7	16位	Up	Any integer between 1 and 65536	Yes	0	No

2.13.1 Basic Timers (TIM6 and TIM7)

The basic timers TIM6 and TIM7 each contain a 16-bit auto-reload counter. These 2 timers are independent of each other and do not share any resources. The basic timer can provide time reference for the general timer. It is directly connected to the DAC internally and directly drives the DAC through the trigger output.

The main functions of the basic timer are as follows:

- 16-bit auto-reload up counter
- 16-bit programmable prescaler (prescaler factor can be configured to any value between 1 and 65536)
- Synchronization circuit for triggering DAC
- Generate interrupt/DMA request on update event.

2.13.2 General Timers (TIMx)

4 general timers (TIM2, TIM3, TIM4 and TIM5) are mainly used for the following occasions: counting input signals, measuring pulse width of input signals, and generating output waveforms, etc.
The main functions of the general timer include:

- 16-bit auto-reload counter (can realize up counting, down counting, up/down counting)
- 16-bit programmable prescaler (prescaler factor can be configured to any value between 1 and 65536)
- TIM2, TIM3, TIM4 and TIM5 support up to 4 channels.
- Channel working mode: PWM output, output compare, single pulse mode output, input capture.
- Generate interrupt/DMA when the following events occur:
  - Update event.
  - Trigger event.
  - Trigger event.
  - Trigger event.
- Timer can be controlled by external signal.
- Connecting multiple timers to achieve timer synchronization or linking.
- Incremental (quadrature) encoder interface: used to track the running trajectory and parse the rotation orien tation.
- Hall sensor interface: used for three-phase motor control.

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- Support capturing internal comparator output signal.

2.13.3 Advanced Control Timers (TIM1 and TIM8)

Advanced control timers (TIM1 and TIM8) are mainly used for the following occasions: counting input signals, measuring pulse width of input signals, and generating output waveforms, etc.
The advanced timer has complementary output function, dead-time insertion and brake function. Suitable for motor control.
The main functions of the advanced timer include:

- 16-bit auto-reload counter. (can realize up counting, down counting, up/down counting)
- 16-bit programmable prescaler. (prescaler factor can be configured to any value between 1 and 65536)
- Programmable repetition counter
- TIM1 supports up to 6 channels, TIM8 supports up to 6 channels.
- 4 capture/compare channels, working mode: PWM output, output compare, single pulse mode output, input capture.
- 4 capture/compare channels, working mode: PWM output, output compare, single pulse mode output, input capture：
  - Update event.
  - Trigger event.
  - Input capture.
  - Output compares.
  - Brake signal input.
- Complementary output with programmable dead time
  - For TIM1, TIM8, channels 1, 2, 3 support this function.
- Timer can be controlled by external signal.
- Connecting multiple timers to achieve timer synchronization or linking.
- Incremental (quadrature) encoder interface: used to track the running trajectory and parse the rotation orientation.
- Hall sensor interface: used for three-phase motor control.

2.13.4 System Time Base Timer (Systick)

This timer is dedicated to real-time operating systems and can also be used as a standard decrementing counter.
It has the following characteristics:

- 24-bit decrementing counter
- Automatic reload function.
- Can generate a maskable system interrupt when the counter is 0

  Programmable clock source

2.13.5 Watchdog Timers (WDG)

Independent Watchdog (IWDG)
The independent watchdog is based on a 12-bit decrementing counter and a 3-bit prescaler, driven by an independent low-speed RC oscillator. It remains effective even if the main clock fails, and can work in STOP0, STOP2 and STANDBY modes. Once activated, if the watchdog is not fed (clearing the watchdog counter) within the set time, it will generate a reset when the counter counts to 0x000. It can be used to reset the entire system when an application problem occurs, or as a free timer to provide timeout management for the application. The watchdog can be configured to be started by software or hardware through option bytes. Reset and low-power wake-up are configurable.

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Window Watchdog (IWDG)

The window watchdog is commonly used to monitor software faults caused by external interference or unforeseen logic conditions that cause the application to deviate from the normal operating sequence. Unless the decrementing counter value is refreshed before the T6 bits become 0, the watchdog circuit will generate an MCU reset when the preset time period is reached. If the 7-bit decrementing counter value (in the control register) is refreshed before the decrementing counter reaches the value of the window register, an MCU reset will also be generated. This indicates that the decrementing counter needs to be refreshed within a limited time window.

Main features:

- WWDG is driven by a clock divided from APB1 clock.
- Programmable free-running decrementing counter.
- Condiftional reset：
  - Generates a reset when the decrementing counter value is less than 0x40 (if the watchdog is started)
  - Generates a reset when the decrementing counter is reloaded outside the window (if the watchdog is st arted)
  - If the watchdog is started and interrupts are allowed, an early wake-up interrupt (EWINT) is generated when the decrementing counter equals 0x40, which can be used to reload the counter toavoi d WWDG reset.

2.14 I²C Bus Interface

Up to 4 independent I2C bus interfaces, providing multi-master functionality, controlling all I2C bus specific ti ming, protocols, arbitration and timing. Supports multiple communication rate modes (up to 1MHz), supports D MA operations, and is compatible with SMBus 2.0. The I2C module has multiple uses, including generation an d verification of CRC codes, SMBus (System Management Bus) and PMBus (Power Management Bus).

- The main functions of the I2C interface are described as follows:
- Multi-master capability: the module can act as either a master device or a slave device;
- I2C master device capabilities:
  - Generates clock.
  - Generates start and stop conditions.
- I2C slave device capabilities:
  - Programmable address detection.
  - I2C interface supports 7-bit or 10-bit addressing, 7-bit slave mode supports dual slave address response capability.
  - Stop bit detection.
- Generate and detect 7-bit/10-bit addresses and broadcast calls.
- Support different communication speeds.
  - Standard speed (up to 100 kHz)
  - Fast (up to 400 kHz)
  - Fast+ (up to 1MHz)
- Status flags:
  - Transmitter/receiver mode flag.
  - Byte transmission complete flag.
  - I2C bus busy flag.
- Error flags:
  - Arbitration lost in master mode.

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  - Acknowledge (ACK) error after address/data transfer.
  - Misplaced start or stop condition detected.
  - Overflow or underflow when clock stretching is disabled.
- 2 interrupt vectors:
  - 1 interrupt for successful address/data communication.
  - 1 interrupt for errors.
- Optional clock stretching feature.
- Single byte buffer with DMA.
- Configurable PEC (Packet Error Checking) generation or verification
- In transmit mode, PEC value can be transmitted as the last byte.
- PEC error checking for the last received byte.
- Compliant with SMBus 2.0
  - 25 ms clock low timeout
  - 10 ms master device cumulative clock low extend time.
  - 25 ms slave device cumulative clock low extend time.
  - Hardware PEC generation/verification with ACK control
  - Supports address resolution protocol (ARP)
- Compliant with PMBus

2.15 Universal Synchronous/Asynchronous Receiver Transmitter (USART)

The N32G451 series integrates 7 serial transceiver interfaces, including 3 universal synchronous/asynchronous receiver transmitters (USART1, USART2 and USART3), and 4 universal asynchronous receiver transmitters (UART4, UART5, UART6, UART7). These 7 interfaces provide asynchronous communication, support IrDA SIR ENDEC transceiver encoding/decoding, multi-processor communication mode, single-wire half-duplex communication mode and LIN master/slave functionality.
The USART1/ UART6/UART7 interface communication rate can reach 4.5Mbit/s, and the communication rate of other interfaces can reach 2.25Mbit/s.
USART1, USART2 and USART3 interfaces have hardware CTS and RTS signal management, ISO7816 compatible smart card mode and SPI-like communication mode, all interfaces can use DMA operations.
The main features of USART are as follows:

- Full-duplex, asynchronous communication
- NRZ standard format
- Fractional baud rate generator system, programmable baud rate, for transmit and receive, up to 4.5Mbits/s
- Programmable data word length (8-bit or 9-bit)
- Configurable stop bits, supporting 1 or 2 stop bits.
- LIN master capability to send synchronous break and LIN slave to detect break, when USART hardware i s configured as LIN, generates 13-bit break, detects 10/11-bit break.
- Output transmit clock for synchronous transmission.
- IRDA SIR encoder/decoder, supporting 3/16-bit duration in normal mode.
- Smart card emulation functionality
  - Smart card interface supports ISO7816-3 standard defined asynchronous smart card protocol.
  - 0.5 and 1.5 stop bits used for smart card.
- Single-wire half-duplex communication
- Configurable multi-buffer communication using DMA, receiving/transmitting bytes in SRAM using centraliz

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ed DMA buffer.

- Independent transmitter and receiver enable bits.
- Detection flags
  - Receive buffer full.
  - Transmit buffer empty.
  - Transmission complete flag
- Parity control
  - Transmit parity bit.
  - Perform parity check on received data.
- Four error detection flags
  - Overrun error.
  - Noise error
  - Frame error.
  - Parity error
- 10 USART interrupt sources with flags
  - CTS change
  - LIN break detection
  - Transmit data register empty.
  - Transmission complete
  - Receive data register full.
  - Idle line detected.
  - Overrun error.
  - Frame error.
  - Noise error
  - Parity error
- Multi-processor communication, enter mute mode if address does not match.
- Wake up from mute mode (via idle line detection or address flag detection)
- Mode configuration:

USART Mode	USART1	USART2	USART3	UART4	UART5	UART6	UART7
Asynchronous mode	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Hardware flow control	Yes	Yes	Yes	No	No	No	No
Multi-buffer communication (DMA)	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Multi-processor communication	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Synchronous	Yes	Yes	Yes	No	No	No	No
Smart card	Yes	Yes	Yes	No	No	No	No
Half-duplex (single-wire mode)	Yes	Yes	Yes	Yes	Yes	Yes	Yes
IrDA	Yes	Yes	Yes	Yes	Yes	Yes	Yes
LIN	Yes	Yes	Yes	Yes	Yes	Yes	Yes

2.16 Serial Peripheral Interface (SPI)

Supports 3 SPI interfaces that can be used as I^2^S interfaces, with SPI and I^2^S sharing resources.
SPI allows the chip to communicate with external devices in a half/full-duplex, synchronous, serial manner. This interface can be configured as master mode and provide communication clock (SCK) to external slave devices. The interface can also work in a multi-master configuration. It can be used for various purposes, including synchronous transmission with a bidirectional data line, and reliable communication using CRC check.

The main functions of the SPI interface are as follows:

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- 3-wire full-duplex synchronous transmission
- Dual-wire unidirectional synchronous transmission with or without a third bidirectional data line
- 8-bit or 16-bit transfer frame format selection
- Master or slave operation
- Support for multi-master mode.
- 8 master mode baud rate prescaler coefficients (maximum is fPCLK/2)
- Slave mode frequency (maximum is fPCLK/2)
- Fast communication in master and slave mode
- NSS management by software or hardware in both master and slave modes: dynamic change of master/slave operation mode
- Programmable clock polarity and phase
- Programmable data order, MSB first or LSB first
- Dedicated transmit and receive flags that can trigger interrupts.
- SPI bus busy status flag
- Hardware CRC for reliable communication
  - In transmit mode, CRC value can be sent as the last byte.
  - In full-duplex mode, automatic CRC check is performed on the last received byte.
- Master mode failure, overload, and CRC error flags that can trigger interrupts.
- Single byte transmit and receive buffer supporting DMA functionality: generating transmit and receive requests
- Maximum interface speed: SPI1 interface 36Mbps, SPI2/SPI3 interface 18Mbps

2.17 Serial Audio Interface(I^2S)

I2S is a 3-wire synchronous serial interface communication protocol. The chip integrates 2 standard I2S interfaces (multiplexed with SPI2 and SPI3) that can work in master or slave mode. These 2 interfaces can be configured for 16-bit, 24-bit or 32-bit transfers, and can be configured as input or output channels, supporting audio sampling rates from 8kHz to 96kHz. It supports four audio standards, including Philips I^2^S standard, MSB and LSB aligned standards, and PCM standard.

In half-duplex communication, it can work in 2 modes: master and slave. When it acts as a master device, it provides clock signals to external slave devices through the interface.

The main functions of the I2S interface are as follows:

- Simplex communication (transmit or receive only)
- Master or slave operation
- 8-bit linear programmable prescaler, obtains precise audio sampling rate (8KHz to 96kHz)
- Data format can be 16-bit, 24-bit or 32-bit.
- Fixed audio channel data packet frame is 16-bit (16-bit data frame) or 32-bit (16, 24 or 32-bit data frame)
- Programmable clock polarity (steady state)
- Underflow flag in slave transmit mode and overflow flag in master/slave receive mode.

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- 16-bit data register for transmit and receive, one register at each end of the channel
- Supported I2S protocols:
  - I2S Philips standard
  - MSB align standard (left align)
  - LSB align standard (right align)
  - PCM standard (long or short frame sync on 16-bit channel frame or 16-bit data frame extended to 32-bit channel frame)
- Data direction is always MSB first
- Both transmit and receive have DMA capability.
- Master clock can be output to external audio device, ratio fixed at 256xFs (Fs is audio sampling rate)

2.18 Secure Digital Input Output Interface (SDIO)

Secure Digital Input and Output, abbreviated as SDIO, the SDIO host interface provides an operating interface between the AHB peripheral bus and multimedia card (MMC), SD memory card, SDIO card devices.

SDIO host features are as follows:

- Supports "MultiMediaCard System Specification Version 4.2", supports 1-bit (default), 4-bit and 8-bit data bus, backward compatible with earlier MMC protocols.
- Supports "SD Memory Card Specifications Version 2.0"
- Supports "SD I/O Card Specification Version 2.0", supports 1-bit (default) and 4-bit data format.
- SDIO clock rate up to 48MHz
- SDIO does not support SPI communication mode.

2.19 Controller Area Network (CAN)

Supports 1 CAN bus interface, compatible with specifications 2.0A and 2.0B (active), bit rate up to 1Mbps. It can receive and send standard frames with 11-bit identifiers and can also receive and send extended frames with 29-bit identifiers.

Main features:

- Supports CAN protocol 2.0A and 2.0B active mode.
- Baudrate is up to 1Mbps
- Supports time triggered communication function.
- Transmit
  - 3 transmit mailboxes.
  - Priority feature of transmit message can be software configured.
  - Records timestamp of transmit SOF moment.
- Receive
  - Two receive FIFOs with 3-level depth.
  - Variable filter group
  - Has 14 filter groups
  - Identifier list
  - FIFO overflow handling mode configurable
  - Records timestamp of receive SOF moment.
- Time triggered communication mode

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  - Automatic retransmission mode is now allowed.
  - 16-bit free running timer
  - Can send timestamp in last 2 data bytes.
- Management
  - Interrupt can be masked.
    Mailbox occupies a separate address space, convenient for improving software efficiency.

2.20 Universal Serial Bus (USB)

The N32G451 series integrates a full-speed USB compatible device controller that follows full-speed USB device (12Mbit/s) standards, endpoints can be configured by software, and has suspend/wake-up functions. The dedicated 48MHz clock for USB is directly generated by the internal main PLL (to ensure communication stability, the clock source must be HSE external high-speed crystal).

The main features of the USB device controller are as follows:
- Compliant with USB2.0 full-speed device technical specifications
- Configurable 1 to 8 USB endpoints
- CRC (Cyclic Redundancy Check) generation/verification, Non-Return-to-Zero Inverted (NRZI) encoding/decoding and bit stuffing
- Supports dual-buffer mechanism for bulk/synchronous endpoints.
- Supports USB suspend/wake-up operation.
- Frame lock clock pulse generation.

  Supports internal 1.5K pull-up resistor on USB DP signal line (firmware controlled), accuracy ±5%

2.21 General Purpose Input Output Interface (GPIO)

Supports up to 80 GPIOs, divided into 5 groups (GPIOA/GPIOB/GPIOC/GPIOD/GPIOE), 16 ports per group. Each GPIO pin can be configured by software as output (push-pull or open-drain), input (with or without pull-up or pull-down) or multiplexed peripheral function port, and most GPIO pins are multiplexed with digital or analog peripherals, and some I/O pins are also multiplexed with clock pins; except for ports with analog input functions, all GPIO pins have large current pass-through capability.

The main features of GPIO are described as follows:
- Each bit of the GPIO port can be configured by software into multiple modes:
  - Input floating.
  - Input pull-up (weak pull-up)
  - Input pull-down (weak pull-down)
  - Analog input
  - Open-drain output
  - Push-pull output.
  - Push-pull multiplexed function.
  - Open drain multiplexed function
- General I/O (GPIO)
  - During and immediately after reset, multiplexed function is not enabled, except BOOT0 and BOOT1 (BOOT0 and BOOT1 are input pull-down), I/O ports are configured in analog input mode
  - During and immediately after reset, multiplexed function is not enabled, I/O ports are configured in analog input mode, after reset, JTAG pins are placed in input pull-up or pull-down mode.
    - JTDI placed in pull-up mode.
    - JTCK placed in pull-down mode.
    - JTMS placed in pull-up mode.

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  - NJTRST placed in pull-up mode.
- When configured as output, the value written to the output data register is output to the corresponding I/O pin. Can be output in push-pull or open-drain mode.

- Individual bit set or clear function.
- External interrupt/wake-up: all ports have external interrupt capability, to use the external interrupt. line, the port must be configured in input mode!
- Multiplexed function: must program the port bit configuration register before using the default multiplexed function
- GPIO lock mechanism, lock mechanism allows freezing IO configuration. When a lock (LOCK) program is executed on a port bit, the configuration of the port bit cannot be changed again until the next reset

2.22 Analog-to-Digital Converter (ADC)

Supports up to 3 12-bit 4.7Msps sampling rate successive approximation ADCs, supporting single-ended and differential inputs, capable of measuring 18 external and 3 internal signal sources, of which ADC1 supports 9 external channels, ADC2 supports 12 external channels, and ADC3 supports 15 external channels.

The main features of ADC are described as follows:

- Supports configurable 12-bit, 10-bit, 8-bit, 6-bit resolution.
  - Maximum sampling rate of 4.7 MSPS at 12-bit resolution
  - Maximum sampling rate of 6.1 MSPS at 10-bit resolution
  - Maximum sampling rate of 7.3 MSPS at 8-bit resolution
  - Maximum sampling rate of 8.9 MSPS at 6-bit resolution
- ADC clock sources are divided into working clock, sampling clock and timing clock.
  - Only AHB_CLK can be configured as the working clock source, up to 144 MHz.
  - PLL can be configured as the sampling clock source, up to 80 MHz, supporting divisions of 1, 2, 4, 6, 8, 10, 12, 16, 32, 32, 64, 128, 256.
  - AHB_CLK can be configured as the sampling clock source, up to 80 MHz, supporting divisions of 1, 2, 4, 6, 8, 10, 12, 16, 32.
  - The timing clock is used for internal timing functions and must be configured to 1 MHz.
- Supports timer-triggered ADC sampling.
- Generates interrupts upon conversion completion, injected conversion completion, and analog watchdog event occurrence.
- Single and continuous conversion modes
- Automatic scanning mode from channel 0 to channel N
- Supports self-calibration.
- Data alignment with embedded data consistency
- Sampling intervals can be programmed separately for each channel.
- External trigger options for both regular and injected conversions
- Discontinuous mode
- Dual mode, combining ADC1 and ADC2
- ADC power supply requirement: 1.8V to 3.6V
- ADC input range: VREF- ≤ VIN ≤ VREF+
- ADC can be operated with DMA, generating DMA requests during regular channel conversion.

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- Analog watchdog function, capable of monitoring one, multiple or all selected channels with high precision. Generates an interruption when the monitored signal exceeds the preset threshold.

2.23 Digital-to-Analog Converter (DAC)

Supports 2 digital-to-analog converters (DAC) with 12-bit digital input and voltage output. The DAC module has 2 output channels, each with a separate converter. The 2 DACs can be used simultaneously without affecting each other. DAC can input a reference voltage VREF+ via a pin to obtain more accurate conversion results.

This dual digital interface supports the following functions:

- Two DAC converters: each with an output channel
- Configurable 8-bit or 12-bit output
- Configurable left or right data alignment in 12-bit mode
- Synchronous update function
- Generates noise waves.
- Generates triangular waves.
- Independent or synchronous conversion of dual DAC channels
- DMA function available for each channel
- External trigger for conversion
  Input reference voltage VREF+

2.24 Temperature Sensor (TS)

The temperature sensor produces a voltage that varies linearly with temperature, with a conversion range between 1.8V < VDDA < 3.6V. The temperature sensor is internally connected to the ADC1_IN16 input channel for converting the sensor's output to a digital value.

2.25 Cyclic Redundancy Check Calculation Unit (CRC)

Integrated CRC32 and CRC16 functions. The cyclic redundancy check (CRC) calculation unit obtains any CRC calculation result based on a fixed generating polynomial. In many applications, CRC-based techniques are used to verify the consistency of data transmission or storage. Within the scope of the EN/IEC 60335-1 standard, it provides a means to detect flash memory errors. The CRC unit can be used to calculate software signatures in real time and compare them with signatures generated during linking and generation of the software.

The main features of the CRC are as follows:

- CRC16：Supports polynomial $X^{16}+X^{15}+X^2+X^0$
- CRC32：Supports polynomial $X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$
- CRC16 calculation time: 1 AHB clock cycle (HCLK)
- CRC32 calculation time: 1 AHB clock cycle (HCLK)
- Configurable cyclic redundancy calculation initial value
  Supports DMA mode.

2.26 Algorithm Hardware Acceleration Engine (SAC)

Embedded with a hardware acceleration engine for algorithms, supporting acceleration of various international algorithms and national cryptographic symmetric encryption algorithms and hash algorithms, greatly improving encryption and decryption speed compared to pure software algorithms.

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Hardware supported algorithms are as follows:

- Supports DES symmetric algorithm.
  - Supports DES and 3DES encryption and decryption operations.
  - TDES supports 2KEY and 3KEY modes.
  - Supports CBC and ECB modes.
- Supports AES symmetric algorithm.
  - Supports 128-bit/192-bit/256-bit key lengths.
  - Supports CBC, ECB, CTR modes.
- Supports SHA hash algorithm.
  - Supports SHA1/SHA224/SHA256
- Supports MD5 digest algorithm.

2.27 Unique Device Serial Number (UID)

The N32G451 series products have two unique device serial numbers of different lengths built-in, a 96-bit UID (Unique device ID) and a 128-bit UCID (Unique Customer ID). These two device serial numbers are stored in the system configuration block of the flash memory. The information they contain is written at the factory and guaranteed to be unique for any N32G451 series microcontroller under any circumstances. The user application or external device can read them through the CPU or JTAG/SWD interface and cannot be modified.

The 96-bit UID is commonly used as a serial number or password. When writing to flash, combining this unique identifier with a software encryption/decryption algorithm further enhances the security of the code in the flash memory.

The 128-bit UCID follows the national technical chip serial number definition and contains chip production and version related information.

2.28 Serial Wire JTAG Debug Port (SWJ-DP)

Integrated with ARM's SWJ-DP interface, which combines the JTAG and Serial Wire Debug interfaces, allowing connection via a Serial Wire Debug interface or JTAG interface. The JTAG JTMS and JTCK signals share pins with SWDIO and SWCLK respectively. A special signal sequence on the JTMS pin is used to switch between JTAG-DP and SW-DP.

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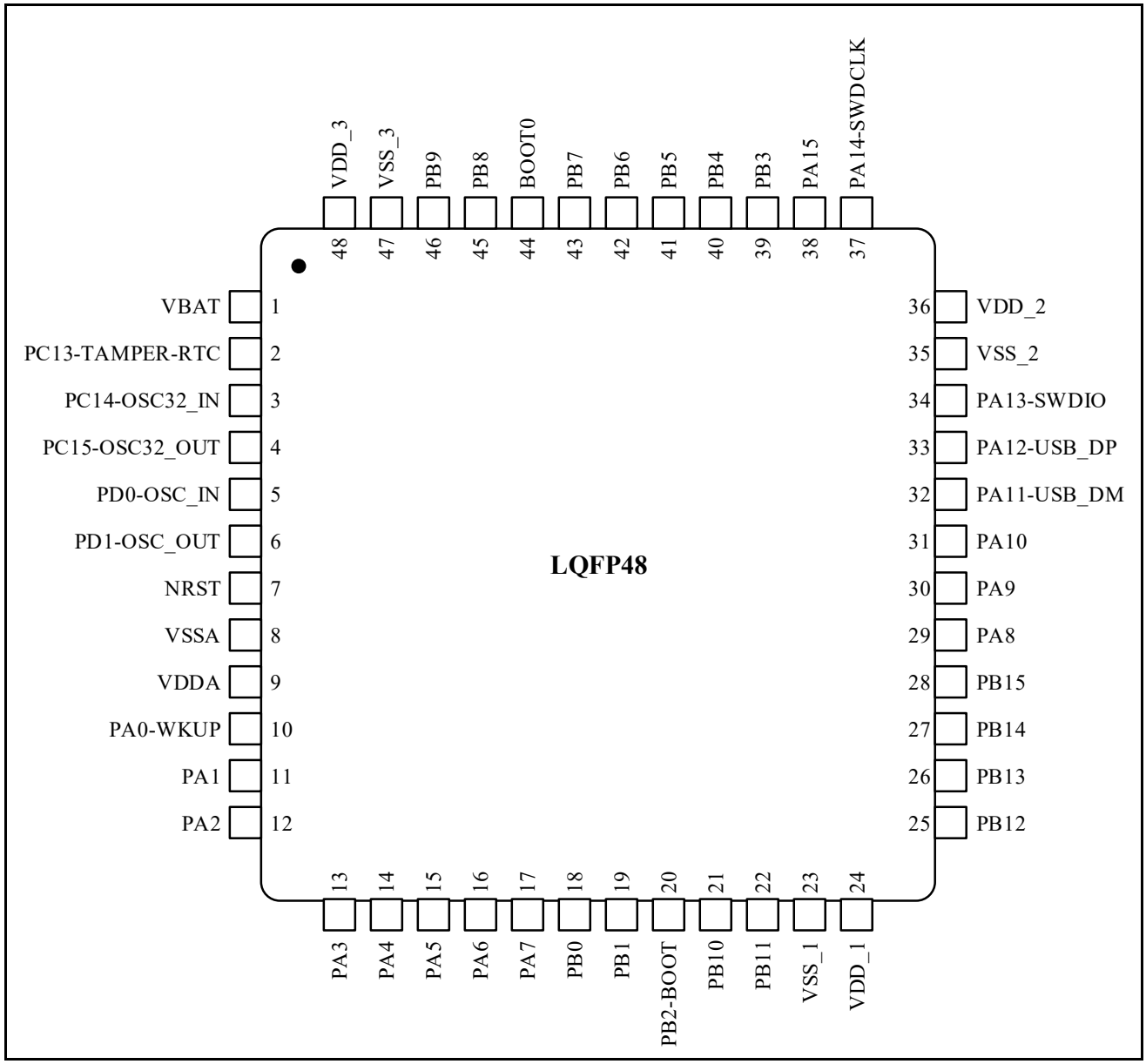
3 Pin Definitions and Descriptors

3.1 Package Diagrams

3.1.1 LQFP48

Figure 3-1 N32G451 Series LQFP48Pin Distribution



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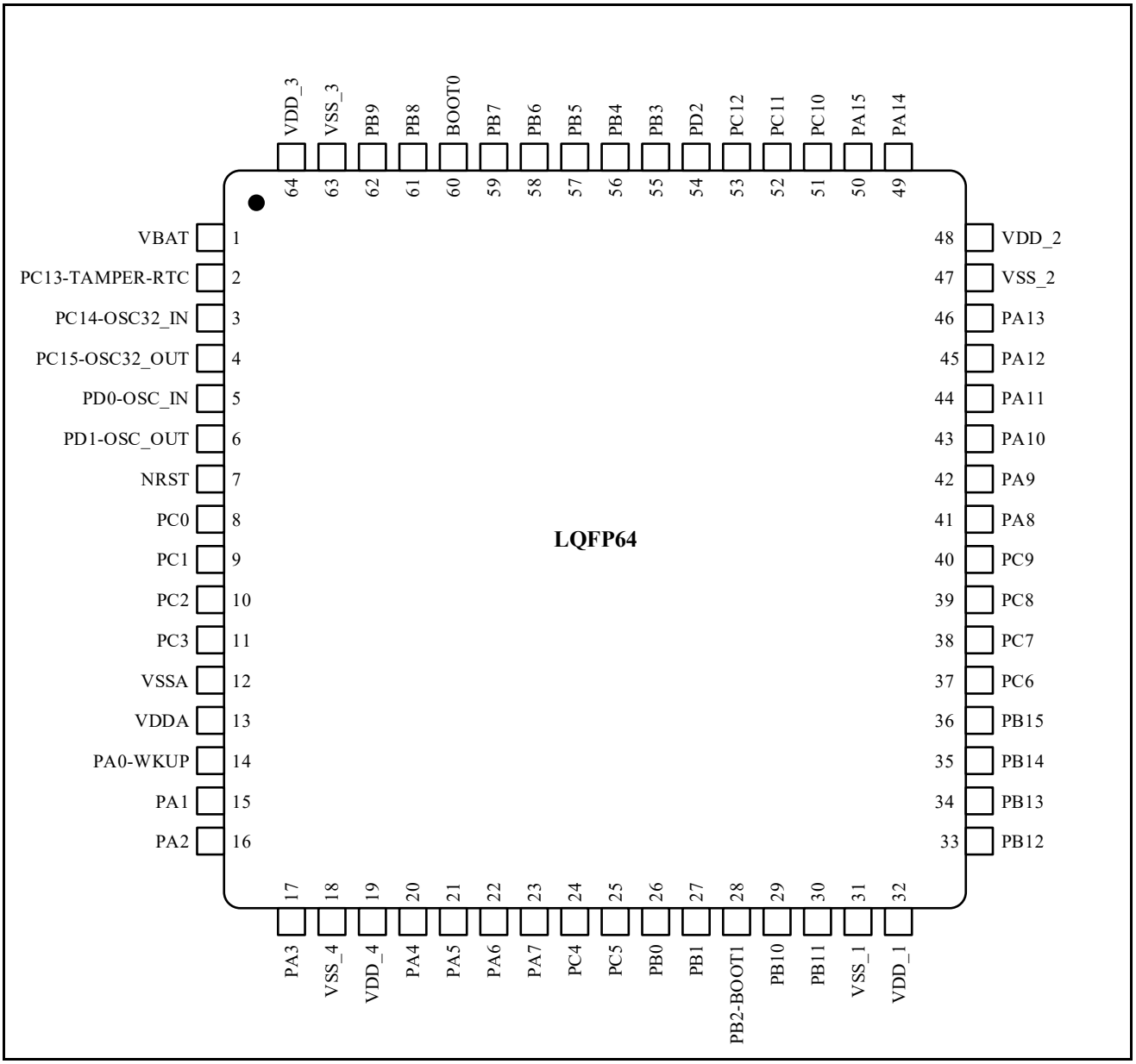
3.1.2 LQFP64

Figure 3-2 N32G451Series LQFP64 Pin Distribution



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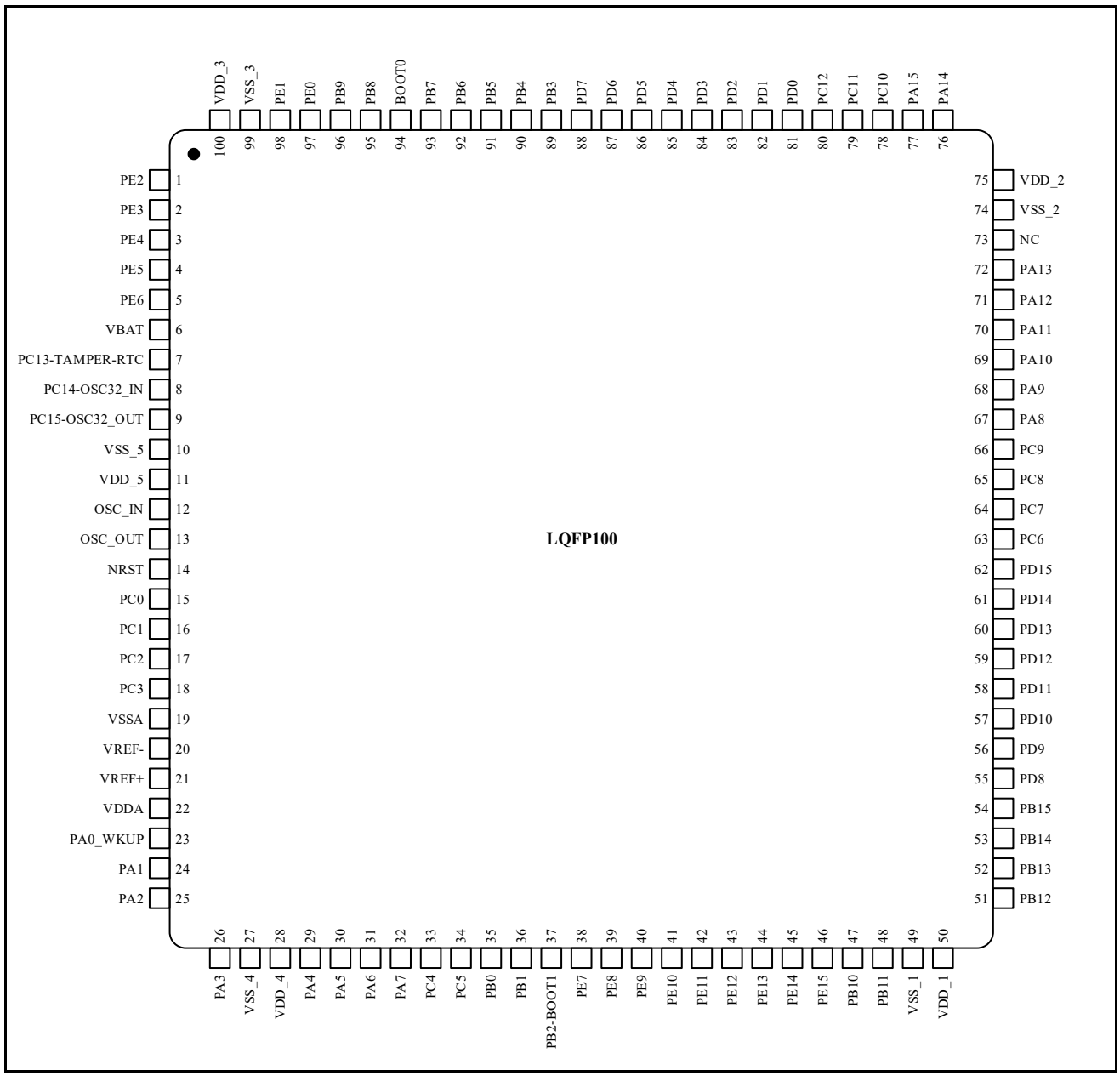
3.1.3 LQFP100

Figure 3-3 N32G451 Series LQFP100 Pin Distribution



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3.2 Pin Multiplexing Definitions

Table 3-1 Pin Definitions

Package			Pin Name	Type[1]	I/OStruccture [2]	Fail-safe(8) Support	Main Function[3] (After Reset)	Optional reuse function[6]	
LQFP48	LQFP64	LQFP100						Default	Redefinition
-	-	1	PE2	I/O	FT	Yes	PE2	UART6_TX	-
-	-	2	PE3	I/O	FT	Yes	PE3	UART6_RX	-
-	-	3	PE4	I/O	FT	Yes	PE4	-	-
-	-	4	PE5	I/O	FT	Yes	PE5	-	-
-	-	5	PE6	I/O	FT	Yes	PE6	-	-
1	1	6	VBAT	S	-	-	VBAT	-	-
2	2	7	PC13-TAMPER- RTC[4]	I/O	TC	Yes	PC13[5]	TAMPER-RTC	-
3	3	8	PC14- OSC32_IN[4]	I/O	TC	Yes	PC14[5]	OSC32_IN	-
4	4	9	PC15- OSC32_OUT[4]	I/O	TC	Yes	PC15[5]	OSC32_OUT	-
-	-	10	VSS_5	S	-	-	VSS_5	-	-
-	-	11	VDD_5	S	-	-	VDD_5	-	-
5	5	12	OSC_IN[7]	I	TC	Yes	OSC_IN	-	-
6	6	13	OSC_OUT[7]	O	TC	No	OSC_OUT	-	-
7	7	14	NRST	I/O	-	-	NRST	-	-
-	8	15	PC0	I/O	TTa	No	PC0	ADC12_IN6[10] I2C3_SCL	UART6_TX
-	9	16	PC1	I/O	TTa	No	PC1	ADC12_IN7[10] I2C3_SDA	UART6_RX
-	10	17	PC2	I/O	TTa	No	PC2	ADC12_IN8[10]	UART7_TX SPI3_NSS I2S3_WS
-	11	18	PC3	I/O	TTa	No	PC3	ADC12_IN9[10]	UART7_RX SPI3_SCK I2S3_CK
8	12	19	VSSA	S	-	-	VSSA	-	-
		20	VREF-	S	-	-	VREF-	-	-
9	13	21	VREF+	S	-	-	VREF+	-	-
		22	VDDA	S	-	-	VDDA	-	-
10	14	23	PA0-WKUP	I/O	TTa	No	PA0	WKUP USART2_CTS ADC1_IN1[9] TIM2_CH1_ETR TIM5_CH1 TIM8_ETR	SPI3_MISO
11	15	24	PA1	I/O	TTa	No	PA1	USART2_RTS ADC1_IN2[9] TIM5_CH2 TIM2_CH2	SPI3_MOSI I2S3_SD

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Package			Pin Name	Type[1]	I/OStruccture [2]	Fail-safe(8) Support	Main Function[3] (After Reset)	Optional reuse function[6]	
LQFP48	LQFP64	LQFP100						Default	Redefinition
12	16	25	PA2	I/O	TTa	No	PA2	USART2_TX TIM5_CH3 ADC12_IN11[10] TIM2_CH3	-
13	17	26	PA3	I/O	TTa	No	PA3	USART2_RX TIM5_CH4 ADC1_IN4[9] TIM2_CH4	-
-	18	27	VSS_4	S	-	-	VSS_4	-	-
-	19	28	VDD_4	S	-	-	VDD_4	-	-
14	20	29	PA4	I/O	TTa	No	PA4	SPI1_NSS USART2_CK DAC_OUT1 ADC2_IN1[9]	I2C2_SCL
15	21	30	PA5	I/O	TTa	No	PA5	SPI1_SCK DAC_OUT2 ADC2_IN2[9]	I2C2_SDA
16	22	31	PA6	I/O	TTa	No	PA6	SPI1_MISO TIM8_BKIN ADC1_IN3[9] TIM3_CH1	TIM1_BKIN
17	23	32	PA7	I/O	TTa	No	PA7	SPI1_MOSI TIM8_CH1N ADC2_IN4[9] TIM3_CH2	TIM1_CH1N
-	24	33	PC4	I/O	TTa	No	PC4	ADC2_IN5[9] UART7_TX	I2C3_SCL
-	25	34	PC5	I/O	TTa	No	PC5	ADC2_IN12[10] UART7_RX	I2C3_SDA
18	26	35	PB0	I/O	TC	No	PB0	ADC3_IN12[10] TIM3_CH3 TIM8_CH2N	TIM1_CH2N UART6_TX
19	27	36	PB1	I/O	TTa	No	PB1	ADC2_IN3[9] TIM3_CH4 TIM8_CH3N	TIM1_CH3N UART6_RX
20	28	37	PB2	I/O	TTa	No	PB2/BOOT1	ADC2_IN13[10]	UART4_TX SPI1_NSS
-	-	38	PE7	I/O	TC	No	PE7	ADC3_IN13[10]	TIM1_ETR UART4_RX SPI1_SCK
-	-	39	PE8	I/O	TC	No	PE8	ADC3_IN6 [10]	TIM1_CH1N UART5_TX SDIO_DAT0 SPI1_MISO
-	-	40	PE9	I/O	TC	No	PE9	ADC3_IN2[9]	TIM1_CH1 UART5_RX SDIO_DAT1 SPI1_MOSI

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Package			Pin Name	Type[1]	I/OStruccture [2]	Fail-safe(8) Support	Main Function[3] (After Reset)	Optional reuse function[6]	
LQFP48	LQFP64	LQFP100						Default	Redefinition
-	-	41	PE10	I/O	TC	No	PE10	ADC3_IN14[10]	TIM1_CH2N SDIO_DAT2 SPI2_NSS I2S2_WS
-	-	42	PE11	I/O	TC	No	PE11	ADC3_IN15[10]	TIM1_CH2 SDIO_DAT3 SPI2_SCK I2S2_CK
-	-	43	PE12	I/O	TC	No	PE12	ADC3_IN4[9]	TIM1_CH3N SDIO_CK SPI2_MISO
-	-	44	PE13	I/O	TC	No	PE13	ADC3_IN3[9]	TIM1_CH3 SPI2_MOSI I2S2_SD SDIO_CMD
-	-	45	PE14	I/O	TC	No	PE14	-	TIM1_CH4
-	-	46	PE15	I/O	TC	No	PE15	-	TIM1_BKIN
21	29	47	PB10	I/O	TC	Yes	PB10	I2C2_SCL USART3_TX	TIM2_CH3
22	30	48	PB11	I/O	TC	No	PB11	I2C2_SDA USART3_RX ADC3_IN1 [9]	TIM2_CH4
23	31	49	VSS_1	S	-	-	VSS_1	-	-
24	32	50	VDD_1	S	-	-	VDD_1	-	-
25	33	51	PB12	I/O	TC	No	PB12	SPI2_NSS I2S2_WS I2C2_SMBA USART3_CK TIM1_BKIN	-
26	34	52	PB13	I/O	TC	No	PB13	SPI2_SCK I2S2_CK USART3_CTS TIM1_CH1N ADC3_IN5[9]	UART5_TX
27	35	53	PB14	I/O	TC	No	PB14	SPI2_MISO TIM1_CH2N USART3_RTS	UART5_RX
28	36	54	PB15	I/O	TC	No	PB15	SPI2_MOSI I2S2_SD TIM1_CH3N	-
-	-	55	PD8	I/O	TC	No	PD8	-	USART3_TX SPI3_NSS I2S3_WS CAN1_RX
-	-	56	PD9	I/O	TC	No	PD9	-	USART3_RX SPI3_SCK I2S3_CK CAN1_TX

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Package			Pin Name	Type(1)	I/OStruccture (2)	Fail-safe(8) Support	Main Function(3) (After Reset)	Optional reuse function(6)	
LQFP48	LQFP64	LQFP100						Default	Redefinition
-	-	57	PD10	I/O	TC	No	PD10	ADC3_IN7(10)	USART3_CK
-	-	58	PD11	I/O	TC	No	PD11	ADC3_IN8(10)	USART3_CTS SPI3_MISO
-	-	59	PD12	I/O	TC	No	PD12	ADC3_IN9(10)	TIM4_CH1 USART3_RTS SPI3_MOSI I2S3_SD
-	-	60	PD13	I/O	TC	No	PD13	ADC3_IN10(10)	TIM4_CH2
-	-	61	PD14	I/O	TC	No	PD14	ADC3_IN11(10)	TIM4_CH3 I2C4_SCL TIM8_CH1
-	-	62	PD15	I/O	FT	Yes	PD15	-	TIM4_CH4 I2C4_SDA TIM8_CH2
-	37	63	PC6	I/O	TC	Yes	PC6	I2S2_MCK TIM8_CH1 SDIO_DAT6 I2C4_SCL	TIM3_CH1 SPI2_NSS I2S2_WS USART2_CTS
-	38	64	PC7	I/O	TC	Yes	PC7	I2S3_MCK TIM8_CH2 SDIO_DAT7 I2C4_SDA	TIM3_CH2 SPI2_SCK I2S2_CK USART2_RTS
-	39	65	PC8	I/O	TC	Yes	PC8	TIM8_CH3 SDIO_DAT0	TIM3_CH3 SPI2_MISO USART2_TX
-	40	66	PC9	I/O	TC	Yes	PC9	TIM8_CH4 SDIO_DAT1	TIM3_CH4 SPI2_MOSI I2S2_SD USART2_RX
29	41	67	PA8	I/O	FT	Yes	PA8	USART1_CK TIM1_CH1 MCO	-
30	42	68	PA9	I/O	FT	Yes	PA9	USART1_TX TIM1_CH2	I2C4_SCL
31	43	69	PA10	I/O	FT	Yes	PA10	USART1_RX TIM1_CH3	I2C4_SDA
32	44	70	PA11	I/O	FT	Yes	PA11	USART1_CTS USBDM CAN1_RX TIM1_CH4	-
33	45	71	PA12	I/O	FT	Yes	PA12	USART1_RTS USBDP CAN1_TX TIM1_ETR	-
34	46	72	PA13	I/O	FT	Yes	JTMS- SWDIO	-	PA13 UART4_TX
-	-	73	Not connected						
35	47	74	VSS_2	S	-	-	VSS_2	-	-

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Package			Pin Name	Type[1]	I/OStruccture [2]	Fail-safe(8) Support	Main Function[3] (After Reset)	Optional reuse function[6]	
LQFP48	LQFP64	LQFP100						Default	Redefinition
36	48	75	VDD_2	S	-	-	VDD_2	-	-
37	49	76	PA14	I/O	FT	Yes	JTCK- SWCLK	-	PA14 UART4_RX
38	50	77	PA15	I/O	FT	Yes	JTDI	SPI3_NSS I2S3_WS	TIM2_CH1_ETR PA15 SPI1_NSS USART2_CTS TIM8_CH1N
-	51	78	PC10	I/O	TC	Yes	PC10	UART4_TX SDIO_DAT2	USART3_TX SPI3_SCK I2S3_CK
-	52	79	PC11	I/O	TC	Yes	PC11	UART4_RX SDIO_DAT3	USART3_RX SPI3_MISO
-	53	80	PC12	I/O	TC	Yes	PC12	UART5_TX SDIO_CLK	USART3_CK SPI3_MOSI I2S3_SD TIM8_CH2N
-	-	81	PD0	I/O	FT	Yes	PD0[7]	-	CAN1_RX UART4_TX
-	-	82	PD1	I/O	FT	Yes	PD1[7]	-	CAN1_TX UART4_RX
-	54	83	PD2	I/O	TC	Yes	PD2	TIM3_ETR UART5_RX SDIO_CMD	SPI3_NSS I2S3_WS TIM8_CH3N
-	-	84	PD3	I/O	FT	Yes	PD3	-	USART2_CTS
-	-	85	PD4	I/O	TC	Yes	PD4	-	USART2_RTS
-	-	86	PD5	I/O	TC	Yes	PD5	-	USART2_TX
-	-	87	PD6	I/O	TC	Yes	PD6	-	USART2_RX
-	-	88	PD7	I/O	TC	Yes	PD7	-	USART2_CK
39	55	89	PB3	I/O	FT	Yes	JTDO	SPI3_SCK I2S3_CK	PB3 TRACESWO TIM2_CH2 SPI1_SCK USART2_RTS TIM8_BKIN
40	56	90	PB4	I/O	FT	Yes	NJTRST	SPI3_MISO	PB4 TIM3_CH1 SPI1_MIS O USART2_TX TIM8_ETR
41	57	91	PB5	I/O	FT	Yes	PB5	I2C1_SMBA SPI3_MOSI I2S3_SD	TIM3_CH2 SPI1_MOS I USART2_RX TIM1_BKIN
42	58	92	PB6	I/O	TC	Yes	PB6	I2C1_SCL TIM4_CH1	USART1_TX
43	59	93	PB7	I/O	TC	Yes	PB7	I2C1_SDA TIM4_CH2	USART1_RX
44	60	94	BOOT0	I	-	-	BOOT0	-	-
45	61	95	PB8	I/O	TC	Yes	PB8	TIM4_CH3 SDIO_DAT4	I2C1_SCL CAN1_RX UART5_TX
46	62	96	PB9	I/O	TC	Yes	PB9	TIM4_CH4 SDIO_DAT5	I2C1_SDA CAN1_TX UART5_RX
-	-	97	PE0	I/O	FT	Yes	PE0	TIM4_ETR	-
-	-	98	PE1	I/O	FT	Yes	PE1	-	-
47	63	99	VSS_3	S	-	-	VSS_3	-	-
48	64	100	VDD_3	S	-	-	VDD_3	-	-

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Notes:

(1) I = Input, O = Output, S = Power, HiZ = High Impedance

(2) FT: Tolerant to 5V; TTa: Tolerant to 3.3V, supports analog peripherals; TC: Common 3.3V I/O

(3) Some functions are only supported in certain chip models.

(4) The PC13, PC14 and PC15 pins are powered through a power switch, and this power switch can only absorb limited current (3mA). Therefore, when these three pins are used as output pins, they have the following restrictions: as output pins, they can only work in 2MHz mode, the maximum drive load is 30pF, and the total output current of the three pins cannot exceed 3mA.

(5) These pins are in the main function state under the backup domain at first power-on, and then even after reset, the state of these pins is controlled by the backup domain registers (these registers are not reset by the main reset system). For specific information on how to control these IO ports, please refer to the battery backup domain and BKP register chapters in the N32G45x User Reference Manual.

(6) Some multiplexed functions can be configured to other pins by software (if the corresponding package has this pin), please refer to the I/O chapter of multiplexed functions and the debug settings chapter in the N32G45x User Reference Manual for details.

(7) Pins 5 and 6 of the LQFP48/64 package are configured as OSC_IN and OSC_OUT function pins by default after chip reset. The software can reset these two pins to PD0 and PD1 functions, when used as PD0 and PD1, these two pins can only be used for common IO functions. However, for LQFP80/100/128 packages, since PD0 and PD1 are inherent function pins, there is no need for software to perform re-mapping settings. For more details, please refer to the I/O chapter of multiplexed functions and the debug settings chapter in the N32G45x User Reference Manual.

(8) Fail-safe means that when a high-level input is applied to the IO when the chip has no power input, there will be no phenomenon of high-level input pouring into the chip, resulting in a certain voltage on the power supply and consuming current.

(9) The corresponding ADC channel is a fast channel, supporting a maximum sampling rate of 5.14MSPS (12Bit).

(10) The corresponding ADC channel is a slow channel, supporting a maximum sampling rate of 4.23MSPS (12Bit).

Note: The pin names marked as ADC12_INx in the table indicate that this pin can be ADC1_INx or ADC2_INx. For example: ADC12_IN9 means that this pin can be configured as ADC1_IN9 or ADC2_IN9.

In the pin PA0 corresponding to the multiplexed function TIM2_CH1_ETR in the table, it means that this function can be configured as TIM2_TI1 or TIM2_ETR. Similarly, the PA15 corresponding to the name of the re-mapped multiplexed function TIM2_CH1_ETR has the same meaning.

For the FT ports in the table, it is necessary to ensure that the voltage difference between the IO voltage and the power supply voltage is less than 3.6V.

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4 Electrical Characteristics

4.1 Test Conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

4.1.1 Minmum and Maximum Values

Unless otherwise specified, all minimum and maximum values are guaranteed under worst-case environmental temperature, supply voltage, and clock frequency conditions through testing 100% of products on the production line at an ambient temperature of TA=25°C.

The data obtained through comprehensive evaluation, design simulation and/or process characteristics as indicated in the notes below each table are not tested on the production line; based on the comprehensive evaluation, the minimum and maximum values are obtained by taking the average value of the sample test and adding or subtracting three times the standard distribution (average±3∑).

4.1.2 Typical Values

Unless otherwise specified, typical data is based on TA=25°C and VDD=3.3V. This data has not been tested and is for user's design guidance only.

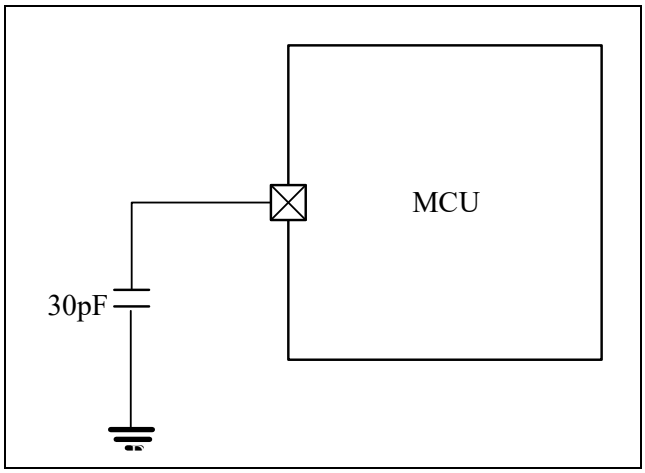
4.1.3 Typical Curves

Unless otherwise specified, these typical curves have not been tested and are for user's design guidance only.

4.1.4 Load Capacitance

The load conditions when measuring the pin parameters are shown in Figure 4-1.

Figure 4-1 Load cinditions for pins



4.1.5 Pin Input Voltage

The measurement method of the input voltage on the pin is shown in Figure 4-2.

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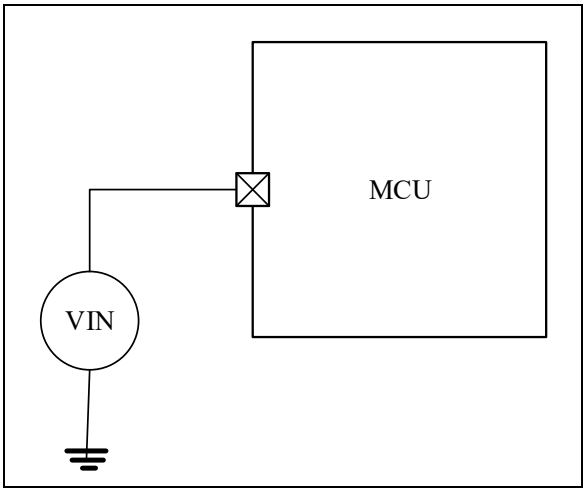
Figure 4-2 Pin Input Voltage



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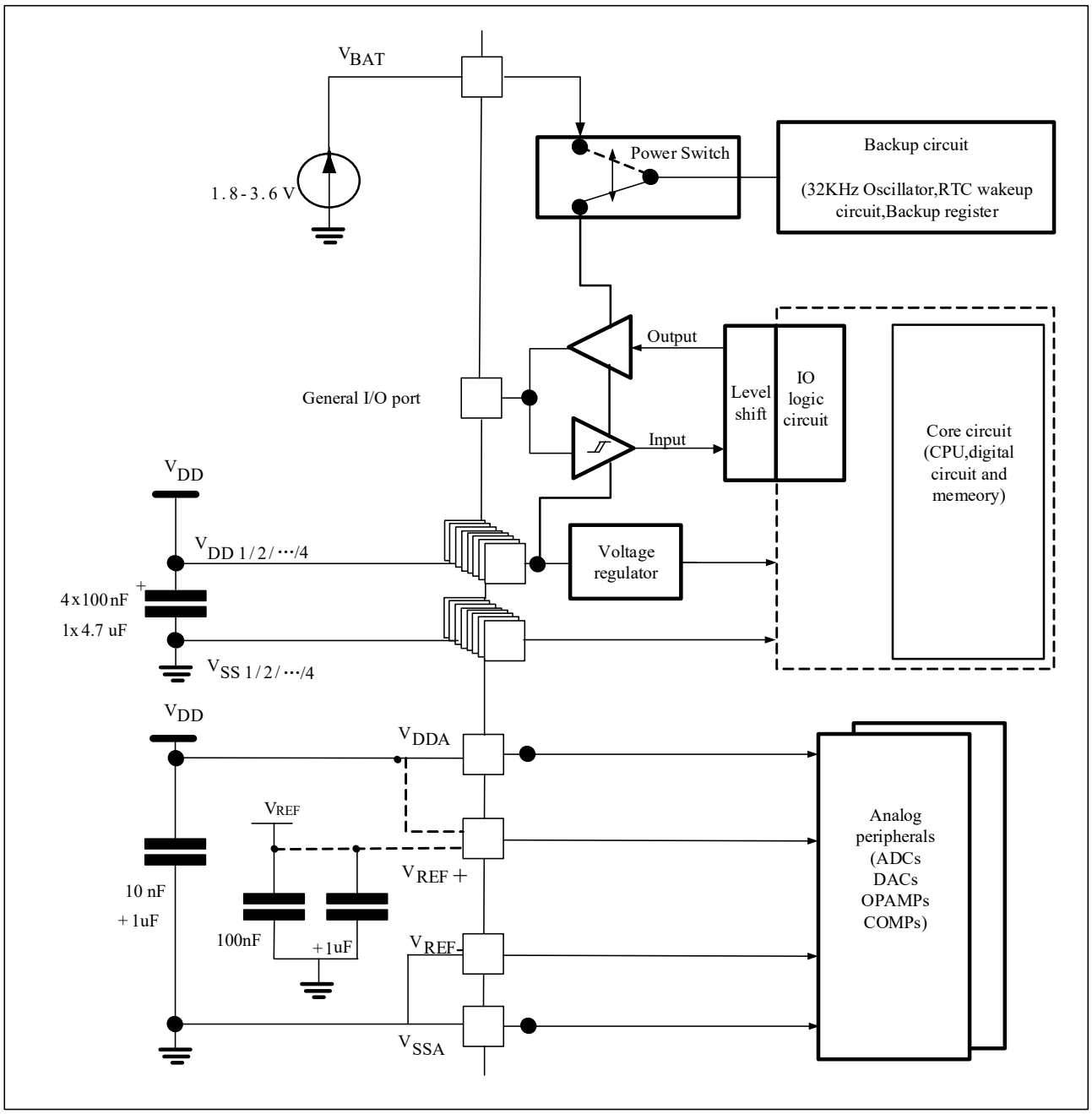
4.1.6 Power Supply Scheme

Figure 4-3 Power supply scheme



Note: The 4.7μF capacitor shown above must be connected to VDD3.

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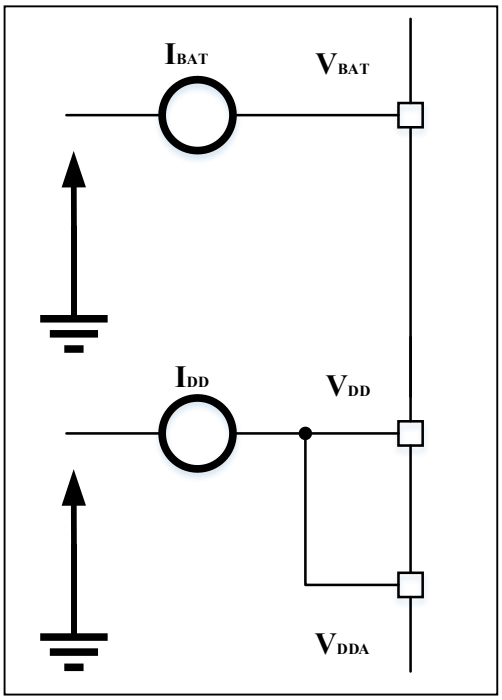
4.1.7 Current Consumption Measurement

Figure 4-4 Current consumption measurement scheme



4.2 Absolute Maximum Ratings

If the load applied to the device exceeds the values given in the "Absolute Maximum Ratings" list (Table 4-1, Table 4-2, Table 4-3), it may cause permanent damage to the device. These are stress ratings only and functional operation of the device under these conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Table 4-1 Voltage Characteristics

Symbol	Description	Minimum	Maximum	Unit
V_{DD}- V_{SS}	External main supply voltge (including V_{DDA} and V_{DD})(1)	-0.3	4.0	V
V_{IN}	Input voltage on 5V tolerant pins(3)	V_{SS}-0.3	5.5	
	Input voltage on other pins(2)	V_{SS}-0.3	V_{DD} + 0.3	
$\lvert \Delta V_{DDx} \rvert$	Voltage difference between different supply p ins	-	50	mV
$\lvert V_{SSx}$- $V_{SS}\rvert$	Voltage difference between different ground p ins	-	50	
$V_{ESD(HBM)}$	ESD voltage (Human Body Model)	See section 4.3.11		

Note:
(1) All power (VDD, VDDA) and ground (VSS, VSSA) pins must always be connected to an external power system within the allowable range.
(2) VIN should not exceed its maximum value, refer to Table 4 2 for current characteristics.
(3) When 5V tolerant pin input is 5.5V, VDD shall not be lower than 2.25V.

Table 4-2 Current Characteristcs

Sumbol	Decription	Maximum(1)	Unit
I_{VDD}	Total current through V_{DD}/V_{DDA} supply line(supply current)(1)(4)	100	mA
I_{VSS}	Total current through V_{SS} ground line (sink current) (1)(4)	100	
I_{IO}	Output sink current on any I/O and control pin	12	

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	Output source current on any I/O and control pin	-12
$I_{INJ(PIN)}$(2)(3)	Injected current on NRST	-5/0
	Injected current on other pins	+/-5

Note:
(1) All power (VDD, VDDA) and ground (VSS, VSSA) pins must always be connected to an external power system within the allowable range.
(2) When VIN>VDD, there is a forward injected current; when VIN<VSS, there is a reverse injected current. IINJ(PIN) should not exceed its maximum value, refer to Table 4 1 for voltage characteristics.
(3) Reverse injected current will interfere with the analog performance of the device. See Section 4.3.20.
(4) When the maximum current occurs, the maximum voltage drop of VDD allowed is 0.1VDD.

Table 4-3 Temperature Characteristics

Symbol	Description	Value	Unit
T_{STG}	Storage temperature	-40 ~ + 125	℃
T_J	Maximum junction temperature	125	℃

4.3 Operating Conditions

4.3.1 General operating conditions

Table 4-4 General operating conditions

Symbol	Parameter	Condition	Minimum	Miximum	Unit
f_{HCLK}	Internal AHB clock frequency	-	0	144	MHz
f_{PCLK1}	Internal APB1 clock frequency	-	0	36	
f_{PCLK2}	Internal APB2 clock frequency	-	0	72	
V_{DD}	Standard operating voltage	-	1.8	3.6	V
V_{DDA}	Analog part opeating voltage	Same as V_{DD}(1)	1.8	3.6	V
V_{BAT}	Backup domain operating voltage	-	1.8	3.6	V
T_A	Ambient temperature (temperature rade 7)	Suffix version 7	-40	105	℃
T_J	Junction temperature range	Suffix version 7	-40	125	℃

Note:(1) It is recommended to use the same power supply for VDD and VDDA, a maximum of 300mV difference between VDD and VDDA is allowed during power-up and normal operation.

4.3.2 Power-up and Power-down Operating Conditions

The parameters given in the table below are tested under the ambient temperature conditions listed in Table 4-4.

Table 4-5 Power-up and power-down operating conditions

Symbol	Parameter	Condition	Minimum	Maximum	Unit
t_{VDD}	V_{DD} Rising Rate	Voltage rises from 0 to V_{DD}	20	∞	μs/V
	V_{DD} Falling Rate	Voltage falls from V_{DD} to 0	80	∞	

4.3.3 Embedded Reset and Power Control Module Characteristics

The parameters given in the following table are based on the environmental temperature and VDD supply voltage conditions listed in Table 4-4.

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Table 4-6 Embedded Reset and Power Control Module Characteristics

Symbol	Parameter	Condition	Min	Type	Max	Unit
V_{PVD}	Programmable Voltage Detector Level Selection (PWR_CTRL MSB = 0)	PRS[2:0]=000 (Rising Edge)	2.09	2.18	2.27	V
		PRS[2:0]=000 (Falling Edge)	2	2.08	2.16	V
		PRS[2:0]=001 (Rising Edge)	2.19	2.28	2.37	V
		PRS[2:0]=001 (Falling Edge)	2.09	2.18	2.27	V
		PRS[2:0]=010 (Rising Edge)	2.28	2.38	2.48	V
		PRS[2:0]=010 (Falling Edge)	2.19	2.28	2.37	V
		PRS[2:0]=011 (Rising Edge)	2.38	2.48	2.58	V
		PRS[2:0]=011 (Falling Edge)	2.28	2.38	2.48	V
		PRS[2:0]=100 (Rising Edge)	2.47	2.58	2.69	V
		PRS[2:0]=100 (Falling Edge)	2.37	2.48	2.59	V
		PRS[2:0]=101 (Rising Edge)	2.57	2.68	2.79	V
		PRS[2:0]=101 (Falling Edge)	2.47	2.58	2.69	V
		PRS[2:0]=110 (Rising Edge)	2.66	2.78	2.9	V
		PRS[2:0]=110 (Falling Edge)	2.56	2.68	2.8	V
		PRS[2:0]=111 (Rising Edge)	2.76	2.88	3	V
		PRS[2:0]=111 (Falling Edge)	2.66	2.78	2.9	V
	Programmable Voltage Detector Level Selection (PWR_CTRL MSB = 1)	PRS[2:0]=000 (Rising Edge)	1.7	1.78	1.85	V
		PRS[2:0]=000 (Falling Edge)	1.61	1.68	1.75	V
		PRS[2:0]=001 (Rising Edge)	1.8	1.88	1.96	V
		PRS[2:0]=001 (Falling Edge)	1.7	1.78	1.85	V
		PRS[2:0]=010 (Rising Edge)	1.9	1.98	2.06	V
		PRS[2:0]=010 (Falling Edge)	1.8	1.88	1.96	V
		PRS[2:0]=011 (Rising Edge)	2	2.08	2.16	V
		PRS[2:0]=011 (Falling Edge)	1.9	1.98	2.06	V
		PRS[2:0]=100 (Rising Edge)	3.15	3.28	3.41	V
		PRS[2:0]=100 (Falling Edge)	3.05	3.18	3.31	V
		PRS[2:0]=101 (Rising Edge)	3.24	3.38	3.52	V
		PRS[2:0]=101 (Falling Edge)	3.15	3.28	3.41	V
		PRS[2:0]=110 (Rising Edge)	3.34	3.48	3.62	V
		PRS[2:0]=110 (Falling Edge)	3.24	3.38	3.52	V
		PRS[2:0]=111 (Rising Edge)	3.44	3.58	3.72	V
		PRS[2:0]=111 (Falling Edge)	3.34	3.48	3.62	V
$V_{PVDhyst}$(1)	PVD Hysteresis	-	-	100	-	mV
V_{POR}	VDD Power-Up/DownReset Threshold	-	-	1.64/1.62	-	V
$T_{RSTTEMPO}$(1)	Reset Duration	-	-	0.8	4	ms

Note:(1) Ensured by design, not tested in production

4.3.4 Built-in Reference Voltage

The parameters given in the table below are tested based on the environmental temperature and VDD supply voltage listed in Table 4.4.

Table 4.7 Built-in Reference Voltage

Symbol	Parameter	Condition	Min	Type	Max	Unit
V_{REFINT}	Internal Reference Voltage	-40℃< T_A< +105℃	1.164	1.20	1.236	V
$T_{S\_vrefint}$(1)	Sampling Time of ADC when reading Intrnal Reference Voltage	-	-	5.1	10(2)	μs

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Note:
(1). *The shortest sampling time is obtained through multiple loops in the application.*
(2). *Ensured by design, not tested in production.*

4.3.5 Power Supply Current Characteristics

Current consumption is a comprehensive indicator influenced by various parameters and factors, including operating voltage, environmental temperature, load on I/O pins, software configuration of the product, operating frequency, flip rate of I/O pins, program location in memory, and executed code, among others.
For details on the measurement method of current consumption, refer to Figure 4.4.
All current consumption measurement values provided in this section for various operating modes are obtained while executing a simplified set of code.

4.3.5.1 Maximum Current Consumption

The microcontroller is under the following conditions:

- All I/O pins are in input mode and connected to a static level - VDD or VSS (no load).
- All peripherals are in the off state unless specifically stated.
- Access time for flash memory is adjusted to the fastest possible frequency it can run (0~32MHz requires 0 wait cycles, 32~64MHz requires 1 wait cycle, 64~96MHz requires 2 wait cycles, 96~128MHz requires 3 wait cycles, 128~144MHz requires 4 wait cycles).
- Instruction prefetch is enabled (Note: This parameter must be set before setting the clock and bus divisio n).
- When peripherals are enabled: fPCLK1 = fHCLK/4, fPCLK2 = fHCLK/2.
- VDD=3.63V, environmental temperature equals 105℃.

The parameters given in Tables 4.8 and 4.9 are tested based on the environmental temperature and VDD supply voltage listed in Table 4.4.

Table 4-7 Maximum current consumption in operating modes, data processing code running from internal flash memory.

Symbol	Paramenter	Condition	f_{HCLK}	Typ(1) T_A = 105℃	Unit
I_{DD}	Supply Current in Operating Mode	External Clock(2), Eansble all Peripherals	144MHz	32	mA
			72MHz	18	
			36MHz	11	
		External Clock(2), Disable all Peripherals	144MHz	15.8	
			72MHz	9.7	
			36MHz	6.7	

1. Based on comprehensive evaluation and not tested in production.
2. Eable PLL when f_{HCLK}>8MHz

Table 4-8 Maximum Current Consumption in Sleep Mode

Symbol	Parameter	Condition	f_{HCLK}	Typ(1) T_A = 105℃	Unit
I_{DD}	Supply current in ssleep mode	External clock(2), Enable all peripherals	144MHz	27	mA
			72MHz	15.5	
			36MHz	10	
		External clock(2), Disable all peripherals	144MHz	9.2	
			72MHz	6.6	
			36MHz	5.1	

Notes:

(1) *Based on comprehensive evaluation and not tested in production..*

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(2) Enable PLL when fHCLK > 8MHz.

4.3.5.2 Typical Curent Cosumption

The MCU is under the following conditions:

- All I/O pins are in input mode and connected to a static level (VDD or VSS) with no load.
- All peripherals are in the disabled state unless specifically stated.
- Flash memory access time is adjusted to the fastest possible frequency (0 wait cycles for 0-32MHz, 1 wait cycle for 32-64MHz, 2 wait cycles for 64-96MHz, 3 wait cycles for 96-128MHz, and 4 wait cycles for 128-144MHz).
- Ambient temperature and VDD supply voltage conditions are listed in Table 4.4.
- Instruction prefetch is enabled (Note: This parameter must be set before configuring clock and bus frequencies). When peripherals are enabled: fPCLK1 = fHCLK/4, fPCLK2 = fHCLK/2, fADCCLK = fPCLK2/4.

Table 4-9 Typical Current Consumption in Run Mode, Data Processing Code Running from Internal Flash

Symbol	Parameter	Cpnditions	f_{HCLK}	Typ(1)		Unit
				Enable all peripherals(2)	Disable all peripherals	
I_{DD}	Running mode supply current	External clock(3)	144MHz	30.3	14.2	mA
			72MHz	17	8.1	
			36MHz	9.3	5.3	
		High-Speed Internal RC Oscillator (HSI) with AHB Prescaler to Reduce Frequency	128MHz	30	12.7	mA
			72MHz	22.5	7.2	
			36MHz	8.8	3.9	

- Typical values are tested at TA=25°C, VDD=3.3V.
- Each analog section of the ADC adds an additional 0.8mA current consumption. In the application environment, this current is only increased when the ADC is enabled (setting the ON bit of the ADC_CTRL2 register).
- External clock is 8MHz, and PLL is enabled when fHCLK > 8MHz.

Table 4-10 Sleep mode typical current consumption

Symbol	Parameter	Condition	f_{HCLK}	Typ(1)		Unit
				Enable all peripherals(2)	Disable all peripherals	
I_{DD}	Sleep mode supply current	External clock(3)	144MHz	25.3	8	mA
			72MHz	13.9	5.3	
			36MHz	8	3.6	
		High-Speed Internal RC Oscillator (HSI) with AHB Prescaler to Reduce Frequency	128MHz	24.2	6.1	mA
			72MHz	13.9	3.5	
			36MHz	7.2	2.2	

- The typical values are obtained at a temperature (TA) of 25°C and a supply voltage (VDD) of 3.3V.
- Each analog part of the ADC (Analog-to-Digital Converter) increases additional current consumption by 0.8mA. This additional current is applicable only when the ADC is enabled (setting the ON bit in the ADC_CTRL2 register).
- External clock is 8MHz, and PLL is enabled when fHCLK > 8MHz.

4.3.5.3 Low-Power Mode Current Consumption

The MCU is under the following conditions：

- All I/O pins are in input mode and connected to a static voltage level (VDD or VSS) with no external load.

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- All peripherals are in a disabled state unless otherwise specified.

Table 4-11 Typical and Maximum Current Consumption in STOP and STANDBY Modes

Symbol	Parameter	Condition	Typ(1)		Unit
			T_A =25℃	T_A =105℃	
I_{DD}	Supply current in STOP0 mode	Regulator in run mode, low-speed and high-speed internal RC oscillators, and high-speed oscillator off (no independent watchdog)	300	1200	μA
		Regulator in low-power mode, low-speed and high-speed internal RC oscillators, and high-speed oscillator off (no independent watchdog)	150	800	
	Supply current in STOP2 mode	External low-speed clock enabled, RTC running, R-SRAM retained, all I/O states retained, independent watchdog off	10	100	
	Supply current in STANDBY mode	Low-speed internal RC oscillator and independent watchdog enabled	3	40	
		Low-speed internal RC oscillator enabled, independent watchdog disabled	2.9	40	
		Low-speed internal RC oscillator and independent watchdog disabled, low-speed oscillator and RTC off	2.7	35	
I_{DD_VBAT}	Supply current in VBAT domain (backup area)	Low-speed oscillator and RTC enabled	2	15	

Based on comprehensive evaluation and not tested in production.

4.3.6 External clock source charateristics

4.3.6.1 External high-speed cource (HSE)

The characteristic parameters given in the following table are measured using a high-speed external clock source, and the ambient temperature and supply voltage comply with the conditions in Table 4 4.

Table 4-12 High-speed external user clock characteristics (Bypass mode)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
fHSE_ext	External user clock frequency(1)	-	4	8	32	MHz
VHSEH	High-level voltge on OSC_IN		0.8V_{DD}	-	V_{DD}	V
VHSEL	Low-level voltage on OSC_IN		V_{SS}	-	0.3V_{DD}	
tw(HSE)	Time of OSC_IN high or low(1)		16	-	-	ns
tr(HSE) tf(HSE)	Rising or fall time of OSC_IN(1)		-	-	20	
Cin(HSE)	Input capacitance of OSC_IN(1)	-	-	5	-	pF
DuCy(HSE)	Duty cycle	-	45	-	55	%
I_L	Input leakage current on OSC_IN	$V_{SS}\leq V_{IN}\leq V_{DD}$	-	-	±1	μA

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Note:(1) Ensured by design, not tested in production.

4.3.6.2 External Low-Speed Clock Source (LSE)

The characteristic parameters in the following table are measured using a low-speed external clock source, with the environmental temperature and supply voltage meeting the conditions specified in Table 4.4.

Table 4-13 Low-speed External User Clock Characteristics (Bypass Mode)

Symbol	Para meter	Condition	Min	Typ	Max	Uint
f_{LSE_ext}	External user clock frequency(1)	-	0	32.768	1000	KHz
V_{LSEH}	High-level voltage on OSC32_IN		$0.7V_{DD}$	-	V_{DD}	V
V_{LSEL}	Low-level voltage on OSC32_IN		V_{SS}	-	200	mV
$t_{w(LSE)}$	Time of OSC32_IN high or low(1)		450	-	-	ns
$t_{r(LSE)}t_{f(LSE)}$	Rise or fall time of OSC32_IN(1)		-	-	50	
$DuCy_{(LSE)}$	Duty cycle	-	30	-	70	%
I_L	Input leakage current on OSC32_IN	$V_{SS}\leq V_{IN}\leq V_{DD}$	-	-	±1	μA

Note:(1) Ensured by design, not tested in production.

Figure 4-5 AC timing diagram of external high-speed clock source

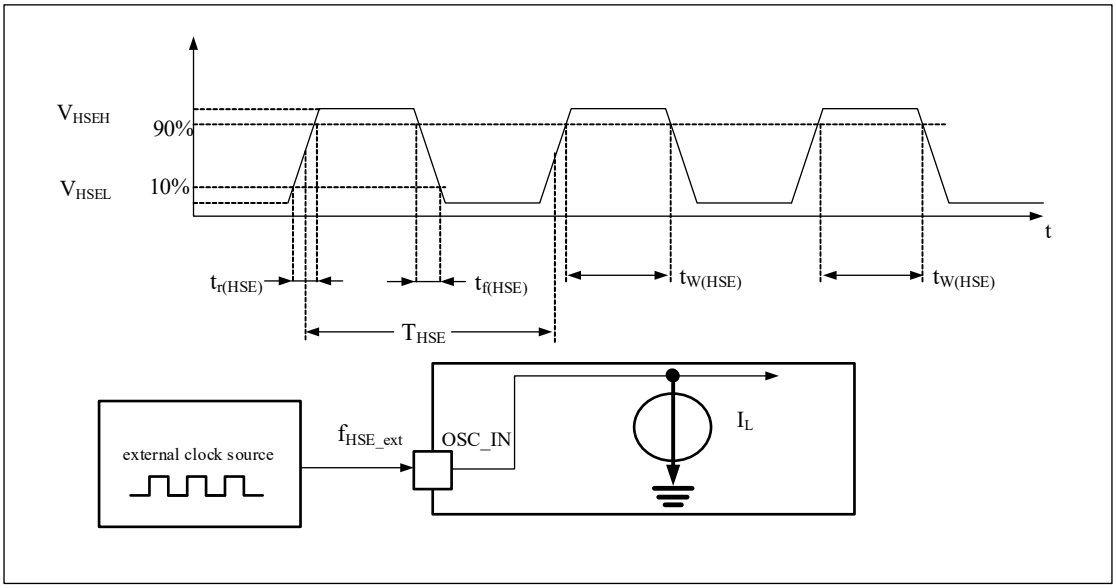

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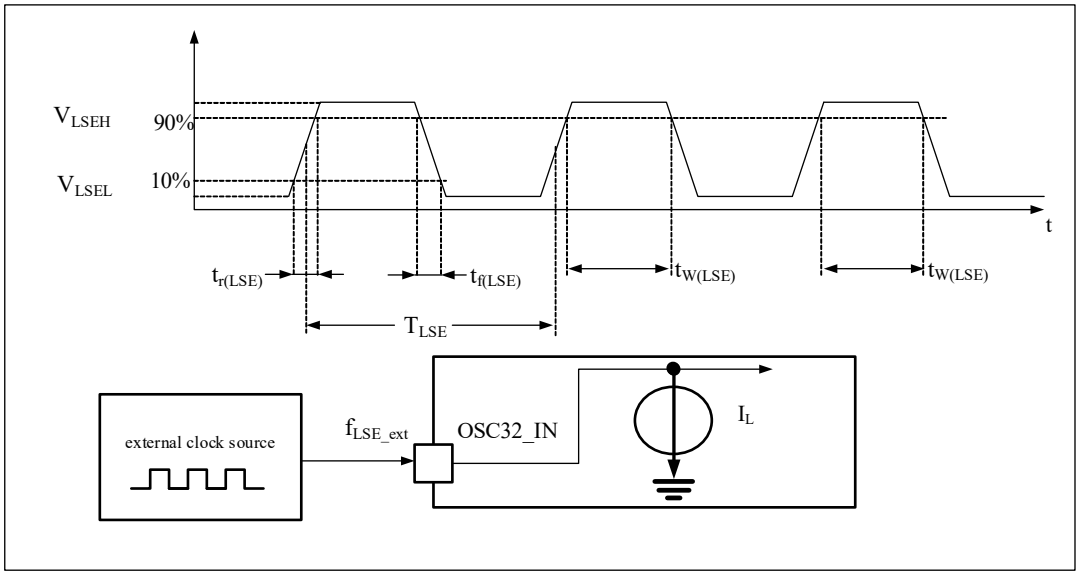
Figure 4-6 AC timing diagram for external low-speed clock source



Using a crystal/ceramic resonator to generate the high-speed external clock

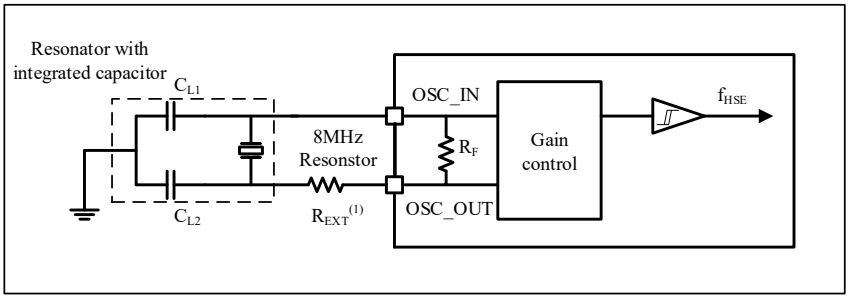
The high-speed external clock (HSE) involves creating an oscillator with a frequency range of 4~32MHz. The information provided in this section is based on the use of typical external components listed in the table, and the results are obtained through comprehensive performance evaluations. In practical applications, it's crucial to place the resonator and the load capacitors as close as possible to the oscillator pins to minimize output distortion and stabilize the startup time. For detailed parameters of the crystal resonator (frequency, packaging, precision, etc.), please consult the respective manufacturer. (The crystal resonator mentioned here is commonly referred to as a passive crystal oscillator or crystal resonator.)

Table 4-14 HSE 4~32MHz Oscillator Characteristics (1)(2)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{OSC_IN}	Oscillator frequency	-	4	8	32	MHz
R_F	Feedback resister	-	-	160	-	kΩ
i_2	HSE drive current	V_{DD}=3.3V，V_{IN}=V_{SS} 30pF load	-	1.3	-	mA
g_m	Oscillator transconductance	Startup	-	10	-	mA/V
$t_{SU(HSE)}$(3)	Startup time (8M cryctal)	V_{DD} is stable	-	3	-	ms

1. The characteristics of the resonator are provided by the crystal/ceramic resonator manufacturer.
2. Guaranteed by design, not tested during production.
3. tSU(HSE) is the startup time, measured from the software enabling HSE to the time of stable 8MHz oscil lation. This value is measured on a standard crystal resonator and may vary significantly depending on the crystal manufacturer.

Figure 4-7 Typical applications using 8MHz crystals



Note:(1) $R_{EXT\ value}$ is determined by the characteristics of the crystal.

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Using a Crystal/Ceramic Resonator to Generate a Low-Speed External Clock

The low-speed external clock (LSE) can be generated using a 32.768 kHz crystal/ceramic resonator oscillator. The information provided in this section is based on the results obtained through a comprehensive characteristic evaluation using the typical external components listed in the table below. In applications, the resonator and load capacitors must be placed as close as possible to the oscillator pins to minimize output distortion and stabilization time at startup. For detailed parameters of the crystal resonator (frequency, package, accuracy, etc.), please consult the corresponding manufacturer. (The crystal resonator mentioned here is what we commonly refer to as a passive crystal)

Note: For CL1 and CL2, it is recommended to use high-quality ceramic capacitors and select crystals or resonators that meet the requirements. CL1 and CL2 usually have the same parameters. Crystal manufacturers typically provide load capacitance parameters as a series combination of CL1 and CL2.

The load capacitance CL is calculated using the following formula: CL = CL1 × CL2 / (CL1 + CL2) + Cstray, where Cstray is the capacitance of the pins and the PCB or PCB-related capacitance.

For example: If a resonator with a load capacitance of CL=6pF is selected and Cstray=2pF, then CL1=CL2=8pF.

Table 4-15 LSE Oscillator Characteristics (fLSE=32.768kHz)(1)

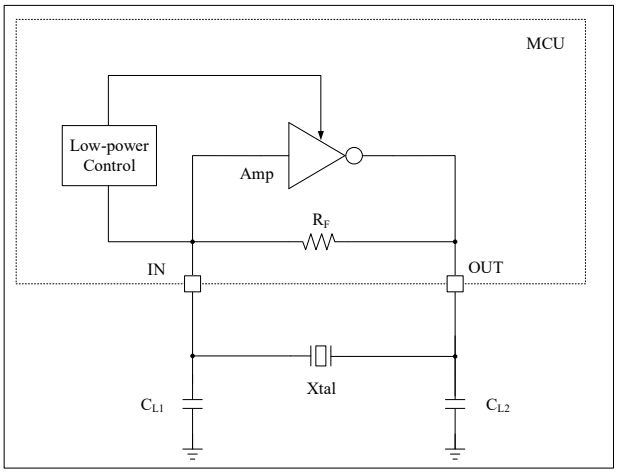
Symbol	Parameter	Condition	Min	Typ	Max	Unit
R_F	Feedback resistance	-	-	5	-	MΩ
g_m	Transconductance of the oscillator	-	5	-	-	μA/V
$t_{SU(LSE)}$(2)	Startup	V_{DD} is stable	-	2	-	s

Notes:

(1) Guaranteed by design, not tested in production.

(2) tSU(LSE) is the startup time, measured from the moment the LSE is enabled by software until a stable 3 2.768 kHz oscillation is obtained. This value is measured on a standard crystal resonator and may vary g reatly depending on the crystal manufacturer.

Figure 4-8 Typical Application Using a 32.768 kHz Crystal (1)(2)



1. Please refer to the LSE Crystal Selection Guide.
2. To ensure crystal stability, adjacent pins should not be toggled while the crystal is operating.

4.3.7 Internal clock source characteristics

The characteristic parameters in the table below are measured under conditions where the ambient temperature and supply voltage comply with the specifications in Table 4.4.

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4.3.7.1 High-speed internal (HSI) RC Oscillator

Table 4-16 HIS Oscillator characteristcs(1)(2)

Symbol	Parameter	Condition	Min	Typ	MAX	Unit
f_{HSI}	Frequency	VDD=3.3V，T_A = 25℃, After calibrartion	7.92(3)	8	8.08(3)	MHz
$DuCy_{(HSI)}$	Duty cycle	-	45	-	55	%
ACC_{HSI}	HIS oscillator temperature drift(4)	VDD=3.3V，T_A = -40~105℃	-2.5	-	2.5	%
$t_{SU(HSI)}$	HIS oscillator start-up tim e	-	-	-	5	μs
$I_{DD(HSI)}$	HIS oscillator power consumption	-	-	40	-	μA

- VDD = 3.3V，TA = -40~105℃, uless otherwise specified.
- Guaranteed by design, not tested during production.
- Production calibration accuracy, excluding soldering effects. Soldering may introduce a frequency deviation of approximately +1.5%.
- Frequency deviation includes the impact of soldering. Data is based on sample testing and not tested during production.

4.3.7.2 Low-Speed Internal (LSI) RC Oscillator

Table 4-17 LSI oscillator charateristcs(1)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
fLSI(2)	Ouput frequency	25℃ Calibration, VDD =3.3V	38	40	42	KHz
		VDD =1.8V ~3.6V, T_A = -40~105℃	30	40	60	KHz
$t_{SU(LSI)}$ (2)	LSI oscillator startup time	-	-	40	80	μs
$I_{DD(LSI)}$ (2)	LSI oscillator power consumption	-	-	0.1	-	μA

Notes:

(1) V_{DD} = 3.3V，T_A = -40~105℃，unless otherwise specified.

(2) *Guaranteed by design, not tested in production.*

4.3.8 Wake-Up Time from Low Power Modes

The wake-up times listed in Table 4.19 are measured during the wake-up phase of an 8MHz HSI RC oscillator. The clock source used for wake-up depends on the current operating mode:

- STOP0, STOP2, or STANDBY modes: The clock source is the RC oscillator.
- SLEEP mode: The clock source is the one used when entering SLEEP mode.

All times are measured under conditions where the environmental temperature and supply voltage comply with the specifications in Table 4.4.

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Table 4-18 Wake-up time from low power modes

Symbol	Parameter	Typ	Unit
$t_{WUSLEEP}$(1)	Wake-up from SLEEP	480	ns
$t_{WUSTOP0}$(1)	Wake-up from STOP0 (regulator in run mode)	20	µs
	Wake-up from STOP0 (regulator in low power mode)	22	
$t_{WUSTOP2}$(1)	Wake-up from STOP2	40	
$t_{WUSTDBY}$(1)	Wake-up from STANDBY	100	

Note:(1) Wake-up time measurement is from the wake-up event to the execution of the first instruction by the us er program.

4.3.9 PLL Characteristics

Table 4-19

Table 4-19 PLL characteristics

Symbol	Parameter	Value			Unit
		Min	Typ	Max(1)	
f_{PLL_IN}	PLL input clock(2)	4	8.0	32	MHz
	PLL input clock duty cycle	40	-	60	%
f_{PLL_OUT}	PLL multiplied output clock	32	-	144	MHz
t_{LOCK}	PLL Ready indication signal output time	-	-	150	µs
Jitter	Rms cycle-to-cycle jitter @144MHz	-	5	-	ps
Ipll	Operating Current of PLL @144MHz VCO frequen cy.	-	700	-	µA

Notes:

(1) Evaluated synthetically, not tested in production.

(2) Ensure the correct multiplication factor to keep fPLL_OUT within the allowed range based on the PLL i nput clock frequency.

4.3.10 FLASH Memory Characteristics

Unless specified otherwise, all characteristic parameters are obtained at TA = -40~105℃.

Tabl 4-20 Flash Memory Characteristics

Symbol	Parameter	Condition	Min(1)	Typ(1)	Max(1)	Unit
tprog	32-bit Programming time	T_A = -40~105℃	-	112	225	µs
t_{ERASE}	Page(2KB) Erase ti me	T_A = -40~105℃	-	2	20(2)	ms
					100(3)	
t_{ME}	Full chip erase time	T_A = -40~105℃;	-	-	100	ms
I_{DD}	Supply current	Read mode, f_{HCLK}=144MHz，3 wait cycles, V_{DD}=3.3V	-	-	3.62	mA
		Write mode, f_{HCLK}=144MHz，V_{DD}=3.3V	-	-	6.5	mA
		Erase mode, f_{HCLK}=144MHz，V_{DD}=3.3V	-	-	4.5	mA
		Power down/standby, V_{DD}=3.3~3. 6V	-	-	0.035	µA
Vprog	Programming voltag e	-	1.8	3.0	3.6	V

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Notes:
(1) Guaranteed by design, not tested in production.
(2) Erase/write cycles for 10k storage space.
(3) Erase/write cycles for 100k storage space.

Table 4-21 Flash Memory Endurance and Data Retention

Symbol	Parameter	Condition	Min(1)	Unit
N_{END}	Endurance (Note: Erase/Write cycles)	T_A = -40~105°C(suffix 7); Flash capacity of 256KB	10	Thousand cycles
		T_A = -40~105°C(suffix 7); Flash capacityof 512KB，with the first 256KB storage space	10	
		T_A = -40~105°C(suffix 7); Flash capacity of 512KB，with the latter 256KB storage space	100	
t_{RET}	Data retenton time	T_A = 85°C	20	years

Note:(1) Evaluated synthetically, not tested in production.

4.3.11 Absolute Maximum Ratings (Electrical Sensitivity)

Performance regarding electrical sensitivity is determined through three different tests (ESD, LU) using specific measurement methods to assess the chip's behavior.

Electrostatic Discharge (ESD)

Electrostatic discharge (ESD) testing involves applying a positive pulse followed by a negative pulse, with a one-second interval, to all pins of all samples.

Table 4-22 ESD Absolute Maximum Ratings

Symbol	Parameter	Condition	Typ	Max(1)	Unit
$V_{ESD(HBM)}$	Electrostatic Discharge Voltage (HBM)	T_A = +25 °C, Compiles with MIL-STD-883K Method 3015.9	3A	4000	V
$V_{ESD(CDM)}$	Electrostatic Discharge Voltage (CDM)	T_A = +25 °C, Compiles with ESDA/JEDEC JS-002-2018	C3	1000	

Note:(1) Evaluated synthetically, not tested in production.

Static Latch-up

To assess latch-up performance, two complementary static latch-up tests are conducted on six samples:

- Provide voltages exceeding the limits to each power pin.
- Inject current into each input, output, and configurable I/O pin.

This testing complies with the JEDEC78E Integrated Circuit Latch-Up standard.

Table 4-23 Electrical sensitivity

Symbol	Parameter	Condition	Type	Min(1)
LU	Static latch-up	T_A = +25 °C, complies with JEDEC78E	II class A	±100mA, 1.5*VDDMAX

Note:(1) Tested under normal temperature conditions.

4.3.12 I/O Port Characteistics

General Input/Output Characteristcs

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Unless otherwise specified, the parameters listed in the following table are measured under the conditions in Ta ble 4-4. All I/O ports are CMOS and TTL compatible.

Table 4-24 I/O Static Characteristics

Symbol	Parameter	Condition	Min	Type	Max	Unit
V_{IL}	Input low-level voltage	TTL port	Vss	-	0.8	V
V_{IH}	Input high-level voltage		2	-	V_{DD}	
V_{IL}	Input low-level voltage	CMOS port	Vss	-	0.35 V_{DD}	
V_{IH}	Input high-level voltage		0.65 V_{DD}	-	V_{DD}	
Vhys	Schmitt trigger voltage hysteresis (1)	V_{DD}=3.3V	200	-	-	mV
		V_{DD}=2.5V	200	-	-	
		V_{DD}=1.8V	0.1*V_{DD} (2)	-	-	
I_{lkg}	Input leakage current (3)	V_{DD}=Maximum V_{PAD}=0 或 V_{PAD}=V_{DD}(5)	-1	-	1	μA
R_{PU}	Weak pull-up equivalent resistance (4)	V_{DD}=3.3V,V_{IN}= V_{SS}	75	-	220	kΩ
		V_{DD} =2.5V, V_{IN} = V_{SS}	95	-	310	
		V_{DD} = 1.8V, V_{IN} = V_{SS}	135	-	500	
R_{PD}	Weak pull-down equivalent resistance (4)	V_{DD}=3.3V,V_{IN}= V_{DD}	75	-	235	kΩ
		V_{DD} = 2.5V, V_{IN} = V_{DD}	85	-	315	
		V_{DD} = 1.8V, V_{IN} = V_{DD}	120	-	495	
C_{IO}	I/O pin capacitance	-	-	5	-	pF

Notes:

(1) *The Hysteresis voltage of Schmitt triggers switching level. Derived from comprehensive evaluation, not tested in production.*

(2) *At least 100mV.*

(3) *Leakage current may exceed the maximum value if there is reverse current injection on adjacent pins.*

(4) *Pull-up and pull-down resistances are designed as switchable PMOS/NMOS implementation.*

(5) *VPAD refers to the input voltage of the I/O pin.*

All I/O ports are CMOS and TTL compatible (no software configuration required), and their characteristics consider the most stringent CMOS process or TTL parameters:

- For VIH:
  - If VDD is between [1.8V~3.08V]; use CMOS characteristics but include TTL.
  - If VDD is between [3.08V~3.60V]; use TTL characteristics but include CMOS.
- For VIL:
  - If VDD is between [1.8V~2.28V]; use TTL characteristics but include CMOS.
  - If VDD is between [2.28V~3.60V]; use CMOS characteristics but include TTL.

Output Drive Current

GPIOs can sink or source up to +/-12mA of current. In user applications, the number of I/O pins must ensure that the drive current does not exceed the absolute maximum ratings given in section 4.2:

The total current drawn by all I/O ports from VDD, plus the maximum operating current drawn by the MCU on VDD, must not exceed the absolute maximum rating IVDD (Table 4-2).
The total current sunk by all I/O ports and flowing out from VSS, plus the maximum operating current flowing out of the MCU on VSS, must not exceed the absolute maximum rating IVSS (Table 4-2).

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Ouput Voltage

Unless otherwise specified, the parameters listed in Table 4-27 are measured under the ambient temperature and V_{DD} supply voltage conditions per Table 4-4. All I/O ports are CMOS and TTL compatible.

Table 4-25 II/O Drive Capability Table

Drive Level	I_{OH}(1), VDD =3.3V	I_{OL}(1), VDD =3.3V	I_{OH}(1), VDD =2.5V	I_{OL}(1), VDD =2.5V	I_{OH}(1), VDD =1.8V	I_{OL}(1), VD D=1.8V	Unit
2	-2	2	-1.5	1.5	-1.2	1.2	mA
4	-4	4	-3	3	-2.5	2.5	mA
8	-8	8	-7	7	-5	5	mA
12	-12	12	-11	11	-7.5	7.5	mA

Note:(1) Guaranteed by design, not tested in production.

Tble 4-26 Output Voltage Characteristics

Symbol	Parameter	Condition	Min	Max	Unit
V_{OL}(1)	Output low-level voltage	V_{DD} = 3.3 V, I_{OL}= 2mA, 4mA, 8mA, and 12mA	V_{SS}	0.4	V
		V_{DD} = 2.5 V, I_{OL}= 1.5mA,3mA, 7mA, and 11mA	V_{SS}	0.4	
		V_{DD} = 1.8 V, I_{OL}=1.2mA, 2.5mA, 5mA, and 7.5m A	V_{SS}	0.2*V_{DD}	
V_{OH}(2)	Output high-leve l voltage	V_{DD} = 3.3 V, I_{OH}= -2mA, -4mA, -8mA, and -12m A	2.4(3)	V_{DD}	
		V_{DD} = 2.5 V, I_{OH}= -1.5mA, -3mA, -7mA, and -11 mA	1.8(3)	V_{DD}	
		V_{DD} = 1.8 V, I_{OH}= -1.2mA, -2.5mA, -5mA, and -7 .5mA	0.8*V_{DD}	V_{DD}	

Notes:

(1) *The current I_{IO} absorbed by the chip must always follow the absolute maximum ratings given in Table 4-2, and the sum of I_{IO} (all I/O pins and control pins) must not exceed I_{VSS}。*

(2) *The current I_{IO} output by the chip must always follow the absolute maximum ratings given in Table 4-2, and the sum of I_{IO} (all I/O pins and control pins) must not exceed I_{VDD}。*

(3) *PC13, PC14, PC15 are not included in this range.*

Input/Output AC Characteristics

The definitions and values for the input/output AC characteristics are given in Figure 4-9 and Table 4-28, respectively. Unless otherwise specified, the parameters listed in Table 4-28 are measured under the ambient temperature and supply voltage conditions per Table 4-4.

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Table 4-27 Input/Output AC Characteristics(1)

DS_CFGy Config	PMODEy[1:0] Config	Symbol	Parameter	Condition	Min	Max	Unit
0	xx (2mA)	$f_{max(IO)out}$	Max Frequency (2)	C_L=5pF,V_{DD}=3.3V	-	75	MHz
				C_L=5pF,V_{DD}=2.5V	-	50	
				C_L=5pF,V_{DD}=1.8V	-	30	
		$t_{(IO)out}$	Output Delay	C_L=5pF,V_{DD}=3.3V	-	3.66	ns
				C_L=5pF,V_{DD}=2.5V	-	4.72	
				C_L=5pF,V_{DD}=1.8V	-	7.12	
		$t_{(IO)in}$	Input Delay	C_L=50fF,V_{DD}=2.97V,V_{DDD}=0.81V input characteristics at 1.8V and 2.5V are derated	-	2	ns
1	00/01 (4mA)	$f_{max(IO)out}$	Max Frequency (2)	C_L=10pF,V_{DD}=3.3V	-	90	MHz
				C_L=10pF,V_{DD}=2.5V	-	60	
				C_L=10pF,V_{DD}=1.8V	-	40	
		$t_{(IO)out}$	Output Delay	C_L=10pF,V_{DD}=3.3V	-	3.5	ns
				C_L=10pF,V_{DD}=2.5V	-	4.5	
				C_L=10pF,V_{DD}=1.8V	-	6.74	
		$t_{(IO)in}$	Input Delay	C_L=50fF,V_{DD}=2.97V,V_{DDD}=0.81V input characteristics at 1.8V and 2.5V are derated	-	2	
1	10 (8mA)	$f_{max(IO)out}$	Max Frequency (2)	C_L=20pF,V_{DD}=3.3V	-	100	MHz
				C_L=20pF,V_{DD}=2.5V	-	75	
				C_L=20pF,V_{DD}=1.8V	-	50	
		$t_{(IO)out}$	Output Delay	C_L=20pF,V_{DD}=3.3V	-	3.42	ns
				C_L=20pF,V_{DD}=2.5V	-	4.73	
				C_L=20pF,V_{DD}=1.8V	-	6.53	
		$t_{(IO)in}$	Input Delay	C_L=50fF,V_{DD}=2.97V,V_{DDD}=0.81V input characteristics at 1.8V and 2.5V are derated	-	2	
1	11 (12mA)	$f_{max(IO)out}$	Max Frequency (2)	C_L=30pF,V_{DD}=3.3V	-	120	MHz
				C_L=30pF,V_{DD}=2.5V	-	90	
				C_L=30pF,V_{DD}=1.8V	-	60	
		$t_{(IO)out}$	Output Delay	C_L=30pF,V_{DD}=3.3V	-	3.34	ns
				C_L=3pF,V_{DD}=2.5V	-	4.26	
				C_L=3pF,V_{DD}=1.8V	-	6.34	
		$t_{(IO)in}$	Input Delay	C_L=50fF,V_{DD}=2.97V,V_{DDD}=0.81V input characteristics at 1.8V and 2.5V are derated	-	2	

Notes:

(1) The drive capability of I/O ports can be configured via DS_CFGy and PMODEy[1:0]. Refer to the description of GPIO port configuration registers in the N32G45x Series User Manual.

(2) Maximum frequency is defined in Figure 4-9.

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Figure 4-9 Input/Output AC Characteristics Definition

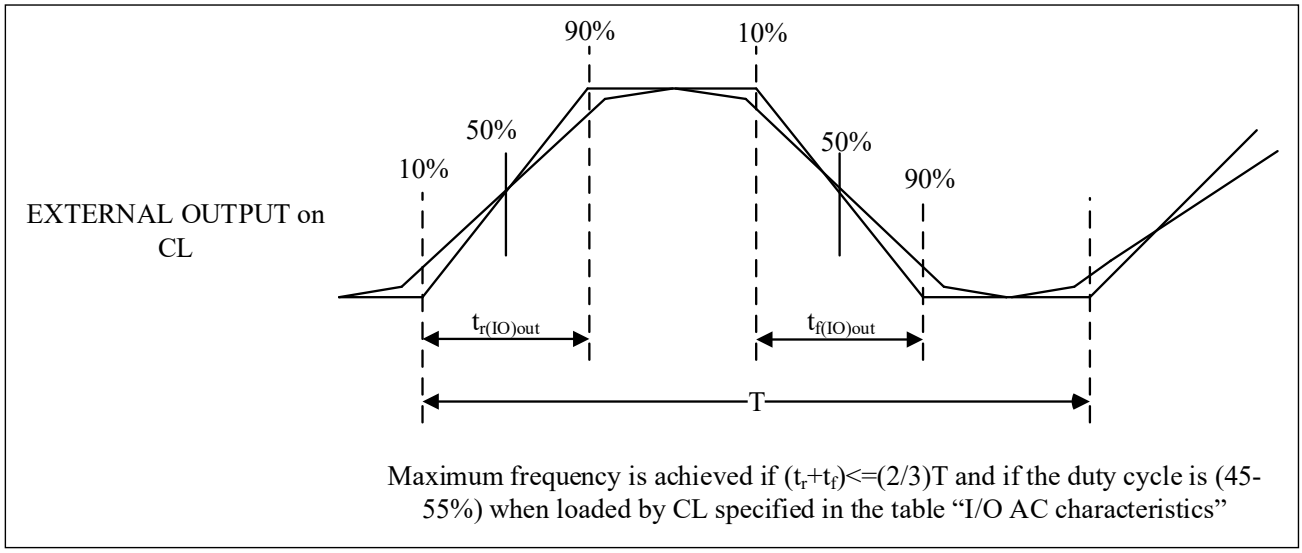
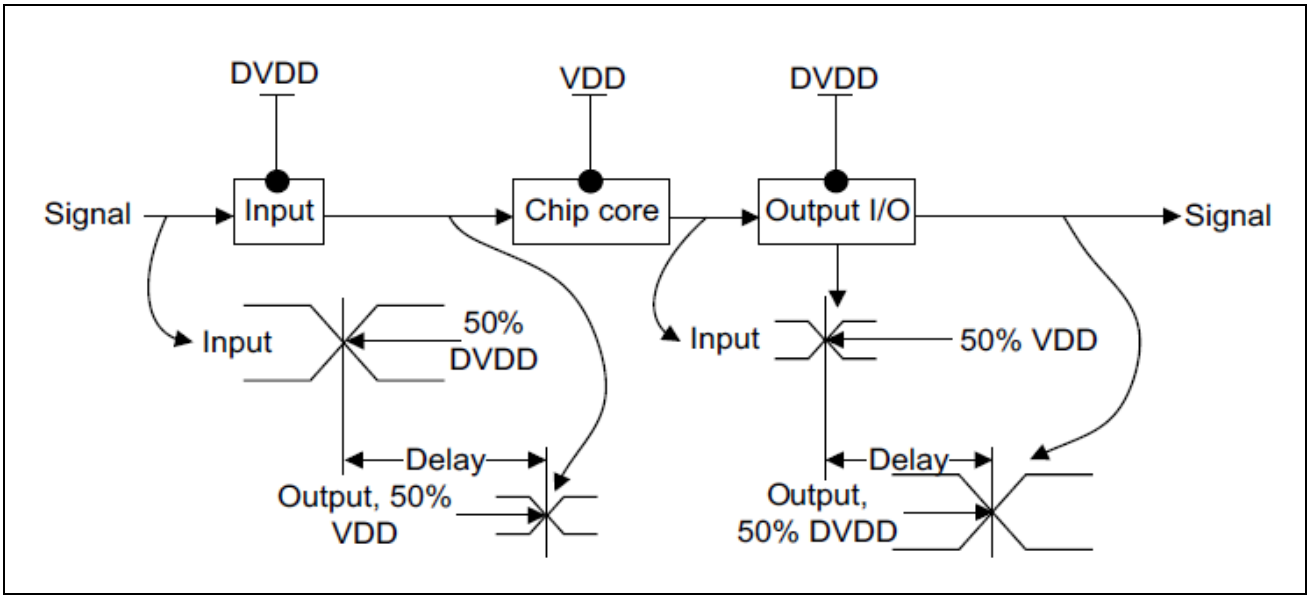


Figure 4-10 Transmission Delay



4.3.13 NRST Pin Characteristics

The NRST pin input driver uses CMOS process and integrates an non-disconnectable pull-up resistor R_{PU}(see T able 4-29). Unless otherwise specified, the parameters listed in Table 4-29 are measured under the conditions th at the ambient temperature and supply voltage meet Table 4-4.

Table 4-28 NRST Pin Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$V_{IL(NRST)}$(1)	NRST input low level voltage	V_{DD} = 3.3 V	Vss	-	0.8	V
		V_{DD} = 1.8 V	Vss	-	0.3*VDD	
$V_{IH(NRST)}$(1)	NRST input high level voltage	V_{DD} = 3.3 V	2	-	VDD	
		V_{DD} = 1.8 V	0.7*VDD	-	VDD	
$V_{hys(NRST)}$	NRST Schmitt trigger voltage hysteresis	V_{DD} = 3.3 V	200	-	-	mV
		V_{DD} = 1.8 V	0.1*VDD	-	-	V
R_{PU}	Weak pull-up equivalent	V_{DD} = 3.3 V	30	50	70	KΩ

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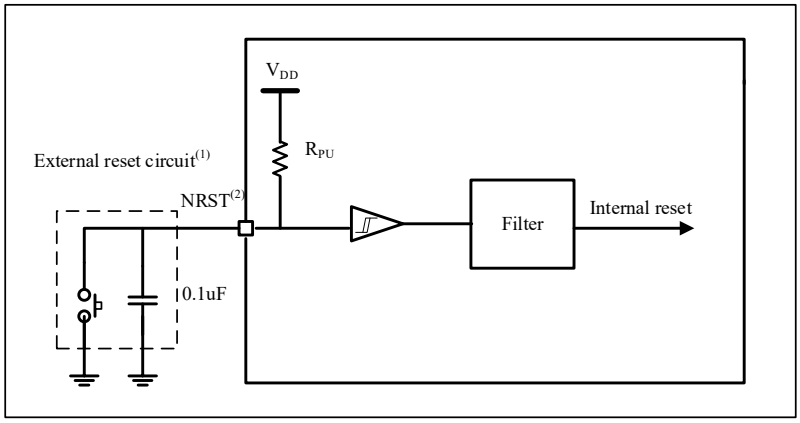
Symbol	Parameter	Condition	Min	Typ	Max	Unit
	resistance(2)					
$V_{F(NRST)}$(1)	NRST input filter pulse	-	-	-	100	ns
$V_{NF(NRST)}$(1)	NRST input non-filter pulse	-	300	-	-	ns

Notes:

(1) Guaranteed by design, not tested in production.

(2) The pull-up resistor is designed as a true resistor in series with a switchable PMOS. The resistance of this PMOS/NMOS switch is small (about 10%).

Figure 4-11 Recommended NRST Pin Protection



Notes:

(1) Filtering effect.

(2) The user must ensure that the voltage on the NRST pin is able to go below the maximum $V_{IL(NRST)}$ listed in Table 4-29, otherwise the MCU cannot be reset.

4.3.14 TIM Characteristics

For detailed characteristics of input/output multiplexed function pins (output compare, input capture, external clock, PWM output), please refer to Section 4.3.12.

Table 4-29 TIM1/8 Characteristics(1)

Symbol	Parameter	Condition	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time	-	1	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$= 144MHz	6.95	-	ns
f_{EXT}	Timer external clock frequency for CH1 to CH4	-	0	$f_{TIMxCLK}$/2	MHz
		$f_{TIMxCLK}$= 144MHz	0	72	MHz
Res_{TIM}	Timer resolution	-	-	16	bit
$t_{COUNTER}$	16-bit counter clock cycle when internal clock is selected	-	1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$= 144MHz	0.00695	455	µs
t_{MAX_COUNT}	Maximum possible count	-	-	65536 x 65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$= 144MHz	-	29.8	s

Note:(1) Guaranteed by design, not tested in production.

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Table 4-30 TIM2/3/4/5 Characteristics(1)

Symbol	Parameter	Condition	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time	-	1	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$= 72MHz	13.9	-	ns
f_{EXT}	Timer external clock frequency for CH1 to CH4	-	0	$f_{TIMxCLK}/2$	MHz
		$f_{TIMxCLK}$= 72MHz	0	36	MHz
Res_{TIM}	Timer resolution	-	-	16	bit
$t_{COUNTER}$	16-bit counter clock cycle when internal clock is selected	-	1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$= 72MHz	0.0139	910	μs
t_{MAX_COUNT}	Maximum possible count	-	-	65536 x 6553 6	$t_{TIMxCLK}$
		$f_{TIMxCLK}$= 72MHz	-	59.6	s

Note: Guaranteed by design, not tested in production.

Table 4-31 IWDG Maximum and minimum count reset times of IWDG (LSI = 40 KHz)

Prescaler	IWDG_PREDIV. PD[2:0]	Min(1) IWDG_RELV.REL[11:0]=0	Max(1) IWDG_RELV.REL[11:0]=0xFFF	Unit
/4	000	0.1	409.6	ms
/8	001	0.2	819.2	
/16	010	0.4	1638.4	
/32	011	0.8	3276.8	
/64	100	1.6	6553.6	
/128	101	3.2	13107.2	
/256	11x	6.4	26214.4	

Note:(1) Guaranteed by design, not tested in production.

Table 4-32 Maximum and minimum count reset times of WWDG (PCLK1 = 36MHz)

Prescaler	WWDG_CFG.TI MERB[1:0]	Min(1) WWDG_CGF.W[6:0]=0x3F	Max(1) WWDG_CFG.W[6:0]=0x7F	Unit
/1	00	0.113	7.28	ms
/2	01	0.227	14.56	
/3	10	0.455	29.12	
/4	11	0.910	58.25	

Note:(1) Guaranteed by design, not tested in production.

4.3.15 I²C Interface Characteristics

Unless otherwise specified, the parameters listed in Table 4-34 are measured under the environmental temperatu re, f_{PCLK1} frequency, and V_{DD} supply voltage conditions that meet Table 4-4.

The I²C interface of the N32G451 products complies with the standard I2C communication protocol, but with t he following limitations: SDA and SCL are not "true" open-drain pins. When configured as open-drain outputs, the PMOS between the pin and VDD is turned off, but still exists.

The I²C interface characteristics are listed in Table 4-34. For detailed characteristics of the multiplexed function pins (SDA and SCL), please refer to Section 4.3.12.

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Table 4-33 I²C Interface Characteristics

Symbol	Parameter	Standard mode(1)(2)		Fast mode(1)(2)		Fast+mode(1)(2)		Unit
		Min	Max	Min	Max	Min	Max	
f_{SCL}	I2C interface frequency	0.0	100	0	400	0	1000	KHz
$t_{h(STA)}$	Start condition hold time	4.0	-	0.6	-	0.26	-	μs
$t_{w(SCLL)}$	SCL clock low time	4.7	-	1.3	-	0.5	-	μs
$t_{w(SCLH)}$	SCL clock high time	4.0	-	0.6	-	0.26	-	μs
$t_{su(STA)}$	Repeated start condition setup time	4.7	-	0.6	-	0.26	-	μs
$t_{h(SDA)}$	SDA data hold time	0	3.4	0	0.9	0	0.4	μs
$t_{su(SDA)}$	SDA setup time	250.0	-	100	-	50	-	ns
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rise time	-	1000	20+0.1Cb	300	-	120	ns
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time	-	300	20+0.1Cb	300	-	120	ns
$t_{su(STO)}$	Stop condition setup time	4.0	-	0.6	-	0.26	-	μs
$t_{w(STO:STA)}$	Time from stop condition to start condition (bus free)	4.7	-	1.3	-	0.5	-	μs
Cb	Capacitive load for each bus	-	400	-	400	-	100	pF
$t_{v(SDA)}$	Data valid time	-	3.45	-	0.9	-	0.45	μs
$t_{v\ (ACK)}$	Acknowledge valid time	-	3.45	-	0.9	-	0.45	μs

Notes:

(1) Guaranteed by design, not tested in production.

(2) To reach the maximum frequency of I^2C in standard mode, f_{PCLK1} must be greater than 2 MHz. To reach the maximum frequency of I^2C in fast mode, f_{PCLK1} must be greater than 4 MHz

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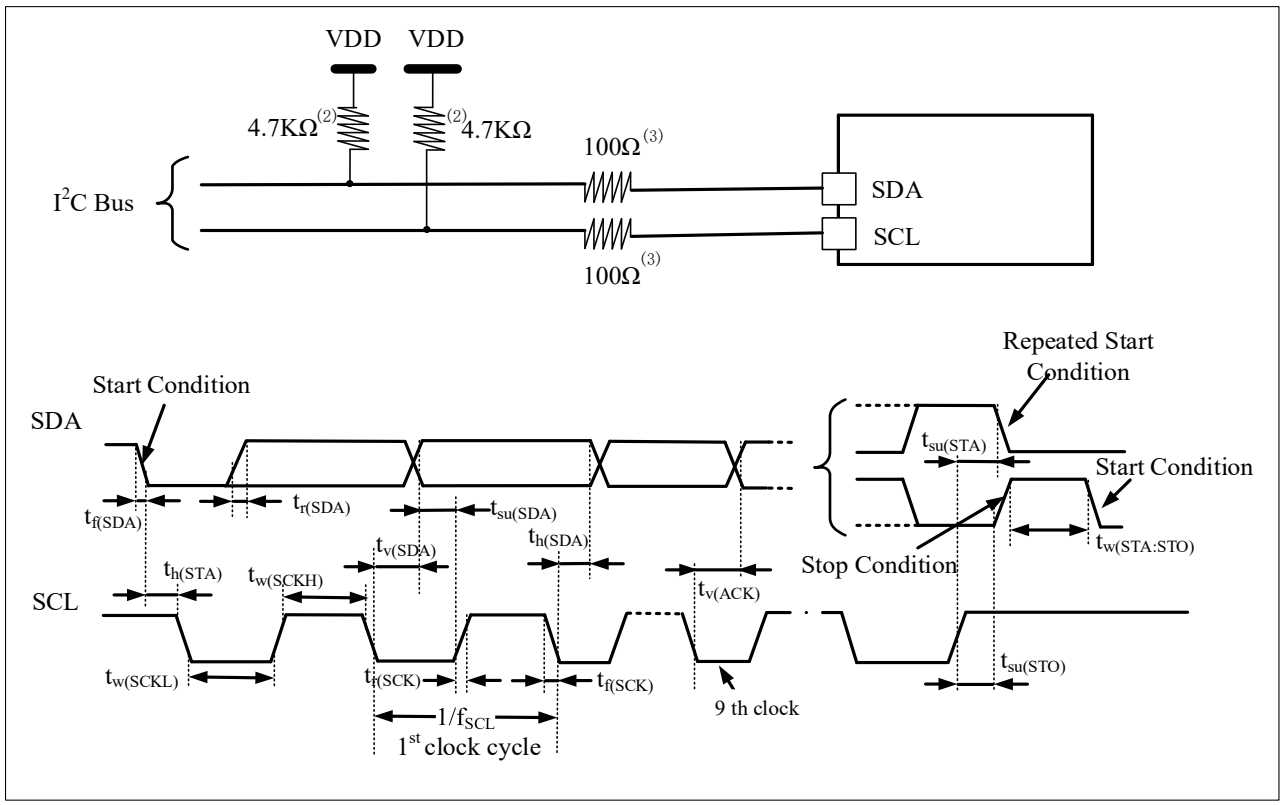
Figure 4-12 I²C Bus AC Waveform and Measurement Circuit (1)



Notes:

(1) Measurement points are set at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$。

(2) The pull-up resistor value depends on the I2C interface speed.

(3) The resistor value depends on the actual electrical characteristics. The serial resistor can be omitted and the signal lines connected directly.

4.3.16 SPI/I²S Interface Characteristics

Unless otherwise specified, the SPI parameters listed in Tables 4-35 and 4-36 and the I²S parameters listed in Table 4-37 are measured under the environmental temperature, f_{PCLKx} frequency, and V_{DD} supply voltage conditions that meet Table 4-4.

For detailed characteristics of input/output multiplexed function pins (NSS, SCLK, MOSI, MISO for SPI; WS, CLK, SD for I²S), please refer to Section 4.3.12.

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Table 4-34 SPI1 Characteristics(1)

Symbol	Parameter	Condition	Min	Max	Unit
f_{SCLK} $1/t_{c(SCLK)}$	SPI clock frequency	Master mode	-	36	MHz
		Slave mode	-	36	
$t_{r(SCLK)}$ $t_{f(SCLK)}$	SPI clock rise and fall time	Load capacitance: C = 30pF	-	6	ns
DuCy(SCK)	SPI slave input clock duty cycle	SPI Slave mode	45	55	%
$t_{su(NSS)}$ (1)	NSS setup time	Slave mode	$4t_{PCLK}$	-	ns
$t_{h(NSS)}$(1)	NSS hold time	Slave mode	$2t_{PCLK}$	-	
$t_{w(SCLKH)}$(1) $t_{w(SCLKL)}$(1)	SCLK high and low time	Master mode	t_{PCLK} - 2	t_{PCLK} + 2	
$t_{su(MI)}$(1)	Data input setup time	Master mode	3.5	-	
$t_{su(SI)}$(1)		Slave mode	3	-	
$t_{h(MI)}$(1)	Data input hold time	Master mode	3	-	
$t_{h(SI)}$(1)		Slave mode	3	-	
$t_{a(SO)}$(1)(2)	Data output access time	Slave mode, f_{PCLK} = 20MHz	0	$3t_{PCLK}$	
$t_{dis(SO)}$(1)(3)	Data output disable time	Slave mode	2	10	
$t_{v(SO)}$(1)	Data output valid time	Slave mode (after enable edge)	-	12.5	
$t_{v(MO)}$(1)		Master mode (after enable edge)	-	6.5	
$t_{h(SO)}$(1)	Data output hold time	Slave mode (after enable edge)	5	-	
$t_{h(MO)}$(1)		Master mode (after enable edge)	-0.5	-	

Table 4-35 SPI2/3 Characteristics(1)

Symbol	Parameter	Condition		Min	Max	Unit
f_{SCLK} $1/t_{c(SCLK)}$	SPI clock frequency	Master mode		-	18	MHz
		Slave mode		-	18	
$t_{r(SCLK)}$ $t_{f(SCLK)}$	SPI clock rise and fall time	Load capacitance: C = 30pF		-	8	ns
DuCy(SCK)	SPI slave input clock duty cycle	SPI slave mode		45	55	%
$t_{su(NSS)}$ (1)	NSS setup time	Slave mode		$4t_{PCLK}$	-	ns
$t_{h(NSS)}$(1)	NSS hold time	Slave mode		$2t_{PCLK}$	-	
$t_{w(SCLKH)}$(1) $t_{w(SCLKL)}$(1)	SCLK high and low time	Master mode		t_{PCLK} - 2	t_{PCLK} + 2	
$t_{su(MI)}$(1)	Data input setup time	Master mode	SPI2	4	-	
			SPI3	5	-	
$t_{su(SI)}$(1)		Slave mode	SPI2	4	-	
			SPI3	5	-	
$t_{h(MI)}$(1)	Data input hold time	Master mode	SPI2	2	-	
			SPI3	2.5	-	
$t_{h(SI)}$(1)		Slave mode	SPI2	2	-	
			SPI3	2	-	

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Symbol	Parameter	Condition		Min	Max	Unit
$t_{a(SO)}$(1)(2)	Data output access time	Slave mode, f_{PCLK} = 20MHz		0	$3t_{PCLK}$	
$t_{dis(SO)}$(1)(3)	Data output disable time	Slave mode		2	10	
$t_{v(SO)}$(1)	Data output valid time	Slave mode (after enable edge)	SPI2	-	13.5	
			SPI3	-	17.5	
$t_{v(MO)}$(1)		Master mode (after enable edge)	SPI2	-	6.5	
			SPI3	-	9	
$t_{h(SO)}$(1)	Data output hold time	Slave mode (after enable edge)	SPI2	4	-	
			SPI3			
$t_{h(MO)}$(1)		Master mode (after enable edge)	SPI2	1	-	
			SPI3			

Notes:

(1) *Guaranteed by design, not tested in production.*

(2) *The minimum value represents the minimum time to drive the output, the maximum value represents the maximum time to obtain the data correctly.*

(3) *The minimum value represents the minimum time to turn off the output, the maximum value represents the maximum time to put the data line in high impedance state.*

Figure 4-13 SPI Timing Diagram -- Slave Mode and CLKPHA=0

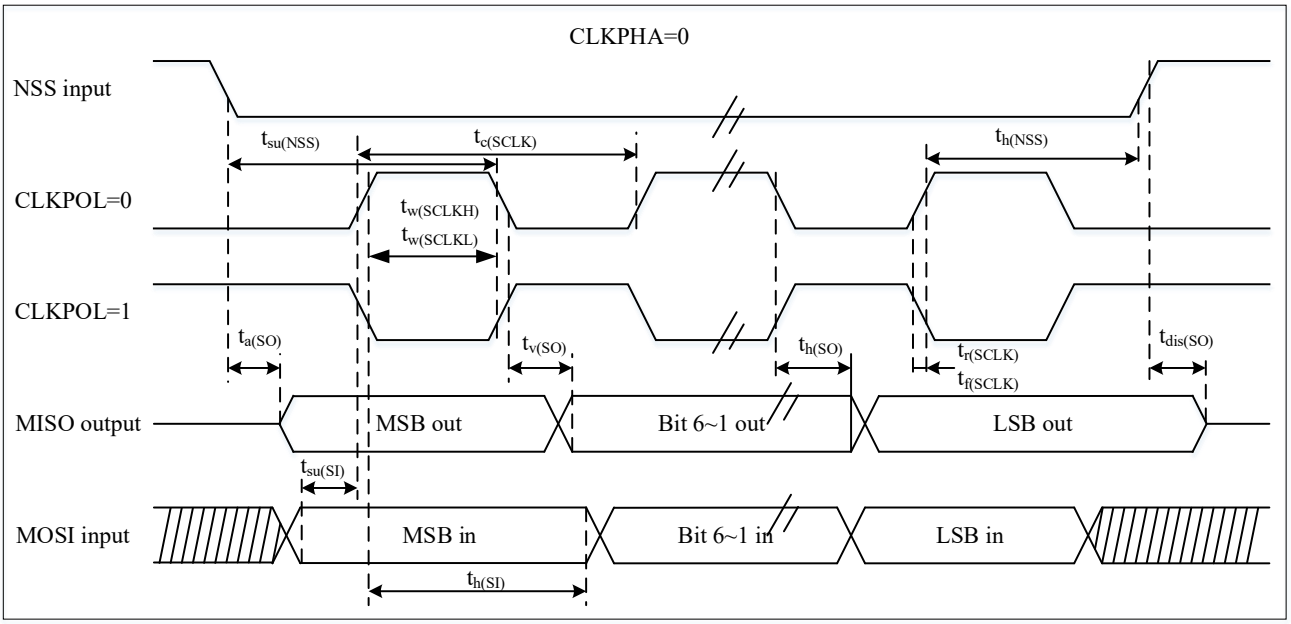

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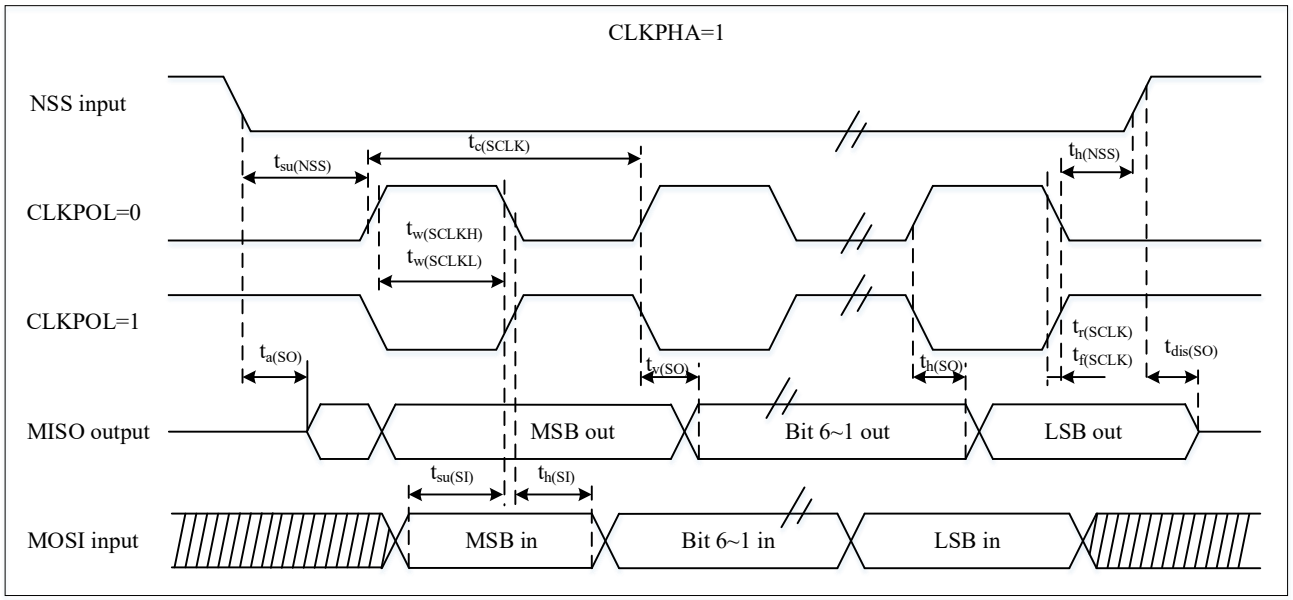
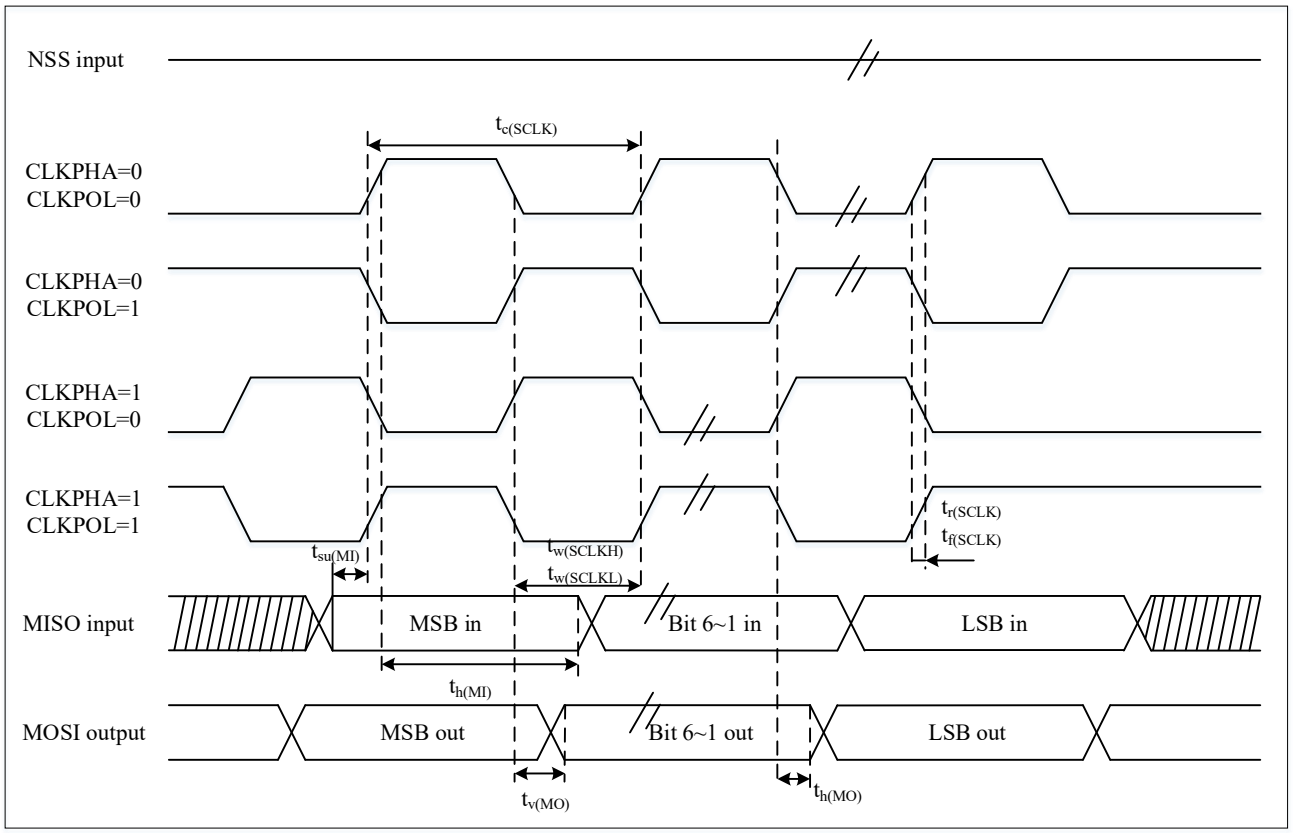
Figure 4-14 SPI Timing Diagram -- Slave Mode and CLKPHA=1(1)



Note:(1) Measurement points are set at $0.3V_{DD}$ and $0.7V_{DD}$。

Figure 4-15 SPI Timing Diagram -- Master Mode (1)



Note:(1) Measurement points are set at $0.3V_{DD}$ and $0.7V_{DD}$。

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Table 4-36 I²S Characteristics(1)

Symbol	Parameter	Condition		Min	Max	Unit
f_{MCLK}	I²S master clock frequency	Master mode		-	256Fs(3)	MHz
f_{CLK} $1/t_{c(CLK)}$	I²S clock frequency	Master mode (32bit)		-	64*Fs(3)	
		Slave mode (32bit)		-	64*Fs(3)	
DuCy(SCK)	I²S slave input clock duty cycle	I²S Slave mode		30	70	%
$t_{r(CLK)}$ $t_{f(CLK)}$	I²S clock rise and fall time	Load capacitance: CL = 50pF		-	8	ns
$t_{v(WS)}$ (1)	WS valid time	Master mode	I2S2	4.5	-	
			I2S3	6.5	-	
$t_{h(WS)}$(1)	WS hold time	Master mode	I2S2	4.5	-	
			I2S3	0.5		
$t_{su(WS)}$ (1)	WS setup time	Slave mode	I2S2	5.5	-	
			I2S3	7	-	
$t_{h(WS)}$(1)	WS hold time	Slave mode	I2S2	1.5	-	
			I2S3	2.5	-	
$t_{w(CLKH)}$(1)	CLK high and low time	Master mode, f_{PCLK} = 16MHz, audio 48kHz		312.5	-	
$t_{w(CLKL)}$(1)				345	-	
$t_{su(SD\_MR)}$(1)	Data input setup time	Master receiver	I2S2	4	-	
			I2S3	5	-	
$t_{su(SD\_SR)}$(1)		Slave receiver	I2S2	4	-	
			I2S3	4.5	-	
$t_{h(SD\_MR)}$(1)(2)	Data input hold time	Master receiver	I2S2	1.5	-	
			I2S3	1.5		
$t_{h(SD\_SR)}$(1)(2)		Slave receiver	I2S2	1.5	-	
			I2S3	1.5		
$t_{v(SD\_ST)}$(1)(2)	Data output valid time	Slave transmitter (after enable edge)	I2S2	-	14	
			I2S3	-	16.5	
$t_{h(SD\_ST)}$(1)	Data output hold time	Slave transmitter (after enable edge)	I2S2	3.5	-	
			I2S3	4.5	-	
$t_{v(SD\_MT)}$(1)(2)	Data output valid time	Master transmitter (after enable edge)	I2S2	-	6.5	
			I2S3	-	6	
$t_{h(SD\_MT)}$(1)	Data output hold time	Master transmitter (after enable edge)	I2S2	-0.5	-	
			I2S3	-0.5	-	

Notes:

(1) *Guaranteed by design, not tested in production.*

(2) *Depends on f_{PCLK}. For example, if f_{PCLK}=8MHz, then T_{PCLK}=1/f_{PCLK}=125ns.*

(3) *Audio sampling frequency.*

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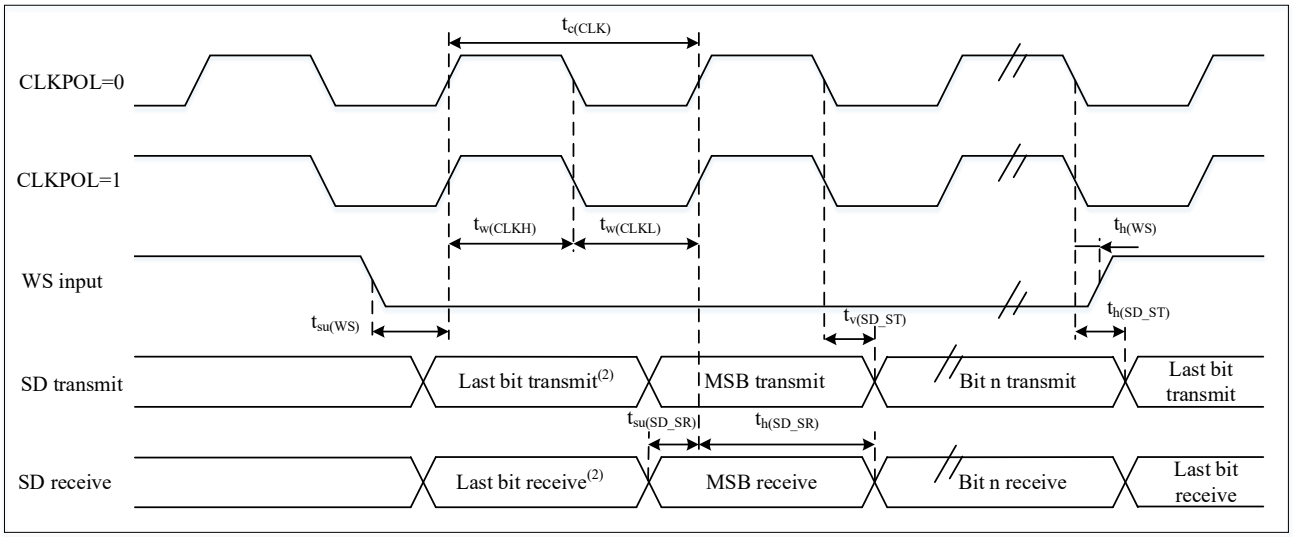
Figure 4-16 Slave Mode Timing Diagram (Philips Protocol)(1)

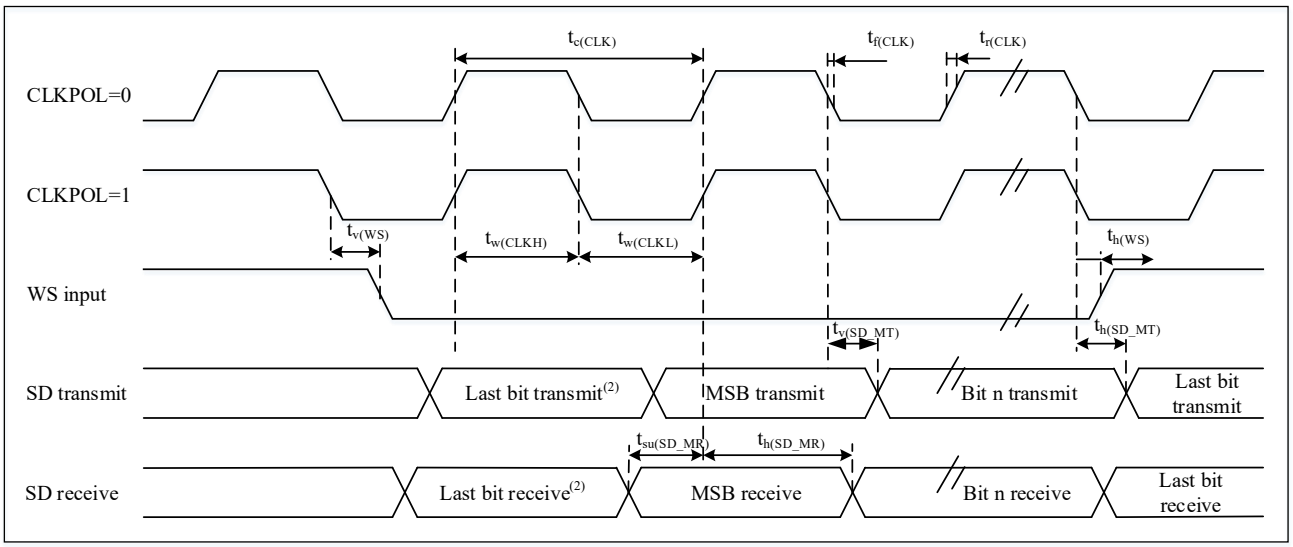


Notes:

(1) Measurement points are set at $0.3V_{DD}$ and $0.7V_{DD}$。

(2) The least significant bit of the previous byte is transmitted/received. There is no transmission/reception of this least significant bit before the first byte.

Figure 4-17 Master Mode Timing Diagram (Philips Protocol)(1)



Notes:

(1) Measurement points are set at $0.3V_{DD}$ and $0.7V_{DD}$。

(2) The least significant bit of the previous byte is transmitted/received. There is no transmission/reception of this least significant bit before the first byte.

4.3.17 SD/SDIO Host Interface Characteristics

Unless otherwise specified, the parameters listed in Table 4-38 are measured under the environmental temperatu re, f_{PCLKx} frequency, and V_{DD}supply voltage conditions that meet Table 4-4.

For detailed characteristics of the multiplexed function pins (D[7:0], CMD, CK), please refer to Section 4.3.12.

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Figure 4-18 SDIO Hogh Speed Mode

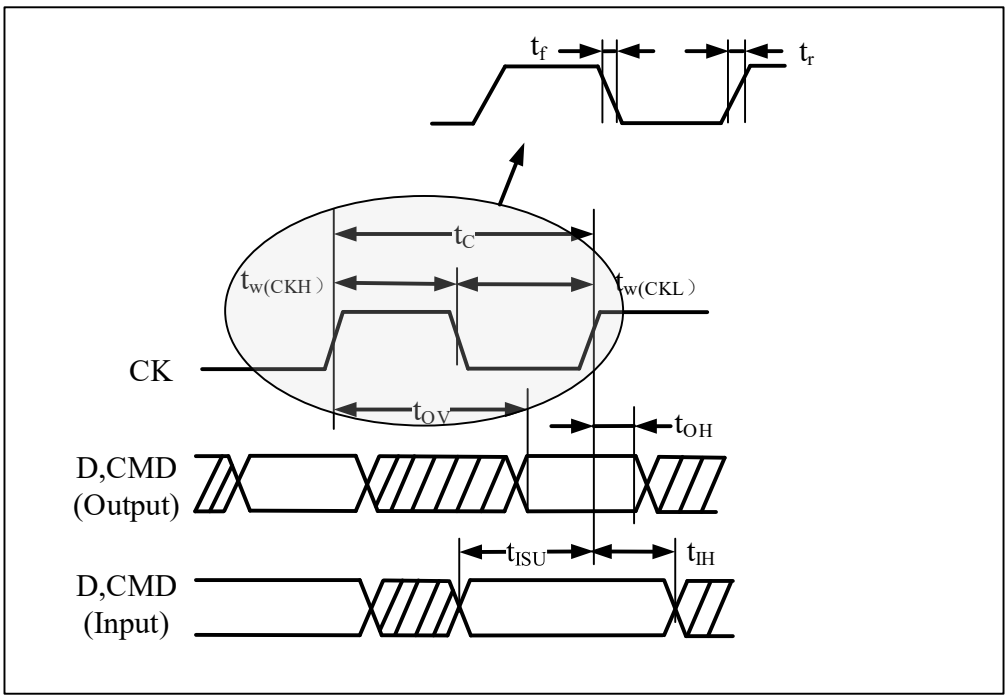

Figure 4-19 SD Default Mode

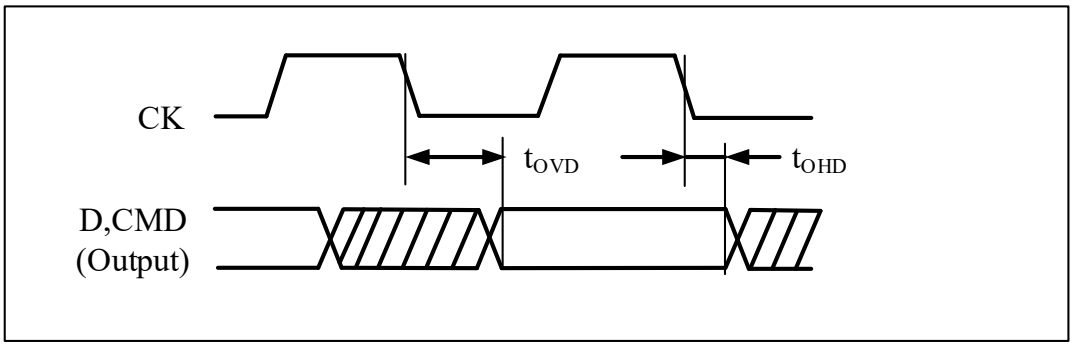

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Table 4-37 SD/MMC Interface Characteristics

Symbol	Parameter	Condition	Min	Max	Unit
f_{PP}	Clock frequency in data transfer mode	CL ≤ 30pF	0	48	MHz
$t_{W(CKL)}$	Clock low time, f_{PP} = 16 MHz	CL ≤ 30pF	32	-	ns
$t_{W(CKH)}$	Clock high time	CL ≤ 30pF	30	-	
t_r	Clock rise time	CL ≤ 30pF	-	6	
t_f	Clock fall time	CL ≤ 30pF	-	6	
CMD、D Input (referenced to CK)					
t_{ISU}	Input setup time	CL ≤ 30pF	1	-	ns
t_{IH}	Input hold time	CL ≤ 30pF	1	-	
CMD, D output in MMC and SD high speed mode (referenced to CK)					
t_{OV}	Output valid time	CL ≤ 30pF	-	6	ns
t_{OH}	Output hold time	CL ≤ 30pF	0	-	
CMD, D output in SD default mode (referenced to CK)					
t_{OVD}	Output valid time	CL ≤ 30pF	-	8	ns
t_{OHD}	Output hold time	CL ≤ 30pF	-1	-	

4.3.18 USB Characteristics

USB (Full Speed) interface has been certified by USB-IF/

Table 4-38 USB Startup Time

Symbol	Parameter	Max	Unit
$t_{STARTUP}$(1)	USB transceiver startup time	1	μs

Note: Guatanteed by design, not tested in production.

Table 4-39 USB DC Characteristics

Symbol	Parameter	Condition	Min(1)	Max(1)	Unit
Input Levels					
V_{DD}	USB operating voltage(2)	-	3.0(3)	3.6	V
V_{DI}(4)	Differential input sensitivity	I(USBDP，USBDM)	0.2	-	V
V_{CM}(4)	Differential common mode range	Including V_{DI} range	0.8	2.5	
V_{SE}(4)	Single-ended receiver threshold	-	1.3	2.0	
Output Levels					
V_{OL}	Static Output Low Level	Connect a load resistor (RL) of 1.5kΩ to 3.6V(5)	-	0.3	V
V_{OH}	Static Output High Level	Connect a load resistor (RL) of 15kΩ toV_{SS}(5)	2.8	3.6	

Notes:

(1) *All voltage measurements are referenced to the device-side ground.*

(2) *The USB operating voltage is specified as 3.0~3.6V to comply with USB 2.0 full-speed electrical specifications.*

(3) *Correct USB functionality for the N32G451 series products is guaranteed at 2.7V, not degraded within the 2.7~3.0V voltage range.*

(4) *RL, connected to the USB driver, is not tested in production.*

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Figure 4-20 USB Timing: Data Signal Rise and Fall Time Definition

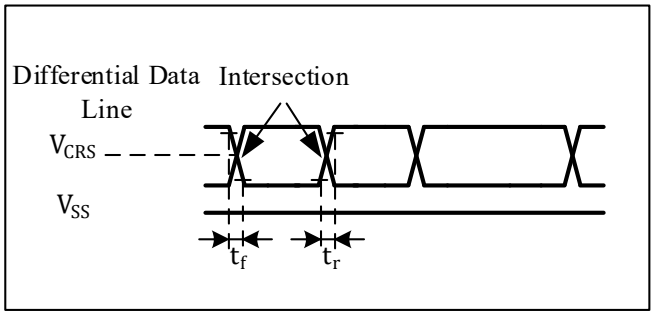

Table 4-40 USB Full Speed Electrical Characteristics

Symbol	Parameter	Condition	Min[1]	Max[1]	Unit
t_r	Rise time[2]	CL ≤ 50pF	4	20	ns
t_f	Fall time[2]	CL ≤ 50pF	4	20	ns
t_{rfm}	Rise and fall time matching	t_r / t_f	90	110	%
V_{CRS}	Output signal cross voltage	-	1.3	2.0	V
Rs	Output series matching resistor	Requires external matching resistor, close to chip pin	27	39	Ω

Notes:

(1) Guaranteed by design, not tested in production.

(2) Measured data signal from 10% to 90%. For more details, see Chapter 7 of USB Specification (version 2. 0).

4.3.19 Controller Area Network (CAN) Interface Characteristics

For details on the characteristics of the input/output multiplexing function pins (CAN_TX and CAN_RX), pleas e see Section 4.3.12.

4.3.20 12-bit Analog-to-Digital Converter (ADC) Electrical Parameters

Unless otherwise specified, the parameters in Table 4-42 are measured using the environmental temperature, fH CLK frequency and VDDA supply voltage that comply with the conditions in Table 4-4. Note: It is recommen ded to perform calibration once at every power-up.

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Table 4-41 ADC Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{DDA}	Supply voltage	-	1.8	-	3.6	V
V_{REF+}	Positive reference voltage	-	1.8	-	V_{DDA}	
f_{ADC}	AADC clock frequency	-	-	-	80	MHz
f_s(2)	Sampling rate	1.8V ≤ V_{DD} ≤ 3.6 V，分辨率12bit	0.01(2)	-	4.7(1)	MHz
		1.8V ≤ V_{DD} ≤ 3.6 V，分辨率10bit	0.012(2)	-	6.1(1)	MHz
		1.8V ≤ V_{DD} ≤ 3.6 V，分辨率8bit	0.014(2)	-	7.3(1)	MHz
		1.8V ≤ V_{DD} ≤ 3.6 V，分辨率6bit	0.0175(2)	-	8.9(1)	MHz
V_{AIN}	Conversion voltage range(3)	-	0(V_{SSA} or V_{REF} Connected to GND)	-	V_{REF+}	V
R_{ADC}(2)	Sampling switch resistance	Fast channel at 3.6V voltage condition	-	-	137.6	Ω
		Slow channel at 3.6Vvoltage condition	-	-	147	Ω
C_{ADC}(2)	Internal sampling and hold capacitor	-	-	5	-	pF
SNDR	Signal-to-Noise and Distortion Ratio	-	-	65	-	dBFS
T_{cal}	Calibration time	-	82			$1/f_{ADC}$
t_S(2)	Sampling time	f_{ADC} = 80 MHz Fast channel resolution 12bit	0.056	-	8.35	μs
		f_{ADC} = 80 MHz Slow channel resolution 12bit	0.056	-	8.35	
Ts(2)	Sampling period	f_{ADC} = 80 MHz Fast channel resolution 12bit	4.5	-	601.5	$1/f_{ADC}$
		f_{ADC} = 80 MHz Slow channel resolution 12bit	4.5	-	601.5	
t_{STAB}(2)	Power-up time	-	6	10	20	μs
t_{CONV}(2)	Total conversion time (including sampling time)	-	8~614 (sampling TS + successive approximation 6.5/8.5/10.5/12.5)			$1/f_{ADC}$

Notea:

(1) Only fast channels supported, f_{ADC} = 80 MHz.

(2) Guaranteed by design, not tested in production.

(3) Depending on different packages, V_{REF+} can be internally connected to V_{DDA}, V_{REF-} can be internally connected to V_{SSA}.

Formula 1：Max R_{AIN} Formula

$$R_{AIN} < \frac{T_S}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$$

The above formula (Formula 1) is used to determine the maximum external impedance so that the error

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can be less than 1/4 LSB. Where N=12 (representing 12-bit resolution).

Table 4-42 ADC Sampling Time(1)(2)

Input	Resolution	Rin（kΩ）	Min Sampling Time（ns）	Input	Resolution	Rin (kΩ)	Min Sampling Time(ns)
Fast channel	12-bit	0.06	37	Slow channel	12-bit	0.05	53
		0.36	45			0.35	73
		0.86	79			0.85	103
		4.86	300			4.85	345
		9.86	576			9.85	651
		19.86	1131			19.85	1257
		49.86	2776			49.85	3051
		99.86	5475			99.85	5982
Fast channel	10-bit	0.06	25	Slow channel	10-bit	0.05	46
		0.36	39			0.35	61
		0.86	64			0.85	88
		4.86	250			4.85	357
		9.86	478			9.85	540
		19.86	935			19.85	1040
		49.86	2294			49.85	2526
		99.86	4532			99.85	4963
Fast channel	8-bit	0.06	22	Slow channel	8-bit	0.05	39
		0.36	33			0.35	50
		0.86	52			0.85	71
		4.86	202			4.85	234
		9.86	391			9.85	457
		19.86	800			19.85	1012
		49.86	1838			49.85	2027
		99.86	3632			99.85	3984
Fast channel	6-bit	0.06	19	Slow channel	6-bit	0.05	32
		0.36	27			0.35	40
		0.86	41			0.85	56
		4.86	153			4.85	177
		9.86	292			9.85	330
		19.86	569			19.85	642
		49.86	1435			49.85	1666
		99.86	3001			99.85	3919

Notes:

(1) Guaranteed by design, not tested in production.

(2) Typical values are measured at T_A=25°C, V_{DD} =3.3V.

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Table 4-43 ADC Accuracy -- Limited Test Conditions (1)(2)

Symbol	Parameter	Test Conditions	Typ	Max(3)	Unit
ET(4)	Total unadjusted error	f_{HCLK} = 72 MHz, f_{ADC} = 72 MHz, sample rate=1.75M sps, V_{DDA} = 3.3V, T_A = 25 °C Measurement is performed after ADC calibration. V_{REF+}= V_{DDA}	±1.3	-	LSB
EO(4)	Offset error		±1	-	
ED	Differential linearity error		±0.7	-	
EL	Integral linearity error		±0.8	-	

Notes:

(1) *The ADC DC accuracy values are measured after internal calibration.*

(2) *ADC accuracy versus reverse injection current: Reverse current injection should be avoided on any standa rd analog input pin as this will significantly degrade the conversion accuracy taking place on another analog input pin. It is recommended to add a Schottky diode (between pin and ground) on the standard analog pins that m ay produce reverse injection current.*

(3) *If the forward injection current is within the IINJ(PIN) and ΣIINJ(PIN) ranges given in Section 4.3.12, it will not affect the ADC accuracy.*

(4) *Guaranteed by synthetic evaluation, not tested in production.*

Figure 4-21 ADC Accuracy Characteristics

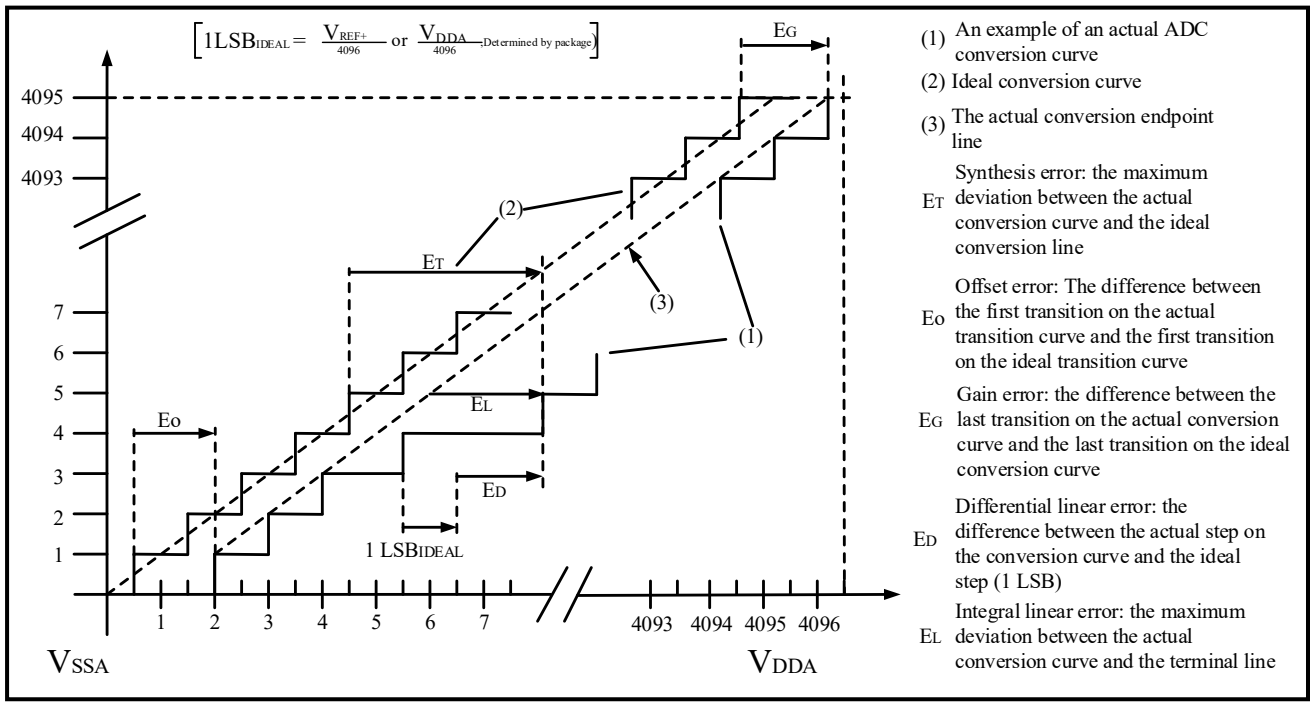

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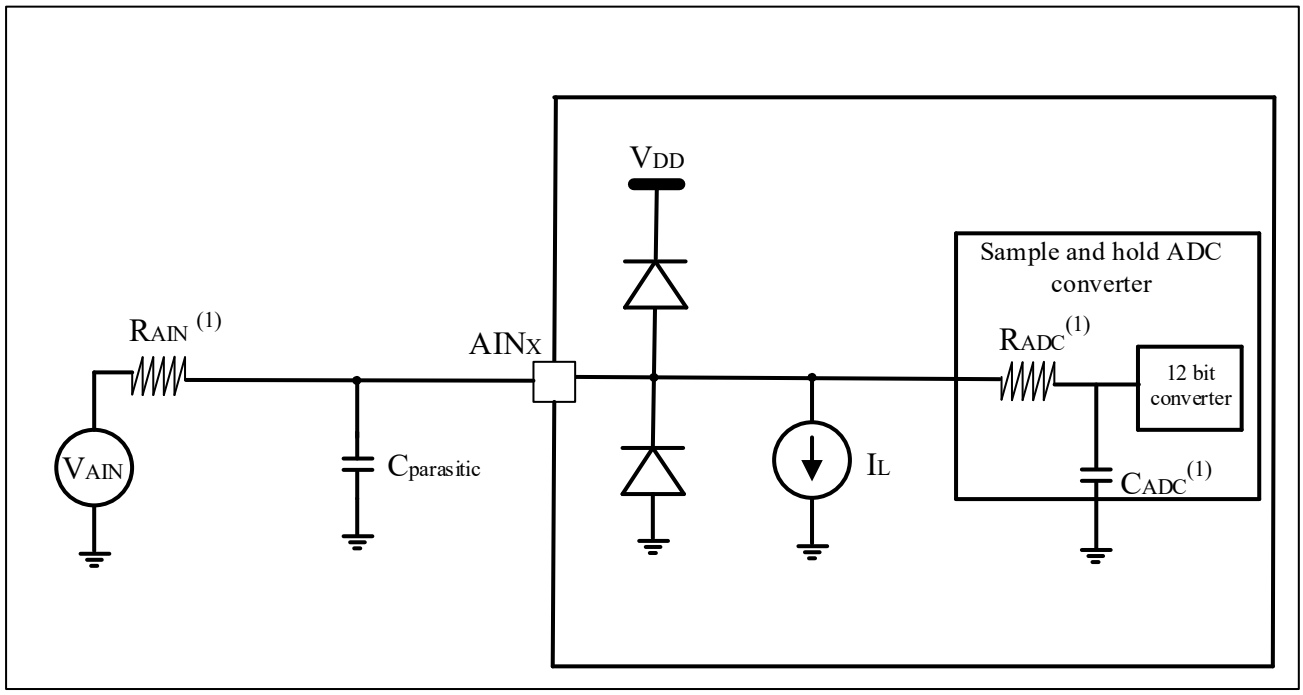
Figure 4-22 Typical Connection Diagram Using ADC



Note:(1) For the values of R_{AIN}、R_{ADC} and C_{ADC}, refer to Table 4-41。

Note: Cparasitic represents the parasitic capacitance on the PCB (related to the quality of soldering and PCB layout) and on the pads (about 7pF). A larger Cparasitic value will reduce the conversion accuracy, which can be resolved by decreas ing f_{ADC}。

PCB Design Recommendations

Depending on whether V_{REF+} is connected to $V_{DDA,}$ 电the power decompling should be connected as shown in FigureFigure 4-23 or FigureFigure 4-24. The 10nF capacitors in the figure must be ceramic capacitors (of good quality)

and should be placed as close to the MCU chip as possible.

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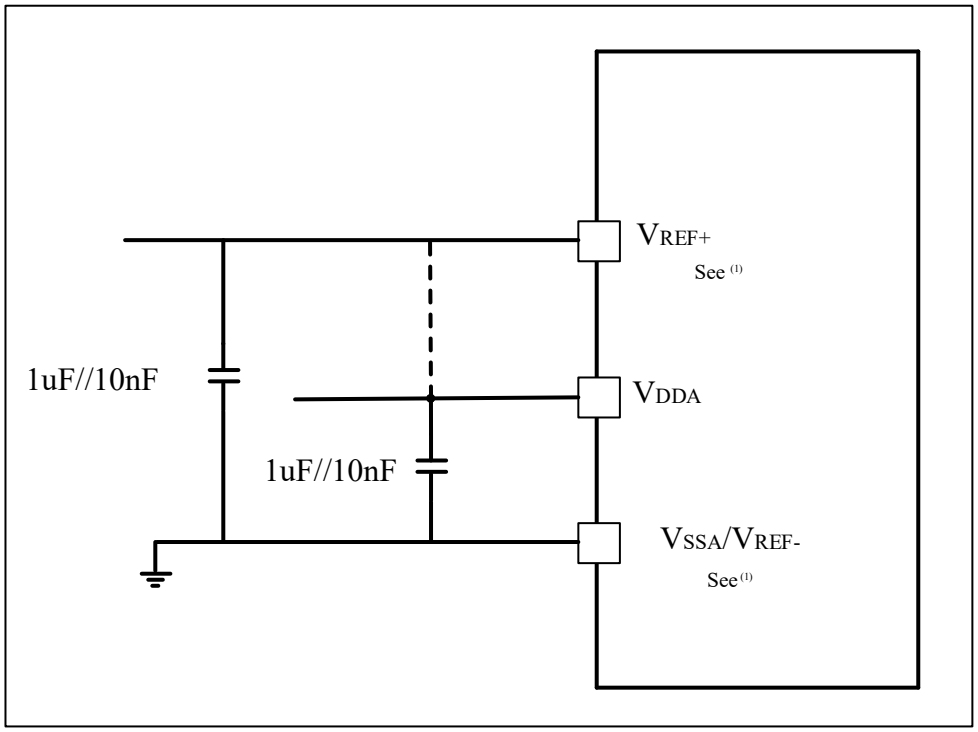
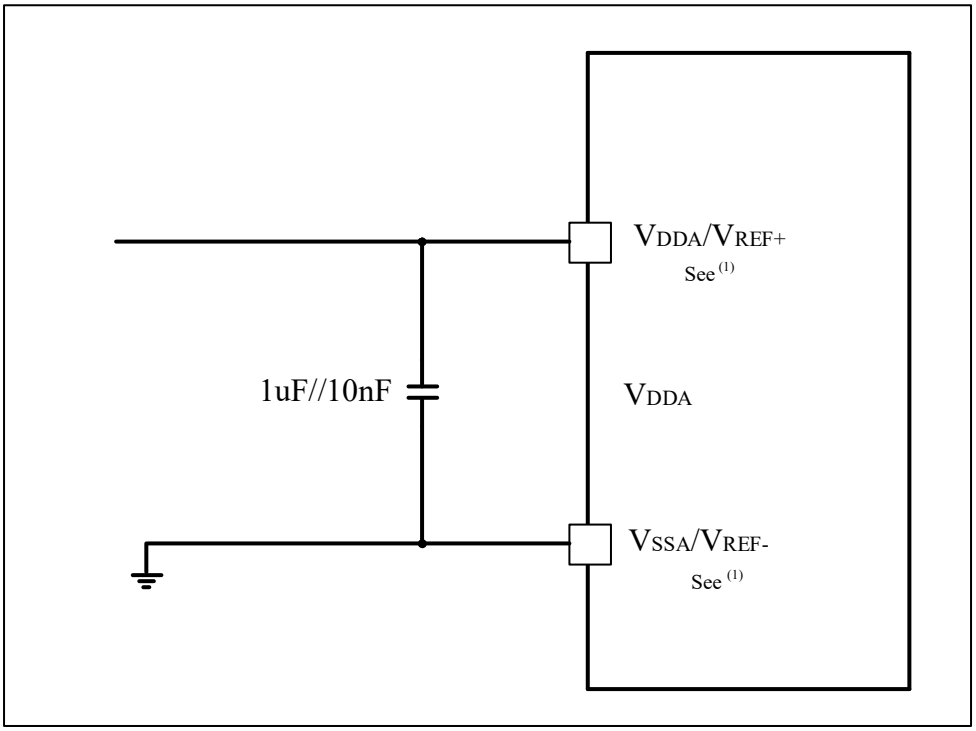
Figure 4-23 Power Supply and Reference Voltage Decoupling Circuit (V_{REF+} Not Connected to V_{DDA})



Note:(1) V_{REF+} and $V_{REF-\ inputsappear}$ inputs only appear in products with more than 100 pins

Figure 4-24 Power Supply and Reference Voltage Decoupling Circuit (V_{REF+} Connected to V_{DDA})



Note:(1) V_{REF+} and V_{REF-} inputs only appear in products with over 100 pins.

4.3.21 12 Digital-to-Analog Converter (DAC) Electrical Parameters

Unless otherwise specified, the parameters in Table 4-45 are measured under ambient temperature conditions, f_{HCLK} frequency and V_{DDA}supply voltage that conform to Table 4-4.

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Table 4-44 DAC Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Comments
V_{DDA}	Analog Supply Voltage	2.4	-	3.6	V	-
V_{DDD}	Digital Supply Voltage	1.0	1.1	1.2	V	-
V_{REF+}	Reference Voltage	2.4	-	3.6	V	V_{REF+} must always be lower than V_{DDA}
V_{SSA}	Ground	0	-	0	V	-
R_L	Load Resistance with Buffer Open	5	-	-	KΩ	Minimum load resistance between DAC_OUT and V_{SSA}
C_L	Load Capacitance	-	-	50	pF	Maximum capacitance on DAC_OUT pin
DAC_OUT Min	DAC_OUT Voltage with Buffer Open (corresponding to 12-bit input values 0x0E0~0Xf1c with	0.2	-	-	V	Specifies max DAC output range when V_{REF+}=3.6V, corresponds to 12-bit input value 0x0E0~0xF1C, when V_{REF+}=2.4V, corresponds to 12-bit input value 0x155~0xEAB。
DAC_OUT Max	DAC_OUT voltage when buffer is on	-	-	V_{REF+} – 0.2	V	
	DAC_OUT voltage when buffer is off	-	-	V_{REF+} – 5LSB		
I_{DD}	DC current consumption in idle mode (syandby mode) (V_{DDD}+V_{DDA}+V_{REF+})	-	425	600	μA	No load, input midpoint 0x800
		-	500	700		No load, when V_{REF+}=3.6V, input max value
I_{DDQ}	DC current consumption inpower-down mode (V_{DDD}+V_{DDA}+V_{REF+})	-	5	350	nA	No load
	DC current consumption in power-down mode (V_{DDA}+V_{REF+})	-	5	200		
DNL	Differntial non-linearity (deviation between 2 Consecutive codes)	-	±0.5	-	LSB	DAC configured for 10 bits (B1=B0=0 always)
		-	±2	-	LSB	DAC configured for 12 bits
INL	Integral non-linearity (deviation value at code 1 and a line between code 0 and code 4095)	-	±6	-	LSB	DAC configured for 12 bits
Offset	Offset error (deviation between measured value at code 0x800 and idle value V_{REF+}/2)	-	±15	-	mV	DAC configured for 12bits
		-	±17	-	LSB	When V_{REF+}=3.6V, DAC configured for 12bits
Gain Error	Gain error	-	±0.5	-	%	DAC configured for 12bits
$t_{SETTLING}$	Settling time (full scale: 10-bit input code changes from min to max value, DAC_OUT reaches its final value ±1 LSB)	-	5	7	μs	C_{LOAD} ≤ 50pF R_{LOAD} ≥ 5kΩ
Update Rate	Maximum frequency to obtain correct DAC_OUT when input code changes by small amount (from value i to i+1LSB)	-	-	1	MS/s	C_{LOAD} ≤ 50pF R_{LOAD} ≥ 5kΩ
t_{WAKEUP}	Time to wake up from power-down mode (setting CHxEN in DAC control register)	-	6.5	10	μs	C_{LOAD} ≤ 50pF，R_{LOAD} ≥ 5kΩ Input code between min and max possible values
PSRR+	Power supply rejection ratio(relative to V_{DD}33A)(static DC measurement)	-	-67	-40	dB	No R_{LOAD}，C_{LOAD} ≤ 50pF

4.3.22 Temperature Sensor (TS) Charactersitics

Unless otherwise specified, the parameters in Table 4-46 are measured under the ambient temperature, fHCLK frequency, and VDDA supply voltage conditions specified in Table 4-4.

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Table 4-45 Temperature Sensor Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_L(1)	Linearity of VSENSE relative to temperature	-	±1	±4	ºC
Avg_Slope(1)	Average slope	-	-4.1	-	mV/ºC
V_{30}(1)	Voltage at 30ºC	-	1.32	-	V
t_{START}(1)	Startup time	-	10	-	µs
T_{S_temp}(2)(3)	ADC sampling time when reading temperature	8.3	-	-	µs

Notes:

(1) *Guaranteed by characterization, not tested in production.*

(2) *Guaranteed by design, not tested in production.*

(3) *Minimum sampling time can be determined by application through multiple iterations.*

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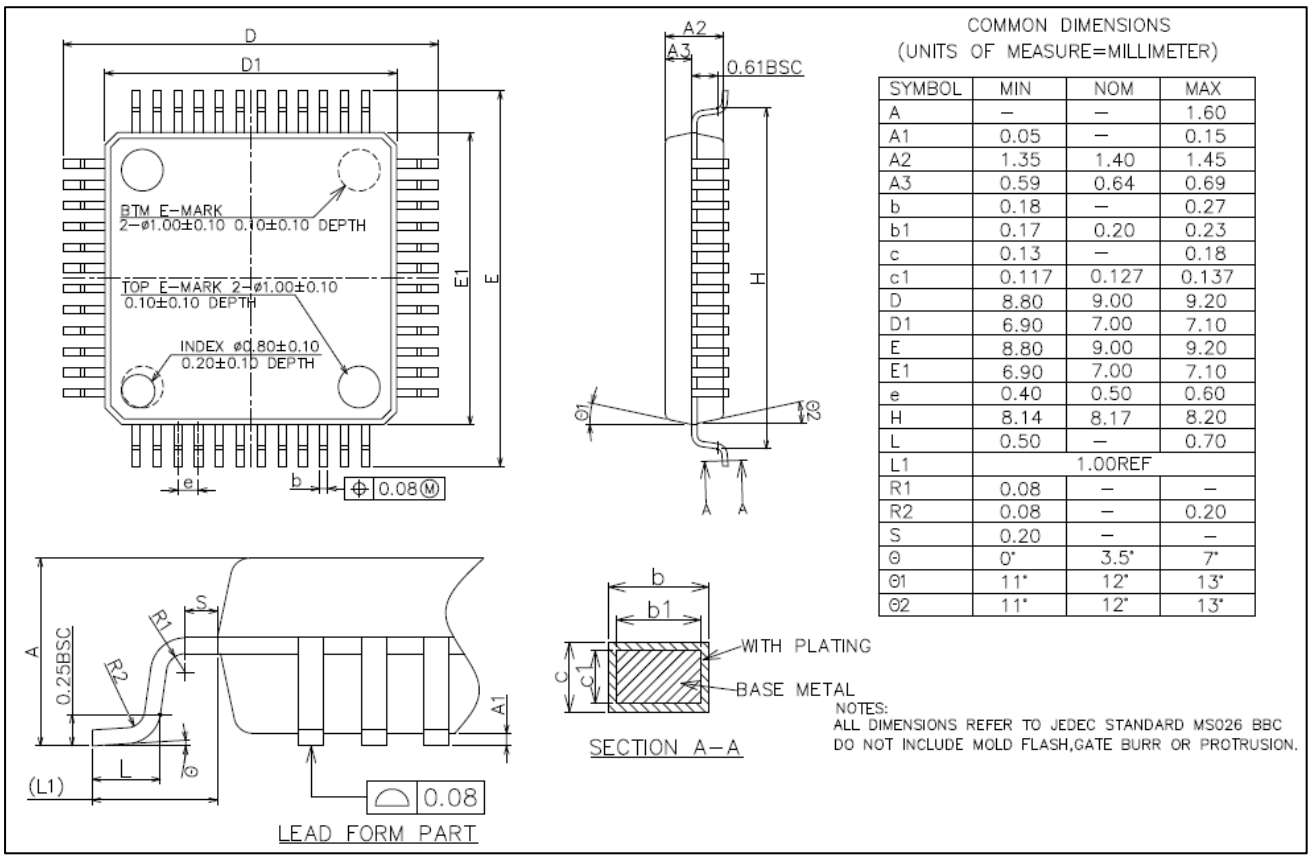
5 Package Dimensions

5.1 LQFP48

Figure 5-1 LQFP48 Package Dimensions



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	–	–	1.60
A1	0.05	–	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	–	0.27
b1	0.17	0.20	0.23
c	0.13	–	0.18
c1	0.117	0.127	0.137
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
e	0.40	0.50	0.60
H	8.14	8.17	8.20
L	0.50	–	0.70
L1		1.00REF	
R1	0.08	–	–
R2	0.08	–	0.20
S	0.20	–	–
θ	0°	3.5°	7°
θ1	11°	12°	13°
θ2	11°	12°	13°

NOTES:
ALL DIMENSIONS REFER TO JEDEC STANDARD MS026 BBC
DO NOT INCLUDE MOLD FLASH,GATE BURR OR PROTRUSION.

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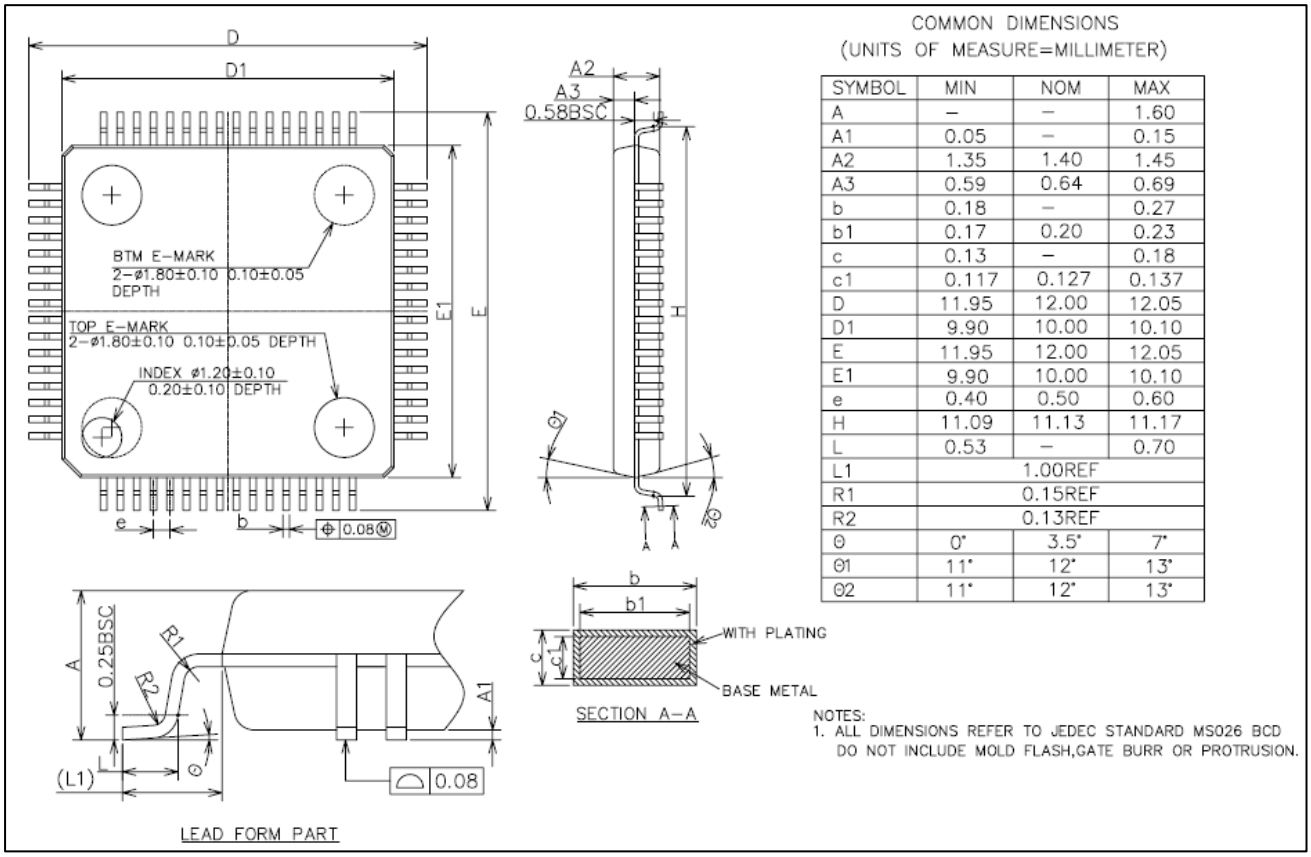
5.2 LQFP64

Figure 5-2 LQFP64 Package Dimensions



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	–	–	1.60
A1	0.05	–	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	–	0.27
b1	0.17	0.20	0.23
c	0.13	–	0.18
c1	0.117	0.127	0.137
D	11.95	12.00	12.05
D1	9.90	10.00	10.10
E	11.95	12.00	12.05
E1	9.90	10.00	10.10
e	0.40	0.50	0.60
H	11.09	11.13	11.17
L	0.53	–	0.70
L1	1.00REF		
R1	0.15REF		
R2	0.13REF		
θ	0°	3.5°	7°
θ1	11°	12°	13°
θ2	11°	12°	13°

NOTES:
1. ALL DIMENSIONS REFER TO JEDEC STANDARD MS026 BCD
DO NOT INCLUDE MOLD FLASH,GATE BURR OR PROTRUSION.

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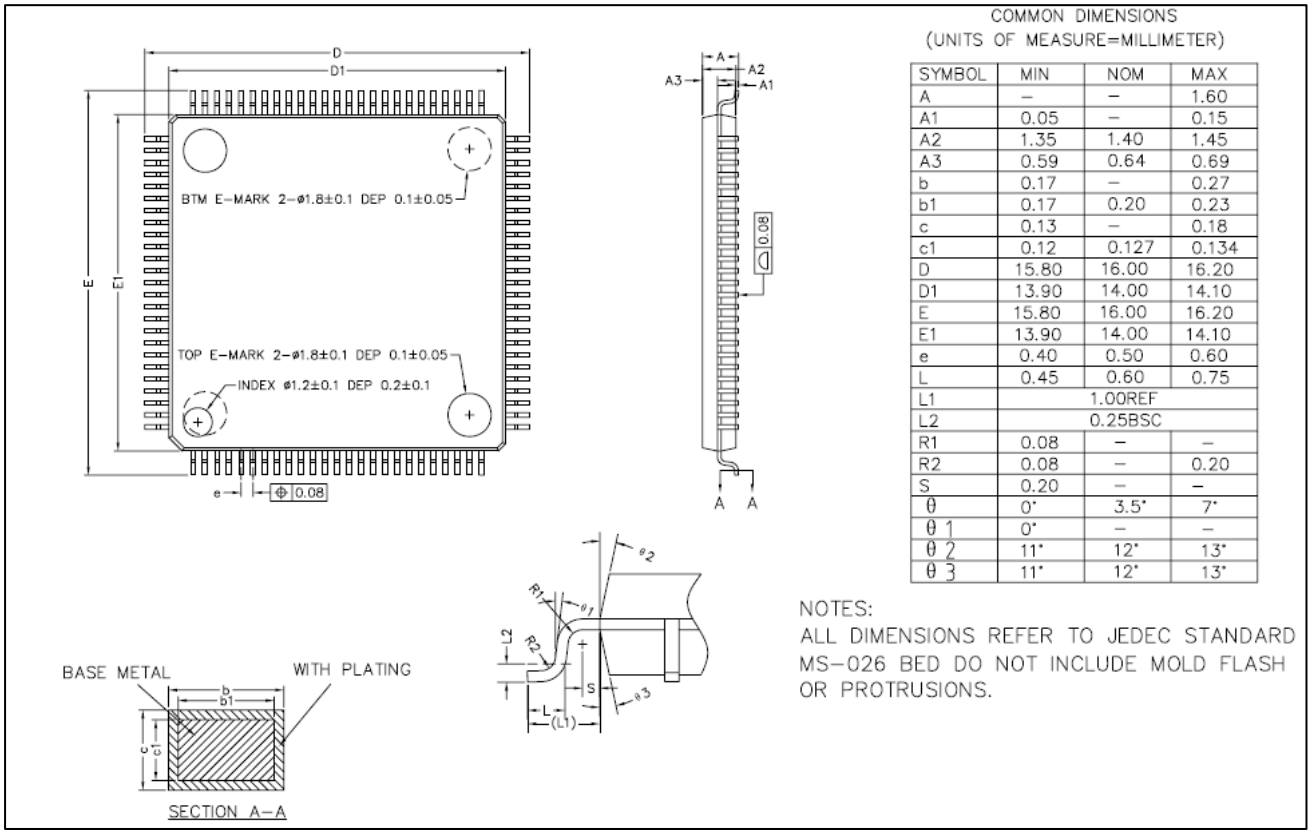
5.3 LQFP100

Figure 5-3 LQFP100 Package Dimensions



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	–	–	1.60
A1	0.05	–	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.17	–	0.27
b1	0.17	0.20	0.23
c	0.13	–	0.18
c1	0.12	0.127	0.134
D	15.80	16.00	16.20
D1	13.90	14.00	14.10
E	15.80	16.00	16.20
E1	13.90	14.00	14.10
e	0.40	0.50	0.60
L	0.45	0.60	0.75
L1	1.00REF		
L2	0.25BSC		
R1	0.08	–	–
R2	0.08	–	0.20
S	0.20	–	–
θ	0°	3.5°	7°
θ 1	0°	–	–
θ 2	11°	12°	13°
θ 3	11°	12°	13°

NOTES:
ALL DIMENSIONS REFER TO JEDEC STANDARD MS-026 BED DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.

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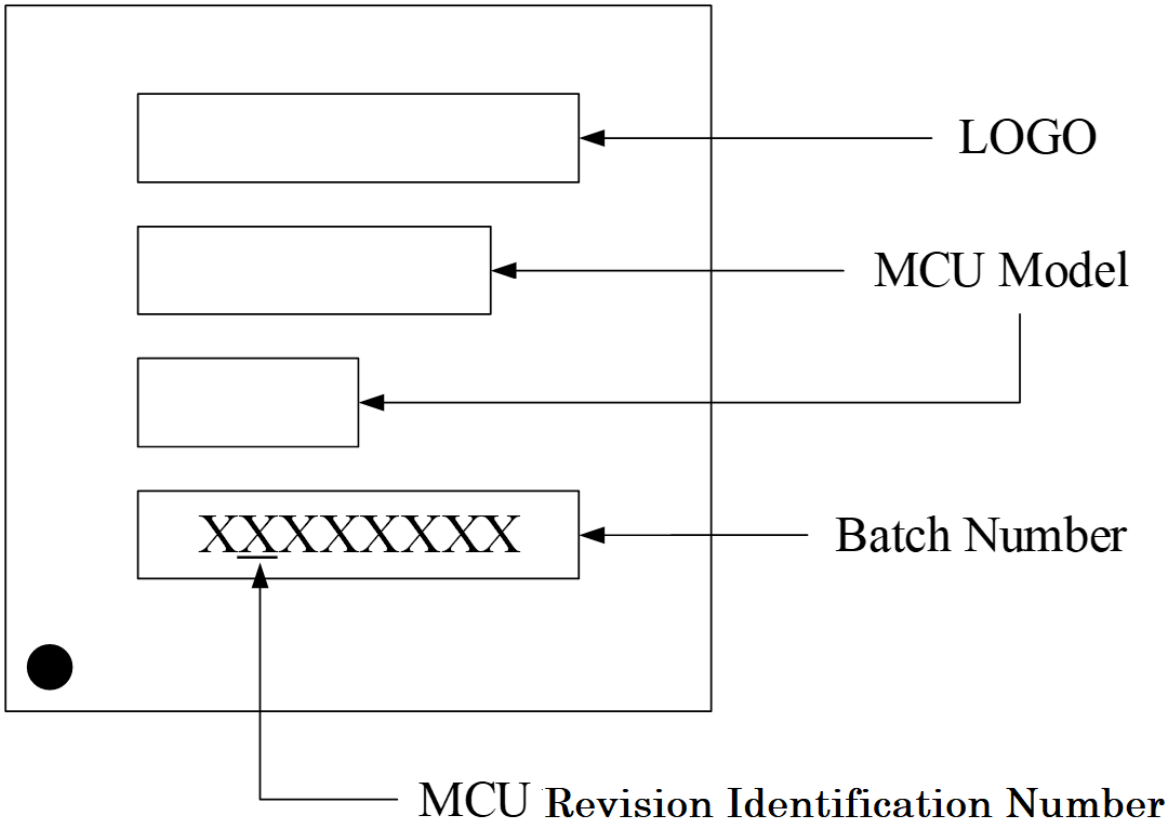
5.4 Maring Description

Figure 5-4 Marking Diagram



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6 Revision History

Version	Data	Changes
V1.0.0	2023.5.28	Initial release

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