N32G451xB/xC/xE Product Brief

The N32G451 series adopts a 32-bit ARM Cortex-M4F core, with a maximum operating frequency of 144MHz, supporting floating-point operations and DSP instructions. It integrates up to 512KB embedded Flash, 96KB SRAM, multiple communication bus interfaces like U(S)ART, I2C, SPI, USB, CAN, and analog interfaces such as 12-bit ADC and DAC. It also features a built-in hardware acceleration engine for encryption algorithms.

Key Features

- **CPU Core**
  - 32-bit ARM Cortex-M4 core + FPU, single-cycle hardware multiply and divide instructions, supports DSP instructions and MPU
  - Built-in 8KB instruction Cache supports Flash accelerator unit for zero-wait program execution.
  - Maximum frequency of 144MHz, 180DMIPS
- **Memories**
  - Up to 512KByte on-chip Flash, supports encrypted storage function, partition management and data protection, supports hardware ECC check, 100,000 erase/write cycles, 10-year data retention.
  - Up to 96KByte on-chip SRAM (including 16KByte Retention RAM), supports hardware parity check.
- **Low Power Management**
  - Stop0 mode: 150uA, RTC Run, all SRAM retained, all IOs retained, 20us fast wake-up.
  - Stop2 mode: 10uA, RTC Run, 16KByte Retention SRAM retained, CPU registers retained, all IOs retained, 40us fast wake-up.
  - Standby mode: 3uA, 84 backup registers retained, all IOs retained, optional RTC Run, 16KByte Retention SRAM retained, supports independent power supply via VBAT pin, 100us fast wake-up.
- **Clock**
  - 4MHz~32MHz external high-speed crystal oscillator
  - 32.768KHz external low-speed crystal
  - High-speed internal RC 8MHz
  - Low-speed Internal RC 40KHz
  - Built-in high-speed PLL
  - Supports 1-channel clock output, configurable as system clock, HSE, HSI or PLL divisional output.
- **Reset**
  - Supports power-on/power-down/brown-out/external pin reset.
  - Supports watchdog reset.

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- **GPIO**
  - Up to 80 GPIOs.
  - Support multiplexed functions.
  - Maximum toggle speed of 50 MHz
  - Most GPIOs are 5V tolerant.
- **Communication Interfaces**
  - 7x U(S)ART interfaces with maximum rate up to 4.5 Mbps.
    - 3x USART interfaces (support 1xISO7816, 1xIrDA, LIN).
    - 4x UART interfaces.
    - 3x SPI interfaces with speed up to 36 MHz, 2 of which support I2S.
  - 4x I2C interfaces (Master/Slave) with speed up to 1 MHz where slave mode can support dual address responses.
  - 1x USB2.0 Full speed Device interface
  - 1x CAN 2.0 A/B bus interface
  - 1x SDIO interface, supports SD/MMC format.
- **Analog Interfaces**
  - 3x 12-bit ADCs with 5Msps,
    - Configurable as 12/10/8/6-bit mode.
    - Sampling rate up to 9Msps in 6-bit mode.
    - Up to 18 external single-ended input channels, supports differential mode.
  - 2x 12-bit DACs with 1Msps
  - Supports external reference voltage.
  - Analog voltage operation from 1.8~3.6V (VDDA)
- **DMA controllers**
  - 2x high-speed DMA controllers each supporting 8 channels, with arbitrary configurable channel source and destination addresses.
- **RTC real-time clock**
  - Supports leap-year calendar, alarm events, periodic wakeup.
  - Supports internal and external clock calibration.
- **Timers and Counters**
  - 2x 16-bit advanced timers with maximum control precision of 6.9ns
    - Support input capture, complementary output, quadrature encoder input etc.
    - Each timer has 4 independent channels, 3 of which support 6-channel complementary PWM output.

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- 4x 16-bit general-purpose timers
    - Support input capture/output compare/PWM output.
    - Each with 4 independent channels.
- 2x 16-bit basic timers
- 1x 24-bit SysTick timer
- 1x 7-bit window watchdog (WWDG)
- 1x 12-bit independent watchdog (IWDG)

- **Programming Methods**
    - Supports SWD/JTAG debugging interface.
    - Supports UART, USB Bootloader
- **Security Features**
    - Built-in hardware acceleration engine for encryption algorithms
    - Supports AES, DES, SHA, MD5 algorithms.
    - Flash storage encryption, multi-user partition management (MMU)
    - TRNG true random number generator
    - CRC16/32 computation
    - Supports write protection (WRP), multiple levels of read protection (RDP) (L0/L1/L2)
    - Supports secure boot, encrypted program download, secure update.
    - Supports clock failure detection, anti-tamper detection.
- **96-bit UID and 128-bit UCID**
- **Operating Conditions**
    - Operating voltage range: 1.8V~3.6V
    - Operating temperature range: -40℃~105℃
    - ESD: ±4KV (HBM model), ±1KV (CDM model)
- **Packages**
    - LQFP48 (7mm x 7mm)
    - LQFP64 (10mm x 10mm)
    - LQFP100 (14mm x 14mm)
- **Ordering Information**

Reference	Part Number
N32G451xB	N32G451CBL7, N32G451RBL7
N32G451xC	N32G451CCL7, N32G451RCL7, N32G451VCL7
N32G451xE	N32G451CEL7, N32G451REL7, N32G451VEL7

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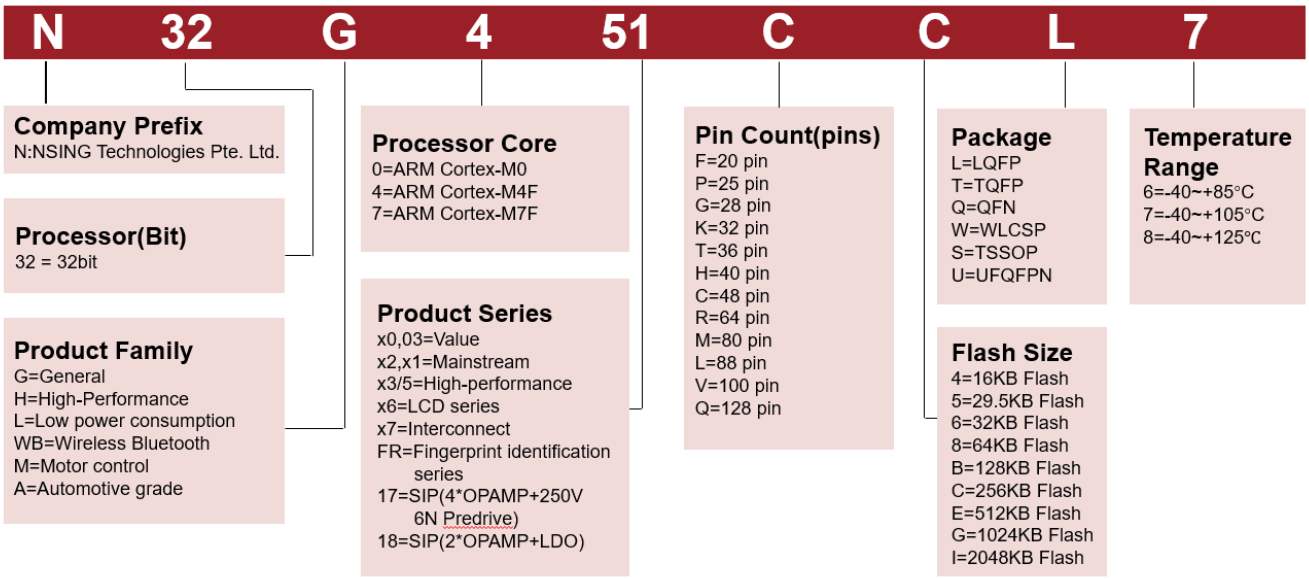
Naming Convention



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Product Configurations

Device		N32G451CB/CC/CE			N32G451RB/RC/RE			N32G451VC/VE	
Flash Capacity (KB)		128	256	512	128	256	512	256	512
SRAM Capacity (KB)		48	96	96	48	96	96	96	96
CPU Frequency		ARM Cortex-M4F @144MHz,180DMIPS							
Operating Environment		1.8~3.6V/-40~105℃							
Timers	General	4							
	Advanced	2							
	Basic	2							
Communication Interfaces	SPI	3							
	I2S	2							
	I2C	3			4				
	USART	3							
	UART	3			4				
	USB	1							
	CAN	1							
	SDIO	No(1)			1				
GPIO		37			51			80	
DMA		2							
DMA Channels		16 Channel							
12bit ADC		3			3			3	
ADC Channels		13 Channel			19 Channel			31 Channel	
12bit DAC		2							
DAC Channels		2 Channel							
Algorithm Support		DES/3DES、AES、 SHA1/SHA224/SHA256, MD5、CRC16/CRC32、TRNG							
Security Protection		Read/Write Protection (RDP/WRP), Storage Encryption, Partition Protection, Secure Boot							
Package		LQFP48			LQFP64			LQFP100	

Note: (1) SDIO is not supported

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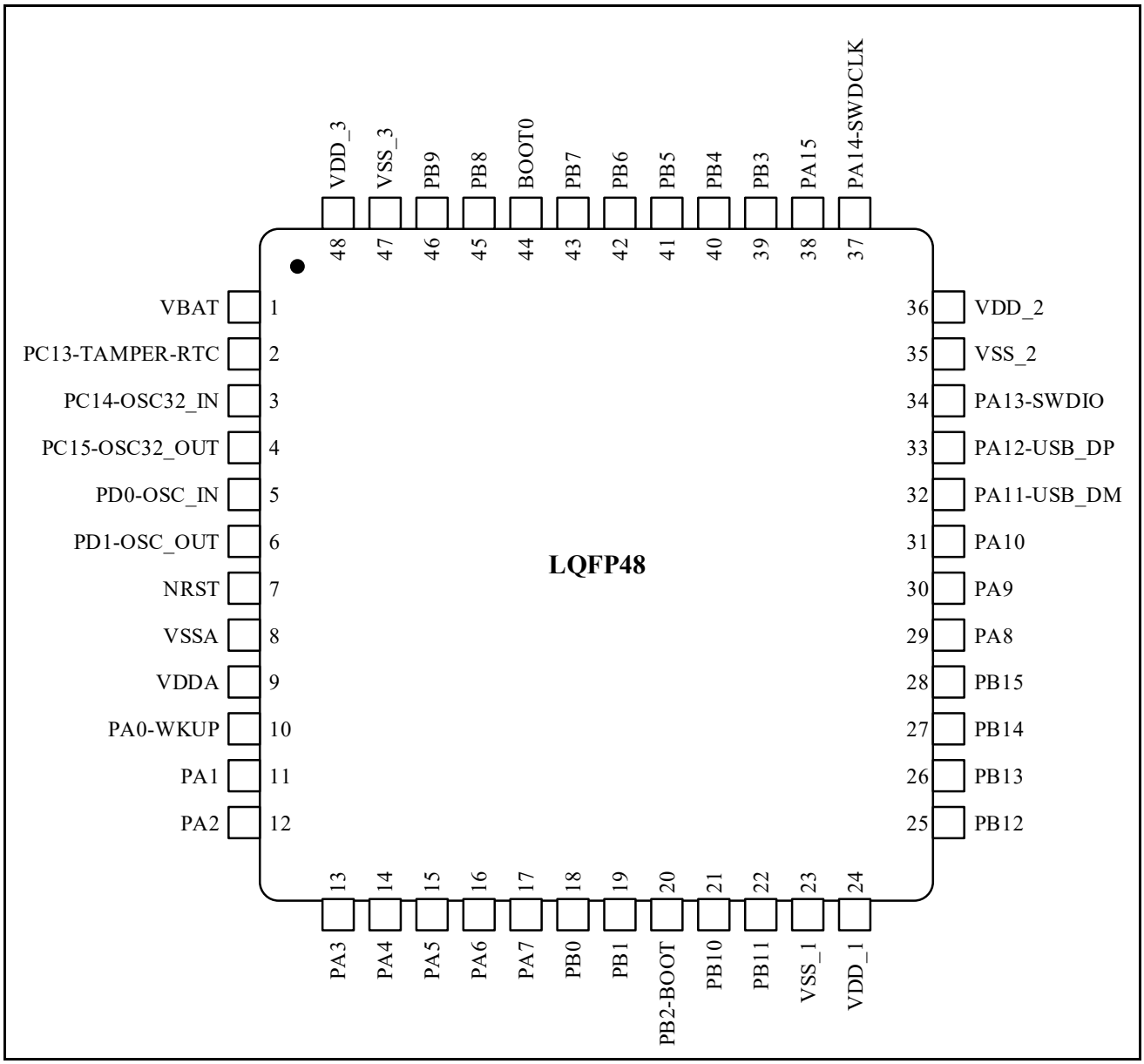
Packages

LQFP48 Package

LQFP48 Pin Assignment



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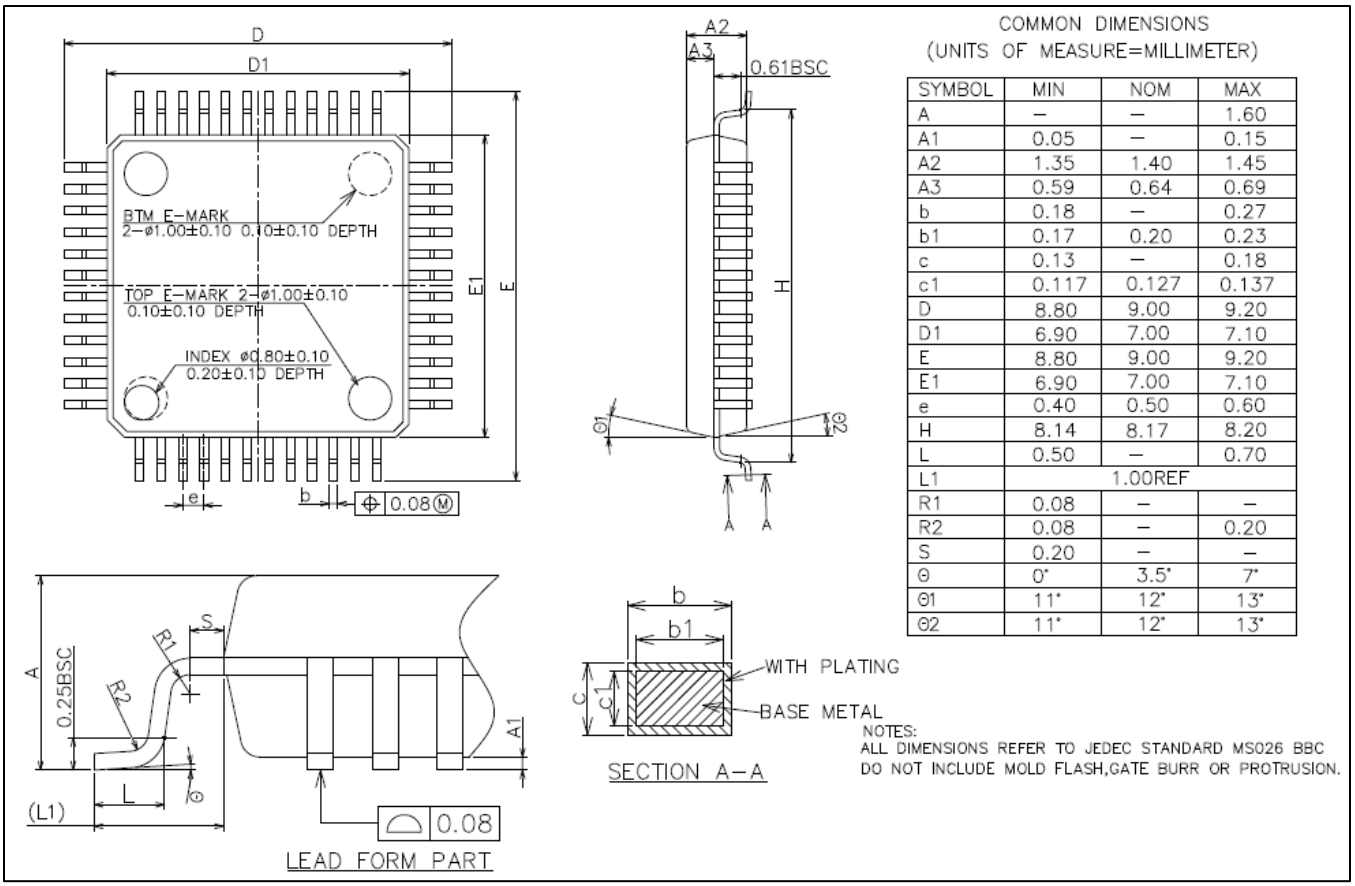
LQFP48 Package Dimensions



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	–	–	1.60
A1	0.05	–	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	–	0.27
b1	0.17	0.20	0.23
c	0.13	–	0.18
c1	0.117	0.127	0.137
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
e	0.40	0.50	0.60
H	8.14	8.17	8.20
L	0.50	–	0.70
L1		1.00REF	
R1	0.08	–	–
R2	0.08	–	0.20
S	0.20	–	–
θ	0°	3.5°	7°
θ1	11°	12°	13°
θ2	11°	12°	13°

NOTES:
ALL DIMENSIONS REFER TO JEDEC STANDARD MS026 BBC
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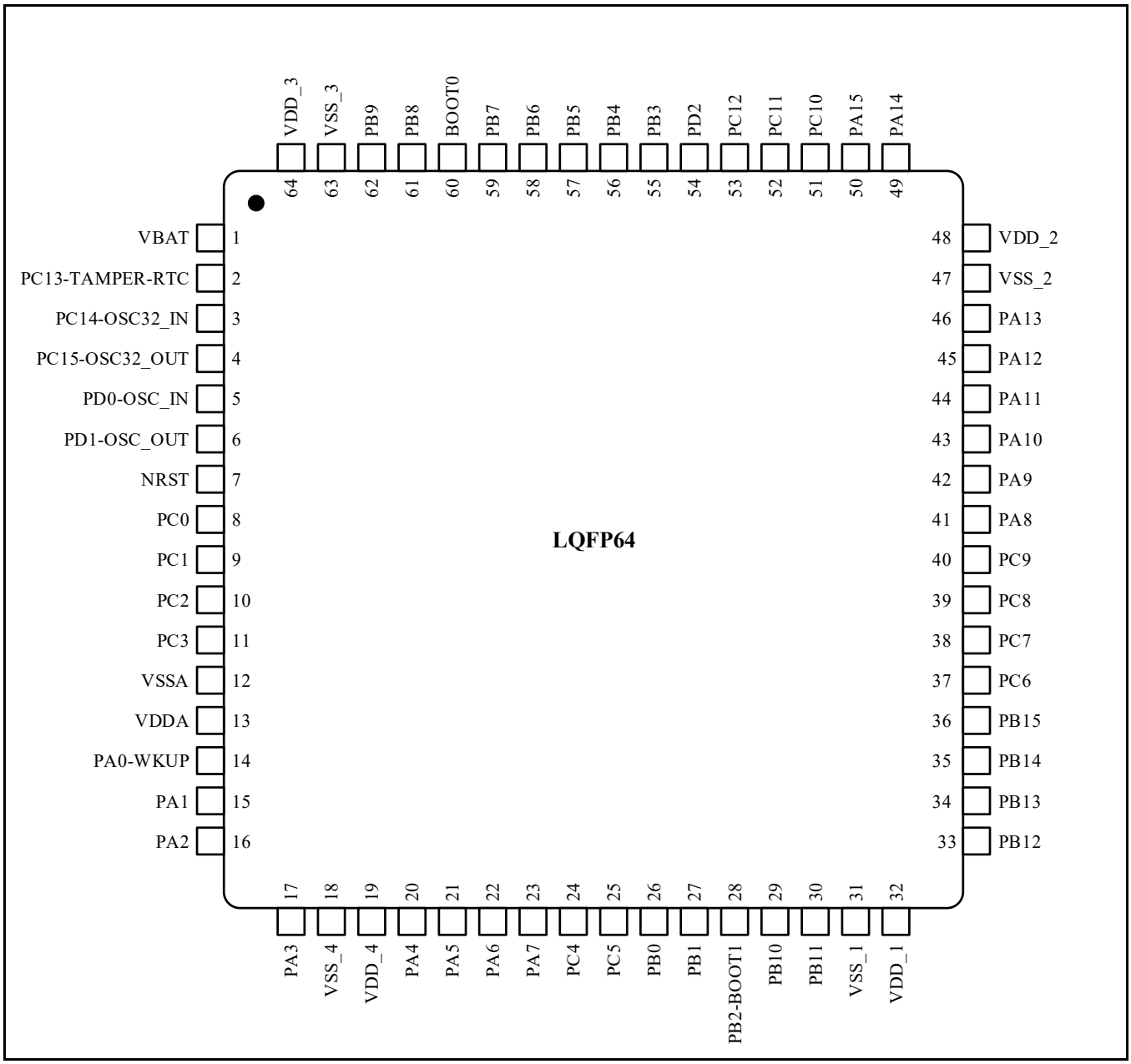
LQFP64 Package

LQFP64 Pin Assignment



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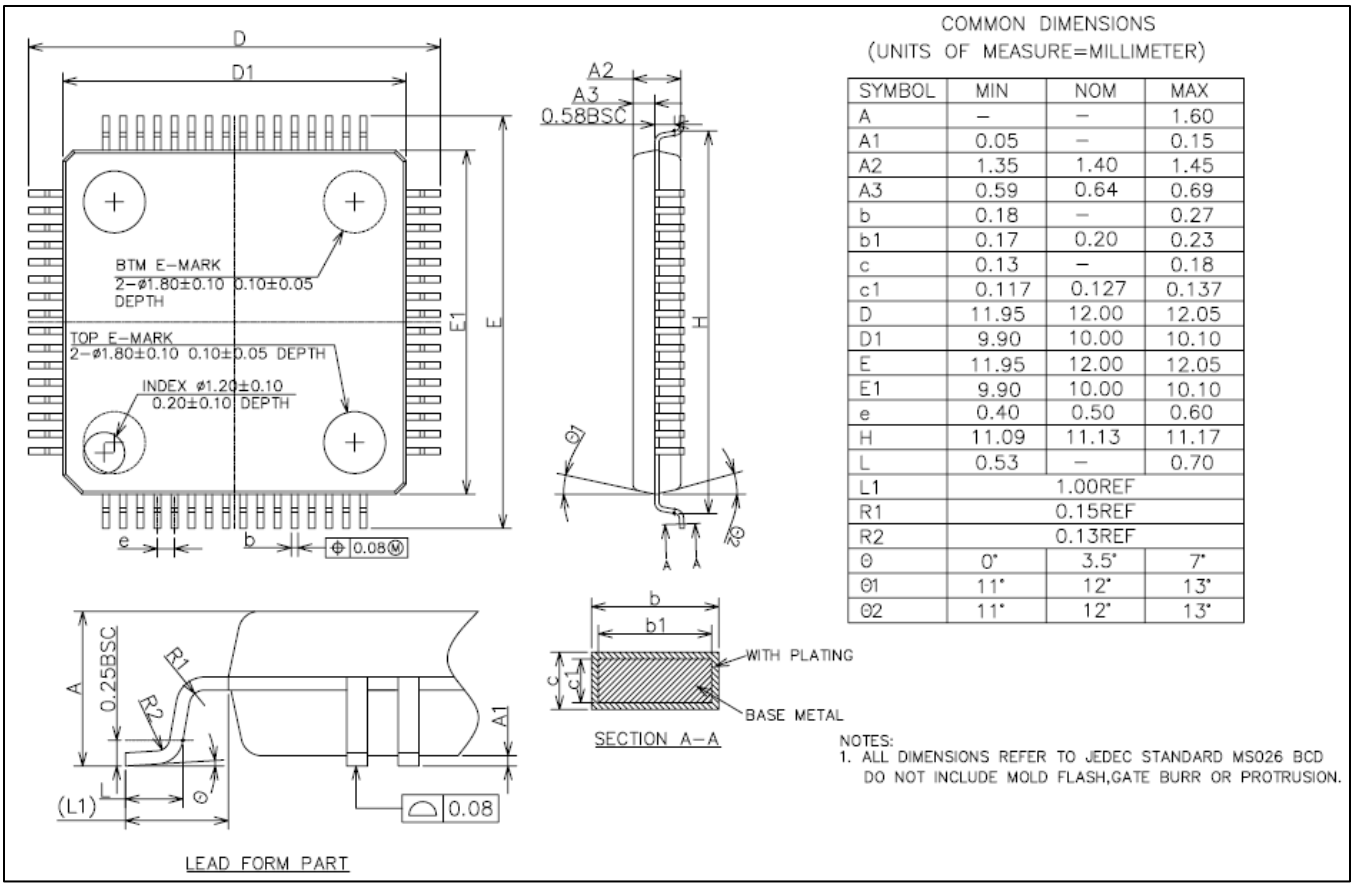
LQFP64 Package Dimensions



COMMON DIMENSIONS
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SYMBOL	MIN	NOM	MAX
A	–	–	1.60
A1	0.05	–	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	–	0.27
b1	0.17	0.20	0.23
c	0.13	–	0.18
c1	0.117	0.127	0.137
D	11.95	12.00	12.05
D1	9.90	10.00	10.10
E	11.95	12.00	12.05
E1	9.90	10.00	10.10
e	0.40	0.50	0.60
H	11.09	11.13	11.17
L	0.53	–	0.70
L1	1.00REF		
R1	0.15REF		
R2	0.13REF		
θ	0°	3.5°	7°
θ1	11°	12°	13°
θ2	11°	12°	13°

NOTES:
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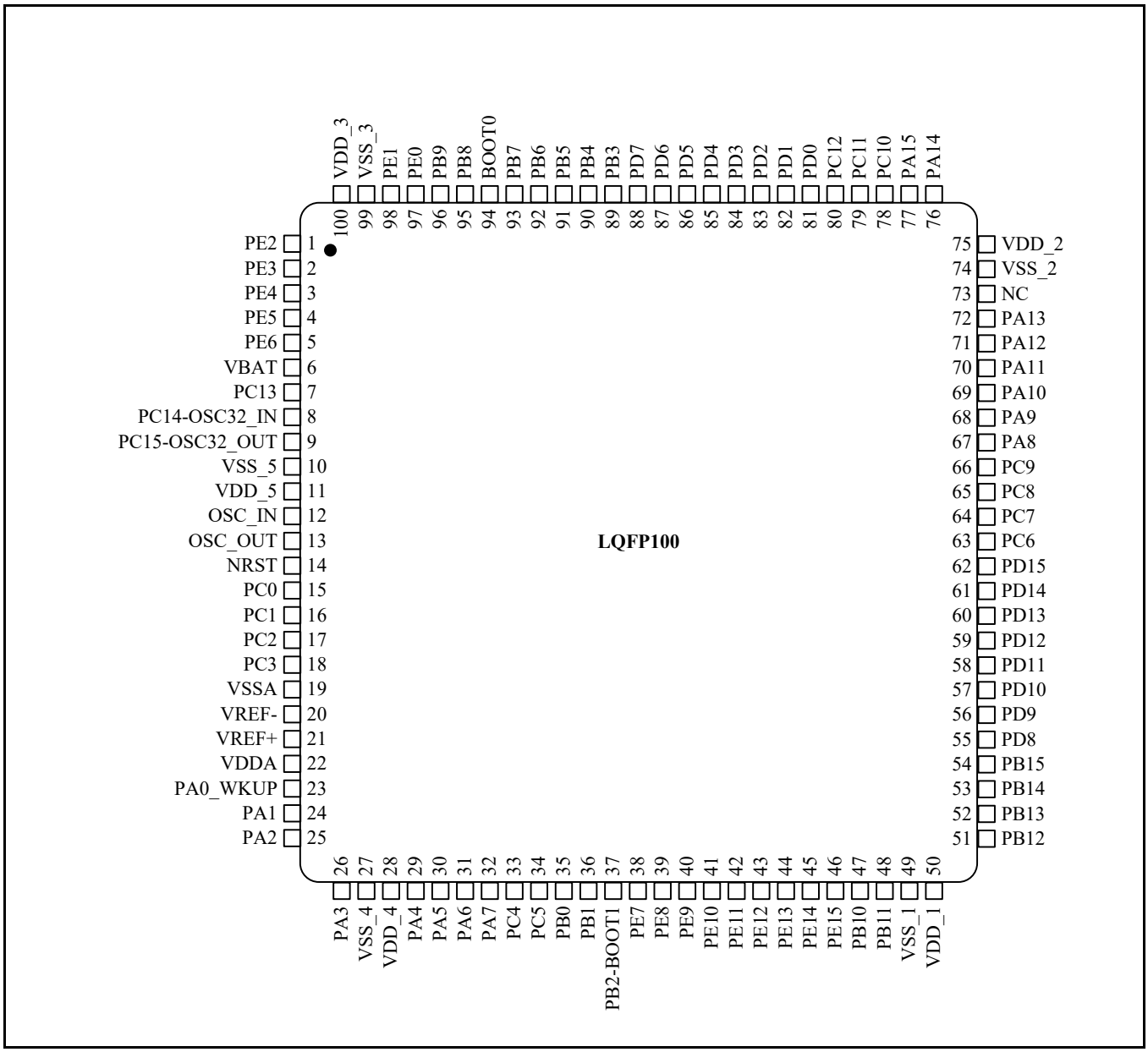
LQFP100 Package

LQFP100 Pin Assignment



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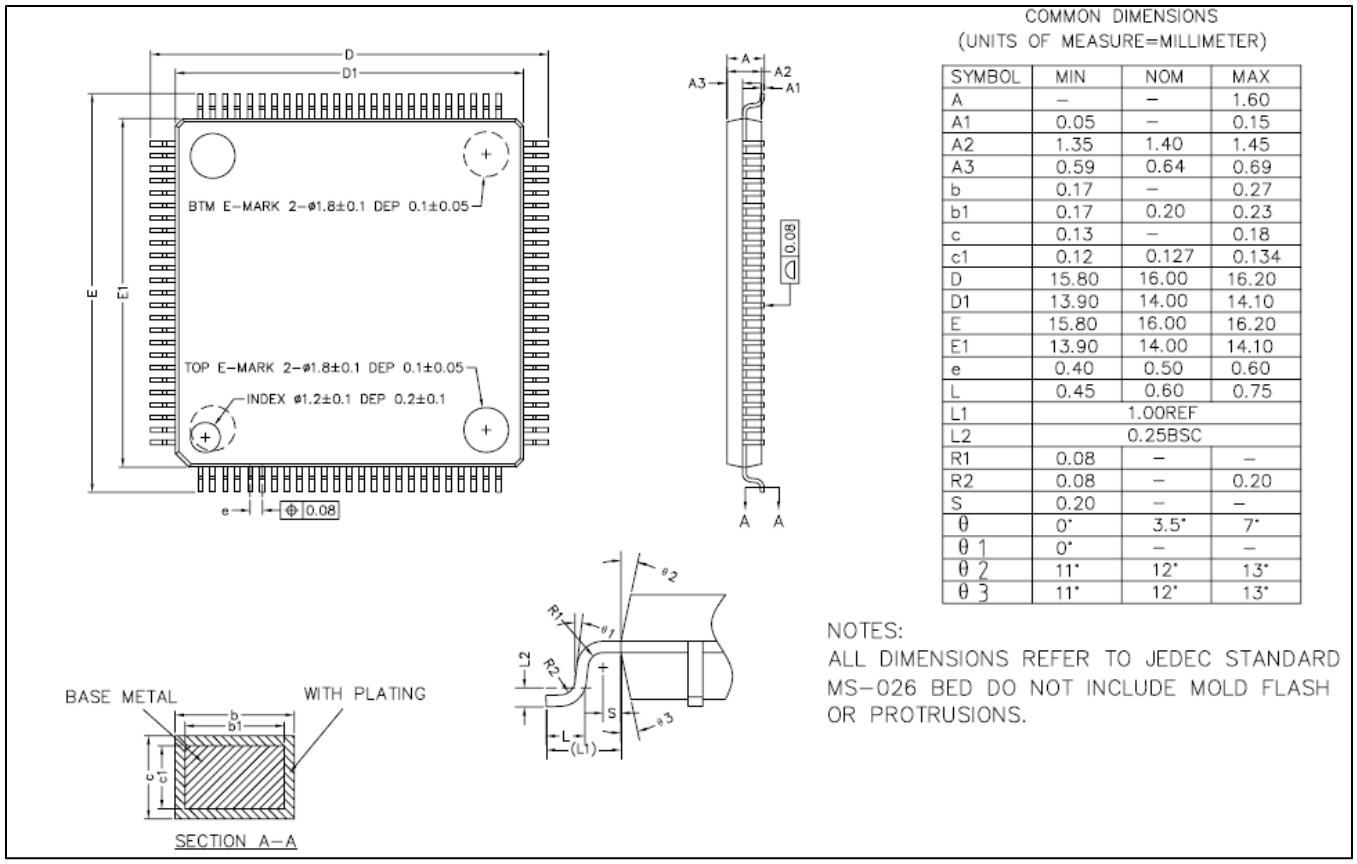
LQFP100 Package Dimensions



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

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A	–	–	1.60
A1	0.05	–	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.17	–	0.27
b1	0.17	0.20	0.23
c	0.13	–	0.18
c1	0.12	0.127	0.134
D	15.80	16.00	16.20
D1	13.90	14.00	14.10
E	15.80	16.00	16.20
E1	13.90	14.00	14.10
e	0.40	0.50	0.60
L	0.45	0.60	0.75
L1	1.00REF		
L2	0.25BSC		
R1	0.08	–	–
R2	0.08	–	0.20
S	0.20	–	–
θ	0°	3.5°	7°
θ1	0°	–	–
θ2	11°	12°	13°
θ3	11°	12°	13°

NOTES:
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Version History

Version	Date	Changes
V1.0.0	2023.5.30	Initial release
V1.0.1	2024.3.28	Error correction

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