N32G032 Series

Errata Sheet

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Contents

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1 Errata List

Table 1-1 Overview of Errata

	Errata Link		Chip Version		
			Version A	Version B	Version C
Ch 2:Power Conctol (PWR)	2.1: Power on after power off		●	●	-
Ch 3: Reset And Clock Control (RCC)	3.1: When running the program, the LSI has deviation		●	●	●
	3.2: LSE is affected by toggling of adjacent pins		●	●	●
	3.3: Abnormal function after PLL division value is reset		●	-	-
	3.4: HSI output jitter		●	-	-
	3.5: LSE has difficulty starting oscillation at high temperatures of 105°C		●	-	-
	3.6: LSE power-up/down related issue		●	●	●
	3.7: HSE instability causes chips to run off		●	●	●
Ch 4: GPIO And AFIO	4.1: GPIO analog function		●	●	●
	4.2: IO reverse current		●	●	●
Ch 5: Analog/Digital Conversion (ADC)	5.1: When the injection channel is triggered, the regular channel is also triggered		●	●	●
	5.2: ADC injected channel conversion		●	●	-
	5.3: ADC input noise		●	●	-
Ch 6: Operational Amplifier (OPAMP)	6.1: The output impedance of OPAMP is higher than expected		●	-	-
Ch 7: Serial Peripheral Interface (SPI)	7.1: SPI	7.1.1: SPI baud rate setting when CRC is enabled	●	●	●
		7.1.2: checking slave mode CRC	●	●	●
		7.1.3: When the power supply voltage is 1.8V~2.0V, the SPI data rate may not reach 12Mbps	●	●	●
	7.2: I^2S	7.2.1: PCM long frame mode	●	●	●
		7.2.2: No MCLK output in I^2S master mode	●	●	●
Ch 8: I^2C Interface	8.1: Handing software event before current byte is transferring		●	●	●
	8.2: Attentions when reading a single byte at time		●	●	●
	8.3: Using DMA concurrently with other peripherals		●	●	-
Ch 9: Universal Synchronous Asynchronous Receiver (USART)	9.1: Parity error flag		●	●	●
	9.2: RTS hardware flow control		●	●	●
Ch 10: Timer (TIM)	10.1: TIM repetitive capture detection		●	●	●
	10.2: ADTIM and GPTIM cannot generate compare events under certain circumstances		●	●	●
Ch 11: Low Power Timer (LPTIM)	11.1: LPTIM COUNTMODE counting		●	●	-
	11.2: LPTIM triggering only "compare match interrupt"		●	-	-
	11.3: LPTIM ARROK and CMPOK interrupt sources limited functionality		●	-	-
Ch 12: Real Time Clock (RTC)	12.1: RTC timing		●	●	-
	12.2: RTC subsecond match		●	●	●
	12.3: RTC second match		●	●	●
	12.4: The RTC calendar function prohibits multiple initializations within 1 second		●	●	●
	12.5: RTC incorrectly triggers TISOVF flag		●	●	●
	12.6: RTC_DATA register locked		●	●	●

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Ch 13: Controller Area Network (CAN)	13.1: CAN Active Error	•	•	•

Notes:

(1) ●: problem present

(2) -: fixed

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2. Power Control (PWR)

2.1 Power On after Power Off

Description

When the power supply voltage drops to around 1.6V (not completely power down) and then returns to the normal operating voltage, there may be a possibility of unsuccessful power-up.

Workaround

When the MCU is powered off, it is necessary to ensure that the chip's VDD voltage drops to below 100mV, and then powered on to the normal operating voltage.

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3. Reset and Clock Control (RCC)

3.1When Running the Program, the LSI Has Deviation

Description

When running the program, the LSI has high jitter, the average frequency (1S time) is 30K±1KHz, and the instantaneous frequency is 20K~45KHz.

Workaround

For precise timing, it is recommended that customers use LSE instead of LSI.

3.2 LSE Is Affected by Toggling of Adjacent Pins

Description

LSE is affected by toggling of adjacent pins.

Workaround

Avoid toggling of adjacent pins of LSE.

3.3 Abnormal Function after PLL Division Value Is Reset

Description

Abnormal function after PLL division value is reset.

Workaround

After a system reset, configure the PLL output division value to 01 first, and then configure it to 00 to reset the function.

3.4 HSI Output Jitter

Description

When the frequency of periodic jitter on VDDD is 2MHz, the frequency deviation of HSI is approximately ±8%.

Workaround

None.

3.5 LSE Has Difficulty Starting Oscillation at High Temperatures of 105°C

Description

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The LSE oscillator has difficulty starting oscillation at high temperature of 105°C.

Workaround

None.

3.6 LSE Power-Up/Down Related Issue

Description

If LSE (Low-Speed External) oscillator is enabled ，When the power supply voltage drops to around 1.6V (not completely power down)and then returns to the normal operating voltage, there may be a possibility of unsuccessful power-up.

Workaround

If LSE has been enabled， when the MCU is powered down, it is necessary to ensure that the chip's VDD voltage drops to below 100mV before powering up to the normal operating voltage.

3.7 HSE Instability Causes Chips to Run Off

Description

When HSE is enabled, running the code directly after the HSE Ready flag is set, then the system program may run off due to the unstable HSE clock.

Workaround

After enabling HSE, add a software delay of about 10 milliseconds, then wait for the HSE Ready flag to be set before running the code.

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4. GPIO and AFIO

4.1 GPIO Analog Function

Description

When the 4 GPIOs(PA1/PA2/PA3/PA4) are in the high-level output state, and they switch to the analog function, there will be a transient output voltage drop of about 30mv during the switching process.

Workaround

Avoid the above usage methods.

4.2 IO Reverse Current

Description

If the IO that does not support failsafe function is powered on before V_{DD}, an exception may occur at this time, and the external pin reset cannot return to normal after the exception.

Workaround

It is recommended that customers use the power-on of V_{DD} prior to the power-on of IO.

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5. Analog/Digital Conversion (ADC)

5.1 When the Injection Channel Is Triggered, the Regular Channel Is also Triggered

Description

When performing ADC continuous conversion with external triggering disabled for regular channels, and an injection channel conversion is triggered by software or hardware, the regular channels may be triggered for conversion, and the corresponding status bits for the regular channels will be set.

Workaround

Ignore the flags and data generated by the regular channels.

5.2 ADC Injected Channel Conversion

Description

Injecting channel conversion is triggered at the moment when regular channel conversion is completed, and the injected channel conversion cannot be completed.

Workaround

None.

5.3 ADC Input Noise

Description

When there's high-frequency noise at around 10MHz in the ADC input signal, the ADC may exhibit anomalies approaching the saturation value of 4096.

Workaround

None.

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6. Operational Amplifier (OPAMP)

6.1 Output Impedance of OPAMP Is Higher than Expected

Description

The output impedance of the operational amplifier (OPAMP) is higher than expected.

Workaround

None.

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7. Serial Peripheral Interface (SPI)

7.1SPI Interface

7.1.1 SPI Baud Rate Setting When CRC Is Enabled

Description

When the CRC function is turned on, depending on the operating environment of the SPI interface, such as board-level delay, ambient temperature, etc. CRC errors may occur for both the SPI master and slave.

In an ideal laboratory environment at room temperature, when the SPI clock is greater than 12MHz, an abnormal CRC check error may occur.

Workaround

When the CRC function is enabled, it is recommended to configure the CRC clock frequency to not exceed 12MHz.

When a CRC exception error occurs, it is recommended to reduce the configured SPI baud rate.

7.1.2 Checking Slave Mode CRC

Description

In SPI operating in slave mode with CRC validation enabled, even if the NSS pin is at a high level, CRC calculation continues if the SPI receives a clock signal.

Workaround

Before using the CRC, clear the CRC data register so that the CRC check of the master and slave devices can be synchronized.

The steps to clear the CRC data register are as follows:

1. SPI enable bit reset (set 0)
2. CRC check bit reset (set 0)
3. CRC check bit set (set 1)
4. SPI enable bit set (set 1)

7.1.3 When the Power Supply Voltage Is 1.8V~2.0V, the SPI Data Rate May Not Reach 12Mbps

Description

When the power supply voltage is 1.8V~2.0V, the SPI data rate may not reach 12Mbps depending on

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the IO and board-level wiring delay characteristics.

The highest communication rate measured in the ideal environment of the laboratory is 12Mbps:

Workaround

If customers have SPI communication requirements at high or low temperatures with 1.8V power supply, it is recommended to contact the technical support of NSING TECHNOLOGIES PTE. LTD .

7.2I²S Interface

7.2.1 PCM Long Frame Mode

Description

When I²S operates in master mode, PCM long frame mode, and the data format is "32bit" or "16bit extended to 32bit", the WS signal is one cycle per 16bit instead of 32bit.

Workaround

When I²S is the master mode and the long frame mode must be used, the 16bit data mode should be used.

7.2.2 No MCLK Output in I²S Master Mode

Description

When the I²S is operating in master mode with the MCLK enable option turned on, and I²S transmission starts, there is no output of the MCLK signal.

Resolution

None.

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8. I²C Interface

8.1 Handing Software Event before Current Byte Transferring

Description

In the occurrence of events EV7, EV7_1, EV6_1, EV6, EV2, EV8, and EV3, it is essential to handle the events before the current byte transfer to prevent issues such as reading an extra byte, obtaining duplicate data, or losing data. If the software fails to read the N-1th byte before the stop signal generation, the data in the shift register for the Nth byte may become corrupted (shifted one bit to the left).

Workaround

- When transferring more than one byte in I²C, consider using DMA if possible.
- When using I²C interrupts, set the interrupt priority to the highest priority in the application.
- When the read data reaches the N-1th byte:
  1. Check that BSF (Byte Shift Flag) is set to 1.
  2. Configure SCL as a GPIO open-drain output and set it to 0.
  3. Set STOPGEN to 1.
  4. Read the N-1th byte.
  5. Configure SCL back to I²C multiplex open-drain output mode.
  6. Read the last byte.

8.2 Attentions When Reading a Single Byte at Time

Description

In the master read mode, errors in reading data may occur when reading single-byte.

Workaround

Single byte read:

1. Upon receiving ADDRF
2. Set ACKEN 0
3. Clear ADDRF bit (by reading STS1 and then STS2)
4. Set STOPGEN to 1
5. Read one byte of data

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8.3 Using DMA Concurrently with Other Peripherals

Description

When using DMA for I^2C communication, concurrent DMA usage by other peripherals may result in abnormal I^2C communication.

Workaround

Two workarounds are available:

- Disable DMA for other peripherals while using DMA for I^2C communication.
- Set the DMALAST bit of I2C_CTRL2 when receiving the penultimate byte.

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9. Universal Synchronous Asynchronous Receiver Transmitter(USART)

9.1 Parity Error Flag

Description

During the reception of a byte of data, if a parity error is detected before receiving the stop bit, the parity error flag is set. During this period, the parity error flag cannot be cleared through software (by reading the status register and then reading the data register). If the parity error interrupt is enabled, it may repeatedly enter the parity error interrupt handling function.

Workaround

When the read data buffer flag is set, clear the parity error flag after receiving the data. If the parity error interrupt is enabled, to avoid multiple enteries into the interrupt handling function, disable the parity error interrupt upon the first entry into the parity error interrupt, and then re-enable the parity error interrupt after receiving the data.

9.2 RTS Hardware Flow Control

Description

When the RTS (Request to Send) hardware flow control is enable, and a USART receives a frame of data, the RTS signal is automatically asserted (pulled high) upon receiving the first byte of data. If this first byte is not promptly read from the data register, upon receiving the next byte of data, the RTS signal is de-asserted (pulled low) again, and the USART waits for the reception of the next frame of data.

Workaround

Before the next new data is received, the data is read out from the data register in time.

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10. Timer (TIM)

10.1 Timer Repetitive Capture Detection

Description

When reading the capture data register data (normally, reading the data register will clear the capture flag), if an external trigger capture occurs, even if the previous capture has been correctly read and the new capture data has been accurately sent to the register, the repeat capture flag is still detected. The system is critical for overcapture, but no capture data is lost.

Workaround

None.

10.2 ADTIM and GPTIM Cannot Generate Compare Events under Certain Circumstances

Description

In edge-aligned mode, and up-counting PWM1 mode, when CCDATx shadow register value is greater than or equal to AR value in current PWM cycle, and if the CCDATx shadow register value cycle is equal to 0 in the next PWM cycle. No compare event will occur when the count value of the PWM period counter is equal to the value of the CCDATx shadow register is 0.

Workaround

If it is not required that "the compare event is generated at the time when the count value = the shadow register of the comparison value =0", the compare event can be generated through another channel.

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11 Low Power Timer (LPTIM)

11.1 LPTIM COUNTMODE Counting

Description

When configuring the LPTIM with the clock source set to internal clock source, and setting the counter mode as the counter increments based on each valid clock pulse on LPTIM external Input1, the count value CNT can only count up to ARR-1, while other configurations can count up to ARR.

Workaround

None.

11.2 LPTIM Can Only Trigger "Compare Match Interrupt"

Description

LPTIM can only trigger "Compare Match Interrupt".

Workaround

None.

11.3 LPTIM ARROK and CMPOK Interrupt Sources limited Functionality

Description

ARROK and CMPOK interrupt sources have limited functionality: they can only generate interrupts when PRE_LOAD_MODE = 1.

Workaround

When PRE_LOAD_MODE = 0, it is recommended to configure the ARR and CMP registers before enabling LPTIM.

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12 Real Time Clock (RTC)

12.1 RTC Timing

Description

While the RTC is active, if an NRST (external reset) occurs, the reset period will cause the RTC to stop counting.

Workaround

None.

12.2 RTC Subsecond Match

Description

When using the RTC programmable alarm clock, disable the matching of date, hour, minute, and second mode, only enable the matching of the sub-seconds mode. This means that an alarm interrupt is generated when the sub-seconds match every second. However, the alarm interrupt is not generated at the first sub-seconds match after enabling RTC alarm, and the alarm interrupt is generated for each sub-second match after that.

Workaround

None.

12.3 RTC Second Match

Description

When the RTC alarm is configured in second match mode, the chip enters SLEEP mode. If an alarm interrupt wakes up the chip from SLEEP mode and the interrupt handling function is executed (only clearing the interrupt flag), and the chip immediately enters STOP mode, the next alarm interrupt cannot wake up the chip from STOP mode.

Workaround

Before configring the RTC time, it is necessary to enter the RTC initialization mode. Before entering this mode, ensure that the sub-second register value is less than the synchronous prescaler value and not equal to 0.

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12.4 The RTC Calendar Function Prohibits Multiple Initializations within 1 Second

Description

Multiple initializations of the RTC calendar function within 1 second will result in the inability to generate RTC alarm interrupts.

Workaround

The interval between two initializations of the RTC calendar function should be more than 1 second.

12.5 RTC Incorrectly Triggers TISOVF Flag

Description

When the system wakes up from STANDBY mode or reset by IWDG timeout, TISOVF flag in RTC may be set incorrectly.

Workaround

Before entering STANDBY mode or when the system is reset by IWDG timeout, when the SHOPF flag is 0, configure RTC_SCTRL.SUBF[14:0] register once, and SHOPF flag will set to 1. When SHOPF flag is 0 again, it should configure RTC_SCTRL.SUBF[14:0] register for the second time. This will solve the issue.

Note: that NRST cannot be triggered during above process.

12.6 RTC_DATE Register Locked

Description

- Before the system software reset, if the RTC_DATE register is not read after reading the RTC_SUBS or RTC_TSH shadow register, and after the system software reset, if the RTC is initialized without configuring or reading the RTC_DATE register, then the RTC_DATE register will revert to its default value;
- When reading the calendar, after reading the RTC_SUBS or RTC_TSH shadow register, the value of the RTC_DATE register remains unchanged.

Workaround

- Read the RTC_DATE register before initializing the RTC;
- After reading the RTC_SUBS or RTC_TSH shadow register, then read the RTC_DATE register.

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13 Controller Area Network (CAN)

13.1 CAN Active Error

Description

In normal mode, if the CAN bit is hard synchronized and the bus rate deviation of other nodes on the bus is too large (approaching or exceeding the synchronization segment), the CAN module is prone to report active errors.

Workaround

None.

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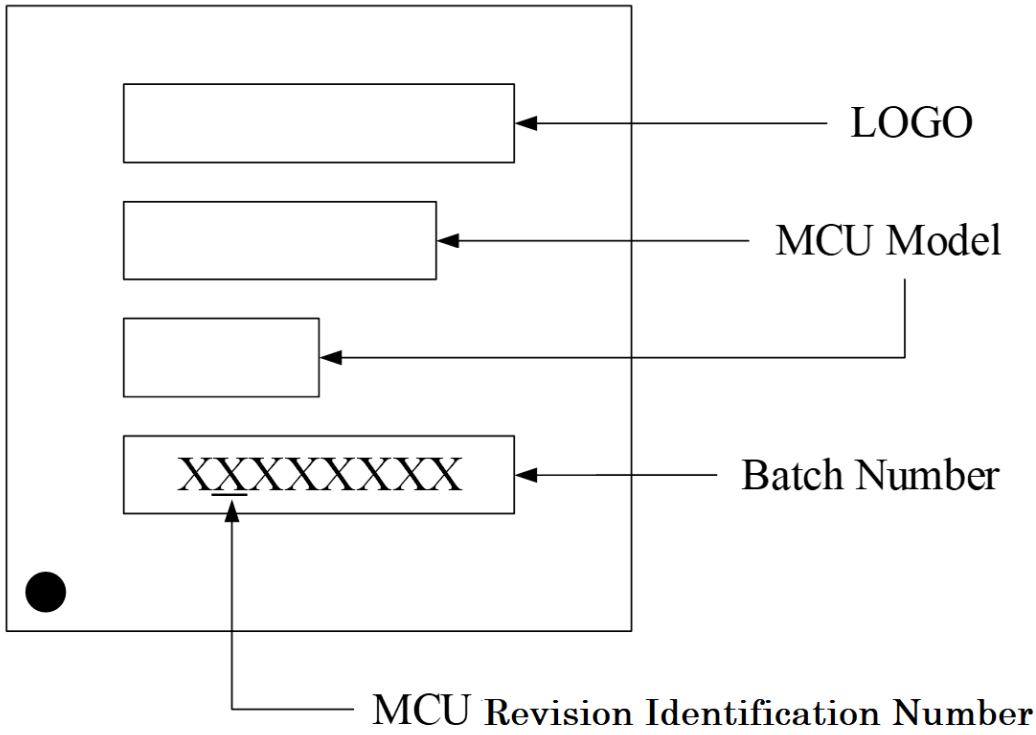
14 Chip marking and Revision Description



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15 Version History

Version	Date	Changes
V1.0.0	2022.10.9	Initial release
V1.1.0	2023.7.31	1) Added Section 7.1.3 2) Changed the SPI clock in Section 7.1.1 from not exceeding 14MHz to not exceeding 12MHzd 3) Added Section 3.6 and 3.7 4) Added Section 13.1 5) Added Section 12.5 and 12.6

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