N32G032x6/x8 Product Brief

The N32G032 series adopts a 32-bit ARM Cortex-M0 core, with a maximum operating frequency of 48MHz, integrated up to 64KB Flash, 16KB SRAM, 1x12-bit 1Msps ADC, 1xOPAMP, 3xCOMP, integrated multiple U(S)ART, I²C, SPI, CAN communication interfaces, and a built-in hardware-accelerated encryption engine.

Key Features

- CPU core
  - 32-bit ARM Cortex-M0 core, supporting Single-cycle hardware multiply instruction
  - Frequency up to 48MHz
- Memories
  - Up to 64Kbyte of embedded Flash memory with ECC
    1. Supports encryption, multi-user partition, data protection
    2. 100,000 erase/write cycles, and 10 years data retention
  - Up to 16KByte of SRAM with hardware parity check
- Low power management
  - STOP mode: RTC operate, 16KByte SRAM retained, CPU register retained, all IOs retained, supports fast wake up with 20us
  - Power down mode: supports wakeup from 3 IOs
- Clock
  - HSE: 4MHz~20MHz high-speed external crystal oscillator
  - LSE: 32.768KHz low-speed external crystal oscillator
  - HSI: High-speed internal RC 8MHz
  - LSI: Low-speed internal RC 30KHz
  - Built-in high-speed PLL
  - Supports 2 clock outputs, which can be configured as system clock, HSI, HSE, LSI, LSE, and PLL clock output that be divided.
- Reset
  - Supports power-on, power-down, and external pin reset
  - Supports watchdog reset
- GPIOs

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- Up to 56 GPIOs
- Support multiplexed functions

- Communication interfaces
  - 6x U(S)ART interfaces
    1. 2x USART interfaces (support 1xISO7816, 1xIrDA, LIN)
    2. 4x UART interfaces
    3. The rate is up to 3 Mbps
    4. Support waking up from STOP mode
  - 3x SPI interfaces, the rate is up to 12 MHz, one of which supports I^2S communication
  - 2x I^2C interfaces, the rate is up to 1 MHz, which can be configured in master/slave mode and support dual address response in slave mode. Support dual-level communication, allowing selection normal level (signal level matches chip VDD) and low level (chip VDD 3.3V or 5V, signal level 1.8V).
  - 1x CAN 2.0A/B bus interface

- Analog interfaces
  - 1x 12bit 1Msps ADC, up to 16 external single-ended input channels
  - 1x operational amplifier with built-in up to 32 times programmable gain amplifier(PGA)
  - 3x high-speed analog comparators which built-in 64-level adjustable comparison reference

- DMA controller
  - 1x high-speed DMA controller
  - Each controller supports 8 channels
  - Channel source address and destination address can be configured arbitrarily

- RTC real-time clock
  - Supports leap year perpetual calendar, alarm event, periodic wake up, support internal and external clock calibration

- Beeper
  - 2x Beepers
  - Supports complementary output
  - The drive capacity up to 16mA

- Timers and counters
  - 2x 16bit advanced timers

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1. Support input capture, complementary output, quadrature encoding input
2. Each timer has 4 independent channels, with 3 channels support 6 pairs complementary PWM outputs

- 2x 16bit general-purpose timers
  1. Support input capture, output comparsion, and PWM output
  2. Each timer has 4 independent channels
- 1x 16bit basic timer
- 1x 16bit low power timer
- 1x 24bit SysTick timer
- 1x 7bit Window Watchdog (WWDG)
- 1x 12bit Independent watchdog (IWDG)

- Programming methods
  - Supports SWD online debugging interface
  - Supports UART Bootloader
- Hardware divider (HDIV) and square root(SQRT)
- Security features
  - Built-in hardware acceleration engine for cryptographic algorithm
  - Supports AES, SM4 algorithms
  - Flash memory encryption, multi-user partition Management Unit (MMU)
  - True random number generator(TRNG)
  - CRC16/32 calculation
  - Supports write protection(WRP), multiple read protection(RDP) levels (L0/L1/L2)
  - Supports external clock failure detection, tamper detection
- 96-bit UID and 128-bit UCID
- Operating conditions
  - Operating voltage range: 1.8V~5.5V
  - Operating temperature range: -40°C~105°C
  - ESD: ±4KV (HBM model), ±1KV (CDM model)
- Packages
  - UFQFPN20(3mm x 3mm)

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- TSSOP20(6.5mm x 4.4mm)
- QFN32(5mm x 5mm)
- LQFP32(7mm x 7mm)
- LQFP48(7mm x 7mm)
- LQFP64(10mm x 10mm)
- WLCSP25(2.128mm x 2.065mm)

- Ordering information

Reference	Part Number
N32G032x6	N32G032F6U7, N32G032F6S7,N32G032P6W7, N32G032K6L7, N32G032K6Q7
N32G032x8	N32G032F8S7, N32G032P8W7, N32G032K8L7, N32G032C8L7, N32G032R8L7

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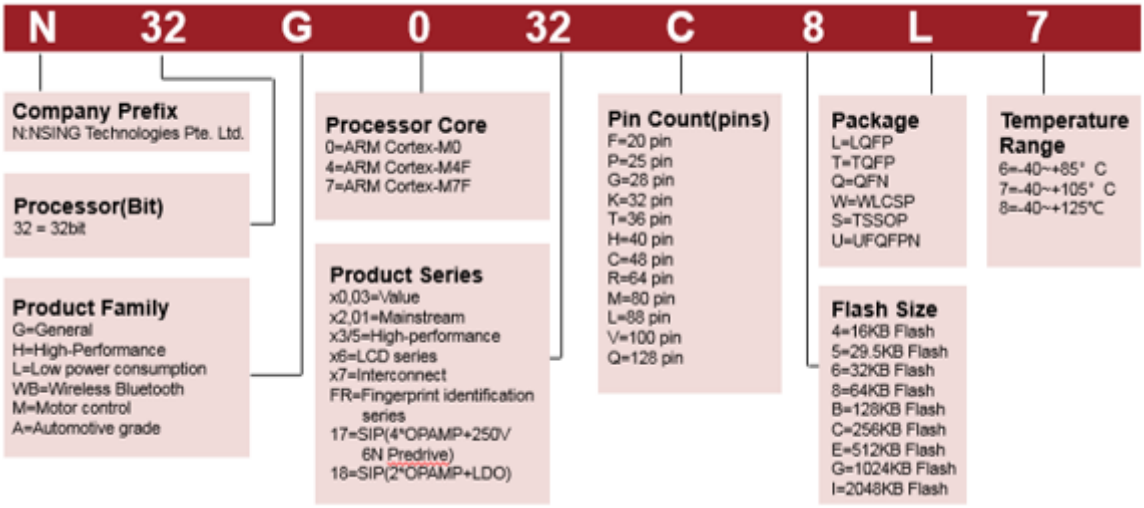
1 Naming Convention

Figure 1-1 N32G032 Series Part Number Information



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2 Product Configurations

Table 2-1 N32G032 Series Resource Configuration

Device		N32G032 F6U7	N32G032 F6/8S7	N32G032 P6/8W7	N32G032 K6Q7	N32G032 K6/8L7	N32G032 C8L7	N32G032 R8L7
Flash capacity (KB)		32	32/64	32/64	32	32/64	64	64
SRAM capacity (KB)		8	8/16	8/16	8	8/16	16	16
CPU frequency		ARM Cortex-M0 @48MHz						
Operating conditions		1.8~5.5V/-40~105℃						
Timers	General	2						
	Advanced	2						
	Basic	1						
	LPTIM	1						
	RTC	1						
Communication interfaces	SPI	1			2		3	3
	I^2S	1						
	I^2C	2						
	USART	2						
	UART	1		2				
	LPUART	2						
	CAN	1						
GPIO		16		21	28	26	40	56
DMA Number of channels		1x 8Channel						
12bit ADC Number of channels		1x 7Channel	1x 9Channel	1x 10Channel	1x 10Channel	1x 10Channel	1x 10Channel	1 16Channel
OPA/COMP		1/2	1/3	1/2	1/3	1/3	1/3	1/3
Beeper		2	1	2				
Algorithm support		AES, SM4, CRC16/CRC32, TRNG						
Security protection		Read and write protection (RDP/WRP), storage encryption, partition protection						
Packages		UFQFPN20	TSSOP20	WLCSP25	QFN32	LQFP32	LQFP48	LQFP64

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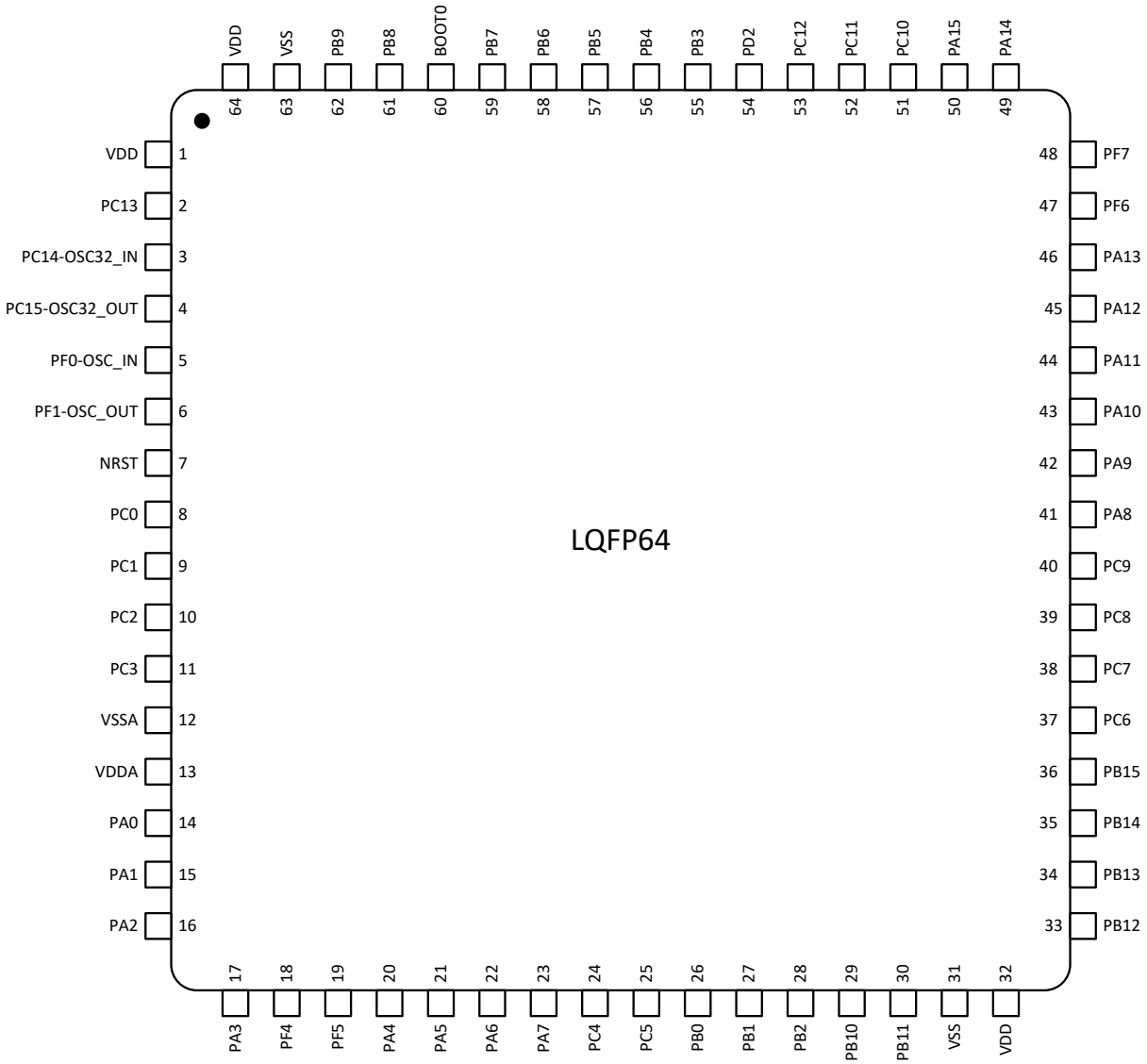
3 Packages

3.1 LQFP64 Package

3.1.1 LQFP64 Pin Assignment



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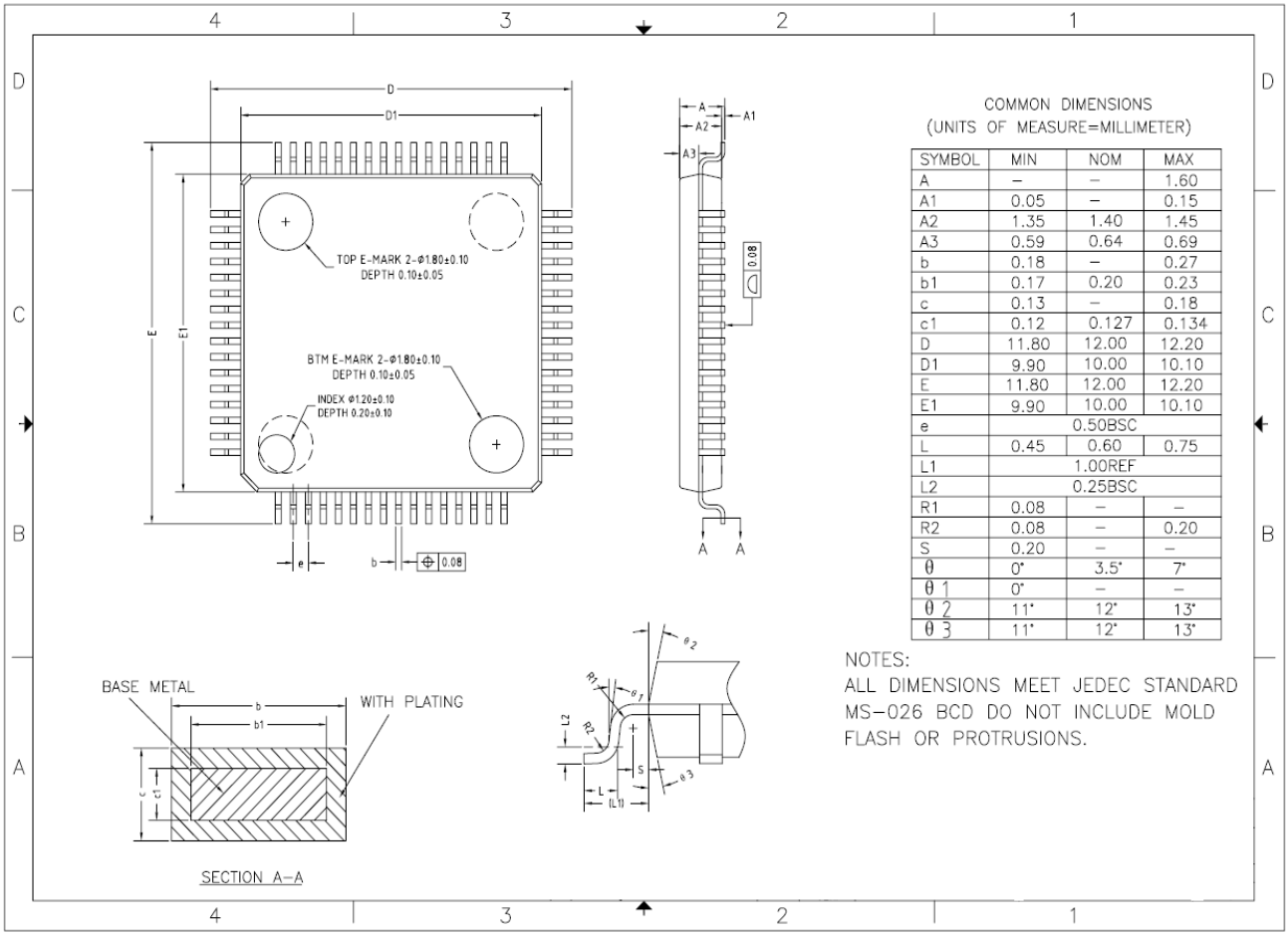
3.1.2 LQFP64(10mm x 10mm) Package Dimentsions



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	–	–	1.60
A1	0.05	–	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	–	0.27
b1	0.17	0.20	0.23
c	0.13	–	0.18
c1	0.12	0.127	0.134
D	11.80	12.00	12.20
D1	9.90	10.00	10.10
E	11.80	12.00	12.20
E1	9.90	10.00	10.10
e		0.50BSC	
L	0.45	0.60	0.75
L1		1.00REF	
L2		0.25BSC	
R1	0.08	–	–
R2	0.08	–	0.20
S	0.20	–	–
θ	0°	3.5°	7°
θ 1	0°	–	–
θ 2	11°	12°	13°
θ 3	11°	12°	13°

NOTES:
ALL DIMENSIONS MEET JEDEC STANDARD MS-026 BCD DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.

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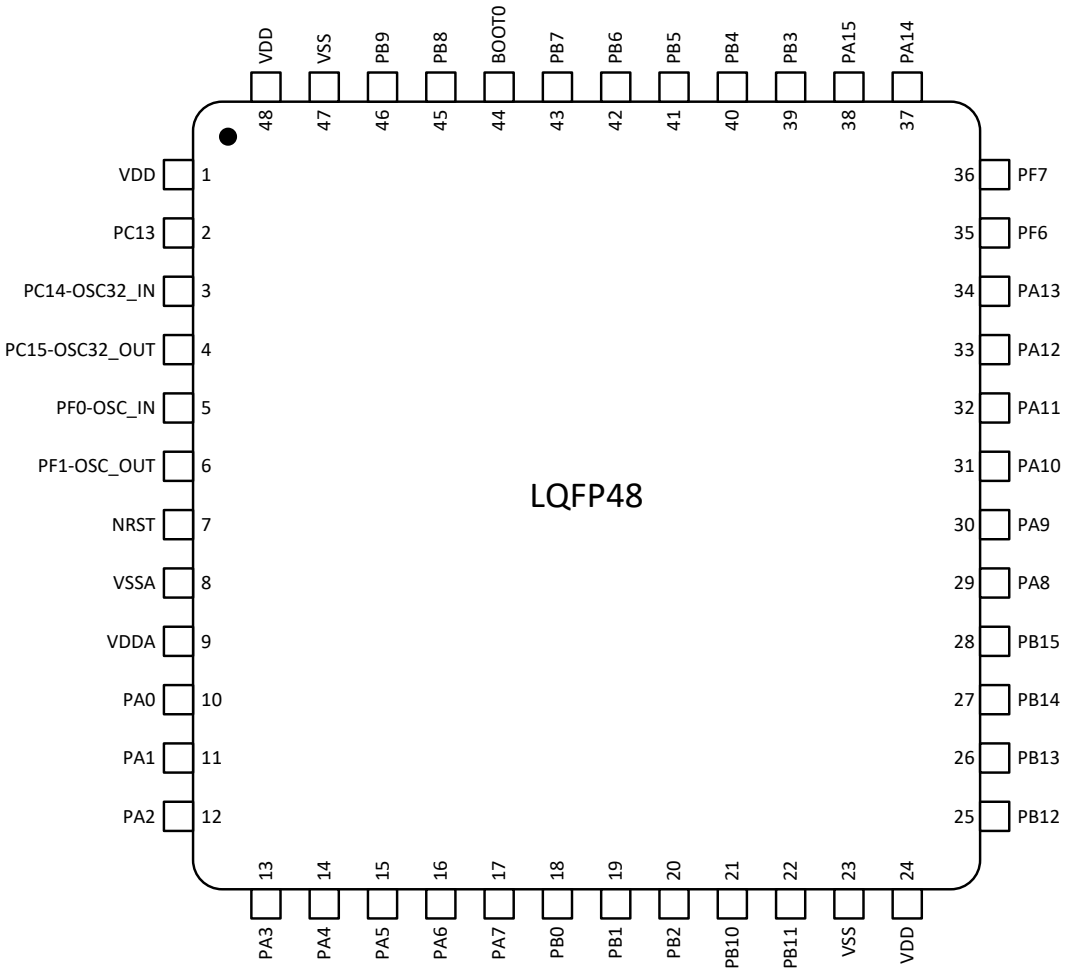
3.2 LQFP48 Package

3.2.1 LQFP48 Pin Assignment



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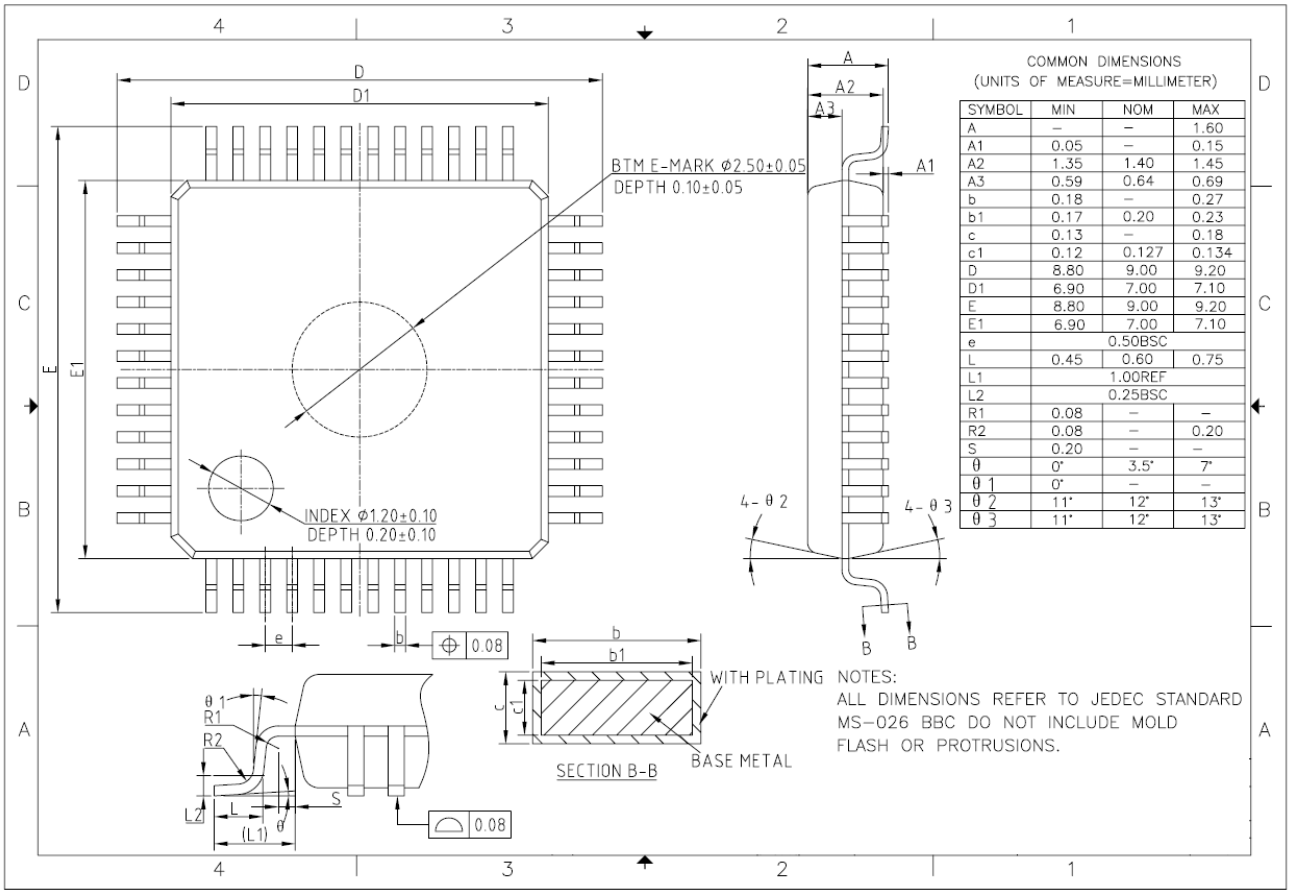
3.2.2 LQFP48(7mm x 7mm) Package Dimensions



SYMBOL	MIN	NOM	MAX
A	–	–	1.60
A1	0.05	–	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	–	0.27
b1	0.17	0.20	0.23
c	0.13	–	0.18
c1	0.12	0.127	0.134
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
e		0.50BSC	
L	0.45	0.60	0.75
L1		1.00REF	
L2		0.25BSC	
R1	0.08	–	–
R2	0.08	–	0.20
S	0.20	–	–
θ	0°	3.5°	7°
θ1	0°	–	–
θ2	11°	12°	13°
θ3	11°	12°	13°

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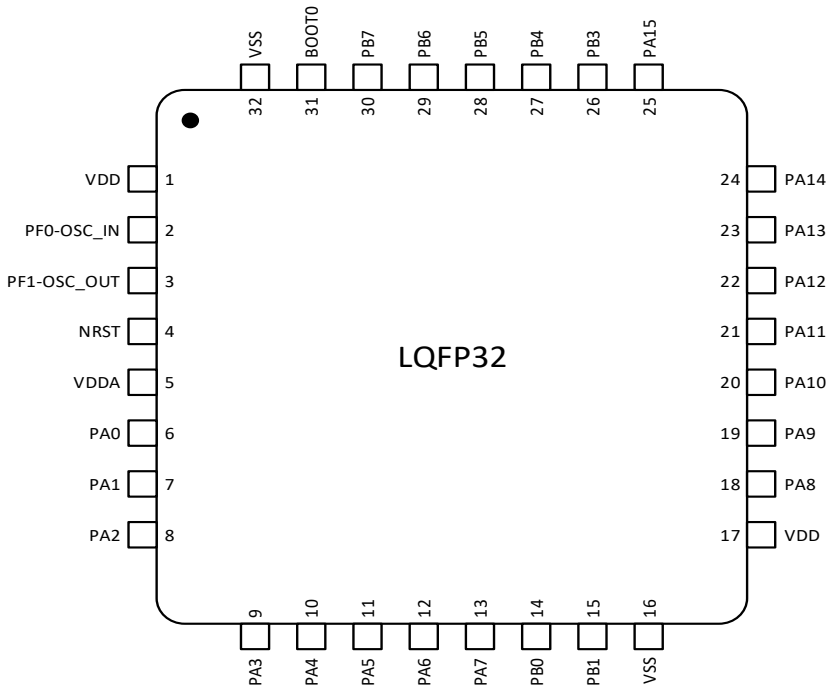
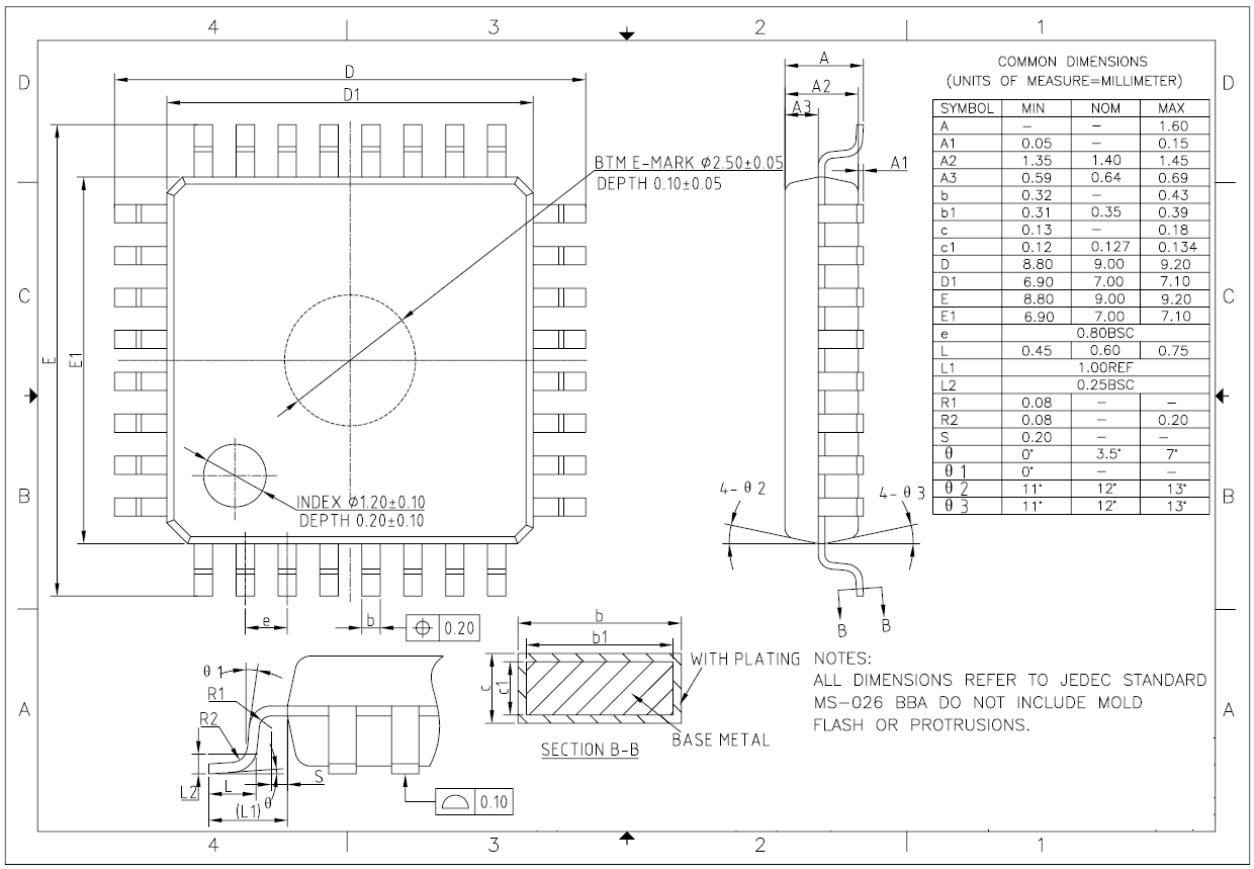
3.3 LQFN32 Package

3.3.1 LQFN32 Pin Assignment



3.3.2 LQFN32(7mm x 7mm) Package Dimensions



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	–	–	1.60
A1	0.05	–	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.32	–	0.43
b1	0.31	0.35	0.39
c	0.13	–	0.18
c1	0.12	0.127	0.134
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
e		0.80BSC	
L	0.45	0.60	0.75
L1		1.00REF	
L2		0.25BSC	
R1	0.08	–	–
R2	0.08	–	0.20
S	0.20	–	–
θ	0°	3.5°	7°
θ1	0°	–	–
θ2	11°	12°	13°
θ3	11°	12°	13°

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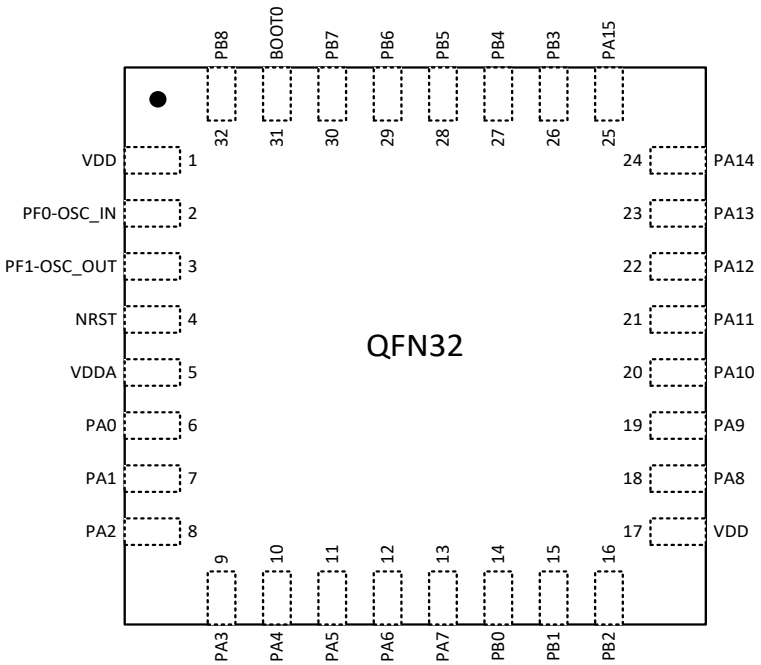
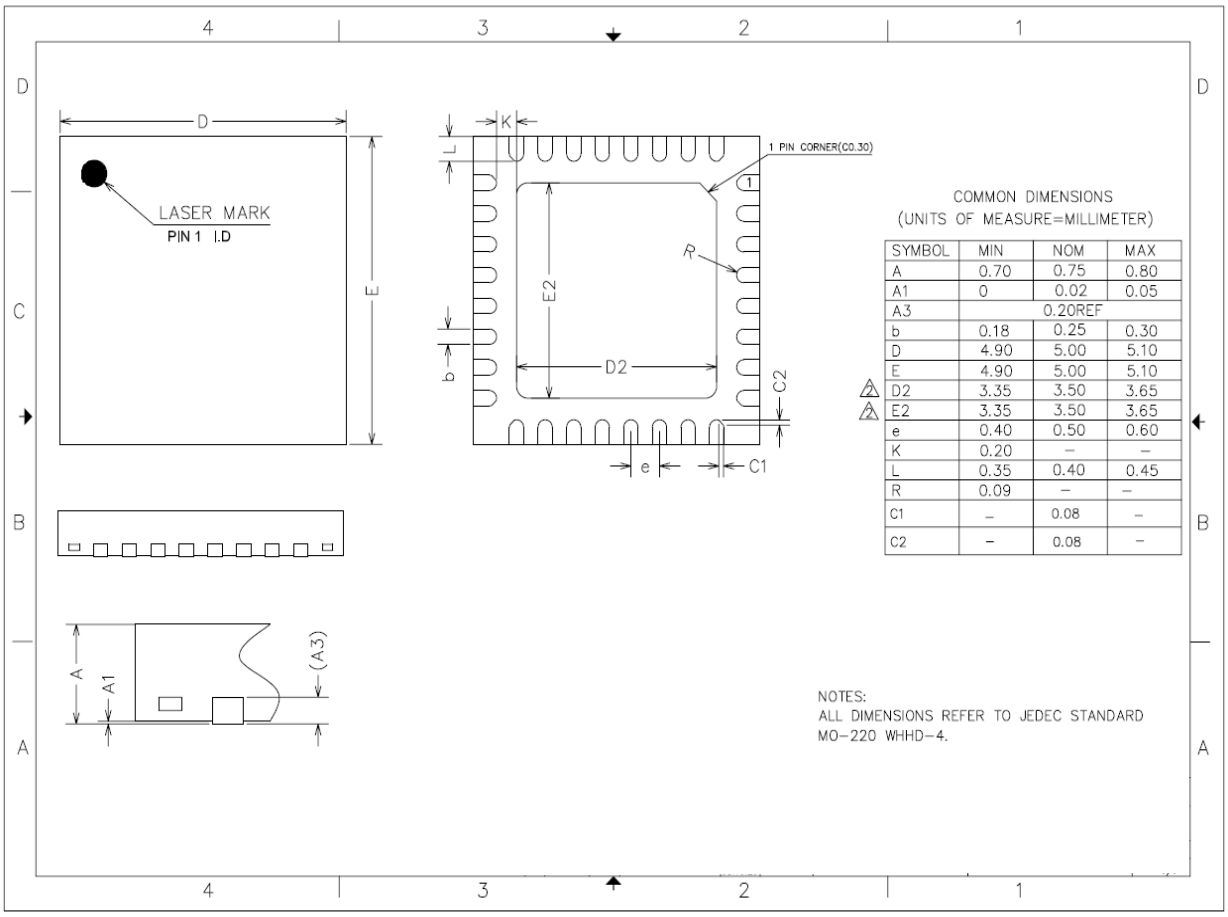
3.4 QFN32 Package

3.4.1 QFN32 Pin Assignment



3.4.2 QFN32(5mm x 5mm) Package Dimensions



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0	0.02	0.05
A3		0.20REF	
b	0.18	0.25	0.30
D	4.90	5.00	5.10
E	4.90	5.00	5.10
D2	3.35	3.50	3.65
E2	3.35	3.50	3.65
e	0.40	0.50	0.60
K	0.20	–	–
L	0.35	0.40	0.45
R	0.09	–	–
C1	–	0.08	–
C2	–	0.08	–

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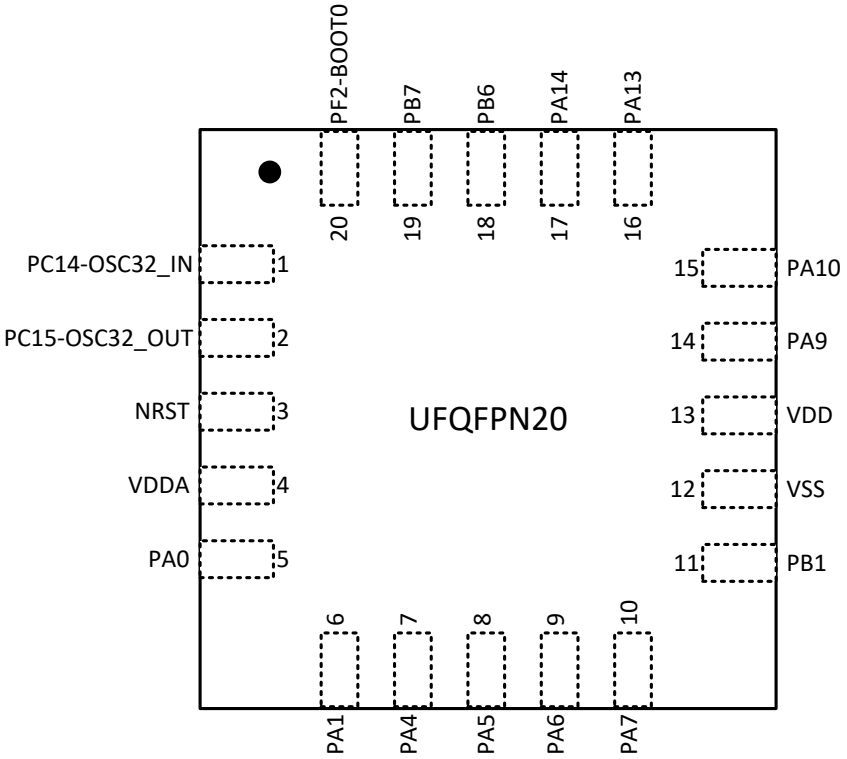
3.5 UFQFPN20 Package

3.5.1 UFQFPN20 Pin Assignment



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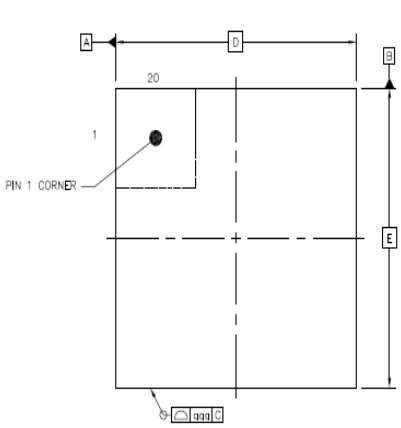
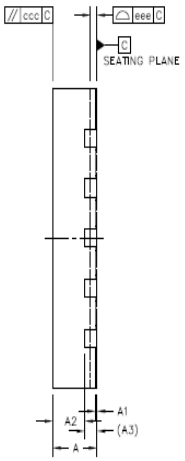
3.5.2 UFQFPN20(3mm x 3mm) Package Dimensions

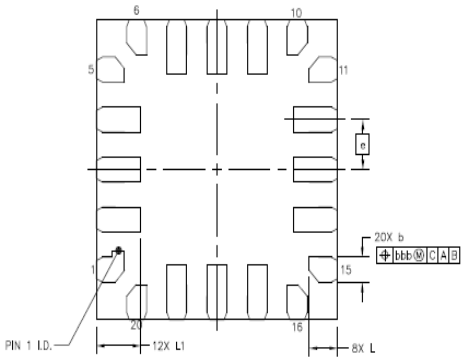


TOP VIEW



SIDE VIEW

		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.5	0.55	0.6
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2	---	0.4	---
L/F THICKNESS		A3		0.152 REF	
LEAD WIDTH		b	0.2	0.25	0.3
BODY SIZE	X	D		3 BSC	
	Y	E		3 BSC	
LEAD PITCH		e		0.5 BSC	
LEAD LENGTH		L	0.25	0.35	0.45
		L1	0.45	0.55	0.65
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		ccc		0.1	
COPLANARITY		eee		0.08	
LEAD OFFSET		bbb		0.1	



BOTTOM VIEW

NOTES
1.REFER TO JEDEC MO-220;
2.COPLANARITY APPLIES TO LEADS, CORNER LEADS AND DIE ATTACH PAD;
3.BAN TO USE THE LEVEL 1 ENVIRONMENT-RELATED SUBSTANCES OF JOET PRESCRIBING;
4.FINISH: Cu/EP • Sn8~20s

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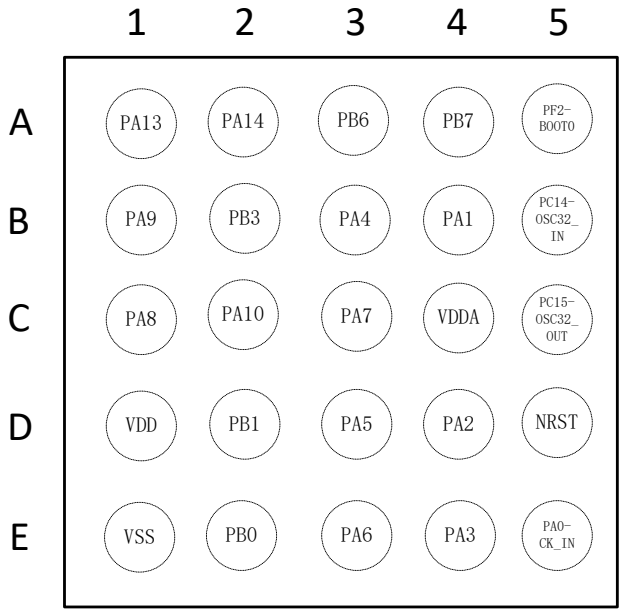
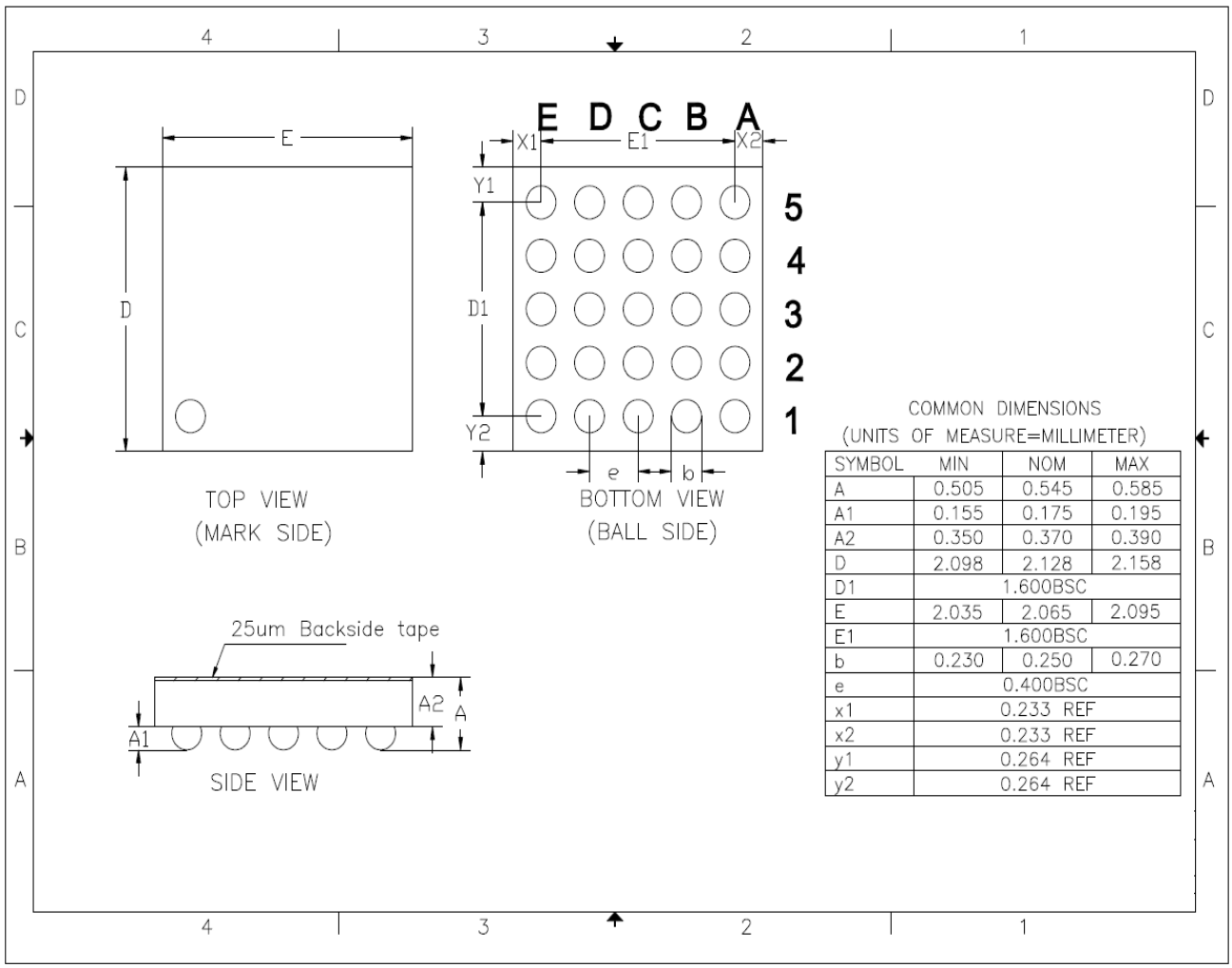
3.6 WLCSP25 Package

3.6.1 WLCSP25 Pin Assignment



3.6.2 WLCSP25(2.128mm x 2.065mm) Package Dimensions



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	0.505	0.545	0.585
A1	0.155	0.175	0.195
A2	0.350	0.370	0.390
D	2.098	2.128	2.158
D1	1.600BSC		
E	2.035	2.065	2.095
E1	1.600BSC		
b	0.230	0.250	0.270
e	0.400BSC		
x1	0.233 REF		
x2	0.233 REF		
y1	0.264 REF		
y2	0.264 REF		

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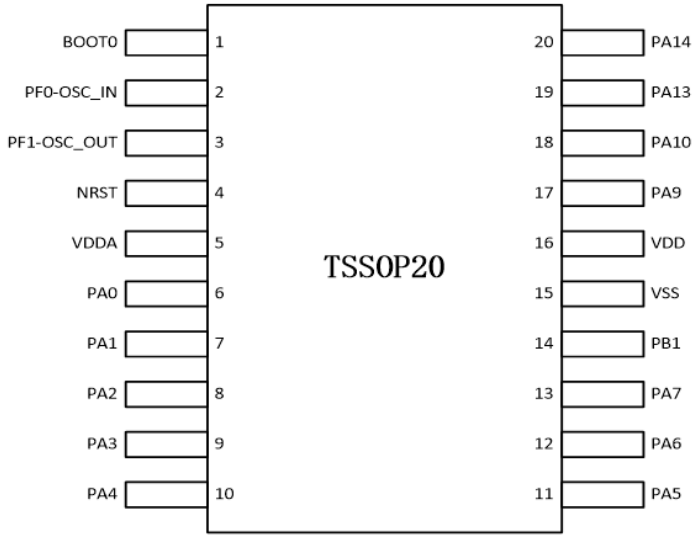
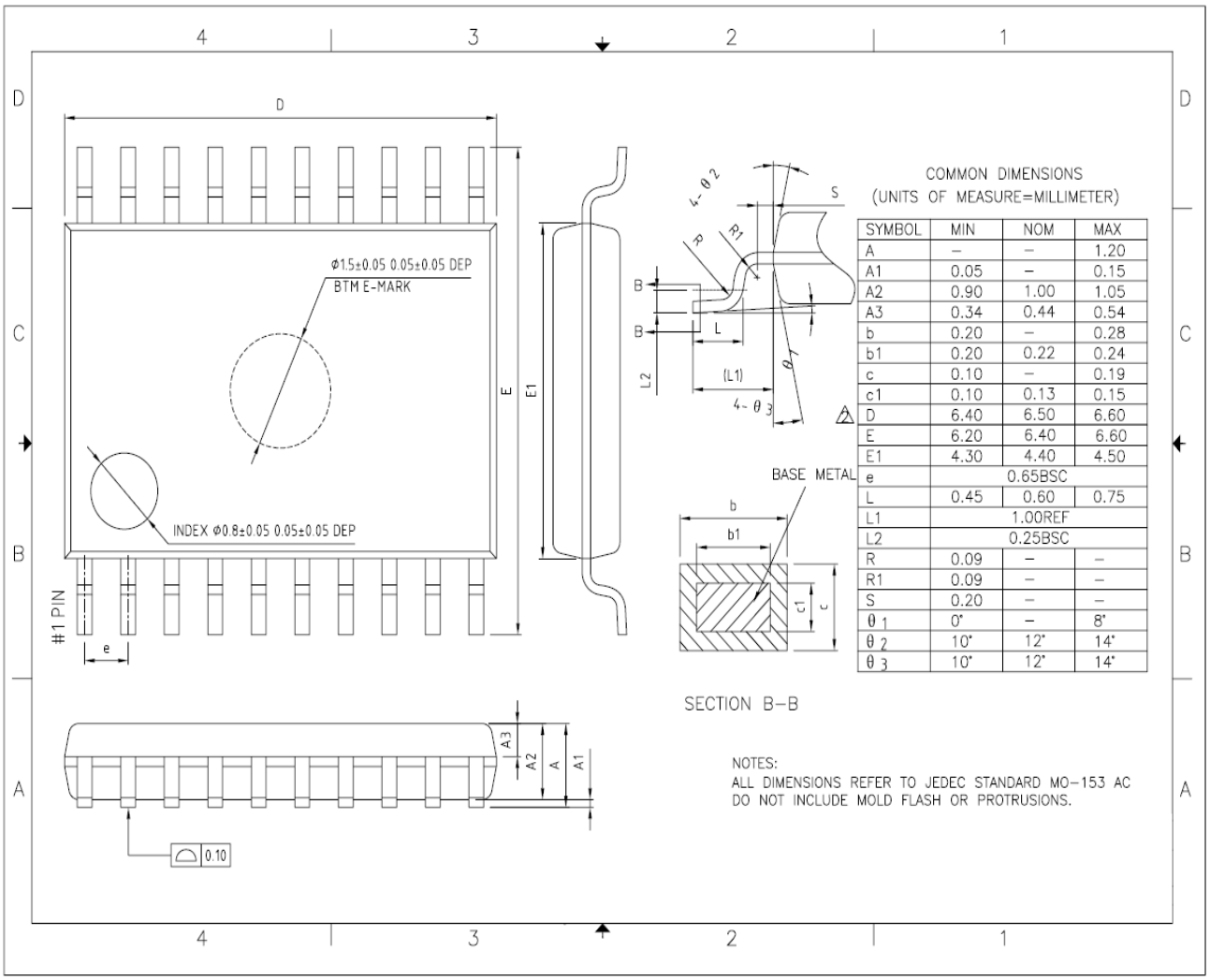
3.7 TSSOP20 Package

3.7.1 TSSOP20 Pin Assignment



3.7.2 TSSOP20(6.5mm x 4.4mm) Package Dimensions



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4 Version History

Version	Date	Changes
V1.0.0	2020.6.10	Initial document
V2.0.0	2021.1.12	Update version
V2.1.0	2022.7.14	1) The clock output in the key features has been changed to two channels, with added outputs for LSE and LSI 2) Removed the volume label from the naming convention in chapter 1 3) Added N32G032K8L7 4) Removed programmable low voltage detection and reset from the key features 5) Removed TSC-related content 6) Deleted N32G032C8Q7 and added N32G032F8S7

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