

# N32G032 x6/x8

# Product Instruction

**N32G032 series based on Arm® Cortex®-M0, run up to 48MHz, up to 64KB embedded flash, 16KB SRAM, integrated analog interface, 1x12bit 1Msps ADC, 1xOPAMP, 3xcomparator, integrated multi-channel U(S)ART, I2C, SPI, CAN and other digital communication interfaces, built-in hardware acceleration engine for cryptographic algorithm.**

## Key feature

### ● Core

- A 32-bit general-purpose microcontroller based on the Arm® Cortex®-M0 core, Single-cycle hardware multiply instruction
- Run up to 48MHz

### ● Encrypted memory

- Up to 64KByte embedded Flash memory, supports encrypted storage, multi-user partition management and data protection, supports hardware ECC verification, data 100,000 cycling and 10 years of data retention
- SRAM of 16KB, supporting hardware parity

### ● Low-power management

- Stop mode: RTC Run, maximum 16KByte SRAM retention, CPU register retention, all IO retention
- Power Down mode: support 3 IO wakeup

### ● Clock

- HSE: 4MHz~20MHz external high-speed crystal
- LSE: 32.768KHz external low-speed crystal
- HSI: Internal high-speed RC OSC 8MHz
- LSI: Internal low-speed RC OSC 30KHz
- Built-in high-speed PLL
- MCO: Support 2-way clock output, configurable SYSCLK, HSI, HSE, LSI, LSE, and PLL clock output that can be divided.

### ● Reset

- Support power-on/power-off/external pin reset
- Support watchdog reset

### ● Communication interface

- 6xU(S)ART, with a maximum rate of 3 Mbps, of which 2 USART interfaces (support 1xISO7816, 1xIrDA, LIN), 4x UART interfaces, 2 of which support low power (LPUART, the highest communication rate in this mode is 9600bps), Stop mode can be awakened
- 3xSPI, up to 12 MHz, one of which supports multiplexing with I2S
- 2xI2C, the rate is up to 1 MHz, which can be configured in master/slave mode and support dual address response in slave mode. Supports dual-level communication: normal level (signal level matches chip VDD) and low level (chip VDD 3.3V or 5V, signal level 1.8V) two levels can be selected.
- 1x CAN 2.0A/B bus interface.

### ● Analog interface

- 1x12bit 1MSPS ADC , up to 16 external single-ended input channels
- 1xOPAMP, internal programmable gain amplifier up to 32 times
- 3xCOMP, built-in 64-level adjustable comparison reference
- **Up to 56 GPIOs**
- **1xDMA, 8-channel, channel source address and destination address can be arbitrarily configurable**
- **1x RTC real-time clock, support leap year perpetual calendar, alarm event, periodic wake up, support internal and external clock calibration**
- **2xBeeper, support complementary output, 16mA output drive capacity**
- **Timer counter**
  - 2x16-bit advanced timer counters, support input capture, complementary output, orthogonal encoding input, each timer support 4 independent channels. 3 of which support 6 pairs complementary PWM outputs
  - 2x16-bit general purpose timer counters, each timer has 4 independent channels, supports input capture/output compare/PWM output
  - 1x16-bit basic timer counters
  - 1x16-bit low power timer counter
  - 1x24-bit SysTick
  - 1x7-bit Window Watchdog (WWDG)
  - 1x12-bit Independent watchdog (IWDG)
- **Programming mode**
  - Support SWD online debugging interface
  - Support UART Bootloader
- **Hardware Divider(HDIV)and Square Root(SQRT)**
- **Security features**
  - Built-in cryptographic algorithm hardware acceleration engine
  - Support AES, SM4 algorithms
  - Flash storage encryption
  - Flash storage encryption, Multi-user partition Management Unit (MMU)
  - TRNG true random number generator
  - CRC16/32 calculation
  - Support write protection(WRP), multiple read protection(RDP) levels (L0/L1/L2)
  - Support external clock failure detection, tamper detection
- **96-bit UID and 128-bit UCID**
- **Working conditions**
  - Operating voltage Range: 1.8V~5.5V
  - Operating Temperature Range: -40°C~105°C
  - ESD: ±4KV (HBM model), ±1KV (CDM model)
- **Package**
  - UFQFPN20(3mm x 3mm)
  - TSSOP20(6.5mm x 4.4mm)

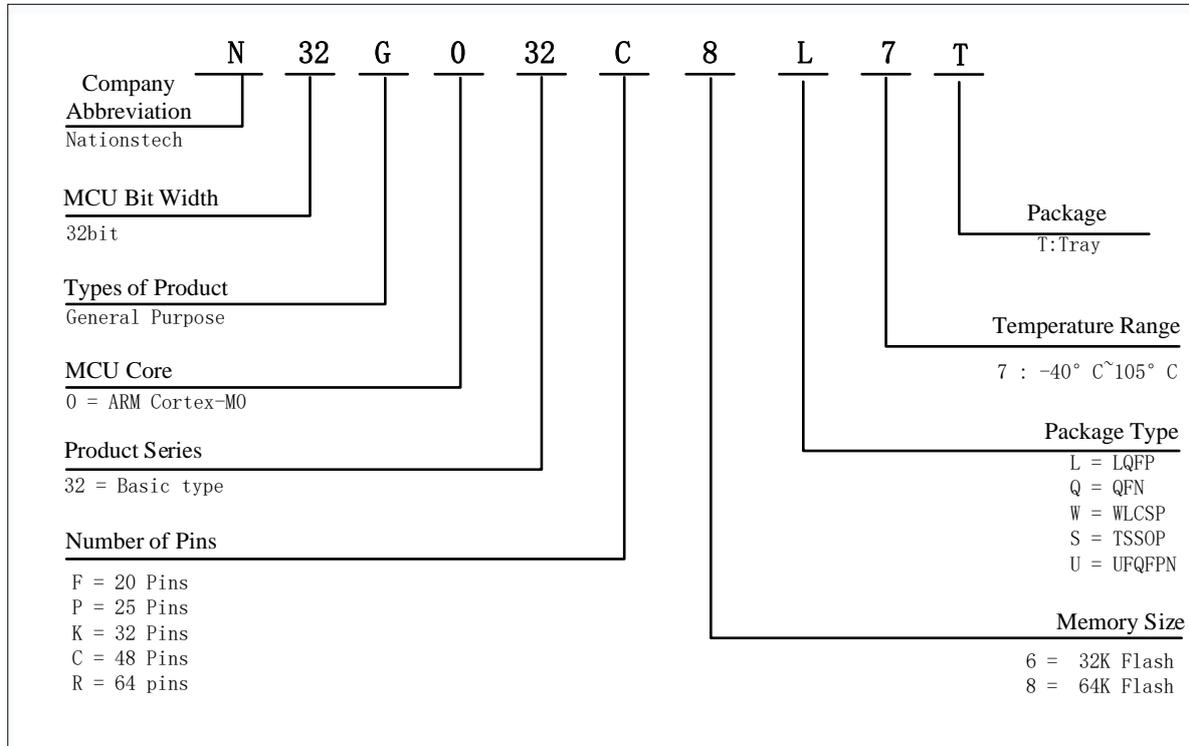
- QFN32(5mm x 5mm)
- LQFP32(7mm x 7mm)
- LQFP48(7mm x 7mm)
- LQFP64(10mm x 10mm)
- WLCSP25(2.128mm x 2.065mm)

● **Order model**

Series	Part Number
N32G032x6 N32G032x8	N32G032F6U7, N32G032F6S7, N32G032F8S7 N32G032P6W7, N32G032P8W7 N32G032K6L7, N32G032K8L7, N32G032K6Q7 N32G032C8L7 N32G032R8L7

# 1 Part number information

Figure 1-1 N32G032 Series order code information



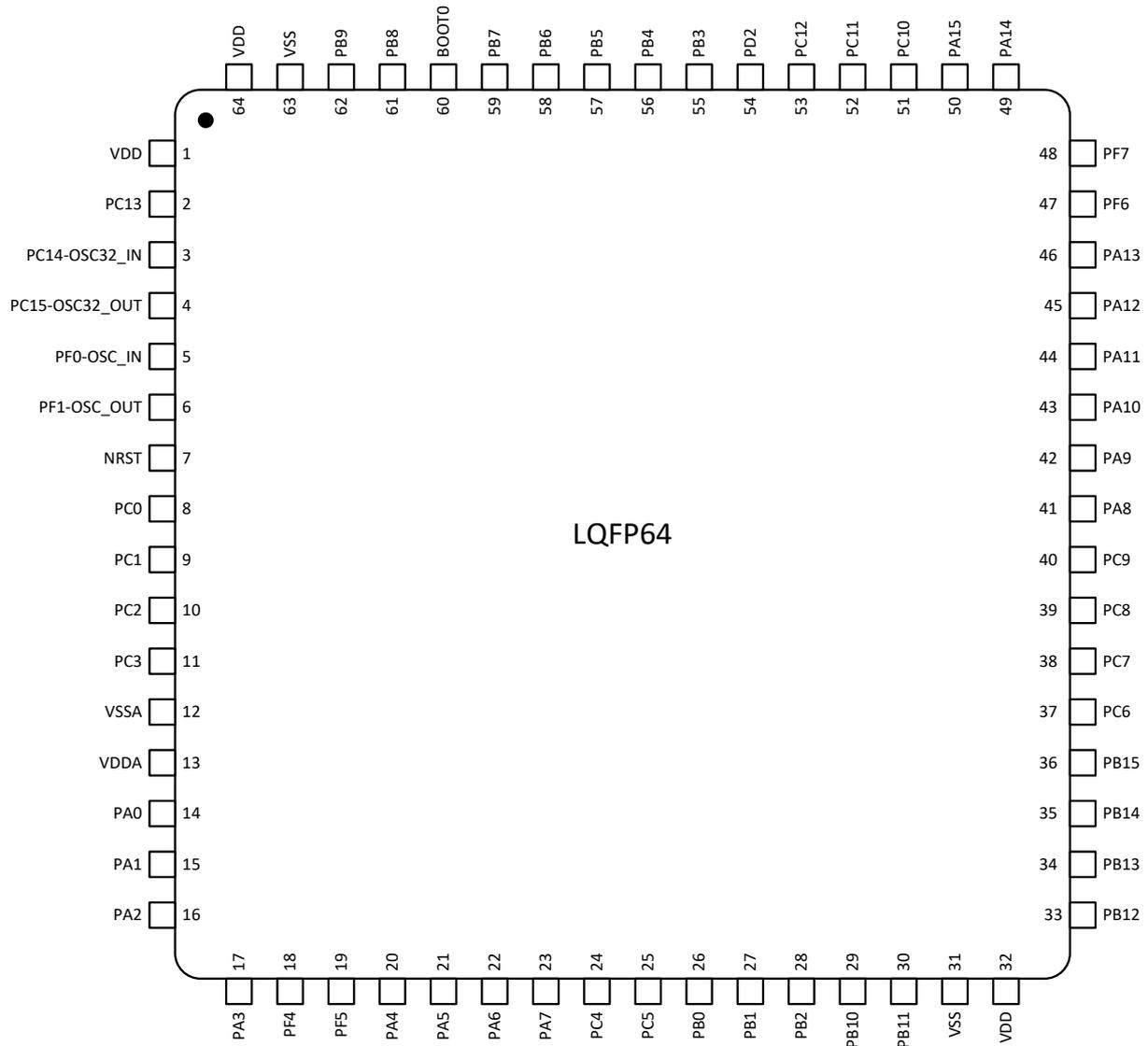
## 2 Product model resource configuration

Part Number	N32G032 F6U7	N32G032 F6/8S7	N32G032 P6/8W7	N32G032 K6Q7	N32G032 K6/8L7	N32G032 C8L7	N32G032 R8L7
Flash capacity (KB)	32	32/64	32/64	32	32/64	64	64
SRAM capacity (KB)	8	8/16	8/16	8	8/16	16	16
CPU frequency	ARM Cortex-M0 @48MHz						
working environment	1.8~5.5V/-40~105°C						
Timer	General	2					
	Advanced	2					
	Basic	1					
	LPTIM	1					
	RTC	1					
communication interface	SPI	1		2		3	3
	I2S	1					
	I2C	2					
	USART	2					
	UART	1	2				
	LPUART	2					
	CAN	1					
GPIO	16		21	28	26	40	56
DMA Number of Channels	1 8Channel						
12bit ADC Number of channels	1 7Channel	1 9Channel	1 10Channel	1 10Channel	1 10Channel	1 10Channel	1 16Channel
OPA/COMP	1/2	1/3	1/2	1/3	1/3	1/3	1/3
Beeper	2	1	2				
Algorithm support	AES、SM4、CRC16/CRC32、TRNG						
security protection	Read and write protection (RDP/WRP), storage encryption, partition protection						
Package	UFQFPN20	TSSOP20	WLCSP25	QFN32	LQFP32	LQFP48	LQFP64

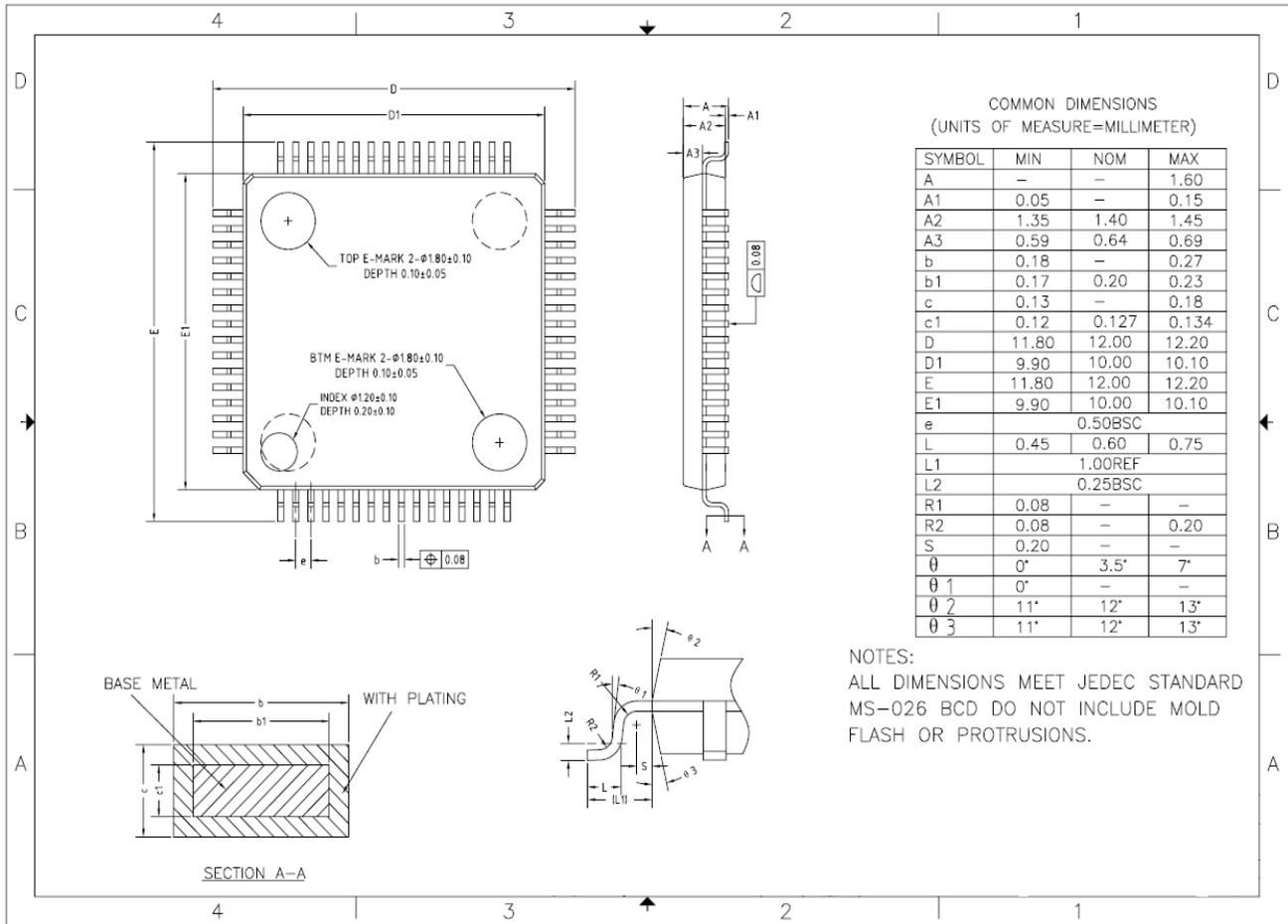
### 3 Package information

#### 3.1 LQFP64

##### 3.1.1 LQFP64 pinouts

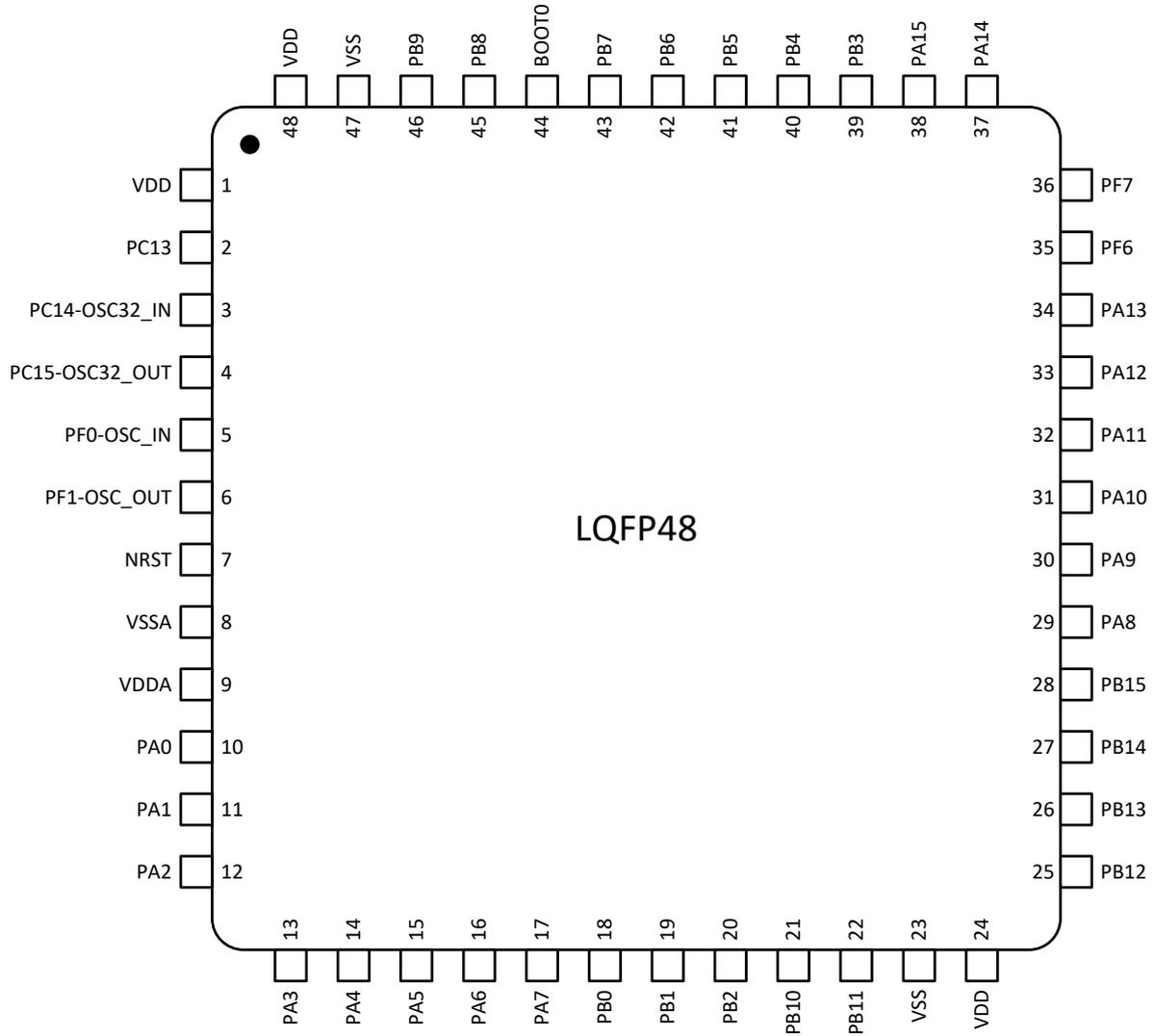


### 3.1.2 LQFP64 package

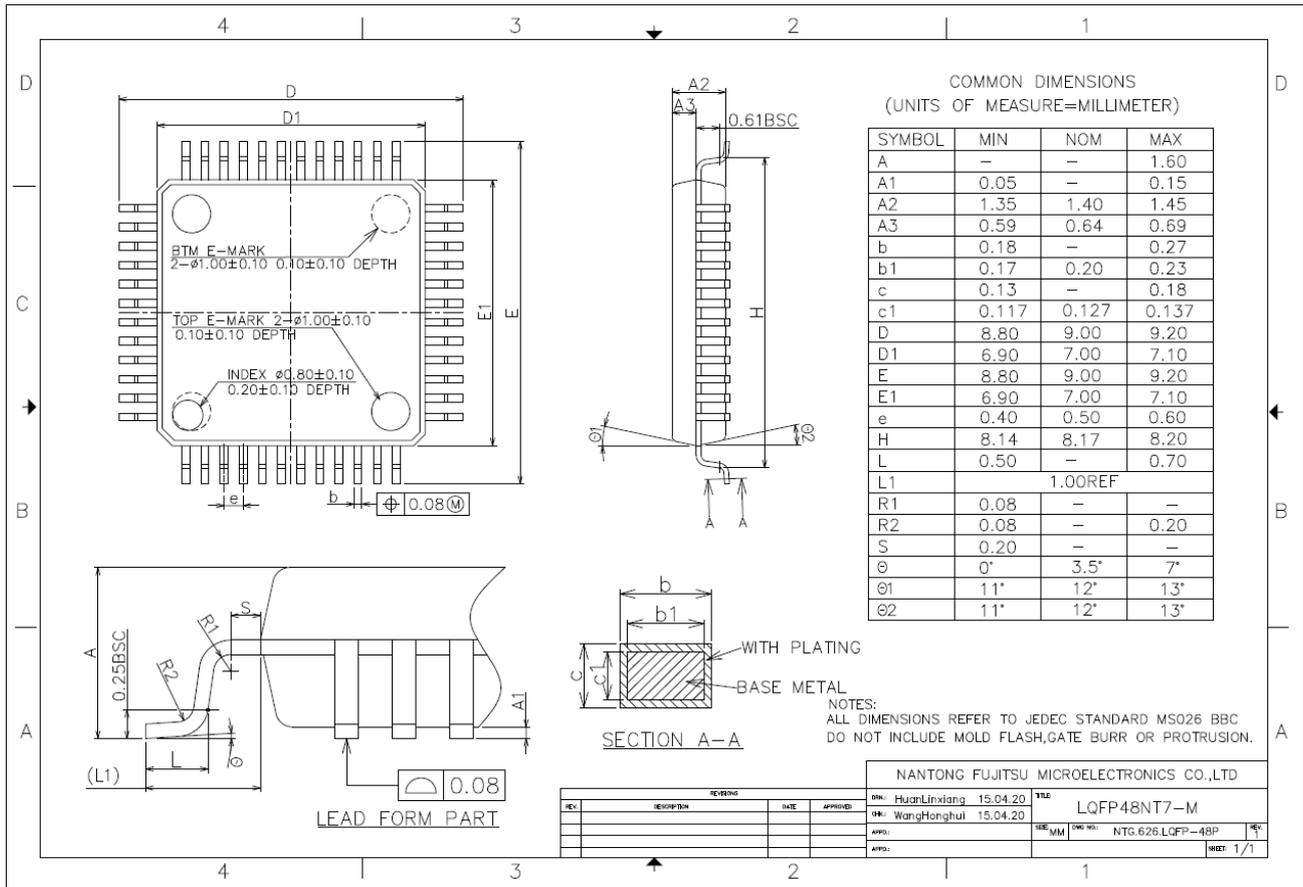


## 3.2 LQFP48

### 3.2.1 LQFP48 pinouts

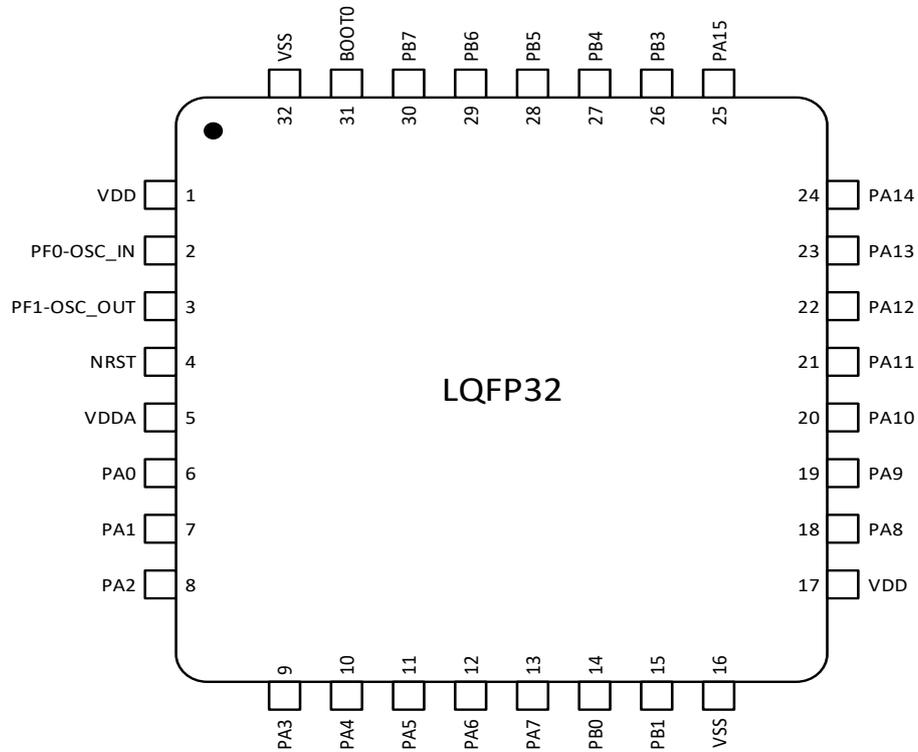


### 3.2.2 LQFP48 package

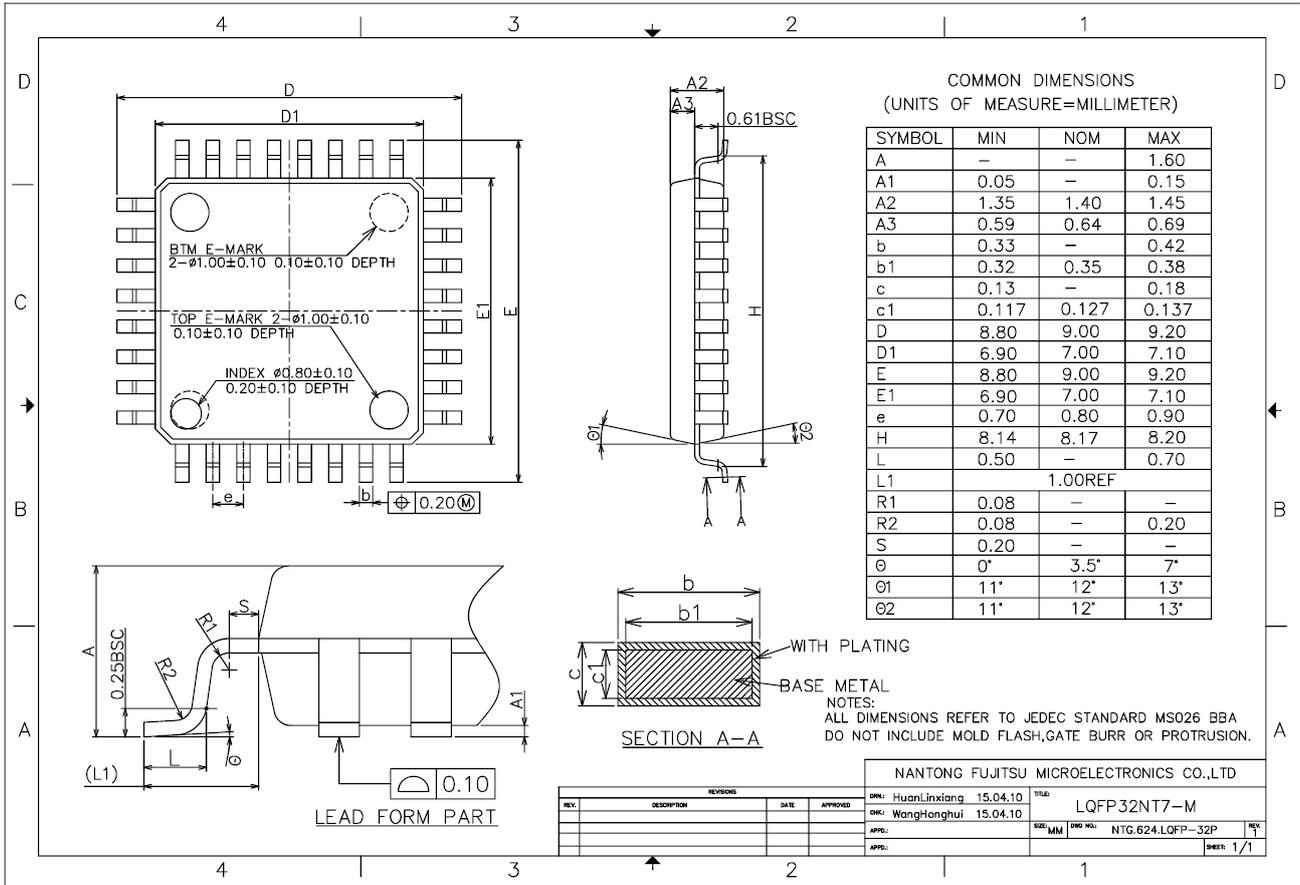


### 3.3 LQFN32

#### 3.3.1 LQFN32 pinouts

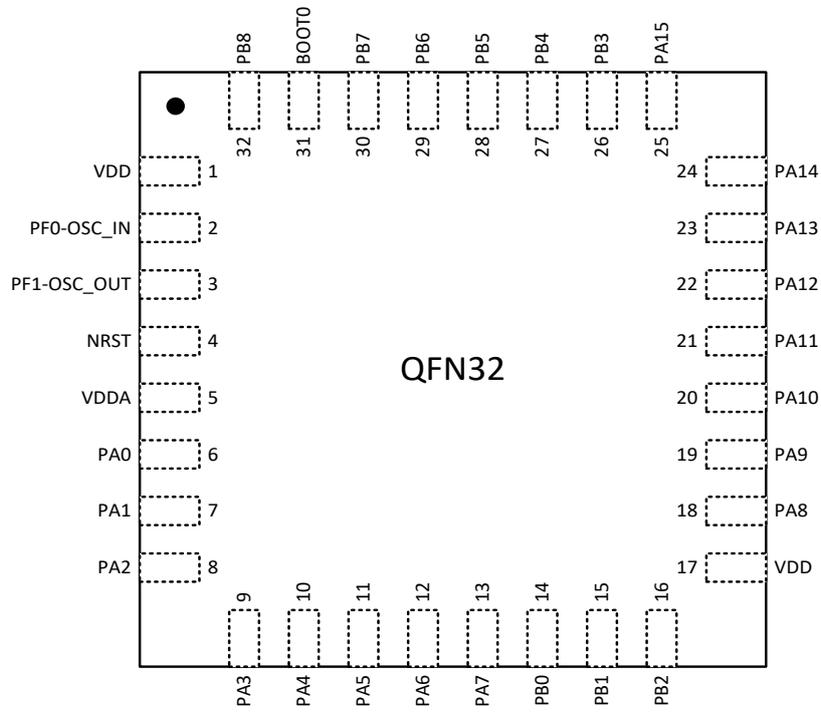


### 3.3.2 LQFN32 package

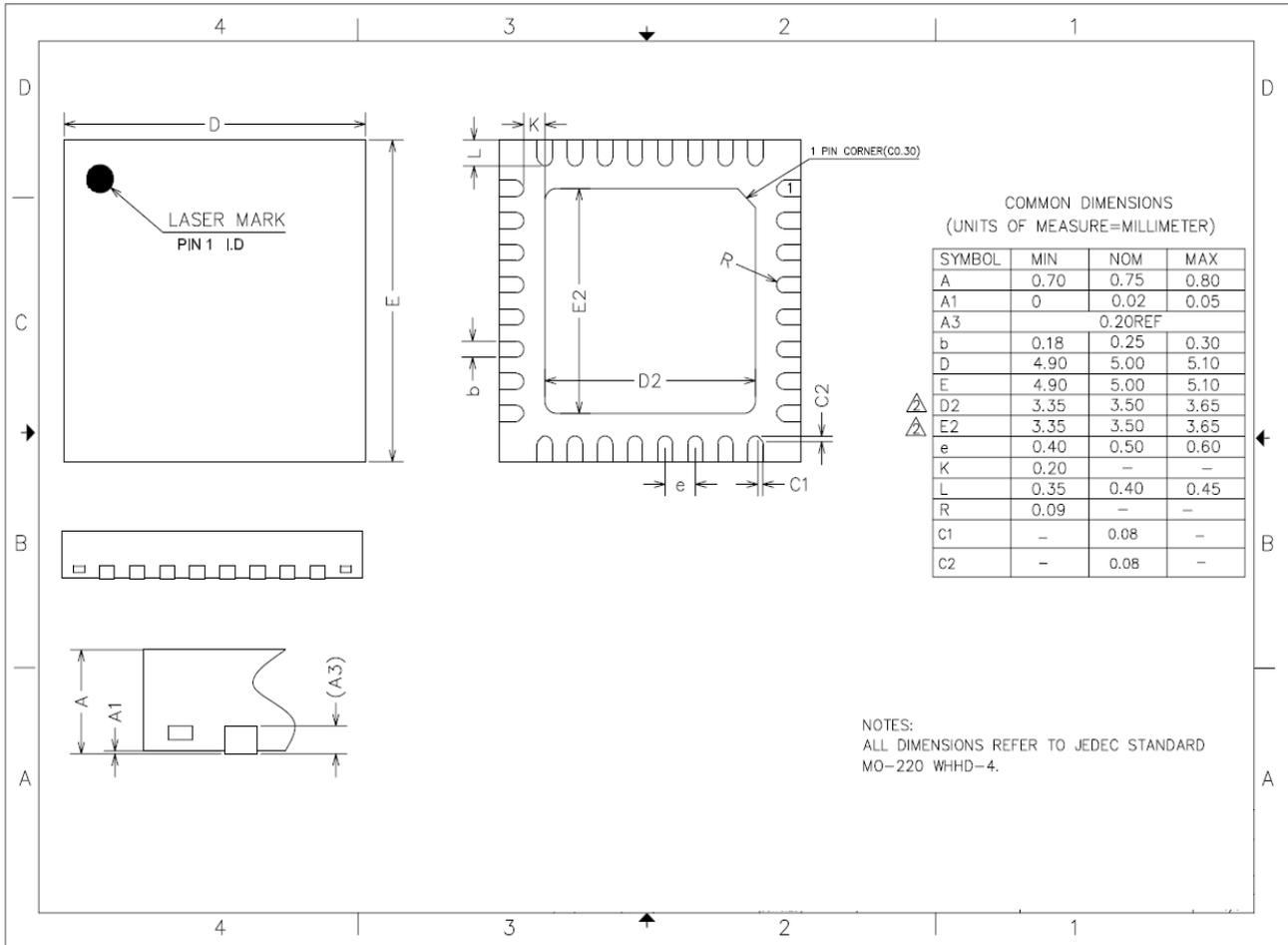


### 3.4 QFN32

#### 3.4.1 QFN32 pinouts

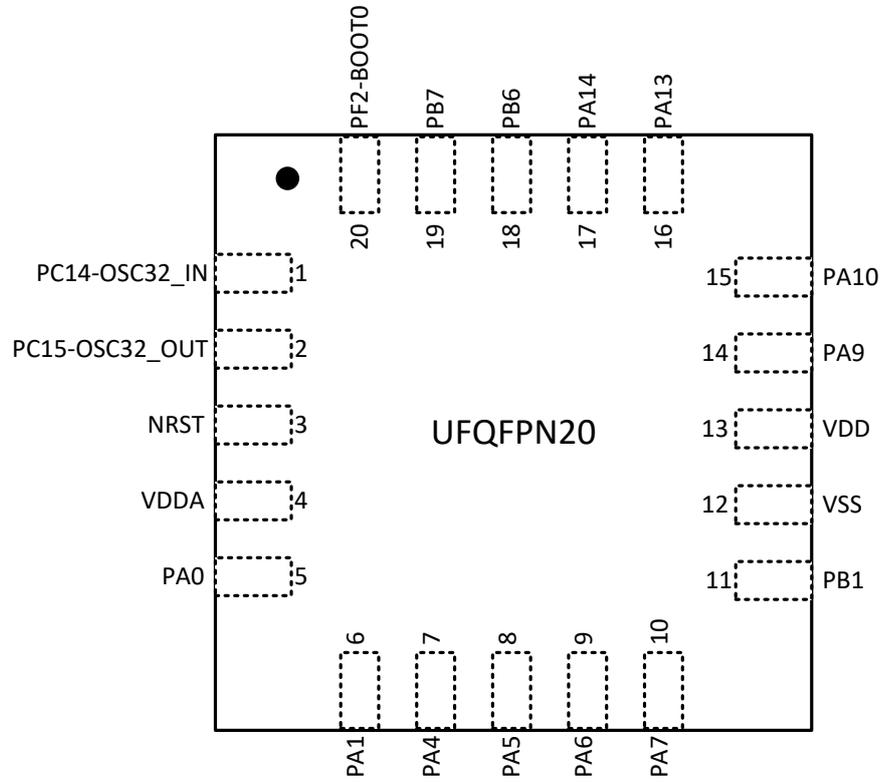


### 3.4.2 QFN32 package



## 3.5 UFQFPN20

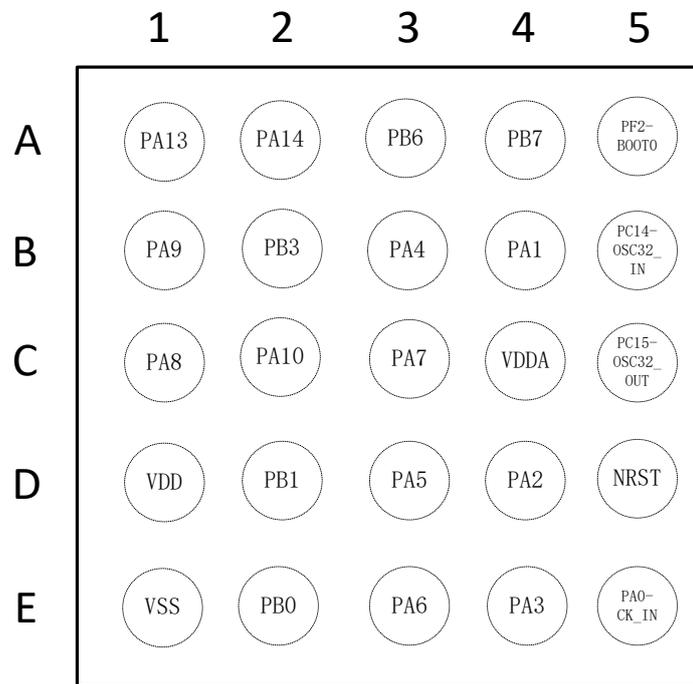
### 3.5.1 UFQFPN20 pinouts



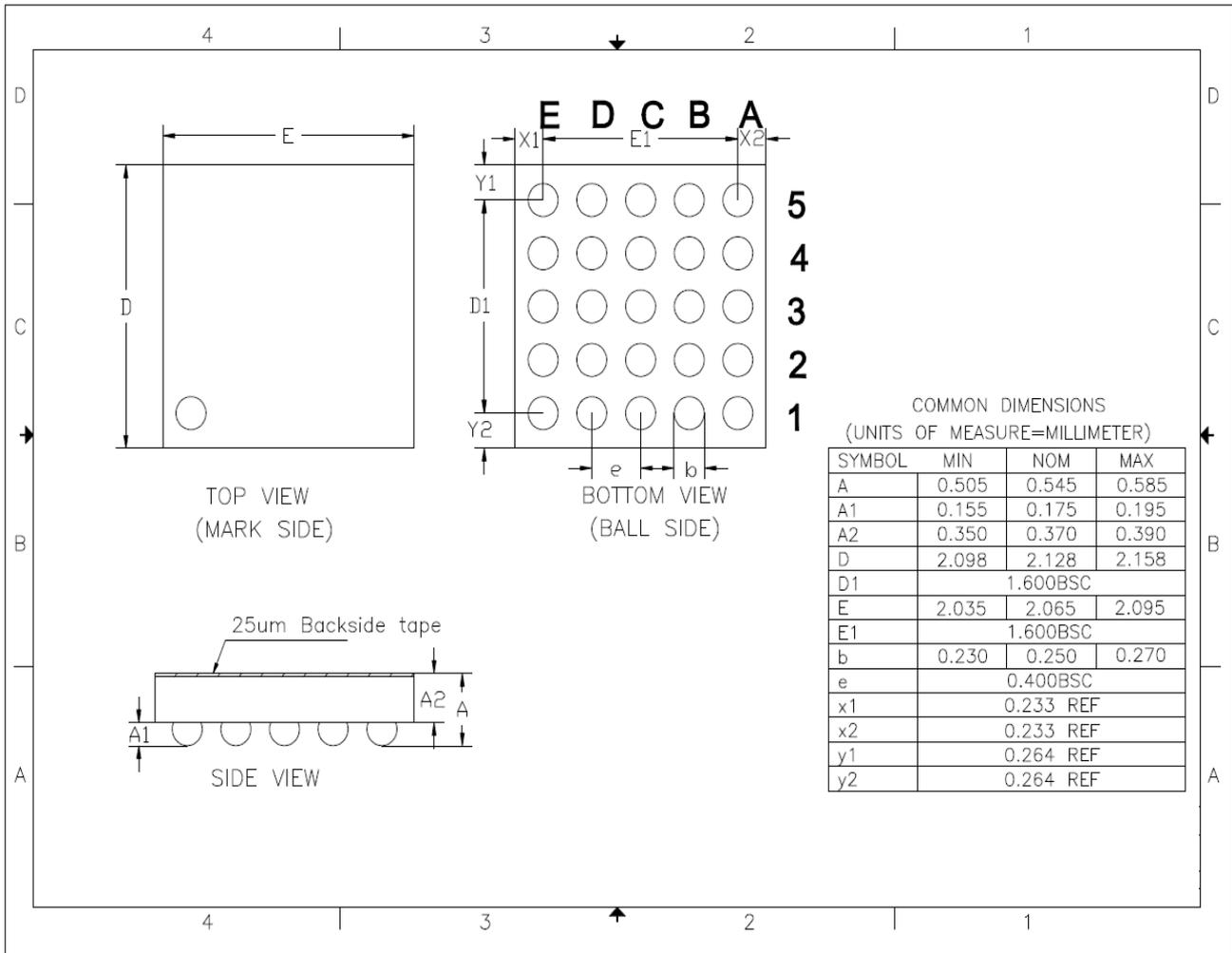


### 3.6 WLCSP25

#### 3.6.1 WLCSP25 pinouts

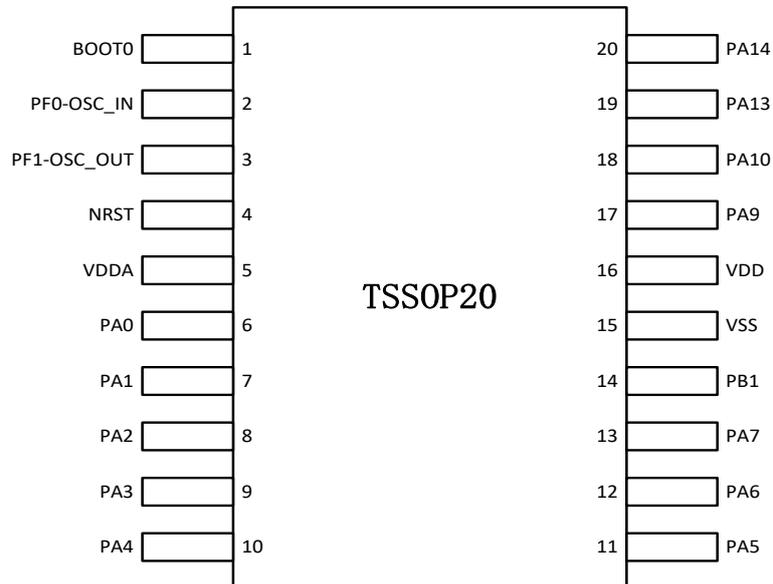


### 3.6.2 WLCSP25 package

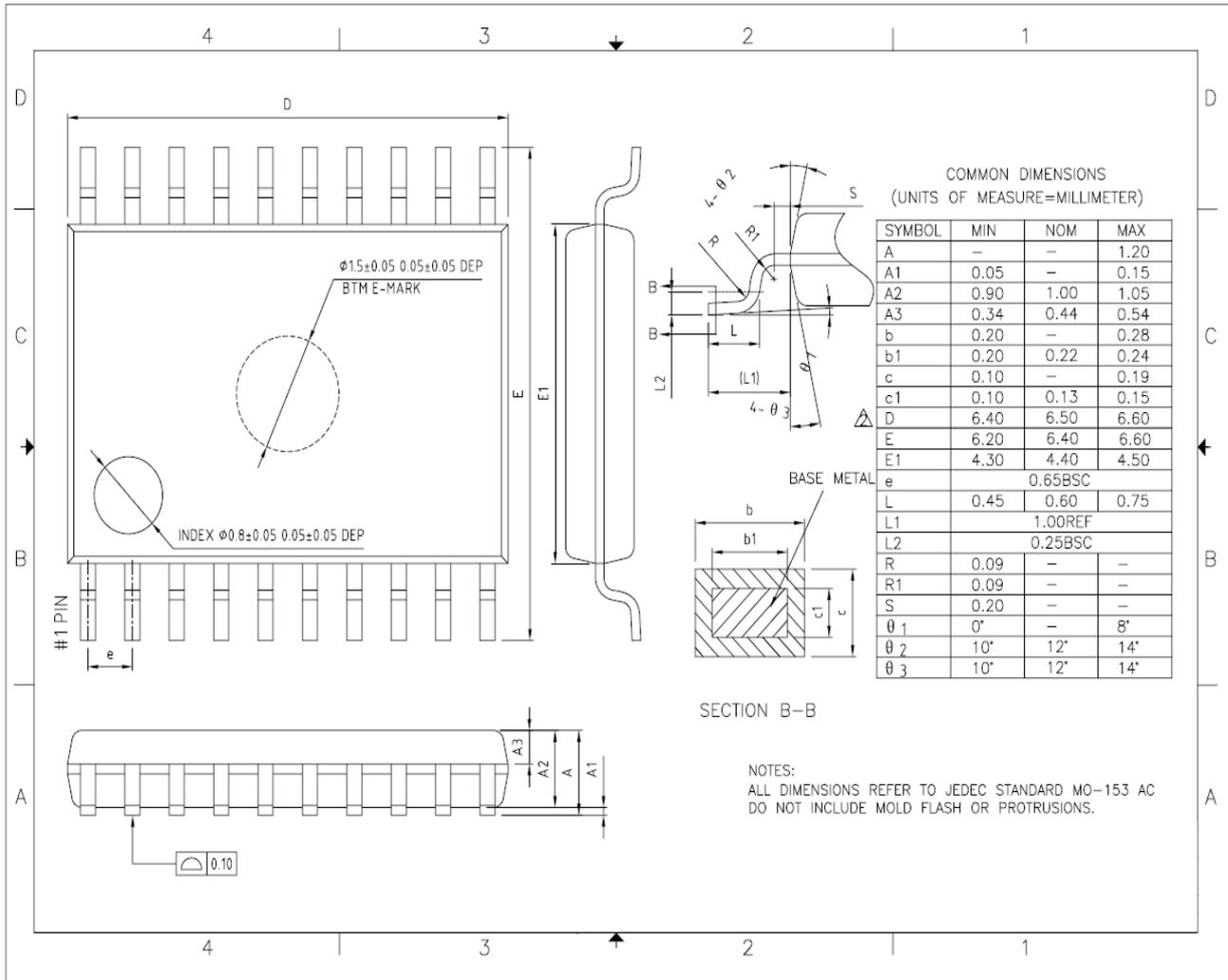


## 3.7 TSSOP20

### 3.7.1 TSSOP20 pinouts



### 3.7.2 TSSOP20 package



## 4 Revision History

<b>Version</b>	<b>Date</b>	<b>Note</b>
V2.1.0	2023.8.23	1. Initial document
V2.2.0	2024.5.07	1. Section 3.2.2. Modify package dimension of LQFP48 2. Section 3.3.2. Modify package dimension of LQFP32

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