

Design Guide

Design Guide for Hardware of N32WB03x Series Chips

Overview

This document is the summary of hardware design experiences of Bluetooth chips by NSING Technologies Inc. and is applicable to be hardware design references for N32WB03x series chips of the Company. It is the detailed specifications for chip hardware design, selection of some important components and cautions for PCB Layout.

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1. Schematic diagram design

1.1. Specifications on power supply design of schematic diagram

- 1) When the external power supply voltage is 1.8V/2.32V~3.6V, it can be directly connected to chip VCC.
- 2) VCCRF, from which the maximum supply is 3.6V, is recommended to be connected to VCC pin in parallel, the resistance R3 of EVB can be removed, connect VCC directly .
- 3) Note the chip GND pin is at the bottom of the chip, and be sure to connect the square bonding pad at the bottom of the chip to GND network for wiring. See Chapter 3.3 for details.

1.2. Differences between two power supply modes

Two power supply modes are available for chips, and the main differences between the two modes are set forth below:

Mode		
Parameters	DCDC power supply mode	LDO power supply mode
BOM difference	4.7uh inductor required	4.7uh inductor not required
Active power consumption	1.8 mA	3.8 mA
Power consumption in Sleep mode	1.6 uA	1.6 uA
RFTX power consumption	4 mA	8 mA
RFRX power consumption	3.8 mA	7.8 mA
RFRX sensitivity	-94 dBm	-95 dBm
RFRX maximum power	+8 dBm	+8 dBm

1.3. Reference schematic diagram for DCDC power supply mode

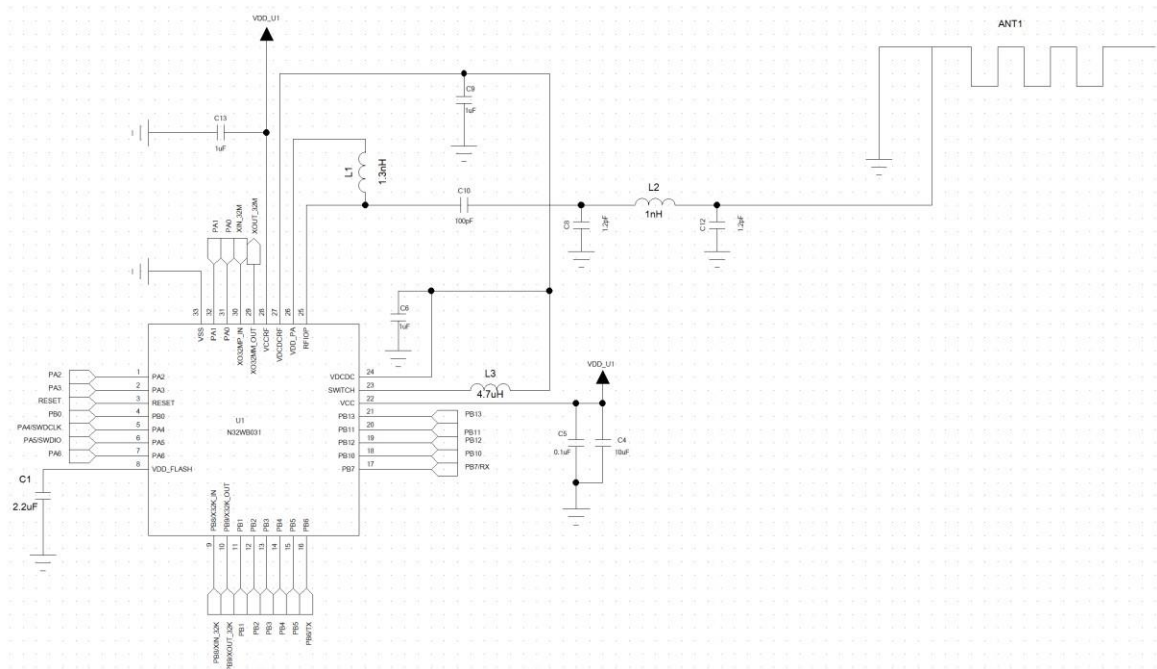


Fig. 1-1 Reference Schematic Diagram for DCDC Power Supply Mode

1.5. Reference schematic diagram for external crystal

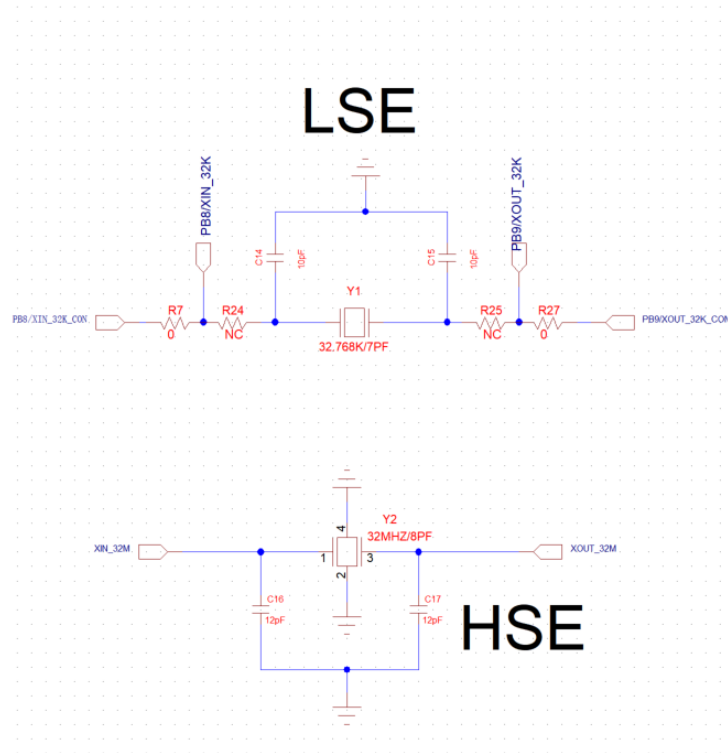


Fig.1-3 Reference Schematic Diagram for External Crystal

1.6. Reference schematic diagram for reset circuit

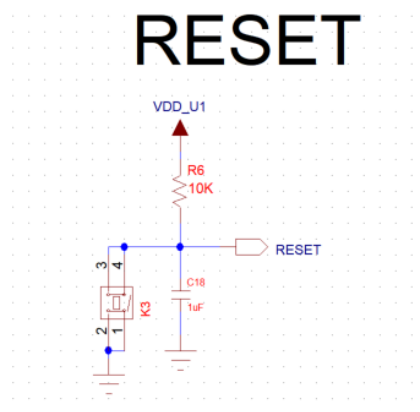


Fig. 1-4 Reference Schematic Diagram for Reset Circuit

1.9. Reference Schematic Diagram for Infrared Transmitter Circuit

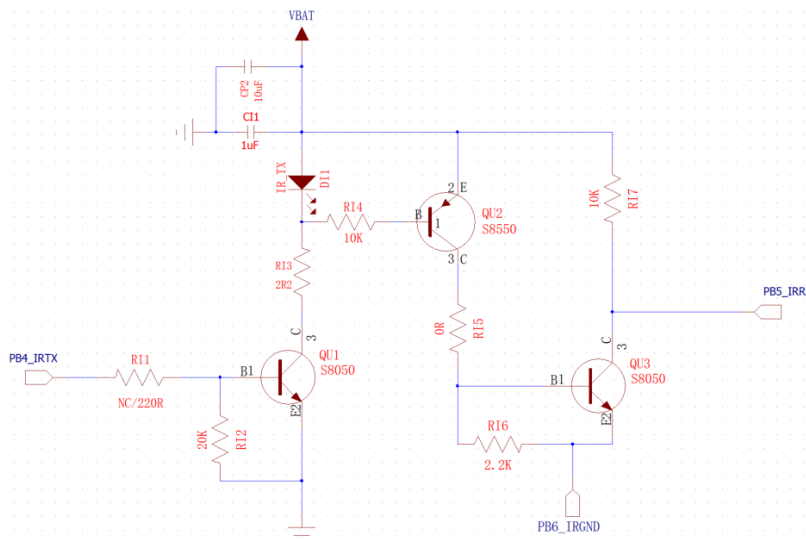


Fig. 1-7 Reference Schematic Diagram for Infrared Transmitter Circuit

2. Specifications on chip pins in the schematic diagram

2.1. Power supply pins

- PIN24(VDCDC) is the power supply pin receiving internal DCDC generated voltage, its typical voltage is 1.15V, it needs to be connected with 1uF decoupling capacitor, and 4.7uH power inductor needs to be provided in series between PIN24(VDCDC) pin and PIN23(SWITCH). This inductor is related to the BLE receiving sensitivity. The inductor selection can refer to 《N32WB031 Development Board Inductor Selection Table.xlsx》.
- PIN27(VDCDCRF) is the internal RF power supply pin receiving internal DCDC generated voltage, can be directly connected to PIN24(VDCDC), its typical voltage is 1.15V and it needs to be connected with 1uF decoupling capacitor.
- **PIN28(VCCRF) is external power supply pin**, needs to be connected with 1uF decoupling capacitor, and its external voltage range is 1.8V/2.32V~3.6 V.
- PIN22(VCC) is external power supply pin, needs to be connected with 0.1uF and 4.7uF decoupling capacitors, and its external voltage range is 1.8V/2.32V~3.6V.

- PIN8(VDD_FLASH) is the internal FLASH power supply pin, needs to be connected only with 0.1uF and 2.2uF decoupling capacitors without external power supply.

2.2. RF pins

- PIN25(RFIOP) is RF pin.
- PIN26(VDD_PA) receives the bias voltage with a range of 0.9V~1.7V generated by internal RF_PA, depending on the internal register configuration, the transmit power is different, and the bias voltage generated is different

2.3. Crystal oscillator pins

- PIN29(XO32MM) and PIN30(XO32MP) are Bluetooth reference clock pins and need to be connected with 32MHz crystals. As the Bluetooth requirement for frequency deviation is high, the frequency deviation of the crystal oscillators should be $\leq \pm 10\text{ppm}$. Note that external 32MHz crystals must be provided for using the Bluetooth function.
- PIN9(XO32KP_IN) and PIN10(XO32KM_OUT) are low-frequency reference clock pins, can also be used as general purpose IO interfaces and need to be connected with 32.768KHz crystals when they are used as clock pins.

2.4. Debug pins

- PIN5(PA4/SWDCLK) and PIN6(PA5/SWDIO) are SWD pins and can also be used as general purpose IO interfaces. When they are used as SWD pins, they can be used to download applications. PIN5(PA4/SWDCLK) needs to be connected to 10K pull-down resistor and PIN6(PA5/SWDIO) to 10K pull-up resistor.
- PIN16(PB6/TX) and PIN17(PB7/RX) are Uart serial port pins, and can also be used as general purpose IO interfaces. They can be used for print when being used as serial port pins.

2.5. AMIC audio pins

- PIN20(PB11/AMIC_N) and PIN21(PB13/AMIC_P) are MIC input pins supporting single-ended input and

differential input with adjustable gain.

- PIN19(PB12/AMIC_BIAS) is the pin for outputting MIC bias voltage, it outputs adjustable MICBIAS voltage with a range of 1.6~2.3V and a typical voltage of 2V.

2.6. IO interface

- For the specific definition of IO interface, see *N32WB03x Datasheet*

3. Design specifications on PCB Layout

3.1. Requirements for RFIOP wiring design

- In order to ensure minimum loss, RF routing should be as short as possible, components should be as compact as possible, and RF routing should be as straight as possible and should not be right angle with the routing width and the space between the route and the peripheral GND equivalent to the recommended value 0.5mm. As PCB material and medium influence the RF routing impedance, the routing width and the space between the route and the peripheral GND can be adjusted properly.
- The wires around RF must be enclosed by the earthing system, with the upper system connecting to the lower layer via GND holes, Try not to route other wires under the RF routing, or there is a GND layer in the middle..
- The zone around antenna front and back must be separated from other routes, to ensure the space between GND and the antenna is 3mm or above and no metal component is in the space.
- Normally, the antenna length is about 30mm, equivalent to 1/4 of the Bluetooth signal wavelength.
- In order to enhance ESD protection capacity, be sure to coat the antenna surface with a solder mask rather than exposing it to the outside.
- Considering that the ESD in the production line of the PCB is not well controlled during the production period, it is suggested to add a TVS tube to the antenna port for protection. The position of the TVS tube resistance is shown in the figure below.

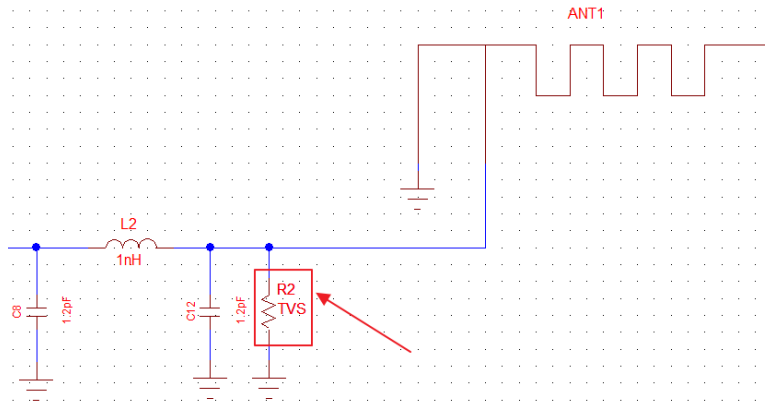


Fig. 3-1 Reference Schematic Diagram for TVS

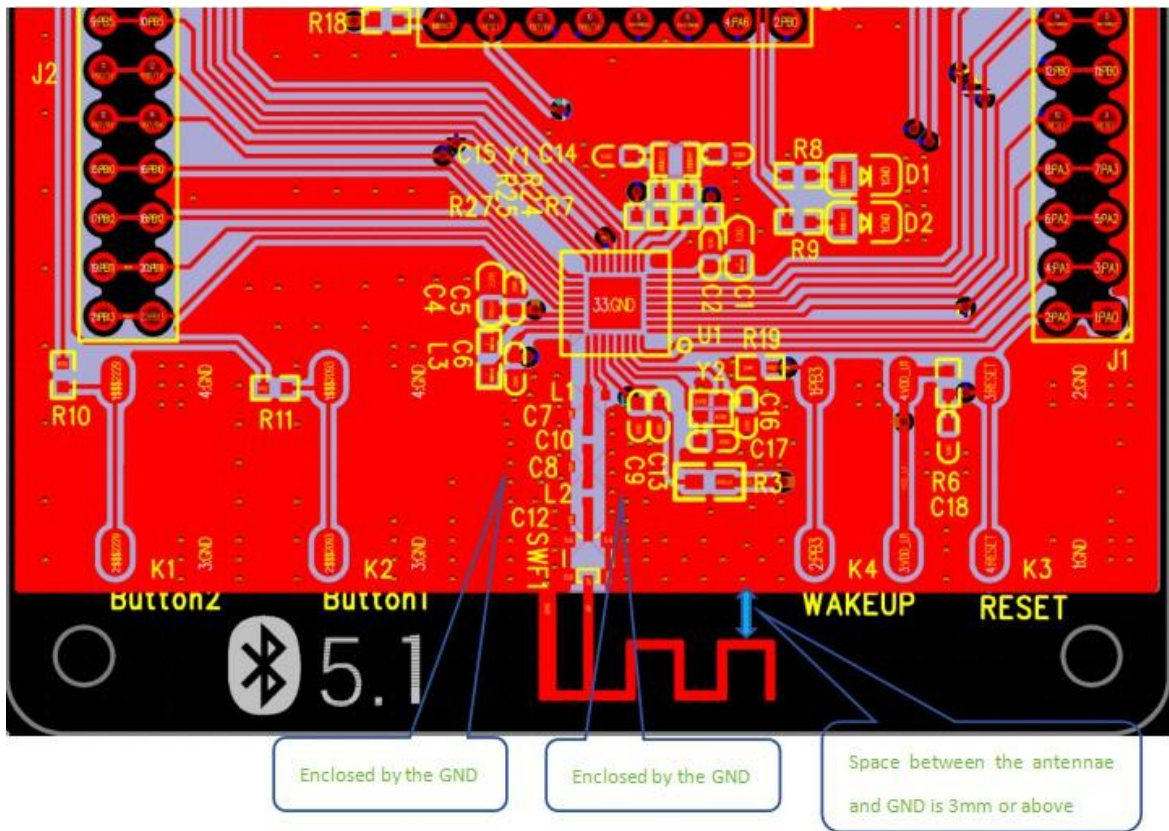
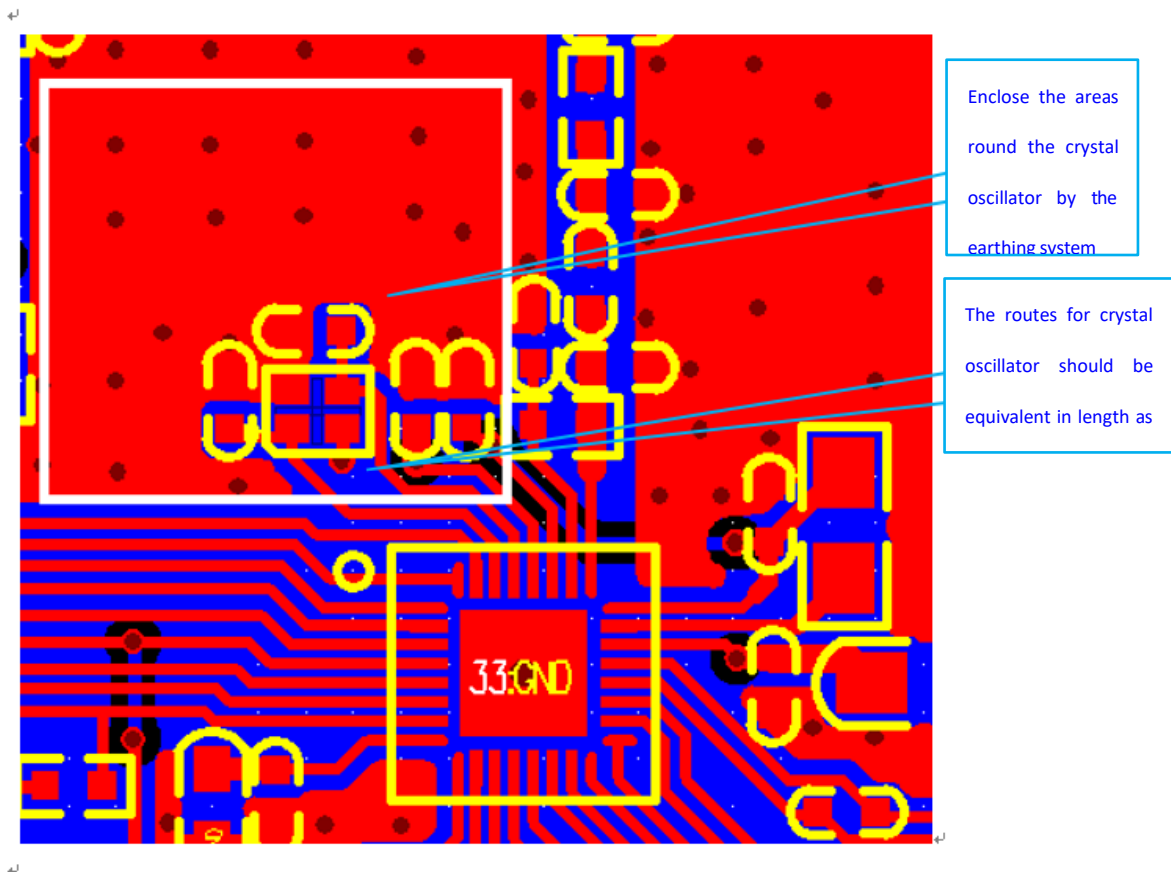


Fig. 3-2 Routing Layout for RF Antennae

3.2. Requirements for routing of 32MHz crystal oscillator

- The two crystal oscillator routes should be as short as possible and as equivalent in length as possible, with the areas around them enclosed by the earthing system, the crystal GND and the Chip GND should be as close as possible..
- Try not to route wires under the crystal oscillator, especially the VDCDCRF wires cannot be routed from below, as the DC voltage generated by Bluetooth broadcast affects the stability of the crystal oscillator frequency. Moreover, do not route large-current power wires, High-speed communication wires or other wires that may interfere with the clock signal around the crystal.



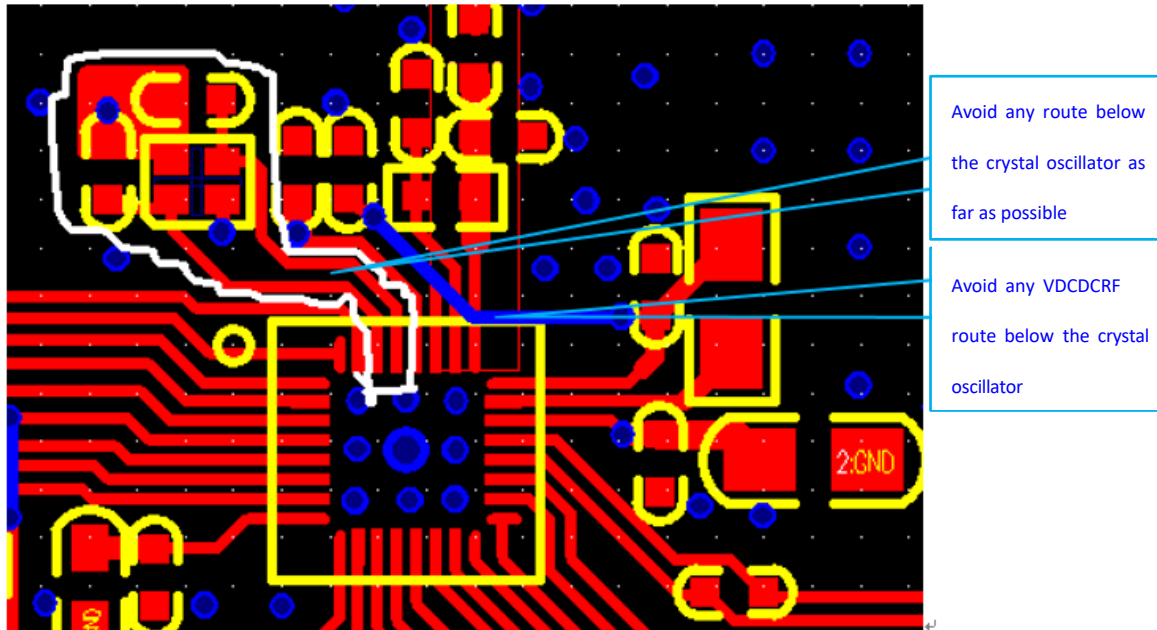


Fig. 3-3 Layout of 32MHz Crystal Oscillator

3.3. Requirements for routing of chip grounding

- The 32 pins of this chip do not have GND, and its GND is at the bottom of the chip.
- The chip packaging center is required to be cladded by a square copper sheet. The space between the copper sheet and the chip pin should be $\geq 0.3\text{mm}$ and $\leq 0.5\text{mm}$, connect the copper sheet with GND via **9 holes**. The center hole may be 0.6mm/0.4mm and the holes around may be 0.5mm/0.3mm. The holes should not be too large to avoid tin leaking and consequent insufficient solder.

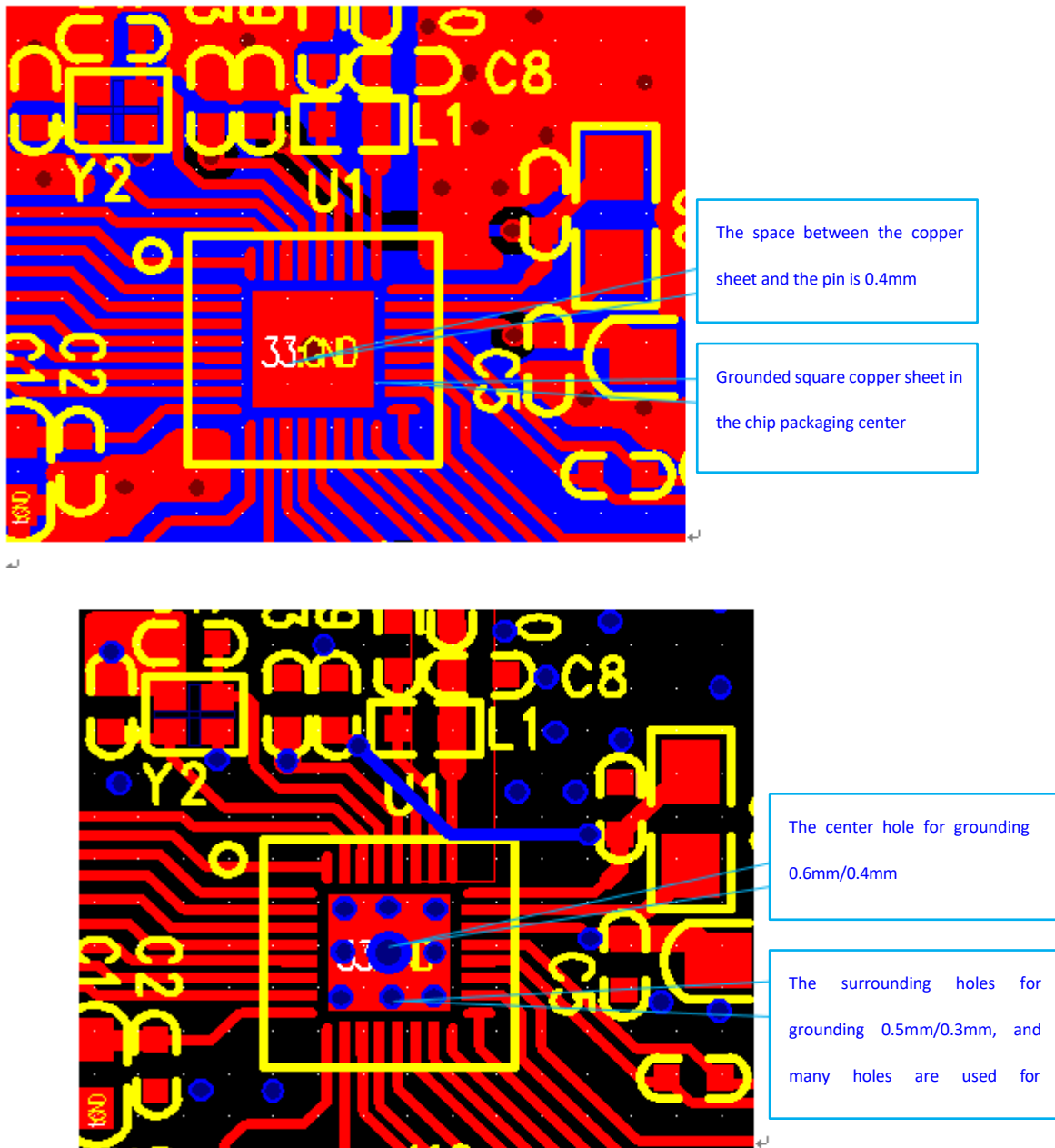


Fig. 3-4 Layout of Chip Ground Routing

3.4. Requirements for power supply routing

- The power supply wire for the chip should be as thick and short as possible, with the filter capacitor as close as possible to the chip.
- If two filter capacitors with difference capacity are used, the smaller one should be

closer to the chip than the larger one.

- The GND of the power decoupling capacitor should be as close as possible to the chip GND.

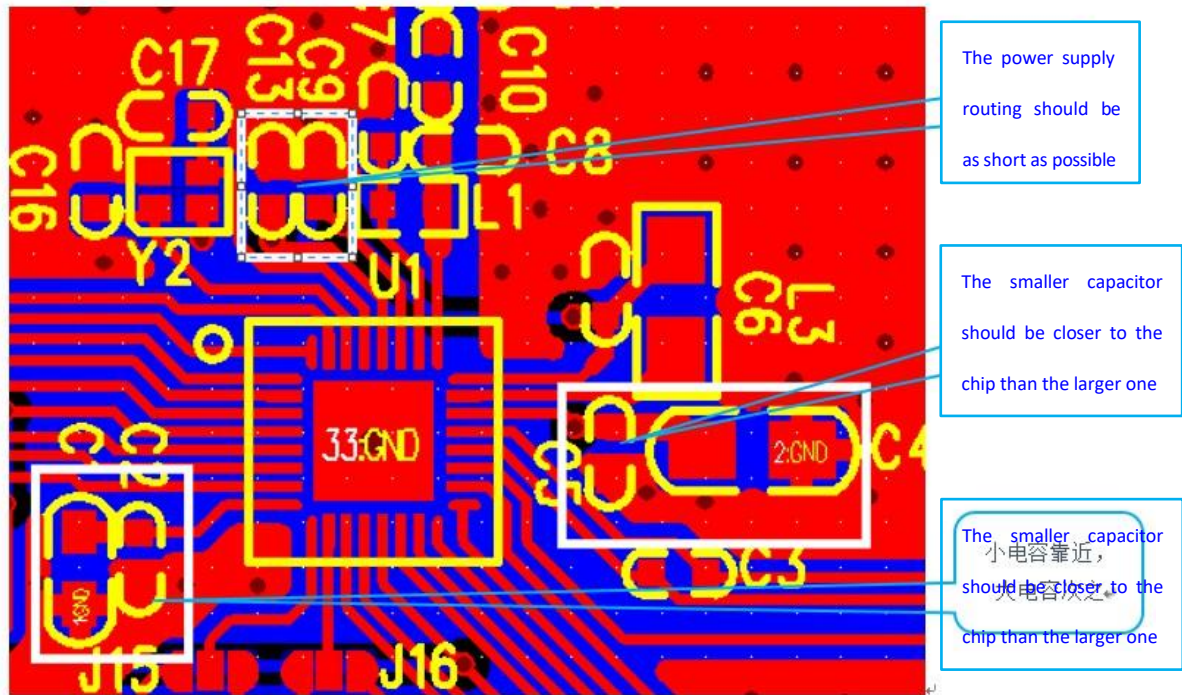


Fig. 3-5 Layout of Power Supply Routing

3.5. Requirements for AMIC audio routing

- PB11/AMIC_N and PB13/AMIC_P support single-ended input and differential input, and their routes should be differential type. The differential wires should be as short and equivalent in spacing as possible, with proper shielding by ground wire for avoiding other signal interference.
- The inside of their audio module should be grounded first and then they are connected with the peripheral ground to avoid the interference from ground wire.

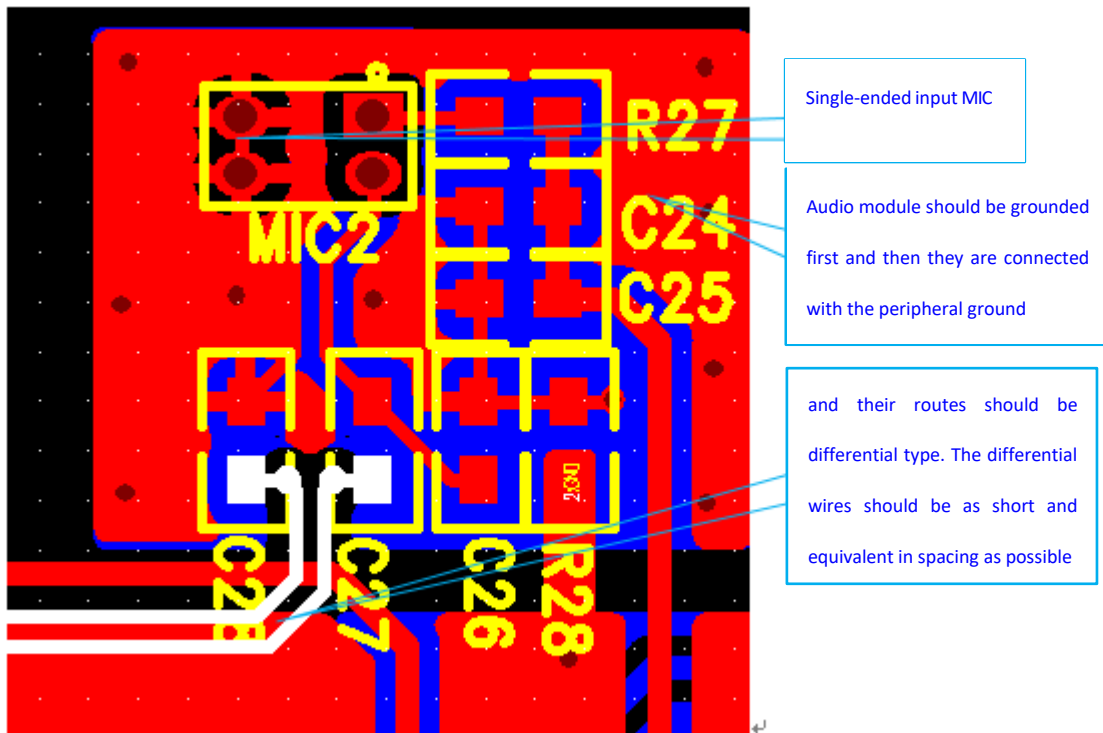
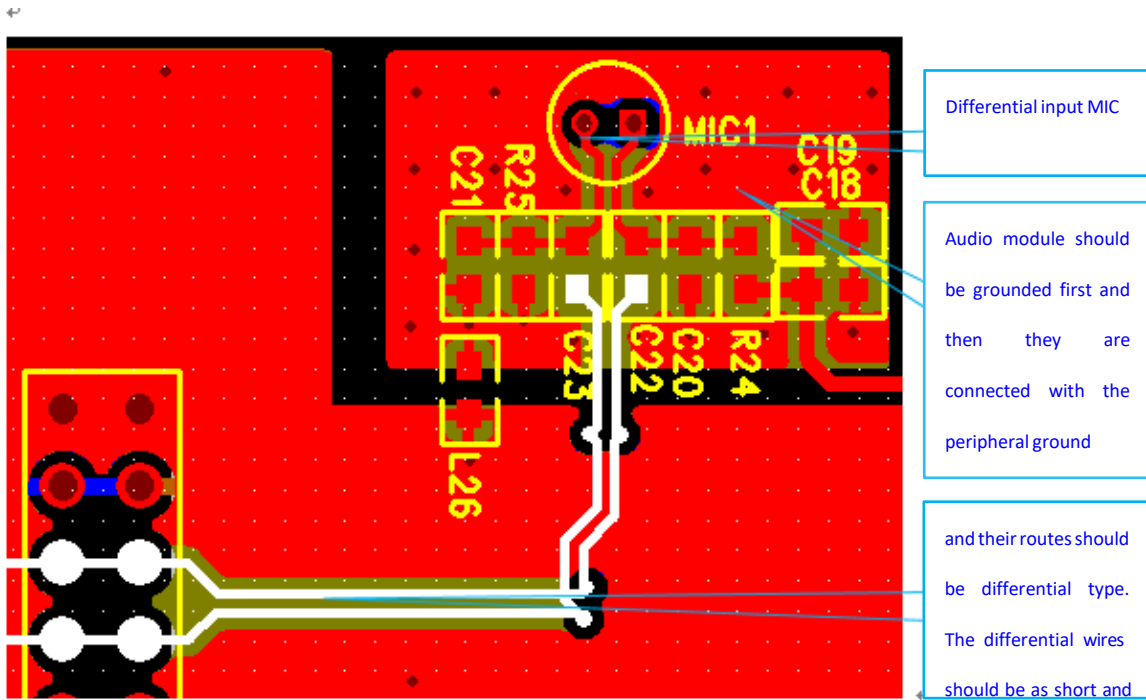


Fig. 3-6 Audio Routing Layout

4. Version history

Date	Version	Modifications
2022/9/27	V1.3	Initial version
2025/8/28	V1.4	<ol style="list-style-type: none">Chapter 1.1 add the VCCRF description of the resistance R3 in EVB.Chapter 1.3,1.4 update the Reference Schematic Diagram.Remove chapter 1.10 , the rf schematic design for conduction/radiation certification test can refer to the EVB.Chapter 2.1 adds a selection guide for DCDC power inductors.Chapter 3.1 add the wire routine description around the RF wire, update the ESD protection description,remove the 0 ohm solution, and update the Fig. 3-2.Chapter 3.2 add the routing requirement of crystal GND and around the crystal.Chapter 3.4 add the routing requirement of the GND of power decoupling capacitor

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